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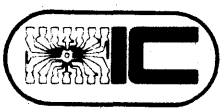
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MANUFACTURER & DISTRIBUTOR DIRECTORY Locate the nearest local source for additional information or quick delivery of needed products. A fingertip communications guide listing the location and phone number for all manufacturer's field sales offices, reps, and distributors, both domestic and international.

PRODUCT INDEX Arranges 84 IC manufacturers in alphabetical order by manufacturer and provides a complete alphanumeric listing of each company's IC standard product line. Adjacent page number references are provided for instant referral to needed technical information.

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DIGITAL
- CMOS
- ECL
- HNIL/HTL
- TTL
- Special

INTERFACE
- Analog Switches
- A/D Converters
- Binary Decimal
- D/A Converters
- Display Drivers
- Error Checking Circuits
- Keyboard Encoders
- Line Drivers, Receivers and Transceivers
- Memory and Peripheral Drivers
- Sense Amplifiers
- Serial Transmitters-Receivers

LINEAR
- Amplifiers, Special Purpose
- Arrays
- Comparators
- Consumer Circuits
- Followers
- Operational Amplifiers
- Phase Locked Loop Circuits
- Telecommunication Circuits
- Timers
- Voltage Regulators
- Other Linear Devices

MEMORY
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- Code Converters
- EAROMs
- FIFOs, LIFOs, PLAS
- PROMs
- RAMs
- ROMs
- Shift Registers

MICROPROCESSORS
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- Development Systems
- Selection Table
  - General Structure
  - Architecture
  - Hardware Support
  - Software Support
  - Alternate Sources

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PART NUMBER INDEX

This index shows the page and line on that page where each device appears in the Master Selection Guide, and application notes are indicated by a ¶ sign. The list is prepared by a computer from the data in these sections so every device in them is listed. The devices are arranged in order by basic numbers so similarly numbered devices from various manufacturers are grouped together. Bold faced listings lead to the data supplied by the manufacturers. Use this index to locate key operational characteristics, application notes, and devices data whenever you have a model number.

how to use the part number index

This Part Number Index is arranged in alpha-numeric sequence, ignoring the manufacturer's prefixes and suffixes and using the basic model numbers. This basic number sequence is sorted by reading the digits from **left** to **right**, assuming that letters come before numbers. (As an example, these numbers would appear in the following order: 5301, 531, 54H01, 54139, 5414.) Under each basic number, the manufacturer's name and full model number is listed. The page references in **BOLD FACE** lead to manufacturers' data and application notes are indicated by a ¶ sign.

The arrangement of this index by base number gives you several advantages. It allows you to find a device by its basic number whether or not you know the name of the manufacturer or the manufacturer's prefixes. Also it groups similar devices together so that when you are looking for data you can quickly determine if the data has been provided in the book by any of the manufacturers and where that data is. Similarly it groups any references to application notes close together so that you do not need to guess which manufacturer might publish application notes on a device before you can locate them.

Once you become familiar with the alpha-numeric numbering sequence, you'll find that this index is very easy to use.

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		MAT-01A	★ **887**
			547-27
			547-42
		MAT-01F	★ **887**
			547-28
			547-43
		MAT-01G	★ **887**
			547-29
			547-44
		MAT-01H	★ **887**
		OP-01	★ **837**
			571-19
		OP-01C	★ **837**
			580-10
		OP-01E	★ **837**
			574-34
		OP-01F	★ **837**
			574-35
		OP-01G	★ **837**
			580-11
		OP-01H	★ **837**
			571-20
		REF-01	★ **890**
			★ **894**
			614-163
			¶ 126-15
		REF-01A	★ **890**
			★ **894**
			614-165
		REF-01C	★ **890**
			614-166
		REF-01D	★ **890**
			614-167
		REF-01E	★ **890**
			614-168
		REF-01H	★ **890**

Arranged alphanumerically from left to right.

IC MASTER

Base Number	Source	Device	Page-Line
01	PMI	REF-01H	614-169
010	Harris	HM010	258-115
	Solitron	CJSE010	607-108
0103	TI	TBM0103	1010-32
			1029-76
0104	Harris	HM0104	258-132
0107	Hughes	HCTR0107	258-66
011	Sanyo	STK011	555-35
	Solitron	CJSE011	604-116
0110	Harris	HM0110	258-126
012	Harris	HM012	258-116
	Solitron	CJSE012	607-109
0126	National	AH0126	311-113
		AH0126C	311-114
0129	National	AH0129	311-81
		AH0129C	311-82
013	Fairchild	SH013C	343-30
		SH013M	343-31
	Harris	HM013	258-117
	Solitron	CJSE013	604-117
0133	National	AH0133	307-86
		AH0133C	307-87
0134	National	AH0134	308-11
		AH0134C	308-12
0139	National	AH0139	312-43
		AH0139C	312-44
014	Solitron	CJSE014	607-110
0140	National	AH0140	311-59
		AH0140C	311-60
0141	National	AH0141	307-61
		AH0141C	307-62
0142	National	AH0142	312-54
		AH0142C	312-55
0143	National	AH0143	309-110
		AH0143C	309-111
0144	National	AH0144	309-76
		AH0144C	309-77
0145	National	AH0145	312-30
		AH0145C	312-31
0146	National	AH0146	309-54
		AH0146C	309-55
015	Sanyo	STK015	555-62
0151	National	AH0151	307-69
		AH0151C	307-70
0152	National	AH0152	307-97
		AH0152C	307-98
0153	National	AH0153	311-68
		AH0153C	311-69
0154	National	AH0154	311-90
		AH0154C	311-91
016	Sanyo	STK016	555-63
0161	National	AH0161	309-63
		AH0161C	309-64
0162	National	AH0162	309-85
		AH0162C	309-86
0163	National	AH0163	312-34
		AH0163C	312-35
0164	National	AH0164	312-48
		AH0164C	312-49
0165	Harris	HD0165	★ 453
			329-9
			¶ 106-15
0168	Harris	HM0168	258-137
017	Solitron	CJSE017	602-54
018	Solitron	CJSE018	606-67
0186	Harris	HM0186	258-142
	National	ADC0186	317-108
019	Solitron	CJSE019	602-55
0190	Hughes	HMUX0190	326-21
02	PMI	CMP-02	★ 906
			549-1
			¶ 138-7
		CMP-02C	★ 906
			549-26
		CMP-02E	★ 906
			549-2
		DAC-02	★ 913
		DAC-02AC	★ 913
			322-53
		DAC-02BC	★ 913
			322-54
		DAC-02CC	★ 913
			322-57
		DAC-02DD	★ 913
			322-61
		OP-02	★ 839

Base Number	Source	Device	Page-Line
02	PMI	OP-02	564-31
			574-36
		OP-02A	★ 839
			571-11
		OP-02C	★ 839
			574-37
		OP-02E	★ 839
			571-12
		REF-02	★ 894
			614-118
			615-131
			¶ 138-7
			¶ 138-8
		REF-02A	★ 894
			614-119
			615-132
		REF-02C	★ 894
			614-120
			615-133
		REF-02D	★ 894
			614-121
			615-134
		REF-02E	★ 894
			614-122
			615-135
		REF-02H	★ 894
			614-123
			615-136
020	Sanyo	STK020	555-64
	Solitron	CJSE020	606-68
0200	Hughes	HCTR0200	206-196
021	Solitron	CJSE021	602-56
022	Sanyo	STK022	555-65
	TI	TL022C	590-2
		TL022M	589-46
024	Sanyo	STK024	555-66
025	Sanyo	STK025G	555-67
	SGS	L025	612-114
03	PMI	DAC-03	★ 911
			★ 913
		DAC-03AD	★ 645
			★ 913
		DAC-03BD	★ 645
			★ 913
			321-80
		DAC-03CD	★ 911
			★ 913
			321-82
		DAC-03DD	★ 645
			★ 913
			321-84
030	DDC	ADH-030-10	324-17
		ADH-030-11	324-16
		ADH-030-12	324-15
		ADH-030-8	324-18
	Harris	HM030	258-134
0301	Signetics	TDA0301	584-20
031	Harris	HM031	258-135
	Sanyo	STK031	555-68
0319	Signetics	TDA0319	552-24
032	Sanyo	STK032	555-69
0320	Hughes	HCTR0320	596-83
0321	Hughes	HSSR0321	214-135
			1028-32
0323	Fairchild	SH0323	601-117
0324	Signetics	TDA0324	595-8
034	Harris	HM034	258-136
0347	Hughes	HCTR0347	596-86
035	Sanyo	STK035	555-71
0351	Hughes	HSSR0351	214-136
			1028-33
0356	Signetics	TDA0356	591-39
036	Sanyo	STK036	555-72
036T1	SGS	L036T1	603-45
037T1	SGS	L037T1	603-101
04	PMI	DAC-04	★ 916
		DAC-04AC	★ 916
			322-42
		DAC-04BC	★ 916
			322-43
		DAC-04CC	★ 916
			322-46
		DAC-04DD	★ 916
			322-51
		OP-04	★ 844

Base Number	Source	Device	Page-Line
04	PMI	OP-04	588-51
		OP-04A	★ 844
			588-34
		OP-04C	★ 844
			588-52
		OP-04E	★ 844
			588-35
040	Harris	HM040	258-139
	Sanyo	STK040A	555-110
0400	TI	SBP0400	¶ 152-14
		SBP0400A	1532-1
		SBP0400AC	1505-105
		SBP0400AM	1505-106
0401	TI	SBP0401A	1532-1
		SBP0401AC	1505-107
		SBP0401AM	1505-108
041	Harris	HM041	258-140
	Sanyo	STK041	555-111
	Siemens	S041	557-105
042	Siemens	S042	545-136
			612-115
043	Sanyo	STK043	555-112
044	Harris	HM044	258-141
	TI	TL044C	593-40
		TL044M	593-22
045	SGS	L045	586-21
0464	Motorola	MCM0464	1010-46
0470	ITT	TDA0470	558-146
05	PMI	DAC-05	★ 913
		DAC-05A	★ 913
			322-55
		DAC-05B	★ 913
			322-58
		DAC-05C	★ 913
			322-62
		DAC-05E	★ 913
			322-56
		DAC-05F	★ 913
			322-59
		DAC-05G	★ 913
			322-65
		OP-05	★ 849
			566-76
			570-55
			¶ 116-14
			¶ 116-15
		OP-05A	566-51
			569-42
		OP-05C	566-87
			572-23
		OP-05E	566-56
			570-56
	Rockwell	A05XX	1505-97
050	DDC	ADH-050	615-168
	Harris	HM050	258-128
	Sanyo	STK050	555-73
051	DDC	ADH-051	615-169
	Harris	HM051	258-129
0512	Harris	HPROM0512-2	1003-50
		HPROM0512-5	1003-51
054	SGS	M054	560-203
055	Harris	HM055	258-130
	Sanyo	STK055	555-74
	SGS	M055	560-204
0555	Signetics	TDA0555	600-22
057	Sanyo	STK057	555-75
058	Sanyo	STK058	555-76
06	PMI	DAC-06	★ 916
		DAC-06A	★ 916
			322-44
		DAC-06B	★ 916
			322-47
		DAC-06C	★ 916
			322-49
		DAC-06E	★ 916
			322-45
		DAC-06F	★ 916
			322-48
		DAC-06G	★ 916
			322-50
060	Sanyo	STK060	555-77
	Sprague	060	¶ 132-13
061	TI	TL061	★ 985
			566-132
		TL061AC	★ 985
			582-13

Base Number	Source	Device	Page-Line
061	TI	TL061AM	★ 985
			576-35
		TL061BC	★ 985
			576-36
		TL061C	★ 985
			587-2
		TL061M	★ 985
			582-14
062	Sanyo	STK062	555-78
	TI	TL062	★ 985
		TL062AC	★ 985
			590-37
		TL062AM	★ 985
			589-16
		TL062BC	★ 985
		TL062C	★ 985
			591-55
		TL062M	★ 985
			590-38
064	TI	TL064	★ 985
		TL064AC	★ 985
		TL064AM	★ 985
			592-43
		TL064BC	★ 985
		TL064C	★ 985
			594-6
			595-33
		TL064M	★ 985
			594-7
066	TI	TL066	★ 985
			567-28
		TL066AC	★ 985
			582-15
		TL066AM	★ 985
			576-37
		TL066BC	★ 985
			576-38
		TL066C	★ 985
			587-3
		TL066M	★ 985
			582-16
07	PMI	OP-07	★ 853
			566-82
			569-22
			¶ 116-16
			¶ 116-17
		OP-07A	★ 853
			566-57
			569-8
		OP-07C	★ 853
			566-92
			569-44
		OP-07D	★ 853
			569-45
		OP-07E	★ 853
			566-83
			569-26
	Rockwell	A07XX	1505-37
070	Sanyo	STK070	555-79
071	TI	TL071	★ 988
		TL071AC	★ 988
			582-11
		TL071AM	★ 988
			576-25
		TL071BC	★ 988
			576-26
		TL071C	★ 988
			585-45
		TL071M	★ 988
			582-12
072	TI	TL072	★ 988
		TL072AC	★ 988
			590-35
		TL072AM	★ 988
			589-14
		TL072BC	★ 988
			589-15
			589-17
		TL072C	★ 988
			591-49
		TL072M	★ 988
			590-36
0723	Signetics	TDA0723	609-62
074	Harris	HM074	258-111
	TI	TL074	★ 988
		TL074AC	★ 988

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★ indicates additional data is provided on the page noted.

Base Number	Source	Device	Page-Line
074	TI	TL074AC	594-2
		TL074AM	★ **988**
		TL074BC	★ **988**
			★ **991**
		TL074C	★ **988**
			595-15
		TL074M	★ **988**
			594-3
0741	Signetics	TDA0741	564-39
			583-17
0748	Signetics	TDA0748	582-54
075	Harris	HM075	258-112
	Sanyo	STK075	555-80
	TI	**TL075**	★ **988**
		TL075AC	★ **988**
			594-4
		TL075BC	★ **988**
		TL075C	★ **988**
			595-16
		TL075M	594-5
076	Harris	HM076	258-113
077	Sanyo	STK077	555-81
078	Sanyo	STK078	555-82
08	AMD	DAC-08	321-7
		DAC-08A	321-1
		DAC-08C	321-19
		DAC-08E	321-12
	Datel	DAC-08BC	321-13
		DAC-08BM	321-14
	National	**DAC-08**	★ **919**
	NEC America	DAC-08C	321-22
	PMI	**DAC-08**	★ **919**
			321-10
			¶ 116-14
			¶ 116-18
			¶ 126-7
			¶ 126-11
			¶ 126-12
			¶ 126-13
			¶ 126-15
			¶ 126-16
		DAC-08A	★ **919**
			321-3
		DAC-08C	★ **919**
			321-23
		DAC-08E	★ **919**
			321-17
		DAC-08H	★ **919**
			321-4
		MUX-08	★ **958**
		MUX-08A	★ **958**
			315-19
		MUX-08AQ	★ **958**
		MUX-08B	★ **958**
			315-29
		MUX-08BQ	★ **958**
		MUX-08E	★ **958**
			315-20
		MUX-08EQ	★ **958**
		MUX-08F	★ **958**
			315-30
		MUX-08FQ	★ **958**
		OP-08	★ **858**
			566-148
		OP-08A	★ **858**
			569-40
		OP-08B	★ **858**
			570-7
		OP-08C	★ **858**
			572-7
		OP-08E	★ **858**
			569-41
		OP-08F	★ **858**
			570-8
		OP-08G	★ **858**
			572-8
	Rockwell	A08XX	1505-38
080	Harris	HM080	258-119
	Sanyo	STK080	555-83
	TI	**TL080**	★ **991**
			¶ 117-9
		TL080AC	★ **991**
			582-20
		TL080AM	★ **991**
		TL080BC	★ **991**
			576-41

Base Number	Source	Device	Page-Line
080	**TI**	**TL080C**	★ **991**
			587-6
		TL080M	★ **991**
			582-21
0800	National	ADC0800	317-31
			¶ 126-2
		ADC0800C	317-30
		DAC-0800LC	321-16
		DAC0800L	321-9
	Telefunken	TBA0800	554-187
0801	Fairchild	μA0801AM	321-2
		μA0801CC	321-20
		μA0801E	321-15
		μA0801M	321-8
		FCB0801	556-111
	National	DAC0801LC	321-21
0802	Fairchild	μA0802AC	320-61
		μA0802AM	320-62
		μA0802BC	320-38
		μA0802CC	320-14
0806	National	DAC0806LC	320-16
0807	National	DAC0807LC	320-40
0808	National	DAC0808L	320-67
		DAC0808LC	320-68
081	Harris	HM081	258-120
	NEC America	μPCF081	582-17
			587-4
	SGS	M081	558-141
	TI	**TL081**	★ **991**
			564-93
			¶ 117-9
		TL081AC	★ **991**
			582-18
		TL081AM	★ **991**
			576-39
		TL081BC	★ **991**
			576-40
		TL081C	★ **991**
			587-5
		TL081M	★ **991**
			582-19
0816	National	ADC0816	612-173
0817	National	ADC0817	317-110
			612-174
082	Sanyo	STK082	555-84
	SGS	M082	558-142
	TI	**TL082**	★ **991**
			¶ 117-9
		TL082AC	★ **991**
			590-39
		TL082AM	★ **991**
			589-18
		TL082BC	589-19
		TL082C	★ **991**
			591-56
		TL082M	★ **680**
			590-40
083	**TI**	**TL083**	★ **991**
			¶ 117-9
		TL083AC	★ **991**
			590-41
		TL083C	★ **991**
			591-57
		TL083M	★ **991**
			590-42
084	Harris	HM084	258-121
	Sanyo	STK084	555-85
	TI	**TL084**	★ **991**
			¶ 117-9
		TL084AC	594-8
		TL084AM	★ **991**
			592-45
		TL084C	★ **991**
			595-34
		TL084M	★ **991**
			594-9
086	Sanyo	STK086	555-86
087	SGS	M087	558-143
089	TI	TL089C	569-35
		TL089I	569-14
09	**PMI**	**OP-09**	★ **864**
		OP-09A	★ **864**
			592-25
		OP-09B	★ **864**
			592-34
		OP-09E	★ **864**

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09	PMI	OP-09E	592-26
		OP-09F	★ **864**
			592-35
090	Harris	HM090	258-123
091	Harris	HM091	258-124
093	Harris	HM093	258-125
1	**Datel**	**SHM-IC-1**	★ **393**
			615-38
		SHM-IC-1M	★ **393**
			615-39
		VFQ-1	613-25
			616-2
	GI	AY1-0212	558-183
		AY1-0212A	558-184
		AY1-1006	558-115
		AY1-1007B	558-126
		AY1-1313	558-155
		AY1-1320	558-84
		AY1-2006	558-116
		AY1-5050	558-127
		AY1-5051	558-108
		AY1-6721/5	558-110
		AY1-6721/6	558-117
		AY1-8622	557-34
1.5	Teledyne C	CDA1-3	310-19
1PD407	ITT	ZTE1.5	614-187
10	NEC America	μPD4071	210-158
	Burr-Brown	MP10	321-57
			1513-26
	Datel	ADC-EK10B	318-1
		DAC-HA10B	321-116
		DAC-HA10BM	321-117
		DAC-HF10B	321-119
		DAC-IC10B	321-68
	DDC	HRDC-10	615-5
		HSDC-10	615-10
		HXDC-10	615-15
		SDAC-10	324-47
	PMI	**DAC-10**	★ **929**
		DAC-10A	★ **929**
			321-100
		DAC-10B	★ **929**
			321-101
		DAC-10E	★ **929**
			321-102
		DAC-10F	★ **929**
			321-103
		OP-10	★ **857**
			566-78
			588-28
			¶ 112-1
			¶ 129-1
		OP-10A	566-79
			588-29
		OP-10C	566-90
			588-38
		OP-10E	566-80
			588-30
	Teledyne C	CAG10	307-10
		CAG10A	307-5
		CAG10B	307-13
		CAG10C	307-7
		CAG10D	307-9
100	**AMI**	**MDC-100**	★**1540**
			1509-155
		TCK-100	★ **352**
	Ferranti	ZNP100	613-142
	Intersil	100	609-29
	Micro Comp	MCC100	556-90
	National	AF100	612-25
		LM100	609-31
			¶ 133-11
			¶ 133-12
			¶ 133-14
			¶ 134-10
	PMI	**DAC-100**	★ **950**
			¶ 126-8
			¶ 126-9
			¶ 126-10
		DAC-100A	★ **950**
			321-90
			321-91
		DAC-100B	★ **950**
			321-92
			321-93
		DAC-100C	★ **950**

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100	PMI	DAC-100C	320-108
			320-109
		DAC-100D	★ **950**
			320-110
			320-111
	Reticon	SAD100	615-84
	Signetics	ST100	598-41
	Silicon G	SG100	609-35
	Siliconix	T100	545-165
100X100	Reticon	RA100X100	613-102
1000	GI	LP1000	1509-178
	Lambda	LAS1000	609-110
	National	AM1000	312-79
			¶ 135-11
	TI	TMS1000	1506-21
			1533-1
			¶ 152-14
10000	Fairchild	F10000	1026-54
		F10000C	218-119
		F10000M	218-121
1001	GI	T1001	561-133
	MOS	MTS1001	1024-21
	National	AM1001	312-80
			¶ 135-11
	Panasonic	MN1001	1009-86
		MN1001-1	1009-39
		MN1001-2	1008-113
	Plessey	SL1001	598-7
		SL1001A	612-108
		SL1001B	612-109
	TRW	TDC1001J	317-10
10010	Fairchild	F10010C	216-67
		F10010M	216-68
100101	Fairchild	F100101	219-117
100102	Fairchild	F100102	219-119
100107	Fairchild	F100107	219-115
100112	Fairchild	F100112	219-103
100114	Fairchild	F100114	220-9
100117	Fairchild	F100117	219-111
100118	Fairchild	F100118	219-113
100123	Fairchild	F100123	219-105
100130	Fairchild	F100130	219-121
100131	Fairchild	F100131	219-107
100136	Fairchild	F100136	219-99
10014	Fairchild	F10014C	219-46
		F10014M	219-47
100141	Fairchild	F100141	220-3
100142	Fairchild	100142	219-125
100145	Fairchild	F100145	219-127
100150	Fairchild	F100150	219-123
100151	Fairchild	F100151	219-109
100155	Fairchild	F100155	220-1
100158	Fairchild	F100158	220-5
10016	Fairchild	F10016C	216-48
		F10016M	216-49
100160	Fairchild	F100160	220-13
100163	Fairchild	F100163	219-131
100164	Fairchild	F100164	219-133
100165	Fairchild	F100165	220-15
100166	Fairchild	F100166	219-97
100170	Fairchild	F100170	219-101
100171	Fairchild	F100171	219-135
100179	Fairchild	F100179	219-95
100181	Fairchild	F100181	219-93
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	Signetics	54H60	254-74
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54H61	Fairchild	54H61	254-79
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54H62	Fairchild	54H62	254-87
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	Signetics	54H62	254-91
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54H71	Fairchild	54H71	234-193
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54H74	Fairchild	54H74	236-182
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54LS01	Fairchild	54LS01	242-66
	National	DM54LS01	242-75
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54LS02	Fairchild	54LS02	245-146
	Motorola	SN54LS02	245-152
	National	DM54LS02	245-154
	Raytheon	54LS02	245-159
	Signetics	54LS02	245-165
	TI	SN54LS02	245-169
54LS03	Fairchild	54LS03	242-68
	Motorola	SN54LS03	242-73
	National	DM54LS03	242-77
	Raytheon	54LS03	242-86
	Signetics	54LS03	242-90
	TI	SN54LS03	242-94
54LS04	Fairchild	54LS04	226-19
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	National	DM54LS04	226-24
	Raytheon	54LS04	226-29
	Signetics	54LS04	226-31
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54LS05	Fairchild	54LS05	226-95
	Motorola	SN54LS05	226-98
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	Signetics	54LS05	226-107
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	Signetics	54LS08	239-44
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	Raytheon	54LS09	239-95
	Signetics	54LS09	239-97
	TI	SN54LS09	239-99
54LS10	Fairchild	54LS10	241-30
	Motorola	SN54LS10	241-33
	National	DM54LS10	241-35
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	Signetics	54LS10	241-42
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	Signetics	54LS107	236-58
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	Motorola	SN54LS109	235-77
	National	DM54LS109	235-79
	Raytheon	54LS109	235-84
	Signetics	54LS109	235-86
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54LS11	Fairchild	54LS11	238-126
	Motorola	SN54LS11	238-129
	National	DM54LS11	238-132
	Raytheon	54LS11	238-137
	Signetics	54LS11	238-139
	TI	SN54LS11	238-141
54LS112	Fairchild	54LS112	235-157
	National	DM54LS112	235-160
	Raytheon	54LS112	235-165
	Signetics	54LS112	235-167
	TI	SN54LS112A	235-169
54LS113	Fairchild	54LS113	235-96
	National	DM54LS113	235-99
	Raytheon	54LS113	235-104
	Signetics	54LS113	235-106
	TI	SN54LS113A	235-108
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	Motorola	SN54LS114	235-130
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54LS12	Fairchild	54LS12	241-88
	National	DM54LS12	241-90
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54LS123	AMD	SN54LS123	251-63
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	Raytheon	54LS125	225-82
	Signetics	54LS125	225-84
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54LS126	Fairchild	54LS126	225-105
	Motorola	SN54LS126	225-108
	National	DM54LS126	225-110
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	Motorola	SN54LS138	232-192
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	National	DM54LS139	232-150
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	Signetics	54LS139	232-159
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	Motorola	SN54LS14	255-193
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54LS147	TI	SN54LS147	254-184
54LS148	AMD	SN54LS148	254-166
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	Signetics	54LS154	233-81
54LS155	Fairchild	54LS155	232-79
	Motorola	SN54LS155	232-82
	National	DM54LS155	232-84
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	Motorola	SN54LS160	229-155
	National	DM54LS160	229-157
	Raytheon	54LS160	229-163
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	Signetics	54LS161	228-37
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	Motorola	SN54LS162	229-204
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	National	DM54LS258	248-91
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54LS353	Fairchild	54LS353	249-97
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54LS362	TI	SN54LS362	1512-129
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	Raytheon	**54LS366**	★ **286**
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	Motorola	SN54LS367	225-148
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	Motorola	SN54LS368	226-166
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	Signetics	54S03	242-120
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54S09	Fairchild	54S09	239-103
	Signetics	54S09	239-105
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54S10	Fairchild	54S10	241-63
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54S197	TI	SN54S197	227-123
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	Signetics	54S20	240-70
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54S258	AMD	SN54S258	248-103
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54S470	National	DM54S470	1004-15
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54S471	National	DM54S471	1004-17
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54S472	**National**	**DM54S472**	★1272
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54S473	**National**	**DM54S473**	★1272
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54S571	**National**	**DM54S571**	★1266
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54S572	**National**	**DM54S572**	★1268
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	National	DM5400	241-119
	Raytheon	5400	241-123
	Signetics	5400	241-125
	TI	SN5400	241-127
5401	Fairchild	5401	242-22
	Ferranti	ZN5401	242-28
	ITT	ITT5401	242-33
	Motorola	MC5401	242-39
	National	DM5401	242-43
	Raytheon	5401	242-48
	Reticon	R5401	258-23
			612-153
	Signetics	5401	242-52
	TI	SN5401	242-56
5402	Fairchild	5402	245-119
	ITT	ITT5402	245-125
	Motorola	MC5402	245-128
	National	DM5402	245-130
		MM5402	557-8
	Signetics	5402	245-135
	TI	SN5402	245-139
5403	Fairchild	5403	242-24
	ITT	ITT5403	242-35
	Motorola	MC5403	242-41
	National	DM5403	242-45
	Raytheon	5403	242-50
	Signetics	5403	242-54
	TI	SN5403	242-58
5404	Fairchild	5404	225-186
	Ferranti	ZN5404	225-190
	ITT	ITT5404	225-194
	Motorola	MC5404	226-3
	National	DM5404	226-5
	Raytheon	5404	226-9
	Signetics	5404	226-12
	TI	SN5404	226-13
5405	Fairchild	5405	226-66
	Ferranti	ZN5405	226-71
	ITT	ITT5405	226-75
	Motorola	MC5405	226-78
	National	DM5405	226-80
		MM5405	557-9
	Raytheon	5405	226-83
	Signetics	5405	226-85
	TI	SN5405	226-89
5406	Fairchild	5406	233-153
	ITT	ITT5406	233-156
	Motorola	MC5406	233-159
	National	DM5406	233-161
	Signetics	5406	233-163
	TI	SN5406	233-165
5407	Fairchild	5407	233-115
	ITT	ITT5407	233-118
	Motorola	MC5407	233-121
	National	DM5407	233-123
	Signetics	5407	233-125
	TI	SN5407	233-127
5408	Fairchild	5408	239-10
	Ferranti	ZN5408	239-12
	ITT	ITT5408	239-15
	Motorola	MC5408	239-18
	National	DM5408	239-20
	Raytheon	5408	239-22
	Signetics	5408	239-24
	TI	SN5408	239-26
5409	Fairchild	5409	239-63
	Ferranti	ZN5409	239-65
	ITT	ITT5409	239-69
	Motorola	MC5409	239-72

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5409	National	DM5409	239-74
	Raytheon	5409	239-76
	Signetics	5409	239-78
	TI	SN5409	239-80
541	Hybrid Sys.	ADC541-8	317-84
		ADC541B-8	317-85
	Plessey	SL541	546-64
	Sanyo	STK541	603-60
	Signetics	NE541	554-114
5410	Fairchild	5410	240-202
	Ferranti	ZN5410	241-4
	ITT	ITT5410	241-8
	Motorola	MC5410	241-14
	National	DM5410	241-16
	Raytheon	5410	241-20
	Signetics	5410	241-22
	TI	SN5410	241-24
54100	Motorola	MC54100	246-72
	Signetics	54100	246-74
	TI	SN54100	246-76
54101	Mitsubishi	M54101	613-119
54104	Fairchild	54104	234-119
54105	Fairchild	54105	234-121
54107	Fairchild	54107	235-200
	Ferranti	ZN54107	236-3
	ITT	ITT54107	236-9
	Motorola	MC54107	236-16
	National	DM54107	236-20
	Signetics	54107	236-26
	TI	SN54107	236-30
54109	National	DM54109	235-64
	Signetics	54109	235-66
	TI	SN54109	235-70
5411	Fairchild	5411	238-114
	ITT	ITT5411	238-116
	National	DM5411	238-118
	Raytheon	5411	238-120
	Signetics	5411	238-122
	SSS	SCL5411	213-98
54110	TI	SN54110	234-163
54116	Fairchild	54116	246-83
	Signetics	54116	246-90
	TI	SN54116	246-95
54118	Ferranti	ZN54118	246-191
54119	Ferranti	ZN54119	246-193
5412	Fairchild	5412	241-74
	Ferranti	ZN5412	241-76
	ITT	ITT5412	241-79
	Raytheon	5412	241-81
	Signetics	5412	241-83
	TI	SN5412	241-85
54120	Motorola	MC54120	255-76
	TI	SN54120	255-78
54121	Fairchild	54121	250-120
	Ferranti	ZN54121	250-122
	ITT	ITT54121	250-126
	Motorola	MC54121	250-129
	National	DM54121	250-131
	Signetics	54121	250-134
	TI	SN54121	250-136
54122	Fairchild	54122	250-163
	Ferranti	ZN54122	250-165
	ITT	ITT54122	250-167
	Motorola	MC54122	250-170
	TI	SN54122	250-173
54123	AMD	SN54123	251-39
			¶ 110-12
	Fairchild	54123	251-41
	Ferranti	ZN54123	251-43
	ITT	ITT54123	251-46
	Motorola	MC54123	251-49
	National	DM54123	251-51
	Raytheon	54123	251-54
	Signetics	54123	251-56
	TI	SN54123	251-58
54125	Fairchild	54125	225-58
	National	DM54125	225-65
	Signetics	54125	225-67
	TI	SN54125	225-69
54126	Fairchild	54126	225-89
	National	DM54126	225-95
	Signetics	54126	225-97
	TI	SN54126	225-99
54128	Signetics	54128	334-39
	TI	SN54128	234-56
			334-40

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5413	Fairchild	5413	255-106
	Ferranti	ZN5413	255-108
	ITT	ITT5413	255-111
	Motorola	MC5413	255-114
	National	DM5413	255-116
	Signetics	5413	255-119
	TI	SN5413	255-121
54132	Fairchild	54132	255-142
	Motorola	MC54132	255-146
	National	DM54132	255-148
	Signetics	54132	255-150
	TI	SN54132	255-152
54136	Motorola	MC54136	244-142
	Raytheon	54136	244-144
	TI	SN54136	244-146
5414	Fairchild	5414	255-176
	Motorola	MC5414	255-180
	National	DM5414	255-182
	Signetics	5414	255-184
	TI	SN5414	255-186
54141	Motorola	MC54141	327-12
	National	DM54141	327-14
54143	TI	SN54143	231-70
54144	TI	SN54144	231-66
54145	Fairchild	54145	231-187
	ITT	ITT54145	231-192
	Motorola	MC54145	231-195
	National	DM54145	232-3
	Raytheon	54145	232-5
	Signetics	54145	232-7
	TI	SN54145	232-9
54147	National	DM54147	254-177
	Signetics	54147	254-180
	TI	SN54147	254-182
54148	National	DM54148	254-153
	Signetics	54148	254-156
	TI	SN54148	254-160
5415	Raytheon	5415	238-169
54150	Fairchild	54150	250-93
	Ferranti	ZN54150	250-95
	Motorola	MC54150	250-100
	National	DM54150	250-102
	Raytheon	54150	250-105
	Signetics	54150	250-107
	TI	SN54150	250-109
54151	Fairchild	54151	249-174
	Ferranti	ZN54151	249-176
	ITT	ITT54151	249-181
	Motorola	MC54151	249-184
	National	DM54151A	249-186
	Raytheon	54151	249-189
	Signetics	54151	249-191
	TI	SN54151A	249-193
54152	Fairchild	54152	249-120
	Motorola	MC54152	249-122
	Raytheon	54152	249-128
	Signetics	54152	249-130
	TI	SN54152A	249-131
54153	Fairchild	54153	248-196
	Ferranti	ZN54153	248-198
	ITT	ITT54153	249-2
	Motorola	MC54153	249-7
	National	DM54153	249-9
	Raytheon	54153	249-12
	Signetics	54153	249-14
	TI	SN54153	249-16
54154	AMD	SN54154	233-48
	Fairchild	54154	233-52
	Ferranti	ZN54154	233-54
	Motorola	MC54154	233-60
	National	DM54154	233-62
	Raytheon	54154	233-70
	Signetics	54154	233-72
	TI	SN54154	233-76
54155	Fairchild	54155	232-54
	Ferranti	ZN54155	232-56
	ITT	ITT54155	232-59
	Motorola	MC54155	232-62
	National	DM54155	232-64
	Raytheon	54155	232-67
	Signetics	54155	232-72
	TI	SN54155	232-74
54156	Fairchild	54156	232-96
	ITT	ITT54156	232-99
	Motorola	MC54156	232-102
	National	DM54156	232-104
54156	Raytheon	54156	232-107
	Signetics	54156	232-109
	TI	SN54156	232-111
54157	AMD	SN54157	247-123
	Fairchild	54157	247-128
	Ferranti	ZN54157	247-130
	ITT	ITT54157	247-135
	Motorola	MC54157	247-140
	National	DM54157	247-144
	Raytheon	54157	247-151
	Signetics	54157	247-155
	TI	SN54157	247-158
54158	Raytheon	54158	248-40
	Signetics	54158	248-42
54159	Raytheon	54159	233-85
	TI	SN54159	233-87
5416	Fairchild	5416	233-133
	ITT	ITT5416	233-136
	Motorola	MC5416	233-139
	National	DM5416	233-141
	Signetics	5416	233-145
	TI	SN5416	233-147
54160	AMD	SN54160	229-114
	Fairchild	54160	229-118
	ITT	ITT54160	229-121
	Motorola	MC54160	229-126
	National	DM54160	229-128
	Raytheon	54160	229-132
	Signetics	54160	229-136
	TI	SN54160	229-143
54161	AMD	SN54161	227-178
	Fairchild	54161	227-184
	Ferranti	ZN54161	227-186
	ITT	ITT54161	227-190
	Motorola	MC54161	227-195
	National	DM54161	227-197
	Raytheon	54161	228-7
	Signetics	54161	228-9
	TI	SN54161	228-14
54162	AMD	SN54162	229-176
	Fairchild	54162	229-178
	ITT	ITT54162	229-181
	Motorola	MC54162	229-184
	National	DM54162	229-186
	Raytheon	54162	229-188
	Signetics	54162	229-190
	TI	SN54162	229-192
54163	AMD	SN54163	227-132
	Fairchild	54163	227-134
	Ferranti	ZN54163	227-136
	ITT	ITT54163	227-139
	Motorola	MC54163	227-142
	National	DM54163	227-144
	Raytheon	54163	227-146
	Signetics	54163	227-148
	TI	SN54163	227-150
54164	AMD	SN54164	253-28
	Fairchild	54164	253-30
			1027-63
	Ferranti	ZN54164	253-32
	ITT	ITT54164	253-35
	National	DM54164	253-40
	Raytheon	54164	253-43
			1027-78
	Signetics	54164	253-45
			1027-82
	TI	SN54164	253-47
54165	Fairchild	54165	252-190
			1027-33
	Ferranti	ZN54165	252-192
	Motorola	MC54165	252-195
			1027-35
	National	DM54165	252-197
			1027-37
	Raytheon	54165	252-199
			1027-39
	Signetics	54165	252-201
			1027-41
	TI	SN54165	253-4
			1027-43
54166	Fairchild	54166	253-11
			1027-45
	Ferranti	ZN54166	253-13
	National	DM54166	253-17
			1027-47
	Raytheon	54166	253-19
54166	Raytheon	54166	1027-49
	Signetics	54166	253-21
			1027-51
	TI	SN54166	253-23
			1027-53
54167	Fairchild	54167	254-127
	Motorola	MC54167	254-130
	TI	SN54167	254-132
5417	Fairchild	5417	233-97
	ITT	ITT5417	233-100
	Motorola	MC5417	233-103
	National	DM5417	233-105
	Signetics	5417	233-107
	TI	SN5417	233-109
54170	Fairchild	54170	247-30
			1010-58
	Ferranti	ZN54170	247-32
			1010-62
	National	DM54170	1010-67
	Raytheon	54170	247-38
			1010-71
	Signetics	54170	247-40
	TI	SN54170	247-42
			1010-75
54173	Fairchild	54173	237-14
	National	DM54173	237-16
	TI	SN54173	237-25
54174	AMD	SN54174	237-164
	Fairchild	54174	237-166
	Ferranti	ZN54174	237-169
	Motorola	MC54174	237-173
	National	DM54174	237-175
	Raytheon	54174	237-177
	Signetics	54174	237-179
	TI	SN54174	237-181
54175	AMD	SN54175	237-39
	Fairchild	54175	237-41
	Ferranti	ZN54175	237-43
	Motorola	MC54175	237-47
	National	DM54175	237-49
	Raytheon	54175	237-52
	Signetics	54175	237-54
	TI	SN54175	237-56
54176	Fairchild	54176	229-57
	Motorola	MC54176	229-63
	National	DM54176	229-73
	TI	SN54176	229-87
54177	Fairchild	54177	227-69
	Motorola	MC54177	227-79
	National	DM54177	227-89
	TI	SN54177	227-101
54178	Fairchild	54178	252-79
			1025-81
	TI	SN54178	252-87
			1025-101
54179	Fairchild	54179	252-91
			1025-83
	TI	SN54179	252-99
			1025-103
54180	Fairchild	54180	255-4
	Ferranti	ZN54180	255-6
	ITT	ITT54180	255-10
	Motorola	MC54180	255-13
	National	DM54180	255-15
	Raytheon	54180	255-19
	Signetics	54180	255-25
	TI	SN54180	255-27
54181	AMD	SN54181	224-18
	Fairchild	54181	224-22
	Ferranti	ZN54181	224-24
	Motorola	MC54181	224-28
	National	DM54181	224-30
	Raytheon	54181	224-33
	Signetics	54181	224-39
	TI	SN54181	224-41
54182	AMD	SN54182	224-92
	Fairchild	54182	224-96
	ITT	ITT54182	224-99
	Motorola	MC54182	224-102
	National	DM54182	224-105
	Raytheon	54182	224-109
	Signetics	54182	224-111
	TI	SN54182	224-113
54184	Ferranti	ZN54184	255-60
	National	DM54184	255-62
	TI	SN54184	255-64
54184	TI	SN54184	1000-25
54185	National	DM54185A	255-70
	TI	SN54185A	255-73
			1000-37
54187	National	DM54187	1020-44
	TI	SN54187	1020-46
54188	TI	SN54188A	1003-28
5419	SSS	SCL5419	213-137
54190	Fairchild	54190	230-58
	ITT	ITT54190	230-61
	Motorola	MC54190	230-64
	National	DM54190	230-68
	Raytheon	54190	230-70
	Signetics	54190	230-72
	TI	SN54190	230-74
54191	Fairchild	54191	228-68
	Ferranti	ZN54191	228-70
	ITT	ITT54191	228-73
	Motorola	MC54191	228-76
	National	DM54191	228-78
	Raytheon	54191	228-80
	Signetics	54191	228-82
	TI	SN54191	228-84
54192	AMD	SN54192	230-103
	Fairchild	54192	230-107
	Ferranti	ZN54192	230-109
	ITT	ITT54192	230-112
	Motorola	MC54192	230-115
	National	DM54192	230-119
	Raytheon	54192	230-122
	Signetics	54192	230-126
	TI	SN54192	230-128
54193	AMD	SN54193	228-113
	Fairchild	54193	228-117
	Ferranti	ZN54193	228-119
	ITT	ITT54193	228-122
	Motorola	MC54193	228-125
	National	DM54193	228-129
	Raytheon	54193	228-134
	Signetics	54193	228-138
	TI	SN54193	228-141
54194	AMD	SN54194	251-87
			1025-77
	Fairchild	54194	251-189
			1025-85
	Ferranti	ZN54194	251-191
	ITT	ITT54194	251-194
			1025-89
	Motorola	MC54194	251-196
			1025-91
	National	DM54194	251-198
	Raytheon	54194	251-200
			1025-93
	Signetics	54194	251-202
			1025-97
	TI	SN54194	252-2
			1025-105
54195	AMD	SN54195	251-86
			1025-107
	Fairchild	54195	251-90
	ITT	ITT54195	251-94
			1025-119
	Motorola	MC54195	251-98
			1026-2
	National	DM54195	251-102
			1026-6
	Raytheon	54195	251-107
			1026-12
	Signetics	54195	251-109
			1026-22
	TI	SN54195	251-114
			1026-24
54196	Fairchild	54196	229-59
	Motorola	MC54196	229-65
	National	DM54196	229-75
	TI	SN54196	229-89
54197	Fairchild	54197	227-71
	Ferranti	ZN54197	227-73
	Motorola	MC54197	227-81
	National	DM54197	227-87
	TI	SN54197	227-103
54198	Fairchild	54198	252-148
			1027-9
	National	DM54198	252-152
			1027-13
	Raytheon	54198	252-155

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54198	Raytheon	54198	1027-17
	Signetics	54198	252-157
			1027-21
	TI	SN54198	252-159
			1027-25
54199	Fairchild	54199	252-133
			1027-11
	National	DM54199	252-139
			1027-15
	Raytheon	54199	252-141
			1027-19
	Signetics	54199	252-143
			1027-23
	TI	SN54199	252-145
			1027-27
542	Sanyo	STK542	604-69
	Signetics	NE542	555-181
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5420	Fairchild	5420	239-200
	Ferranti	ZN5420	240-5
	ITT	ITT5420	240-8
	Motorola	MC5420	240-13
	National	DM5420	240-15
	Raytheon	5420	240-19
	Signetics	5420	240-21
	TI	SN5420	240-23
5421	Fairchild	5421	238-71
	ITT	ITT5421	238-73
	Raytheon	5421	238-75
	Signetics	5421	238-77
5422	Fairchild	5422	240-148
	Raytheon	5422	240-151
	TI	SN5422	240-153
54221	AMD	SN54221	250-190
	TI	SN54221	250-193
5423	Fairchild	5423	245-61
	Motorola	MC5423	245-63
	National	DM5423	245-67
	TI	SN5423	245-70
5424	SSS	SCL5424	208-88
			326-17
54246	TI	SN54246	325-161
54247	TI	SN54247	325-133
54248	TI	SN54248	325-67
54249	TI	SN54249	325-91
5425	Fairchild	5425	245-45
	Ferranti	ZN5425	245-47
	ITT	ITT5425	245-49
	Motorola	MC5425	245-52
	National	DM5425	245-54
	SSS	SCL5425A	213-145
	TI	SN5425	245-57
54251	National	DM54251	250-46
	TI	SN54251	250-48
54255	Raytheon	54255	232-132
54259	AMD	SN54259	246-13
	TI	SN54259	246-20
5426	Fairchild	5426	233-175
	ITT	ITT5426	233-179
	Motorola	MC5426	233-181
	National	DM5426	233-183
	Signetics	5426	233-189
	TI	SN5426	233-191
54265	TI	SN54265	255-94
5427	Fairchild	5427	245-85
	Ferranti	ZN5427	245-87
	Motorola	MC5427	245-91
	National	DM5427	245-93
	Signetics	5427	245-95
	SSS	SCL5427A	213-146
	TI	SN5427	245-97
54278	TI	SN54278	254-138
54279	Fairchild	54279	246-166
	Signetics	54279	246-168
	TI	SN54279	246-170
5428	Ferranti	ZN5428	245-121
	Signetics	5428	245-137
	TI	SN5428	245-141
54283	Fairchild	54283	223-30
	Raytheon	54283	223-46
	TI	SN54283	223-52
54284	National	DM54284	223-154
	TI	SN54284	223-155
54285	TI	SN54285	223-158
54290	Fairchild	54290	228-200
	Motorola	MC54290	229-13
54290	TI	SN54290	229-22
54293	Fairchild	54293	227-5
	Motorola	MC54293	227-19
	TI	SN54293	227-26
54298	Fairchild	54298	237-120
			248-10
	Motorola	MC54298	237-122
			248-12
	Signetics	54298	237-124
			248-14
	TI	SN54298	237-126
			248-16
543	Sanyo	STK543	605-28
	Signetics	NE543	559-20
			615-103
5430	Fairchild	5430	239-113
	Ferranti	ZN5430	239-117
	ITT	ITT5430	239-121
	Motorola	MC5430	239-124
	National	DM5430	239-126
	Signetics	5430	239-129
	SSS	SCL5430	562-145
	TI	SN5430	239-131
54304	Mitsubishi	M54304	223-108
5432	Fairchild	5432	245-4
	Ferranti	ZN5432	245-6
	ITT	ITT5432	245-9
	National	DM5432	245-11
	Signetics	5432	245-13
	TI	SN5432	245-15
5433	Signetics	5433	245-181
	TI	SN5433	245-183
543570	**National**	**DM543570**	★1266
54365	National	DM54365	225-125
			234-72
	TI	SN54365	225-132
			234-75
54366	National	DM54366	226-145
			234-79
	TI	SN54366	226-151
			234-82
54367	National	DM54367	225-127
			234-85
	TI	SN54367	225-134
			234-88
54368	National	DM54368	226-147
			234-92
	TI	SN54368	226-152
			234-95
5437	Fairchild	5437	241-170
	Ferranti	ZN5437	241-181
	ITT	ITT5437	241-184
	Motorola	MC5437	241-187
	National	DM5437	241-189
	Raytheon	5437	241-194
	Signetics	5437	241-196
	SSS	SCL5437A	213-147
	TI	SN5437	241-198
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	Motorola	MC74H87	254-64
	TI	SN74H87	254-66
74LS00	Fairchild	74LS00	241-134
	ITT	ITT74LS00	241-135
	Motorola	SN74LS00	241-138
	National	DM74LS00	241-140
	NEC America	μPB74LS00	241-141
	Raytheon	74LS00	241-145
	Signetics	74LS00	241-147
	TI	SN74LS00	241-149
74LS01	Fairchild	74LS01	242-67
	ITT	ITT74LS01	242-71
	National	DM74LS01	242-76
	Raytheon	74LS01	242-83
	Signetics	74LS01	242-89
	TI	SN74LS01	242-93
74LS02	Fairchild	74LS02	245-147
	ITT	ITT74LS02	245-150
	Motorola	SN74LS02	245-153
74LS02	National	DM74LS02	245-155
	NEC America	μPB74LS02	245-156
	Raytheon	74LS02	245-160
	Signetics	74LS02	245-166
	TI	SN74LS02	245-170
74LS03	Fairchild	74LS03	242-70
	ITT	ITT74LS03	242-72
	Motorola	SN74LS03	242-74
	National	DM74LS03	242-78
	NEC America	μPB74LS03	242-79
	Raytheon	74LS03	242-87
	Signetics	74LS03	242-91
	TI	SN74LS03	242-95
74LS04	Fairchild	74LS04	226-20
	ITT	ITT74LS04	226-21
	Motorola	SN74LS04	226-23
	National	DM74LS04	226-25
	NEC America	μPB74LS04	226-26
	Raytheon	74LS04	226-30
	Signetics	74LS04	226-32
	TI	SN74LS04	226-34
74LS05	Fairchild	74LS05	226-96
	ITT	ITT74LS05	226-97
	Motorola	SN74LS05	226-99
	National	DM74LS05	226-101
	NEC America	μPB74LS05	226-102
	Raytheon	74LS05	226-106
	Signetics	74LS05	226-108
	TI	SN74LS05	226-110
74LS08	Fairchild	74LS08	239-33
	ITT	ITT74LS08	239-34
	Motorola	SN74LS08	239-36
	National	DM74LS08	239-38
	NEC America	μPB74LS08	239-39
	Raytheon	74LS08	239-43
	Signetics	74LS08	239-45
	TI	SN74LS08	239-47
74LS09	Fairchild	74LS09	239-87
	ITT	ITT74LS09	239-88
	National	DM74LS09	239-92
	Raytheon	74LS09	239-96
	Signetics	74LS09	239-98
	TI	SN74LS09	239-100
74LS10	Fairchild	74LS10	241-31
	ITT	ITT74LS10	241-32
	Motorola	SN74LS10	241-34
	National	DM74LS10	241-36
	NEC America	μPB74LS10	241-37
	Raytheon	74LS10	241-41
	Signetics	74LS10	241-43
	TI	SN74LS10	241-45
74LS107	Fairchild	74LS107	236-39
	ITT	ITT74LS107	236-41
	National	DM74LS107	236-47
	Raytheon	74LS107	236-55
	Signetics	74LS107	236-59
	TI	SN74LS107A	236-63
74LS109	Fairchild	74LS109	235-75
	ITT	ITT74LS109A	235-76
	Motorola	SN74LS109	235-78
	National	DM74LS109	235-80
	NEC America	μPB74LS109	235-81
	Raytheon	74LS109	235-85
	Signetics	74LS109	235-87
	TI	SN74LS109A	235-89
74LS11	Fairchild	74LS11	238-127
	ITT	ITT74LS11	238-128
	Motorola	SN74LS11	238-130
	National	DM74LS11	238-133
	NEC America	μPB74LS11	238-134
	Raytheon	74LS11	238-138
	Signetics	74LS11	238-140
	TI	SN74LS11	238-142
74LS112	Fairchild	74LS112	235-158
	ITT	ITT74LS112	235-159
	National	DM74LS112	235-161
	Raytheon	74LS112	235-166
	Signetics	74LS112	235-168
	TI	SN74LS112A	235-170
74LS113	Fairchild	74LS113	235-97
	ITT	ITT74LS113	235-98
	National	DM74LS113	235-100
	NEC America	μPB74LS113	235-101
	Raytheon	74LS113	235-105
	Signetics	74LS113	235-107
	TI	SN74LS113A	235-109
74LS114	Fairchild	74LS114	235-128
	ITT	ITT74LS114	235-129
	Motorola	SN74LS114	235-131
	National	DM74LS114	235-133
	Raytheon	74LS114	235-139
	Signetics	74LS114	235-141
	TI	SN74LS114A	235-143
74LS12	Fairchild	74LS12	241-89
	National	DM74LS12	241-91
	Raytheon	74LS12	241-95
	Signetics	74LS12	241-97
	TI	SN74LS12	241-99
74LS122	National	DM74LS122	250-176
	NEC America	μPB74LS122	235-162
	Raytheon	**74LS122**	★ 275
			250-180
	TI	SN74LS122	250-182
74LS123	AMD	SN74LS123	251-64
	ITT	ITT74LS123	251-65
	National	DM74LS123	251-67
	Raytheon	**74LS123**	★ 275
			251-73
	TI	SN74LS123	251-75
74LS124	TI	SN74LS124	256-16
			597-70
74LS125	Fairchild	74LS125	225-76
	ITT	ITT74LS125	225-77
	National	DM74LS125	225-79
	Raytheon	74LS125	225-83
	Signetics	74LS125	225-85
	TI	SN74LS125A	225-87
74LS126	Fairchild	74LS126	225-106
	ITT	ITT74LS126	225-107
	Motorola	SN74LS126	225-109
	National	DM74LS126	225-111
	Raytheon	74LS126	225-115
	Signetics	74LS126	225-117
	TI	SN74LS126A	225-119
74LS13	Fairchild	74LS13	255-127
	ITT	ITT74LS13	255-128
	Motorola	SN74LS13	255-129
	National	DM74LS13	255-131
	Raytheon	**74LS13**	★ 264
			255-136
	Signetics	74LS13	255-138
	TI	SN74LS13	255-140
74LS132	Fairchild	74LS132	255-157
	ITT	ITT74LS132	255-158
	National	DM74LS132	255-162
	Raytheon	**74LS132**	★ 264
			255-166
	Signetics	74LS132	255-167
	TI	SN74LS132	255-170
74LS133	Fairchild	74LS133	239-188
	ITT	ITT74LS133	239-189
74LS136	Fairchild	74LS136	244-152
	ITT	ITT74LS136	244-153
	Motorola	SN74LS136	244-155
	National	DM74LS136	244-157
	Raytheon	74LS136	244-161
	Signetics	74LS136	244-163
	TI	SN74LS136	244-165
74LS138	AMD	SN74LS138	232-186
	Fairchild	74LS138	232-190
	ITT	ITT74LS138	232-191
	Motorola	SN74LS138	232-193
	National	DM74LS138	232-195
			1511-15
	NEC America	μPB74LS138	232-196
	Raytheon	74LS138	232-202
	Signetics	74LS138	232-204
	TI	SN74LS138	232-206
			1511-17
74LS139	AMD	SN74LS139	232-142
	Fairchild	74LS139	232-146
	ITT	ITT74LS139	232-147
	Motorola	SN74LS139	232-149
	National	DM74LS139	232-151
	NEC America	μPB74LS139	232-152
	Raytheon	74LS139	232-158
	Signetics	74LS139	232-160
	TI	SN74LS139	232-162
74LS14	Fairchild	74LS14	255-191
	ITT	ITT74LS14	255-192
	National	DM74LS14	255-196
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74LS145	Fairchild	74LS145	232-13
	Signetics	74LS145	232-14
	TI	SN74LS145	232-16
74LS147	TI	SN74LS147	254-185
74LS148	AMD	SN74LS148	254-167
	TI	SN74LS148	254-171
			1512-142
74LS15	Fairchild	74LS15	238-174
	ITT	ITT74LS15	238-175
	Motorola	SN74LS15	238-177
	National	DM74LS15	238-179
	Raytheon	74LS15	238-183
	Signetics	74LS15	238-185
	TI	SN74LS15	238-187
74LS151	AMD	SN74LS151	249-199
	Fairchild	74LS151	249-203
	ITT	ITT74LS151	250-2
	Motorola	SN74LS151	250-4
	National	DM74LS151	250-6
	NEC America	μPB74LS151	250-7
			250-61
	Raytheon	74LS151	250-13
	Signetics	74LS151	250-15
	TI	SN74LS151	250-17
74LS152	Fairchild	74LS152	249-137
	Motorola	SN74LS152	249-139
	Raytheon	74LS152	249-143
74LS153	AMD	SN74LS153	249-22
	Fairchild	74LS153	249-26
	ITT	ITT74LS153	249-27
	Motorola	SN74LS153	249-29
	National	DM74LS153	249-31
	NEC America	μPB74LS153	249-32
	Raytheon	74LS153	249-38
	Signetics	74LS153	249-40
	TI	SN74LS153	249-42
74LS154	National	DM74LS154	233-80
	Signetics	74LS154	233-82
74LS155	Fairchild	74LS155	232-80
	ITT	ITT74LS155	232-81
	Motorola	SN74LS155	232-83
	National	DM74LS155	232-85
	NEC America	μPB74LS155	232-86
	Raytheon	74LS155	232-90
	Signetics	74LS155	232-91
	TI	SN74LS155	232-93
74LS156	Fairchild	74LS156	232-117
	ITT	ITT74LS156	232-118
	Motorola	SN74LS156	232-120
	National	DM74LS156	232-122
	Raytheon	74LS156	232-126
	Signetics	74LS156	232-127
	TI	SN74LS156	232-129
74LS157	AMD	SN74LS157	247-163
	Fairchild	74LS157	247-167
	ITT	ITT74LS157	247-168
	Motorola	SN74LS157	247-170
	National	DM74LS157	247-172
	NEC America	μPB74LS157	247-173
	Raytheon	74LS157	247-179
	Signetics	74LS157	247-181
	TI	SN74LS157	247-183
74LS158	AMD	SN74LS158	248-47
	Fairchild	74LS158	248-51
	ITT	ITT74LS158	248-52
	Motorola	SN74LS158	248-54
	National	DM74LS158	248-56
	Raytheon	74LS158	248-62
	Signetics	74LS158	248-64
	TI	SN74LS158	248-66
74LS160	AMD	SN74LS160	229-149
	Fairchild	74LS160	229-153
	ITT	ITT74LS160A	229-154
	Motorola	SN74LS160	229-156
	National	DM74LS160	229-158
	Raytheon	74LS160	229-162
	Signetics	74LS160	229-165
	TI	SN74LS160A	229-167
74LS161	AMD	SN74LS161	228-20
	Fairchild	74LS161	228-24
	ITT	ITT74LS161A	228-25
	Motorola	SN74LS161	228-27
74LS161	National	DM74LS161	228-30
	NEC America	μPB74LS161	228-28
	Raytheon	74LS161	228-36
	Signetics	74LS161	228-38
	TI	SN74LS161A	228-40
74LS162	AMD	SN74LS162	229-198
	Fairchild	74LS162	229-202
	ITT	ITT74LS162A	229-203
	Motorola	SN74LS162	229-205
	National	DM74LS162	229-207
	Raytheon	74LS162	230-7
	Signetics	74LS162	230-8
	TI	SN74LS162A	230-10
74LS163	AMD	SN74LS163	227-156
	Fairchild	74LS163	227-160
	ITT	ITT74LS163A	227-161
	Motorola	SN74LS163	227-163
	National	DM74LS163	227-165
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	Signetics	74LS163	227-173
	TI	SN74LS163A	227-175
74LS164	AMD	SN74LS164	253-53
	Fairchild	74LS164	253-58
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	ITT	ITT74LS164	253-54
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	Motorola	SN74LS164	253-60
		74LS164	1027-70
	National	DM74LS164	253-62
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	NEC America	μPB74LS164	253-63
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	Signetics	74LS164	253-70
			1027-81
	TI	SN74LS164	253-72
			1027-85
74LS165	Fairchild	74LS165	253-7
	TI	SN74LS165	253-9
74LS166	TI	SN74LS166	253-26
74LS168	AMD	SN74LS168	230-171
	Fairchild	74LS168	230-174
	National	DM74LS168	230-176
	TI	SN74LS168	230-178
74LS169	AMD	SN74LS169	228-173
	Fairchild	74LS169	228-176
	National	DM74LS169	228-178
	TI	SN74LS169A	228-180
74LS170	AMD	SN74LS170	247-47
			1010-57
	Fairchild	74LS170	247-51
			1010-61
	ITT	ITT74LS170	247-52
			1010-64
	Motorola	SN74LS170	247-54
			1010-66
	National	DM74LS170	247-56
			1010-70
	Raytheon	74LS170	247-60
			1010-54
	Signetics	74LS170	247-66
			1010-74
	TI	SN74LS170	247-68
			1010-78
74LS173	Fairchild	74LS173	237-30
	National	DM74LS173	237-32
	Signetics	74LS173	237-34
	TI	SN74LS173	237-36
74LS174	AMD	SN74LS174	237-186
	Fairchild	74LS174	237-190
	ITT	ITT74LS174	237-191
	Motorola	SN74LS174	237-192
	National	DM74LS174	237-194
	Raytheon	74LS174	237-200
	Signetics	74LS174	238-2
	TI	SN74LS174	238-4
74LS175	AMD	SN74LS175	237-61
	Fairchild	74LS175	237-65
	ITT	ITT74LS175	237-66
	Motorola	SN74LS175	237-70
	National	DM74LS175	237-72
	NEC America	μPB74LS175	237-73
	Raytheon	74LS175	237-79
	Signetics	74LS175	237-81
74LS175	TI	SN74LS175	237-83
74LS181	AMD	SN74LS181	224-46
	Fairchild	74LS181	224-49
	Motorola	SN74LS181	224-51
	Raytheon	74LS181	224-55
	Signetics	74LS181	224-59
	TI	SN74LS181	224-61
74LS183	TI	SN74LS183	223-115
74LS189	National	DM74LS189	★1289
			1011-57
74LS190	AMD	SN74LS190	230-79
	Fairchild	74LS190	230-83
	ITT	ITT74LS190	230-84
	Motorola	SN74LS190	230-86
	National	DM74LS190	230-88
	Raytheon	74LS190	230-94
	Signetics	74LS190	230-96
	TI	SN74LS190	230-98
74LS191	AMD	SN74LS191	228-89
	Fairchild	74LS191	228-93
	ITT	ITT74LS191	228-94
	Motorola	SN74LS191	228-96
	National	DM74LS191	228-98
	Raytheon	74LS191	228-104
	Signetics	74LS191	228-106
	TI	SN74LS191	228-108
74LS192	AMD	SN74LS192	230-136
	Fairchild	74LS192	230-140
	ITT	ITT74LS192	230-141
	Motorola	SN74LS192	230-143
	National	DM74LS192	230-145
	NEC America	μPB74LS192	230-146
	Raytheon	74LS192	230-152
	Signetics	74LS192	230-154
	TI	SN74LS192	230-156
74LS193	AMD	SN74LS193	228-147
	Fairchild	74LS193	228-151
	ITT	ITT74LS193	228-152
	Motorola	SN74LS193	228-154
	National	DM74LS193	228-156
	NEC America	μPB74LS193	228-157
	Raytheon	74LS193	228-163
	Signetics	74LS193	228-165
	TI	SN74LS193	228-167
74LS194	AMD	SN74LS194A	252-7
	Fairchild	74LS194	252-11
			1025-114
	ITT	ITT74LS194A	252-12
	Motorola	SN74LS194	252-14
	NEC America	μPB74LS194	252-15
	Raytheon	74LS194A	252-21
	Signetics	74LS194A	252-22
	TI	SN74LS194A	252-24
74LS195	AMD	SN74LS195A	251-119
	Fairchild	74LS195	251-123
			1025-116
	ITT	ITT74LS195A	251-124
	Motorola	SN74LS195	251-126
	NEC America	μPB74LS195	251-127
	Raytheon	74LS195	1026-21
		74LS195A	251-133
	Signetics	74LS195A	251-135
	TI	SN74LS195A	251-138
74LS196	Fairchild	74LS196	229-94
	ITT	ITT74LS196	229-95
	Motorola	SN74LS196	229-97
	National	DM74LS196	229-99
	Raytheon	74LS196	229-103
	Signetics	74LS196	229-104
	TI	SN74LS196	229-106
74LS197	Fairchild	74LS197	227-108
	ITT	ITT74LS197	227-109
	Motorola	SN74LS197	227-111
	National	DM74LS197	227-113
	Raytheon	74LS197	227-117
	Signetics	74LS197	227-118
	TI	SN74LS197	227-120
74LS20	Fairchild	74LS20	240-30
	ITT	ITT74LS20	240-31
	Motorola	SN74LS20	240-33
	National	DM74LS20	240-35
	NEC America	μPB74LS20	240-36
	Raytheon	74LS20	240-40
	Signetics	74LS20	240-42
	TI	SN74LS20	240-44
74LS201	TI	SN74LS201	1012-71
74LS209	Motorola	SN74LS209	239-90
74LS21	Fairchild	74LS21	238-83
	ITT	ITT74LS21	238-84
	Motorola	SN74LS21	238-86
	National	DM74LS21	238-88
	NEC America	μPB74LS21	238-89
	Raytheon	74LS21	238-93
	Signetics	74LS21	238-95
	TI	SN74LS21	238-97
74LS214	TI	SN74LS214	1016-39
74LS215	TI	SN74LS215	1016-25
74LS22	Fairchild	74LS22	240-158
	ITT	ITT74LS22	240-159
	Motorola	SN74LS22	240-161
	National	DM74LS22	240-163
	Raytheon	74LS22	240-167
	Signetics	74LS22	240-169
	TI	SN74LS22	240-171
74LS221	ITT	ITT74LS221	250-195
	National	DM74LS221	250-197
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	Signetics	74LS221	251-7
	TI	SN74LS221	251-9
74LS240	AMD	SN74LS240	256-116
			332-48
	Fairchild	74LS240	256-118
			332-52
	ITT	ITT74LS240	256-119
			332-53
	MMI	74LS240	256-121
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	Raytheon	74LS240	★ 279
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			333-2
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	Signetics	74LS240	256-128
			333-5
	TI	SN74LS240	256-130
			333-7
74LS241	AMD	SN74LS241	256-148
			332-16
	Fairchild	74LS241	256-150
			332-20
	ITT	ITT74LS241	256-151
			332-21
	MMI	74LS241	256-153
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	Raytheon	74LS241	★ 279
			256-159
			332-35
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	Signetics	74LS241	256-160
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	TI	SN74LS241	256-162
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74LS242	ITT	ITT74LS242	256-45
			340-52
	Raytheon	74LS242	★ 282
			256-48
			340-55
	Signetics	74LS242	256-51
			340-58
	TI	SN74LS242	256-54
			340-60
74LS243	AMD	SN74LS243	340-51
	ITT	ITT74LS243	256-46
			340-53
	Raytheon	74LS243	★ 282
			256-50
			340-57
	Signetics	74LS243	256-52
			340-59
	TI	SN74LS243	256-56
			340-61
74LS244	AMD	SN74LS244	256-185
	ITT	ITT74LS244	256-175
	MMI	74LS244	256-177
	Raytheon	74LS244	★ 279
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	Signetics	74LS244	256-182
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	TI	SN74LS247	325-140
74LS248	National	DM74LS248	325-58
	TI	SN74LS248	325-74
74LS249	National	DM74LS249	325-86
	TI	SN74LS249	325-96
74LS251	AMD	SN74LS251	250-53
	Fairchild	74LS251	250-57
	ITT	ITT74LS251	250-58
	Motorola	SN74LS251	250-60
	NEC America	μPB74LS251	1512-135
	Raytheon	74LS251	250-67
	Signetics	74LS251	250-71
	TI	SN74LS251	250-73
			1512-137
74LS253	AMD	SN74LS253	249-60
	Fairchild	74LS253	249-64
	ITT	ITT74LS253	249-65
	Motorola	SN74LS253	249-67
	National	DM74LS253	249-70
	NEC America	μPB74LS253	249-71
	Raytheon	74LS253	249-77
	Signetics	74LS253	249-79
	TI	SN74LS253	249-81
74LS255	Raytheon	74LS255	232-137
74LS256	Fairchild	74LS256	246-33
74LS257	AMD	SN74LS257	248-116
	Fairchild	74LS257	248-120
	ITT	ITT74LS257	248-121
	Motorola	SN74LS257	248-123
	National	DM74LS257	248-125
	Raytheon	74LS257	248-132
	Signetics	74LS257	248-134
	TI	SN74LS257	248-137
74LS258	AMD	SN74LS258	248-83
	Fairchild	74LS258	248-87
	ITT	ITT74LS258	248-88
	Motorola	SN74LS258	248-90
	National	DM74LS258	248-92
	NEC America	μPB74LS258	248-93
	Raytheon	74LS258	248-99
	Signetics	74LS258	248-100
	TI	SN74LS258	248-102
74LS259	Fairchild	74LS259	246-25
	ITT	ITT74LS259	246-26
	Motorola	SN74LS259	246-28
	TI	SN74LS259	246-30
			1512-163
74LS26	Fairchild	74LS26	242-175
	National	DM74LS26	242-177
	Raytheon	74LS26	242-181
	Signetics	74LS26	242-183
	TI	SN74LS26	242-185
74LS260	Fairchild	74LS260	245-76
	Signetics	74LS260A	245-78
74LS261	ITT	ITT74LS261	223-134
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	Signetics	74LS261	223-141
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74LS266	Fairchild	74LS266	244-182
	ITT	ITT74LS266	244-183
	Motorola	SN74LS266	244-185
	National	DM74LS266	244-187
	Raytheon	74LS266	244-191
	Signetics	74LS266	244-193
	TI	SN74LS266	244-195
74LS27	Fairchild	74LS27	245-102
	ITT	ITT74LS27	245-103
	Motorola	SN74LS27	245-105
	National	DM74LS27	245-107
	NEC America	μPB74LS27	245-108
	Raytheon	74LS27	245-112
	Signetics	74LS27	245-114
	TI	SN74LS27	245-116
74LS273	AMD	SN74LS273	238-21
	ITT	ITT74LS273	238-22
	Signetics	74LS273	238-23
	TI	SN74LS273	238-25
74LS275	TI	SN74LS275	224-5
74LS278	TI	SN74LS278	254-141
74LS279	Fairchild	74LS279	246-175
	ITT	ITT74LS279	246-176
	Motorola	SN74LS279	246-178
	National	DM74LS279	246-180
74LS279	NEC America	μPB74LS279	246-181
	Raytheon	74LS279	246-185
	Signetics	74LS279	246-187
	TI	SN74LS279	246-189
74LS28	Fairchild	74LS28	245-149
	ITT	ITT74LS28	245-151
	Raytheon	74LS28	245-164
	Signetics	74LS28	245-168
	TI	SN74LS28	245-172
74LS280	Fairchild	74LS280	255-31
	TI	SN74LS280	255-33
74LS281	AMD	SN74LS281	224-130
74LS283	Fairchild	74LS283	223-61
	ITT	ITT74LS283	223-63
	Motorola	SN74LS283	223-67
	National	DM74LS283	223-72
	Raytheon	74LS283	223-80
	Signetics	74LS283	223-82
	TI	SN74LS283	223-86
74LS289	National	DM74LS289	1011-63
74LS290	Fairchild	74LS290	229-34
	ITT	ITT74LS290	229-36
	Motorola	SN74LS290	229-40
	Signetics	74LS290	229-50
	TI	SN74LS290	229-54
74LS293	Fairchild	74LS293	227-38
	ITT	ITT74LS293	227-40
	Motorola	SN74LS293	227-44
	Signetics	74LS293	227-52
	TI	SN74LS293	227-56
74LS295	Fairchild	74LS295	252-37
			1025-118
	Motorola	SN74LS295	252-39
	National	DM74LS295A	1025-70
	NEC America	μPB74LS295	252-40
	Raytheon	74LS295A	252-44
	Signetics	74LS295	252-45
	TI	SN74LS295B	252-47
74LS298	Fairchild	74LS298	237-136
			248-179
	Motorola	SN74LS298	237-138
			248-181
	Raytheon	74LS298	237-142
			248-185
	Signetics	74LS298	237-143
			248-186
	TI	SN74LS298	237-145
			248-188
74LS299	AMD	SN74LS299	252-169
	ITT	ITT74LS299	252-172
	Raytheon	74LS299	252-181
	TI	SN74LS299	252-183
74LS30	Fairchild	74LS30	239-139
	ITT	ITT74LS30	239-140
	Motorola	SN74LS30	239-142
	National	DM74LS30	239-144
	NEC America	μPB74LS30	239-145
	Raytheon	74LS30	239-149
	Signetics	74LS30	239-151
	TI	SN74LS30	239-153
74LS314	TI	SN74LS314	1016-38
74LS315	TI	SN74LS315	1016-23
74LS32	Fairchild	74LS32	245-20
	ITT	ITT74LS32	245-21
	Motorola	SN74LS32	245-23
	National	DM74LS32	245-25
	NEC America	μPB74LS32	245-26
	Raytheon	74LS32	245-30
	Signetics	74LS32	245-32
	TI	SN74LS32	245-34
74LS320	TI	SN74LS320	256-12
			597-15
74LS322	AMD	SN74LS322	223-174
			253-105
	TI	SN74LS322	223-178
			253-109
74LS323	AMD	SN74LS323	252-171
	ITT	ITT74LS323	252-173
	TI	SN74LS323	252-185
74LS324	TI	SN74LS324	256-10
			597-17
74LS325	TI	SN74LS325	256-18
			597-73
74LS326	TI	SN74LS326	256-20
			597-75
74LS327	TI	SN74LS327	256-22
74LS327	TI	SN74LS327	597-77
74LS33	Fairchild	74LS33	245-187
	Raytheon	74LS33	245-191
	Signetics	74LS33	245-193
	TI	SN74LS33	245-195
74LS347	TI	SN74LS347	325-142
74LS348	TI	SN74LS348	254-173
			1512-145
74LS352	Fairchild	74LS352	249-91
	National	DM74LS352	249-93
	TI	SN74LS352	249-95
74LS353	Fairchild	74LS353	249-98
	National	DM74LS353	249-100
	TI	SN74LS353	249-102
74LS362	TI	SN74LS362	1512-130
74LS363	TI	SN74LS363	246-53
74LS364	TI	SN74LS364	238-37
74LS365	Fairchild	74LS365	225-141
	ITT	ITT74LS365	225-144
	Motorola	SN74LS365	225-147
	National	DM74LS365	225-151
	NEC America	μPB74LS365	225-154
	Raytheon	**74LS365**	★ **286**
			225-159
	Signetics	74LS365	225-165
	TI	SN74LS365A	225-169
74LS366	Fairchild	74LS366	226-160
	Motorola	SN74LS366	226-165
	National	DM74LS366	226-169
	NEC America	μPB74LS366	226-172
	Raytheon	**74LS366**	★ **286**
			226-177
	Signetics	74LS366	226-183
	TI	SN74LS366A	226-187
74LS367	Fairchild	74LS367	225-143
	ITT	ITT74LS367	225-145
	Motorola	SN74LS367	225-149
	National	DM74LS367	225-153
	NEC America	μPB74LS367	225-155
	Raytheon	**74LS367**	★ **286**
			225-163
	Signetics	74LS367	225-167
	TI	SN74LS367A	225-171
74LS368	Fairchild	74LS368	226-162
	ITT	ITT74LS368	226-163
	Motorola	SN74LS368	226-167
	National	DM74LS368	226-171
	NEC America	μPB74LS368	226-173
	Raytheon	**74LS368**	★ **286**
			226-181
	Signetics	74LS368	226-185
	TI	SN74LS368A	226-189
74LS37	Fairchild	74LS37	242-3
	ITT	ITT74LS37	242-4
	Motorola	SN74LS37	242-6
	National	DM74LS37	242-8
	NEC America	μPB74LS37	242-9
	Raytheon	74LS37	242-13
	Signetics	74LS37	242-15
	TI	SN74LS37	242-17
74LS373	AMD	SN74LS373	246-42
	ITT	ITT74LS373	246-43
	MMI	74LS373	246-45
	Raytheon	**74LS373**	★ **288**
			246-51
	TI	SN74LS373	246-55
74LS374	AMD	SN74LS374	238-30
	MMI	74LS374	238-33
	Raytheon	**74LS374**	★ **288**
			238-31
	TI	SN74LS374	238-39
74LS375	ITT	ITT74LS375	246-149
	NEC America	μPB74LS375	246-152
	Signetics	74LS375	246-160
	TI	SN74LS375	246-164
74LS377	AMD	SN74LS377	238-54
	Fairchild	74LS377	238-57
	ITT	ITT74LS377	238-55
	Raytheon	**74LS377**	★ **288**
			238-59
	TI	SN74LS377	238-61
74LS378	AMD	SN74LS378	237-156
	ITT	ITT74LS378	237-157
	Signetics	74LS378	237-158
	TI	SN74LS378	237-160
74LS379	AMD	SN74LS379	237-98
74LS379	TI	SN74LS379	237-100
74LS38	Fairchild	74LS38	242-153
	ITT	ITT74LS38	242-154
	Motorola	SN74LS38	242-156
	National	DM74LS38	242-162
	NEC America	μPB74LS38	242-163
	Raytheon	74LS38	242-160
	Signetics	74LS38	242-164
	TI	SN74LS38	242-167
74LS381	AMD	SN74LS381	224-83
	ITT	ITT74LS381	224-84
	TI	SN74LS381	224-86
74LS384	AMD	SN74LS384	223-164
	TI	SN74LS384	223-168
74LS385	AMD	SN74LS385	223-126
	TI	SN74LS385	223-130
74LS386	ITT	ITT74LS386	244-102
	National	DM74LS386	244-75
	Raytheon	74LS386	244-114
	Signetics	74LS386	244-118
	TI	SN74LS386	244-122
74LS388	AMD	SN74LS388	237-113
74LS390	Fairchild	74LS390	230-38
	Signetics	74LS390	230-42
	TI	SN74LS390	230-44
74LS393	Fairchild	74LS393	227-63
	TI	SN74LS393	227-66
74LS395	Fairchild	74LS395	252-52
	National	DM74LS395	252-54
	NEC America	μPB74LS395	252-55
	Raytheon	**74LS395**	★ **291**
			252-59
	Signetics	74LS395	252-61
	TI	SN74LS395A	252-63
74LS396	TI	SN74LS396	247-5
			253-113
74LS398	TI	SN74LS398	237-147
			248-190
74LS399	AMD	SN74LS399	237-131
			248-175
	TI	SN74LS399	237-149
			248-192
74LS40	Fairchild	74LS40	240-103
	ITT	ITT74LS40	240-104
	Motorola	SN74LS40	240-106
	National	DM74LS40	240-108
	NEC America	μPB74LS40	240-109
	Raytheon	74LS40	240-113
	Signetics	74LS40	240-115
	TI	SN74LS40	240-117
74LS42	Fairchild	74LS42	231-164
	ITT	ITT74LS42	231-165
	Motorola	SN74LS42	231-167
	National	DM74LS42	231-169
	NEC America	μPB74LS42	231-170
	Raytheon	**74LS42**	★ **266**
			231-174
	Signetics	74LS42	231-176
	TI	SN74LS42	231-178
74LS424	TI	SN74LS424	1510-174
74LS43	**Raytheon**	**74LS43**	★ **266**
			231-93
74LS44	**Raytheon**	**74LS44**	★ **266**
			231-113
74LS445	TI	SN74LS445	232-18
74LS47	Fairchild	74LS47	325-108
	National	DM74LS47	325-123
	TI	SN74LS47	325-136
74LS48	Fairchild	74LS48	325-41
	National	DM74LS48	325-56
	TI	SN74LS48	325-72
74LS481	TI	SN74LS481	224-179
			1508-55
			1532-3
74LS49	Fairchild	74LS49	325-80
	National	DM74LS49	325-84
	TI	SN74LS49	325-94
74LS490	Fairchild	74LS490	230-41
	TI	SN74LS490	230-46
74LS51	Fairchild	74LS51	243-161
	ITT	ITT74LS51	243-162
	Motorola	SN74LS51	243-164
	National	DM74LS51	243-166
	NEC America	μPB74LS51	243-167
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	ITT	ITT74LS54	243-34
	Motorola	SN74LS54	243-36
	National	DM74LS54	243-38
	NEC America	μPB74LS54	243-39
	Raytheon	74LS54	243-43
	Signetics	74LS54	243-45
	TI	SN74LS54	243-47
74LS55	Fairchild	74LS55	243-180
	Motorola	SN74LS55	243-182
	National	DM74LS55	243-184
	NEC America	μPB74LS55	243-185
	Raytheon	74LS55	243-189
	Signetics	74LS55	243-191
	TI	SN74LS55	243-193
74LS57	NEC America	μPB74LS57	248-126
74LS63	TI	SN74LS63	257-2
74LS668	TI	SN74LS668	230-180
74LS670	AMD	SN74LS670	247-74
			1010-80
	Fairchild	74LS670	247-78
			1010-82
	ITT	ITT74LS670	247-79
			1010-83
	Motorola	SN74LS670	247-81
			1010-85
	National	DM74LS670	247-83
			1010-87
	Raytheon	74LS670	247-89
			1010-89
	Signetics	74LS670	247-91
			1010-91
	TI	SN74LS670	247-93
			1010-93
74LS73	Fairchild	74LS73	236-37
	ITT	ITT74LS73	236-40
	Motorola	SN74LS73	236-43
	National	DM74LS73	236-45
	Raytheon	74LS73	236-51
	Signetics	74LS73	236-57
	TI	SN74LS73A	236-61
74LS74	Fairchild	74LS74	236-167
	ITT	ITT74LS74	236-168
	Motorola	SN74LS74	236-170
	National	DM74LS74	236-172
	NEC America	μPB74LS74	236-173
	Raytheon	74LS74	236-177
	Signetics	74LS74	236-179
	TI	SN74LS74A	236-181
74LS75	Fairchild	74LS75	246-147
	ITT	ITT74LS75	246-148
	National	DM74LS75	246-151
	Raytheon	74LS75	246-156
	Signetics	74LS75	246-158
	TI	SN74LS75	246-162
74LS76	ITT	ITT74LS76	236-105
	National	DM74LS76	236-107
	Raytheon	74LS76	236-111
	Signetics	74LS76A	236-113
	TI	SN74LS76	236-115
74LS77	Fairchild	74LS77	246-114
	National	DM74LS77	246-115
	Raytheon	74LS77	246-119
74LS78	ITT	ITT74LS78	235-40
	National	DM74LS78	235-42
	Raytheon	74LS78	235-46
	Signetics	74LS78	235-48
	TI	SN74LS78A	235-50
74LS83	Fairchild	74LS83	223-59
	ITT	ITT74LS83A	223-62
	Motorola	SN74LS83	223-65
	National	DM74LS83A	223-69
	Raytheon	74LS83A	223-76
	Signetics	74LS83A	223-81
	TI	SN74LS83A	223-84
74LS85	Fairchild	74LS85	225-14
	Motorola	SN74LS85	225-16
	National	DM74LS85	225-16
	Raytheon	74LS85	225-22
	Signetics	74LS85	225-24
	TI	ITT74LS85	225-15
		SN74LS85	225-26
74LS86	Fairchild	74LS86	244-100
	ITT	ITT74LS86	244-101
	Motorola	SN74LS86	244-104
74LS86	NEC America	μPB74LS86	244-106
	Raytheon	74LS86	244-110
	Signetics	74LS86	244-116
	TI	SN74LS86	244-120
74LS90	Fairchild	74LS90	229-32
	ITT	ITT74LS90	229-35
	Motorola	SN74LS90	229-38
	National	DM74LS90	229-42
	Raytheon	**74LS90**	★ **268**
			229-46
	Signetics	74LS90	229-48
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74LS91	**Raytheon**	**74LS91**	★ **272**
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	TI	SN74LS91	253-99
74LS92	Fairchild	74LS92	231-14
	Motorola	SN74LS92	231-16
	National	DM74LS92	231-18
	Raytheon	**74LS92**	★ **268**
			231-22
	Signetics	74LS92	231-24
	TI	SN74LS92	231-26
74LS93	Fairchild	74LS93	227-36
	ITT	ITT74LS93	227-39
	Motorola	SN74LS93	227-42
	Raytheon	**74LS93**	★ **268**
			227-48
	Signetics	74LS93	227-50
	TI	SN74LS93	227-54
74LS95	Fairchild	74LS95	251-175
			1025-112
	ITT	ITT74LS95B	251-176
	Motorola	SN74LS95	251-178
	National	DM74LS95	1026-9
	Raytheon	74LS95	1026-17
		74LS95B	251-182
	Signetics	74LS95B	251-183
	TI	SN74LS95B	251-185
74LS96	ITT	ITT74LS96	252-124
	Signetics	74LS96	252-126
	TI	SN74LS96	252-128
74L164	National	DM74L164	1027-56
	TI	SN74L164	1027-58
74L187	National	DM74L187A	1020-88
74L91	National	DM74L91	1027-89
	TI	SN74L91	1027-87
74L95	National	DM74L95	1025-50
	TI	SN74L95	1025-46
74L99	TI	SN74L99	1025-45
74R00	Raytheon	74R00	241-162
74R02	Raytheon	74R02	246-4
74R04	Raytheon	74R04	226-48
74R05	Raytheon	74R05	226-122
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74R11	Raytheon	74R11	238-154
74R112	Raytheon	74R112	235-187
74R113	Raytheon	74R113	235-122
74R114	Raytheon	74R114	235-30
74R15	Raytheon	74R15	238-193
74R181	Raytheon	74R181	224-63
74R182	Raytheon	74R182	224-116
74R20	Raytheon	74R20	240-57
74R22	Raytheon	74R22	240-181
74R40	Raytheon	74R40	240-132
74R64	Raytheon	74R64	243-96
74R65	Raytheon	74R65	243-107
74R74	Raytheon	74R74	236-193
74SL14	Motorola	SN74SL14	255-194
74S00	Fairchild	74S00	241-168
	Ferranti	ZN74S00	241-170
	Hitachi	HD74S00	241-171
	National	DM74S00	241-173
	Signetics	74S00	241-175
	TI	SN74S00	241-177
74S02	Fairchild	74S02	245-174
	National	DM74S02	245-175
	Signetics	74S02	245-177
	TI	SN74S02	245-179
74S03	Fairchild	74S03	242-114
	Ferranti	ZN74S03	242-116
	Hitachi	HD74S03	242-117
	National	DM74S03	242-119
	Signetics	74S03	242-121
	TI	SN74S03	242-123
74S04	Fairchild	74S04	226-54
74S04	Hitachi	HD74S04	226-57
	National	DM74S04	226-59
	Signetics	74S04	226-61
	TI	SN74S04	226-64
74S05	Fairchild	74S05	226-128
	Hitachi	HD74S05	226-131
	National	DM74S05	226-133
	Signetics	74S05	226-135
	TI	SN74S05	226-139
74S08	Fairchild	74S08	239-57
	Signetics	74S08	239-59
	TI	SN74S08	239-61
74S09	Fairchild	74S09	239-104
	Signetics	74S09	239-106
	TI	SN74S09	239-108
74S10	Fairchild	74S10	241-64
	Hitachi	HD74S10	241-65
	National	DM74S10	241-67
	Signetics	74S10	241-70
	TI	SN74S10	241-72
74S109	Fairchild	74S109	235-91
74S11	Fairchild	74S11	238-160
	Hitachi	HD74S11	238-161
	National	DM74S11	238-163
	Signetics	74S11	238-165
	TI	SN74S11	238-167
74S112	Fairchild	74S112	235-172
	Hitachi	HD74S112	235-173
	Motorola	SN74S112	235-176
	National	DM74S112	235-177
	Signetics	74S112	235-179
	TI	SN74S112	235-181
74S113	Fairchild	74S113	235-111
	Hitachi	HD74S113	235-112
	Motorola	SN74S113	235-115
	National	DM74S113	235-116
	Signetics	74S113	235-118
	TI	SN74S113	235-120
74S114	Fairchild	74S114	235-145
	Hitachi	HD74S114	235-146
	National	DM74S114	235-148
	Signetics	74S114	235-150
	TI	SN74S114	235-152
74S124	TI	SN74S124	256-24
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74S132	Fairchild	74S132	255-172
	TI	SN74S132	255-174
74S133	Fairchild	74S133	239-192
	Hitachi	HD74S133	239-191
	National	DM74S133	239-194
	Signetics	74S133	239-196
	TI	SN74S133	239-198
74S134	Fairchild	74S134	239-177
	Hitachi	HD74S134	239-178
	National	DM74S134	239-179
	Signetics	74S134	239-181
	TI	SN74S134	239-183
74S135	Fairchild	74S135	244-199
	Hitachi	HD74S135	244-200
	National	DM74S135	244-201
	Signetics	74S135	244-202
	TI	SN74S135	245-2
74S136	National	DM74S136	244-166
74S138	AMD	SN74S138	233-3
	Fairchild	74S138	233-5
	National	DM74S138	233-8
	Signetics	74S138	233-9
	TI	SN74S138	233-11
74S139	AMD	SN74S139	232-166
	Fairchild	74S139	232-168
	National	DM74S139	232-169
	Signetics	74S139	232-171
	TI	SN74S139	232-173
74S140	Fairchild	74S140	234-107
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	National	DM74S140	234-109
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	Signetics	74S140	234-111
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	TI	SN74S140	234-113
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74S15	Fairchild	74S15	238-197
	Hitachi	HD74S15	239-2
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74S15	Signetics	74S15	239-6
	TI	SN74S15	239-8
74S151	AMD	SN74S151	250-19
	Fairchild	74S151	250-21
	Hitachi	HD74S151	250-24
	National	DM74S151	250-26
	Signetics	74S151	250-28
	TI	SN74S151	250-30
74S153	AMD	SN74S153	249-44
	Fairchild	74S153	249-46
	National	DM74S153	249-47
	Signetics	74S153	249-50
	TI	SN74S153	249-52
74S157	AMD	SN74S157	247-185
	Fairchild	74S157	247-189
	National	DM74S157	247-191
	Signetics	74S157	248-2
	TI	SN74S157	248-5
74S158	AMD	SN74S158	248-69
	Fairchild	74S158	248-71
	National	DM74S158	248-73
	Signetics	74S158	248-75
	TI	SN74S158	248-78
74S160	AMD	SN74S160	229-169
74S161	AMD	SN74S161	228-42
74S162	TI	SN74S162	230-12
74S163	TI	SN74S163	228-48
74S167	Fairchild	74S167	254-135
74S168	TI	SN74S168A	230-182
74S169	TI	SN74S169	228-182
74S172	Signetics	74S172	247-97
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74S174	AMD	SN74S174	238-6
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	Hitachi	HD74S174	238-9
	National	DM74S174	238-11
	Signetics	74S174	238-13
	TI	SN74S174	238-15
74S175	AMD	SN74S175	237-85
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	Fairchild	74S175	237-87
	Hitachi	HD74S175	237-88
	National	DM74S175	237-90
	Signetics	74S175	237-91
	TI	SN74S175	237-92
74S179	Signetics	74S179	251-146
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74S181	AMD	SN74S181	224-65
	Fairchild	74S181	224-68
	Hitachi	HD74S181	224-71
	Signetics	74S181	224-74
	TI	SN74S181	224-76
74S182	Fairchild	74S182	224-118
	National	DM74S182	224-122
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	National	DM7425	245-55
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9LS03	Fairchild	9LS03C	242-64
		9LS03M	242-65
	Raytheon	9LS03C	242-84
		9LS03M	242-85
9LS04	Fairchild	9LS04C	226-17
		9LS04M	226-18
	Raytheon	9LS04C	226-27
		9LS04M	226-28
9LS05	Fairchild	9LS05C	226-93
		9LS05M	226-94
	Raytheon	9LS05C	226-103
		9LS05M	226-104
9LS08	Fairchild	9LS08C	239-30
		9LS08M	239-31
	Raytheon	9LS08C	239-40
		9LS08M	239-41
9LS09	Fairchild	9LS09C	239-84
		9LS09M	239-85
	Raytheon	9LS09C	239-93
		9LS09M	239-94
9LS10	Fairchild	9LS10C	241-28
		9LS10M	241-29
	Raytheon	9LS10C	241-38
		9LS10M	241-39
9LS107	Raytheon	9LS107C	236-52
		9LS107M	236-53
9LS109	Fairchild	9LS109C	235-72
		9LS109M	235-73
	Raytheon	9LS109C	235-82
		9LS109M	235-83
9LS11	Fairchild	9LS11C	238-124
		9LS11M	238-125
	Raytheon	9LS11C	238-135
		9LS11M	238-136
9LS112	Fairchild	9LS112C	235-155
		9LS112M	235-156
	Raytheon	9LS112C	235-163
		9LS112M	235-164
9LS113	Fairchild	9LS113C	235-94
		9LS113M	235-95
	Raytheon	9LS113C	235-102
		9LS113M	235-103
9LS114	Fairchild	9LS114C	235-125
		9LS114M	235-126
9LS114	Raytheon	9LS114C	235-134
		9LS114M	235-137
9LS12	Raytheon	9LS12C	241-92
		9LS12M	241-93
9LS122	**Raytheon**	**9LS122**	★ **275**
		9LS122C	★ **275**
			250-177
		9LS122M	★ **275**
			250-178
9LS123	**Raytheon**	**9LS123**	★ **275**
		9LS123C	★ **275**
			251-68
		9LS123M	★ **275**
			251-69
9LS125	Fairchild	9LS125C	225-73
		9LS125M	225-74
	Raytheon	9LS125C	225-80
		9LS125M	225-81
9LS126	Fairchild	9LS126C	225-103
		9LS126M	225-104
	Raytheon	9LS126C	225-112
		9LS126M	225-113
9LS13	Fairchild	9LS13C	255-124
		9LS13M	255-125
	Raytheon	**9LS13**	★ **264**
		9LS13C	★ **264**
			255-133
		9LS13M	★ **264**
			255-134
9LS132	Fairchild	9LS132C	255-154
		9LS132M	255-155
	Raytheon	**9LS132**	★ **264**
		9LS132C	★ **264**
			255-163
		9LS132M	★ **264**
			255-164
9LS133	Fairchild	9LS133C	239-185
		9LS133M	239-186
9LS136	Fairchild	9LS136C	244-149
		9LS136M	244-150
	Raytheon	9LS136C	244-158
		9LS136M	244-159
9LS138	Fairchild	9LS138C	232-187
		9LS138M	232-188
	Raytheon	9LS138C	232-197
		9LS138M	232-198
9LS139	Fairchild	9LS139C	232-143
		9LS139M	232-144
	Raytheon	9LS139C	232-153
		9LS139M	232-154
9LS14	Fairchild	9LS14C	255-188
		9LS14M	255-189
	Raytheon	**9LS14**	★ **264**
		9LS14C	★ **264**
			255-197
		9LS14M	★ **264**
			255-198
9LS15	Fairchild	9LS15C	238-171
		9LS15M	238-172
	Raytheon	9LS15C	238-180
		9LS15M	238-181
9LS151	Fairchild	9LS151C	249-200
		9LS151M	249-201
	Raytheon	9LS151C	250-8
		9LS151M	250-9
9LS152	Fairchild	9LS152C	249-133
		9LS152M	249-134
	Raytheon	9LS152C	249-140
		9LS152M	249-141
9LS153	Fairchild	9LS153C	249-23
		9LS153M	249-24
	Raytheon	9LS153C	249-33
		9LS153M	249-34
9LS155	Fairchild	9LS155C	232-77
		9LS155M	232-78
	Raytheon	9LS155C	232-87
		9LS155M	232-88
9LS156	Fairchild	9LS156C	232-114
		9LS156M	232-115
	Raytheon	9LS156C	232-123
		9LS156M	232-124
9LS157	Fairchild	9LS157C	247-164
		9LS157M	247-165
	Raytheon	9LS157C	247-174
		9LS157M	247-175
9LS158	Fairchild	9LS158C	248-48
9LS158	Fairchild	9LS158M	248-49
	Raytheon	9LS158C	248-57
		9LS158M	248-60
9LS160	Fairchild	9LS160C	229-150
		9LS160M	229-151
	Raytheon	9LS160C	229-159
		9LS160M	229-160
9LS161	Fairchild	9LS161C	228-21
		9LS161M	228-22
	Raytheon	9LS161C	228-31
		9LS161M	228-32
9LS162	Fairchild	9LS162C	229-199
		9LS162M	229-200
	Raytheon	9LS162C	229-208
		9LS162M	230-3
9LS163	Fairchild	9LS163C	227-157
		9LS163M	227-158
	Raytheon	9LS163C	227-166
		9LS163M	227-167
9LS164	Fairchild	9LS164C	253-55
			1027-61
		9LS164M	253-56
			1027-62
	Raytheon	**9LS164**	★ **272**
		9LS164C	★ **272**
			253-64
			1027-74
		9LS164M	★ **272**
			253-65
			1027-75
9LS168	Fairchild	9LS168C	230-172
9LS169	Fairchild	9LS169C	228-174
9LS170	Fairchild	9LS170C	247-48
		9LS170M	247-49
	Raytheon	9LS170C	247-57
		9LS170M	247-58
9LS173	Fairchild	9LS173C	237-27
		9LS173M	237-28
9LS174	Fairchild	9LS174C	237-187
		9LS174M	237-188
	Raytheon	9LS174C	237-195
		9LS174M	237-196
9LS175	Fairchild	9LS175C	237-62
		9LS175M	237-63
	Raytheon	9LS175C	237-75
		9LS175M	237-74
9LS181	Fairchild	9LS181C	224-47
		9LS181M	224-48
	Raytheon	9LS181C	224-52
		9LS181M	224-53
9LS190	Fairchild	9LS190C	230-80
		9LS190M	230-81
	Raytheon	9LS190C	230-89
		9LS190M	230-90
9LS191	Fairchild	9LS191C	228-90
		9LS191M	228-91
	Raytheon	9LS191C	228-99
		9LS191M	228-100
9LS192	Fairchild	9LS192C	230-137
		9LS192M	230-138
	Raytheon	9LS192C	230-147
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	Raytheon	9LS193C	228-158
		9LS193M	228-159
9LS194	Fairchild	9LS194C	252-8
		9LS194M	252-9
	Raytheon	9LS194AC	252-16
		9LS194AM	252-17
9LS195	Fairchild	9LS195C	251-120
		9LS195M	251-121
	Raytheon	9LS195AC	251-128
		9LS195AM	251-129
		9LS195C	1026-18
		9LS195M	1026-19
9LS196	Fairchild	9LS196C	229-91
		9LS196M	229-92
	Raytheon	9LS196C	229-100
		9LS196M	229-101
9LS197	Fairchild	9LS197C	227-105
		9LS197M	227-106
	Raytheon	9LS197C	227-114
		9LS197M	227-115
9LS20	Fairchild	9LS20C	240-27
		9LS20M	240-28
9LS20	Raytheon	9LS20C	240-37
		9LS20M	240-38
9LS21	Fairchild	9LS21C	238-80
		9LS21M	238-81
	Raytheon	9LS21C	238-90
		9LS21M	238-91
9LS22	Fairchild	9LS22C	240-155
		9LS22M	240-156
	Raytheon	9LS22C	240-164
		9LS22M	240-165
9LS221	**Raytheon**	**9LS221**	★ 275
		9LS221C	★ 275
			250-198
		9LS221M	★ 275
			251-3
9LS240	**Raytheon**	**9LS240**	★ 279
			336-36
		9LS240C	★ 279
			332-62
		9LS240M	★ 279
			332-63
9LS241	**Raytheon**	**9LS241**	★ 279
			336-38
		9LS241C	★ 279
			332-30
		9LS241M	★ 279
			332-31
9LS242	**Raytheon**	**9LS242**	★ 282
		9LS242C	★ 282
			340-54
		9LS242M	★ 282
			340-7
9LS243	Raytheon	9LS243	★ 282
		9LS243C	★ 282
			340-56
		9LS243M	★ 282
			340-9
9LS244	**Raytheon**	**9LS244**	★ 279
		9LS244C	★ 279
		9LS244M	★ 279
9LS251	Fairchild	9LS251C	250-54
		9LS251M	250-55
	Raytheon	9LS251C	250-62
		9LS251M	250-63
9LS253	Fairchild	9LS253C	249-61
		9LS253M	249-62
	Raytheon	9LS253C	249-72
		9LS253M	249-73
9LS255	Raytheon	9LS255C	232-134
		9LS255M	232-135
9LS257	Fairchild	9LS257C	248-117
		9LS257M	248-118
	Raytheon	9LS257C	248-127
		9LS257M	248-128
9LS258	Fairchild	9LS258C	248-84
		9LS258M	248-85
	Raytheon	9LS258C	248-94
		9LS258M	248-95
9LS259	Fairchild	9LS259C	246-22
		9LS259M	246-23
9LS26	Fairchild	9LS26C	242-172
		9LS26M	242-173
	Raytheon	9LS26C	242-178
		9LS26M	242-179

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		9LS260M	245-74
9LS261	**Raytheon**	**9LS261**	★ 284
		9LS261C	★ 284
			223-136
		9LS261M	★ 284
			223-137
9LS266	Fairchild	9LS266C	244-179
		9LS266M	244-180
	Raytheon	9LS266C	244-188
		9LS266M	244-189
9LS27	Fairchild	9LS27C	245-99
		9LS27M	245-100
	Raytheon	9LS27C	245-109
		9LS27M	245-110
9LS279	Fairchild	9LS279C	246-172
		9LS279M	246-173
	Raytheon	9LS279C	246-182
		9LS279M	246-183
9LS28	Fairchild	9LS28C	245-148
	Raytheon	9LS28C	245-161
		9LS28M	245-162
9LS283	Fairchild	9LS283C	223-56
		9LS283M	223-57
	Raytheon	9LS283C	223-77
		9LS283M	223-78
9LS290	Fairchild	9LS290C	229-29
		9LS290M	229-30
9LS293	Fairchild	9LS293C	227-33
		9LS293M	227-34
9LS295	Fairchild	9LS295C	252-34
		9LS295M	252-35
	Raytheon	9LS295AC	252-41
		9LS295AM	252-42
9LS298	AMD	9LS298C	248-170
		9LS298M	248-171
	Fairchild	9LS298C	237-132
			248-176
		9LS298M	237-133
			248-177
	Raytheon	9LS298C	237-139
			248-182
		9LS298M	237-140
			248-183
9LS299	Raytheon	9LS299C	252-174
		9LS299M	252-175
9LS30	Fairchild	9LS30C	239-136
		9LS30M	239-137
	Raytheon	9LS30C	239-146
		9LS30M	239-147
9LS32	Fairchild	9LS32C	245-17
		9LS32M	245-18
	Raytheon	9LS32C	245-27
		9LS32M	245-28
9LS33	Fairchild	9LS33C	245-185
	Raytheon	9LS33C	245-188
		9LS33M	245-189
9LS365	Fairchild	9LS365C	225-136
		9LS365M	225-137
	Raytheon	**9LS365**	★ 286
		9LS365C	★ 286
			225-156
		9LS365M	★ 286
			225-157
9LS366	Fairchild	9LS366C	226-155
		9LS366M	226-156
	Raytheon	**9LS366**	★ 286
		9LS366C	★ 286
			226-174
		9LS366M	★ 286
			226-175
9LS367	Fairchild	9LS367C	225-138
		9LS367M	225-139
	Raytheon	**9LS367**	★ 286
		9LS367C	★ 286
			225-160
		9LS367M	★ 286
			225-161
9LS368	Fairchild	9LS368C	226-157
		9LS368M	226-158
	Raytheon	**9LS368**	★ 286
		9LS368C	★ 286
			226-178
		9LS368M	★ 286
			226-179
9LS37	Fairchild	9LS37C	241-202
		9LS37M	241-203
	Raytheon	9LS37C	242-10

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		9LS37M	242-11
9LS373	**Raytheon**	**9LS373**	★ 288
		9LS373C	★ 288
		9LS373M	★ 288
9LS374	**Raytheon**	**9LS374**	★ 288
		9LS374C	★ 288
		9LS374M	★ 288
9LS377	**Raytheon**	**9LS377**	★ 288
		9LS377C	★ 288
		9LS377M	★ 288
9LS38	Fairchild	9LS38C	242-150
		9LS38M	242-151
	Raytheon	9LS38C	242-157
		9LS38M	242-158
9LS386	Raytheon	9LS386C	244-111
		9LS386M	244-112
9LS390	Fairchild	9LS390C	230-36
9LS393	Fairchild	9LS393C	227-60
		9LS393M	227-61
9LS395	Fairchild	9LS395C	252-50
9LS395	**Raytheon**	**9LS395**	★ 291
		9LS395C	★ 291
			252-56
		9LS395M	★ 291
			252-57
9LS40	Fairchild	9LS40C	240-100
		9LS40M	240-101
	Raytheon	9LS40C	240-110
		9LS40M	240-111
9LS42	Fairchild	9LS42C	231-161
		9LS42M	231-162
	Raytheon	**9LS42**	★ 266
		9LS42C	★ 266
			231-171
		9LS42M	★ 266
			231-172
9LS43	**Raytheon**	**9LS43**	★ 266
		9LS43C	★ 266
			231-90
		9LS43M	★ 266
			231-91
9LS44	**Raytheon**	**9LS44**	★ 266
		9LS44C	★ 266
			231-110
		9LS44M	★ 266
			231-111
9LS490	Fairchild	9LS490C	230-39
9LS51	Fairchild	9LS51C	243-158
		9LS51M	243-159
	Raytheon	9LS51C	243-168
		9LS51M	243-169
9LS54	Fairchild	9LS54C	243-30
		9LS54M	243-31
	Raytheon	9LS54C	243-40
		9LS54M	243-41
9LS55	Fairchild	9LS55C	243-177
		9LS55M	243-178
	Raytheon	9LS55C	243-186
		9LS55M	243-187
9LS670	Fairchild	9LS670C	247-75
		9LS670M	247-76
	Raytheon	9LS670C	247-84
		9LS670M	247-85
9LS73	Fairchild	9LS73C	236-34
		9LS73M	236-35
	Raytheon	9LS73C	236-48
		9LS73M	236-49
9LS74	Fairchild	9LS74C	236-164
		9LS74M	236-165
	Raytheon	9LS74C	236-174
		9LS74M	236-175
9LS75	Raytheon	9LS75C	246-153
		9LS75M	246-154
9LS76	Raytheon	9LS76C	236-108
		9LS76M	236-109
9LS77	Raytheon	9LS77C	246-116
		9LS77M	246-117
9LS78	Raytheon	9LS78C	235-43
		9LS78M	235-44
9LS83	Fairchild	9LS83C	223-54
		9LS83M	223-55
	Raytheon	9LS83AC	223-73
		9LS83AM	223-74
9LS85	Fairchild	9LS85C	225-12
	Raytheon	9LS85C	225-19
		9LS85M	225-20
9LS86	Fairchild	9LS86C	244-97
		9LS86M	244-98

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	Raytheon	9LS86C	244-107
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9LS90	Fairchild	9LS90C	229-27
		9LS90M	229-28
	Raytheon	**9LS90**	★ 268
		9LS90C	★ 268
			229-43
		9LS90M	★ 268
			229-44
9LS91	**Raytheon**	**9LS91**	★ 272
		9LS91C	★ 272
			253-94
			1027-95
		9LS91M	★ 272
			253-95
			1027-96
9LS92	Fairchild	9LS92C	231-11
		9LS92M	231-12
9LS92	**Raytheon**	**9LS92**	★ 268
		9LS92C	★ 268
			231-19
		9LS92M	★ 268
			231-20
9LS93	Fairchild	9LS93C	227-31
		9LS93M	227-32
	Raytheon	**9LS93**	★ 268
		9LS93C	★ 268
			227-45
		9LS93M	★ 268
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9LS95	Fairchild	9LS95C	251-172
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	Raytheon	9LS95BC	251-178
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		9LS95BM	251-180
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9S04	Fairchild	9S04AC	226-55
		9S04AM	226-56
9S05	Fairchild	9S05AC	226-129
		9S05AM	226-130
9S41	Fairchild	9S41C	239-110
		9S41M	239-111
9S42	Fairchild	9S42C	242-190
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90	Burr-Brown	DAC90B	321-31
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900	SGS	TCA900	558-72
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9000	Fairchild	9000C	234-115
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9001	Fairchild	9001C	234-117
		9001M	234-118
	ITT	ITT9001	234-123
9002	Fairchild	9002C	241-105
		9002M	241-106
	ITT	ITT9002-1	241-113
		ITT9002-5	241-114
	National	DM9002C	241-121
9003	Fairchild	9003C	241-2
		9003M	241-3
	ITT	ITT9003-1	241-10
		ITT9003-5	241-11
	National	DM9003C	241-18
9004	Fairchild	9004C	240-2
		9004M	240-3
	ITT	ITT9004-1	240-10
		ITT9004-5	240-11
	National	DM9004C	240-17
9005	Fairchild	9005C	244-7
		9005M	244-8
	ITT	ITT9005-1	244-15
		ITT9005-5	244-16
	National	DM9005C	244-23
9006	Fairchild	9006C	244-65
		9006M	244-66
	National	DM9006C	244-67
9007	Fairchild	9007C	239-115
		9007M	239-116
9008	Fairchild	9008C	243-5
		9008M	243-6
	ITT	ITT9008-1	243-7
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	National	DM9008C	243-9
9009	Fairchild	9009C	240-77
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901	**National**	**BLC901**	★1656
	Plessey	SL901	560-29
9012	Fairchild	9012C	242-26
		9012M	242-27
	National	DM9012C	242-47
9014	Fairchild	9014C	244-136
		9014M	244-139
9015	Fairchild	9015C	245-42
		9015M	245-43
9016	Fairchild	9016C	225-188
		9016M	225-189
	ITT	ITT9016-1	225-196
		ITT9016-5	225-197
	National	DM9016C	226-7
9017	Fairchild	9017C	226-68
		9017M	226-70
902	**National**	**BLC902**	★1656
9020	Fairchild	9020C	235-193
		9020M	235-194
	ITT	ITT9020-1	235-195
		ITT9020-5	235-196
9022	Fairchild	9022C	236-83
		9022M	236-84
	ITT	ITT9022-1	236-90
		ITT9022-5	236-91
9024	Fairchild	9024C	235-59
		9024M	235-60
	ITT	ITT9024-1	235-62
		ITT9024-5	235-63
903	Panasonic	AN903	547-132
904	IPI	MC904	319-18
	Panasonic	AN904	547-187
905	Panasonic	AN905	547-133
9050	AMD	9050C	1009-70
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9060	AMD	9060C	1009-75
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9080	AMD	9080A	1514-2
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91L0	AMD	91L0EC	1018-107
91L01	AMD	91L01A	1014-84
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91L02	AMD	91L02	1017-59
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		91L02CM	1016-98
91L11	AMD	91L11A	1014-78
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9403	**Fairchild**	**9403**	★**1613**
		9403C	★**1613**
			1001-58
			1504-91
		9403DC	★**1613**
		9403DM	★**1613**
		9403M	★**1613**
			1001-59
			1504-92
		9403PC	★**1613**
9404	Fairchild	9404C	1504-83
		9404M	1504-84
9405	**Fairchild**	**9405A**	★**1620**
		9405AC	★**1620**
			224-150
			224-159
			1504-78
		9405ADC	★**1620**
		9405ADM	★**1620**
		9405AM	★**1620**
			224-151
			224-162
			1504-80
		9405APC	★**1620**
		9405C	1504-77
		9405M	1504-79
9406	Fairchild	9406C	1001-83
			1504-106
		9406M	1001-84
			1504-107
9407	Fairchild	9407C	1504-87
		9407M	1504-88
9408	**Fairchild**	**9408**	★**1625**
		9408AC	1504-73
		9408AM	1504-75
		9408C	★**1625**
			1504-72
		9408DC	★**1625**
		9408M	★**1625**
			1504-74
9409	Fairchild	F9409	1516-4
		9409	1507-9
941	NEC America	μPD941	556-57
9410	Fairchild	9410C	247-110
			1011-5
			1504-116
		9410M	247-111
			1504-117
9411	Fairchild	9411C	328-3
			1504-112
		9411M	1504-113
9412	Fairchild	9412C	1504-103
		9412M	1504-104
9414	Fairchild	9414	255-101
			1504-98
9415	Fairchild	9415	255-102
			1504-99
9416	Fairchild	9416	255-103
			1504-100
9417	Fairchild	9417	255-104
			1504-101
9423	Fairchild	9423	1001-81
		9423C	1504-95
		9423M	1504-96
943	NEC America	μPD943	556-58
9440	Fairchild	9440	1512-115
946	NEC America	μPD946	556-59
947	NEC America	μPD947	556-60
95H00	Fairchild	95H00C	1026-57
95H90	Fairchild	95H90C	259-81
			596-177
		95H90M	259-82
			596-178
95H91	Fairchild	95H91C	259-12
			596-160
		95H91M	596-161
950	NEC America	μPD950	556-61
	Plessey	TBA950	560-148
9500	ITT	TDA9500	560-138
95000	Fairchild	F95000	219-83
95002	Fairchild	F95002	219-69
95003	Fairchild	F95003	219-73
95004	Fairchild	F95004	219-65
95010	Fairchild	F95010	219-51
95016	Fairchild	F95016	219-49
95029	Fairchild	F95029	219-53
9505	Rockwell	CRC9505	312-67
9509	Rockwell	CRC9509	314-1
951	NEC America	μPD951	556-62
9510	Rockwell	CRC9510	314-19
95101	Fairchild	F95101	219-79
95102	Fairchild	F95102	219-77
95103	Fairchild	F95103	219-75
95105	Fairchild	F95105	219-71
95106	Fairchild	F95106	219-63
95107	Fairchild	F95107	219-57
95109	Fairchild	F95109	219-67
9511	AMD	AM9511C	1510-136
		AM9511M	1510-137
		9511	258-5
			1513-29
		9511-4	258-6
			1513-30
95110	Fairchild	F95110	219-59
95111	Fairchild	F95111	219-61
95115	Fairchild	F95115	219-89
95116	Fairchild	F95116	219-87
95124	Fairchild	F95124	219-85
95130	Fairchild	F95130	219-81
9517	AMD	AM9517C	1511-23
		AM9517M	1511-24
	DDC	9517	615-99
9518	DDC	9518	615-100
9519	AMD	9519C	1511-86
		9519M	1511-87
952	NEC America	μPD952	556-63
95231	Fairchild	F95231	219-55
9551	AMD	9551	¶ 148-3
		9551C	1510-182
		9551M	1510-183
9555	AMD	9555	¶ 148-3
		9555C	1511-97
		9555M	1511-98
96L02	Fairchild	96L02C	251-16
		96L02M	251-17
96S02	Fairchild	96S02C	251-33
		96S02M	251-34
960	Signetics	TAA960	545-24
9600	AMD	9600C	250-156
		9600M	250-157
	Fairchild	9600C	250-160
		9600M	250-161
9601	AMD	9601C	250-141
		9601M	250-142
	Fairchild	9601C	250-143
		9601M	250-144
	ITT	ITT9601-1	250-145
		ITT9601-5	250-146
	Motorola	MC9601	250-148
	National	DM9601	250-150
	Raytheon	RF9601	250-152
9602	AMD	9602C	251-14
		9602M	251-15
	Fairchild	9602C	251-18
		9602M	251-19
	ITT	ITT9602-1	251-20
		ITT9602-5	251-21
	Motorola	MC9602	251-23
	National	DM9602	251-25
	NEC America	μPB9602	251-26
	Raytheon	RF9602	251-28
	Signetics	N9602	251-29
		S9602	251-30
96101	Fairchild	96101	234-33
		96101C	331-64
		96101M	332-2
96106	Fairchild	96106	336-7
9612	Fairchild	9612	¶ 109-7
		9612C	333-11
		9612EC	333-13
		9612M	333-12
9613	Fairchild	9613	¶ 109-7
		9613C	337-21
		9613M	337-22
9614	AMD	9614	¶ 105-9
		9614C	333-14
		9614M	333-15
	Fairchild	9614	¶ 109-7
		9614C	333-16
		9614M	333-17
9614	ITT	ITT9614-1	333-18
		ITT9614-5	333-19
	TI	9614C	333-20
9615	AMD	9615	¶ 105-9
		9615C	337-6
		9615M	337-7
	Fairchild	9615	¶ 109-7
		9615C	337-8
		9615M	337-9
	ITT	ITT9615-1	337-10
		ITT9615-5	337-11
	TI	9615C	337-12
9616	AMD	9616C	331-39
		9616M	331-40
	Fairchild	9616	331-41
			¶ 109-6
			¶ 109-7
		9616E	331-42
		9616M	331-43
9617	AMD	9617C	335-22
		9617M	335-23
	Fairchild	9617	¶ 109-6
			¶ 109-7
		9617C	335-24
9620	AMD	9620	¶ 105-9
		9620C	337-2
		9620M	336-56
	Fairchild	9620C	337-3
		9620M	336-57
9621	AMD	9621	¶ 105-9
		9621C	331-11
		9621M	331-12
	Fairchild	9621	331-13
		9621M	331-14
	Raytheon	RC9621	331-15
		RM9621	331-16
9622	Fairchild	9622C	337-36
		9622M	337-37
	Raytheon	RC9622	337-38
		RM9622	337-39
9624	Fairchild	9624C	254-1
		9624M	254-2
9625	Fairchild	9625C	253-179
		9625M	253-180
9626	Fairchild	9626	340-37
9627	Fairchild	9627	¶ 109-7
		9627C	337-33
		9627M	337-34
9628	Fairchild	9628	340-44
9634	Fairchild	9634	¶ 109-7
9635	Fairchild	9635	¶ 109-7
9636	Fairchild	9636	¶ 109-7
		9636C	331-1
		9636M	331-2
9637	Fairchild	9637	¶ 109-7
		9637C	336-50
		9637M	336-51
	TI	μA9637C	336-52
		μA9637M	336-53
9638	Fairchild	μA9638C	333-54
		μA9638M	333-55
		9638	¶ 109-7
	TI	μA9638C	333-56
		μA9638M	333-57
9640	Fairchild	9640	¶ 109-7
		9640C	256-89
			341-38
		9640M	256-90
			341-31
9641	Fairchild	9641C	256-91
			341-39
		9641M	256-92
			341-32
9642	Fairchild	9642C	341-44
		9642M	341-35
9643	**Fairchild**	**9643**	★ **652**
			343-116
		9643ARC	★ **652**
		9643ATC	★ **652**
		9643DC	★ **652**
		9643PC	★ **652**
		9643RC	★ **652**
		9643TC	★ **652**
9644	**Fairchild**	**9644**	★ **652**
			343-105
		9644ARC	★ **652**
9644	**Fairchild**	**9644ATC**	★ **652**
		9644RC	★ **652**
		9644TC	★ **652**
9645	Fairchild	9645	343-100
9646	Fairchild	9646	343-32
9647	Fairchild	9647	344-52
9648	Fairchild	9648	344-58
9660	AMI	S9660	558-160
9664	Fairchild	9664AC	326-104
		9664BC	326-105
		9664C	326-103
9665	Fairchild	9665	346-103
			548-49
9666	Fairchild	9666	346-119
			548-50
9667	Fairchild	9667	346-71
			548-51
9668	Fairchild	9668	346-90
			548-52
97C09	National	AM97C09C	313-69
97C10	National	AM97C10C	313-76
97C11	National	AM97C11C	313-31
97C12	National	AM97C12C	313-42
970	Fairchild	TBA970	546-38
			561-159
	Signetics	TAA970	545-133
9702	AMD	9702-1	1004-37
9709	National	AM9709C	313-70
9710	National	AM9710C	313-77
9711	National	AM9711C	313-32
9712	National	AM9712C	313-43
980	Signetics	TCA980	545-134
9818	TI	SBP9818C	1023-13
		SBP9818M	1023-14
99	**AMI**	**EVK-99**	★**1544**
	National	AF99	598-174
			612-29
990	Fairchild	TBA990	559-177
	National	TBA990	560-7
	Plessey	TBA990	560-37
	Signetics	TBA990	560-79
	Telefunken	TBA990	560-105
9900	**AMI**	**S9900**	★**1575**
			1512-117
			1515-1
	TI	SBP9900	1512-119
			1532-2
		TMS9900	1512-120
			1534-1
			¶ 145-17
			¶ 145-18
			¶ 152-12
			¶ 152-14
9901	**AMI**	**S9901**	★**1577**
			1512-149
	TI	TMS9901	1512-150
9902	**AMI**	**S9902**	★**1579**
			1512-157
	TI	TMS9902	1512-159
9903	**AMI**	**S9903**	★**1581**
			1512-153
	TI	TMS9903	1512-154
9904	AMI	S9904	1512-128
	TI	TIM9904	1512-131
9905	AMI	S9905	1512-134
	TI	TIM9905	1512-138
9906	AMI	S9906	1512-161
	OEI	9906	565-43
			585-48
	TI	TIM9906	1512-164
9907	AMI	S9907	1512-141
	TI	TIM9907	1512-143
9908	OEI	9908	565-45
			568-8
			588-21
	TI	TIM9908	1512-146
991	Siemens	TAA991	554-56
9910	OEI	9910	545-29
			563-42
9911	OEI	9911	545-38
			563-24
9912	OEI	9912	565-7
			565-26
			568-23
			587-37
9916	OEI	9916	565-35
9916	OEI	9916	568-4
			587-45
9940	**AMI**	**S9940**	★**1583**
			1512-123
	TI	TMS9940	1512-124
		TMS9940E	1512-126
9963	OEI	9963	545-32
			563-2
9972	TI	TMS9972	1512-166
9980	**AMI**	**S9980**	★**1585**
			1512-118
			1515-2
	TI	TMS9980	1512-121
			1534-2
9996	AMI	S9996	1020-8

PART NUMBER GUIDE

Each IC manufacturer has his own unique method at identifying products, usually through a system of logos, device number prefixes and suffixes. This Part Number Guide is arranged alphabetically by manufacturer and describes each company's part number system. JAN nomenclature is also covered.

Manufacturer	Part Number — Prefix	Part Number — Suffix	Example

ADVANCED MICRO DEVICES



Note: Alternate source devices follow original manufacturer's part number and marking system.

Prefix

Functional Group
- **25** MSI
- **26** Computer Interface
- **27** Bipolar Memory
- **28** MOS
- **29** Bipolar Microprocessor
- **90** MOS
- **91** MOS
- **92** MOS
- **94** MOS
- **95** MOS

Type
- **L** Low Power
- **S** Schottky
- **LS** Low Power Schottky
- **(Blank)** Standard

Suffix

Package
- **D** Hermetic DIP
- **P** Molded
- **F** Flat
- **X** Dice

Temperature Range
- **C** Commercial
- **M** Military

Example

Prefix	Device	Suffix
AM25	S 05	D M

AM25 — Functional Group; S — Type; 05 — Device Number; D — Package; M — Temperature Range

AMERICAN MICROSYSTEMS

AMI®

Prefix

Family
- **S** Standard

Suffix

Package Type
- **1** Plastic
- **2** Cer-DIP
- **3** SLAM
- **4** Ceramic (Three Layer)
- **5** TO Type

Package/Pins
- **C** 22 Pin Plastic or Cer-DIP
- **D** 14 Pin Plastic or Ceramic
- **F** 12 Pin TO
- **H** 16 Pin Cer-DIP, SLAM, or Ceramic
- **I** 28 Pin Cer-DIP or SLAM
- **L** 24 Pin Cer-DIP or SLAM
- **M** 40 Pin SLAM
- **P** 18 Pin Plastic or Cer-DIP
- **T** 40 Pin Plastic
- **U** 16 Pin Plastic
- **W** 24 Pin Plastic
- **Z** 28 Pin Plastic

Example

Prefix	Device	Suffix
S	1103X	2 P

S — Family; 1103X — Version; 2 — Package Type; P — Number of Pins

ANALOG DEVICES

ANALOG DEVICES

Prefix

AD Analog Devices

Suffix

Temperature Range
- **A,B,C** Industrial Range
- **J,K,L** Commercial Range
- **S,T,U** Military Range

Package
- **D** 8 Pin Ceramic DIP
- **DN** Ceramic DIP
- **F** Ceramic Flatpack
- **H** TO-5 Type Can
- **N** Plastic DIP

Example

Prefix	Device	Suffix
AD	7516	JN

JN — Temperature Range; Package

BECKMAN INSTRUMENTS

Beckman

BECKMAN

Prefix

Family (Model Number)
- 801-809, 851-859 Voltage Regulators
- 811-816, 862, 863 Ladder Networks
- 822, 823, 833, 866 Amplifiers
- 840 Voltage References
- 845-872, 877 D/A Converters
- 873, 876 A/D Converters
- 882, 883 Active Filters

Suffix

Package Type
- **M** Metal
- **C** Ceramic
- **G** Glass

Version (Function)
- **I** Current
- **V** Voltage

Accuracy Level
- **D1** Best Level
- **D2**

Example

Prefix	Device	Suffix
877-	85	MV- D1

877- — Family; 85 — Model No.; MV- — Package Type; V — Version (Function); D1 — Accuracy Level

BURR-BROWN

BURR-BROWN

Prefix

Temperature
- **H, J, K, L** 0°C to +75°C
- **R, S, T** −55°C to +125°C
- **A, B, C** −25°C to +85°C

Suffix

Package
- **M** Metal
- **P** Plastic
- **Q** MIL-883 Screening

Example

Prefix	Device	Suffix
	3532	AMQ

AM — Temperature Range; Q — Package; MIL-883 Screening

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Manufacturer	Part Number: Prefix	Part Number: Suffix	Example

DATEL SYSTEMS

Family
- **ADC** A/D Converters
- **AM** Amplifiers
- **DAC** D/A Converters
- **DAS** Data Acquisition System
- **FLT** Filters
- **MV, MX** Multiplexer
- **SHM** Sample-Hold
- **VF** Voltage to Freq. Converters

Package — Monolithic
- **1** 14 Pin DIP
- **2** TO-99

Seal — Hybrid
- **G** Epoxy
- **M** Hermetic

Temperature
- **C** 0°C to 70°C
- **M** −55°C to 125°C
- **R** −25°C to +85°C

Prefix	Device	Suffix
AM	490	2 A
DAC	HZ12B	G C

Package — Selection — Seal — Temperature

ELECTRONIC ARRAYS

Note: Alternate source devices follow original manufacturer's part number and marking system.

Family
- **10** Static Shift Register
- **12** Dynamic Shift Register
- **15** N Channel ROM
- **20** Keyboard Encoder
- **3X** Dynamic ROM
- **4X** Static ROM

Package
- **D** Hermetic DIP
- **F** Flat Pack
- **P** Molded DIP
- **T** TO-Can
- **X** Dice

Temperature Range
- **C** 0° to 70°C
- **I** −55°C to 85°C
- **L** −55°C to 100°C
- **M** −55°C to 125°C
- **X** Other

Prefix	Device	Suffix
EA	1500A	DM

Family — Package — Temperature Range

EMM/SEMI

A. Semi Product

Special Application
- **B** Reduced Power Supply Level Operation
- **L** Very Low Power Operation
- **M** MIL-STD-883, Condition B

Electrical Variation
- **U** Standard
- **A** Variation A
- **B** Variation B, etc.

Temperature Range
- **C** 0°C to +70°C
- **D** 0°C to +70°C Plus 168 Hour Supplemental Burn-in
- **M** −55°C to +125°C Plus 168 Hour Supplemental Burn-in
- **S** −35°C to +85°C Plus 168 Hour Supplemental Burn-in

Package
- **A** DIP, Ceramic, 18 Pin
- **B** DIP, Plastic, 18 Pin
- **C** DIP, Ceramic, 22 Pin
- **D** DIP, CERDIP, Ceramic, 22 Pin
- **E** DIP, CERDIP, Ceramic, 18 Pin
- **G** Chip Carrier, Ceramic, Leadless, 22 Pin
- **P** DIP, Plastic, 22 Pin

Prefix	Device	Suffix
M	4200	UCC

Special Application — Electrical Variation — Temperature Range — Package

B. General Instrument

Second Source Marking

Family
- **RO** ROM
- **RA** RAM

Prefix	Device
SEMI	RA-3-4256

Family — Package

EXAR INTEGRATED SYSTEMS

XR Exar

Grade
- **C** Commercial
- **M** Military (Ceramic package and −55°C to 125°C)
- **( )** The absence of C or M Indicates a Commercial Part with Tighter Specs

Package
- **D** Dice
- **P** Plastic
- **N** Ceramic
- **T** TO-99, TO-100, TO-101 Metal Can

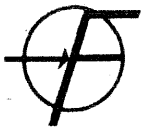
Prefix	Device	Suffix
XR	567	CP

Grade — Package

Part Number

Manufacturer	Prefix	Suffix	Example

FAIRCHILD



FAIRCHILD

F Fairchild
SH Hybrid
μA Linear

Package
C Chip (Dice)
D Ceramic DIP
E Plastic Can
F Flat Pac
H Metal Can
J Metal Power Package (TO-66)
K Metal Power Package (TO-3)
P Plastic DIP
R Ceramic Mini DIP
T Plastic Mini DIP
U Power Package (Molded, TO-220)
W Plastic TO-92

Temperature — Check Device Data for Specific Values
C 0°C to 70°C/75°C (CMOS −40°C to 85°C)
L MOS −55°C to 85°C, Hybrid −20°C to 85°C
M −55°C to 85°C/125°C

Prefix	Device	Suffix
μA	741	AHM

Electrical Class (if used)
Package
Temperature

Note: Alternate source devices follow original manufacturer's part number and marking systems.

FUJITSU



FUJITSU LIMITED

MB Micro Block
MBM Micro Block Modified and Industry Standard Numbers

Speed
N Slowest
E
H
Y Fastest

Package
C Ceramic
M Molded (Plastic)

Prefix	Device	Suffix
MB	8227	E M

Speed
Package

GENERAL INSTRUMENT



Designation
CU Array
AY Array
DL Shift Register Dynamic ≥ 50 Bits
DS Shift Register Dynamic < 50 Bits
LC Linear Circuit
LG Logic Cells
MEN N and P Channel FETs
MU Multiplexer
RA RAM
RO ROM
SL Shift Register Static ≥ 50 Bits
SS Shift Register Static < 50 Bits

Temperature and Processing
0 MTOS −55°C to 85°C
1 MTOS 0°C to 70°C
4 N Channel
5 MTNS 0°C to 70°C
6 −55°C to 125°C
7 MTNS
8 Silicon Gate −55°C to 125°C
9 Silicon Gate 0°C to 70°C

Description — Multiplexers
WX Indicates Typical R_{ds}(on) In Hundred Ohms Steps:
01 ≤ 100 ohms
02 < 200 ohms
03 ≤ 300 ohms, etc.
YZ Total Number of Channels

Custom
Custom Number Assigned

Package Identification (Not Marked on Package)
01 Dice
12 8 Lead DIP
14 TO-5 4 Lead
15 TO-78 8 Lead
16 TO-5 8 Lead
17 TO-5 8 Lead High Profile
21 TO-5 10 Lead
22 TO-5 10 Lead Isolated
23 TO-100 10 Lead
29 24 Lead Plastic DIP
30 14 Lead Plastic DIP
31 16 Lead Plastic DIP
32 24 Lead Plastic DIP
33 40 Lead Plastic DIP
35 36 Lead Plastic Flat Pack
51 TO-8 12 Lead Low Profile
55 16 Lead DIP
60 10 Lead Flat Pack
61 14 Lead Flat Pack
62 16 Lead Flat Pack
63 20 Lead Flat Pack
64 24 Lead Flat Pack
65 40 Lead Flat Pack
66 36 Lead
68 44 Lead Flat Pack
69 14 Lead DIP
71 16 Lead DIP
72 24 Lead DIP .6 MIL Centers
73 24 Lead DIP .5 MIL Centers
74 40 Lead DIP .6 MIL Centers
75 40 Lead DIP 1.05 MIL Centers
76 28 Lead DIP
77 18 Lead DIP

Prefix	Device	Suffix
RO-6	WXYZ	(XX)

Desig-nation
Temp. and Processing
Description
Package Identification

(Continued)

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Manufacturer	Part Number Prefix	Part Number Suffix	Example

GENERAL INSTRUMENT (cont)

ROM/RAM
WXYZ Total Number of Bits

Shift Registers
W Indicates the Number of Redundant Configurations:
1 Single 3 Triple
2 Dual 4 Quad, etc.
XYZ Total No. of Bits per Configuration

Arrays/Linear/Logic
WXYZ Arbitrary Number Assigned

79 24 Lead DIP .6 MIL Centers
80 14 Lead Ceramic RIP
81 16 Lead Ceramic DIP

HARRIS

Family
A Analog
D Digital
I Interface
M Memory

Package
1 DIP
2 TO-5 Type
3 Plastic DIL
7 Mini DIP
9 Flat Pack
0 Chip Form

Exceptions
HPROMX-0152-X
HPROMX-1024-X
HPROMX-8256-X

Temperature Range
2 −55°C to 125°C
4 −25°C to 85°C
5 0°C to 75°C
6 25°C Probe (Dice only)
8 Dash 8 Program, MIL-STD-883, Class B — Example: HA-2700-8
9 −40°C to 85°C

Exceptions
The 54C/74C CMOS Family Temperature Designation is Contained in the Part Number

Example:
54CXX −55°C to 125°C
74CXX −40°C to 85°C

Prefix	Device	Suffix
HM1	7620	5

Family
Package
Temperature Range

HUGHES AIRCRAFT

Prefix
H Standard
S Special

Family
CMP Microprocessor
CTR Counter
CUS Custom
DSR Dynamic Shift Register
SSR Static Shift Register
SUB Subsystem
MUL Multiple
DIG Discrete Insulated Gate
DGP Discrete General Purpose
DSW Discrete Switch
PLA Programmable Logic Array

Package
D Cerdip or Ceramic DIP
F Flat Pack
P Plastic DIP
T TO

Prefix	Device	Suffix
HCTR	0320	D

Family
Package

INTEL

Package
B CerDIP (Ceramic or Window Lid) (Hermetic)
C Ceramic (Metal Lid) DIP (Hermetic)
D CerDIP (Glass Seal) DIP (Hermetic)
P Plastic DIP
M Metal Can Package (Hermetic)
On military temperature devices /B indicates MIL-STD-883 level B processing; /C, level C processing.

Prefix	Device	Suffix
P	5101	L
C	8080	A
MD	3601	/C

Military Temp.
Package
Suffix

INTERNATIONAL MICROCIRCUITS

MM Master MOS Array
SCC Special Custom Circuit

Family
1 Small Chip
2 Special Size
3 Medium Chip
6 Large Chip

Package
C Ceramic
P Plastic DIP
S Special

Prefix			Suffix
MM 6	013	B-P	28

Family
Metal Option
Change Level
Package
No. of Pins

(Most ICs are custom and are marked only with the purchaser's marks)

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Manufacturer	Part Number Prefix	Part Number Suffix	Example

INTERSIL

A. Hybrid

Temperature
- C 0°C to 70°C
- M −55°C to 125°C

Package
- B Interpack
- D Dual-In-Line Package Ceramic
- E Small TO-8 Type
- F Flat Package, Ceramic
- G TO-8 Type
- H Flat Package, Silicon
- I 16 Pin DIP (0.6 x 0.7 Lead Space)
- J Dual-In-Line Cerdip
- L Leadless Ceramic
- P Dual-In-Line Package, Plastic
- T TO-5 Type
- DR TO-72 with No. 4 Lead Connected to Case

Pins (No. of)

H	6	F	22
A	8	G	24
B	10	I	28
C	12	J	32
D	14	K	36
E	16	L	40
N	18	M	48

- V 8, .230" Pin Circle
- W 10, .230" Pin Circle
- Y 8, No. 4 Lead Connected to Case
- Z 10, No. 5 Lead Connected to Case

Prefix	Device	Suffix
DG	126A	M D D

Analog Gate
Temperature
Package
No. of Pins

Characteristics
- 5 Analog
- 7 Digital
- 9 Interface

General Type
- 0 Gates
- 1 Amplifiers
- 2 Clock Drivers
- 3 D/A and A/D

Temperature (See First Example)

Package (See First Example)

Pins (See First Example)

Prefix	Device	Suffix
IH 5	0 01 C	P A

Intersil
Hybrid
Character-istics
General Type
Temperature
Package
No. of Pins

B. Linear, Low Power, Watch and Clock Circuits

Intersil
- I
- IC

Circuits
- L Linear
- CM Watch, Clock

Temperature
- C Commercial (0°C to 70°C)
- I Industrial (−20°C to 70°C)
- M Military (−55°C to 125°C)

Package (See First Example)

Pins (See First Example)

Prefix	Device	Suffix
IC L	8001	C T Z

Intersil
Circuit
Temperature
Package
No. of Pins

C. Memory Circuits

Process
- 5 Bipolar
- 6 CMOS

General Type
- 0 Drivers
- 1 Processing Element
- 2 Field Programmable Logic Array (FPLA)
- 3 Read Only Memory (ROM)
- 4 Interface Element
- 5 Random Access Memory (RAM)
- 6 Programmable Read Only Memory (PROM)
- 7 Shift Register

Bipolar Process (Only)
- S Schottky
- — Gold Doped

Temperature
- C Commercial (0°C to 70°C)
- I Industrial (−40°C to 70°C)
- M Military (−55°C to 125°C)

Package (See First Example)

Pins (See First Example)

Speed Select
- **Alpha** Bipolar and CMOS
- **Numerical** MOS

Prefix	Suffix
I M 5 5 S 08	ACJ E

Intersil
Memory
Circuit
Process
General Type
Bipolar Process (only)
Specific Type
Speed Select
Temperature
Package
No. of Pins

ITT SEMICONDUCTORS

- ITT
- SAA
- SAJ
- SAY
- TAA
- TBA
- TCA
- TDA

Temperature Range
- 1 −55°C to 125°C
- 5 0°C to 70°C

Package
- B Flat Package
- C TO-5 Style
- D Ceramic DIP
- J Ceramic DIP
- N Plastic DIP

Prefix	Device	Suffix
ITT	9316	1D

Temperature Range
Package

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Manufacturer	Part Number: Prefix	Part Number: Suffix	Example

JAN NOMENCLATURE

Prefix
- **J** **JAN** Qualified Device
- **M38510** Military Designation

Device
The "Slash" numbering signifies the specification and specifies the device type. See Military Parts Directory.
Note: The J or JAN prefix is very important. If it is not there it is not a JAN device.

Device Class
- **A** Missiles and Manned Spacecraft
- **B** General Military
- **C** Less Critical Military Applications

Case Outline
- **A** ¼″ x ¼″ Flat Pack, 14-Pin
- **B** ⅛″ x ¼″Flat Pack, 14-Pin
- **C** ¼″ x ¾″ Dual-In-Line, 14-Pin
- **D** ¼″ x ⅜″ Flat Pack, 14-Pin
- **E** ¼″ x ¾″ Dual-In-Line, 16-Pin
- **F** ¼″ x ⅜″ Flat Pack, 16-Pin
- **G** 8-Lead Can
- **H** ¼″ x ¼″ Flat Pack, 10-Lead
- **I** 10-Lead Can
- **J** ½″ x 1¼″ Dual-In-Line, 24-Pin
- **K** ⅜″ x ½″ Flat Pack, 24-Pin
- **L** ⅜″ x ½″ Flat Pack, 24-Pin
- **Z** ¼″ x ⅜″ Flat Pack, 24-Pin

Lead Finish
- **A** Kovar or Alloy 42, with Hot Solder Dip
- **B** Kovar or Alloy 42, with Bright Acid Tin Plate
- **C** Kovar or Alloy 42, with Gold Plate

Prefix	Device	Suffix
JM38510	/XXXXX	B C B

Device Class
Case Outline
Lead Finish

LAMBDA

- **L** Overvoltage Regulator
- **LAS** Regulator
- **PM** Switching Transistor
- **PMD** Discrete
- **PMR** Dual Rectifier

Prefix	Device	Suffix
LAS	14	12

Voltage

MASTER LOGIC

Family
- **ML** CMOS Gate Array
- **MLA** CMOS Custom
- **F** Other

Gate Capacity
- **50** 50 Gates
- **75** 75 Gates
- **100** 100 Gates
- **150** 150 Gates
- **200** 200 Gates

Package
- **P** Plastic
- **CD** CerDIP
- **SB** Side Brazed

Pins
By Count

(Most ICs are marked with ML prefix as well as purchaser's marks)

Prefix	Device	Suffix
ML	150	P-24

Family
Gate Capacity
Package
Pins

MICRO COMPONENTS

MCC Micro Components
- **D** Diode Flip Chip
- **N** NPN Flip Chip
- **P** PNP Flip Chip

Package
- **O** Loose Component
- **D** Dual-In-Line
- **P** "Pill," Small Round Package
- **T** TO-Can
- **4** 4 Leads
- **8** 8 Leads

Circuit Style
- **B** National Dual Source
- **S** Signetics Dual Source

(ICs are marked with **MCC** prefix)

Prefix	Device	Suffix
MCC	122	OD8
MCC	555	B
D	823	

Package/Circuit

MICRO NETWORKS

MN Micro Networks

Temperature Range
- **(No Suffix)** 0°C to 70°C
- **E** −55°C to 85°C
- **H** −55°C to 125°C
- **B** Processing to 883A Method 5004.2

Prefix	Device	Suffix
MN	3000	H B

Temperature Range
Processing

MICRO POWER SYSTEMS

MP Micro Power

Prefix	Device	Suffix
MP	7520	T D 0025

Level of Performance
Package
Special Processing

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Manufacturer	Part Number: Prefix	Part Number: Suffix	Example

MITEL SEMICONDUCTOR

Description
- **MA** Linear
- **MT** Digital
- **MS** Telecom
- **MD** Custom
- **SIL** Siltek CMOS

Version
- **A** Modified Version, Unilaterally Interchangeable with Unlettered Version.
- **B** Unilaterally Interchangeable with A and Unlettered Versions.

Package Style, Temperature Range:
- **C** Frit Seal Ceramic DIP, −40°C to 85°C
- **D** White Ceramic DIP, −55°C to 125°C
- **E** Plastic DIP, −40°C to 85°C
- **F** Frit Seal Ceramic DIP, −55°C to 125°C
- **H** Plated Chip, −40°C to 85°C
- **I** Plated Chip, −55°C to 125°C
- **J** Ceramic DIP, 24-Leads
- **K** Ceramic, Flat Pack
- **L** Ceramic DIP, 28-Leads
- **M** Ceramic DIP, 40-Leads
- **N** Plastic DIP, 24 Leads
- **O** Plastic DIP, 28-Leads
- **S** Plastic DIP, 40-Leads
- **W** Wafer, Probe Tested

MIL Process Option
- **B** MIL-883, Class C Plus 168 Hr. Burn-In
- **R** High-Reliability Plastic DIP

Prefix	Device	Suffix
SIL	4098	BER

Version
Package/Temperature
MIL Process Option

MITSUBISHI

M Mitsubishi

Temperature
- **5** Industrial/Commercial
- **9** Military

Series

1 Linear Circuit	**45** TTL
17 Linear Circuit	**46** TTL
3 TTL	**47** TTL
32 TTL	**81** MOS
33 TTL	**85** MOS
43 TTL	**86** MOS
44 TTL	**9** DTL

Package
- **E** Plastic-Sealed Metal DIL
- **K** Glass-Sealed Ceramic DIL
- **L** Plastic-Molded SIL
- **P** Plastic-Molded DIL
- **S** Metal-Sealed Ceramic DIL
- **T** Can-Sealed Glass Metal
- **Y** Can-Sealed Glass Metal

Prefix	Device	Suffix
M 5 1	99	A Y

Temp.
Series
Version
Package

MONOLITHIC MEMORIES

MMI

Temperature
- **5** Military TTL
- **6** Commercial TTL

Type
- **0** Character Generator
- **2** ROM
- **3** PROM
- **5** RAM
- **7** Computer Logic

Package
- **D** Ceramic
- **F** Flat Pack
- **J** CERDIP
- **N** Plastic
- **W** Ceramic

Prefix	Device	Suffix
5 2	05	D

Temp.
Type
Package

MOSTEK

MOSTEK

MK Mostek

Package
- **E** Leadless Chip Carrier
- **F** Flat Ceramic Package
- **K** Tin Plated Frit-Sealed Ceramic
- **N** Plastic Dual-In-Line
- **P** Ceramic Dual-In-Line
- **T** Ceramic Dual-In-Line with Transparent Lid

Prefix	Device	Suffix
MK	4096	P

Package

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Manufacturer	Part Number: Prefix	Part Number: Suffix	Example

MOTOROLA

"The circle is not used in marking ICs."

Description

- **MC** Packaged Integrated Circuits
- **MCB** Packaged Beam-Lead Integrated Circuits. (Followed by F Suffix When in Flat Pack)
- **MCBC** Beam-Lead Integrated Circuit Chips Unencapsulated Integrated Circuit Chips
- **MCC** Unencapsulated Integrated Circuit Chips
- **MCCF** Flip-Chip Linear Integrated Circuits
- **MCE** Dielectrically Isolated Integrated Circuits
- **MCM** Integrated Circuit Memories
- **LM** Pin-for-Pin Equivalent to Linear Integrated Circuits Made by National Semiconductor
- **MMS** Memory Systems

Package

- **F** Flat Ceramic Package
- **G** Metal Can Package (TO-5 Types)
- **K** Metal Power Package (TO-3 Types)
- **L** Ceramic Dual-In-Line Case
- **P** Plastic Package
- **PQ** ICs Packaged In Staggered-Lead Plastic DIP Packages
- **R** Metal Power Packages (TO-66 Types)
- **U** Ceramic Package

Prefix	Device	Suffix
MC	14510	L

Description

Package

NATIONAL

DEVICE NUMBER (for Digital Devices):
CDXXXX-CMOS —
C Suffix −40°C to 85°C,
M Suffix −55°C to 125°C.

DM54XX — All numbers beginning with 5 denote −55°C to 125°C temperature operation.

DM74XX — If the "74" is indicated, the operating temperature is 0°C to 70°C.

DM7XXX — All other numbers beginning with 7 (besides the "74" shown above) are NSC proprietary products and a 7 here indicates −55°C to 125°C.

DM8XXX — All numbers beginning with 8 denote 0°C to 70°C temperature operation.

Description

- **AD** Analog to Digital
- **AH** Analog Hybrid
- **AM** Analog Monolithic
- **CD** CMOS
- **DA** Digital to Analog
- **DH** Digital Hybrid
- **DM** Digital Monolithic
- **DS** Digital Special
- **LFT** Linear FET Monolithic
- **LH** Linear Hybrid
- **LM** Linear Monolithic
- **LX** Transducer
- **MA** Module
- **MH** MOS Hybrid
- **MM** MOS Monolithic

Form

- **C** Complete
- **B** Building Block
- **D** Digital Panel Meter Chip
- **M** Module
- **S** Card Systems

Resolution

- **08** 8 Bits
- **10** 10 Bits
- **12** 12 Bits
- **25** 2½ Digit
- **35** 3½ Digit
- **37** 3¾ Digit
- **45** 4½ Digit

Linear Devices
With proprietary linear circuits, a 1-2-3 numbering system is employed.
The 1 denotes a Military temperature range device (−55°C to 125°C), the 2 denotes an Industrial device (−25°C to 85°C), and the 3 denotes a Commercial device (0°C to 70°C). i.e. LM101/LM201/LM301. Exception to this are the LM1800 Series; some hybrid circuits which employ a "C" Suffix; and second-source products which follow the original manufacturers numbering system.

Characteristics

- **A** Improved Electrical Specs
- **C** Reduced Temperature Range

Package

- **D** Glass/Metal DIP
- **F** Flat Pack (0.25" Wide)
- **G** TO-8 (12 Lead) Metal Can
- **H** TO-5 (Multi-Lead) Metal Can
- **J** Glass/Glass
- **K** TO-13 Power Pack
- **M** Wide Trak Power Pack
- **N** Molded DIP
- **P** TO-202 Plastic Power Pack
- **R** Low Temperature Ceramic Pack
- **S** 14 Lead Power Pack SGS Power Pack
- **T** TO-220 Plastic Power Pack
- **W** Flat Pack (0.275" Wide)
- **Z** TO-92

Technology

- **P** PMOS
- **C** CMOS
- **H** Hybrid
- **B** Bipolar
- **N** NMOS
- **L** Linear
- **I** I^2L

Prefix	Device	Suffix
AD C	08 00	P C N

Converter Products:

Form

Resolution

More Than One in Family

Technology

Temperature Range

Package

Prefix	Device	Suffix
LM	101	A F

Characteristics

Package

NEC

μP Micropackage Family

- **A** Discrete
- **B** Digital Bipolar
- **C** Linear
- **D** Digital CMOS

Package

- **C** Plastic
- **D** Ceramic or CerDIP

Prefix		Suffix
μP F	xxxxx	P S

Family

Package

Modification

Part Number

Manufacturer	Prefix	Suffix	Example

NITRON

(ICs are identified by the **NC** prefix)

Description
- **NC** Packaged ICs
- **NCM** Packaged Memory ICs
- **NIT** Memory Modules

NC	7010	
Prefix	Device	Suffix

Description

NORTEC

NORTEC

- **NE** Nortec Electronics
- **NE** 6003BZD
- **NE** 1103-146D

Electrical Selections
- **11**
- **BZ** Electrical Selections
- **146**
- **etc.**

Package
- **D** Ceramic DIP
- **F** Flatpack
- **H** Metal Can
- **J** CerDIP
- **N** Molded DIP
- **P** 8-Pin DIP
- **Y** Dice

Prefix	Device	Suffix
NE	6003	11 D

Electrical Selections

Package

PANASONIC (MATSUSHITA)

MATSUSHITA

Description
- **AN** Analog
- **DN** Digital Bipolar
- **J** Development Type
- **MN** MOS

Prefix	Device
DN	830

PLESSEY

(All ICs are marked **PLESSEY**)

Description
- **ML** MOS Linear (w/Gate Protection)
- **MP** MOS Digital
- **MT** MOS Linear (without Gate Protection)
- **NOM** MNOS Memory Elements and Arrays
- **SAA, SBA** Alternate Sourced Consumer Devices
- **SL** Bipolar Linear
- **SP** Bipolar Digital

Package
- **CM** Multilead TO-5
- **DC** Dilmon
- **DG** Ceramic Dual-In-Line
- **DP** Plastic Dual-In-Line
- **EP** Power Stud
- **FM** Ten Lead Flatpack
- **GM** Fourteen Lead Flatpack
- **KM** TO-3
- **QG** Ceramic Quad-In-Line
- **QP** Plastic Quad-In-Line
- **RP** Power Findip
- **SP** Plastic Single-In-Line

Prefix	Device	Suffix
SP	8735B	DG

Description

Package

PRECISION MONOLITHICS

PMI

Description
- **AD** Analog to Digital Converter
- **CMP** Voltage Comparator
- **DAC** Digital to Analog Converter
- **MAT** Matched Transistors
- **MUX** MUX Analog Multiplexer
- **OP** Operational Amplifier
- **PM** Second Source Devices
- **REF** Voltage Reference
- **SMP** Sample and Hold
- **SSS** Second Source Devices

Package (Last Alphabetical Character)
- **H** 6-Pin TO-78
- **J** 8-Pin TO-99
- **K** 10-Pin TO-100
- **L** 10-Pin Flatpack
- **M** 14-Pin Flatpack
- **N** 24-Pin Flatpack
- **P** 8-Pin Plastic Mini DIP
- **Q** 16-Pin Hermetic DIP
- **V** 24-Pin Hermetic DIP
- **X** 18-Pin Hermetic DIP
- **Y** 14-Pin Hermetic DIP

Prefix	Device	Suffix
DAC	01	C Y

Grade

Package

PRO ELECTRON

First Two Letters

Digital
- **FA - FZ**
- **GA - GZ** Identify the Family
- **etc.**

Solitary Circuits
- **S** Solitary Circuit
- **T** Analog Circuit
- **U** Mixed Analog/Digital

(The second letter has no special significance, except H means Hybrid.)

Third Letter

Temperature Range
- **A** Temp. Range not specified below
- **B** 0°C to +70°C
- **C** −55°C to +125°C
- **D** −25°C to +70°C
- **E** −25°C to +85°C
- **F** −40°C to +85°C
- **G** −55°C to +85°C

Suffix or Version Letter (Recommended)

Single Letter
- **C** Cylindrical
- **P** Plastic DIL
- **D** Ceramic DIL
- **Q** Quad-In-Line
- **F** Flat Pack
- **U** (Uncased) Chip

Other letters have no fixed meaning except Z means customized wiring.

Two Letters

First Letter: General Shape
- **C** Cylindrical
- **D** Dual-In-Line (DIL)
- **E** Power DIL (with External Heat Sink)
- **F** Flat (Leads on 2 Sides)
- **G** Flat (Leads on 4 Sides)
- **K** Diamond (TO-3 Family)
- **M** Multiple-In-Line (Except Dual-, Triple-, Quad-In-Line)
- **Q** Quad-In-Line (QUIL)
- **R** Power QUIL (with External Heat Sink)
- **S** Single-In-Line (as TO-127 or TO-220)
- **T** Triple-In-Line

Prefix	Device	Suffix
GFB	7400	-DP
GMB	74LS00A	-DC
SAC	2000	
TDA	1000	P

(Continued)

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Manufacturer	Part Number: Prefix	Part Number: Suffix	Example

PRO ELECTRON (cont)

If a circuit is designed for a wider temperature range, the letter indicating a narrower temperature range or the letter "A" can be used.

Device or Serial Number
Either a 4-digit number assigned by PRO ELECTRON or the serial number (even a combination of figures and letters) of an existing type designation which can be extended to a minimum of a 4-digit number by adding zeros in front of it.

Second Letter: Material
- **C** Metal-Ceramic
- **G** Glass-Ceramic (cerDIP)
- **M** Metal
- **P** Plastic

RAYTHEON SEMICONDUCTOR

Temperature
- **LH1, LM1** −55°C to 125°C
- **LH2, LM2** −25°C to 85°C
- **LH3, LM3** 0°C to 70°C
- **RC** 0°C to 70°C
- **RM** −55°C to 125°C
- **RV** −40°C to 85°C
- **54** −55°C to 125°C
- **74** 0°C to 70°C
- **MAX-xxxx-2** −55°C to 125°C
- **MAX-xxxx-5** 0°C to 70°C

HA Series
- **HA1** 14-Pin Ceramic DIP
- **HA3** 14-Pin Plastic DIP

Microcomputer Components
- **AM**
- **R**
- **93**

Package

Most Devices
- **BM** 16-Pin Epoxy-B DIP
- **CH** Gold-Backed Chip, Visually Inspected to MIL-STD-883A, Method 2012, and Packaged in Waffle Pack.
- **CJ** 14-Pin Ceramic Flatpak
- **CL** 16-Pin Ceramic Flatpak
- **CK** 14-Pin Ceramic Flatpak
- **D** 14-Pin Metal DIP
- **DB** 14-Pin Epoxy-B DIP
- **DC** 14-Pin Ceramic DIP
- **DD** 16-Pin Ceramic DIP
- **DE** 8-Pin Ceramic DIP
- **DM** 16-Pin Ceramic DIP
- **DZ** 40-Pin Ceramic DIP
- **F** Flatpak
- **FV** 28-Pin Ceramic Flatpak
- **FZ** 42-Pin Ceramic Flatpak
- **H** 3, 8 or 10-Pin Metal Can
- **J** 14 or 16-Pin Ceramic DIP
- **K** TO-3 Power Pack
- **MB** 16-Pin Epoxy-B DIP
- **ML** 16-Pin Ceramic DIP, Side Brazed
- **MS** 20-Pin Ceramic DIP, Side Brazed
- **MZ** 40-Pin Ceramic DIP, Side Brazed
- **N** 24-Pin Glass/Metal Flatpak
- **N** Epoxy-B DIP (LM Series)
- **NB** 8-Pin Epoxy-B DIP
- **PS** 20-Pin Epoxy-B DIP
- **PU** 24-Pin Epoxy-B DIP
- **PV** 28-Pin Epoxy-B DIP
- **PZ** 40-Pin Epoxy-B DIP
- **Q** 10-Pin Flatpak (¼" x ¼")
- **R** 24-Pin Ceramic DIP
- **T** 3, 8, 10 or 12-Pin Metal Can
- **TK** 9-Pin TO-66 Power Pack
- **W** 14-Pin Ceramic Flatpak

Beam Lead Chip
- **BL**

HA Series
- **2** −55°C to +125°C
- **5** 0°C to +70°C
- **8** −55°C to +125°C

XR Series
- **M** Ceramic −55°C to +125°C
- **N** Ceramic −40°C to +85°C
- **P** Epoxy −40°C to +85°C
- **CN** Ceramic 0°C to +75°C
- **CP** Epoxy 0°C to +75°C

Prefix	Device	Suffix
54	153	DD
RC	4130	DB
LM	118	H
HA1	4741	5
XR	2207	CN

Prefix	Device	Suffix
AM	2901	D M B

Package
Temperature Range
Processing

(Continued)

Manufacturer	Part Number: Prefix	Part Number: Suffix	Example

RAYTHEON SEMICONDUCTOR (cont)

Raytheon ICs are identified by an **RAY** prefix to the date code.

Microcomputer Components Package
- **D** Hermetic DIP
- **F** Flatpak
- **P** Plastic DIP
- **X** Chip

Temperature
- **C** 0°C to +75°C
- **M** −55°C to +125°C

Process to MIL-M-883B
- **B**

RCA

RCA Solid State

Description
- **CA** Linear ICs
- **CD** Digital ICs
- **CDP** Microprocessor ICs
- **MW** MOS ICs

Version
- **A** Modified Version, Unilaterally Interchangeable with Prototype
- **B** Modified Version, Unilaterally Interchangeable with A Version, and with Prototype
- **C** Modified Version, Unilaterally Interchangeable with B, A, and Prototype Versions

Package
- **D** Ceramic DIP
- **E** Plastic DIP
- **F** Ceramic DIP, Frit Seal
- **G** Hermetic Chip in Plastic Package
- **H** Chip
- **K** Ceramic Flat Package
- **L** Beam-Lead Device
- **Q** Quad-In-Line Plastic Package
- **S** TO-5 Package with DIL-CAN
- **T** TO-5 Package

Prefix	Device	Suffix
CD	4070	BD

Version — BD
Package — BD

RETICON

RETICON®

Previous Products
- **RA** Area Array
- **RL** Linear Array
- **SAD** Serial Analog Delay
- **SAM** Serial Analog Memory
- **SAP** Serial Analog Processor
- **TAD** Tapped Analog Delay

New Analog Products
- **R5** Reticon Analog

Family
- **0** Complex Special Functions
- **1** Simple Delays
- **2** Tapped Delay
- **3** Analog Memory
- **4** Correlator
- **5** Multiplexer, Parallel to Serial Converter
- **6** Filters

Code
- No. of Columns and Lines
- No. of Elements
- No. of Storage Elements
- No. of Storage Elements
- No. of Storage Elements
- No. of Taps

Prefix	Device	Suffix
RA	50x50	A
RL	1024	C
TAD	12	

Code — 12
Revision — C

Prefix	Device	Suffix
R5 X	YY	A -1

Family — X
Revision (If Required) — A
Member of Device Type (If Required) — -1

ROCKWELL (COLLINS)

Rockwell

CRC Products

CRC Devices

Package
- **1** Ceramic DIP
- **2** Flatpack
- **3** Plastic DIP

Temperature
- **1** −55°C to 125°C
- **2** −25°C to 85°C
- **3** 0°C to 70°C

Prefix	Device	Suffix
CRC	1504	-1 -2

Package — -1
Temperature Range — -2

SANYO

Designation
- **LA** Bipolar Linear
- **LB** Bipolar
- **LC** CMOS
- **LM** PMOS

Prefix	Device
LA	1230

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Manufacturer	Part Number: Prefix	Part Number: Suffix	Example
SGS-ATES SEMICONDUCTOR	(Prefixes assigned by the European Association "PRO ELECTRON") **H** High Level Logic **HB** CMOS **L** Linear Professional **M** MOS **TAA** Linear Consumer **TBA** Linear Consumer **TCA** Linear Consumer **TDA** Linear Consumer		Prefix: TDA, Device: 1200
SIGNETICS	**Temperature** **LM** Linear IC — Alternate Source **N or None** 0°C to 70°C **N8** 0°C to 75°C **S(E)** −55°C to 125°C **SA** −40°C to 85°C **5400 Series** −55°C to 125°C **7400 Series** 0°C to 70°C	**Package** **N** 8, 14, 16, 18, 20, 22, 24, 28, 40 Lead DIL Plastic **F** 8, 14, 16, 18, 20, 22, 24 Lead Ceramic DIP **I** 8, 14, 16, 18, 22, 24, 28, 40, 50 Lead Ceramic DIP Side Brazed **W** 10, 14, 16, 24 Lead Ceramic Flat Pack **Q** 10, 14, 16, 24 Lead Ceramic Flat, Bottom Brazed **K** 10 Lead TO-100 Header, Low Profile **L** 10 Lead TO-100 Header Tall Can **T** 8 Lead TO-99 Header **DA** TO-3 Solid Header, Can **DB** TO-5 Solid Header, Can **R** 16, 18, 24, 28, 40 Lead Beryllia Flat Pack **S** TO-92 Plastic **U** TO-220, 3 Lead	Prefix: N, Device: 74123, Suffix: N Prefix: N, Device: 8X02, Suffix: N Temperature Package
SILICON GENERAL	**SG** Silicon General	**Characteristics** **A** Improved Electrical Specifications **C** Reduced Temperature Range **Package** **F** Flat Pack **J** 14, 16-Pin DIP (CerDIP) **K** TO-3 Power Pack **M** 8-Pin Plastic DIP **N** 14, 16-Pin Plastic DIP **T** TO-5 Metal Can (TO-39/99/100/101) **Y** 8-Pin DIP (CerDIP)	Prefix: SG, Device: 1524, Suffix: J Prefix: SG, Device: 108A, Suffix: T Characteristics Package
SILICONIX	**Description** **D** Driver for FET Switch **DF** Digital LSI **DGM** Driver with FET Switches (Monolithic Version of Hybrid Device) **G** Multi-Channel FET Switches **H** High Voltage (28V) Logic **L** Linear IC **LD** A/D Converter **LH** Hybrid Linear IC (2nd Source) **LM** Linear IC (2nd Source) **Si** 2nd Source Part **S** Power Logic Switch	**Temperature** **A** −55°C to 125°C **B** −20°C to 85°C **C** 0°C to 70°C **Package** **A** Metal Can **F** Flatpack **J** Plastic DIP **K** Ceramic DIP **L** Flatpack **P** Hermetic DIP **R** Hermetic DIP **MIL Process Option** **MIL-883, Class A** **2** MIL-883, Class B **3** MIL-883, Class C **4** In-House Screening Plus 168 Hr. Burn-In	Prefix: DG, Device: 200, Suffix: BA-X Temperature Package MIL Process Option
SOLID STATE SCIENTIFIC	**Reliability** **A** MIL-883-A **B** MIL-883-B **C** MIL-883-C **S** Standard **Other Letters** **CM** CMOS **C** Complementary **L** Logic **M** Memory	**Process** **A** AL Gate Bulk **B** High Voltage AL Gate **S** Silicon on Sapphire **Package** **C** Ceramic DIP **D** Ceramic DIP **E** Epoxy DIP **H** Chip **F** Flat Pack **T** TO-5	Prefix: SCL, Device: 4000, Suffix: AE+ Reliability Process Package Special Screening

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SOLITRON

CM CMOS

Package Style, Temperature Range
- **AD** Ceramic DIP, −55°C to 125°C
- **AE** Epoxy Encapsulated DIP, −40°C to 85°C
- **AF** CerDIP, −55°C to 125°C

Prefix	Device	Suffix
CM	4000	AD

Package/Temperature

SPRAGUE ELECTRIC

A. UC Series
UD Series
UG Series
UL Series

Family
- **C** CMOS
- **D** Display Drivers
- **G** Hall Effect Circuits
- **L** Linear Circuits

Temperature
- **N** Limited Temperature Range, −25°C to 70°C Typical
- **S** Extended Temperature Range

Package
- **A** Plastic DIP
- **B** Plastic DIP with Heat Sink Tabs
- **C** Chip
- **D** TO-99
- **E** 8-Pin Plastic DIP with Pins 1, 4, 5, 8 Only
- **F** TO-86 or 30 Lead Flat Package
- **G** TO-99
- **H** 9-Pin Hermetic DIP
- **J** TO-87
- **K** TO-100
- **L** TO-100
- **M** 8-Pin Plastic DIP
- **N** 14-Pin Plastic Quad-In-Line
- **P** Batwing DIP
- **Q** Batwing Quad-In-Line
- **R** 8-Lead DIP with Unformed Leads
- **S** 4-Pin SIP
- **T** 3-Pin SIP
- **W** TO-100 with Miniature Tube Base Adapter Base

Prefix	Device	Suffix
ULN	2111	A

Family
Temperature
Package

B. UH Series

Package
- **C** Hermetic Flatpack
- **D** Hermetic DIP
- **P** Plastic DIP

Prefix	Device
UHP	400

Package

STANDARD MICROSYSTEMS

Family
- **CG** Character Generator
- **COM** Communications
- **CRT** CRT Display
- **KR** Keyboard Encoding

Package
- **P** Plastic
- **C** Ceramic

Temperature
- **T** −25°C to 85°C
- **(Blank)** 0°C to 70°C

An H in the Suffix Indicates High Speed
A U in the Suffix Indicates Ultra High Speed

Prefix	Device	Suffix
COM	2502	P

Family
Package
Temperature Range

TELEDYNE PHILBRICK

TELEDYNE PHILBRICK

Description
- **1000 Series** Operational Amplifier, Module
- **1300 Series** Operational Amplifier, IC
- **1400 Series** Operational Amplifier, FET IC
- **1700 Series** Operational Amplifier Chopper Stabilized
- **2200 Series** Power Supply, AC Input, PC Mount
- **2300 Series** Power Supply, DC Input, PC Mount
- **2400 Series** Power Supply, AC Input, Chassis Mount
- **4000 Series** Digital to Analog Converters
- **4100 Series** Analog to Digital Converters
- **4300 Series** Non-Linear Function Modules
- **4400 Series** Non-Linear Function Modules
- **4500 Series** Multiplexers
- **4700 Series** Voltage to Frequency and Frequency to Voltage Converters
- **4800 Series** Sample-Hold Amplifiers

TELEDYNE SEMICONDUCTOR

For alternate source devices, the original manufacturer's part number and marking system is used.

Temperature/Electrical
- **A** −55°C to 125°C, Selected Electrical Performance (HiNIL −30°C to 70°C) 15V Supply
- **B** −55°C to 125°C, Premium Electrical Performance
- **C** 0°C to 70°C, Industrial Electrical Performance (HiNIL −30°C to 85°C); 12V Supply
- **M** −55°C to 125°C

Package
- **E** Metal Can
- **H** Flat Pack
- **J** Plastic DIP
- **L** CerDIP
- **N** Ceramic DIP
- **P** Plastic Mini DIP, 8 Lead
- **Y** Dice

Device	Suffix
709	BE

Temperature/Electrical
Package

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TELEFUNKEN

Note: ICs are marked **TFK**

(Prefixes Assigned by the European Association "PRO ELECTRON")

Proprietary Devices
- **U** Integrated Circuits
  - **B** Bipolar
  - **M** MOS

Prefix	Device	Suffix
U	113	B

TEXAS INSTRUMENTS

- **RSN** Radiation Hardened Circuit
- **SBP** Bipolar Processor
- **SMC** MOS High Reliability
- **SN** Standard Prefix
- **SNM** High Reliability, Level I
- **SNA** High Reliability, Level II
- **SNC** High Reliability, Level III
- **SNH** High Reliability, Level IV
- **TL** Linear
- **TMS** MOS

Temperature (Most Devices)
- **52 Series** −55°C to 125°C
- **54 Series** −55°C to 125°C
- **55 Series** −55°C to 125°C
- **62 Series** −25°C to 85°C
- **72 Series** 0°C to 70°C
- **74 Series** 0°C to 70°C
- **75 Series** 0°C to 70°C
- **TF Series** −40°C to 85°C
- **TP Series** −55°C to 125°C
- **TMS C Series** −25°C to 85°C
- **TMS L Series** 0°C to 70°C
- **TMS M Series** −55°C to 125°C
- **TMS R Series** −55°C to 85°C

Package
- **FA** Flat Package
- **J** Ceramic Flat Package
- **JA** DIP
- **JB** DIP
- **JP** DIP
- **L** Metal Can
- **LA** Metal Can
- **N** Plastic DIP
- **ND** Plastic DIP with Tab
- **NE** Plastic DIP with Tabs
- **P** Plastic DIP
- **RA** Flat Package
- **SB** Flat Package
- **T** Metal Flat Package
- **W** Ceramic Flat Package

Speed (MOS Only)
- −15 150ns Max. Access
- −20 200ns Max. Access
- −25 250ns Max. Access

Prefix	Device	Suffix
SN 74	S188	J

Description
Temperature Range
Package

Prefix	Device	Suffix
TMS	4027	-15 JL

Speed
Package
Temperature Range

TOSHIBA

Description
- **TA** Bipolar Linear
- **TC** CMOS
- **TD** Bipolar Digital
- **TM** MOS

Package
- **P** Plastic
- **M** Metal
- **A** Improved Type
- **C** Ceramic

Prefix	Device	Suffix
TA	7173	AP

WESTERN DIGITAL

Package
- **A** 40 Lead DIP, Ceramic
- **B** 40 Lead DIP, Plastic
- **C** 24 Lead DIP, Ceramic
- **D** 24 Lead DIP, Plastic
- **E** 28 Lead DIP, Ceramic
- **F** 28 Lead DIP, Plastic
- **G** 22 Lead DIP, Ceramic
- **H** 22 Lead DIP, Ceramic

Prefix	Device	Suffix
TR1602	A	01

Package
Special Parameter

ZILOG

Family
- **Z80**
- **Z**

Speed
- **A** 4.0 MHz
- **blank** 2.5 MHz

Device
- **CPU** Central Processor Unit
- **PIO** Parallel Input/Output Unit
- **CTC** Counter Timer
- **SIO** Serial Input/Output
- **DMA** Direct Memory Access

Package
- **C** Ceramic
- **P** Plastic

Screening
- **S** Standard
- **M** Military

Prefix	Device	Suffix
Z80 A	CPU	CM

Family
Speed
Package
Screening

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APPLICATION NOTE DIRECTORY

The Application Note Directory is a comprehensive guide to the many IC application notes available. It lists the devices covered, describes each note, and tells who publishes each one.

how to use the application note directory

The application notes in this directory can be located by function or device number.

1. To find out what is published by function, locate the closest topics in the index below, turn to the pages indicated, and scan through the listings.

2. To find all the application notes covering a given device, look up the device in the Part Number Index at the front of this book. The ¶ sign leads to application notes.

3. To find out what application notes are available from a particular manufacturer, look up the manufacturer in the Product Index. The table gives you the titles and the page locations for each manufacturer's application notes in this directory.

The application note descriptions are organized under the headings: Digital, Linear, Memory and Microprocessor. Beneath those headings are functional and applications categories arranged alphabetically. Within each category the notes are arranged in alphabetical sequence by manufacturer. The mixing of functions and applications is necessary, since application notes do not lend themselves to classification entirely by function or entirely by application. When an application note fits under several categories, it is listed in one and cross referenced by the others. This may mean that you have to spend five minutes checking a number of categories to be sure you've found everything you want, but finding suitable information can save you considerable design time.

If an application note covers specific devices or it shows in some detail how certain devices are used, these device numbers are listed in parentheses just below the title.

The application note descriptions are as short as possible. They are designed to save you time in reading while giving an overall sense of the contents. The length of each note is indicated in parentheses on the last line; if the note is bound into a book, the last line will show that it is part of a handbook, databook, catalog, etc.

Once you have determined which application notes you need, contact the manufacturer's sales office or write to the manufacturer. Be sure to give both the title and the application note number. Addresses and phone numbers are listed in the Manufacturers and Distributors Directory.

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DIGITAL

Arithmetic

1 **"A Successive Approximation Register"**
(AM2502, AM2503, AM2504, AM25L02, AM25L03, AM25L04)
Operation, logic, coding of these 8 and 12 bit TTL devices. Describes applications in systems performing recursive arithmetic operations; as ring counters; serial-to-parallel converters.
Advanced Micro Devices Application Note (11 pg.)

2 **"The AM2506 — A Latching ALU"**
(AM2506)
Combines four-bit arithmetic logic unit and four-bit latch. Describes application in high-speed multiple word adder, multiple master-slave registers, 16-word arithmetic register, multiplication at 16 MHz rate.
Advanced Micro Devices Application Note (4 pg.)

3 **"Multiplying Made Easy for Digital Assemblies"**
(AM2505)
Discusses multiplication algorithms and use of the device.
Advanced Micro Devices (6 pg.)

4 **"Overflow Detector in Binary Adders"**
(AM9309)
Discusses the detection of overflow errors using an IC multiplexer.
Advanced Micro Devices (2 pg.)

5 **"A 2's Complement Digital Multiplier: The AM2505"**
(AM2505)
Discusses high speed multiplication and use of this device to perform 2's complement multiplication.
Advanced Micro Devices (11 pg.)

6 **"AM25S10 Four-Bit Shifter"**
(AM25S10)
Provides functional description and discusses logic equivalents. Applications: up-shift, down and around end shifts, scaling and fixed multiplication.
Advanced Micro Devices Application Note (10 pg.)

7 **"Two's Complement Multiplication"**
See Digital Signal Processing Handbook under (Digital) LSI General (AMD).

8 **"Applications of the TTL/MSI 93S43 4-Bit by 2-Bit Two's Complement Multiplier"**
(93S43)
How to implement a combinatorial multiplication array of any size for two's complement numbers. How to multiply in other number representations. Speed/hardware tradeoffs, normalization of floating point numbers after multiplying, rounding or truncation of double length products.
Fairchild Application, Note 329 (15 pg.)

9 **"MECL 10,000 Arithmetic Elements MC10179, MC10180, MC10181"**
See listing under (Digital) High Speed Logic (Motorola).

10 **"NBCD Sign and Magnitude Adder/Subtracter"**
(MC14560, MC14561)
Describes CMOS parallel adder-subtracters for both signed and unsigned natural binary coded decimal (NBCD) numbers.
Motorola AN-738 (7 pg.)

11 **"High-Speed TTL Adders"**
(DM5483, DM7483)
Describes 16-bit parallel adders, using the DM7283, DM8383, and connections for ripple-carry addition. Also describes BCD adder techniques implemented with these devices. Shows how the devices can be used to improve the performance of MOS storage systems.
National AN-35 (6 pg.)

Arithmetic (cont)

12 **"Arithmetic Arrays Using Standard COS/MOS Building Blocks"**
(CD4001, CD4008, CD4011, CD4013, CD4019)
Describes design of a 32-bit full adder/arithmetic logic system. Discusses four-bit full adder, quad AND-OR select gate, dual D-type flip-flop, input NAND gates, input NOR gates, and arithmetic register.
RCA ICAN-6600 (6 pg.)

13 **"COS/MOS Rate Multipliers — Versatile Circuits for Synthesizing Digital Functions"**
(CD4089, CD4527)
Describes operation of a rate multiplier, and the effects of cascading. Covers addition, subtraction, multiplication, division, square and higher order roots, frequency ratios and integration. Also discusses symmetric operations.
RCA ICAN-6739 (12 pg.)

14 **"Converting To and From Binary Using the SN74184 and SN74185A"**
(SN74184, SN74185A, SN74283, SN74284, SN74285)
Compares conventional shift and add technique to conversion from binary to BCD using the 74185A. Tells how to interconnect these converter packages for 6-bit through 20-bit binary inputs and 4, 5 or 6 decade BCD inputs. Describes conversion of fractions using the 74283, 74284 and 74285.
Texas Instruments Application Report CA-171 (19 pg.)

15 **"Fast Multipliers Using TTL Read Only Memories"**
See listing under (Memory) ROMS. Texas Instruments)

CMOS

16 **"Intrinsically Safe Data Acquisition"**
Presents methods by which CMOS circuitry can be used in the construction of intrinsically safe low-level multiplexers, A/Ds, and instrumentation amplifiers.
Burr-Brown AN-84 (4 pg.)

17 **"Minimizing Gate Oxide Failures Due to Handling"**
Describes oxide failure mechanisms, evaluates input protection techniques, and recommends handling procedures to avoid failure.
Harris Application Report 208 (3 pg.)

18 **"CMOS: Some Application Guidelines"**
Presents General Guidelines when using CMOS.
Harris Application Note 209 (7 pg.)

19 **"Using Junction Isolated CMOS"**
Covers problems and application rules related to forward biasing CMOS inputs and outputs.
Harris Application Note 210 (4 pg.)

20 **"Avoiding CMOS Noise-Sensitivity Problems"**
Describes noise sensitivity problems peculiar to MOS technologies and solution to these problems.
Harris Semiconductor AN-211 (6 pgs.)

CMOS (cont)

1 "CMOS Analog Multiplexers and Switches; Applications, Considerations"
Covers selection criteria, parameter definitions, handling and design precautions, typical applications, and other topics concerning CMOS analog multiplexers and switches.
Harris Semiconductor AN-520 (9 pg.)

2 "Getting the Most Out of CMOS Devices for Analog Switching Jobs"
Describes latch-proof junction isolation, floating-body junction isolation, and dielectric isolation as solutions to CMOS problems when applied to analog design.
Harris Semiconductor AN-521 (7 pg.)

3 "MasterMOS, a Custom CMOS System"
(MasterMOS)
Describes the construction of these devices which are customized by changing the metalization pattern.
International Microcircuits (6 pg.)

4 "MasterMOS Design Manual"
(MasterMOS)
Detailed instructions and drawing for customizing these arrays.
International Microcircuits $35.00 (70 pg.)

5 "A New CMOS Analog Gate Technology"
See listing under (Linear) Switches. (Intersil)

6 "NBCD Sign and Magnitude Adder/Subtracter"
See listing under Arithmetic (Motorola)

7 "A 3½ Digit DVM Using an Integrated Circuit Dual Ramp System"
See listing under (Linear) Instrumentation (Motorola)

8 "Noise Immunity Comparison of CMOS Versus Popular Bipolar Logic Families"
Compares the noise immunities of TTL, DTL, HTL, and CMOS logic families. Discusses common noise sources, precautions against noise, noise specification, and standard noise tests.
Motorola AN-707 (8 pg.)

9 "Introduction to CMOS Integrated Circuits with Three-State Outputs"
Describes a wide variety of CMOS ICs incorporating transmission gates with standard logic. Gives design rules. Covers applications in analog switching and multiplexing, digital multiplexing, and data bussing.
Motorola AN-715 (19 pg.)

10 "Scanning Logic for RF Scanner-Receivers Using CMOS Integrated Circuits"
Describes rf scanner-receiver control functions using standard CMOS devices. Covers crystal switching and priority channel monitoring with mention of phase-locked loop designs.
Motorola AN-753 (7 pg.)

11 "CMOS Monostable Multivibrators"
(MC14538B)
Covers theory of operation with emphasis on pulse widths, retriggerable and non-retriggerable operation. Describes use in a tachometer.
Motorola AN-772 (7 pg.)

CMOS (cont)

12 "CMOS, the Ideal Logic Family"
(MM54C Series, MM74C Series)
Describes characteristics of CMOS circuits. Discusses system considerations, such as unused inputs, data bussing, paralleling circuits for extra drive, and interface to other logic families.
National AN-77 (8 pg.)

13 "CMOS Linear Applications"
(MM74C00, MM74C02, MM74C04)
Describes use of CMOS devices biased to operate at the midpoint of the transfer characteristics.
National AN-83 (3 pg.)

14 "CMOS Oscillators"
Describes square wave oscillators that can be built with CMOS logic elements.
National AN-118 (4 pg.)

15 "54C/74C Family Characteristics"
(MM54C Series, MM74C Series)
Discusses output, noise and temperature characteristics, power consumption, and propagation delay for the 54C/74C logic family.
National AN-90 (6 pg.)

16 "MM54C/74C Voltage Translation/Buffering"
See listing under Interface (National)

17 "Designing with MM74C908, MM74C918 Dual High Voltage CMOS Drivers"
(MM74C908, MM74C918)
Presents curves for power dissipation design limits. Shows simple driver circuits plus flasher, oscillator, siren and latch applications.
National AN-177 (12 pg.)

18 "COS/MOS Integrated Circuits Manual"
(CD4000 series)
Discusses fabrication, logic system design, and applications of RCA COS/MOS circuits.
RCA CMS-271 $2.50 (224 pg.)

19 "Noise Immunity of COS/MOS Integrated-Circuit Logic Gates"
(CD4000A, CD4001A)
Evaluates noise immunity of the CD4000A/01A gates with respect to external noise, crosstalk, transmission-line reflections, power-linet noise, and ground-line noise. Includes schematics and logic diagrams.
RCA ICAN-6176 (8 pg.)

20 "A Typical Data-Gathering & Processing System Using CD4000A-Series COS/MOS Parts"
(CD4000 Series)
Describes data-gathering and processing system using CMOS circuits. Includes discussion of input signal conditioning and transmission, the digital processor unit, receiver, memory, arithmetic unit, display unit, output buffer, output transmitter, receiver, and control unit.
RCA ICAN-6210 (11 pg.)

21 "Gate-Oxide Protection Circuit in RCA COS/MOS Digital Integrated Circuits"
(CD4000 Series)
Gives description and schematics for the protection circuits.
RCA ICAN-6218 (2 pg.)

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DIGITAL

CMOS (cont)

1 **"Radiation Resistance of the COS/MOS CD4000A Series"**
(CD4000A Series)
Provides a graph plotting permanent radiation resistance of CD4000A series. Discusses design considerations for increasing resistance.
RCA ICAN-6224 (2 pg.)

2 **"Guide to Better Handling and Operation of CMOS Integrated Circuits"**
Recommends specific handling and operating practices to minimize the probability of damage in the manufacturing and field environments.
RCA ICAN-6525 (5 pg.)

3 **"Using the CD4047A in COS/MOS Timing Applications"**
(CD4047)
Compares this monostable-astable multivibrator with simpler types of oscillator circuits and discusses applications, including a noise discriminator, low-pass and band-pass filters, a frequency discriminator, and a pulse generator.
RCA ICAN-6230 (13 pg.)

4 **"A COS/MOS PCM Telemetry and Remote Data Acquisition Design"**
(CD4000 Series)
Describes data transmission formats and the following data acquisition sections: analog and digital multiplexers, A/D converters, transmission formatters and system programmers.
RCA ICAN-6289 (12 pg.)

5 **"Power Supplies for COS/MOS"**
(CD4000 Series)
Discusses the factors involved in the selection of CMOS supply voltages including the system operating frequency, noise immunity and power dissipation. Examples of simple power supply circuits are also given.
RCA ICAN-6304 (5 pg.)

6 **"Applications of the RCA-CD4093B COS/MOS Schmitt Trigger"**
(CD4093B)
Describes characteristics of the CD4093 quad 2-input Schmitt trigger. Covers applications in waveshaping (sinewave to square-wave, edge delay, edge detection), power-on reset, astable multivibrators and use as a Schmitt trigger for noise immunity.
RCA ICAN-6346 (6 pg.)

7 **"Using the CD4520B to Design Dividers with Symmetrical Outputs"**
(CD4520B)
Describes how to use this CMOS counter to divide an input frequency by N where N is any integer from 2 to 256 and obtain outputs with approximately 50% duty cycles.
RCA ICAN-6362 (10 pg.)

8 **"Fundamentals of Testing COS/MOS Integrated Circuits"**
Describes the techniques employed in testing CMOS devices to assure their adherence to data sheet specs.
RCA ICAN-6532 (14 pg.)

9 **"Understanding Buffered and Unbuffered CMOS Characteristics"**
Presents the relative merits of buffered and unbuffered CMOS devices. Provides background, definitions, and an applications chart.
RCA ICAN-6558 (8 pg.)

CMOS (cont)

10 **"Radiation Resistance of the COS/MOS CD4000A and CD4000B Series"**
(CD4000 Series)
Studies permanent and transient radiation as they affect CMOS devices.
RCA ICAN-6563 (3 pg.)

11 **"Power-Supply Considerations for COS/MOS Devices"**
(CD4000 Series)
Includes discussion of quiescent device dissipation, switching characteristics, ac dissipation and ac performance characteristics, calculating system power, power supply regulation and filtering requirements.
RCA ICAN-6576 (6 pg.)

12 **"Interfacing COS/MOS with Other Logic Families"**
(CD4000A Series)
Describes conditions governing interface of CMOS 4000A series with other logic families.
RCA SSD-203 ICAN-6602 (12 pg.)

13 **"Battery-Powered Digital-Display Clock/Timer and Metering Applications Utilizing the RCA CD4026A and CD4033A Decade Counters 7-Segment Output Types"**
(CD4009, CD4010, CD4026, CD4033)
Describes the CD4026A/33A ICs and their use with 7-segment display units. Discusses interface packages and methods to help the designer optimize his system. Includes a discussion of battery-operated systems for digital clocks and watches.
RCA ICAN-6733 (16 pg.)

14 **"CMOS/MOS Interfacing Simplified"**
See listing under (Digtial) Interface (RCA)

15 **"CMOS/MOS Rate Multipliers — Versatile Circuits for Synthesizing Digital Functions"**
See listing under (Digital) Arithmetic (RCA)

16 **"Design of Fixed and Programmable Counters Using the RCA 4018A COS/MOS Presettable Divide-by-"N" Counter"**
See listing under (Digital) Counters. (RCA)

17 **"Application of CD4016A Quad Bilateral Switch"**
See "Transmission and Multiplexing of Analog or Digital Signals Using the CD4016A Quad Bilateral Switch" Under (Digital) Data Transmission. (RCA)

18 **"Using Complementary MOS Circuits"**
(SCL4013A, SCL4046A, SCL4018A, SCL4026A, SCL4029A, SCL4404A)
Reviews CMOS operation, cost, and reliability. Discusses application of the SCL4018A in a three decade rate multiplier; the SCL4029A in counting devices; the SCL4404A and SCL4031A in A/D converters; and SCL4016A in analog switching.
Solid State Scientific AN-101 (6 pg.)

19 **"CMOS Expandable Gates"**
(SCL4402A, SCL4412A)
Compares the transfer characteristics of ordinary CMOS gates to those gates using double buffered output. Includes performance characteristics and discusses expansion of SCL4412A and SCL4402A to 12-input NOR, 16-input OR, and other combinations.
Solid State Scientific AN-102 (3 pg.)

20 **"CMOS Integrated Circuits in Automotive Applications"**
General discussion, also includes discussion of high current circuits, constant current or constant impedance circuit, digital time delay circuit, digital low-pass filter.
Solid State Scientific AN-103 (5 pg.)

CMOS (cont)

1 **"Interfacing with CMOS"**
Describes electrical characteristics of CMOS inputs and outputs. Discusses interfacing CMOS with CMOS, PMOS, NMOS, DTL/TTL, HTL, and CL.
Solid State Scentific An-104 (5 pg.)

2 **"Improved CMOS Gate Design"**
(SCL4000 Series)
Description of the output buffering of the SCL4000 Series
Solid State Scientific AN-105 (3 pg.)

3 **"A Simplified Approach to Testing CMOS Inverters and Gates"**
Bench tests using a lower supply and a V-O-M are described. They include continuity, input leakage, quiescent device current, output voltage, noise immunity, output drive current and threshold voltage.
Solid State Scientific AN-107 (4 pg.)

4 **"Applications of CMOS Integrated Circuits in Communications Equipment"**
(SCL4000 Series)
Uses of SCL4000 Series circuits as frequency synthesizers, digital frequency displays, frequency scanners, and squelch circuits.
Solid State Scientific AN-108 (4 pg.)

5 **"CMOS Wave Shaping and Level Detection"**
Describes methods to obtain modified transfer charactertistics of double buffered NAND gates, by connecting inputs together, connecting extra inputs to V_{cc}, etc. Shows how to obtain variable amounts of hysteresis, and describes systems of level detection using trigger circuits.
Solid State Scientific AN-109 (5 pg.)

6 **"Using the SCL 4528 Dual Monostable Multivibrator"**
(SCL4528)
Describes operating modes and timing, equations for pulse width calculations.
Solid State Scientific AN-111 (6 pg.)

Consumer

7 **"A Naviation Receiver That Uses A Digital Frequency Synthesizer"**
(μA719)
Gives schematics for a navigation receiver. Discusses the digital frequency synthesizer, varactor tuned RF amplifier, AGC amplifier, mixer, IF amplifier, and detector portions.
Fairchild Application Note 178 (6 pg.)

8 **"Industrial Clock/Timer Featuring Back-up Power Supply Operation"**
Describes the design and operation of a clock timer with digital readout suitable for industrial control applications. CMOS circuits are used for reduced power.
Motorola AN-718A

9 **"Calculator Learns to Keep Time"**
Describes stopwatch and keyboard controlled interval timing functions using the MM5736 calculator chip.
National AN-119 (8 pg.)

10 **"Handheld Calculator Battery Systems"**
Describes the tradeoffs in battery performance for 6.5-9.5v calculators driven by 2, 3 and 4 cell as well as 9v. batteries.
National AN-149 (4 pg.)

Consumer (cont)

11 **"High Voltage Shift Registers Move Displays"**
See listing under (Memory) Shift Registers (National)

12 **"Timekeeping Advances Through COS/MOS Technology"**
Discusses basic oscillator design considerations, practical oscillator circuits, and some typical timing-circuit applications, including wristwatches, wall clocks, and auto clocks.
RCA ICAN-6086 (12 pg.)

13 **"CMOS Integrated Circuits in Automotive Applications"**
See listing under (Digital) CMOS. (Solid State Scientific)

14 **"Automotive Electronics: Choosing the Right Technology"**
Defines operational considerations and compares CMOS, PMOS, and bipolar.
Sprague TP 74-5 (10 pg.)

Counters

15 **"Single IC Forms 2-to-9-Bit Ring Counter"**
(AM2503)
Describes use of device to make a ring counter.
Advanced Micro Devices (2 pg.)

16 **"Design for a Battery Operated Frequency Counter"**
(ICM7207A, ICM7208)
Describes the design, circuit and layout of a 7 digit frequency and period measurement counter.
Intersil A015 (6 pg.)

17 **"Using the MK5009P MOS Counter Time-Base Circuit"**
(MK5009)
Describes the use of the MK5009 along with complete circuits for a digital frequency meter, pulse generator and digitally-programmable one-shot. Discusses operation of the units oscillator circuit.
Mostek AN-104 (4 pg.)

18 **"Applications Using the MK50395 Six Decade Counter Display Totalizer"**
(MK50395, MK50396, MK50397)
Discusses use of the counter in batch control position measurement, greater-than less-than detection, automatic stop, frequency counter, darkroom timer, digital tuning, and N-Pulser applications.
Mostek (16 pg.)

19 **"Application Information Using Mostek's Six-Decade Counter/Display Totalizer"**
(MK50395)
Covers circuit operation and input/output requirements. Describes use in a batch control system, a position measurement system and greater than-less than detection.
Mostek (8 pg.)

20 **"Programmable Counters Using the MC10136 and MC10137 MECL Universal Counters"**
(MC10136, MC10137)
Circuit operation and use in programmable counters with no external gating. Also use in high-frequency counters operating up to 110 MHz.
Motorola AN-584 (4 pg.)

21 **"Battery-Powered 5 MHz Frequency Counter"**
Describes a battery operated 5 MHz counter built with CMOS for low power operation. Discusses methods to minimize power consumption.
Motorola AN-717 (9 pg.)

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Counters (cont)

1 **"Five Digit Accumulator/Elapsed Time Indicator"**
(MC14534)
Describes in detail the circuit for a CMOS 5 digit elapsed time indicator and a 99,999 count accumulator with a 1-999 prescaler.
Motorola AN-743 (5 pg.)

2 **"The Logical Design of Shift Counters"**
Presents two techniques to aid in designing shift-register counters. Gives results for "sequence tree" and "count multiplication" techniques for cycle lengths of 30 or less. Shows solutions for both "D" flip-flops and J-K flip-flops as the input elements of the shift register.
Motorola AN-576 (8 pg.)

3 **"An MSI 500 MHz Frequency Counter Using MECL and MTTL"**
See listing under High Speed Logic. (Motorola)

4 **"Calculator Chip Makes A Counter"**
(MM5736, MM5739)
Discusses use of the MM5736 calculator chip as a counter operating up to 120 Hz.
National AN-112 (6 pg.)

5 **"Keyboard Programmable Divide-by-"N" Counter with Symmetrical Output"**
(MM54C922, MM74C922)
Describes a circuit to divide by 1 through 16 by pushing a single key for each division ratio.
National DB-5 (2 pg.)

6 **"Design of Fixed and Programmable Counters Using the RCA 4018A COS/MOS Presettable Divide-by-"N" Counter"**
(CD4018)
Describes the use of this device in single-decade and multi-decade fixed and programmable divided-by-"N" counters. System considerations, such as switch simplifications, components minimization, and speed are also discussed.
RCA ICAN-6498 (6 pg.)

7 **"ECL High Speed Counters"**
Discusses design considerations when constructing high speed counters using the TI ECL 2500 Series.
Texas Instruments Application Report CA-147 (8 pg.)

8 **"Using the SN74160 Family of Synchronous Counters"**
(SN74160, SN74161, SN74162, SN74163)
Describes carry circuit operation, cascading and programming.
Texas Instruments Application Report CA-174 (7 pg.)

Data Transmission

9 **"Line Drivers and Receivers"**
(AM2614, AM2615, 9614, 9615, 9620, 9621, DM7831, DM8831)
Discusses single ended, differential, unbalanced differential digital communications systems and line matching methods. Describes the above circuits and their use in systems.
Advanced Micro Devices Application Note (12 pg.)

10 **"Remote Multiplexing"**
Discusses acquisition of data at sensors distant from the location where the data is required and the control of actuators at a distance from the control system. Topics include interconnection, data transmission integrity, temperature, and electrical and mechanical protection.
Burr Brown AN-80 (6 pg.)

Data Transmission (cont)

11 **"Distributed Data Processing"**
Outlines design considerations dealing with remote data acquisition systems. Discusses distributed data processing and related topics such as system reliability, maintenance, network configurations and partitioning, and data base management.
Burr Brown AN-81 (5 pg.)

12 **"Intrinsically Safe Data Acquisition"**
See listing under (Digital) CMOS (Burr-Brown)

13 **"Stable FSK Modems Featuring the XR-2207, XR-2206, and XR-2211"**
(XR2206, XR2207, XR2211)
Describes designing a modulator-demodulator for use in frequency-shift keying. Circuit designs and the adjustment procedure for frequency tuning is included.
Exar AN-01 (5 pg.)

14 **"Using the Data Concentrator in Data Communications"**
(AY1016)
Describes counter, decoding matrix, and multiplexer switch sections of the AY5-1016 data concentrator. Describes commutator.decommutator and polling system applications plus use as a digitally programmable gain amplifier, and as a clock generator.
General Instrument Microelectronics (11 pg.)

15 **"The AY-5-1011 Terminal Transmitter for Key-To-Tape Data Accumulation System and Other Applications"**
(AY5-1011)
Describes features of this parallel-to-serial converter and discusses its use in key-to-tape systems.
General Instruments Microelectronics (6 pg.)

16 **The UAR/T in Data Communications**
(AY5-1013)
Describes this full duplex receiver/transmitter and discusses its application in computer, terminal and slow speed device interfacing. Also covers use in polling.
General Instrument Microelectronics (4 pg.)

17 **"High Speed Digital Communications"**
(HD245, HD246, HD545, HD546)
Describes the use of the HD-245 family in a current mode digital communication system (up to 2 Mbs over 1,000-ft-long line.)
Harris Application Note 205 (4 pg.)

18 **"Receiver/Transmitter Noise Immunity"**
(HD245, HD246, HD545, HD546)
Discusses HD-245 transmitter/receiver system noise: External magnetic and capacitive effects, crosstalk, and ground line noise. Includes a comparison with voltage mode and differential voltage switching type systems.
Harris Application Note 207 (4 pg.)

19 **"Using the 8251 Universal Synchronous/Asynchronous Receiver/Transmitter"**
(8251)
Describes this USART, covering its use as a component and as a communication-link in 8080 systems. Includes flowcharts and program listings.
Intel Application Note AP-16 $1.00 (32 pg.)

20 **"Bussing with MECL 10,000 Integrated Circuits"**
(MC10111, MC10123)
Describes use of MECL 10,000 circuits in high speed data transmission systems with emphasis on transmission line construction and termination.
Motorola AN-726 (6 pg.)

Data Transmission (cont)

1 **"Low Speed Modem Fundamentals"**
(MC6860)
Describes interface circuitry and performance of the MC6860 low speed modem. Evaluation of the system performance in the presence of Gaussian noise is given, as well as a brief description of data couplers.
Motorola AN-731 (15 pg.)

2 **"Low Speed Modem System Design Using the MC6860"**
(MC6860)
Describes the MC6860 modem. Provides filter design tables and equations to develop a complete 100 series compatible system.
Motorola AN-747 (13 pg.)

3 **"Device Operation and System Implementation of the Asynchronous Communications Interface Adapter (MC6850)"**
(MC6850)
Provides information on ACIA transmitter and receiver operation, initialization, status register bits, use in a microcomputer based communications system, software requirements, and transmission subroutines.
Motorola AN-754 (11 pg.)

4 **"Integrated Circuits for Digital Data Transmission"**
(DS7820, DS7830, DS8820, DS8830)
Describes the operation and use of the DS7830 line driver and DS7830 line receiver for transmission systems using twisted-pair lines. Includes a mathematical design analysis of this line receiver.
National AN-22 (16 pg.)

5 **"Data Bus and Differential Line Drivers and Receivers"**
(DS7820, DS7830, DS7831, DS7832, DS7833, DS7834, DS7835, DS7836, DS7837, DS7838, DS7839, DS8820, DS8830, DS8831, DS8832, DS8833, DS8834, DS8835, DS8836, DS8837, DS8838, DS8839, DS1488, DS1489)
Includes schematics and describes the operation of these line drivers, receivers and transceivers.
National AN-83 (12 pg.)

6 **"Transmission Line Characteristics"**
(DM7400, DS7820, DS7830, DS75452, DS8820, DS8830)
Describes the characteristics of digital signals in transmission lines and the characteristics of the line that effect transmission quality. Also compares the performance of unbalanced and balanced circuits in digital systems.
National AN-108 (6 pg.)

7 **"Operational Aspects of Nitron's Data Terminal Transmitter and Receiver"**
(NC2257, NC2259, NC2260)
Discusses basic operation of the NC2257/2259/2260 IC's, and application in various types of communications systems.
Nitron Communications Note 1 (24 pg.)

8 **"Using High Speed Memory in Pulse Code Modulated Systems for Switching Applications"**
Discusses digital message switching and implementation with a conventional digital crossbar switch as well as with a switch using high speed memory and data multiplexing.
Nortec Applications Note, No. 29 (4 pg.)

9 **"Transmission and Multiplexing of Analog or Digital Signals Utilizing the CD4016A Quad Bilateral Switch"**
(CD4016A)
Describes features and operation of this switch. Discusses applications, including switching, gating digital or analog signals, multiplexing and demultiplexing, D/A conversion, sample and hold, and squelch-control.
RCA ICAN-6601 (12 pg.)

Data Transmission (cont)

10 **"A COS/MOS PCM Telemetry and Remote Data Acquisition Design"**
See listing under (Digital) CMOS (RCA)

11 **"A Typical Data-Gathering and Processing System Using CD4000A-Series COS/MOS Parts"**
See listing under (Digital) CMOS (RCA)

12 **"Data Transmission with SN55107 Series"**
(SN55107, SN55108, SN55109, SN55110, SN75107, SN75108, SN75109, SN75110)
Demonstrates the use of these line drivers and receivers in solving two multiplexing problems: a party line addressing system; and data/clock signals in a bipolar line. Receiver and driver characteristics are provided.
Texas Instruments Application Report CA-146 (8 pg.)

13 **"Asynchronous Receiver/Transmitter"**
(TR1602)
General description of asynchronous transmission and operation of TR1602, which is capable of full or half duplex operation. Describes application in distributed computer networks.
Western Digital Application Report 1 (12 pg.)

Encoders

14 **"Using the AY-5-9100 in Telephone Equipment"**
(AY5-9100)
Describes use of this four phase dynamic logic circuit in mains powered dialers, line powered telephones, card readers, and in standard multifrequency tone dialer keyboards.
General Instrument Microelectronics (10 pg.)

15 **"Designing with the HD-0165 Keyboard Encoder"**
(HD0165)
The organization and truth table for this encoder are presented. The use of two circuits for encoding up to 256 keys, battery operation, examples of a teletypewriter keyboard and universal keyboard encoders are described.
Harris Application Note 204 (8 pg.)

16 **"Using the MM5704 Keyboard Interface in Keyboard Systems"**
(MM5704)
Discusses features, operation, and programming of this device. Discusses use with the MM5702 timing and control chip of the Microprogrammable Arithmetic Processing System, and in a standard ASCII encode system.
National AN-52 (11 pg.)

17 **"MOS Encoder Plus PROM Yield Quick Turnaround Keyboard Systems"**
(MM5740)
Describes use of a binary coded keyboard encoder with a PROM to build prototype or small volume keyboard systems.
National AN-139 (4 pg.)

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Encoders (cont)

1 **"Exclusive-OR Code Converters"**
(DM7086)
Covers use of exclusive-OR gates to do Gray/Binary and Binary/Hamming code conversion.
National DB-2 (2 pg.)

2 **"Interface Circuitry and Performance Optimization TMX2141 Encoder, TMX2151 Decoder"**
(2141, 2151)
Provides design notes including pulse width and timing considerations for these pulse width signalling devices.
TMX Bulletin 751 (7 pg.)

General

3 **"Don't Be Confused by Switching Time Specifications"**
Uses a TTL J-K flip-flop to explain switching time specifications.
Advanced Micro Devices (4 pg.)

4 **"MOS 100-Bit Word Generator"**
Describes how to build a 100-bit word generator using MOS ICs.
National MB-1 (2 pg.)

5 **"MOS Clock Savers"**
Design and use of MOS Clock-Drive Networks. Offers tips for saving power and lowering component costs.
National MB-5 (2 pg.)

6 **"Solid-State Devices Manual"**
Provides tutorial information on discrete devices and IC's with emphasis on consumer, hobbyist and experimenter applications.
RCA SC-16 $5.00 (750 pg.)

7 **"Criteria for Choosing Resins and Evaluation Tests for Discrete and Integrated Power Devices in Plastic Packages"**
See listing under (Linear) General (SGS-ATES)

High Speed Logic

8 **"F10,000 Series ECL"**
(ECL Series)
Operation and circuit parameters are described for the Fairchild ECL series.
Fairchild Application Note 330 (6 pg.)

9 **"IC Crystal Controlled Oscillators"**
(MC1023, MC1662, MC10101, MC10116)
Describes use of MC1023 OR/NOR gate as an amplifier and oscillator. Discusses square wave oscillator circuits with crystal control capable of output frequencies up to 150 MHz. Examples use MC10116/10101, and MC1662.
Motorola AN-417B (4 pg.)

10 **"High Speed Monostable Multivibrators Designed with MECL Integrated Circuits"**
(MC1023, MC1026)
Discusses two configurations using the MC1023 clock driver and a delay element that offer performance in excess of 70 MHz and pulse widths of 4 nanoseconds. Covers methods of obtaining the delay.
Motorola AN-418 (5 pg.)

High Speed Logic (cont)

11 **"The MC1600 Series MECLIII Gates"**
(MC1660, MC1661, MC1662, MC1663, MC1664, MC1665)
Gives typical operating characteristics and explains the operation of various gates in the MECL III family. Describes recommended layout, breadboarding, and testing procedures.
Motorola AN-504 (14 pg.)

12 **"Interconnection Techniques for Motorola's MECL 10,000 Series Emitter Coupled Logic"**
(MECL)
Describes some of the characteristics of high digital signal lines and gives wiring rules for MECL 10,000 circuits. Discusses p-c board interconnects, board-to-board interconnects, and wirewrapping techniques.
Motorola AN-556 (22 pg.)

13 **"Using Shift Registers as Pulse Delay Networks"**
(MC10135)
Discusses a high-speed delay shift register using the MC10135 flip flop.
Motorola AN-565 (3 pg.)

14 **"MECL Positive and Negative Logic"**
(MECL)
Describes equivalences between positive and negative ECL logic and provides guides for converting between them.
Motorola AN-567 (2 pg.)

15 **"Testing MECL 10,000 Integrated Logic Circuits"**
(MECL)
Describes AC and DC tests in a 50 ohm transmission-line environment for measuring logic levels or noise margins, circuit current, input currents, propagation delays, edge speeds, and flip-flop toggle rates.
Motorola AN-579 (6 pg.)

16 **"An MSI 500 MHz Frequency Counter Using MECL and MTTL"**
(MECL)
Describes design of 8-digit LED readout counter using MECL III, 10,000 and TTL. Discusses two prescalers using MECL, two input amplifier designs, and a time-base controller for the counter's multiphase clock.
Motorola AN-581 (9 pg.)

17 **"Measure Frequency and Propagation Delay with High Speed MECL Circuits"**
(MECL)
Describes ECL frequency counter useful to 160 MHz and a propagation delay measuring circuit capable of 100-picosecond resolution.
Motorola AN-586 (2 pg.)

18 **"AC Noise Immunity of MECL 10,000 Integrated Circuits"**
(MECL)
Discusses AC noise immunity. Describes test circuits for measuring this immunity and the results to be expected for MECL 10,000 circuits.
Motorola AN-592 (6 pg.)

19 **"Simulate MECL System Interconnections with a Computer Program"**
Develops a basic computer program that allows the user to simulate the performance of signal lines and to analyze termination techniques. Applies to ECL and other high speed digital systems.
Motorola AN-700 (10 pg.)

High Speed Logic (cont)

1 **"Understanding MECL 10,000 DC and AC Data Sheet Specifications"**
(MECL)
Discusses basic MECL 10,000 gate structure, transfer curve and dc levels. Covers specifications data sheet, including power supply drain current, high and low output voltages, propagation delay, rise and fall times, and toggle frequency.
Motorola AN-701 (7 pg.)

2 **"MECL 10,000 Arithmetic Elements MC10179, MC10180, MC10181"**
(MC10179, MC10180, MC10181)
Describes 10180 dual adder/subtractor, 1018 4-bit arithmetic logic unit/function generator, and 10179 lookahead carry block. Discusses their operation in parallel adders, in both ripple and look-ahead systems.
Motorola AN-709 (11 pg.)

3 **"Interfacing with MECL 10,00 Integrated Circuits"**
(MC1650, MC1692, MC10115, MC10116, MC10124, MC10125, MC-10128, MC10129, MC10216)
Discusses circuits to interface ECL with TTL, TTL and IBM busses, MOS, low level signals, and LEDs.
Motorola AN-720 (9 pg.)

4 **"A High Speed FIFO Memory Using the MECL MC1143 Register File"**
(MCM10143)
Describes the required features of a high speed FIFO design. Different approaches are compared and a design is shown using the MC10143 Multiport Register File.
Motorola AN-730 (6 pg.)

5 **"Bussing with MECL 10,000 Integrated Circuits"**
See listing under (Digital) Data Transmission (Motorola)

High Speed TTL

6 **"The MC3000/MC3100 Series Transistor-Transistor Logic Flip-Flops"**
(MC3050, MC3051, MC3052, MC3060, MC3061, MC3062, MC3150, MC3151, MC3152, MC3160, MC3162)
Describes basic operation of the various flip-flops available in the MC3000/3100 (54H/79H) series and gives typical operating characteristics of each.
Motorola AN-493 (14 pg.)

7 **"Series 54S/74S Schottky TTL Applications"**
(SN54S Series, SN74S Series)
Analyzes Schottky clamping techniques and circuits, reviews circuit performance, including discussion of transfer characteristics, switching times, and a-c noise. Discusses power supply considerations, line driving and receiving, noise sources and their abatement. Normalized loading/driving capability information and the pinouts of ICs are discussed.
Texas Instruments Application Report CA-176 (45 pg.)

HNIL/HTL

8 **"Noise Immunity with Motorola High Threshold Logic"**
(MC660 Series)
Compares noise immunity characteristics between High Threshold Logic (HTL) and standard saturated logic devices. Discusses noise injection and noise reduction techniques.
Motorola AN-298 (5 pg.)

9 **"Operation and Application of MHTL J/C Flip-Flops"**
(MC663, MC664)
Describes operation and characteristics of the J-K MC663P and the master-slave R-S MC664P flip-flops. Discusses applications as ripple and decade shift counters.
Motorola AN-414 (8 pg.)

10 **"Using Motorola High Threshold Logic"**
(MC660 Series)
Describes MC660 series ICs and provides many of the characteristics of these units. Application examples include logic translation, line driving, and trigger circuits.
Motorola AN-467 (11 pg.)

11 **"Converting Relay Control Systems to Digital I/C's"**
(MC660 Series)
Defines and discusses basic Boolean algebra and logic functions and presents method of converting relay diagrams to logic diagrams. Gives examples of conversion method using High Threshold Logic circuits and presents a system design to accomplish this.
Motorola AN-524 (11 pg.)

12 **"Design Techniques with HiNIL 367 Quad Schmitt Trigger"**
(367)
General discussion of Schmitt Trigger and the differences of the 367, which ignores open inputs and offers 3.5v noise immunity. Applications include line receivers, pulse stretchers, ac detectors, free-running and voltage-controlled oscillators.
Teledyne Semiconductor HiNIL Application, Note 2, (4 pg.)

13 **"Designing Programmable Controllers with HiNIL"**
(380)
Applications of the HiNIL 380 BCD to decade decoder including the generation of odd sequences of output pulses, the controlling of more than one load, and the switching on and off of loads.
Teledyne Semiconductor Digital Microcircuits Application, Note 3 (4 pg.)

14 **"HiNIL 375 Universal Shift Register"**
(375)
Operation and applications of this synchronous 4-bit device as a 4 and 8-bit shift-left, shift-right register, 7 and 8-bit parallel-to-serial and serial-to-parallel converters and various counters.
Teledyne Semiconductor HiNIL Application Note 4 (10 pg.)

15 **"High Noise Immunity Logic — Powerful, Versatile, and Growing"**
(300 Series)
Generally describes the HiNIL family use and features. Covers interface to other families, noise immunity, operating considerations and input protection.
Teledyne Semiconductor Digital Application Note 5 (5 pg.)

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HNIL/HTL (cont)

1 **"The HiNIL 347-A Dual Retriggerable One Shot with High Noise Immunity"**
(347)
Description and application details for this device are provided along with diagrams showing its use in pulse generators, coincidence detectors, frequency dividers, voltage to frequency and frequency to voltage converters, a pulse absence detector and an ac line presence detector.
Teledyne Semiconductor Digital Application Note 6 (6 pg.)

2 **"High Noise Immunity Logic"**
(300 Series)
Discussion includes noise immunity, loading rules, fanout, passive pull-up loading, collector or-ing, second level gating, driver pull-up, system interfaces.
Teledyne Semiconductor Digital Catalog (7 pg.)

3 **"Combining HNIL and CMOS — An Optimum Design Technique"**
See listing under (Digital) Interface (Teledyne Semiconductor)

I^2L

4 **"Custom IC Design Using I^2L Technology"**
(XR-IIL-CHIP)
Compares I^2L to other technologies. Describes design procedure for linear and digital circuits using master chips.
Exar (5 pg.)

Interface

See also Decoders.

5 **"Digital Display Systems"**
Discusses decoding, format, multiplexing, zero suppression for LED, LCD, incandescent, fluorescent and gas discharge displays.
Fairchild Application Note 212/2 (24 pg.)

6 **"9616/9617 EIA Interface Driver and Receiver"**
(9616, 9617)
Gives performance characteristics for these devices and describes their use in data communications equipment. Describes EIA standard RS232-C.
Fairchild Application Note 320 (6 pg.)

7 **"The Interface Handbook, Line Drivers and Receivers"**
(9612, 9613, 9614, 9615, 9616, 9617, 9627, 9634, 9635, 9636, 9637, 9638, 9640, 8T13, 8T14, 8T23, 8T24, 55107, 55108, 55109, 55110, 55121, 55122, 75107, 75108, 75109, 75110, 75112, 75121, 75122, 75123, 75124, 75154, 75207, 75208)
This comprehensive book covers the basics of transmission line theory along with methods for determining signal quality. Major chapters are titled: Data Transmission Lines and their Characteristics; Reflections, Computations and Waveforms; Long Transmission Lines and Data Signal Quality; and Forms of Operation (single/differential, direction of flow, analysis of common interfaces, etc.)
Fairchild Interface Handbook (118 pg.)

8 **"ASCII Bus Interface Logic Uses IM5200 FPLA"**
(IM5200)
Explains ASCII interface bus and how IM5200 provides discrete logic and address storage required by it.
Intersil Application Bulletin MB002 (6 pg.)

Interface (cont)

9 **"Semiconductors for Plated-Wire Memories"**
(MC4006, MC4007, MC4038, MC4040, MC4043, MC1514, MC1546)
Discusses operation and electrical characteristics of plated wire memories. Covers applications of drivers, sense amplifiers, and decoders as interface circuits. Also discusses memory organization and memory-related semiconductor applications.
Motorola AN-533 (15 pg.)

10 **"Interface Techniques Between Industrial Logic and Power Devices"**
Presents worst case design approaches to illustrate methods of interfacing McMOS and MHTL logic to various ac and dc power load levels.
Motorola AN-712A (19 pg.)

11 **"Interface Considerations for Numeric Display Systems"**
(MC14511, MC14543)
Gives basic information on LCD, LED, gas discharge, fluorescent and incandescent displays. Discusses interfacing 7 segment displays to logic with emphasis on multiplexed systems.
Motorola AN-741 (25 pg.)

12 **"Interfacing with MECL 10,000 Integrated Circuits"**
See listing under (Digital) High Speed Logic (Motorola)

13 **"MM54C/MM74C Voltage Translation/Buffering"**
(MM54C901, MM54C902, MM54C903, MM54C904, MM74C901, MM74C902, MM74C903, MM774C904)
Interfacing PMOS to CMOS, CMOS to CMOS with different voltage levels, and CMOS to two standard TTL loads are illustrated using 74C901 series devices.
National MB-18 (2 pg.)

14 **"Driving 7-Segment LED Displays with National Semiconductor Circuits"**
(DM5446A, DM5447A, DM5448A, DM7446A, DM7447A, DS75491, DS75492, DS7856, DS7858, DS8856, DS8857, DS8858, DS8861, DS8863, DS8864, DS8865, DS8866)
Discusses configurations and construction of 7-segment LEDs and drive modes. Describes BCD to 7-segment decoder drivers, BCD to 7-segment LED drivers, MOS to LED segment drivers, four and five segment drivers, as well as digit drivers. Describes calculator and digital clock applications.
National AN-99 (12 pg.)

15 **"Using the MM5704 Keyboard Interface in Keyboard Systems"**
See listing under (Digital) Encoders (National)

16 **"TTL/MOS/DTL Interfaces"**
Techniques for coupling the above devices and characteristics of the interfaces.
National MB-7 (2 pg.)

17 **"COS/MOS Interfacing Simplified"**
(CD4000 Series)
Covers interfacing 4000A and B series with TTL, DTL, ECL, NMOS, PMOS, industrial and power control circuits, op amps and displays.
RCA ICAN-6315 (7 pg.)

18 **"Applications of the RCA CD4093B COS/MOS Schmitt Trigger"**
See listing under (Digital) CMOS (RCA)

19 **"Interfacing COS/MOS with Other Logic Families"**
See listing under (Digital) CMOS (RCA)

Interface (cont)

1 **"Interfacing with CMOS"**
See listing under (Digital) CMOS (Solid State Scientific)

2 **"Completely Monolithic IC Series for Gas Discharge Display Interface"**
(UDN-6144, UDN-6164, UDN-6184, UDN-7183, UDN-7184, UDN-7186)
Describes operation of high voltage IC's to drive the digits and segments of 200v (Panaplex) gas discharge displays.
Sprague Electric Microcircuit Application Report MAR75-1 (8 pg.)

3 **"Expanding the Frontiers of IC Interface for Electronic Displays"**
Presents interface IC basics concerning incandescent, gas discharge, LED, plasma, fluorescent, and hot wire displays.
Sprague Electric (10 pg.)

4 **"Using Bipolar Logic to Improve Performance in CMOS and Microprocessor Systems"**
Suggests the use of HiNIL for improving noise performance, input protection, and output drive, and of LP Schottky for improved speed/power.
Teledyne Semiconductor Digital Application Note 7 (4 pg.)

5 **"Combining HNIL and CMOS — An Optimum Design Technique"**
(300 Series)
Discusses noise immunity, HNIL/74C interface, Schmitt trigger input and high current output.
Teledyne Semiconductor Digital Catalog (3 pg.)

6 **"TTL to MOS and MOS to TTL Interface Circuits"**
(SN7400, SN75107, SN75207, SN75270, SN75370, SN75450, SN-75451, TMS1103, TMS4062)
Describes MOS/TTL interface circuits using bipolar transistors, JFETS, MOSFETS, and ICs.
Texas Instruments Application Report CA-170 (11 pg.)

LSI, General

7 **"Design of Custom LSI Circuitry for Modern Digital Systems"**
Discusses design of LSI devices. Covers size considerations, numbers of input/output connections, number of output drivers, use of repetitive patterns, use of computer aided design techniques, speed versus size and power, and interfacing.
General Instrument Microelectronics (7 pg.)

Multiplexers

8 **"TTL MSI Multiplexers and Demultiplexers"**
(DM7210, DM7842, DM8210, DM8842)
Describes features of DM7210 multiplexer and DM7842 demultiplexer and discusses their use in a synchronous digital data transmission system, a keyboard entry decoder, and as minterm generators.
National AN-37 (8 pg.)

PLAs

9 **"How to Design with Programmable Logic Arrays"**
(DM8575, DM8576)
Discusses operation of PLAs and use as code converters, decode elements in digital processors and sequential controllers.
National AN-89 (8 pg.)

10 **"MOS Programmable Logic Arrays"**
(TMS2000 Series, TMS2200 Series)
Describes TMS2000 and TMS2200 Series programmable logic arrays. Describes their internal logic and operations. Provides ordering instructions.
Texas Instruments Application Report CA-158 (13 pg.)

Pulse Handling

11 **"Nanosecond Pulse Handling Techniques in I/C Interconnections"**
Discusses problems of pulse transmission and measurement for TEM mode on coax, stripline, and above-ground wire systems.
Motorola AN-270 (6 pg.)

Trigger Circuits

12 **"Advantages of the AM26123 Compared with the AM54/74123"**
(AM26123, SN54123, SN74123)
Discusses changes in the pulse width circuits and the addition of on output latch.
Advanced Micro Devices Application Brief (4 pg.)

13 **"CMOS Schmitt Triggers"**
(MC14093B, MC14583B, MC14584B)
Operating characteristics, theory of operation, and Schmitt trigger applications are covered for digital logic systems.
Motorola AN-768 (8 pg.)

14 **"1.3 Volt IC Flasher, Oscillator, Trigger, or Alarm"**
See listing under (Linear) Timers (National)

15 **"Series ULN-3300M Schmitt Trigger Integrated Circuits — Typical Applications and Operation"**
(ULN-3303, ULN-3304, ULN-3305, ULN-3306)
Describes device and use in multivibrators, switches, timers, and more.
Sprague AN-27450.19

16 **"Design Techniques with HiNIL 367 Quad Schmitt Trigger"**
See listing under (Digital) HNIL/HTL (Teledyne Semiconductor)

17 **"The HiNIL 347 — A Dual Retriggerable One Shot with High Noise Immunity"**
See listing under (Digital) HNIL/HTL (Teledyne Semiconductor)

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DIGITAL

TTL, General

1 **"Medium Scale Integration in the Numerical Control Field"**
(MC4016, MC4018, MC4024, MC4044, MC4324, MC4344)
Discusses operation of MC4016 decade programmable cascadeable counter, MC4324/4024 dual voltage controlled multivibrator, and MC4344/4044 frequency phase detector. Describes applications of these devices in audio frequency comparator, frequency synthesizer, and motor speed control circuits.
Motorola AN-541 (10 pg.)

2 **"TTL Integrated Circuits — Applications of MSI Devices"**
Covers counters, modulo-N dividers, decoders, switches, adders, comparators, parity generators, shift registers and bus-ORable flip-flop. Describes many applications, including up/down counters, a stepping waveform generator, shift registers, frequency synthesizers, digital data demultiplexer, analog commutator, minterm generator, ripple carry parallel adder and tape position locator.
National AN-36 (23 pg.)

3 **"Tri-State Logic in Modular Systems"**
(DS7831, DM8093, DM8094, DM8214, DM8230, DM8551, DM8552, DM8598, DS8831, DM8840, DM8842, DM8846)
Discusses output drive characteristics, logical control, safety factors in Tri-State Logic circuits. Describes applications, including complex switching functions, driving and transmitting, multiplexing, data storage, decoding, and data manipulation.
National AN-43 (16 pg.)

4 **"Characteristics and Applications of Tri-State IC's"**
~~(DM7093, DM7490, DM7214, DM7230, DM7551, DM7598, DS7831,~~ DS8831)
Describes application of the general configuration of the Tri-State logic family and discusses application of the following: quad bus-buffer gates, dual 4:1 multiplexer, demultiplexer and bus-interchange switch, quad-D flip-flop, expandable 256-bit ROM, and quad driver.
National AN-45 (12 pg.)

5 **"Tri-State Logic in High Speed Memories of Microprogrammed Computers"**
(DM8551)
Discusses tri-state logic in general and its use in scratchpad memories. Covers storage of microinstructions and program constants in high-speed ROMs.
National AN-47 (5 pg.)

6 **"Tri-State Logic Applied in a Computer System Can Reduce System Cost and Provide Added Performance"**
(DM8556)
Analyzes Tri-State characteristics using the DM8556 counter/register as an example. Shows how performance of PDP-8 can be improved using TSL.
National AN-73 (7 pg.)

LINEAR

Active Filters

7 **"Function Circuits, Design and Applications"**
See listing under (Linear) General (Burr-Brown)

8 **"Active Filter Design Handbook"**
(UAF7000, ACF7032, ACF7092, ACF7096)
Covers designing with universal building blocks, effects of op amp performance on state-variable filters and design of an elliptic active RC filter.
General Instrument $4.50 (48 pg.)

9 **"High Q Notch Filter"**
(LM102, LM202, LM302)
Describes use of LM102 connected to a twin "T" network to form a high Q, 60 Hz notch filter.
National Linear Applications Handbook, Vol. I LB-5 (2 pg.)

Amplifiers, Current

10 **"Application of the LH0002 Current Amplifier"**
(LH0002)
Circuit operation. Describes uses in a differential input-output op amp, booster amplifier, level shifter, pulse transformer driver, and transmission line driver.
National AN-13 (4 pg.)

Amplifiers, Instrumentation

11 **"AD520 Monolithic Instrumentation Amplifier"**
(AD520)
Describes performance of this instrumentation amplifier. Covers application as a bridge amplifier, ground loop eliminator, and floating measurement amp. Appendix compares instrumentations amplifier to several multiple op amp circuits.
Analog Devices (6 pg.)

12 **"Instrumentation Amplifiers — Versatile Differential Input Gain Blocks"**
(3660, 3670)
Describes the features and general operation of instrumentation amplifiers. Depicts their use in bridge circuits, in reducing ground loop interference, and in driven guard input circuits.
Burr-Brown AN-75 (6 pg.)

13 **"Optical Coupling Extends Isolation-Amplifier Utility"**
(3450, 3650)
Explains isolation amplifier fundamentals, optical coupling, and use of the amp in medical electronics and industrial motor control.
Burr-Brown AN-85 (8 pg.)

14 **"Instrumentational Amplifiers"**
(LM114, LM118)
Discusses general purpose instrumentation amplifier, using LM114 matched transistors ahead of an LM118 op amp that is optimized for wide bandwidth.
National Linear Application Handbook, Vol. II, LB-21 (2 pg.)

15 **"Instrumentation Amplifier"**
(LM101A, LM102, LM107)
Describes a differential-input instrumentation amplifier using LM102 and LM107 and variable gain version that also uses LM101A.
National Linear Applications Handbook, Vol. I LB-2 (2 pg.)

Amplifiers, Instrumentation (cont)

1 **"OP-10 Instrumentation Amplifier CMRR Versus Frequency Improvement"**
(OP-10)
Discusses optimization of CMRR versus frequency response of a three op amp instrumentation amplifier.
Precision Monolithics AB-2 (1 pg.)

2 **"Application of the RCA CA3000 Integrated-Circuit DC Amplifier"**
(CA3000)
Describes circuit and application as modulated oscillator, crystal oscillator, low-frequency mixer, cascaded RC-coupled feedback amp, narrow-band tuned amp, and Schmitt trigger.
RCA ICAN-5030 (11 pg.)

3 **"The Instrumentation Amp vs the Op Amp: Which, Where, and How to Use Them"**
Compares an op amp connected as a differential amp with an instrumentation amp built from several general purpose op amps. Discusses how to put each one together, and when and where to use them.
Teledyne Philbrick AN-29 (6 pg.)

Amplifiers, Operational

4 **"An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change"**
Contains considerable information on good grounding practices and op amp decoupling.
Analog Devices Application Note (8 pg.)

5 **"AD513, AD516, IC FET Input Operational Amplifiers"**
(AD513, AD516)
Describes the circuit and operation. Applications include: comparator, precision clipper, current-to-voltage converter, and a timer.
Analog Devices Technical Bulletin (4 pg.)

6 **"Applying the AD504 Precision IC Operational Amplifier"**
(AD504)
Describes this amplifier and offers notes on its noise, thermal and dynamic performance. Applications: instrumentation amplifier, stable reference regulator, instrument input amplifier and high gain ac amplifier.
Analog Devices Technical Bulletin (7 pg.)

7 **"High Speed Op Amps — How Fast is Fast?"**
Comments on op-amp characteristics, including slew rate, settling time, stability and phase margin.
Analog Devices Reprint (6 pg.)

8 **"IC FET Input Operational Amplifiers"**
(AD503, AD506)
Describes these devices and their circuit characteristics. Applications: triangle and square wave generator, charge amplifier, track and hold amplifier, D.C. voltmeter, peak rectifier, bridge amplifier and current-to-voltage converters.
Analog Devices Technical Bulletin (6 pg.)

9 **"Protect Op Amps from Overloads"**
Discusses protection from power-supply faults, keeping input voltages at safe levels, and limiting output currents.
Burr-Brown AN-60 (3 pg.)

Amplifier, Operational (cont)

10 **"Combine Two Op Amps to Avoid the Speed Accuracy Compromise"**
(3521)
Discusses interconnecting low drift and wideband op amps to form a composite op amp.
Burr-Brown AN-64 (2 pg.)

11 **"Check Five Op Amp Specs in One Test"**
Describes a test circuit that generates signals providing measurements of open loop gain, offset voltage, input bias current, quiescent current, and output voltage swing.
Burr-Brown AN-65 (1 pg.)

12 **"Using Op Amps in Low Noise Applications"**
Discusses shot noise and noise from source resistances.
Burr-Brown AN-68 (2 pg.)

13 **"Design of a Unique Precision Controlled Current Source"**
(3500)
Diagrams a current source using an op amp and a complementary FET pair to form a current source with differential input and bipolar current output.
Burr-Brown AN-74 (2 pg.)

14 **"Designing with Operational Amplifiers: Application Alternatives"**
Amplifier improvement techniques, signal analyzers, signal conditioners, absolute value circuits, signal generators, computing circuits, data transmission circuits, as well as test and measurement circuits are discussed. Circuit designs and explanations of circuit operation are provided.
Burr-Brown $21.25 (220 pg.)

15 **"Frequency Compensation Techniques for an Integrated Operational Amplifier"**
(μA702A)
Presents design techniques for frequency compensation of μA702A which are applicable to other IC operational amplifiers.
Fairchild Application Bulletin 117/2 (8 pg.)

16 **"The μA739 — A Low-Noise Dual Operational Amplifier"**
(μA739)
Describes the circuit and operating characteristics. Covers d-c circuit performance, low-frequency analysis, power consumption, noise, short-circuit protection, amplifier isolation, and compensation techniques.
Fairchild Application Note 175/1 (8 pg.)

17 **"The μA776, an Operational Amplifier with Programmable Gain, Bandwidth, Slew-Rate, and Power Dissipation"**
(μA776)
Describes methods for setting the master bias current, discusses amplifier frequency response as a function of this current. Discusses applications, including a 600 nanowatt amplifier, a low-cost sample and hold circuit, a current controlled oscillator, multiplexing, and phase shifting.
Fairchild Application Note 218 (5 pg.)

18 **"A Low Drift, Low Noise Monolithic Operational Amplifier for Low Level Signal Processing"**
(μA725)
Describes operation of μA725, which offers low offset drifts, low input currents, low noise performance, and massive open loop gain. Shows how to minimize offset voltage drift with temperature in IC operational amplifiers and how to improve the common-mode rejection.
Fairchild Application Note 277 (10 pg.)

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Amplifier, Operational (cont)

1 **"The μA715 — A Versatile High Speed Operational Amplifier"**
(μA715)
Describes application as an image orthicon head amplifier, general purpose video amplifier, 40dB high input impedance amplifier, and high speed sample and hold circuit.
Fairchild Application Note 265 (4 pg.)

2 **"Applications of the μA749 Dual Operational Amplifier"**
(μA749)
Describes applications as a dual level comparator, positive or negative peak detector, peak-to-peak detector, and as an offset null circuit.
Fairchild Application Note 268 (2 pg.)

3 **"The μA749 Dual Operational Amplifier"**
(μA749)
Discusses the circuit, input voltage range, latch-up, output voltage range, power dissipation, noise, separation, high frequency compensation, and output capability.
Fairchild Application Note 269 (8 pg.)

4 **"Applications of the μA741 Operational Amplifier"**
(μA741)
Describes applications of this amplifier as a unity gain voltage follower, integrator, differentiator, voltage regulator reference amplifier, high voltage regulated power supply control element, clipping amplifier, and a comparator.
Fairchild Application Note 289/1 (4 pg.)

5 **"An Improved Sample and Hold Circuit Using the μA740"**
(μA740)
Basic discussion of acquisition and hold times. Description of circuit using this op amp as the buffer amplifier.
Fairchild Application Note 297 (3 pg.)

6 **"Applications of the μA777"**
(μA777)
Discusses use of this operational amplifier as a pulse amplifier, Wein Bridge oscillator, variable gain differential amplifier, power amplifier.
Fairchild Application Note 300 (3 pg.)

7 **"Operational Amplifiers as Inductors"**
(μA777)
Includes derivation of equivalent circuit and necessary component values to obtain inductances from millihenries to kilohenries, using the μA777 as an example. Describes application in voltage controlled sinewave oscillators and in bandpass and notch filters.
Fairchild Application Note 321 (5 pg.)

8 **"Radiation Testing of Linear Microcircuits"**
See listing under (Linear) General (Fairchild)

9 **"HA-909 Operational Amplifier"**
(HA-909, HA-911)
Discusses applications as a unity gain breadboard op amp, servo preamplifier, high-Q bandpass filter, Wien bridge oscillator, and phase-delay filters.
Harris Application Note 501 (2 pg.)

10 **"HA-909 Operational Amplifiers Performance Tailoring"**
(HA-909, HA-911)
Discusses how to optimize HA-909's offset, power dissipation, bandwidth, large signal bandwidth, slew rate, transient response, and stability with reactive loads.
Harris Application Note 502 (3 pg.)

Amplifier, Operational (cont)

11 **"Automatic Phase Margin Testing"**
(HA-2600)
How to test op amps using an HA-2600 comparator, the 8405A vector voltmeter and a sweep generator.
Harris Application Note 504 (2 pg.)

12 **"A High Impedance Hysteresis Circuit"**
(HA-2520, HA-2620)
Describes HA-2520/HA-2620 used as a hysteresis amplifier and covers output voltage limiting.
Harris Application Note 505 (2 pg.)

13 **"Equivalent Input Noise Measurements on High Gain Monolithic Operational Amplifiers"**
(HA-709, HA-909, HA-2520, HA-2600)
Broadband noise versus bandwidth measurements for HA-709, 909, 2520, and 2600 op amps.
Harris Application Note 506 (2 pg.)

14 **"A Simple Function Generator Using Operational Amplifiers"**
(HA-2600, HA-2510)
Describes square and triangular waveform generator using HA-2600 and HA-2510 op amps.
Harris Application Note 507 (2 pg.)

15 **"Test Procedures for Operational Amplifiers"**
Circuit for measuring offset voltage, bias current, offset current, open loop voltage gain, common mode and power supply rejection ratios, output voltage/current, power dissipation, and making continuity checks.
Harris Application Note 508 (2 pg.)

16 **"A Simple Comparator Using the HA-2620"**
(HA-2620)
Describes op amp comparator circuit capable of driving approximately ten logic gates.
Harris Application Note 509 (1 pg.)

17 **"A Simple Square-Triangle Waveform Generator"**
(HA-2510, HA-2600, HA-2620)
Circuit for waveform generator using three op amps.
Harris Application Note 510 (2 pg.)

18 **"The HA-2400 PRAM Four Channel Operational Amplifier"**
(HA-2400, HA-2405)
This is a programmable input stage, operational amplifier. This note describes its applications including an analog multiplexer with buffered input and output, an inverting or non inverting amplifier with a programmable gain, a sine wave oscillator with programmable frequency, and a track and hold/sample and hold circuit.
Harris Application Note 514 (8 pg.)

Amplifier, Operational (cont)

1 **"Operational Amplifier Stability: Input Capacitance Considerations"**
(HA-2600, HA-2605)
Discusses overcoming stray capacitance in op amps, such as the HA-2600.
Harris Application Note 515 (2 pg.)

2 **"The HA-2530/2535 Wideband High Slew Inverting Amplifier"**
(HA-2530, HA-2535)
Briefly discusses internal circuit. Shows how closed-loop frequency response can be predicted. Describes application as a fast settling coaxial driver, a 10 MHz coaxial line driver, a wide range signal separator, a high frequency triangular wave generator, and a current-to-voltage converter.
Harris Application Note 516 (11 pg.)

3 **"Applications of a Monolithic Sample-and-Hold/Gated Operational Amplifier"**
(HA-2420, HA-2425)
Describes HA-2420/2425 circuit. Applications include various track-and-hold/sample-and-hold configurations, an A/D converter, a demultiplexer, an integrated-hold-reset amplifier, a gated operational amplifier, and a peak detector with reset.
Harris Application Note 517 (8 pg.)

4 **"The HA-2900 Monolithic Chopper Stabilized Amplifier"**
(HA-2900)
Discusses offset voltage and current drift and chopper stabilization, then describes the circuit. Applications include a high impedance differential instrumentation amplifier, use as an integrator, and several wide bandwidth configurations.
Harris Application Note 518 (8 pg.)

5 **"Operational Amplifier Noise Prediction"**
Provides a noise model, a procedure for computing output noise, and spot noise curves for many Harris amplifiers.
Harris Semiconductor AN-519 (10 pg.)

6 **"The 8007 — A High Performance FET-Input Operational Amplifier"**
(8007)
Circuit description, applications as log and antilog amplifiers, photocell amplifier, peak detector, sample and hold circuits, high impedance buffer, and Wien Bridge oscillator.
Intersil Application Bulletin A005 (6 pg.)

7 **"The 8043 — A Low Cost Dual FET-Input Operational Amplifier"**
(8043)
Summary of circuit characteristics. Applications as automatic offset suppression circuit, staircase generation, sample and hold circuit, and instrumentation amplifier.
Intersil application Bulletin A008 (6 pg.)

8 **"Single Power Supply Operation of IC Operational Amplifiers"**
(MC1430, MC1431, MC1433, MC1530, MC1531, MC1533, MC1709, MC1709C)
Describes a split zener biasing technique that permits the use of these operational amplifiers from a single power supply. Discusses general circuit as well as specific ac and dc device considerations to minimize operating and design problems.
Motorola AN-403 (3 pg.)

Amplifier, Operational (cont)

9 **"The MC1535 Monolithic Dual Operational Amplifier"**
(MC1435, MC1535)
Gives complete ac and dc circuit analysis and discusses electrical characteristics. Discusses applications in a differential input-differential output circuit configuration, and as a signal envelope detector. Describes an input compensation scheme for fast slew rate.
Motorola A-411 (9 pg.)

10 **"The MC1539 Operational Amplifier and its Applications"**
(MC1439, MC1539)
Discusses dc and ac operation and the performance of this amplifier. Describes a high frequency feed-forward scheme and application as a comparator, voltage follower, differential amplifier, and a summing amplifier.
Motorola AN-439 (22 pg.)

11 **"A Simple Technique for Extending Op Amp Power Bandwidth"**
(MC1433, MC1533)
Describes a method of reducing loop gain and using only as much compensation as needed to increase the power bandwidth. Cites the MC1533G as an example.
Motorola AN-459 (3 pg.)

12 **"Using Transient Response to Determine Operational Amplifier Stability"**
(MC1439, MC1539)
Describes a technique for evaluating the stability of any feedback amplifier configuration by analyzing its response to a step-function input. Includes a theoretical analysis and an example using the MC1539 operational amplifier.
Motorola AN-460 (9 pg.)

13 **"The MC1556 Operational Amplifier and its Applications"**
(MC1456, MC1556)
Gives characteristics and describes operation. Discusses application as a voltage follower, high impedance bridge amplifier, and a logarithmic amplifier.
Motorola AN-522 (8 pg.)

14 **"Analysis and Design of the Op/Amp Current Source"**
Develops expressions for the transfer function and output impedance of voltage controlled op amp current source using both ideal and non-ideal models. Discusses effects of parameter and temperature variations on performance.
Motorola AN-587 (7 pg.)

15 **"Drift Compensation Techniques for Integrated DC Amplifiers"**
Op amp bias current and offset voltage compensation are discussed. Current compensation techniques for high impedance levels and methods to achieve chopper-stabilized drift performance at low impedance levels are covered.
National Linear Applications Handbook, Vol. I, AN-3 (4 pg.)

16 **"Monolithic Operational Amplifiers — The Universal Linear Component"**
(LM101, LM102)
Applications of the LM101 and, in some cases, the LM102, include free-running multivibrator, level shifting amplifier, voltage comparator, servo preamplifier, and computing circuits. Frequency compensation techniques are discussed in detail.
National Linear Applications Handbook, Vol. I, AN-4 (10 pg.)

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Amplifier, Operational (cont)

1 "Low Power Operational LH0001 Amplifier"
(LH0001)
Operation of circuit offering 0.2 mv typical offset voltage at 25°C and quiescent supply currents in 100 μA range.
National Linear Applications Handbook, Vol. I, An-10 (4 pg.)

2 "Noise Specs Confusing?"
Explanation of terms and factors contributing to noise, calculation of noise figure and signal to noise ratio. Gives points on selecting low noise amplifiers.
National AN-104 (8 pg.)

3 "An Applications Guide for Operational Amplifiers"
(LH101, LH201, LM101, LM201, LM301)
Discusses application of operational amplifiers, grouping them in five categories: simple amplifiers, operational circuits, transducer amplifiers, wave shapers and generators, and power supplies.
National AN-20 (12 pg.)

4 "A Simplified Test Set for Operational Amplifier Characterization"
(LM101, LM201, LM301, LM709)
Gives a functional description of set that allows quantitative characterization of the dc operational amplifier parameters for the LM101 and LM709. Discusses the circuit, includes construction information, and gives a layout for the tester circuit boards.
National AN-24 (12 pg.)

5 "IC Op Amp Beats FETs on Input Current"
(LM108, LM208, LM308)
Describes LM108 operation and performance. Applications: sample and hold circuit, integrator, sine wave oscillator, capacitance multiplier, instrumentation amplifier, logarithmic converter, transducer amplifier, current source and voltage comparator. Discusses PC board construction.
National Linear Applications Handbook, Vol. I, AN-29 (20 pg.)

6 "Logarithmic Converters"
(LM101A, LM102, LM108)
Describes log generators, anti-log generators, cube generators, and multiplier/dividers, using the LM101A and LM108 op amps.
National Linear Applications Handbook, Vol. I, AN-30 (4 pg.)

7 "Op Amp Circuit Collection"
(LM101A, LM102, LM107, LM108)
Gives schematics only for some 90 cireuits using one or more of the following operational amplifiers: LM101A, LM102, LM107, LM108. Includes basic, signal generation and signal processing circuits.
National Linear Applications Handbook, Vol. I, AN-31 (20 pg.)

8 "New Design Techniques for FET Op Amps"
(LH0022, LH0022C, LH0042C, LH0052, LH0052C)
Gives parameters for LH0022, LH0042 and LH0052 operational amplifiers. Discusses rationale for FETs in these devices, describes the circuits. Describes application as voltage followers, integrators, sample/hold amplifiers, comparators, instrumentation and charge amplifiers.
National Linear Applications Handbook, Vol. I, AN-63 (12 pg.)

9 "Micropower Circuits Using the LM4250 Programmable Op Amp"
(LM4250, LM4250C)
Describes LM4250 circuit and bias current setting procedure. Applications: 500 nano-watt amplifier, micro-power comparator meter amplifier, pulse generator, instrumentation amplifier and a 5v regulator for CMOS logic circuits.
National AN-71 (8 pg.)

Amplifier, Operational (cont)

10 "The LM3900 — A New Current-Differencing Quad of ±Input Amplifiers"
(LM3900)
Describes Norton "current mirror" circuit. Emphasizes the amplifiers' application in circuits for single power supply systems. Discusses use in ac and dc amplifiers, voltage regulators, RC active filters, waveform generators, phase locked loops, and voltage controlled oscillators.
Also covers designing digital and switching circuits, and special applications, including tachometers, squaring amplifiers, positive fedback oscillators, line operated audio amplifiers, and power circuits.
National AN-72 (39 pg.)

11 "Applications for a High Speed FET Input Op Amp"
(LH0062, LH0062C)
Describes circuit, performance, compensation techniques for LH0062. Discusses applications in high speed sample and hold circuit, high speed peak detector, programmable integrator, and wide band ac voltmeter. Covers heat sinking, guarding, and bootstrapping.
National AN-75 (4 pg.)

12 "Use the LM158/LM358 Dual, Single Supply Op Amp"
(LM158, LM258, LM358)
Proposes using this dual op amp with a single supply in place of the MC1458/MC1558 with a split supply.
National AN-116 (4 pg.)

13 "LM143 Monolithic High Voltage Operational Amplifier Applications"
(LM143, LM243, LM343)
Describes circuit. High voltage applications: 130v p-p drive, ±34 CMV instrumentation amplifier. high compliance current source. Current boosted applications: 100 ma, 1 amp, high compliance. 90 W audio amplifier. High voltage power supplies. Also application tips.
National AN-127 (12 pg.)

14 "A Linear Multiple Gain-Controlled Amplifier"
Discusses gain control with FETs in the feedback path of an operational amplifier. Considers remote or multichannel gain control, volume expansion, and volume compression/limiting as possible applications.
National AN-129 (8 pg.)

15 "A Linear Multiple Gain Controlled Amplifier"
Portrays a linear control function with over three decades of gain achieved with a FET in the feedback path of a non-inverting amplifier. Gain control with FETs, distortion, bandwidth, and the control time constant are other subjects touched upon.
National FET Databook (8 pg.)

16 "Binary/BCD Gain Programmed Amplifiers"
Illustrates construction of a gain programmed amplifier using an FET quad current mode switch, 4 binary weighted resistors, and an op amp.
National FET Databook (3 pg.)

17 "The Monolithic Op Amp: A Tutorial Study"
Detailed paper on the design of IC operational amplifiers.
National Linear Applications Handbook, Vol. II (18 pg.)

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Amplifier, Operational (cont)

1 **"Feedforward Compensation Speeds Op Amp"**
(LM101A, LM201A, LM301A)
Compares standard frequency compensation with feedforward frequency compensation of LM101A. Charts open loop response for both compensation networks. Shows fast integrator circuit.
National Linear Applications Handbook, Vol. I, LB-2 (2 pg.)

2 **"Fast Compensation Extends Power Bandwidth"**
(LM101A, LM201A, LM301A)
Describes frequency compensation technique that extends power bandwidth of LM101A for non-inverting gains of unity to ten and also reduces gain error at moderate frequencies.
National Linear Applications Handbook, Vol. I, LB-4 (2 pg.)

3 **"Precision AC/DC Converters"**
(LM101A, LM201A, LM301A)
Describes the use of the LM101A in a circuit for eliminating diode threshold potential, use as a precision clamp, as a fast half wave rectifier, and precision AC to DC converter.
National Linear Applications Handbook, Vol. I, LB-8 (2 pg.)

4 **"Universal Balancing Techniques"**
Describes offset voltage adjustment for inverting amplifiers using less than 10 K source resistance or using any type of feedback element, for non-inverting amplifiers, for voltage followers, and for differential amplifiers.
National Linear Applications Handbook, Vol. I, LB-9 (2 pg.)

5 **"Speed Up the LM108 with Feedforward Compensation"**
(LM108, LM208, LM308)
Describes simple feedforward network for use with LM108 to achieve a factor of five improvement in speed.
National Linear Applications Handbook, Vol. I, LB-14 (2 pg.)

6 **"Easily Tuned Sine Wave Oscillators"**
(LM101A, LM111, LM201A, LM211, LM301A, LM311)
Describes a circuit using the LM101A and LM111 that provides both a sine and square wave output for frequencies for below 20 Hz to above 20 KHz. Also describes low distortion sine wave oscillator using two LM101As.
National Linear Applications Handbook, Vol. I, LB-16 (2 pg.)

7 **"LM118 Op Amp Slews 70 V/μS"**
(LM118, LM218, LM318)
Describes this operational amplifier with 15 MHz bandwidth. Covers a compensation scheme to approximately double bandwidth and slew rate, and one for minimum setting time.
National Linear Applications Handbook, Vol. I, LB-17 (2 pg.)

8 **"Predicting Op Amp Slew Rate Limited Response"**
Discusses slew rate limiting and gives curves for sine wave and step voltage response.
National Linear Applications Handbook, Vol. I, LB-19 (2 pg.)

9 **"Low Drift Amplifiers"**
(LM121, LM725, LM741, LM308)
Discusses problems causing drift in amplifiers and recommends solutions. Includes discussion of thermal and electrical shielding, resistor choice, circuit layout, and offset balancing.
National Linear Application Handbook, Vol. II, LB-22 (2 pg.)

10 **"True RMS Detector"**
Describes circuit using operational amplifiers that provide dc output equal to rms value of input with 2% accuracy for a 20 V_{p-p} input signal from 50 Hz to 100 kHz.
National Linear Applications Handbook, Vol. II, LB-25 (2 pg.)

Amplifier, Operational (cont)

11 **"Low Current Ammeter"**
(LM216A)
Depicts construction of an ammeter using the LM216A op amp.
National LB-37 (2 pg.)

12 **"Specifying Selected Op Amps and Comparators"**
See listing under (Linear) Comparators (National)

13 **"IC Preamp Challenges Choppers On Drift"**
See listing under (Linear) Pre-amplifiers (National)

14 **"Digital Nulling of OP-05 and SSS725"**
(DAC-08, OP-05, SSS725)
Shows digitally controlled offset nulling achieved by imbalancing the first stage collector currents of the op amp with a D/A.
Precision Monolithics AB-3 (1 pg.)

15 **"Simple Precision Millivolt Reference Uses No Zeners"**
(OP-05)
Describes −3.5 mv to 3.5 mv reference built with instrumentation op amp and a potentiometer.
Precision Monolithics AN-10 (1 pg.)

16 **"The OP-07 Ultra-Low Offset Voltage Op Amp — A Bipolar Op Amp that Challenges Choppers, Eliminates Nulling"**
(OP-07)
Describes circuit design, compares performance to other devices. Covers application in a voltage reference, a high accuracy buffer, a D/A test system, a composite summing amplifier, an absolute value circuit, an analog computer building block, and as a thermocouple amplifier.
Precision Monolithics AN-13 (12 pg.)

17 **"Minimization of Noise in Operational Amplifier Applications"**
(OP-07)
Describes internal and external sources of noise. Helps to locate noise sources by frequency. Gives examples of noise calculation using the OP-07 as an example.
Precision Monolithics AN-15 (11 pg.)

18 **"The OP-17, OP-16, OP-15 as Output Amplifiers for High Speed D/A Converters"**
(DAC-08, DAC-20, DAC-76, OP-15, OP-16, OP-17)
Illustrates design of high speed, voltage output D/A converters using these devices. Circuit diagrams for high speed, low drift, and low power applications are provided.
Precision Monolithics AN-24 (3 pg.)

19 **"Applications of the RCA CA3048 Integrated Circuit Amplifier Array"**
(CA3048)
Discusses operating parameters for this 4-amplifier array and covers applications, including Hartley and Colpitts oscillators, an astable multivibrator, four-channel linear mix, and a gain-controlled amplifier.
RCA ICAN-4072 (8 pg.)

20 **"Application of the RCA CA3008 and CA3010 Integrated-Circuit Operational Amplifiers"**
(CA3008, CA3010)
Describes operating characteristics of two op amps and their application in video amplifiers, frequency-shaping amplifiers, comparators, integrators, differentiators, scaling adders. Also covers the addition of a power output stage and/or input emitter followers.
RCA ICAN-5015 (15 pg.)

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Amplifier, Operational (cont)

1 **"Application of the RCA CA3015 and CA3016 Integrated-Circuit Operational Amplifiers"**
(CA3015, CA3016)
Describes operating characteristics at ±12 v. Applications covered are: 50-dB amplifier; twin-T bandpass amplifier, 20-dB, 10 MHz bandpass amplifier; and voltage follower.
RCA ICAN-5213 (6 pg.)

2 **"Application of RCA CA3033 and CA3033A High Performance Integrated-Circuit Operational Amplifiers"**
(CA3033, CA3033A)
Describes the basic circuit and operation. Covers application as a 250 mw, power amplifier and shows use in a DVM as a multivibrator, staircase generator, and comparator.
RCA ICAN-5641 (8 pg.)

3 **"Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers"**
(CA3090, CA3080A)
This device has an additional control terminal for flexibility. Circuit operation is discussed. Applications covered: communications and industrial systems, modulators, multiplexers, sample and hold circuits, gain control circuits, and micropower comparators. Appendix discusses current mirrors.
RCA ICAN-6668 (16 pg.)

4 **"Measurement of Burst (Popcorn) Noise in Linear Integrated Circuits"**
Discusses "pass-fail" criteria and describes a test set up for measuring burst noise. The setup includes a high gain amplifier-filter, a bipolar comparator, and a counter-latch-timer control circuit.
RCA ICAN 6732 (8 pg.)

5 **"L144 Programmable Micro-Power Triple Op Amp"**
(L144)
Describes device function, elements of programming, effects of slew rate limiting. Applications discussed include instrumentation amplifier, tone detectors, triple-amplifier active filters, and a micropower double-ended limit detector.
Siliconix AN73-6 (6 pg.)

6 **"Operational Amplifier Parameter Definition and Measurement Guide"**
Defines parameters and means of measuring them.
Teledyne Philbrick AN-23 (8 pg.)

7 **"Logarithmic Amplifiers and Operators Parameter Definition and Measurement"**
Defines and explains logarithmic amplifier parameters.
Teledyne Philbrick AN-27 (3 pg.)

8 **"The Instrumentation Amp vs the Op Amp: Which, Where, and How to Use Them"**
See listing under (Linear) Amplifiers, Instrumentation (Teledyne Philbrick)

9 **"Designing with TL080 BIFET Op Amps"**
(TL080, TL081, TL082, TL083, TL084)
Presents data sheet information, performance characteristics, and various applications including an IC preamplifier, a positive feedback bandpass filter, and a quadrature oscillator.
Texas Instruments CA-193 (11 pg.)

Amplifiers, Power

10 **"Power D/A Converters Using the IH8510"**
See listing under (Linear) Converters (Intersil)

11 **"The MC1554 One-Watt Monolithic Integrated Circuit Power Amplifier"**
(MC1554)
Describes the circuit, including dc characteristics, frequency response, and distortion. Shows how to calculate package power dissipation using the curves on the data sheet. Describes application, as one watt non-inverting, inverting, pulse power, and three-watt differential output amplifiers.
Motorola AN-401 (7 pg.)

12 **"Audio Handbook"**
See listing under (Linear) Consumer, Audio (National)

13 **"LM380 Power Audio Amplifier"**
See listing under (Linear) Consumer, Audio (National)

14 **"LM377, LM378, LM379 Dual Two, Four, and Six Watt Power Amplifiers"**
(LM377, LM378, LM379)
Discusses operation, choice and use of these circuits in audio applications. Covers distortion and heat dissipation. Also covers use in a bridge configuration, plus use as a Wein bridge power oscillator, motor drive, power comparator, relay and lamp driver.
National AN-125 (11 pg.)

15 **"Application of the RCA CA3020 and CA3020A Integrated Circuit Multi-Purpose, Wide-Band Power Amplifiers"**
(CA3020, CA3020A)
Circuit description and operation. Both circuits operate from single supply voltage as low as +3 v, offer voltage gains over 60 dB with a 3 dB bandwidth of 8 MHz. Discussion of audio, broadband and video amplifier, video line driver, motor controller and servo amp applications.
RCA ICAN-5766 (8 pg.)

16 **"TBA820 Two-Watt Monolithic Audio Amplifier"**
(TBA820)
Lists main electrical characteristics of device and presents typical applications.
SGS-ATES Technical Note 114 (11 pg.)

17 **"TCA940 Fully Protected Audio Amplifier"**
(TCA940)
Presents temperature and output short circuit protection features of the device along with a description of its performance. Illustrates use of the device in a stereo amplifier and an equalized amplifier for magnetic pickups.
SGS-ATES Technical Note 119 (15 pg.)

18 **"TBA810S/AS Thermally Protected Power Amplifier"**
(TBA810)
Description of the device followed by discussion of its performance. Also shows examples of use in tone control, TV, radio and tape playback channel applications.
SGS-ATES Technical Note 120 (16 pg.)

19 **"TCA830S-Thermally Protected Audio Power Amplifier"**
(TCA830S)
Briefly describes how the device functions followed by an examination of performance under different supply and load conditions. Portable AM/FM receiver, intercom, and magnetic tape player circuits are shown.
SGS-ATES Technical Note 126 (15 pg.)

Amplifiers, Power (cont)

1 **"TDA2020/TDA2010 HI-FI Monolithic Amplifiers"**
(TDA2020, TDA2010)
Describes these power amplifiers and how to apply them.
SGS-ATES Technical Note 130 (12 pg.)

Amplifiers, RF

2 **"An Integrated Circuit AGC IF Amplifier"**
(μA757)
Describes circuit and performance of μA757, which is recommended for applications in military and industrial equipment, also speech compressor amplifiers.
Fairchild Application Note 204 (4 pg.)

3 **"A High Gain Integrated Circuit RF-IF Amplifier with Wide Range AGC"**
(MC1590G)
Describes operation and Y parameters of the MC1590G. Applications include mixer plus IF, video, single and two-stage RF amplifiers.
Motorola AN-513 (10 pg.)

4 **"A Two-Stage 1kW Solid-State Linear Amplifier"**
Discusses the design of 50W and 300W linear amplifiers for the 1.6 to 30 MHz frequency band.
Motorola AN-758 (16 pg.)

5 **"Linear Amplifiers for Mobile Operation"**
Discusses the design of a portable amplifier suitable for amateur radio applications.
Motorola AN-762 (8 pg.)

6 **"A Compiete Monolithic AM/FM/SSB IF Strip"**
See listing under (Linear) Consumer, AM/FM (National)

7 **"Applications of the LM173/LM273/LM373"**
(LM173, LM273, LM373)
Discusses FM, AM, and SSB operation of this multi-mode IF amplifier/detector.
National Linear Applications Handbook, Vol. I, LB-13 (2 pg.)

8 **"Tuned Circuit Design Using Monolithic RF/IF Amplifiers"**
(LM171, LM703)
Discusses operating parameters for the LM171 and LM703 in emitter-coupled and cascode configurations. Brief description of 10.7 MHz emitter-coupled stage and 100 MHz cascode amplifier.
National Linear Applications Handbook, Vol. I, AN-6 (6 pg.)

9 **"Logarithmic IF Strips Using Monolithic Integrated Circuits"**
(SL521)
Describes operation of this log amplifier in successive detection type IF strips with center frequencies from 10 to 100 MHz. Covers broadband and narrow band circuits and describes in detail a 60 MHz wide-range logarithmic amplifier.
Plessey Semiconductor Technical Communication (3 pg.)

10 **"Logging IF Strip"**
(SL1521)
Describes a logging IF strip using Plessey IC's.
Plessey Semiconductor (2 pg.)

Amplifiers, RF (cont)

11 **"Application of the RCA CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers"**
(CA3004, CA3005, CA3006)
Discusses operating modes, Y parameters, noise performance, video amp capabilities, gain control, cross modulation and modulation distortion. Covers application as single-ended RF amplifier, tuned IF amplifier, mixer, suppressed-carrier modulator and product detector.
RCA ICAN-5022 (26 pg.)

12 **"Application of the RCA CA3002 Integrated-Circuit IF Amplifier"**
(CA3002)
Describes circuit, operating modes, characteristics, and application as an envelope detector, product detector, and a Schmitt trigger.
RCA ICAN-5036 (9 pg.)

13 **"Application of the RCA CA3028A and CA3028B Integrated-Circuit RF Amplifiers in the HF and VHF Ranges"**
(CA3028A, CA3028B)
Describes circuits and operating modes. Covers use as an RF amp, autodyne converter, IF amp, and limiter.
RCA ICAN-5337 (10 pg.)

14 **"Application of the RCA CA3021, CA3022, and CA3023 Integrated-Circuit Wideband Amplifiers"**
(CA3021, CA3022, CA3023)
Describes circuit and operating characteristics. Covers video, 10 MHz IF, 455 KHz IF, 28 MHz two-stage limiter, and 500 kHz limiting amplifier applications.
RCA ICAN-5338 (12 pg.)

15 **"Principal Features and Applications of the RCA CA3040 Integrated-Circuit Wideband Amplifier"**
(CA3040)
Discusses bias modes, characteristics and ratings, stability, mounting, connections, and typical wideband amplifier circuits.
RCA ICAN-5977 (11 pg.)

Amplifiers, Sense

16 **"Semiconductors for Plated-Wire Memories"**
See listing under (Digital) Interface (Motorola)

17 **"An Integrated Sense Amplifier for Core Memories"**
(MC1440, MC1540)
Discusses core memories and design considerations for a sense amplifier. Establishes performance and environment specs for amplifier design, analyzes design of MC1540, and discusses measured performance.
Motorola AN-245A (7 pg.)

18 **"The MC1541, A Gated Dual-Channel Sense Amplifier for Core Memories"**
(MC1441, MC1541)
Discusses circuit operation, design considerations, interface problems, and applications.
Motorola AN-474 (10 pg.)

LINEAR

Amplifiers, Video

1 **"A Wide Band Monolithic Video Amplifier"**
(MC1552G, MC1553G)
Describes basic operation of the MC1552G and MC1553G, and the characteristics obtained as a function of the devices' operating modes. Applications: pulse amplifier, summing/scaling amplifier, oscillator, and tuned amplifier.
Motorola AN-404 (13 pg.)

2 **"Using the MC1545, A Monolithic Gated Video Amplifier"**
(MC1445, MC1545)
Describes ac and dc operations and discusses applications as a video switch, amplitude modulator, balanced modulator, pulse amplifier, frequency shift keyer and wideband differential amplifier.
Motorola AN-475 (7 pg.)

3 **"Gated Video Amplifier Applications — The MC1545"**
(MC1445, MC1545)
Reviews basic operation and discusses applications, including several modulators, gated multivibrators, gated oscillators and FSK systems. Also discusses AGC, single supply operations, and temperature compensation of the active gate.
Motorola AN-491 (15 pg.)

4 **"Television Video IF Amplifier Using Integrated Circuits"**
See listing under (Linear) Consumer, TV (Motorola)

5 **"Application of the RCA CA3001 Integrated-Circuit Video Amplifier"**
(CA3001)
Describes circuit and operating characteristics. Covers cascaded stages and use as a Schmitt trigger.
RCA IICAN-5038 (9 pg.)

6 **"The SG1401 Video Amplifier"**
(SP1401)
Discussion of fixed and variable gain. The high frequency stability is discussed to aid in optimizing the various configurations for this device.
Silicon General Linear IC Product Guide (2 pg.)

Arrays

7 **"Using the SL362C Low Noise Transistor Pair"**
(SL362)
Provides general data on noise performance plus application in DC to 200 MHz amplifier.
Plessey Semiconductor Technical Communication (4 pg.)

8 **"Application of the RCA CA3018 Integrated Circuit Transistor Array"**
(CA3018)
Array of two isolated silicon epitaxial transistors plus two transistors with emitter-base common connections, suited for closely matched device requirements or interconnections with non-integrable components. Applications covered include IF-RF, video, agc, audio and dc amplifiers.
RCA ICAN-5296 (5 pg.)

9 **"Application of the RCA CA3019 Integrated-Circuit Diode Array"**
(CA3019)
Describes circuit configuration, operating characteristics and applications, including balanced modulator, high-speed gates, balanced mixer, and a ring modulator.
RCA ICAN-5299 (6 pg.)

Arrays (cont)

10 **"Designing with an IC Transistor Array Containing Matched Super-Beta Transistors"**
(CA3095)
Describes CA3095 IC array. Applications: low frequency amplifier, low noise video amplifier, long-delay monostable multivibrator, low-input-bias current comparator, analog timer for long delays, high input impedance dc-voltmeter circuit, and tape-head preamplifier.
RCA ICAN-6222 (9 pg.)

11 **"Monolithic Darlington Arrays Reduce Interface Cost and Complexity"**
(ULN-2001A, ULN-2002A, ULN-2003A)
Discusses packaging and heat dissipation of these 50v, 100-350 ma units. Covers parallel operation, input currents and control of up to 125 watts.
Sprague Electric Microcircuit Application Report MAR 75-2 (8 pg.)

12 **"Series ULN-2000A Darlington Transistor Arrays-Description and Application"**
(ULN-2001A, ULN-2002A, ULN-2003A ULN-2004A)
Describes circuit capabilities and its use as an interface.
Sprague (7 pg.)

Communications

See also (Digital) Data Transmission

13 **"HC-55516/32 CVSD Concept and Operations"**
(HC55516, HC55532)
Outlines Continuously Variable Slope Delta Modulation and compares it to pulse code modulation.
Harris Application Note 522 (5 pg.)

14 **"Communication System Transmission Losses"**
Derives equations for computing insertion losses for components in a communication system. Gives computer generated tables, series resistance and reactance plus parallel resistance and reactance for various system impedances.
Motorola AN-710 (5 pg.)

15 **"A Unique Monolithic AGC/Squelch Amplifier"**
(LM170, LM270, LM370)
Describes operation of LM170. Applications: agc circuits with peak or with transistor detectors, squelch preamplifier with hysteresis, voice-operated-relay controls, Wein bridge oscillators, decade tunable oscillators, and a modulated 455 kHz signal generator.
National AN-51 (12 pg.)

16 **"SL600 Series — Integrated Circuits for Radio Communications"**
(SL600 Series)
Describes circuits and applications for the following: RF/IF amplifiers; limiting RF amplifier/detector; AGC generators; AF amplifier, VOGAD side tone amplifier, AM detector, AGC amplifier and SSB demodulator; multimode detector; microphone/headphone amplifier; double balanced modulators; and a square log device. Describes synchrodyne, superhet, SSB and multimode receivers; SSB and AM transmitters; SSB transceiver, a multi/mode transceiver and a Morse keyer.
Plessey Semiconductor Applications Manual (92 pg.)

Communications (cont)

1 **"CRC8030 Telephone DTMF Receiver"**
(CRC8030)
Discusses dual-tone multi-frequency signaling. Includes specifications, test data, and interface capabilities.
Rockwell Application Note (28 pg.)

2 **"The CRC8030 Dual Tone Multi-Frequency Receiver"**
(CRC8030)
Discusses various approaches to DTMF receiver design and DTMF signaling. Includes a chart of receiver specifications and a description of the device.
Rockwell (11 pg.)

3 **"Applications of CMOS Integrated Circuits in Communications Equipment"**
See listing under (Digital) CMOS. (Solid State Scientific)

4 **"Modems"**
See listings under (Digital) Data Transmission

Comparators

5 **"AM685/AM686/AM687 Designing with High Speed Comparators"**
(685, 686, 687)
Gives a mathematical analysis of circuit operation. Discusses use as a pulse detector, precision monostable and applications requiring hysteresis.
Advanced Micro Devices Application Note (10 pg.)

"A New High Speed Comparator, the AM685"
(685)
Describes the circuit design, technology and performance of the 685. Discusses use in a fast A/D.
Advanced Micro Devices Application Note (9 pg.)

7 **"Varying Comparator Hysteresis without Shifting Initial Trip Point"**
Describes adding a positive feedback circuit to introduce precise variable hysteresis into the usual comparator switching action.
Burr-Brown AN-62 (1 pg.)

8 **"The μA760 — A High Speed Monolithic Voltage Comparator"**
(μA760)
Gives a functional description and cites typical performance characteristics. Discusses applications, including level detectors and line receivers, zero crossing detectors, high speed A/D converters, pulse width modulators, and fast peak detectors.
Fairchild Application Note 311 (8 pg.)

9 **"The μA750 Dual Comparator Subsystem"**
(μA750)
Discusses the circuit design considerations and applications, including use in a combined heater/air conditioner control, a malfunction indicator, an analog status indicator and display, and a minimum frequency detector.
Fairchild Application Note 315 (7 pg.)

10 **"Radiation Testing of Linear Microcircuits"**
Includes the 702. See listing under (Linear) General. (Fairchild)

11 **"A Simple Comparator Using the HA2620"**
See listing under (Linear) Amplifiers, Operational (Harris)

Comparators (cont)

12 **"A High Speed Dual Differential Comparator — the MC1514"**
(MC1414, MC1514)
Describes circuit operation and applications, including level and limit detectors, multivibrators, line receivers, sense amplifiers, zero crossing pulse generator and a peak voltage detector.
Motorola AN-547 (13 pg.)

13 **"Precision IC Comparator Runs from 5V Logic Supply"**
(LM111, LM211, LM311)
Describes the LM111 circuit. Applications: photodiode level detector, zero crossing detectors, digital interface circuits, multivibrators, oscillators, and a frequency doubler. Includes application hints.
National Linear Applications Handbook, Vol. I, AN-41 (6 pg.)

14 **"LM139/LM239/LM339 — A Quad of Independently Functioning Comparators"**
(LM139, LM239, LM339)
Describes LM139 circuit. Applications: comparators with hysteresis, limit comparators with lamp drivers, zero crossing detectors, oscillators, MOS clock drivers, wide range VCO, AND/NAND gates, OR/NOR gates, multivibrators, time delay generators, pulse width modulator, temperature alarm, tape reader and peak detector.
National AN-74 (16 pg.)

15 **"Application of Programmable Micropower Comparators"**
(L161)
Describes the device and how to program it. Also describes the effects of programming on AC characteristics, limit, zero crossing, and level detectors; DC to DC converter applications.
Siliconix AN76-7

16 **"Comparing the High Speed Comparators"**
(LM160, LM161, LM260, LM261, LM360, LM361)
Compares LM360 to μA760 and LM261 to NE529. Covers application as a peak detector for tape and disk file channels and in a high-speed 3-bit A/D converter.
National AN-87 (6 pg.)

17 **"Fast Voltage Comparators with Low Input Current"**
(LM102, LM106, LM202, LM206, LM302, LM306)
Describes use of LM102 to buffer the input of the LM106 comparator. Applications: comparators for fast A/D converters, for zero crossing detectors, and for ac coupled signals.
National Linear Applications Handbook, Vol. I, LB-6 (2 pg.)

18 **"An IC Voltage Comparator for High Impedance Circuitry"**
(LM111, LM211, LM311)
Describes LM111 circuit and comparison to LM106/LM710. Applications: zero crossing detector driving an analog switch, detector for a magnetic transducer, comparator for a low level photodiode, and driving a ground-referred load.
National Linear Applications Handbook, Vol. I, LB-12 (2 pg.)

19 **"Specifying Selected Op Amps and Comparators"**
Discusses the most common parameters that are tested on operational amplifiers and comparators and the relative difficulty of testing on high speed equipment. Gives a guideline to tightened specifications.
National Linear Applications Handbook, Vol. II, LB-26 (2 pg.)

20 **"Microvolt Comparator"**
(LM111, LM211, LM311, LM121A, LM221A, LM321A)
Describes an LM121A preamplifier driving an LM111 comparator.
National Linear Applications Handbook, Vol. II, LC-32 (2 pg.)

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Consumer, AM/FM

1 **"Integrated Circuits for FM Receivers"**
(μA703, μA753, μA758, μA3075)
Describes ICs capable of performing all basic functions of an FM stereo receiver, except the front end. Discusses 753 IF block, CA3075 2nd IF block, 758 stereo multiplex decoder, 706 audio power amplifier.
Fairchild Application Note 318 (7 pg.)

2 **"The μA758 — A Phase Locked Loop FM Stereo Multiplex Decoder"**
(μA758)
Gives functional description of this device, including input buffer/amplifier and bias supply, demodulator, stereo switch and lamp driver, VCO, frequency dividers, pilot phase and amplitude detectors. Discusses operating characteristics, testing and alignment.
Fairchild Application Note 319/1 (11 pg.)

3 **"The μA732 and μA767 Integrated Circuit Stereo Multiplex Decoders"**
(μA732, μA767)
Discusses stereo demodulation, stereo/monaural switching, and interstation audio mute switching sections of these devices. Describes performance characteristics, external components required, alignment and user options.
Fairchild Application Note 286 (8 pg.)

4 **"A Fully Integrated High Quality AM/FM Stereo Receiver"**
(μA706, μA720, μA739, μA753, μA758, μA3075)
Describes receiver using ICs with a comparison to discrete design.
Fairchild Application Note 328/1 (6 pg.)

5 **"Integrated Circuit IF Amplifiers for AM/FM and FM Radios"**
(MC1350, MC1355, MC1357, MFC4010, MFC6010)
Discusses the use of ICs in four IF amplifiers: a high performance FM, a quadrature detector FM, a composite AM/FM, and an economy model FM receiver.
Motorola AN-543A (14 pg.)

6 **"Scanning Logic for RF Scanner-Receivers Using CMOS Integrated Circuits"**
See listing under (Digital) CMOS (Motorola)

7 **"A Complete Monolithic IF Strip for AM/AGC Applications**
(LM172, LM272)
Circuit operation of LM172/LM272. Covers application in superheterodyne and low frequency T.R.F. receivers.
National Linear Applications Handbook, Vol. I, AN-15 (6 pg.)

8 **"A Complete Monolithic AM/FM/SSB IF Strip"**
(LM273, LM373, LM274, LM374)
Discusses LM273/LM373, and LM274/LM374 IF amplifier/detectors. Includes description of FM, SSB, and AM detection. Applications include: FM slope detector, double conversion IF strip, and coherent phase locked receiver. Also includes application hints.
National AN-54 (8 pg.)

9 **"LM1800 (LM1310, LM1310E) Phase Locked Loop FM Stereo Demodulator"**
(LM1310, LM1800)
Describes this demodulator and discusses typical performance.
National AN-81 (11 pg.)

Consumer, AM/FM (cont)

10 **"Low Cost IC Stereo Receiver"**
(LM1800, LM1820, LM3089)
Describes the complete circuit and performance of an AM/FM/Stereo receiver.
National AN-147 (4 pg.)

11 **"FM Remote Speaker System"**
Describes an FM transmitter which couples to its companion receiver thru the power lines. The system transmits speech or music and is suitable for home use as well as some factory applications.
National AN-146 (4 pg.)

12 **"Low Cost AM Radio System Using LM1820 and LM386"**
(LM1820, LM286)
Presents circuit diagram of a simple AM radio without an rf preamplifier ahead of the mixer.
National Linear Applications Handbook, Vol. II, LB-29 (2 pg.)

13 **"Audio Handbook"**
See listing under Consumer, Audio (National)

14 **"AM/SSB Transceivers and Noise Blanking Using SL1600 Series Circuits"**
(SL1623, SL1626, SL1640, SL1641)
Describes the sub-systems used in AM-SSB transceivers.
Plessey Semiconductor (10 pg.)

15 **"An SSB Transceiver for Citizens' Ban Using Plessey SL1600 Integrated Circuits**
(SL1600 series)
Describes the design of a SSB transceiver.
Plessey Semiconductor (4 pg.)

16 **"An AM Receiver Using the Plessey SL1600 Series"**
(SL1600 series)
Describes the design of a simple AM receiver.
Plessey Semiconductor (7 pg.)

17 **"SL1600 Series Transceiver Applications"**
(SL1600 series)
Discusses simple SSB and multimode transceiver design.
Plessey Semiconductor (32 pg.)

18 **"Integrated Circuits for FM Broadcast Receivers"**
(CA3005, CA3011, CA3012, CA3013, CA3014)
Discusses circuits for FM tuner, IF amplifier, limiter, and detector applications.
RCA ICAN-5269 (7 pg.)

19 **"Integrated-Circuit Frequency-Modulation IF Amplifiers"**
(CA3012, CA3028)
Describe CA3012 and CA3028 differential amplifiers and application in IF-Amplifier strips.
RCA ICAN-5380 (7 pg.)

20 **"An IC for AM Radio Applications"**
(CA3088)
Describes CA3088E and application as a basic subsystem in AM broadcast receivers, as a 10.7 MHz IF amp, and as a general-purpose amplifier array.
RCA ICAN-6022

Consumer, AM/FM (cont)

1 "Application of the RA3089E FM-IF Subsystem"
(CA3089)
Discusses stability considerations and following circuits: quadrature-detector, audio and AFC, mute, tuning meter and rf-agc, if amplifier/detector system and stereo decoder. Also covers operation at frequencies other than 10.7 MHz.
RCA ICAN-6257 (8 pg.)

2 "Integrated-Circuit Stereo Decoder Using the CA3090AQ Stereo Multiplex Demodulator"
(CA3090AQ)
Gives circuit description. Describes the LC oscillator, reactance, stereo defeat, dc coupled flip-flop preamplifier and phase splitter circuits.
RCA ICAN-6259 (10 pg.)

3 "TDA1200 FM-IF System for High Performance Radio Receivers"
(TDA1200)
Gives a detailed description of the device. Describes relative performance of device when used in an FM tuner, an AM/FM car radio, and a portable AM/FM radio.
SGS-ATES Technical Note 117 (12 pg.)

Consumer, Audio

4 "MOS Circuit for Electronic Organs"
(S2193, S2688, S8890, S10110, S10129, S10130, S10131, S50240, S50241, S50242)
Describes the use of ICs for various electronic organ circuits.
American Microsystems AP74-10 (7 pg.)

5 "Applications of the μA739 and μA749 Dual Preamplifier Integrated Circuits in Home Entertainment Equipment"
(μA739, μA749)
Describes circuit operation. Discusses d-c and a-c considerations, compensation and noise performance. Covers applications as a stereo tape amplifier, a high fidelity phonograph preamplifier, and a TV remote control amplifier.
Fairchild Application Note 171 (7 pg.)

6 "A High Output Power, (5 Watt), Low Distortion, IC Audio Amplifier"
(μA706)
Describes circuit, functions, design considerations of the μA706. Discusses application as an audio amplifier with the speaker load connected to ground, with the speaker load between supply and output, and discusses use in an FM stereo receiver.
Fairchild Application Note 317/1 (6 pg.)

7 "Designing a Basic Organ System Using the MK50240"
(MK50240)
Describes an organ system using the MK50240 Top Octave Generator for each octave.
Mostek (3 pg.)

8 "LM380 Power Audio Amplifier"
(LM380)
Describes the circuit and general operating characteristics. Applications: phono amplifier, bridge amplifier, and intercom.
National AN-69 (7 pg.)

Consumer, Audio (cont)

9 "Audio Handbook"
(LM171, LM377, LM378, LM379, LM380, LM381, LM382, LM384, LM386, LM387, LM388, LM389, LM390, LM391, LM703, LM1303, LM1310, LM1351, LM1800, LM1820, LM2111, LM3011, LM3065, LM3075, LM3089, MM5837)
Contains discussions and design particulars on many areas including preamplifiers; AM, FM, and Stereo; power amplifiers; controls, networks and power supply design—covers practical as well as theoretical aspects.
National $4.00 (188 pg.)

10 "Application of the RCA CA3007 Integrated-Circuit Audio Amplifier"
(CA3007)
Describes circuit. Covers application as dual-supply audio driver in a direct-coupled audio amp, and as single-supply audio driver in a capacitor-coupled audio amp.
RCA ICAN-5037 (4 pg.)

11 "Use of Analog Delay Lines for Audio Speed Change without Pitch Changes"
(SAD1024)
Describes technique for increasing or slowing the speed of a recording.
Reticon Application Note No. 112 (4 pg.)

12 "Build a Simple Comb-Filter or Flanger with a Bucket Brigade Delay Line"
(SAD1024)
Describes a flanger (electronic sound modifier) and what is needed to build one.
Reticon Application Note No. 113 (4 pg.)

13 "TDA1054M — Cassette Recorder Preamplifier with ALC"
(TDA1054M)
Discusses features of the device and preamplifier noise. Applications in Hi-Fi, stereo, and dynamic range compressors are described.
SGS-ATES Technical Note 124 (24 pg.)

14 "M252 and M253 Rhythm Generators for Electronic Organs"
(M252, M253)
Defines and describes rhythm generators. Presents these two devices, and describes their use in electronic organs.
SGS-ATES Technical Note 131 (21 pg.)

15 "TCA600/900 and TCA610/910 Integrated Motor Speed Regulators"
See listing under (Linear) Industrial Control (SGS-ATES)

16 "The ULN-2280 Amplifier"
(ULN-2280)
Describes this single power amplifier circuit and discusses applications as a low-cost phonograph amplifier, amplifier with tone controls, common mode amplifier, full bridge amplifier, and a mono FM receiver.
Sprague Electric Microcircuit Application Report MAR 73-2 (6 pg.)

17 "Low-Cost-Dual Class B Driver"
(ULN-2277, ULN-2278)
Describes the ULN-2277/78 ICs and describes use in dual 2-watt and dual 15-watt amplifiers.
Sprague Electric Microcircuit Application Report MAR 73-5 (3 pg.)

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Consumer, Medical

1 **"A Personalized Heart-Rate Monitor with Digital Readout"**
(MC1776, MC14013, MC14040, MC14572)
Describes digital heart-rate monitor using the MC1776 op amp and CMOS digital ICs.
Motorola AN-714 (4 pg.)

Consumer, TV

2 **"2 Watt Sound System"**
See listing under (Linear) Consumer, AM/FM (ITT Semiconductor)

3 **"Television Video IF Amplifier Using Integrated Circuits"**
(MC1330, MC1350, MC1352, MC1353)
Discusses requirements of the video IF section of a TV receiver. Describes MC1350/2/3 amplifier and MC1330 detector circuits. Includes design for a practical TV IF amplifier and detector.
Motorola AN-545 (11 pg.)

4 **"Hybrid Modules for CATV Line Extender and Trunk Amplifiers"**
(MHW560, MHW561, MHW562)
Covers circuit, packaging, and thermal considerations of MHW560/1/and 2 hybrid modules.
Motorola AN-563 (5 pg.)

5 **"Television Horizontal APC/AFC Loops: The Last 10 Percent"**
Discusses some of the common problems that may be encountered in the design of horizontal APC/AFC loops and methods to avoid or overcome them.
Motorola AN-727 (15 pg.)

6 **"A Medium Cost PLL Varactor Tuning System Utilizing Off-the-Shelf Logic"**
Describes a frequency domain tuning scheme for varactor TV tuners.
Motorola AN-729 (14 pg.)

7 **"A Synthetic Spectrum Tuning System for TV"**
Describes a tuning system which generates a complete spectrum of TV channel markers to achieve precise tuning on any channel.
Motorola AN-739 (12 pg.)

8 **"A Phase-Locked Loop Tuning System for Television"**
Describes a frequency domain tuning system using direct digital count down of the local oscillator.
Motorola AN-744 (10 pg.)

9 **"A Disassociated Intercarrier Television Video IF Amplifier"**
(MC1331)
Discusses a video IF system using the MC1331 low level multiplier detector.
Motorola AN-751 (9 pg.)

10 **"Video Amplifier Design: Know Your Picture Tube Requirements"**
(MC1323)
Describes video systems designed to alleviate design compromises associated with driving a unitized gun picture tube.
Motorola AN-761 (26 pg.)

Consumer, TV (cont)

11 **"The MC1323 — A Fully Programmable Demodulator"**
(MC1323)
Describes operation of this NTSC demodulator and use with various picture tube phosphors, especially color temperature D6500.
Motorola AN-763 (16 pg.)

12 **"An Approach to a Low-Noise TV IF System"**
(MC1331)
Discusses TV system noise figure and system trade offs, a technique to measure the IF contribution and ways to minimize the IF noise.
Motorola AN-765 (8 pg.)

13 **"A Color TV Primer for the EE"**
Describes the basic circuits in a TV and the IC's used therein.
National Linear Applications Handbook, Vol. II (pg.)

14 **"Application of the RCA CA3044 and CA3044V1 Integrated Circuits In Automatic-Fine-Tuning Systems"**
(CA3044)
Describes circuits, operating characteristics and dynamic performance of this wideband amplifier for AFC applications.
RCA ICAN-5831 (5 pg.)

15 **"Feedback-Type Volume-Control Circuits for RCA CA3041 and A3042 Integrated Circuits"**
(CA3041, CA3042)
Describes several types of volume controls for television receivers using these ICs, with a detailed discussion of feedback control.
RCA ICAN-5841 (4 pg.)

16 **"Application of the CA3126Q Chroma-Processing IC Using Sample-and-Hold Circuit Techniques"**
(CA3126Q)
Detailed circuit description of this device, which requires only one adjustment; a trimmer capacitor to tune the crystal filter. Discusses performance data, the phase detector, sample and hold circuits, the VCO loop, first chroma amplifier and ACC servo loop, and the second chroma amplifier.
RCA ICAN-6247 (8 pg.)

17 **"Description and Application of the RCA CA3120E Integrated-Circuit TV-Signal Processor"**
(CA3120)
Describes the operation and application of this device which includes TV video noise processor, agc and sync separator circuits.
RCA ICAN-6302 (9 pg.)

18 **"A Single IC for the Complete PIX-IF-System in TV Receivers"**
(CA3068)
Gives a detailed description of the circuit functions of the CA3068 and its use in color and b/w TV receivers.
RCA ICAN-6303 (17 pg.)

19 **"A Flexible Integrated-Circuit Color Demodulator for Color Television"**
(CA3067)
Describes circuit operation of the CA3067, including its output amplifiers, demodulator, demodulator preamp, and tint control amplifier. Describes use of this circuit in a red-green-blue system.
RCA ICAN-6724 (8 pg.)

Consumer, TV (cont)

1 **"Vertical Deflection Output Stages Using Audio Integrated Circuits"**
(TAA611, TAA621, TBA641, TBA800, TBA810, TBA820)
Characterizes the advantages and working principles of vertical deflection circuits using audio IC's. Seven circuits, covering small and large screen performance, are included.
SGS-ATES Technical Note 118 (18 pg.)

2 **"An Approach to a Unified Chroma System"**
Describes design approach that will eventually allow fabrication of a complete single-chip chroma system.
Sprague Electric TP 74-3 (9 pg.)

3 **"An Integrated Two-Watt Sound System for Television Applications"**
(ULN-2211)
Describes the design and use of the ULN-2211 limiter-detector-amplifier.
Sprague Electric TP 72-05 (9 pg.)

4 **"The Type ULN-2214 TV-Sound System"**
(ULN-2214)
Detailed discussion of the design and performance characteristics of this FM limiter-detector-amplifier circuit.
Sprague Electric TP 75-4 (17 pg.)

Converters

Also see Instrumentation.

5 **"Analog-Digital Conversion Notes"**
Covers many aspects of A/D and D/A converters including use, testing and specifying. Extensive applications information includes data systems, acquisition, distribution, communication.
Analog Devices $5.95 (254 pg.)

6 **"Beckman Model 845 Digital-to-Analog Converter"**
(845)
Discusses basic D/A converter performance including interface and transfer characteristics, then covers the performance of the 845 series.
Beckman Instruments (9 pg.)

7 **"D/A Converter Differential Linearity Error — It Really Shows Up"**
Discusses differential linearity, the difference in analog output for a change between two successive digital input codes. Gives graphs of two examples with the same linearity specification.
Burr-Brown AN-58 (2 pg.)

8 **"Don't Forget D/A Converter Tempco"**
Discusses offset, gain and linearity drift with temperature.
Burr-Brown AN-59 (3 pg.)

9 **"Principles of Data Acquisition and Conversion"**
Discusses basic principles of analog to digital systems including sampling rate, aperture error, accuracy, resolution, throughput, and codes.
Burr-Brown AN-79 (5 pg.)

10 **"Squeeze High Performance Out of Low-Cost Hybrid Data Converters"**
Lists ways in which converter performance can be improved by the addition of a few external components.
Burr-Brown AN-86 (4 pg.)

Converters (cont)

11 **"Intrinsically Safe Data Acquisition"**
See listing under (Digital) CMOS (Burr-Brown)

12 **"FX-209 AP Notes"**
(FX-209)
Describes use of the FX-209 delta modulation analog to digital converter as an AGC amplifier, audio delay line and as an audio scrambler.
CMA (6 pg.)

13 **"Graphs Give Aperture Time Required for A-D Conversion"**
Presents two graphs, aperture time versus rate of voltage change and versus frequency, for resolutions from 4 to 16 bits.
Datel Technical Note V-14 (4 pg.)

14 **"Know Your Converter Codes"**
Describes the various A/D and D/A converter codes.
Datel Bulletin V-12 (6 pg.)

15 **"Designer's Guide to V/F Converters"**
Spells out the theory and operation of V/F and F/V converters. Calibration procedures and such applications as ratiometric measurement and frequency difference measurement are covered.
Datel (18 pg.)

16 **"Applications of the ZN425E 8-Bit A-D/D-A Converter"**
(ZN425E)
Covers converter definitions, calibration, bipolar operation. Applications: ramp generation, peak detect, channel selection, weighing system, bargraph drive, multiply/divide, and function generation.
Ferranti (31 pg.)

17 **"Digital-to-Analog Converter Applications"**
(HI1080, HI1085)
Operating modes and applications of HI-1080 converter, which features resistor ladder network and switching devices on same chip. Discusses cascaded D to A converter as well as up-down counter and successive approximation A to D converters.
Harris Application Note 511 (7 pg.)

18 **"Counter Type A to D Converter"**
(HI1080)
Circuit details of an A to D converter employing a unidirectional digital counter and the Hi-1080 eight-bit D to A converter to generate a ramp voltage.
Harris Application Note 512 (3 pg.)

19 **"Applications of a Monolithic Sample-and-Hold/Gated Operational Amplifier"**
See (Linear) Amplifiers, Operational (Harris)

20 **"A-8400 User Guide"**
(A8400)
Theory, circuit details, operation, and design examples of this v/f and f/v converter.
Intech/FMI (18 pg.)

21 **"Digital-to-Analog Converter Circuits Using the 8018A"**
(8018A, 8019A, 8020A)
Discusses D/A converters, both in general and their electrical specifications. Describes circuit operation for 8018A and covers its expansion to 8 and 12 bit units. Also discusses generating reference currents using zeners, pnp transistors or high-gain operational amplifiers as references. Describes system interface requirements.
Intersil Application Bulletin A010 (8 pg.)

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Converters (cont)

1 **"Selecting A/D Converters"**
Compares and contrasts successive approximation and integrating A/D conversion techniques with respect to speed, accuracy, and cost.
Intersil A016 (6 pg.)

2 **"The Integrating A/D Converter"**
Discusses the dual slope technique with considerable attention to error analysis.
Intersil A017 (4 pg.)

3 **"Do's and Don'ts of Applying A/D Converters"**
Examines topics concerning proper system design when using A/D converters. Subjects treated include ground loop errors, components, references, capacitive coupling, and thermal effects.
Intersil A018 (2 pg.)

4 **"Power D/A Converters Using the IH8510"**
(IH8510, AH8520, IH8521, 7105, 7120)
Discusses the addition of a power amplifier to a D/A converter. Briefly describes use for motor control and programmable power supplies.
Intersil A021 (4 pg.)

5 **"Voltage Transients (Glitches)"**
(MN3008)
Discusses D/A converter analog voltage spikes appearing in the output following a change of input code.
Micro Networks AN-101 (2 pg.)

6 **"Truncation of A/D Converters"**
Describes how to reduce or to program the number of bits converted.
Micro Networks AN-102 (2 pg.)

7 **"When Should a Sample Hold Amplifier be Used?"**
Covers the use of sample-hold amplifiers with A/D converters. Discusses use with dynamically changing signals and the droop rate of the sample-hold circuit.
Micro Networks AN-103 (2 pg.)

8 **"MN312 Connections for Bipolar Output"**
(MN312)
Shows use of an external op amp to convert a unipolar output to bipolar.
Micro Networks AN-104 (2 pg.)

9 **"Serial to Parallel Conversion"**
(MN502, MN5200, MN5210)
Covers timing considerations in the conversion of A/D converter output from serial to parallel form.
Micro Networks AN-106 (2 pg.)

10 **"Simplifying the Digital to Analog Converter through Hybrid Technology"**
Considers basic design problems of D/A converters and gets into hybrid design. Includes construction techniques, specifications and testing.
Micro Networks (10 pg.)

11 **"Analog-to-Digital Conversion Techniques"**
Discusses open-loop and feedback techniques: frequency, pulse width, cascade, ramp, counter, successive approximation, multiple comparison subranging, nonlinear conversion, double and triple ramp conversion.
Motorola AN-471 (21 pg.)

Converters (cont)

12 **"Analog-to-Digital Cyclic Converter"**
(MC1456)
Discusses circuits and operation of medium speed-medium accuracy converter that uses successive approximation technique in which unknown analog input voltage is successively compared to reference voltage to determine each bit of digital output. A comparison of gray and binary code operation and an error analysis are provided.
Motorola AN-557 (10 pg.)

13 **"A Single Ramp Analog-to-Digital Converter"**
Discusses an A/D converter which incorporates a calibration cycle to insure 12 bit accuracy. Briefly covers errors encountered in the converter described.
Motorola AN-559 (9 pg.)

14 **"High Speed Digital-to-Analog and Analog-to-Digital Techniques"**
Gives overview that includes voltage and current output D/As; parallel (flash), tracking, successive approximation, and parallel ripple A/Ds as well as nonsynchronous and synchronous VTF A/D. Glossary of terms.
Motorola AN-702 (14 pg.)

15 **"Binary D/A Converters Can Provide BCD-Coded Conversion"**
(MC1408, MC1508)
Describes the MC1508 D/A converter used as a 2 or 2½ digit BCD converter. Describes application in a 2½ digit digital voltmeter.
Motorola AN-713 (4 pg.)

16 **"Successive Approximation A/D Conversion"**
(MC1408, MC14559)
Describes advances in successive approximation techniques with emphasis on SARs (Successive Approximation Registers.) Shows both a normal and a high speed A/D using these methods.
Motorola AN-716 (8 pg.)

17 **"Autoranging Digital Multimeter Using the MC14433 CMOS A/D Converter"**
(MC14433)
Describes using the MC14433 A/D converter to build an autorange digital multimeter. The multimeter includes ac and dc voltage ranges from 200mV to 200V, ac and dc current from 2mA to 2A full scale, and resistance ranges from 2 kilohms to 2 megohms full scale.
Motorola AN-769 (5 pg.)

18 **"Data Acquisition Networks with NMOS and CMOS"**
See listing under (Microprocessors) Applications (Motorola)

19 **"Analog-to-Digital Conversion Techniques with the M6800 Microprocessor System"**
See listing under (Microprocessor) Systems (Motorola)

20 **"Applications of the MC1405/MC14435 in Digital Meters"**
See listing under (Linear) Instrumentation (Motorola)

21 **"Digital Voltmeters and the MM5330"**
(MM5330)
Describes basic counting techniques for building digital voltmeters and shows how the MM5330 can be used in a dual slope system.
National AN-155 (8 pg.)

22 **"Specifying A/D and D/A Converters"**
Explains and defines the data sheet terms for these converters.
National AN-156 (6 pg.)

Converters (cont)

1 **"Data Acquisition System Interface to Computers"**
(ADC1200, ADC1210, MM5357)
Compares three configurations for multiple input analog to digital converter systems—Random Addressed Multiplexed, Parallel Conversion, and Multiplexed with Memory. Gives detailed comparisons of costs, A/D and interface requirements.
National AN-159 (18 pg.)

2 **"Analog-to-Digital Converter Testing"**
(ADC0800, ADC1210, ADC1211)
Describes a low cost test circuit with board layout for testing A/Ds using a storage scope readout.
National AN-179 (6 pg.)

3 **"A Cheap and Easy DC-DC Converter"**
(LM555)
Design equations, derivations, and schematics used to construct a DC-DC converter.
National AN-183 (4 pg.)

4 **"High Speed Warning Device for Automobiles"**
Proposes a tachometer device operating from the spark coil primary.
National Linear Applications Handbook, Vol. II, LB-33 (2 pg.)

5 **"Logarithmic Converters"**
See listing under (Linear) Amplifiers, Operational (National)

6 **"SC/MP as an Analog-to-Digital Converter"**
See listing under (Microprocessors) Applications (National)

7 **"Strobing the DAC-08 Under Logic Control"**
(DAC-08)
Gives connections for strobing the output of this DAC.
Precision Monolithics AB-1 (1 pg.)

8 **"A Low Cost, High-Performance Tracking A/D Converter"**
(DAC-100, CMP-01)
Basic operation of 8-bit tracking converter that uses DAC-100 series 10-bit D/A converter, CMP-01 series comparator, and 4-bit MSI up/down counters.
Precision Monolithics AN-6 (8 pg.)

9 **"A Low Cost, Easy-to-Build Successive Approximation Analog-to-Digital Converter"**
(DAC-100, CMP-01)
General discussion of feedback A/D converters. Operation of A/D converter capable of 8-bit conversions in 6 μs. The system is expandable to 10-bit resolution. It uses DAC-100, CMP-01, and a successive approximation register.
Precision Monolithics AN-11 (8 pg.)

10 **"Interfacing Precision Monolithics Digital-to-Analog Converters with CMOS Logic"**
(DAC-100, DAC-01)
Analyzes input circuits of these DACs and CMOS interfaces. Describes a complete 10-bit DAC and an 8-bit A/D.
Precision Monolithics AN-14 (4 pg.)

11 **"Low Cost, High Speed Analog-to-Digital Conversion with the DAC-08"**
(DAC-08)
Discusses the successive approximation technique to A/D and describes three designs with conversion times of 1, 2, and 4 μ sec.
Precision Monolithics AN-16 (7 pg.)

Converters (cont)

12 **"DAC-08 Applications Collection"**
(DAC-08)
Discusses the dual output, and high compliance. Covers use in a CRT display driver, bridge transducer control system, A/D converter, waveform generator, digital additions/subtraction with analog output, digital attenuator and microprocessor controlled A/D converter.
Precision Monolithics AN-17 (12 pg.)

13 **"Differential and Multiplying Digital-to-Analog Converter Applications"**
(DAC-08)
Describes use in 2-quadrant, 4-quadrant and AC-coupled multiplication. Also covers differential and ratiometric conversion, a nulling bridge circuit, a power monitor, and algebraic computation circuits with analog output.
Precision Monolithics AN-19 (8 pg.)

14 **"Exponential Digitally Controlled Oscillator Using DAC-76"**
(DAC-76)
Depicts a 4-IC microprocessor-controlled oscillator with a 8159 to 1 frequency range covering 2.5 Hz to 20 kHz. The circuit uses an exponential current output D/A converter as a programmable current source.
Precision Monolithics AN-20 (3 pg.)

15 **"3 IC 8-Bit Binary Digital to Process Current Converter with 4-20 mA Output"**
(REF-01, DAC-08, OP-14)
Delineates the construction of a process current converter operating from −5v and 23v supplies. Complete theory of operation followed by calibration procedures and a detailed parts list are included.
Precision Monolithics AN-21 (2 pg.)

16 **"Software Controlled A/D Conversion Using DAC-08 and the 8080A Microprocessor"**
(DAC-08, 8080A)
Describes software controlled, 8-bit A/D conversion using the DAC-08 and the 8080A. Subjects include I/O interface considerations, I/O control using memory mapping, and a successive approximation A/D conversion algorithm.
Precision Monolithic AN-22 (4 pg.)

17 **"D/A Converter Generates Hyperbolic Functions"**
(DAC-20)
Explains operating theory and design considerations of a two IC hyperbolic function generator. Includes circuit diagrams.
Precision Monolithics AN-23 (3 pg.)

18 **"Digital-to-Analog Conversion Using the RCA CD4007A COS/MOS IC"**
(CD4007A)
Discusses resistance networks for DAC's and a voltage-follower amp for single-supply operation. Describes a 3-bit COS-MOS DAC.
RCA ICAN-6080 (6 pg.)

19 **"The 4151 Voltage to Frequency Converter"**
(RC4151, RM4151, RV4151)
Describes various uses of this v/f and f/v converter.
Raytheon Semiconductor Application Note (8 pg.)

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Converters (cont)

1 **"Function and Application of 3½ Digit A/D Converter Set"**
(LD110, LD777)
Describes the operation of the LD110 digital processor and the LD111 analog processor. Various DVM circuits are shown including circuits for ratio, current, ac voltage and frequency measurements. A detailed error analysis is provided.
Siliconix AN74-1 (12 pg.)

2 **"More Applications of the LD110/LD114 ±3½ A/D Converters"**
(LD110, LD111, LD114)
Provides circuits to construct LCDs, multiplexed displays, gas discharge displays, and a DC-DC converter. Also details the differences between the LD110 and LD114.
Siliconix AN76-4 (8 pg.)

3 **"Applying the LD130 ± Digit A/D Converter"**
(LD130)
Discusses device features and its use in displays, interface, and instrumentation.
Siliconix AN76-5 (16 pg.)

4 **"Solve Your Measurement Problems"**
Discusses v/f and f/v converters and their use in data acquisition problems.
Teledyne Philbrick AN-20 (6 pg.)

5 **"Designing High Speed Data Acquisition Systems"**
Discusses the basics of data acquisition systems; focusing on sample-and-hold circuits and multiplexer modules.
Teledyne Philbrick AN-21 (12 pg.)

6 **"How to Specify and Test Voltage to Frequency and Frequency to Voltage Converters"**
Defines device parameters, specifications, and test techniques.
Teledyne Philbrick AN-22 (4 pg.)

7 **"Specifying and Testing Analog-to-Digital Converters"**
Defines the basic parameters, specifications, and test methods.
Teledyne Philbrick AN-24 (7 pg.)

8 **"Specifying and Testing Digital-to-Analog Converters"**
Defines basic parameters, specifications and test methods.
Teledyne Philbrick AN-25 (7 pg.)

9 **"Repetitive Mode Operation for Models 4109/4111 Integrating A/D Converters"**
(4109, 4111)
Runs through external trigger generator and sure start circuit schemes which are used when the devices must run without ceasing to convert.
Teledyne Philbrick AN-28 (2 pg.)

10 **"Specifying and Testing Sample-Hold Amplifiers"**
Defines various sample-hold amplifier parameters and outlines methods of testing for them.
Teledyne Philbrick AN-30 (5 pg.)

11 **"Modular V/F's and F/V's: Simple Solutions to Everyday Conversion Problems"**
Examines applications of V/F's and F/V's. Also demonstrates how accuracy can be improved with the addition of more components.
Teledyne Philbrick AN-32 (7 pg.)

Converters (cont)

12 **"Using the 8750 3½ Digit A/D Converter"**
(8750)
Supplies diagrams showing interface to autoranging circuits, to gas discharge displays, and to two independent displays operated from one A/D.
Teledyne Semiconductor AN-9 (4 pg.)

13 **"Applications for the 9400 Voltage to Frequency/ Frequency to Voltage Converter"**
(9400)
Contains 25 block diagrams of applications in which the device is used.
Teledyne Semiconductor AN-10

Drivers

See also (Digital) Interface

14 **"CMOS Line Drivers"**
States reasons for using CMOS line drivers.
National AN-158 (4 pg.)

15 **"Driving Burroughs' Bar Graph Display"**
Shows the use of comparators and flip-flops to drive these displays.
National DB-4 (2 pg.)

16 **"MOS Clock Drivers"**
(MH0007, MH0009, MH0012, MH0013)
Lists the characteristics of various MOS clock drivers and how they differ in their input stages.
National MB-9 (2 pg.)

17 **"PIN Diode Drivers"**
See listing under (Linear) Switches. (National)

18 **"Driver Circuits for the JFET Analog Switch"**
See listings under (Linear) Switches. (Siliconix)

19 **"Logic to Power Converter Circuits"**
(400-series, 500-series)
Covers the operation of the 400 and 500 high current driver series.
Sprague Electric TP 71-3 (6 pg.)

Followers

20 **"A Fast Integrated Voltage Follower with Low Input Current"**
(LM102)
Circuit description. Use of the LM102 for analog commutator, sample and hold ac amplifier and active filter applications.
National Linear Applications Handbook, Vol. I, AN-5 (11 pg.)

21 **"The LM110 — An Improved IC Voltage Follower"**
(LM110, LM210, LM310)
Compares LM102 and LM110 circuits. Shows diagrams of LM110 as a high pass active filter, high Q notch filter, bandpass filter, and low drift sample and hold circuit.
National Linear Applications Handbook, Vol. I, LB-11 (2 pg.)

22 **"Monolithic Operation Amplifiers — The Universal Linear Component"**
See (Linear) Amplifiers. Operational (National)

Followers (cont)

1 **"Applications for a New Ultra-High Speed Buffer"**
(LH0033, LH0033C)
Describes LH0033 fast voltage follow/buffer. Applications: high speed dual limit comparator for MOS logic, instrumentation shield/line driver, high speed sample and hold circuit, 4.5 MHz notch filter, high input impedance AC coupled amplifier, output buffer.
National AN-48 (4 pg.)

General

2 **"Nonlinear Circuits Handbook"**
Covers principles, circuits, performance, specifications, testing and applications for multipliers, dividers, squares, log circuits, multifunction and rms-to-dc converters.
Analog Devices $5.95 (535 pg.)

3 **"Function Circuits, Design and Applications"**
Covers design theory and applications for such analog functions as multipliers, dividers, logarithmic amplifiers, exponentiators, RMS converters, and active filters. Includes notes on specifying and testing these functions.
Burr-Brown $18.65 (300 pg.)

4 **"Intrinsically Safe Data Acquisition"**
See listing under (Digital) CMOS (Burr-Brown)

5 **"Custom IC Design Using I^2L Technology"**
See (Digital) I^2L (Exar)

6 **"Radiation Testing of Linear Microcircuits"**
(μA702, μA709, μA710, μA711)
Describes tested performance of μA702 and μA709 operational amplifiers and μA710 and μA711 comparators after having been irradiated with fast neutrons of energies greater than 0.01 MeV.
Fairchild Application Note 195 (13 pg.)

7 **"Solid State Gas/Smoke Detector Systems"**
Describes semiconductor and ionization chamber systems with some discussion of the use of these with CMOS ICs.
Motorola AN-735 (9 pg.)

8 **"Noise Sources"**
Reviews noise basics. Includes discussion of resistive, capacitive, and inductive noise sources.
National FET Databook (3 pg.)

9 **"The Noise Figure Fallacy"**
Describes problems of defining and calculating the noise figure.
National FET Databook (2 pg.)

10 **"Linear Applications, Vol. 1"**
Feb. 1973, includes National application notes (AN) 1-6, 8, 10, 13, 15, 20, 21, 23, 24, 28-34, 38, 41, 42, 46, 48, 49, 51, 53, 54, 56, 63, 64, 69-72, 74, 75 and Linear Briefs (LB) 1-20, individually described elsewhere.
National $4.00 (432 pg.)

11 **"Linear Applications, Vol. 2"**
Includes National application notes (AN) 79, 81, 82, 87, 88, 97, 103, 104, 110, 115, 116, 125, 129, 132, 146, 147, 151, 153, 154, 156, 161, 162 and Linear Briefs (LB) 21-34, individually described elsewhere.
National $4.00 (256 pg.)

General (cont)

12 **"CMOS Linear Applications"**
See listing under (Digital) CMOS (National)

13 **"Constant Current LED"**
See listing under (Linear) Regulators (National)

14 **"Surface Acoustic Wave Technology"**
Presents surface acoustic wave fundamentals and use in delay lines, pulse compression filters, bandpass filters, oscillators and discriminators.
Plessey Semiconductor (10 pg.)

15 **"Solid-State Devices Manual"**
Provides tutorial information on discrete devices and ICs, with emphasis on consumer, hobbyist and experimenter applications.
RCA SC-16 $5.00 (750 pg.)

16 **"Linear Integrated Circuits"**
Basic circuit elements, fabrication, packaging, and interconnection techniques are discussed. Data and application information on RCA linear IC's is included.
RCA IC-41 $2.50 (416 pg.)

17 **"Criteria for Choosing Resins and Evaluation Tests for Discrete and Integrated Power Devices in Plastic Packages"**
Describes the criteria and experimental procedures used in the choosing of moulding resin for plastic packaged devices.
SGS-ATES Technical Note 132 (15 pg.)

Industrial Control

18 **"Electronic Controller with an Equilibrium Sustaining Mode"**
(3500 series)
Discusses a controller formed with two operational amplifiers in a pulse width modulation circuit with feedback. The feedback operates from a heater through the medium being heated to sense amplifiers.
Burr-Brown AN-63 (2 pg.)

19 **"Sequential Industrial Control Using the IM5200 FPLA"**
(IM5200)
Describes theory and advantages of using this FPLA. Example included.
Intersil Application Bulletin MB0001 (6 pg.)

20 **"Variable Speed Control System for Induction Motors"**
(MC673, MC688)
Describes control scheme implemented with discrete components and IC logic coupled by an LED and a photo transistor. Gives example of a circuit used to drive a Class F, 60 Hz, permanent-split, capacitor induction motor with a 13 oz. in. load rating.
Motorola AN-575A (5 pg.)

21 **"A ROM-Digital Approach to PWM-Type Speed Control of AC Motors"**
Describes a pulse width modulation scheme to control motor speed. Shows a CMOS-ROM system to provide variable frequency drive for 1, 2, or 3 phase motors.
Motorola AN-733 (12 pg.)

22 **"A Variable Frequency Control for 3φ Induction Motors"**
Describes a variable frequency, variable voltage drive system for 3-phase induction motor controls.
Motorola AN-766 (10 pg.)

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Industrial Control (cont)

1 **"Temperature Measurement Method Based on Matched Transistor Pair Requires No Reference"**
(MAT-01, OP-10)
Discusses properties of matched transistor pairs, then describes temperature measuring systems built with a matched pair, constant current sources, and a differential amplifier (OP-10)
Precision Monolithics AN-12 (8 pg.)

2 **"TCA600/900 and TCA610/910 Integrated Motor Speed Regulators"**
(TCA600, TCA610, TCA900, TCA910)
Introduces speed regulator basic and describes device performance. Portable and car mounted applications are depicted.
SGS-ATES Technical Note 113 (10 pg.)

3 **"Signetics Analog Manual"**
(μA723, LM381, LM382, MC1488, MC1489, MC1496, PA239, ULN2111, 521, 522, 526, 529, 540, 542, 550, 555, 560, 561, 562, 565, 566, 569, 592) Covers linear IC processing and design, operation amplifier characteristics and applications, voltage regulators, interface circuits, timers, communications circuits, consumer circuits, phase locked loops, and DMOS devices (314 pg.) and data sheets (321 pg.)
Signetics $5.95 (635 pg.)

Instrumentation

Also see Converters

4 **"Application Notes AN-205"**
(FX205)
Describes use of the FX205 pseudo sinewave generator as a tone generator, tone-burst generator, a divide by eight sinewave source and an fsk generator.
Consumer Microcircuits of America AN-205 (16 pg.)

5 **"A Digital Voltmeter Using the AY-5-3507"**
(AY5-3507)
Gives schematics for the analog section, reference voltage generator, clock oscillator, and display circuitry required in addition to this logic IC to build a 3½ digit voltmeter.
General Instrument Microelectronics (5 pg.)

6 **"A Precision Waveform Generator and Voltage Controlled Oscillator"**
(8038)
Discusses the 8038 circuit and operation. Covers external adjustments, power-supply connections, frequency modulation, sweeping, and use in phase locked loops.
Intersil Application Bulletin A012 (8 pg.)

7 **"Low Cost Digital Panel Meter Designs"**
(ICL7106, ICL7107)
Supplies complete assembly instructions for Intersil's LCD and LED evaluation kits as well as descriptions of individual components.
Intersil A023 (6 pg.)

8 **"The Integrating A/D Converter"**
See (Linear) Converters (Intersil)

"A 3½ Digit DVM Using an Integrated Circuit Dual Ramp System"
(MC1405, MC14435)
Describes a complete digital voltmeter based on the MC1405/14435 device pair. Includes input buffers and autopolarity.
Motorola AN-746 (6 pg.)

Instrumentation (cont)

9 **"Applications of MC1405/MC14435 in Digital Meters"**
(MC1405, MC14435)
Provides a detailed applications reference for this two chip, dual slope A/D converter system.
Motorola AN-748 (18 pg.)

10 **"Solid State Altimeter for Transponder Applications"**
(LX3702)
Describes a solid state altimeter using a pressure transducer. The unit provides an altitude transmission code for use with transponders, plus digital readout.
National AN-109 (8 pg.)

11 **"Wide Range Function Generator"**
Construction of a function generator for sine waves as well as square and triangular waveforms that operates below 10 Hz up to 1 MHz, with usable output to approximately 2 MHz. Design technique, circuit design, and construction directions.
National AN-115 (4 pg.)

12 **"Dual Polarity 3½ Digit DVM Realized with Simple CMOS Interface"**
(ADC3711, LF11300)
Describes an auto-zero, auto-polarity 3½-digit DVM using the LF-11300 and the MM74C928 (ADC3711).
National AN-165 (2 pg.)

13 **"LM2907, LM2917 Tachometer/Speed Switch Building Block Applications"**
(LM2907, LM2917)
Covers basic circuit and use. Applications illustrated include: speed switch, analog display driver, automotive tachometer, motor speed controls, skid sensor, A/D converter, frequency doubler.
National Linear Applications Handbook, Vol. II, AN-162 (16 pg.)

14 **"RMS Converters and Their Applications"**
(LH0091)
Covers RMS converter basics and specifications. Sketches applications including spectrum analysis, harmonic distortion, noise, vibration analysis, and DVM uses.
National AN-180 (4 pg.)

15 **"A Fully Differential Input Voltage Amplifier"**
(LM3900)
Describes operation of instrumentation amplifier built with LM3900. Also shows how a transducer bridge amplifier system can be developed with LM3900.
National Linear Applications Handbook, Vol. I, LB-20 (2 pg.)

16 **"Precise Tri-Wave Generation"**
(LM118, LM119)
Describes triangle-wave generator consisting of the LM118 integrator and two LM119 comparators. Discusses applications including VCO, regulator and operational amplifier testing.
National Linear Application Handbook, Vol. II, LB-23 (2 pg.)

17 **"3½ Digit DVM Demonstrator Board"**
(LD110, LD111)
Supplies the schematics, parts-list and art-work for a DVM demonstrator board.
Siliconix DA74-1 (4 pg.)

18 **"LD130 ±3 Digit DVM Demonstrator Board"**
(LD130)
Presents a DVM circuit and the PC board layout used to build a demonstrator board.
Siliconix DA76-2 (2 pg.)

Instrumentation (cont)

1 **"Build an Autoranging DMM with the LD130 A/D Converter"**
(LD130)
Discusses the construction of a DMM using this device.
Siliconix DA76-3 (7 pg.)

2 **"Build a Portable 0 to 99.9°F Liquid Crystal Display Thermometer"**
(DF411, LD130)
Furnishes all pertinent equations, component lists, schematics, and the PC foil pattern need to build a battery operated thermometer.
Siliconix DA77-1 (4 pg.)

3 **"LD120/LD121 4½ Digit DVM"**
(LD120, LD121)
Details construction of a DVM using these devices.
Siliconix DA77-2 (4 pg.)

4 **"EPN2100 Thermal Printer"**
(EPN2100)
Detailed discussion of this solid state thermal printer and its interface requirements.
Texas Instruments Application Report CA-163 (6 pg.)

5 **"EPN2500 Thermal Printer"**
(EPN2500, SN74492, SN4495, TMS2502)
Discusses this thermal printer and its interface requirements. Includes a description of the SN75495 Row Driver and the SN75492 Digit Driver to interface the printhead to MOSFET logic circuits, and the TMS2502 character generator for providing alphanumeric characters.
Texas Instruments Application Report CA-175 (10 pg.)

Modulators

6 **"MC1596 Balanced Modulator"**
(MC1496, MC1596)
Describes device operation and applications, including modulators and demodulators for AM, SSB, and suppressed carrier AM, frequency doublers; and HF/VHF double balanced mixers.
Motorola AN-531 (12 pg.)

7 **"Simplifying Converter Design with a New Integrated Regulating Pulse Width Modulator"**
(SG1524, SG2524, SG3524)
Describes various functions within the device and describes such applications as a low current polarity converter, a DC to DC converter, and a +5 to ±15V flyback converter.
Silicon General (7 pg.)

8 **"Deadband Control with the SG1524 Regulating Pulse Width Modulator Circuit"**
(SG1524, SG2524, SG3524)
Discusses techniques to control the amount of deadband in push-pull inverter applications.
Silicon General Linear Brief 6 (1 pg.)

Multipliers

9 **"AD530 Complete Monolithic Multiplier, Divider, Square Rooter"**
(AD530)
Describes the device, its circuit, external connections and adjustments. Applications include use in a precision rectifier, a phase sensitive demodulator, an automatic level control, a voltage controlled filter, a voltage controlled oscillator, an amplitude modulator and a frequency discriminator.
Analog Device Technical Bulletin (11 pg.)

10 **"A Practical Guide to Applying IC Multipliers"**
Describes theory, gives definitions, covers use in dividers, squares, vector summation, rms to dc conversion, 2ϕ oscillator, and balanced modulators.
Analog Devices (11 pg.)

11 **"Reducing the Total Error of the AD530, AD531, AD532, and AD533 Multipliers"**
(AD530, AD531, AD532, AD533)
Describes method of empirically reducing errors using external resistors.
Analog Devices Application Brief (2 pg.)

12 **"Analog Modules Multiply User's Options"**
Discusses various types of multipliers, logarithmic converters, dividers and square rooters, peak detectors and comparing circuits. Applications: electron beam welder, 3-mode carriage control, position control, fog visionmeter, optical measuring system, and lab pressure standard.
Burr-Brown AN-55 (6 pg.)

13 **"A Primer on Analog Multiplier Specifications"**
Discusses dc and dynamic performance specifications, including output and input offset, gain error, linearity, small signal and full power frequency response, output slewing rate, and settling time.
Burr-Brown AN-51 (6 pg.)

14 **"Analog Shaping"**
(4301)
Describes the use of the 4301 multifunction circuit which has the transfer function XY/Z. Includes rms to dc conversion, exponentiation, trigonometric functions, vector computation, and use as a log amp.
Burr-Brown AN-70 (5 pg.)

15 **"Function Circuits, Design and Applications"**
See listing under (Linear) General (Burr-Brown)

16 **"Analysis and Basic Operation of the MC1595"**
(MC1495, MC1595)
Gives equations for the analysis of this linear four-quadrant multiplier and discusses characteristic performance. Covers multiplication, division, mean squares, square roots, roots and powers.
Motorola AN-489 (14 pg.)

17 **"Wideband Amplifier/Multiplier"**
(SG1402)
Operation and applications of the SG1402. Describes use as a single-ended variable gain amplifier, a modulator, and a demodulator.
Silicon General Linear IC Product Guide (4 pg.)

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Multipliers (cont)

1 **"Dual Linear-Antilog Voltage Controlled Amplifier"**
(SSM2000, SSM2020)
Discusses control circuits, voltage controlled amplifier, four quadrant multiplier, voltage controlled filter and voltage controlled quadrature oscillator applications.
Solid State Music (4 pg.)

Phase Locked Loops

2 **"Precision PLL System Using the XR2207 and the XR2208"**
(XR2207, XR2208)
Defines phase locked loop parameters and describes this two-chip PLL system. Includes circuit interconnections for both single supply and split-supply operation. Also gives PLL design equations.
Exar TB-1002 (6 pg.)

3 **"The μA758, a Phase-Locked Loop FM Stereo Multiplex Decoder"**
See listing under (Linear) Consumer, AM/FM. (Fairchild)

4 **"Introduction to the Phase Locked Loop"**
(HA-2820)
General discussion of phase locked loops. Describes applications including a bandpass filter, FM receivers, data modems and synchronizers, a motor speed control, and a frequency synthesizer. Discusses features of HA-2800 and 2820 PLL.
Harris Application Note 601 (7 pg.)

5 **"A General Analysis of the Phase Locked Loop"**
Discusses a linear model, stability considerations and steady state response for phase locked loops.
Harris Application Note 602 (8 pg.)

6 **"The HA-2820/2825 Low Frequency Phase Locked Loop"**
(HA-2820, HA-2825)
Explains circuitry of these phase locked loops in 0.1 Hz to 3 MHz operation. Discusses methods for obtaining parameters of a linear model from device's performance curves. External connections are illustrated with an FM demodulator circuit.
Harris Application Note 605 (7 pg.)

7 **"MTTL and MECL Avionics Digital Frequency Synthesizer"**
Describes phase detector, emitter coupled oscillator, prescaler, programmable counter and gives phase locked loop analysis, for a 118 MHz to 136 MHz synthesizer.
Motorola AN-532A (10 pg.)

8 **"Phase-Locked Loop Design Fundamentals"**
(MC4016, MC4024, MC4044, MC4316, MC4324, MC4344)
Outlines fundamental design concepts for phase locked loops implemented with ICs. Gives equations using Laplace Transforms needed to evaluate the basic loop performance and briefly describes a design using MC4000 series devices.
Motorola AN-535 (11 pg.)

9 **"A New Generation of Integrated Avionic Synthesizers"**
Discusses several different types of servo phase locked loop systems and describes a synthesizer for avionic equipment.
Motorola AN-553 (9 pg.)

Phase Locked Loops (cont)

10 **"A Frequency Synthesizer for Aircraft Automatic Direction Finding Systems"**
(MC4016, MC4044, MC1658)
Describes a phase locked loop frequency synthesizer, which includes a MC4016 programmable decade counter, a MC4044 phase detector, and a MC1658 voltage controlled multivibrator.
Motorola AN-594 (10 pg.)

11 **"An ADF Frequency Synthesizer Utilizing Phase-Lock-Loop ICs"**
(MC1648, MC3062, MC4016, MC4018, MC4044, MC7400)
Describes circuit for a synthesizer suitable for the local oscillator function in aircraft Automatic Direction Finder equipment. Covers programming, trouble shooting, power supply requirements, performance, circuit modifications, and circuit construction.
Motorola AN-564 (9 pg.)

12 **"Crystal Switching Methods for MC12060/MC12061 Oscillators"**
(MC12060, MC12061)
Discusses methods of using diodes as rf switches to select crystals for these oscillators. The techniques are useful for electronic selection of one of a group of crystals with minimum disturbance to the series resonant frequency of the selected crystal.
Motorola AN-756 (5 pg.)

13 **"A Medium Cost PLL Varactor Tuning System Utilizing Off-the-Shelf Logic"**
See listing under (Linear) Consumer, TV (Motorola)

14 **"A Phase-Locked Loop Tuning System for Television"**
See listing under (Linear) Consumer, TV (Motorola)

15 **"The Phase-Locked Loop IC as a Communication System Building Block"**
(LM565, LM1496, LM1596)
Discusses basic phase locked loop operation, design considerations, noise performance and describes the IM565 circuit. Applications: IRIG channel demodulator, FSK demodulator, and weather satellite picture demodulator.
National Linear Applications Handbook, Vol. I, AN-46 (12 pg.)

16 **"SL650 Phase-Locked Loop Applications"**
(SL650, SL651)
Describes the circuit and application of this device that can operate to 0.5 MHz. Applications: Modulators-AM, FM, FSK, PAM, SCAM, tone burst, phase shift, delta, PWM, Waveform Generators-sine, triangle, mark/space ratio, staircase: Demodulators; Modem Systems, and a Digital Voltmeter.
Plessey Semiconductor SL650 Applications (32 pg.)

17 **"Applications of the COS/MOS CD4059A Programmable Divide-by-N Counter: Digital Frequency Synthesis for FM Tuners and CB Transceivers"**
(CD4059)
Discusses frequency synthesis using the counter for an FM digital tuner and a CB transceiver.
RCA ICAN-6374 (12 pg.)

18 **"Low-Power Digital Frequency Synthesizers Utilizing COS/MOS ICs"**
(CD4000 Series)
Reviews digital phase-locked loops. Describes their implementation with CMOS for use in FM receiver synthesizers, both heterodyne and prescaling types.
RCA ICAN-6716 (15 pg.)

Photosensitive Devices

1 **"Light Sense"**
Covers optoelectronic sensors and systems including light activated switches and selfscanned photodiode arrays.
Integrated Photomatrix $6.00 (147 pg.)

2 **"Applications of Reticon Photodiode Arrays in Electron and X-Ray Detectors"**
(RL Series)
Describes the use of self-scanning photodiode arrays for detecting soft X-rays (1 to 10A) and electrons in the 10 to 100 KEV range.
Reticon Application Note 101 (4 pg.)

Power Control

3 **"A Monolithic Zero-Crossing AC Trigger (Trigac) for Thyristor Power Controls"**
(μA724)
Describes the μA742 zero-crossing ac trigger, which minimizes radio frequency interference generation. Discusses the circuit and operation of this device. Covers application with an SCR in a half wave circuit, full wave circuits, isolated system connections, and multi-phase power systems.
Fairchild Application Note 208 (5 pg.)

4 **"A 20 KHz, 1 KW Line Operated Inverter"**
Describes application in 208-volt, line-operated, computer mainframe power supply. The output capability of the inverter is 5 v at 200 amp.
Motorola AN-588 (6 pg.)

5 **"Servo Motor Drive Amplifiers"**
Discusses design of transformerless, AC servo amps using power Darlington transistors and IC op amps. Describes two power amplifiers, one using a 28 v power supply, the other, high voltage transistors. Also covers four op amp preamps and 90° phase shifters.
Motorola AN-590 (7 pg.)

6 **"Pulse Width Modulation for Small DC Motor Control"**
(MC1458, MC1709, MC14011)
Discusses several circuits, using discrete, operational amplifier and IC devices, for developing pulse width modulation drive signals. Describes how these signals can control the speed of small motors, primarily permanent magnet type.
Motorola AN-705 (4 pg.)

7 **"Phase Control of AC Power with the SL440"**
(SL440)
Describes the operations of the SL440 power control circuit, and supply requirements. Applications include use with inductive loads, three phase systems, lighting, heating, motor and power supply control.
Plessey Semiconductor (38 pg.)

8 **"Some Applications of a Programmable Power Switch/Amplifier"**
(CA3094)
Brief circuit description of CA3094. Device delivers three watts average power, 10 watts peak power to external load. Applications include Class A power amplifiers and driver amplifiers for complementary transistors, wideband power multivibrators, oscillators, comparators, voltage regulators, analog timers, and motor-speed controllers.
RCA ICAN-6048 (12 pg.)

Power Control (cont)

9 **"Triac Power Controls for Three-Phase Systems"**
(CA3059)
Describes basic approach to designing triac control circuits for use in the switching of three-phase power. Outlines basic design rules and describes CA3059 zero-voltage switch. Discusses methods of isolation of dc logic circuitry. Covers recommended configurations for power control circuits.
RCA AN-6054 (6 pg.)

10 **"Features and Applications of RCA IC Zero-Voltage Switches"**
See listing under (Linear) Switches. (RCA)

11 **"ICs for Phase and Burst Control of SCR or Triac"**
(L120, L121)
Examines 2 ICs which are suitable for SCR and Triac firing. Description includes diagrams, equations, and applications in ON-OFF control and proportional control.
SGS-ATES Technical Note 116 (12 pg.)

12 **"A Monolithic Amplifier-Detector SCR Firing Circuit"**
(ULN-2300)
Describes the operation of the ULN-2300 linear differential amplifier with integral SCR. Covers response, impedance characteristics and closed loop charactertistics, open loop gain vs. temperature, and describes use as a sensitive control, as a drive amplifier in a typical control system and as a control for counters, relays, motors.
Sprague Electric TP69-4 (12 pg.)

13 **"Applications of High-Voltage/High-Current Monolithic Interface Circuits"**
(060, 400 Series, 500 Series)
Application of Series 060 Dual Darlington Switch and Series 400/500 Power Drivers in aircraft lamp drive circuit, solenoid printer, and 4-phase bipolar stepping motor.
Sprague Electric TP 72-4 (5 pg.)

Power Supplies

14 **"Power Supply Design Using the ICL8211 and ICL8212"**
(ICL8211, ICL8212)
Describes use of these devices as positive and negative voltage regulators, constant current sources, high voltage and overvoltage protection circuits, supply window detectors and power failure-shutdown systems.
Intersil A027 (8 pg.)

15 **"Fast IC Power Transistor with Thermal Protection"**
(LM195)
Circuit design of the LM195 IC power transistor, a three terminal device with safe area protection plus current and thermal limiting. Applications: 6 amp variable output switching regulator, 1 amp positive and negative voltage regulators, time delay circuit, and optically controlled switch, power amplifier and voltage follower.
National AN-110 (6 pg.)

16 **"+5 to −15 Volts DC Converter"**
(LM311)
Describes use of the LM311 comparator for this voltage conversion.
National Linear Applications Handbook, Vol. I, LB-18 (2 pg.)

17 **"General Purpose Power Supply"**
(LM395)
Diagrams a 25V, 10A supply using parallel LM395s for pass elements. elements.
National Linear Applications Handbook, Vol. II, LB-28 (2 pg.)

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Preamplifiers

1 **"Applications of the μA739 and μA749 Dual Preamplifier Integrated Circuits in Home Entertainment Equipment"**
See listing under (Linear) Consumer, Audio. (Fairchild)

2 **"Audio Handbook"**
See listing under (Linear) Consumer, Audio (National)

3 **"LM381 Low Noise Dual Preamplifier"**
(LM381)
Describes the circuit. Discusses application as various tape amplifiers, phono preamplifier, and an audio mixer.
National AN-64 (12 pg.)

4 **"LM381A Dual Preamplifier for Ultra-Low Noise Applications"**
(LM381)
Gives detailed description of circuit operations of LM381A.
National AN-70 (4 pg.)

5 **"IC Preamp Challenges Choppers on Drift"**
(LM108A, LM121)
Describes circuit of the IM121 preamplifier and discusses offset balancing, achieving of low drift, and typical operating performance. Also covers effects of the associated operational amplifier citing the LM108A as an example.
National AN-79 (8 pg.)

6 **"Versatile IC Preamp Makes Thermocouple Amplifier with Cold Junction Compensation"**
(LM321, LM308A)
Discusses use of LM321 preamp with LM308A operational amplifier to form a precision, low-drift operational amplifier that also acts as a cold junction compensator.
National Linear Application Handbook, Vol. II, LB-24 (2 pg.)

Regulators

7 **"The Voltage Regulator Applications Handbook"**
(μA104, μA105, μA109, μA723, μA7600, μA7800, μA78L00, μA78M00, μA79E00)
Gives specifications and parameters for various IC regulators and includes a selection guide. It devotes two chapters to each major regulatory family, the first chapter describes design and electrical characteristics, the second discusses electrical and thermal considerations which are useful as application guidelines.
Includes appendices covering switching regulator and power supply design and a guide to the selection and operation of suitable power transistors. Applications of 7800 and 78M00 include fixed output, current and dual polarity regulators.
The 79E00 applications include use as a high current negative voltage regulator. The 723 is discussed in 150 mA maximum, positive shunt regulators with high line rejection or high input voltage, floating positive regulators, medium/high output current negative regulators, and several other applications.
The 104, 105, and 109 applications include high current, switching and floating regulators.
Fairchild Voltage Regulator Applications Handbook (96 pg.)

8 **"Designing Digitally-Controlled Power Supplies"**
(MC1406, MC1408, MC1466, MC1723)
Discusses two approaches to designing power supplies, one using the MC1723 voltage regulator, the other using the MC1466 floating regulator with optoelectronic isolation. Also discusses BCD-to-binary converter and memory options.
Motorola AN-703 (8 pg.)

Regulators (cont)

9 **"A New Approach to Switching Regulators"**
Describes a 24 volt 3 ampere switching mode supply which operates at 20 kHz from a 120 volt AC line with 70% efficiency. Briefly discusses load-line shaping to reduce power losses and to reduce noise.
Motorola AN-719 (11 pg.)

10 **"Voltage Regulator Handbook"**
(MC78L00, MC78M00, MC7700, MC7800, MLM109, MLM209, MLM309, MC79L00, MC7900, MLM105, MLM205, MLM305, MLM104, MLM204, MLM304, MC1723, MC1469, MC1569, MC1463, MC1563, MC1468, MC1568, MC1466, MC1566, MC3420, MC3423, LM117, LM317, LM123, LM323)
Discusses basic voltage regulator theory and design including such relevant topics as series pass elements, heatsinking, layout, input power supply design, reliability, and troubleshooting. Also contains product data sheets.
Motorola $2.50 (202 pg.)

11 **"A Versatile, Monolithic Voltage Regulator"**
(LM100)
Circuit operation. Applications for the LM100 between 2 v to 30 v (up to 2 amps with two external transistors) are discussed. Includes high power, switchback current limiting, negative voltage, temperature compensating, and switching regulators.
National Linear Applications Handbook, Vol. I, AN-1 (11 pg.)

12 **"Designing Switching Regulators"**
(LM100)
LM100 applications discussed include high current, driven switching, current limiting, negative and high voltage regulators, as well as switching, and linear regulator combinations.
National Linear Applications Handbook, Vol. I, AN-2 (12 pg.)

13 **"Tracking Voltage Regulators"**
(LM104, LM105, LM204, LM205, LM304, LM305)
Describes adjusting several regulator voltages with one potentiometer, tracking positive and negative regulators using the LM104 as an amplifier, and tracking regulators with different output voltages.
National Linear Applications Handbook, Vol. I, LB-7 (2 pg.)

14 **"New Uses for the LM100 Regulator"**
(LM100)
Applications include shunt regulator, switching regulator with overload shutoff, temperature controller, power amplifier, SSB transmitter, light-intensity regulator, and photomultiplier tube supply.
National Linear Applications Handbook, Vol. I, AN-8 (12 pg.)

15 **"IC Regulators Simplify Power Supply Design"**
(LM104, LM105, LM204, LM205, LM304, LM305)
Describes use of LM104 and LM105, in 0.2 and 2A regulator circuits. Provides circuit construction hints.
National Linear Applications Handbook, Vol. I, LB-10 (2 pg.)

16 **"High Stability Regulators"**
(LM108A, LM109, LM208A, LM209, LM308A, LM309)
Describes design and gives schematics for high stability positive and negative regulators using LM109 and LM108A.
National Linear Applications Handbook, Vol. I, LB-15 (2 pg.)

Regulators (cont)

1 "Designs for Negative Voltage Regulators"
(LM104, LM204, LM304)
Describes the LM104 and covers pitfalls that cause unexpected failures as well as protection schemes. Including discussions of high current regulators, symmetrical power supplies, high voltage regulators, switching and high current switching regulators, and driven switching regulators.
National Linear Applications Handbook, Vol. I, AN-21 (16 pg.)

2 "The LM105 — An Improved Positive Regulator"
(LM105, LM205, LM305)
Describes the circuit of this regulator, power limitations, using booster transistors, foldback current limiting, and dominant failure mechanisms.
National Linear Applications Handbook, Vol. I, AN-23 (8 pg.)

3 "IC Provides On-Card Regulation for Logic Circuits"
(LM109, LM209, LM309)
Discusses design of regulators in general and describes the LM109. Covers application as a fixed 5V regulator, adjustable-output regulator, current regulator and high stability regulator.
National AN-42 (6 pg.)

4 "LM125/LM126/LM127 Precision Dual Tracking Regulators"
(LM125, LM126, LM127)
Circuit description, operation and applications, including current boosting, are discussed along with charts depicting external current limiting characteristics and a discussion of foldback current limiting. Electronic turn-off of the output without removing the input voltage is also described.
National AN-82 (15 pg.)

5 "LM340 Series — Three Terminal Positive Regulators"
(LM340)
Describes this 1 ampere regulator circuit. Applications: constant current source, high current regulator with short circuit current limit, 5 v regulator for TTL, adjustable output voltage regulators, tracking dual regulator, and high voltage regulators.
National AN-103 (12 pg.)

6 "Constant Current LED"
(NSL4944)
Describes how this two lead LED/IC device can be used not only as an indicator but also as a rectifier and constant current source.
National AN-153 (4 pg.)

7 "Applications for an Adjustable IC Power Regulator"
(LM117, LM217, LM317)
Covers basic LM117 circuit operation. Shows basic applications plus use for multiple outputs, current regulation, constant voltage/constant current, and a voltage to 2-wire (10-50 ma) current transmitter.
National AN-178 (4 pg.)

8 "Three-Terminal Regulator is Adjustable"
(LM117, LM217, LM317)
Covers basic LM117 circuit operation, overload protection circuits and operating considerations. Includes applications with logic shutdown, multiple regulators with single control, switching regulators and battery chargers.
National AN-181 (3 pg.)

Regulators (cont)

9 "Improving Power Supply Reliability with IC Power Regulators"
(LM117, LM217, LM317)
Describes various regulator circuit design practices to improve system reliability.
National AN-182 (3 pg.)

10 "Worst Case Power Dissipation in Linear Regulators"
(LM100, LM104, LM200, LM204, LM300, LM304)
Discusses problems of excessive dissipation in regulators and suggests solutions using LM100 and LM104.
National Linear Applications Handbook, Vol. I, LB-3 (2 pg.)

11 "Adjustable Three-Terminal Regulator for Low Cost Battery Charging Systems"
(LM317)
Discusses the ability to adjust the output of the LM317 voltage regulator as it relates to battery charging systems.
National LB-35 (2 pg.)

12 "A Novel FET Micropower Voltage Regulator"
Depicts the building of a micropower voltage regulator using FETs.
National FET Databook (2 pg.)

13 "Voltage Regulator Handbook"
(LM109, LM120, LM123, LM125, LM126, LM127, LM145, LM340, LM341, LM342, LM7800, LM78L00)
Covers product selection; heat flow and thermal resistance; commercial and custom heat sinks; applications of positive, negative and dual regulators; power supply design and includes data sheets for the product families listed above.
National Voltage Regulator Handbook, $3.00 (139 pg.)

14 "The 4195 Regulator"
(RC4195, RM4195)
Describes application as a ±15 v, 100 ma regulator; a ±2.5 a regulator; a ±15 to ±50 v unit, or a complementary ±3 to ±27 v device.
Raytheon Semiconductor Application Note (9 pg.)

15 "Applications of the CA3085 Series Monolithic IC Voltage Regulators"
(CA3085)
Circuit description of positive regulators with output currents up to 100 milliamperes from −55°C to +125°C. Applications include high-current and constant-current regulators; switching, dual-tracking and high-voltage regulators. Use as a general purpose amplifier, and various methods of current limiting are mentioned.
RCA ICAN-6157 (11 pg.)

16 "A Switching Regulator Using an RCA P-N-P Power Darlington Transistor"
(CA3085)
Gives a detailed discussion of a 28 v input, 4-16 v, 11 a, switching regulator.
RCA AN-6195 (8 pg.)

17 "Using a Dual-Polarity, Tracking Voltage Regulator"
(SG1501, SG2501, SG3501)
Describes the circuit and use of the SG1501 series of dual regulators.
Silicon General Applications Bulletin 1 (6 pg.)

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Regulators (cont)

1 **"Designing Switching Voltage Regulators with the TL497"**
(TL497)
Covers principals of operation and use as a step-down, step-up or inverting regulator.
Texas Instruments Application Report CA-189 (16 pg.)

Switches

2 **"Applications of the μA742 TRIGAC — A Zero Crossing AC Trigger"**
(μA742)
Describes this TRIGAC circuit. Includes a discussion of the transfer characteristics and performance plus operation from ac and dc supplies. Applications: 110 V ac single threshold control; single phase, 110 V ac dual threshold control with hysteresis; 110 V ac dual threshold control with time proportioning; with time proportioning for Y or Δ loads; operating with transformer isolation between control circuit and ac line; output pulse amplifier with transformer; output pulse inverter; period extender for time proportioning; initial cycle delay; sensor failure detection circuit; time delay "relay" circuit; 208V ac dual threshold control 110V ac, 400 Hz dual threshold control with single TRIGAC for Y loads.
Also includes a section listing parts and component location diagrams for these applications and discusses operation with a fixed dc supply. Covers use of the TRIGAC with nonresistive loads, discusses thyristor cells, and full wave output power switches for use with the device.
Fairchild (30 pg.)

3 **"Understanding and Applying the Analog Switch"**
(IH5001, IH5009, IH5025, IH5040)
Compares parameters of analog switches. Applications of several switch families are discussed, including 3-channel differential multiplexer, gain programmable amplier, gain ranging circuit, sample and hold circuit.
Intersil Application Bulletin A003 (16 pg.)

4 **"The IH5009 Series of Low Cost Analog Switches"**
(IH5009 Series)
Describes circuit parameters, logic compatibility, and virtual ground switching applications including 4-channel multiplexer, gain ranging circuit, gain programmable amplifier and 16-channel multiplexer.
Intersil Application Bulletin A0004 (8 pg.)

5 **"A New CMOS Analog Gate Technology"**
General discussion of "latch up." Describes "floating body" process, which eliminates this problem.
Intersil Application Note A006 (2 pg.)

6 **"Application of the MC3416 Crosspoint Switch"**
(MC3416)
Describes operation and use of this 4 × 4 balanced crosspoint switch in telephone applications including PABX. Appendices cover dielectric isolation, SCR action and testing.
Motorola AN-760 (15 pg.)

7 **"High Speed MOS Commutators"**
(MM451, MM453, MM454)
Discusses the lowered threshold voltages in commutators, on and off resistances, switching speed, noise and high-frequency noise control.
National Linear Applications Handbook, Vol. I, AN-28 (8 pg.)

Switches (cont)

8 **"Analog-Signal Commutation"**
(MM450, MM451, MM454, MM550, MM551, MM552)
Describes dc characteristics involved in MOS IC switching of analog signals when the signal input range varies between ± 10 v.
National Linear Applications Handbook, Vol. I, AN-33 (6 pg.)

9 **"Applications of MOS Analog Switches"**
(LH0014, LH0019)
Discusses basic commutation circuits and describes the use of the LH0014 and LH0019 in linear amplifier applications, including reset functions and chopper circuits. Covers use of MOS switches as suppressed carrier double-sideband modulators and double-sideband demodulators. Also describes a circuit for a phase-locked loop AM-FM detector without tuned circuits.
National Linear Applications Handbook, Vol. I, AN-38 (8 pg.)

10 **"PIN Diode Drivers"**
(DH0035, DH0035C)
Describes PIN diode switching requirements and application of DH0035 as a driver. Includes discussion of anode ground and cathode ground designs and of repetition rate considerations.
National AN-49 (6 pg.)

11 **"High Speed Analog Switches"**
(AM1000, AM1001, AM1002)
Discusses time domain multiplexing, current mode multiplexing, the switching characteristics of the AM1000 J-FET switches, and drive circuits.
National AN-53 (6 pg.)

12 **"Features and Applications of RCA IC Zero-Voltage Switches"**
(CA3058, CA3059, CA3079)
Discusses zero-voltage switch operation in general. Operation primarily with thyristors in ac power control and switching applications, including electric heating, oven/broiler control, machine control, light control and industrial systems.
RCA ICAN-6538 (6 pg.)

13 **"Applications of the RCA CA3062 IC Photo-Detector and Power Amplifier in Switching Circuits"**
(CA3062)
Describes circuit operation and application in a latched memory circuit, a light activated triac control, a triac control with automatic shut off and alarm, and a triac intrusion alarm system.
(RCA ICAN-6538 (6 pg.)

14 **"Some Applications of a Programmable Power Switch/Amplifier"**
See listing under (Linear) Power Control. (RCA)

15 **"FETs as Analog Switches"**
General discussion of FET operation: detailed discussion of factors affecting switch performance, including specific load problems and applicable driver circuits.
Siliconix AN72-2 (12 pg.)

16 **"IC Multiplexer Increases Analog Switching Speeds"**
(DG506, DG181)
Describes single and two level IC multiplexing systems, including the advantages and disadvantages of each.
Siliconix AN73-2 (5 pg.)

Switches (cont)

1 **"Switching High-Frequency Signals with FET Integrated Circuits"**
(DG133, DG171, DG181, DG200)
Discussion of DG133/171/181/200 as rf switches. Gives equivalent circuits. "Off" isolation and "On" performance data. Applications: control of video monitor and switching between two video cameras.
Siliconix AN73-3 (16 pg.)

2 **"Driver Circuits for the JFET Analog Switch"**
Discussion and comparison of resistor-coupled diode charge transfer, space transistor charge transfer, and switched resistor driver circuits for JFET switches.
Siliconix AN73-5 (12 pg.)

3 **"Analog Switches in Sample and Hold Circuits"**
Covers the effects of FET analog switch current handling capability on settling time and the effects of offset characteristics on sample and hold system accuracy. Describes inverting and non-inverting sample and hold circuits.
Siliconix AN74-2 (4 pg.)

4 **"CMOS Analog Switches — A Powerful Design Tool"**
Describes CMOS switch construction, characteristics and operating precautions. Applications include: a four channel switch to multiplex a scope input, a low pass filter with digitally controlled frequency response, an amplifier with programmable inputs and gain, a sample and hold circuit, a latching switch, high frequency switching and multiplexer systems.
Siliconix AN75-1 (16 pg.)

5 **"Designing with Monolithic FET Switches"**
Describes MOSFET and JFET switch operation plus driver considerations.
Siliconix TA73-2 (4 pg.)

6 **"Analog Switches and Their Applications"**
(DG300 series, DG506)
Introduces basic semiconductor theory and discusses in detail FET analog switches. Various circuit combinations including driver circuits, multiplexing, sample-and-hold circuits, N-path filters, and converters are also analyzed.
Siliconix $4.00 (324 pg.)

7 **"High Speed CMOS Analog Switches"**
(DG300 Series, DG181 Series)
Discusses the devices in low power, multiplexing, and thermocouple applications. (Includes AN76-6)
Siliconix (24 pg.)

8 **"Magnetically-Activated Monolithic Integrated Circuits for Analog and Digital Applications"**
(ULN-3006)
Discusses the Hall effect, digital sensing and experiments in linear sensing.
Sprague Electric TP 71-11 (10 pg.)

9 **"In IC Form Hall Effect Devices Can Take on Many New Applications"**
(ULN-3006)
Describes the Hall effect, suggests linear and digital applications.
Sprague Electric TP 71-12 (5 pg.)

10 **"Modes of Actuation for Type ULN-3006 'Hall Effect' Switches"**
(ULN-3006)
Describes magnetic operation of this non-contact, switching device.
Sprague Electric Application Note 27404.1 (4 pg.)

Switches (cont)

11 **"Suggested Output Loads for Type ULN-3006 'Hall Effect' Switches"**
(ULN-3006)
Diagrams connections to use the open collector output to drive transistors, thyristors, TTL and MOS circuits.
Sprague Electric Application Note 27404.2 (2 pg.)

12 **"Specifying and Testing Multiplexers"**
Describes how Teledyne Philbrick defines and measures analog multiplexer parameters with emphasis on CMOS types.
Teledyne Philbrick Applications Bulletin AN-31 (4 pg.)

Thermal Considerations

For Temperature Sensors see (Linear) Transducers

13 **"Thermal Evaluation of Integrated Circuits"**
Describes four methods for thermal evaluation, including reverse biasing substrate diodes.
Fairchild Application Note 205 (8 pg.)

14 **"Mounting Procedure for, and Thermal Aspects of, Thermopad Plastic Power Devices"**
Covers various methods of mounting and heat-sinking Motorola case number 77, 90, and 199 plastic power devices. Also discusses thermal resistance considerations, lead forming, and circuit board cleaning.
Motorola AN-290B (9 pg.)

15 **"Transient Thermal Resistance — General Data and Its Use"**
Discusses transient thermal resistance and its use and describes methods using various degrees of approximations to determine the junction temperature rise of a device. Also covers the concept of a duty cycle family of curves to simplify calculation of junction temperature rise under a repetitive pulse train.
Motorola AN-569 (15 pg.)

16 **"Mounting Techniques for Metal Packaged Power Semiconductors"**
Discusses preparation of mounting surfaces, using thermal compounds, and fastening techniques. Gives typical interface thermal resistance for a number of packages.
Motorola AN-599 (5 pg.)

17 **"Low Cost LED Thermometer"**
See listing under (Linear) Transducers. (National)

18 **"Micropower Thermometer"**
See listing under (Linear) Transducers. (National)

19 **"Thermal Resistance of Integrated Circuit Packages"**
Describes method of measuring package thermal resistance while package is immersed in a constant-temperature, circulating oil bath that acts as an infinite heat sink.
Sprague Electric TP 72-7 (5 pg.)

20 **"Thermal Design for Plastic Integrated Circuits"**
(ULN-2277)
Discussion of chip power dissipation—using amplifier as an example, heat dissipation, ULN-2277 dual 2-watt audio power heat sinks, heat sink finishes, and forced air cooling.
Sprague Electric TP 74-1 (7 pg.)

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Thermal Considerations (cont)

1 **"New Heat Sinking Techniques for Hermetic DIPs"**
Describes use of stamped and extruded heat sinks and method of reversing IC die and bonding chip directly to Kovar base.
Sprague Electric TP 74-4 (4 pg.)

Timers

2 **"Single-Chip Frequency Synthesizer Employing the XR2240"**
(XR2240)
Describes use of this timer/counter as a single-chip frequency synthesizer: $f_o = f, (m/n + 1)$ Where $f_o < 200$ kHz. Describes generating 100 Hz synchronized to 60 Hz line.
Exar TB-1003 (3 pg.)

3 **"Precision Timer"**
(ZN1034E)
Explains the device and its use in various applications including a wiper control, a metronome, and a battery charger.
Ferranti Electric (19 pg.)

4 **"Versatile Timer Operates from Microseconds to Hours"**
(LM122)
Describes the LM122 circuit and its operation. Includes discussion of pin functions, timing errors and noisy environments. Discusses use as various timers, as a pulse width detector, a comparator, an oscillator, a two-terminal time delay switch, and a frequency to voltage converter.
National AN-97 (12 pg.)

5 **"Using National Clock Integrated Circuits in Timer Applications"**
(MM5309, MM5311, MM5312, MM5315)
Describes demultiplexing techniques to generate time intervals and low frequency square waves. Gives as an example a fail-safe lighting timer.
National AN-143 (4 pg.)

6 **"1.3 Volt IC Flasher, Oscillator Trigger, or Alarm"**
(LM3903)
Describes circuit operation. Covers various flasher, tone generator and trigger circuits, especially for low voltage applications in anything from toys to laboratory equipment.
National AN-154 (10 pg.)

7 **"MM5865 Universal Timer Applications"**
(MM5865)
Provides block diagram and system description, discusses general timing and programming capabilities, suggests timing and counting applications.
National AN-168 (10 pg.)

8 **"A 4-Digit, 7-Function Stop Watch/Timer"**
(MM5865)
Gives detailed instructions for the circuit and construction of a 4-digit, 7-function timer with a display resolution of 0.01, 0.1, and 1 second, using the MM5865.
National AN-169 (14 pg.)

9 **"Problem Solving with the Dual Set Point Timer"**
(DF215)
Describes the device and its use as various timers and controls.
Siliconix AN76-2 (10 pg.)

Transducers

10 **"The LX1602A Pressure Transducer and Altimeter Applications"**
(LX1602A)
Describes how to use this transducer along with additional electronics to build an altimeter that operates over a range of −1,000 feet to +50,000 feet.
National AN-91 (3 pg.)

11 **"Installation Ideas for Pressure Transducers"**
(LX1600, LX1700, LX1400, LX1701)
Provides suggestions for mounting National transducers for various applications. Includes diagrams and typical mounting configurations.
National AN-92 (4 pg.)

12 **"Transducers in Fluid Flow Applications"**
(LX1602A)
Discusses application of LX1602A in pressure vessel, open flow and closed flow applications.
National AN-93 (8 pg.)

13 **"LX Series Pressure Transducers: Design and Applications Information"**
(LX1600A, LX1601A, LX1602A)
Describes hybrid transducer circuit and applications, including pressure to frequency converter, latching altitude detector, digital readout barometer and altimeter.
National AN-94 (8 pg.)

14 **"Pressure Transducer Load Cell"**
(LX1700G)
Describes use of LX1700G pressure transducer to measure weight.
National AN-95 (4 pg.)

15 **"Pressure Transducers as Accelerometers"**
(LX1700G)
Discusses uses of accelerometers and describes scheme of converting LX series pressure transducers to cover ranges from fractions to thousands of g's.
National AN-96 (4 pg.)

16 **"A New Interfacing Concept: The Monolithic Temperature Transducer"**
(LX5600, LX5700)
Covers alternate methods of powering the LX5600, load isolation and an unusual active thermal shield (the shield tracks the surface temperature of the sensor.) Describes use as a thermal transducer, temperature to frequency converter, and a temperature controller with rate-of-change sensing. Discusses use of differential temperature measurements for liquid or moving air detection (including) wind) and for position sensing (using a heat source as a position reference.
National AN-132 (10 pg.)

17 **"Micropower Thermometer"**
(LX5600)
Describes use of the LX5600 as a thermometer whose ouput is a current proportional to temperature and can drive a meter for direct readout.
National Linear Applications Handbook, Vol. II, LB-27 (2 pg.)
(LX5700)

18 **"Low Cost LED Thermometer"**
Presents circuit for a −40° to 100°C thermometer with a conversion circuit for −40° to 199°F.
National Linear Applications Handbook, Vol. II, LB-30 (2 pg.)

Transducers (cont)

1 **"Crystal Oven Controller and Precision Voltage Reference"**
(LM199,, LM299, LM399, LM199A, LM299A, LM399A)
Shows the use of the LM199 both as an oven temperature controller and a voltage reference at the same time.
National Linear Applications Handbook, Vol. II, LB-31 (2 pg.)

2 **"Simple Temperature Control"**
(LX5600)
Discusses setting up a temperature control system using the LX5600.
National LB-36 (2 pg.)

3 **"The Multi-Level Switch Kit, Part No. SK1007"**
Details the use of any LX series pressure transducer to produce a high level analog output as well as three independent switch points.
National TB-1 (2 pgs.)

4 **"Transducer Sensor Diaphram 15 Million Cycle Life Test"**
Findings in the continuing test of National's transducer sensing elements — a silicon membrane approx. 1 mil. thick.
National TB-3 (1 pg.)

5 **"Use of the SK1007 Pressure Transducer Kit in Vault Alarm Systems"**
Describes application of this multi-level switch kit with a pressure transducer in vault alarm systems.
National TB-7 (2 pg.)

6 **"Transducer Fluid Filled Option"**
Describes the "Fluid-Filled" methods of protecting transducers from hostile environments. Rates the resistance of silicone rubber to some common fluids.
National TB-8 (2 pg.)

7 **"REF-02 Temperature Controller"**
(CMP-02, REF-02)
Describes temperature control using the REF-02 and the CMP-02 comparator.
Precision Monolithics AB-4 (1 pg.)

8 **"Thermometer Application of the REF-02"**
(REF-02)
Discusses thermometer essentials, bandgap voltage reference theory, and basic circuit design using device.
Precision Monolithics AN-18 (4 pg.)

Voltage References

9 **"1.2 Volt Reference"**
(LM113, LM313)
Describes the LM113 temperature compensated shunt regulator diode. Applications: low voltage regulator circuits, bias current source for a differential amplifier, and an electronic thermometer circuit.
National Linear Applications Handbook, Vol. I, (N-56 (4 pg.)

10 **"IC Voltage Reference has 1 PPM per Degree Drift"**
(LM199, LM299, LM399, LM199A, LM299A, LM399A)
Describes this device with a sub surface Zener and an on-chip temperature stabilizer. Several applications are also covered.
National Linear Applications Handbook, Vol. II, AN-161 (6 pg.)

Voltage Reference (cont)

11 **"IC Zener Eases Reference Design"**
(LM129, LM329)
Describes LM129 circuit and operation. Covers use in voltage reference and regulator applications.
National AN-173 (3 pg.)

12 **"References for A/D Converters"**
(LM199, LM399, LM199A, LM399A)
Discusses requirements of references for various accuracies of A/D converters. Gives reference circuit designs.
National AN-184 (4 pg.)

13 **"A Micropower Voltage Reference"**
Describes a voltage reference made by operating a JFET slightly below pinch-off along with an op amp to convert current to voltage.
National Linear Applications Handbook, Vol. II, LB-34 (2 pg.)

14 **"Crystal Oven Controller and Precision Voltage Reference"**
See listing under (Linear) Transducers (National)

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MEMORY

Analog

1 "Delaying AF Signals with MOS Delay-Lines TCA350"
(TCA350)
Discusses bucket brigade circuits and practical applications employing this device.
ITT Semiconductors (pg. 7)

2 "MOS Delay Lines"
(DM8000, DM8510, DM8830, MM506)
Covers use of MOS shift registers to build delay lines.
National MB-4 (2 pg.)

3 "Acoustic Applications of Serial Analog Delay Devices"
(SAD1024)
Covers use in reverberation, vibrato, chorus, wow and flutter control plus considerations in using this device.
Reticon Application Note 104 (8 pg.)

4 "Bucket Brigade Devices Circa 1976"
Gives history of development, construction features, and advantages of bucket brigade devices.
Reticon Technical No. 107 (11 pg.)

5 "A Tapped Analog Delay for Sampled Data Signal Processing"
Introduces tapped analog delays and gives various applications heretofore accomplished by digital techniques.
Reticon Application Note No. 105 (11 pg.)

6 "Serial Operation of Clocked Analog Delay Lines to Obtain Long Delay"
(SAD1024)
Describes advantages, coupling, and performance of device.
Reticon Application Note No. 109 (8 pg.)

7 "Implementation of Discrete-Time Analog Filter and Processing Systems"
(TAD32)
Discusses tapped analog delay device operation and areas of application, including transversal and recursive filters.
Reticon Application Note No. 111 (10 pg.)

8 "Charge Transfer Devices for Sampled-Data Processing"
Discusses the application of charge transfer devices to analog and digital signal processing. Compares CTD devices. Describes Tapped Analog Delay, the Binary Analog Correlator, the Analog Correlator and the Transversal Filter.
Reticon Application Notes No. 114 (11 pg.)

CAMs

9 "Designing with the SCM5533 CMOS Content Addressable Memory"
(SCM5533)
Describes operation, matching, expansion, multifield association, pattern recognition, learning and a target acquisition system.
Solid State Scientific AN-110 (14 pg.)

Character Generators

10 "A CRT Display System Using NMOS Memories"
(MC6545, MCM6570, MCM6571)
Discusses basic crt operation, character formation and describes the 8K-bit MCM6570 character generators. Describes a 128-character system in detail, including counter and retrace control, memory select, and address register sections.
Motorola AN-706A (15 pg.)

11 "American and European Fonts in Standard Character Generators"
(MM4240, MM5240, MM4241, MM5241)
Depicts the standard 64 character subsets for these devices.
National AN-57 (6 pg.)

12 "DM8678 Bipolar Character Generator"
(DM8678)
Explains the operation of the device and the various features which include circuit address latches, the line counter, the 7-bit shift register, and the output buffer.
National AN-167 (4 pg.)

13 "The Systems Approach to Character Generators"
See listing under (Memory) ROMs. (National)

14 "Digital Display Systems"
Using TTL compatible MOS ROMs to generate displays. Gives circuit diagrams and a sample readout.
National MB-8 (2 pg.)

15 "7 x 9 Display Character Generator"
Uses three MOS ROMs and some TTL logic to create a font of 64 7 × 9 dot-type characters. A circut diagram and suggested character forms are provided.
National MB-13 (2 pg.)

Interface

16 "The Recovery of Recorded Digital Information in Drum, Disk and Tape Systems"
Reviews methods for converting the analog signal obtained from a magnetic recording into digital format.
Motorola AN-711 (10 pg.)

17 "Applying Modern Clock Drivers to MOS Memories"
(DS0025, DS0026)
Covers use of 0025/26 drivers in MOS memory systems. Information includes selection of packages and heat sinks, power dissipation, rise and fall time, power supply decoupling, system clock line ringing and crosstalk, input coupling techniques, and sample calculations.
National AN-76 (12 pg.)

18 "Interfacing Circuits for MOS Dynamic Random Access Memories"
Discusses interfacing methods employing level shifters (TTL to MOS levels) with boosters, level shifters (MOS to TTL levels), and sense amplifiers.
Nortec Applications Note No. 25 Rev. A (3 pg.)

interface (cont)

1 **"Charge Pump Driver for 7001 Rams"**
(SN54508)
Defines a method for driving the charge storage pump input of a 7001 RAM. Provides a description of the basic storage pump RAM cell and the charge pump circuit diagram. Gives performance curves.
Texas Instruments Application Report CA-178 (6 pg.)

2 **"High Speed TTL Interfacing for 7001 Static RAMs"**
(SN75261, SN75365)
Illustrates interface techniques for driving the 7001 RAM chip-select input, and sensing the memory output.
Texas Instruments Application Report CA-179 (8 pg.)

Microprogramming

3 **"Tri-State Logic in High Speed Memories of Microprogrammed Computers"**
See listing under (Digital) TTL, General. (National)

4 **"How to Design with the 8X02 Control Store Sequencer"**
See listing under (Microprocessor) Systems (Signetics)

"Signetics Micro Assembler Reference Manual"
See listing under (Microprocessor) Programming (Signetics)

PROMs

5 **"Programming AMI S6834 and S5204A EPROMs"**
(S5204A, S6834)
Compares on-board versus dedicated-socket programming and suggestions on programming system design.
American Microsystems (3 pg.)

6 **"EA2708 EPROM Application Note"**
(EA2708)
Comments on read characteristics of the device and its use in microprocessor systems.
Electronic Arrays (8 pg.)

7 **"Programmable Read Only Memories"**
(93417, 93427, 93436, 93438, 93448, 93452, 93453)
Gives general background on PROMs, describes programming procedures, discusses power switching, address expansion, 8-bit binary to decimal decoding and programmed logic controller.
Fairchild Application Note 333 (16 pg.)

8 **"Application of the Intel 2708 8K Erasable PROM"**
(2708)
Covers characteristics, operation, programming and erasure, reduced power and interface.
Intel Application Note AP-17 (15 pg.)

9 **"Intel Memory Design Handbook"**
See listing under (Memory) RAMs (Intel)

10 **"Programming the MCM5003/5004 Programmable Read Only Memory"**
(MCM5003, MCM5004)
Discusses programming methods for this 64 × 8 bit memory, describes circuit and operation. Describes a simple programmer using five ICs and a more sophisticated version using 25 ICs offering automatic sequencing.
Motorola AN-550 (12 pg.)

PROMs (cont)

11 **"PROM Power-Down Circuits"**
(DM74S287)
Describes several ways to power-down bipolar, three-state PROMs.
National AN-171 (4 pg.)

12 **"A PROM Programmer for the SC/MP LCDS"**
(SC/MP, MM4204, MM5204)
Provides a method for the user of the SC/MP LCDS to program MM4204 PROMs. Using wire-wrap techniques the user can construct a programmer that plugs into the SC/MP LCDS backplane and programs a 512 x 8 PROM in 10 seconds.
National AN-189 (23 pg.)

RAMs

13 **"Application of First-In First-Out Memories"**
(Am2812, Am2813, Am2814, 3341)
Describes the function of a first-in, first-out memory, methods of constructing FIFO buffers and the operation of the above P-channel MOS devices. Discusses storage and control, expansion methods, interfacing, and applications in an N-bit shift register and as a key encoder on key matrix.
Advanced Micro Devices Application Note (9 pg.)

14 **"The AM9338 Multiple Port Memory"**
(9338)
Describes applications for this 8-word by 1-bit three-address memory, including the working store for high-speed, three address computers; first in, first out (asynchronous buffer) memory; and direct address/indirect address memory.
Advanced Micro Devices Application Note 4 (pg.)

15 **"Application of the EMM/SEMI 4200 Static RAM to the Intel 8080A Microprocessor"**
(4200)
Describes suggested logic interface to connect this 4K × 1 static RAM to 8080A MPU.
EMM/Semi Application Note S103A (4 pg.)

16 **"Application of EMM/SEMI 4K Static RAM to Motorola M6800 Microprocessor"**
(4200)
Describes suggested logic interface to connect this 4K × 1 static RAM to the M6800 MPU.
EMM/Semi Application Note S104 (6 pg.)

17 **"Checking Out the EMM/Semi 4200 in 2107B or 4060 Sockets"**
(4200)
Suggests circuit changes to permit acceptance of the 4200 static RAM in sockets wired for 2107B or 4060 Sockets.
EMM/Semi Application Note S102 (2 pg.)

18 **"TTL/MSI 9334 8-Bit Addressable Latch"**
(9334)
Describes operation and applications, including 16 and 32-bit addressable latches, 16-word by 4-bit memory, demultiplexer and decoder, 8-bit A/D converter and a 16-bit serial-to parallel converter.
Fairchild Application Note 220 (8 pg.)

19 **"Understanding the FIFO"**
(3351)
Covers 3351 FIFO operation, cascading, plus use in data rate buffering, parallel operation, and burst operation.
Fairchild APP 332 (8 pg.)

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RAMs (cont)

1 "Designing Non-Volatile Memory Systems with Intel's 5101 RAM"
(5101)
Describes internal circuits and operation of the RAM. Outlines circuit techniques for battery supported non-volatile operation. Describes use of the device with the MCS-40 microcomputer.
Intel Application Note AP-12 (28 pg.)

2 "Which Way for 16k?"
Considers various aspects of 16k RAMs including 64 and 128 cycle refresh and the advantages versus disadvantages of latching.
Intel Application Note AP-22 (7 pg.)

3 "Applications of the Intel 2104A 4k RAM"
(2104A)
Discusses operation of the device including power distribution and decoupling.
Intel Application Note AP-23 (13 pg.)

4 "MOS Static RAMs"
(2101, 2102, 2111, 2112, 5101)
Presents devices, failure mechanisms, testing methods and results.
Intel RR-9 (7 pg.)

5 "2416 16K CCD Memory"
(2416)
Describes device, failure modes, reliability tests and results.
Intel RR-11 (5 pg.)

6 "Intel Memory Design Handbook"
(1103, 2107A, 2107B, 2416, 3207A, 3222, 3245, 5101, 5235, 5244)
Combines various RAM, ROM, PROM and CCD application notes plus information on support circuits.
Intel $5.00 (265 pg.)

7 "AMS7001 Basic Storage Module High Speed Memories"
(7001)
Discusses AMS7001 storage module operation, backplane wiring, addressing scheme, and power requirements.
Intersil AN-35 (18 pg.)

8 "Using the TM-200 Semiconductor Memory Card"
(7001)
Describes this memory card using the AMS7001 RAM. Includes detailed diagrams.
Intersil AN-36 (22 pg.)

9 "Layout Considerations Using 4K MOS RAMs"
Discusses orientation, packing, drivers, power distribution, trace widths, signal levels, bypass caps, and bus bars.
Intersil AN-37 (4 pg.)

10 "CMOS RAMs"
(IM6508, IM6523, IM6524)
Provides a block diagram and describes the operation and interface requirements for these 256 × 1 and 1024 × 1 CMOS RAMs.
Intersil Application Bulletin M002 (8 pg.)

11 "Considerations for Designing a High Density, Low Power Memory System"
(MK4200)
Describes a 16K × 8 memory array using the MK4200 4K RAM and CMOS logic.
Mostek (3 pg.)

RAMs (cont)

12 "An In-Depth Look at Mostek's High Performance MK4027"
(MK4027)
Describes operation of this 16-pin, 4K RAM.
Mostek (15 pg.)

13 "Why 'Edge-Activated' Static Memories?"
(MK4104, MK4114, MK32000, MK36000)
Describes these devices with static memory cells and dynamic peripheral circuitry. Compares performance to fully static devices.
Mostek (4 pg.)

14 "A Non-Volatile Microprocessor Memory Using 4K N-Channel MOS RAMs"
(MCM6605, MC6800)
Describes the design of a 8192-byte non-volatile memory using the MCM6605 4K × 1 RAM and CMOS control logic to reduce the power requirement in the standby mode.
Motorola AN-732A (17 pg.)

15 "The Design of an N-Channel 16K x 16-Bit Memory System for the PDP-11"
(MCM6605, MC3450, MC3452, MC3459, MC3460)
Briefly describes operation of the MCM6605 NMOS RAM, the details, the design of a PDP-11 add-on mainframe memory using this device. The interface ICs and system performance are also discussed.
Motorola AN-740 (15 pg.)

16 "A CMOS Keyboard Data Entry System for Bus Oriented Memory Systems"
(MC14419)
Describes a keypad to binary data entry system for placing data in RAM memories. It allows data to be entered through keystrokes, encoding 4-bits at a time.
Motorola Application Note AN-759 (4 pg.)

17 "Semiconductor for Plated Wire Memories"
See listing under (Digital) Interface. (Motorola)

18 "A High Speed FIFO Memory Using the MECL MC10143 Register File"
See listing under (Digital) High Speed Logic (Motorola)

19 "A Method of Implementing Stacks with Existing Minicomputer Memory"
Gives detailed description of a controller for a stock of programmable size up to 256 words for a 16-bit minicomputer with less than 16k of memory. Tells how stack size can be increased to 4096 words by adding ten ICs.
National AN-60 (4 pg.)

20 "Using Tri State™ Logic for Rubber Band Memories"
Describes the construction and use of scratch/pad memories to store data at a rapid rate and then release it as required. They serve as buffers between systems operating at different clock rates.
National AN-68 (4 pg.)

21 "A Simple Power Saving Technique for the MM5262 2k RAM"
(MM5265)
Describes method for decoding the clocks of unselected chips in a memory array to save power. Discusses application in 8k × 16 memory.
National AN-86 (4 pg.)

RAMs (cont)

1 **"Designing Memory Systems Using the MM5262"**
(MM4262, MM5262)
Provides a detailed description of this 2048 × 1 PMOS dynamic RAM, operating instructions, and a diagram of a 16K × 10 memory using the device.
National AN-144 (14 pg.)

2 **"Pulsed Power Supply Operation of Selected MM2102 Static RAM"**
(MM2102, SM1480)
Covers method for operating selected 2102s (SM61480s) in a power-down mode.
National AN-172 (3 pg.)

3 **"MOS Scratch Pad/Content Addressable Memory System"**
Describes a 64-bit Scratch Pad/Content Addressable Memory using MOS devices. Includes circuit diagrams and discusses circuit operations.
National MB-11 (2 pg.)

4 **"Memory Systems Built with the Nortec 6002"**
(6002)
Describes circuits for the bit driver/sense amplifier required to interface the 6002 with TTL. Discusses external support circuit parameters and internal circuit operations that affect system performance.
Nortec Applications Note No. 28 (4 pg.)

5 **"Memory Systems Built with the Nortec 6002"**
(6002)
Describes use of this 1024-bit RAM in building a general purpose memory module with 425,984 bit capacity.
Nortec Applications Note No. 30 (14 pg.)

6 **"Printed Circuit Layout Considerations for Dynamic Memory Arrays"**
Gives P.C. layout guidelines for MOS dynamic memories (also applicable to standard TTL circuits.)
Nortec Applications Note No. 31 (2 pg.)

7 **"Designing Memory Systems with the Nortec 6003 RAM"**
(6003)
Describes operation of this 2048-bit RAM, including a discussion of memory timing, refresh control, array control signals, device output sensing, and array driver circuits.
Nortec Applications Note No. 32 (9 pg.)

8 **"Memory Systems Characteristics and Applications for the CD4061A"**
(CD4061A)
Describes basic device operation, application in memory systems, and testing including construction of an all CMOS memory tester.
RCA ICAN-6445

9 **"Driving the TMS4030 RAM Using the SN75363 or SN75322"**
(SN75322, SN7536, TMS4030)
Driving the TMS4030 chip enable clock with these ICs, switching speeds versus system size, general performance characteristics and performance comparisons are provided.
Texas Instruments Application Report CA-181 (7 pg.)

RAMs (cont)

10 **"Memory System Design Utilizing TMS4050/4051 4k Dynamic RAMs"**
(TMS4050, TMS4051)
Reviews speed considerations, then steps through drafting a 4k dynamic RAM system. Two sample circuit examples are outlined.
Texas Instruments Application Report MOSA1 (56 pg.)

11 **"Introduction to Refreshing TI 4k Dynamic RAMs"**
(TMS2102, TMS4051)
Methods of refreshing dynamic RAMs are discussed. Compares static RAMs with dynamic RAMs also.
Texas Instruments Application Report MOSA3 (12 pg.)

ROMs

12 **"Using the EA4600 ROM in M6800 Microcomputer Systems"**
(EA4600)
Takes up use of the ROM for use as memory, an I/O device, or as a data converter in the microcomputer system.
Electronic Arrays M-16 (14 pg.)

13 **"ROM Application Note"**
(EA2708, EA3200, EA4700, EA8308A, EA8316E)
General discussion of ROMs and characteristics of each device.
Electronic Arrays (11 pg.)

14 **"Interfacing of the EA4900 16K ROM in an MCS-4 Microprocessor System"**
(EA4900)
Considers timing, power supplies, and logic levels for interfacing these devices.
Electronic Arrays (8 pg.)

15 **"Monolithic Diode Matrices"**
Describes programming and use of diode matrices. Applications: teletypewriter coding matrix, decimal decode for displays, nines complement-BCD, shift register matrices, and ROMs.
Harris Application Note 206 (16 pg.)

16 **"Intel Memory Design Handbook"**
See listing under (Memory) RAMs (Intel)

17 **"MCS2026-002"**
(MCS2026-002)
Describes connections to use this demonstrator version of the 16K (2048 × 8) dynamic ROM, which can be used as an adder, counter, encoder, decoder or shift register.
MOS Technology Application Note MCS2026-002 (8 pg.)

18 **"Code Conversion with Semiconductor Read Only Memories"**
(MCM4000)
Describes methods for converting data from binary to BCD and vice versa, from the Hollerith to the common 8-bit codes, and from one 8-bit code to another.
Motorola AN-506 (13 pg.)

19 **"Replacing Sequential Logic with ROMs"**
Describes design methods for using ROMs to replace sequential logic, that is to replace designs that would require random or combinational logic with feedback loops.
Motorola AN-722 (19 pg.)

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ROMs (cont)

1 **"The Systems Approach to Character Generators"**
(MM5240, MM5241)
Discusses use of MM5240 and MM5241 ROMs in character generation. Includes discussion of CRT raster scan displays, refresh memory modulation, control logic, bipolar compatibility, printing applications, and raster scan systems.
National AN-40 (12 pg.)

2 **"The Application of ROMs"**
(MM5203, MM5230, MM5232, MM5240)
Describes applications of read only memories in table look up, code conversion and generation, character generation, random logic generation, and microprogamming.
National AN-61 (12 pg.)

3 **"Saving ROMs in High-Resolution Dot-Matrix Displays and Printers"**
(MM5232, MM5240, MM5241, DM8596, MM8597)
Describes two-stage, column-generation approach called "intermediate coding" that save more than 25% of ROM capacity when several ROM's are needed to store a font.
National AN-85 (8 pg.)

4 **"Custom ROM Programming"**
Gives forms for submitting truth tables for various National read only memories.
National AN-100 (8 pg.)

5 **"Trig Function Generators"**
Instead of simply cascading ROM to increase resolution and accuracy of the look-up tables, this note describes interpolation techniques to increase trig function accuracy with less memory.
National MB-10 (2 pg.)

6 **"MOS Goes Bipolar"**
See listing under (Memory) Shift Registers. (National)

7 **"Fast Multipliers Using TTL Read Only Memories"**
(SN74182, SN74H183, SN74283, SN74284, SN74285)
Reviews fundamental algorithm of binary multiplication. Shows use of ROMs for multiplication, two's complement multiplication, and truncated multiplications.
Texas Instruments Application Report CA-172 (11 pg.)

Shift Registers

8 **"A Random Pattern Generator for Testing Digital Delay Elements"**
Describes the use of a linear feedback shift register for digital testing.
Advanced Micro Devices Application Note (3 pg.)

9 **"Applications of Dynamic Shift Registers"**
(1402A, 1403A, 1404A, 1405A, Am2802, Am2803, Am2804, Am2805, Am2806, Am2807, Am2808)
Discusses dynamic shift register storage in general, clock timing, circuits for clock drivers, interfacing with TTL, and recirculating registers.
Advanced Micro Devices Application Note (7 pg.)

Shift Registers (cont)

10 **"Schottky TTL MSI Registers"**
(AM25S07, AM25S08, AM25909, SN54S174, SN54S175, SN54S194, SN54S195, SN74S174, SN74S175, SN74S194, SN74S195)
Describes these 4 and 6-bit registers, their operation and applications. Contains logic diagrams and function tables. Applications covered include: longer words, use with dynamic shift registers, selective bus storage, use as a LIFO memory, psuedo random feedback, unique counting codes, permutation of inputs, and use in arithmetic.
Advanced Micro Devices Application Note (16 pg.)

11 **"High-Speed Shift Registers Use TTL RAMs and Counters to do all the Shifting"**
Describes how to build a high speed shift register using a RAM accessed by counters.
Advanced Micro Devices (2 pg.)

12 **"9338 8-Bit Multiple Port Register"**
(9338)
Describes the features of this device, the TTL/MSI equivalent and parallel serial expansion capabilities. Covers use as three address arithmetic unit with eight registers, and use in a first-in first-out memory.
Fairchild Application Note 294 (6 pg.)

13 **"The MC7491A 8-Bit Serial Shift Register and the MC7495 4-Bit Shift Register"**
(MC5491A, MC5495, MC7491A, MC7495)
Describes operation of these devices and discusses application as shift counters, delay lines, buffers, serial-parallel converters, parallel-serial converters, ring counters, and parallel arithmetic units. Also describes use in a teletypewriter-computer interface system.
Motorola AN-530A (9 pg.)

14 **"The Logic Design of Shift Counters"**
See listing under (Digital) Counters. (Motorola)

15 **"Using Shift Registers as Pulse Delay Networks"**
See listing under (Digital) High Speed Logic (Motorola)
Microprocessors

MICROPROCESSORS

Applications

1 **"Application Techniques for the MCS-48 Family"**
(8748, 8048, 8355, 8243, 8755, 8155)
Introduces the MCS-48 family and describes the implementation of such subsystems as: analog input and output, the use of tables for function evaluation, receiving and transmitting serial code, and parity generation.
Intel Application Note AP-24 $1.00 (23 pg.)

2 **"Using Mosteks F8 Microprocessor in a Scanned Seven-Segment Display Application"**
(F8)
Discusses the advantages of the F8 as a numeric display interface in μP based devices.
Mostek (16 pg.)

3 **"Using Mosteks F8 in a Scanned Keyboard Application"**
(F8)
Discusses application of the F8 to eliminate hardware outside the processor to encode the keyboard. Uses a keyboard scanning technique.
Mostek (16 pg.)

4 **"A Floppy Disk Controller Using the MC6852 SSDA and Other M6800 Family Parts"**
(MC6852, M6820)
Discusses a floppy disk controller built using a synchronous serial data adapter as the primary data interface with the MPU. All non-data operation (seek, drive selection, etc.) in the controller are handled by a peripheral interface adapter.
Motorola AN-764 (17 pg.)

5 **"Data Acquisition Networks with NMOS and CMOS"**
(MC14433, MC6800)
Discusses an 8-channel data acquisition network using the MC14433 A/D converter and the MC6800 microprocessor.
Motorola AN-770 (11 pg.)

6 **'A CRT Terminal Using the M6800 Family"**
(MC6800)
Describes a CRT controller for "glass-teletype," smart, programmable, and intelligent CRT terminals. The display format is 24 rows of 80 characters using a Motorola M3000 Video Monitor.
Motorola AN-771 (13 pg.)

7 **"MOS Delay Lines"**
(MM506)
Describes the characteristics of static and dynamic shift registers used in delay line. Discusses application as series/parallel delay lines and as substitutes for magnetic drum memories. Also covers specialized clocking techniques, such as two-speed clocking.
National AN-25 (8 pg.)

8 **"High Voltage Shift Registers Move Displays"**
(MM5081)
Describes use of the MM5081 high voltage shift register for driving gas discharge or lamp displays, i.e. moving messages or moving graphics.
National AN-44 (14 pg.)

9 **"Low Frequency Operation with Dynamic Shift Registers"**
Discusses operation of two forms of dynamic shift registers: ratioless and ratio. Recommends techniques, such as keeping clock amplitudes high, to design added margin into systems. Discusses temperature considerations, packaging.
National AN-55 (4 pg.)

Applications (cont)

10 **"Design Considerations of MOS Dynamic Shift Registers with Tri-State Outputs"**
(MM4012, MM4013, MM5012, MM5013)
Describes operation of MOS shift registers with Tri-State push-pull outputs. Includes discussion of the dynamic characteristics and maximum clock frequency.
National AN-65 (4 pg.)

11 **"MOS Goes Bipolar"**
Shows what voltages are required to combine MOS Shift Registers and Read Only Memories with bipolar devices. Presents interface diagrams.
National MB-12 (2 pg.)

12 **"Mask Programming Specializes MOS Shift Register Designs"**
(MM4007, MM4019, MM5007, MM5019)
Describes customizing MOS shift register bit lengths by programming a metalization mask used to manufacture these devices. Dual registers from 20 to 256 bits, and single registers from 40 to 512 bits are available. Describes single register taped output options.
National MB-14 (2 pg.)

13 **"Static Shift Register Operating Curves"**
How to use the minimum/maximum clock pulse width operating curves included in National's static shift register data sheets.
National MB-15 (2 pg.)

14 **"Double-Clocking Cuts Standard Registers to Non-Standard Sizes"**
Describes a method of double-clocking for N data input periods to make the register appear shortened by N bits. When this is achieved, the clock rate resumes normal frequency.
National MB-16 (2 pg.)

15 **"COS/MOS MSI Counter and Register Design and Applications"**
See listing under (Digital) CMOS (RCA)

16 **"HiNIL 375 Universal Shift Register"**
See listing under (Digital) HNIL/HTL (Teledyne Semiconductor)

17 **"M6800 Microprocessor Application Manual"**
(M6800)
Describes the use of the 6800 family of parts. Gives details of practical applications including the development of hardware and software, design of a point of sale terminal and interfaces to peripherals.
Motorola $25.00 (716 pg.)

18 **"Multiple Microprocessors in Instrument Systems"**
(IMP-8, IMP-16)
Discusses systems built with central microcomputers plus peripheral microprocessors to distribute intelligence. Illustrates concepts with a data acquisition and setpoint control system.
National AN-106 (8 pg.)

19 **"The IMP-8C as a Data Concentrator"**
(IMP-8C)
Describes the use of this microprocessor in data concentrator applications. Covers use with a full duplex modem, and the terminal controller interface.
National AN-113 (6 pg.)

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Applications (cont)

1 **"Data Handling with the IMP-8"**
(IMP-8, IMP-16)
Covers basic concepts for transferring data from a memory to peripherals.
National AN-117 (4 pg.)

2 **"Microprocessor Mates with MOS/LSI Keyboard Encoder"**
(IMP-16)
Shows how to interface a keyboard to the IMP-16 microprocessor for text editing.
National AN-128 (6 pg.)

3 **"For Data Communications Systems: A Front-End Preprocessor for 16-Bit Minicomputer Hosts"**
General discussion of how preprocessing techniques used in large-scale host computers can be scaled down for application in mini-based systems.
National AN-131 (4 pg.)

4 **"The IMP-16 in Communication Applications**
(IMP-16)
Discusses communication processor functions, requirements for communications microprocessors and system considerations. Gives programming examples including status monitoring, data transmission, message routing, interrupt handling and error control.
National AN-134 (6 pg.)

5 **"Communication Interfaces for the IMP-16"**
(IMP-16)
Describes the use of this microprocessor in leased line and switched line applications with the communications conforming to EIA standard RS232-C.
National AN-152 (13 pg.)

6 **"A Data Concentrator Using PACE"**
(PACE)
Describes the use of this microprocessor to take data from several slow speed lines and transmit it over one line.
National AN-164 (5 pg.)

7 **"Microprocessor Security Systems Made Easy"**
(SC/MP)
Describes program for sequencing through multiple inputs and actuating a simple output (relay, alarm, etc.) using NIBL.
National AN-174 (2 pg.)

8 **"Using Standard National Calculators in Industrial and Microprocessor Applications"**
Describes how to add low cost, low speed arithmetic capability using calculator components and standard logic.
National AN-176 (4 pg.)

9 **"SC/MP as an Analog-to-Digital Converter"**
(SC/MP)
Equations and diagrams for using the SC/MP as an A/D and D/A converter. Also lists sources of error that may result.
National AN-191 (3 pg.)

10 **"PACE Logic Designers Guide to Programmed Equivalents to TTL Functions"**
(PACE)
Shows how standard TTL/MSI logic functions and subsystems are implemented in software for the PACE microprocessor.
National $5.00 (131 pg.)

Applications (cont)

11 **"SC/MP Microprocessor Applications Handbook"**
(SC/MP)
Describes the SC/MP as a general purpose microprocessor covering applications, addressing, instruction set, implementing systems, buffering and interface. Covers use with A/D converters, keyboards, display systems, recorders and printers.
National $5.00 (160 pg.)

12 **"8X300 Computer to I/O Bus Emulator"**
(8X300)
Explains how the 8X300 system emulates a Microdata 1600 I/O bus. Shows how Microdata I/O bus compatible peripherals may be connected to and controlled by a standard 8X300 system.
Signetics (2 pg.)

13 **"8X300 CRT Controller"**
(8X300)
Describes how a CRT controller can be realized using the 8X300 Microcontroller.
Signetics (24 pg.)

14 **"8X300 Data Concentrator"**
(8X300)
Explains how the 8X300 can be used to multiplex low speed terminals.
Signetics (2 pg.)

15 **"8X300 Teletype Multiplexer"**
(8X300)
Explains how to easily interface an 8X300 to a teletype or similar asynchronous device. Also shows how an 8X300 can be used as a front end multiplexer for a large computer system.
Signetics (2 pg.)

16 **"Application Note for CRT5027"**
(CRT5027, CG5004L)
Discusses the configuration of a bus oriented, microprocessor based, CRT display system. Includes diagrams and flow chart.
Standard Microsystems (5 pg.)

17 **"TMS9900 Floppy Disk Controller"**
(TMS9900)
Illustrates use of the TMS9900 microprocessor system as floppy disk drive controller that interfaces to a RS-232C type terminal. Includes descriptions of hardware, diskette data transfer, and software.
Texas Instruments Application Report MOSA5 (68 pg.)

18 **"TMS9900 CRT Controller"**
(TMS9900)
Analyzes a CRT controller system that employs a TMS9900 microprocessor. Contains diagrams of the system and a software monitor routine.
Texas Instruments Application Report MOSA6 (32 pg.)

General

19 **"Distributed Data Processing"**
See listing under (Digital) Data Transmission (Burr-Brown)

20 **"A Non-Volatile Microprocessor Memory Using 4K N-Channel MOS RAMs"**
See listing under (Memory) RAMS (Motorola)

General (cont)

1 **"Microprocessors — An Introduction"**
Shows system components, defines terms and describes operation of an elementary computer system.
National AN-114 (4 pg.)

2 **"Increasing Throughput for IMP-16 Serial Input/Output"**
(MM5303)
Describes use of device to improve communication between microprocessor and peripheral with little increase in component count.
National AN-160 (7 pg.)

3 **"SC/MP Mates with Cassette Recorder"**
(SC/MP)
Describes a method of storing digital information on cassette tape.
National AN-166 (12 pg.)

4 **"Timesharing Users Manual"**
(IMP-8, IMP-16)
Gives user information to assemble IMP-8 or IMP-16 programs using Tymshare, Inc. services, or IMP-16 programs using the General Electric Computer Timesharing facility.
National (35 pg.)

5 **"Microprocessors — Why They Evolved and What They Are"**
Offers background material and describes common microprocessor terms.
National IB-1 (2 pg.)

Programming

6 **"Microprogramming Handbook"**
(2911, 2909, 29811, 2922, 29803)
Discusses microprogramming a bipolar processor. Includes sections on microprogram memory, sequencing, branching, jumping, and subroutines.
Advanced Micro Devices, $5.00 (44 pg.)

7 **"HM-6100 Microprocessor Basic 4K Software"**
(HMS6100)
Describes the Digital Equipment Corp. PDP-8 software.
Harris Application Note HM003 (4 pg.)

8 **"HM-6100 ROM Based Subroutine Calls"**
(HM6100)
Describes two methods for returning to the proper program location after executing a subroutine.
Harris Application Note HM008 (4 pg.)

9 **"Series 3000 Cross Microprogramming System CROMIS Reference Specification"**
(3000)
Describes the CROMIS microprogramming system for the 3000 series computing elements. It supports the user who wants to generate microcode.
Intel $5.00 (77 pg.)

10 **"8080/8085 Assembly Language Programming Manual"**
(8080A, 8085)
Primarily a reference manual, this manual describes the 8080/8085 instruction set, assembly language concepts, assembler directives, macros, programming techniques and interrupts.
Intel $5.00 (210 pg.)

Programming (cont)

11 **"PL/M-80 Programming Manual"**
(8080, PL/M-80)
Provides in readable format a complete description of the PL/M language as implemented by the PL/M-80 compiler.
Intel $5.00 (134 pg.)

12 **"MCS-48 and UPI-41 Assembly Language Manual"**
(8041, 8048, 8741, 8748, MCS-48, UPI-41)
Describes the assembly language for programming the MCS-48 and UPI-41 single device microcomputers. Covers procedures and controls for operating the assemblers to translate the source file into object code.
Intel $5.00 (192 pg.)

13 **"Series 3000 Microprogramming Manual"**
(3000)
Fundamentals of the 3000 series microprocessor and Cross Microprogramming System are described. Presents XMAS, XMAP languages and microprogramming techniques.
Intel $5.00 (73 pg.)

14 **"IM6100 CMOS Microprocessor Basic 4K Software"**
(IM6100)
Describes use of the Digital Equipment Corp. PDP-8 software.
Intersil Application Bulletin M003 (7 pg.)

15 **"ROM Based Subroutine Calls with the IM6100"**
(IMS6100)
Describes two methods for returning to the proper program location after executing a subroutine.
Intersil Application Bulletin M008 (6 pg.)

16 **"6500 Programming Manual"**
(MCS6500 Series)
Describes the software aspects of the 6500 microprocessor family and related support devices.
MOS Technology $6.95

17 **"F8 Programmer's Guide"**
(F8)
Describes how to write uprograms for the F8 microprocessor system which cause the system to function as a discrete logic element.
Mostek $5.95 (304 pg.)

18 **"M6800 Evaluation Module Users Guide"**
(M6800)
Provides general information, installation instructions, preparation and operating procedures for the M6800 evaluation module.
Motorola $5.00 (150 pg.)

19 **"M6800 Microprocessor Programming Manual"**
(M6800)
Provides information needed to program the unit, discusses the instruction set, source language, assembler, simulator, Build-Virtual-Machine and HELP programs. Gives program examples.
Motorola $10.00 (303 pg.)

20 **"IMP-16 Programming Techniques"**
(IMP-16)
Discusses several aspects of the instruction set to enable programmer to code more efficiently. Includes discussion of subroutines, subroute parameter passing, recursive subroutines, as well as sample programs.
National AN-111 (6 pg.)

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MICROPROCESSORS

Programming (cont)

1 **"A Microprogram Development System"**
(IMP-16)
Describes the application of microprogramming to LSI processors and the advantages of a microprogram development system for hardware and software.
National AN-123 (6 pg.)

2 **"IMP-8 Assembler Manual"**
(IMP-8)
Presents preliminary information on the use of IMP-8 assembler language.
National (60 pg.)

3 **"IMP-8 Programming Manual"**
(IMP-8)
Provides information for the programming of the IMP-8 family of microprocessors and microcomputers.
National (111 pg.)

4 **"IMP-8 Utilities Reference Manual"**
(IMP-8)
Provides information on the IMP-8 debugging program, loader programs, the standard teletype and I/O package, and the paper tape-punch package.
National (57 pg.)

5 **"IMP-16 Assembler Program Description Manual"**
(IMP-16)
Describes the internal structure of the IMP-16 Assembler. It covers the general organization, functions required for conversion to operate on a different machine, and a detailed subroutine and data description.
National (105 pg.)

6 **"IMP-16 Microsymbolic Assembler"**
(IMP-16)
The microsymbolic assembler is a collection of routines that make it possible to write microprograms for the IMP-16 in symbolic language. This manual describes the statements, character set and basic program elements.
National (21 pg.)

7 **"Installation of IMP-16 Assembler on System 360/370 Operator Manual"**
(IMP-16)
Provides information for installing the IMP-16 assembler and punch programs on an IBM 360-370 computer.
National (18 pg.)

8 **"PACE Assembly Language Programming Manual"**
(PACE)
Discusses writing assembly language or machine language programs. Coding conventions, I/O formats, and macros are also covered.
National $5.00 IPC-16S/969Y (110 pg.)

9 **"SC/MP Microprocessor Assembly Language Programming Manual"**
(SC/MP)
Covers an overview, Assembly Language, statements, programming techniques, macros and I/O formats.
National $5.00 (108 pg.)

10 **"Timesharing Manual for the RCA CDP1802 COSMAC Microprocessor"**
(CDP1802)
Discusses two assembly languages in the COSMAC software development package. Examines using the package, tells how to use it and develops a sample program.
RCA MPM-202 $10.00 (58 pg.)

Programming (cont)

11 **"Serial Input/Output"**
(2650)
Covers use of the Sense/Flag capability for serial input/output.
Signetics AS50 (3 pg.)

12 **"Bit and Byte Testing Procedures"**
(2650)
Describes several methods of testing the contents of the internal registers.
Signetics AS51 (4 pg.)

13 **"General Delay Routines"**
(2650)
Covers software routines to generate time delays.
Signetics AS52 (3 pg.)

14 **"Binary Arithmetic Routines"**
(2650)
Covers routines for binary addition, subtraction, multiplication and division.
Signetics AS53 (15 pg.)

15 **"Conversion Routines"**
(2650)
Covers Binary to BCD, BCD to ASCII, Hexadecimal to ASCII and vice versa.
Signetics AS54 (17 pg.)

16 **"2650 Initialization"**
(2650)
Covers start up procedures.
Signetics MP51 (1 pg.)

17 **"2650 Evaluation Printed Circuit Board"**
(2650)
Covers features and connections for this card level evaluation and design tool.
Signetics SP50 (14 pg.)

18 **"2650 Demo System"**
(2650)
Complete demonstration system when used with the 2650 PC1001.
Signetics SP51 (7 pg.)

19 **"Support Software for Use with the NCSS Timesharing System"**
(2650)
Covers a cross-assembler, cross-simulator and two utility programs (to load the 2650 and to burn PROMs.)
Signetics SP52 (7 pg.)

20 **"Simulator, Version 1.2"**
(2650)
Changes to the simulator.
Signetics SP53 (1 pg.)

21 **"Pipbug"**
(2650)
Program for the 2650 PC1001 demonstration card.
Signetics SS50 (13 pg.)

22 **"Absolute Object Format"**
(2650)
Describes the format of the absolute code.
Signetics SS51 (1 pg.)

Programming (cont)

1 **"Signetics Micro Assembler Reference Manual"**
(N2901, N3002, 8X02)
Describes this FORTRAN program developed as a design tool for writing microprograms. This microprogram defines his own assembly language, writes the microprogram, then assembles it to generate tapes to load memory. Suitable for most microprogrammed applications.
Signetics $4.00 (74 pg.)

Systems

2 **"AM2914 Priority Interrupt Encoder"**
(2913, 2914, 2900, 9080A)
Provides data sheet information on devices. Outlines construction of a microprogrammable, bipolar, LSI interrupt structure for the 2900 and 9080A processors using the 2914.
Advanced Micro Devices (33 pages)

3 **"The 8080A/9080A MOS Microprocessor Handbook"**
(8080A, 9080A, 8212, 8255, 9555, 8251, 9551)
Provides descriptions of the 9080A CPU and the associated clock generator and system controllers. Supplies data sheet information on various I/O interfaces, support circuits, and memories. An application section covers clock generation, memory system design, timing, interrupts, and multiplication.
Advanced Micro Devices, $7.95 (280 pg.)

4 **"A Microprogrammed 16-Bit Computer"**
(2901, 2902, 2914, 2913, 29705)
Presents computer design starting with the specification of a computer from a functional standpoint. Describes architectural units including the ALU, the Program Control Unit, and memory.
Advanced Micro Devices $5.00 (47 pg.)

5 **"S6800 Microprocessor Hardware Book"**
(S6800)
Provides System description and data sheets.
American Microsystems (72 pg.)

6 **"S6800 Hardware Reference Manual"**
(S6800)
Detailed descriptions of the system operation.
American Microsystems $15.00 (225 pg.)

7 **"F8 Microprocessor Application Manual"**
(F8)
Covers details concerning bit manipulation, RAM expansion of the I/O ports, subroutines and boot strap loaders.
Fairchild

8 **"Static Memory Systems Utilizing the HM-6100"**
(HM6100)
Describes CMOS, nonvolatile CMOS and NMOS memory systems.
Harris Application Note HM004 (7 pg.)

9 **"HM-6100 CMOS Microprocessor Teletype Interface"**
(HD6402, HM6100)
Describes a teletype interface using the HM6100 and a UART.
Harris Application Note HM005 (7 pg.)

10 **"HM-6100 Operator Console"**
(HM6100)
Describes the 6900-CONTRL console for the prototyping system.
Harris Application Note HM006 (4 pg.)

Systems (cont)

11 **"HM-6100 CMOS Microprocessor Memory Extension"**
(HM6100)
Discusses a memory extension controller to increase the memory from 4096 to 32,768 words.
Harris Application Note HM007 (4 pg.)

12 **"8255 Programmable Peripheral Interface Applications"**
(8255)
Provides hardware and software information for this byte oriented I/O device. Examples cover character printer, paper tape and 8080-8080 interface applications.
Intel Application Note AP-15 $1.00 (32 pg.)

13 **"Memory-Mapped I/O and Vectored Interrupts for Intel 4-Bit Microcomputer Systems"**
(4009, 4289)
Describes the expansion to 16 or 256 4-bit input ports, to 64 8-bit input ports, to vectored interupts, to vectored inputs and to 128 output ports.
Intel Application Note AP-19 (6 pg.)

14 **"Intel MULTIBUS Interfacing"**
(Multibus, 8080)
Describes this system bus structure, signals and characteristics. Includes electrical and mechanical information needed to build slave modules.
Intel AP-28 $1.00 421 pg.)

15 **"Simplify Your Dynamic RAM/Microprocessor Interface"**
(2104A, 2107A, 2107B, 2116)
Compares static and dynamic RAMs, then outlines elements of dynamic RAM/μP interface design including: refresh techniques, address multiplexing, memory overlap and transmission line effects.
Intel Application Note APR-1 $1.00 (65 pg.)

16 **"8080/8080A Microcomputer"**
(8080/8080A)
Presents device, failure mechanisms, testing methods and results.
Intel RR-10 (13 pg.)

17 **"8080 Microcomputer Systems User's Manual"**
(8080A)
Data sheets, architecture, timing requirements, and instruction sets for the MSC80 family.
Intel $5.00 (238 pg.)

18 **"MCS-48 Microcomputer User's Manual"**
(8048, 8748, 8035, 8155, 8243, 8355, 8755, MCS-48)
Describes the system architecture, instruction set, programming, expansion, hardware and software examples, extensive data sheets.
Intel $5.00 (305 pg.)

19 **"CPI-41 User's Manual"**
(8041, 8741, 8243, UPI-41)
Describes this Universal Peripheral Interface device operation, instruction set, system design and interfacing.
Intel $5.00 (115 pg.)

20 **"MCS-85 User's Manual"**
(8085, MCS-85)
Describes this 8085 based system and peripheral components. Extensive coverage through data sheets.
Intel $5.00 (273 pg.)

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MICROPROCESSORS

Systems (cont)

1 **"Using the 8251 Universal Synchronous/Asynchronous Receiver/Transmitter"**
See listing under (Digital) Data Transmission (Intel)

2 **"Static Memory Systems for the IM6100"**
(IM6100)
Describes CMOS, nonvolatile CMOS and NMOS memory systems for the IM6100.
Intersil Application Bulletin M004 (14 pg.)

3 **"Teletype Interface for the IM6100 CMOS Microprocessor"**
(IM6100)
Describes a teletype interface using the IM6100 and a UART.
Intersil Application Bulletin M005 (10 pg.)

4 **"IM6100 Operator Console"**
(IM6100)
Describes the 6900-CONTRL console for the prototyping system.
Intersil Application Bulletin M006 (17 pg.)

5 **"IM6100 CMOS Microprocessor Memory Extension"**
(IM6100)
Discusses a memory extension controller to increase the memory from 4096 to 32,768 words.
Intersil Application Bulletin M007 (6 pg.)

6 **"A Powerful Microprogram Controller: The 67110"**
(65110)
Describes features of the device including organization, internal interrupts, and memory expansion.
Monolithic Memories (5 pg.)

7 **"5701/6701: 4-Bit Expandable Bipolar Microcontroller"**
(5701, 6701)
Provides functional descriptions of the device, instruction set, timing and more.
Monolithic Memories Application Note (23 pg.)

8 **"6500 Hardware Manual"**
(MCS6500 series)
Describes the hardware aspects of the 6500 microprocessor family and related support devices.
MOS Technology $6.95

9 **"TIM Manual"**
(MCS6530)
Describes the program contained in the ROM portion of the 6530-004.
MOS Technology $5.00

10 **"F8 Microprocessor Hardware Support-Evaluation Kit"**
(F8)
Describes this kit and its use. Includes a sample program to acquaint the user with F8 machine language and to program the kit.
Mostek (20 pg.)

11 **"Expanding Mostek's F8 Microprocessor External Interrupt Capability"**
(F8)
A detailed discussion of servicing control inputs in a F8 based system with emphasis on implementing interrupt driven systems.
Mostek (12 pg.)

Systems (cont)

12 **"Subroutine Neting and Multiple Interrupt Handling Using Mostek's F8 Microprocessor"**
(F8)
Discusses the use and implementation of subroutines and interrupts as they apply to programming an F8 based system.
Mostek (16 pg.)

13 **"Z80 Interfacing Techniques for Dynamic RAM"**
(Z80, MK4027, MK4116)
Provides specific examples of interfacing 16-pin dynamic memories to the Z80 microprocessor. Includes timing diagrams and refresh information.
Mostek

14 **"Analog-to-Digital Conversion Techniques with the M6800 Microprocessor System"**
(MC1405, MC6800)
Describes successive approximation and dual ramp techniques for A/D conversion using the M6800. Gives flow diagrams, source programs and schematics. Appendix gives program for binary to BCD conversion.
Motorola AN-757 (35 pg.)

15 **"A Simple High Speed Bipolar Microprocessor Illustrates System Design and Microprogram Techniques"**
(MC10801, MC10803)
Describes a complete bipolar LSI systems design using 10 ICs to perform 2's complement add, subtract, multiply and divide.
Motorola AN-744 (12 pg.)

16 **"MEK6800D2 Microcomputer Kit System Expansion Techniques"**
(MC6800)
Covers techniques to add 8K or 16K of memory, I/O port expansion, power-up auto-reset, switch selectable monitor operation, and RS-232 or current-loop data terminal operation.
Motorola AN-771 (23 pg.)

17 **"M6800 Systems Utilizing the MC6875 Clock Generator/Driver"**
(MC6875)
Gives extensive design examples using the MC6875 in systems including slow or dynamic memories, and DMA (multiprocessor) applications.
Motorola AN-775 (20 pg.)

18 **"M6800 System Microcomputer System Design Data"**
(M6800)
Describes the family of parts including data sheets.
Motorola (165 pg.)

19 **"Device Operation and System Implementation of the Asynchronous Communications Interface Adapter (MC6850)"**
See listing under (Digital) Data Transmission (Motorola)

20 **"Applications of LSI Processors"**
(IMP-16)
Describes system architecture and operation of IMP-16C, 16-bit parallel processor with self-contained memory. Describes applications in a data communication link analyzer, in point-of-sales and in retailing systems.
National AN-98 (8 pg.)

Systems (cont)

1 "Increasing the Number of Control Flags and Jump Conditions in the IMP-16C"
(IMP-16C)
Describes simple and economical method of increasing the number of testable jump conditions and the number of control flags on the IMP-16C microprocessor.
National AN-101 (4 pg.)

2 "Clock-Hold Schemes for the IMP Microprocessor Family"
(IMP-8C, IMP-16C)
Presents scheme to extend the clock-hold function for additional periods of the main system clock, using the DM8570 shift register.
National AN-105 (4 pg.)

3 "IMP-16 Interrupts"
(IMP-16)
Describes various type of interrupts, including an overview of interrupt structure, example of interrupt request and service, multi-level and control panel interrupts.
National AN-107 (23 pg.)

4 "IMP-16C Peripheral Interfacing Simplified"
(IMP-16C)
Explores techniques for interfacing peripheral devices to the microprocessor.
National AN-124 (4 pg.)

5 "IMP-16L DMA — What It Is and How to Use It"
(IMP-16)
Discusses general theory of the DMA Bus, gives examples of priority expansion and data transfer.
National AN-135 (6 pg.)

6 "Designing with the IMP Chip Set"
(IMP-16)
Describes some of the major considerations in the implementation of 4 to 32 bit systems using the IMP series of devices. A 16 bit system is covered in detail.
National AN-141 (10 pg.)

7 "Using a Microprocessor Beyond Apparent Speed"
(IMP-16)
Covers the concept of cycle stealing, a technique in which a peripheral device communicates directly with memory or another peripheral device while the CPU is doing work other than using the data and address buses.
National AN-142 (6 pg.)

8 "Number Cruncher (MM57109) Interface to Microprocessor"
(MM57109)
Describes the MM57109 number cruncher unit which can perform most arithmetic functions found in complex hand-held calculators and interfaces either to a microprocessor or a random logic system. Provides schematics of interface logic and a flow chart for initialization of the device.
National AN-186 (10 pg.)

9 "Clock Considerations For SC/MP-II"
(SC/MP)
Shows several methods of providing a clock for the SC/MP-II.
National AN-188 (4 pg.)

Systems (cont)

10 "Serial Data Transfers with SC/MP-II"
(SC/MP)
Discusses serial data I/O data transfer using the SC/MP-II extension register.
National AN-190 (3 pg.)

11 "Increasing the Number of JUMP Conditions and Control Flags in the IMP-4C"
(IMP-4)
Presents a method of providing eight control flags with the use of the RALU flag, and seven extra testable conditions.
National IB-2 (2 pg.)

12 "GCP/P Product Description"
(GCP/P)
Delineates the system, gives a functional description of the CROM and RALU devices, and presents the general purpose macroinstruction set. Appendices cover a microprogram to implement the IMP-16 instructions set and the use of the RALU status flag.
National (61 pg.)

13 "IMP-4 Technical Description"
(IMP-4)
Describes the general purpose instruction set, gives functional and system descriptions, describes the development system and shows specific programming examples.
National (77 pg.)

14 "IMP-8C Application Manual"
(IMP-8)
Describes the IMP-8C's operational features, functional and logic operation, and input/output interfacing in sufficient detail to permit the user to adapt the card to various applications.
National (119 pg.)

15 "IMP-8C/200 Microprocessor, IMP-8P Microcomputer Product Description"
(IMP-8)
Describes the IMP-8C microprocessor card and the IMP-8P prototyping tool (microcomputer) as systems.
National (10 pg.)

16 "IMP-16-L Product Description"
Describes the features of the IMP-16L general microcomputer system.
National (8 pg.)

17 "POWR I/O CROM Technical Description"
(IMP-16)
Describes the instruction repertoire and use of this unit which expands the variety of memory and input-output operations of the IMP-16.
National (22 pg.)

18 "PACE Technical Description"
(PACE)
Defines and explains how to use the hardware and software that support the PACE system.
National (96 pg.)

19 "PACE Microprocessor System Design Manual"
(PACE)
Introduces the PACE system and basic design requirements. Details memory interfacing and peripheral interface techniques.
National $5.00 1PAC-16A/928 (79 pg.)

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Systems (cont)

1 **"N8080 System Design Manual"**
(INS8080A, DP8212, DP8216, DP8224, DP8226, DP8228, DP8238, INS8251, INS8255)
Describes the INS8080A μP including architecture, timing, data and instruction representation, and I/O operation and control. Also covers use of various support chips.
National $5.00 INS-8A/900 (72 pg.)

2 **"SC/MP Technical Description"**
(SC/MP)
Describes the SC/MP system plus its hardware and systems.
National (64 pg.)

3 **"Data Acquisition System Interface to Computers"**
See listing under (Linear) Converters (National)

4 **"A PROM Programmer for the SC/MP LCDS"**
See listing under (Memory) PROMs (National)

5 **"μPD371 Magnetic Tape Cassette/Cartridge Controller Users Manual"**
(μPD371)
Gives description, timing and circuit diagrams. Assembly language listing for use with NEC's 8080A.
NEC Microcomputers $10.00 (58 pg.)

6 **"μPD372 Floppy Disk Controller Users Manual"**
(μPD372)
Provides text, timing diagrams and schematics plus software listings.
NEC Microcomputers $10.00 (70 pg.)

7 **"μPD372 Mini-Floppy Disk Controller Users Manual"**
(μPD372)
Supplements the Floppy Disk Manual for Mini-Floppy applications.
NEC Microcomputers $10.00 (44 pg.)

8 **"MN1400 Series 4-Bit One-Chip Microcomputers User's Manual"**
(MN1400, MN1402, MN1498, MN1499)
Introduces the MN1400 family. Encompasses system architecture, timing, and the instruction set including examples of various commands and routines.
Panasonic (65 pg.)

9 **"Programmable Interval Timer and Counter for Use with RCA COSMAC Development Systems"**
(CDP1800)
Gives the circuits and logic diagrams for a programmable interval timer and counter for use with the COSMAC development systems. Discusses the commands used for its operation and gives four sample programs.
RCA ICAN-6482

10 **"Interrupt Priority Resolution Circuit for Use with RCA COSMAC Development Systems"**
(CDP1800)
Circuit and program for use when resolution in software is not sufficiently efficient.
RCA ICAN-6485 (3 pg.)

11 **"Adding Two-Level I/O Interface Capability to RCA COSMAC Development Systems"**
(CDP1800)
Circuit to expand I/O capability.
RCA ICAN-6486 (2 pg.)

Systems (cont)

12 **"Alphanumeric Display for Use with RCA COSMAC Development Systems"**
(CDP1800)
Circuit and program for self-scanning dot-matrix display.
RCA ICAN-6488 (3 pg.)

13 **"Analog-to-Digital Converter for Use with RCA COSMAC Development Systems"**
(CDP1800)
Circuit and program to use the Burr-Brown ADC55 12-bit converter.
RCA ICAN-6490 (2 pg.)

14 **"PROM Programmer for RCA COSMAC Development Systems"**
(CPD1800)
Circuit and program to program, copy, verify and list contents of 1702, 2704 and 2708 PROM's.
RCA ICAN-6491 (8 pg.)

15 **"Hexadecimal Keyboard Interface for Use with RCA COSMAC Development Systems"**
(CPD1800)
Circuit and program including debounce routine for 16 key keyboard.
RCA ICAN-6516 (2 pg.)

16 **"Guide to Better Handling and Operations of CMOS Interated Circuits"**
Recommends specific handling and operating practices to minimize the probability of damage in manufacturing and field environments.
RCA ICAN-6525 (5 pg.)

17 **"Register-Based Output Functions for RCA COSMAC Microprocessors"**
(CDP1802, CDP1852)
Describes circuits using the CDP1852 I/O port for outputting information from any of the 16 general purpose scratch pad registers of the CDP1802 microprocessor.
RCA ICAN-6562

18 **"Design of Clock Generators for Use with RCA COSMAC Microprocessor"**
(CDP1802)
Describes a crystal controlled clock generator using-on-chip circuits and crystal and RC generators using external circuits.
RCA ICAN-6565

19 **"Power-On Reset/Run Circuits for the RCA CDP1802 COSMAC Microprocessor"**
Provides diagrams and discussions of several circuits which enable a power-on reset/run capability for the device.
RCA ICAN-6581 (2 pg.)

20 **"User Manual for the CDP1802 COSMAC Microprocessor"**
(CDP1802)
Describes the device architecture and its instruction set with examples of each command. Reviews basic programming techniques and supplies timing diagrams.
RCA MPM-201A $5.00 (115 pg.)

21 **"Microprocessor Prototyping Card"**
(2650)
Describes features of the 2650PC1001 microcomputer.
Signetics Application Memo (2 pg.)

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Systems (cont)

1 **"A Guide to the Selection of Support Components for the Series 3000 Microprocessor"**
(N3001, N3002)
Categorizes the various components used to implement major sections of a typical microprocessor system.
Signetics AM-1 (4 pg.)

2 **A User's Guide to the Series 3000 Microprocessor Chip Set"**
(N3001, N3002)
Describes devices, instruction sets. Design examples included.
Signetics AM-2 (14 pg.)

3 **"Address and Data Bus Interfacing Techniques"**
(2650)
Discusses address and data bus drive requirements. Covers methods for increasing the system drive capability.
Signetics MP53 (8 pg.)

4 **"How to Design with the Control Store Sequencer, 8X02"**
(8X02)
Presents a functional description and gives microprogramming system suggestions.
Signetics Bipolar Application Memo 3 (6 pg.)

5 **"8X300 Input/Output Design"**
(8X300)
Describes typical interfacing techniques to the 8X300 using 8T32/33 or 8T35/36 bidirectional I/O ports.
Signetics (2 pg.)

6 **"8X300 Floppy Disk Interface"**
(8X300)
Describes the 8X300 control of a floppy disk drive with a minimum amount of additional circuitry.
Signetics (2 pg.)

7 **"8X300 Remote Alphanumeric Terminal Controller"**
(8X300)
Describes how an 8X300 interfaces to a simple keyboard/display device with a minimal amount of interface circuitry.
Signetics (2 pg.)

Systems (cont)

8 **"8X300 Interface to External Read/Write Memory"**
(8X300)
Explains how to connect the 8X300 Interface Vector (IV) bytes to the address, data and control lines of an external memory.
Signetics (3 pg.)

9 **"8X300 256 Way Branch"**
(8X300)
Explains how the 8X300 Execute instruction provides a fast and efficient method of converting one code structure to another in communications applications.
Signetics (1 pg.)

10 **"8X300 Fast IV Select"**
(8X300)
Explains how the Interface Vector (IV) bytes and working storage can be selected within the same instruction where it is used.
Signetics (1 pg.)

11 **"Interfacing the 8700 A/D Converter with the 8080 μP System"**
(8700, 8701, 8702)
Presents use of the 8700 A/D converter with the 8080 microprocessor. Provides techniques for interfacing the two and methods for handling multiple converts with increased throughput.
Teledyne Semiconductor AN-8 (6 pg.)

12 **"Minimum System Design TMS 9900 16-Bit Microprocessor"**
(TMS9900)
Explains system design, system performance, and minimum system configuration.
Texas Instruments Application Report (CA-184A (7 pg.)

13 **"TMS 5501 I/O in TMS 8080A μP Systems"**
(TMS5501, TMS8080A)
Describes operation and use of this input/output controller.
Texas Instruments Application Report (CA-185A (18 pg.)

14 **"Software Design for Microprocessors"**
(SBP0400, TMS1000, TMS5501, TMS8080, TMS9900)
Presents basic microprocessor fundamentals. Includes such topics as basic terms, basic machine architecture, instruction sets, and programming. Sample design problems are examined.
Texas Instruments $12.50 (385 pg.)

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MILITARY PARTS DIRECTORY

This section is divided into three parts: a table of those manufacturers willing to perform MIL-STD-883 screening, a two way military to commercial cross reference index, and the Qualified Parts List broken down into functions. It not only shows what devices are on the list and which manufacturers supply them, but also it decodes the military numbers into familiar terms.

how to use the military parts directory

The next page contains a table showing the manufacturers who have advised that they want to screen devices to MIL-STD-883 and/or perform other environmental screening. The table also indicates which companies are currently qualified to supply one or more devices on the QPL list. Such achievement is apt to indicate that these companies are well equipped to perform 883 testing. The following two pages provides convenient cross references between M38510 numbers and their commercial equivalents; plus indication of what devices are listed in the latest QPL.

The heart of this section is the functional QPL parts list. It is based on the latest Defense Electronics Supply Center Qualified Products List (QPL-38510-XX) at the time of publication. The revision and date of this list are indicated at the bottom of each page. Like the Master Selection Guide, the devices are classified my major functions; within each function the devices are arranged in alphanumeric order, which automatically groups CMOS together, 5400 Series together, etc.

A complete military part number includes a three letter suffix signifying the device class and packaging. The definitions of these letters are given in the Part Number Guide under "JAN Nomenclature." All the devices listed here meet class B and C requirements, a few devices (CMOS) meet class A specifications. The package styles and lead finishes that each manufacturer is qualified to supply can be determined by consulting the official QPL or by contacting the individual manufacturers. Once you have found the names of the companies you need to contact, you can reach them by using the information in the Manufacturers and Distributors Directory.

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MANUFACTURER	MIL-M-38510 QPL				MIL-STD-883 SCREENING			OTHER SCREENING	
	Linear	TTL	Other Bipolar	CMOS	Class A	Class B	Class C	Military	Industrial
Advanced Micro Devices	X	X			X	X	X	X	X
American Micro-systems, Inc.						X	X	X	X
Analog Devices						X	X		
Beckman Instruments					X	X	X	X	X
Burr-Brown Research						X	X	X	X
Datel						X	X	X	X
Electronic Arrays						X	X	X	X
EMM/Semi						X	X	X	X
Exar Integrated Systems						X	X	X	X
Fairchild Semiconductor	X	X	DTL		X	X	X	X	X
General Instrument						X	X		X
Harris Semiconductor			PROM		X	X	X	X	X
Hughes					X	X	X	X	X
Hybrid Systems					X	X	X	X	X
Intel						X	X	X	X
International Microcircuits								X	X
Intersil	X				X	X	X	X	X
ITT Semiconductor		X	DTL		X	X	X	X	X
LSI Computer Systems					X	X	X	X	X
Micro Networks						X	X	X	X
Micropac					X	X	X		
Micro Power						X	X	X	X
Mitel Semiconductor					X	X	X	X	X
Monolithic Memories					X	X	X	X	X
Mostek						X			
Motorola Semiconductor		X	ECL		X	X	X	X	X
National Semiconductor	X	X		X	X	X	X	X	X
NEC America						X	X		X
NEC Microcomputers						X	X		X
Nitron						X	X	X	X
Nortec						X	X	X	X
Plessey Semiconductor					X	X	X		
Precision Monolithics					X	X	X	X	X
Raytheon Semiconductor		X			X	X	X	X	X
RCA Solid State	X			X	X	X	X	X	X
Rockwell						X	X	X	X
Signetics	X	X			X	X	X	X	X
Silicon General					X	X	X	X	X
Siliconix					X	X	X	X	X
SMC Microsystems						X	X	X	X
Solid State Scientific					X	X	X	X	X
Solitron					X	X	X	X	X
Sprague Electric					X	X	X	X	X
Standard Microsystems						X	X	X	X
Synertek						X	X	X	X
Teledyne Philbrick					X	X	X	X	X
Teledyne Semiconductor						X	X	X	X
Texas Instruments	X	X	RAM		X	X	X	X	X
TRW					X	X	X	X	X
Zilog						X	X	X	X

EXPLANATION:

The "MIL-M-38510" section indicates the IC manufacturers currently providing Q.P.L. ICs. More detailed information on the specific devices is given in the Qualified Products lists which follow.

The "MIL-STD-883 Screening" section lists those manufacturers who are both set up and actively want to screen devices to the levels indicated. "Other Screening" shows those who report that they want business calling for special military and industrial environment screening procedures.

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Cross Reference
Commercial to Military

Device	M38510/	QPL
DG300	Proposed	
DG301	Proposed	
DF302	Proposed	
DG303	Proposed	
DG304	Proposed	
DG305	Proposed	
DG306	Proposed	
HPROM0512	20101	X
TMS4050	23502	X
TMS4060	23501	
0026	03501	
101A	10103	X
102	10601	
10501	06001	X
10502	06002	X
10504	06201	
10505	06003	X
10506	06004	X
10507	06005	X
10509	06006	X
10531	06101	
10535	06104	
10576	06103	
10597	06202	
106	10303	
10631	06102	
108A	10104	
110	10602	
111	10304	X
118	10107	X
2101	10105	
2108	10106	
2111	10305	
2680	23501	X
3018	10801	X
3045	10802	X
4000	05201	X
4001	05202	X
4002	05203	X
4006	05701	X
4007	05301	X
4008	05401	
4009	05501	X
4010	05502	X
4011	05001	X
4012	05002	X
4013	05101	X
4014	05702	X
4015	05703	X
4017	05601	X
4018	05602	X
4019	05302	X
4020	05603	X
4021	05704	X
4022	05604	X
4023	05003	X
4024	05605	X
4025	05204	X
4027	05102	X
4030	05303	X
4031	05705	X
4034	05706	
4041	05505	X
4049	05503	X
4050	05504	X
5280	23505	
5303	20101	
5304	20102	
54H00	02304	X
54H01	02306	X
54H04	02305	X
54H08	15501	X
54H10	02303	X
54H101	02205	X
54H103	02206	X
554H11	15502	X
43H20	02302	X
54H21	15503	X
43H22	02307	X
54H30	02301	X
54H40	02401	X
54H50	04001	X
54H51	04002	X
54H53	04003	X
54H54	04004	X
54H55	04005	X
54H72	02201	X
54H73	02202	X
54H74	02203	X
54H76	02204	X
54LS00	30001	X
54LS02	30301	X
54LS03	30002	X
54LS04	30003	X
54LS05	30004	X
54LS08	31004	X
54LS10	30005	X
54LS107	30108	X
54LS109	30109	X
54LS11	31001	X
54LS112	30103	X
54LS113	30104	X
54LS114	30105	X
54LS12	30006	X
54LS122	31403	
54LS123	31401	
54LS125	32301	
54LS126	32302	
54LS13	31301	X
54LS132	31302	X
54LS138	30701	X
54LS139	30702	X
54LS14	31303	X
54LS15	31002	X
54LS151	30901	X
54LS153	30902	X
54LS157	30903	X
54LS158	30904	X
54LS164	30606	
54LS174	30106	X
54LS175	30107	X
54LS181	30801	X
54LS194	30601	
54LS195	30602	
54LS20	30007	X
54LS21	31003	X
54LS22	30008	X
54LS221	31402	
54LS251	30905	
54LS253	30908	
54LS257	30906	
54LS258	30907	
54LS26	32102	X
54LS266	30303	X
54LS27	30302	X
54LS28	30204	X
54LS283	31202	X
54LS295	30606	
54LS30	30009	X
54LS32	30501	X
54LS365	32201	
54LS366	32202	
54LS367	32203	
54LS368	32204	
54LS37	30202	X
54LS38	30203	X
54LS395	30607	
54LS40	30201	X
54LS42	30703	
54LS47	30704	
54LS51	30401	X
54LS54	30402	X
54LS73	30101	X
54LS74	30102	X
54LS76	30110	X
54LS83	31201	X
54LS85	31101	X
54LS86	30502	X
54LS95	30603	
54LS96	30604	
54L00	02004	X
54L02	02701	X
54L03	02006	X
54L04	02005	X
54L10	02003	X
54L121	04201	
54L122	04202	
54L164	02802	
54L193	02503	
54L20	02002	X
54L30	02001	X
54L42	02901	
54L43	02902	
54L44	02903	
54L46	02904	
54L47	02905	
54L51	04101	
54L54	04102	
54L55	04103	
54L71	02101	X
54L72	02102	X
54L73	02103	X
54L74	02105	X
54L78	02104	X
54L86	02601	
54L90	02501	
54L91	02806	
54L93	02502	
54L95	02801	X
54S00	07001	X
54S02	07301	X
54S03	07002	X
54S04	07003	X
54S05	07004	X
54S08	08003	
54S09	08004	
54S10	07005	X
54S11	08001	X
54S112	07102	
54S113	07103	
54S114	07104	
54S133	07009	X
54S134	07010	X
54S135	07502	
54S140	08101	X
54S15	08002	X
54S151	07901	X
54S153	07902	X
54S157	07903	X
54S158	07904	X
54S174	07105	
54S175	07106	
54S181	07801	X
54S182	07802	
54S194	07601	
54S195	07602	
54S20	07006	X
54S22	07007	X
54S251	07905	
54S257	07906	
54S258	07907	
54S30	07008	
54S40	07201	X
54S51	07401	X
54S64	07402	X
54S65	07403	X
54S74	07101	X
54S85	08201	X
54S86	07501	X
5400	00104	X
5401	00107	X
5402	00401	X
5403	00109	X
5404	00105	X
5405	00108	X
5406	00801	X
5407	00803	X
5408	01601	X
5409	01602	X
5410	00103	X
54107	00203	X
5412	00106	X
54116	01503	X
54121	01201	X
54122	01202	X
54123	01203	X
54125	15301	
54126	15302	X
5413	15101	X
54132	15103	X
5414	15102	X
54145	01005	X
54147	15601	
54148	15602	
54150	01401	X
54151	01406	X
54153	01403	X
54154	15201	X
54155	15202	X
54156	15203	X
54157	01405	X
5416	00802	X
54160	01303	X
54161	01306	X
54162	01305	X
54163	01304	X
54164	00903	X
54165	00904	X
5417	00804	X
54170	01801	X
54174	01701	X
54175	01702	X
54180	01901	X
54181	01101	X
54182	01102	X
54192	01308	X
54193	01309	X
54194	00905	X
54195	00906	X
5420	00102	X
5423	00402	X
5425	00403	X
5426	00805	X
5427	00404	X
5428	16201	
5430	00101	X
5432	16101	X
54365	16301	
54366	16302	
54367	16303	
54368	16304	
5437	00302	X
5438	00303	X
5440	00301	X
5442	01001	X
5443	01002	X
5444	01003	X
5445	01004	X
5446	01006	
5447	01007	
5448	01008	X
5449	01009	X
5450	00501	X
5451	00502	X
5453	00503	X
5454	00504	X
5470	00206	X
5472	00201	X
5473	00202	X
5474	00205	X
5475	01501	X
5476	00204	X
5477	01502	X
5479	00207	X
5482	00601	X
5483	00602	X
5485	15001	X
5486	00701	X
5490	01307	X
5492	01301	X
5493	01302	X
5495	00901	X
5496	00902	X
55107	10401	X
55108	10402	X
55113	10405	X
55114	10403	X
55115	10404	X
555	10901	X
556	10902	
5603	20201	
5623	20202	
710	10301	X
711	10302	X
723	10201	X
741	10101	X
747	10102	X
76L42	02906	X
76L70	02805	X
7831	10406	
7832	10407	
8250	15204	X
8251	15205	X
8252	15206	X
9093	03304	
930	03001	X
9300	15901	X
9304	00603	X
9309	01404	X
9312	01402	X
9314	01504	X
932	03101	
9322	01405	X
9324	15002	X
933	03105	
935	03002	X
936	03003	X
940	03002	X
944	03102	
945	03301	
946	03004	X
948	03302	
950	03303	
951	03201	
957	03103	
958	03104	
9601	01204	X
9602	01205	X
962	03005	X

NOTE: Items marked X in the QPL column are listed on QPL-38510-30 with at least one source.

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Cross Reference
Military to Commercial

M38510/	Device	QPL	M38510/	Device	QPL	M38510/	Device	QPL	M38510/	Device	QPL
00101	5430	X	02006	54L03	X	06001	10501	X	15302	54126	X
00102	5420	X	02101	54L71	X	06002	10502	X	15501	54H08	X
00103	5410	X	02102	54L72	X	06003	10505	X	15502	54H11	X
00104	5400	X	02103	54L73	X	06004	10506	X	15503	54H21	X
00105	5404	X	02104	54L78	X	06005	10507	X	15601	54147	
00106	5412	X	02105	54L74	X	06006	10509	X	15602	54148	
00107	5401	X	02201	54H72	X	06101	10531		15901	9300	X
00108	5405	X	02202	54H73	X	06102	10631		16101	5432	X
00109	5403	X	02203	54H74	X	06103	10576		16201	5428	
00201	5472	X	02204	54H76	X	06104	10535		16301	16301	
00202	5473	X	02205	54H101	X	06201	10504		16302	16302	
00203	54107	X	02206	54H103	X	06202	10597		16303	16303	
00204	5476	X	02301	54H30	X	07001	54S00	X	16304	16304	
00205	5474	X	02302	54H20	X	07002	54S03	X	20101	HPROM0512	X
00206	5470	X	02303	54H10	X	07003	54S04	X	20102	5304	
00207	5479	X	02304	54H00	X	07004	54S05	X	20201	5603	
00301	5440	X	02305	54H04	X	07005	54S10	X	20202	5604	
00302	5437	X	02306	54H01	X	07006	54S20	X	23501	2680	X
00303	5438	X	02307	54H22	X	07007	54S22	X	23501	TMS4060	
00401	5402	X	02401	54H40	X	07008	54S30		23502	TMS4050	X
00402	5423	X	02501	54L90		07009	54S133	X	23505	5280	
00403	5425	X	02502	54L93		07010	54S134	X	30001	54LS00	X
00404	5427	X	02503	54L193		07101	54S74	X	30002	54LS03	X
00501	5450	X	02601	54L86		07102	54S112		30003	54LS04	X
00502	5451	X	02701	54L02	X	07103	54S113		30004	54LS05	X
00503	5453	X	02801	54L95	X	07104	54S114		30005	54LS10	X
00504	5454	X	02802	54L164		07105	54S174	X	30006	54LS12	X
00601	5482	X	02805	76L70		07106	54S175	X	30007	54LS20	X
00602	5483	X	02806	54L91		07201	54S40	X	30008	54LS22	X
00603	9304	X	02901	54L42		07301	54S02	X	30009	54LS30	X
00701	5486	X	02902	54L43		07401	54S51	X	30101	54LS73	X
00801	5406	X	02903	54L44		07402	54S64	X	30102	41574	X
00802	5416	X	02904	54L46		07403	54S65	X	30103	54LS112	X
00803	5407	X	02905	54L47		07501	54S86	X	30104	54LS113	X
00804	5417	X	02906	76L42		07502	54S135		30105	54LS114	X
00805	5426	X	03001	930	X	07601	54S194		30106	54LS174	X
00901	5495	X	03002	935	X	07602	54S195		30107	54LS175	X
00902	5496	X	03003	936	X	07801	54S181	X	30108	54LS107	X
00903	54164	X	03004	946	X	07802	54S182		30109	54LS109	X
00904	54165	X	03005	962	X	07901	54S151	X	30110	54LS76	X
00905	54194	X	03101	932		07902	54S153	X	30201	54LS40	X
00906	54195	X	03102	944		07903	54S157	X	30202	54LS37	X
01001	5442	X	03103	957		07904	54S158	X	30203	54LS38	X
01002	5443	X	03104	958		07905	54S251		30204	54LS28	X
01003	5444	X	03105	933		07906	54S257		30301	54LS02	X
01004	5445	X	03201	951		07907	54S258		30302	54LS27	X
01005	54145	X	03301	945		08001	54S11	X	30303	54LS266	X
01006	5446		03302	948		08002	54S15	X	30401	54LS51	X
01007	5447		03303	950		08003	54S08		30402	54LS54	X
01008	5448	X	03304	9903		08004	54S09		30501	54LS32	X
01009	5449	X	03501	0026		08101	54S140	X	30502	54LS86	X
01101	54181	X	04001	54H50	X	08201	54S85	X	30601	54LS194	
01102	54182	X	04002	54H51	X	10101	741	X	30602	54LS195	
01201	54121	X	04003	54H53	X	10102	747	X	30603	54LS95	
01202	54122	X	04004	54H54	X	10103	101A	X	30604	54LS96	
01203	54123	X	04005	54H55	X	10104	108A		30606	54LS164	
01204	9601	X	04101	54L51	X	10105	2101	X	30606	54LS295	
01205	9602	X	04102	54L54	X	10106	2108		30607	54LS395	
01301	5492	X	04103	54L55		10107	118	X	30701	54LS138	X
01302	5493	X	04201	54L121		10201	723	X	30702	54LS139	X
01303	54160	X	04202	54L122		10301	710	X	30703	54LS42	
01304	54163	X	05001	4011	X	10302	711	X	30704	54LS47	
01305	54162	X	05002	4012	X	10303	106		30801	54LS181	X
01306	54161	X	05003	4023	X	10304	111	X	30901	54LS151	X
01307	5490	X	05101	4013	X	10305	2111		30902	54LS153	X
01308	54192	X	05201	4000	X	10401	55107	X	30903	54LS157	X
01309	54193	X	05102	4027	X	10402	55108	X	30904	54LS158	X
01401	54150	X	05202	4001	X	10403	55114	X	30905	54LS251	
01402	9312	X	05203	4002	X	10404	55115	X	30906	54LS257	
01403	54153	X	05204	4025	X	10405	55113	X	30907	54LS258	
01404	9303	X	05301	4007	X	10406	7831		30908	54LS253	
01405	9322	X	05302	4019	X	10407	7832		31001	54LS11	X
01405	54157	X	05303	4030	X	10601	102		31002	54LS15	X
01406	54151	X	05401	4008		10602	110		31003	54LS21	X
01501	5475	X	05501	4009	X	10801	3018		31004	54LS08	X
01501	5475	X	05502	4010	X	10802	3045	X	31101	54LS85	X
01502	5477	X	05503	4049	X	10901	555	X	31201	54LS83	X
01503	54116	X	05504	4050	X	10902	556		31202	54LS283	X
01504	9314	X	05505	4041	X	15001	5485	X	31301	54LS13	X
01601	5408	X	05601	4017	X	15002	9324	X	31302	54LS14	X
01602	5409	X	05602	4018	X	15101	5413	X	31303	54LS132	X
01701	54174	X	05603	4020	X	15102	5414	X	31401	54LS123	
01702	54175	X	05604	4022	X	15103	54132	X	31402	54LS221	
01801	54170		05605	4024	X	15201	54154	X	31403	54LS122	
01901	54180	X	05701	4006	X	15202	54155	X	32102	54LS26	X
02001	54L30	X	05702	4014	X	15203	54156	X	32201	54LS365	X
02002	54L20	X	05703	4015	X	15204	8250	X	32202	54LS366	X
02003	54L10	X	05704	4021	X	15205	8251	X	32203	54LS367	X
02004	54L00	X	05705	4031	X	15206	8252	X	32204	54LS368	X
02005	54L04	X	05706	4034		15301	54125		32301	54LS125	
									32302	54LS126	

NOTE: Items marked X in the QPL column are listed on QPL-38510-30 with at least one source.

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DIGITAL

ARITHMETIC FUNCTION

Device	M38510/	Description	Source
5482	00601	2-Bit Binary Full Adder	ITT Motorola
5483	00602	4-Bit Binary Full Adder (Look-Ahead Carry)	ITT Motorola Signetics TI
5485	15001	4-Bit Magnitude Comparator	Motorola Signetics
54181	01101	Arithmetic Logic/ Function Generator	Signetics
54182	01102	Look-Ahead Carry Generator	Motorola Signetics
54LS83	31201	4-Bit Binary Full Adder	Raytheon
54LS85	31101	4-Bit Magnitude Comparator	Signetics TI
54LS181	30801	ALU/Function Generator	Signetics
54LS283	31202	4-Bit Binary Full Adder	Raytheon
54S85	08201	4-Bit Magnitude Comparator	Signetics
54S181	07801	ALU/Function Generator	Signetics
9304	00603	Dual Full Adder	Motorola
9324	15002	4-Bit Magnitude Comparator	Motorola

BUFFERS, INVERTERS

4007	05301	Dual Complementary Pair plus Inverter	National RCA
4009	05501	Hex Buffer/Converter, Inverting	National RCA
4010	05502	Hex Buffer/Converter, Non-Inverting	National RCA
4041	05505	Quad True/ Complement Buffer	RCA
4049	05503	Hex Buffer/Converter, Inverting	National RCA
4050	05504	Hex Buffer/Converter, Non-Inverting	National RCA
5404	00105	Hex Inverter	Fairchild ITT Motorola National Signetics TI
5405	00108	Hex Inverter, O/C	Fairchild ITT Motorola National Signetics TI
5437	00302	Quad 2-Input NAND Buffer	ITT Motorola National Signetics TI
5438	00303	Quad 2-Input NAND Buffer, O/C	Fairchild Motorola National Signetics TI
5440	00301	Dual 4-Input NAND Buffer	Fairchild ITT Motorola National Signetics TI
54125/6	15301/2	Quad Gated Buffer, 3 State	Signetics
54H04	02305	Hex Inverter	Fairchild ITT Motorola Signetics TI
54H40	02401	Dual 4-Input NAND Buffer	Motorola Signetics TI
54LS04	30003	Hex Inverter	Fairchild Motorola National Signetics
54LS05	30004	Hex Inverter, O/C	National Signetics
54LS28	30204	Quad 2-Input NOR Buffer	Signetics
54LS37	30202	Quad 2-Input NAND Buffer	National Signetics
54LS40	30201	Dual 4-Input NAND Buffer	National Signetics
54L04	02005	Hex Inverter	National
54S04	07003	Hex Inverter	Signetics
54S05	07004	Hex Inverter, O/C	Signetics
54S40	07201	Dual 4-Input NAND Buffer	Signetics
935	03002	Hex Inverter	ITT
936	03003	Hex Inverter	ITT

COUNTERS

Device	M38510/	Description	Source
4017	05601	Decade Counter/Divider, Decoded Output	RCA
4018	05602	Presettable Divide-by-N Counter	RCA
4020	05603	14-Bit Binary Counter	RCA
4022	05604	Divide-by-8 Counter/ Divider, Decoded Output	RCA
4024	05605	7-Bit Binary Counter	RCA
5490	01307	Decade Counter, Ripple	ITT Motorola
5492	01301	Divide-by-12 Counter (÷2, ÷6)	ITT Motorola Signetics
5493	01302	4-Bit Binary Counter	ITT Motorola Signetics
54160	01303	Synchronous Decade Counter	Motorola National Signetics
54161	01306	Synchronous 4-Bit Binary Counter	ITT Motorola National Signetics
54162	01305	Fully Synchronous Decade Counter	Motorola National Signetics
54163	01304	Fully Synchronous 4-Bit Binary Counter	Motorola National Signetics
54192	01308	Decade Up/Down Counter	Motorola
54193	01309	Binary Up/Down Counter	Motorola

DECODERS

5442	01001	BCD-to-Decimal Decoder	ITT Motorola Signetics
5443	01002	Excess 3-to-Decimal Decoder	Motorola Signetics
5444	01003	Excess 3-Gray-to-Decimal Decoder	Motorola Signetics
5445	01004	BCD-to-Decimal Decoder, O/C	Motorola
5448	01008	BCD-to-Seven Segment Decoder/Driver with 30V Output	Motorola
5449	01009	BCD-to-7 Segment Decoder, O/C	Motorola
54145	01005	BCD-to-7 Segment Decoder	Motorola
54148	15602	8-Bit Priority Encoder	Signetics
54154	15201	4-Line to 16-Line Decoder/Demultiplexer	Signetics
54155	15202	Dual 2-Line to 4-Line Decoder/Demultiplexer	Motorola
54156	15203	Dual 2-Line to 4-Line Decoder/Demultiplexer	Motorola
54LS138	30701	3-to-8-Line Decoder/ Demultiplexer	Fairchild Motorola Raytheon
54LS139	30702	Dual 2-Line to 4-Line Decoder/Demultiplexer	Fairchild Motorola Raytheon
54LS42	30703	BCD to Decimal Decoder	Motorola
8250	15204	Binary-to-Octal Decoder	Signetics
8251	15205	BCD-to-Decimal Decoder	Signetics
8252	15206	BCD-to-Decimal Decoder	Signetics

DRIVERS

5406	00801	Hex Inverter Buffer/ Driver, O/C High Voltage Output	Fairchild Motorola National TI
5407	00803	Hex Buffer/Driver, O/C High Voltage Output	Fairchild Motorola National TI
5416	00802	Hex Inverter Buffer/ Driver, O/C High Voltage Output	Fairchild Motorola National TI
5417	00804	Hex Buffer/Driver, O/C High Voltage Output	Fairchild Motorola National TI

FLIP-FLOPS

Device	M38510/	Description	Source
4013	05101	Dual "D" Flip-Flop with Set/Reset	National RCA
4027	05102	Dual J-K Master-Slave Flip-Flop	National RCA
5470	00206	Positive Edge-Triggered J-K Flip-Flop	Fairchild ITT Motorola Signetics TI
5472	00201	J-K Master Slave Flip-Flop (AND Inputs)	ITT Motorola National Signetics TI
5473	00202	Dual J-K Master Slave Flip-Flop	ITT Motorola National Signetics TI
5474	00205	Dual D-Type Edge-Triggered Flip-Flop	Fairchild ITT National Signetics TI
5476	00204	Dual J-K Master Slave Flip-Flop with Preset and Clear	ITT National Signetics TI
5479	00207	Dual D-Type Flip-Flop	Motorola
54107	00203	Dual J-K Master Slave Flip-Flop	Motorola National Signetics TI
54174	01701	Hex D-Type Flip-Flop	Motorola National Signetics
54175	01702	Quad D-Type Flip-Flop	Motorola National Signetics
54H72	02201	J-K Master-Slave Flip-Flip (AND Inputs)	Motorola Signetics
54H73	02202	Dual J-K Master-Slave Flip-Flop	Signetics Motorola
54H74	02203	Dual D-Type Edge-Triggered Flip-Flop	Signetics
54H76	02204	Dual J-K Flip-Flop	TI Signetics
54H101	02205	J-K Negative Edge-Triggered Flip-Flop (AND-OR Inputs)	Motorola Signetics
54H103	02206	Dual J-K Negative Edge Triggered Flip-Flop	Motorola Signetics
54LS73	30101	Dual J-K Master Slave Flip-Flop	TI
54LS74	30102	Dual D-Type Positive Edge-Triggered Flip-Flop with Preset and Clear	Motorola TI
54LS76	30110	Dual J-K Master Slave Flip-Flop with Preset and Clear	Signetics TI
54LS107	30108	Dual Master Slave Flip-Flop	TI
54LS109	30109	Dual J-K Positive Edge-Triggered Flip-Flop with Preset and Clear	Fairchild Motorola Signetics TI
54LS112	30103	Dual J-K Negative Edge-Triggered Flip-Flop with Preset and Clear	Fairchild Signetics TI
54LS113	30104	Dual J-K Negative Edge-Triggered Flip-Flop with Separate Preset and Clock	TI
54LS114	30105	Dual J-K Negative Edge-Triggered Flip-Flop with Clock, Clear, and Preset	Fairchild TI
54LS174	30106	Hex D-Type Flip-Flop	AMD Motorola Raytheon Signetics TI
54LS175	30107	Quad D-Type Flip-Flop	AMD Fairchild Motorola Raytheon TI
54L71	02101	J-K Master-Slave Flip-Flop (AND-OR Inputs)	National
54L72	02102	J-K Master-Slave Flip-Flop (AND Inputs)	National
54L73	02103	Dual J-K Master-Slave Flip-Flop	National
54L74	02105	Dual D-Type Edge-Triggered Flip-Flop	National
54L78	02104	Dual J-K Master-Slave Flip-Flop	National
54S74	07101	Dual D Flip-Flop	Signetics

BASED ON QPL-38510-31, 1 NOVEMBER 1977

GATES, AND/NAND

Device	M38510/	Description	Source
4011	05001	Quad 2-Input NAND Gate	National RCA
4012	05002	Dual 4-Input NAND Gate	National RCA
4023	05003	Triple 3-Input NAND Gate	National RCA
5400	00104	Quad 2-Input NAND Gate	Fairchild ITT Motorola National Signetics TI
5401	00107	Quad 2-Input NAND Gate, O/C	Fairchild ITT Motorola National Signetics TI
5403	00109	Quad 2-Input NAND Gate, O/C	Fairchild ITT Motorola National Signetics TI
5408	01601	Quad 2-Input AND Gate	Fairchild ITT Motorola Signetics
5409	01602	Quad 2-Input AND Gate, O/C	Fairchild Motorola Signetics
5410	00103	Triple 3-Input NAND Gate	Fairchild ITT Motorola National Signetics TI
5412	00106	Triple 3-Input NAND Gate, O/C	TI
5420	00102	Dual 4-Input NAND Gate	Fairchild ITT Motorola National Signetics TI
5426	00805	Quad 2-Input NAND Gate, O/C	Signetics
5430	00101	8-Input NAND Gate	Fairchild ITT Motorola National Signetics TI
54H00	02304	Quad 2-Input NAND Gate	Fairchild ITT Motorola Signetics TI
54H01	02306	Quad 2-Input NAND Gate, O/C	Motorola Signetics TI
54H08	15501	Quad 2-Input AND Gate	Motorola Signetics
	15504	Quad 2-Input AND Gate	Motorola
54H10	02303	Triple 3-Input NAND Gate	Fairchild ITT Motorola Signetics TI
54H11	15502	Triple 3-Input AND Gate	Motorola Signetics
54H20	02302	Dual 4-Input NAND Gate	Fairchild ITT Motorola Signetics TI
54H21	15503	Dual 4-Input AND Gate	Motorola Signetics
54H22	02307	Dual 4-Input NAND Gate, O/C	Fairchild Motorola Signetics
54H30	02301	8-Input NAND Gate	Fairchild ITT Motorola Signetics TI
54LS00	30001	Quad 2-Input NAND Gate	Fairchild National Motorola Signetics
54LS03	30002	Quad 2-Input NAND Gate, O/C	Motorola National Signetics

GATES, AND/NAND (cont)

Device	M38510/	Description	Source
54LS08	31004	Quad 2-Input AND Gate	Fairchild Motorola National Raytheon Signetics TI
54LS10	30005	Triple 3-Input NAND Gate	Fairchild National Signetics
54LS11	31001	Triple 3-Input AND Gate	Fairchild Motorola National Raytheon Signetics TI
54LS12	30006	Triple 3-Input NAND Gate, O/C	National Signetics
54LS15	31002	Triple 3-Input AND Gate, O/C	National Signetics
54LS20	30007	Dual 4-Input NAND Gate	Fairchild National Signetics
54LS21	31003	Dual 4-Input AND Gate	Fairchild National Signetics
54LS22	30008	Dual 4-Input NAND Gate, O/C	National Signetics
54LS26	32102	Quad 2-Input NAND Gate, O/C, to 15V	Signetics
54LS30	30009	8-Input NAND Gate	Fairchild National Signetics
54LS38	30203	Quad 2-Input NAND Gate, O/C	National Raytheon TI
54L00	02004	Quad 2-Input NAND Gate	National
54L03	02006	Quad 2-Input NAND Gate, O/C	National
54L10	02003	Triple 3-Input NAND Gate	National
54L20	02002	Dual 4-Input NAND Gate	National
54L30	02001	8-Input NAND Gate	National
54S00	07001	Quad 2-Input NAND Gate	Signetics
54S03	07002	Quad 2-Input NAND Gate, O/C	Signetics
54S10	07005	Triple 3-Input NAND Gate	Signetics
54S11	08001	Triple 3-Input AND Gate	Signetics
54S15	08002	Triple 2-Input AND Gate, O/C	Signetics
54S20	07006	Dual 4-Input NAND Gate	Signetics
54S22	07007	Dual 4-Input NAND Gate, O/C	Signetics
54S133	07009	13-Input NAND Gate	Signetics
54S134	07010	12-Input NAND Gate, 3 State	Signetics
930	03001	Dual 4-Input NAND Gate, Expandable	Fairchild ITT
946	03004	Quad 2-Input NAND Gate	Fairchild ITT
962	03005	Triple 3-Input NAND Gate	Fairchild ITT

GATES, AND-OR/AND-OR-INVERT

Device	M38510/	Description	Source
4019	05302	Quad AND-OR Select Gate	National RCA
5450	00501	2-2-Input AOI Gate, Expandable	ITT Motorola National Signetics TI
5451	00502	2-2-Input AOI Gate, Expandable	ITT Motorola National Signetics TI
5453	00503	2-2-2-2-Input AOI Gate, Expandable	ITT Motorola National Signetics TI
5454	00504	2-2-2-2-Input AOI Gate	ITT Motorola National Signetics TI
54H50	04001	2-2-Input AOI Gate, Expandable	Motorola Signetics
54H51	04002	Dual 2-2-Input AOI Gate	Motorola Signetics
54H53	04003	2-2-2-3-Input AOI Gate, Expandable	Motorola Signetics

GATES, AND-OR/AND-OR-INVERT (cont)

Device	M38510/	Description	Source
54H54	04004	2-2-2-3-Input AOI Gate	Motorola Signetics
54H55	04005	4-4-Input AOI Gate, Expandable	Motorola Signetics
54LS51	30401	Dual 2-3-Input AOI Gate	Motorola National Raytheon Signetics
54LS54	30402	2-2-2-3-Input AOI Gate	Motorola National Raytheon Signetics
54S51	07401	2-2-Input AOI Gate	Signetics
54S64	07402	4-2-3-2-Input AOI Gate	Signetics
54S65	07403	4-2-3-2-Input AOI Gate, O/C	Signetics

GATES, EXCLUSIVE OR/NOR

Device	M38510/	Description	Source
4030	05303	Quad Exclusive OR Gate	National
5486	00701	Quad 2-Input Exclusive OR Gate	Fairchild ITT Motorola Signetics TI
54LS86	30502	Quad 2-Input Exclusive OR	Motorola National Signetics
54LS266	30303	Quad 2-Input Exclusive NOR Gate, O/C	National Signetics TI
54S86	07501	Quad 2-Input Exclusive OR Gate	Signetics
10507	06005	Triple 2-Input Exclusive OR/NOR Gate	Motorola

GATES, OR/NOR

Device	M38510/	Description	Source
4000	05201	Dual 3-Input NOR Gate plus Inverter	RCA
4001	05202	Quad 2-Input NOR Gate	National RCA
4002	05203	Dual 4-Input NOR Gate	National RCA
4025	05204	Triple 3-Input NOR Gate	National RCA
5402	00401	Quad 2-Input NOR Gate	Fairchild ITT Motorola National Signetics TI
5423	00402	Dual 4-Input NOR Gate with Strobe, Expandable	Motorola TI
5425	00403	Dual 4-Input NOR Gate with Strobe	Motorola TI
5427	00404	Triple 3-Input NOR Gate	Fairchild Motorola Signetics TI
5432	16101	Quad 2-Input OR Gate	Signetics
54LS02	30301	Quad 2-Input NOR Gate	Fairchild National Raytheon Signetics
54LS27	30302	Triple 3-Input NOR Gate	Fairchild Motorola National Raytheon Signetics TI
54LS32	30501	Quad 2-Input OR Gate	Fairchild Motorola National Raytheon Signetics
54L02	02701	Quad 2-Input NOR Gate	National
54S02	07301	Quad 2-Input NOR Gate	Signetics
10501	06001	Quad 2-Input OR/NOR Gate	Motorola
10502	06002	Quad 2-Input Gate (3 NOR, 1 OR/NOR)	Motorola
10505	06003	2-3-2-Input OR/NOR Gate	Motorola
10506	06004	4-3-3-Input OR/NOR Gate	Motorola
10509	06006	4-5-Input OR/NOR Gate	Motorola

LATCHES

Device	M38510/	Description	Source
5475	01501	Quad Bistable Latch, Complementary Output	Motorola Signetics
5477	01502	Quad Bistable Latch	Motorola Signetics
54116	01503	Dual 4-Bit Latch with Clear	Signetics
9314	01504	Quad Multifunction Latch	Motorola

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MULTIPLEXERS

Device	M38510/	Description	Source
54150	01401	16-Channel Data Selector/Multiplexer	Signetics
54151	01406	8-Input Multiplexer	Motorola Signetics
54153	01403	Dual 4-Channel Data Selector/Multiplexer	Motorola National Signetics
54LS151	30901	8-Input Multiplexer	Raytheon
54LS153	30902	Dual 4-Channel Data Selector/Multiplexer	Raytheon
54LS157	30903	Quad 2-Input Multiplexer, Non-Inverting	Raytheon
54LS158	30904	Quad 2-Input Multiplexer, Inverting	Raytheon
54S151	07901	8-Input Multiplexer	Signetics
54S153	07902	Dual 4-Channel Data Selector/Multiplexer	Signetics
54S157	07903	Quad 2-Input Multiplexer, Non-Inverting	Signetics
54S158	07904	Quad 2-Input Multiplexer, Inverting	Signetics
9309	01404	Dual 4-Input Multiplexer	AMD ITT Motorola Signetics
9312	01402	8-Channel Data Selector/ Multiplexer	AMD ITT Motorola
9322	01405	Quad 2-Input Data Selector/Multiplexer (Non-Inverting)	AMD ITT Motorola Signetics

MULTIVIBRATORS

54121	01201	Monostable Multivibrator	ITT Motorola Signetics
54122	01202	Retriggerable Monostable Multivibrator with Clear	Motorola
54123	01203	Dual Retriggerable Monostable Multivibrator with Clear	Motorola Signetics
9601	01204	One Shot Multivibrator	Motorola
9602	01205	Dual One Shot Multivibrator	Motorola

MISCELLANEOUS

5413	15101	Dual 4-Input NAND Schmitt Trigger	Motorola Signetics
5414	15102	Hex Schmitt Trigger, Inverting	Motorola Signetics
54132	15103	Quad 2-Input NAND Schmitt Trigger	Motorola Signetics
54180	01901	9-Bit Odd/Even Parity Generator/Checker	Motorola Signetics
54LS13	31301	Dual 4-Input NAND Schmitt Trigger	Signetics TI
54LS14	31302	Hex Schmitt Trigger, Inverting	Signetics TI
54LS132	31303	Quad 2-Input NAND Schmitt Trigger	Signetics TI

INTERFACE

ANALOG SWITCHES

DG300	—	Dual SPST	See Siliconix information on pages 160 through 167
DG301	—	SPDT	
DG302	—	Dual DPST	
DG303	—	Dual SPDT	
DG304	—	Dual SPST	
DG305	—	SPDT	
DG306	—	Dual DPST	

The above Analog Switches have been proposed for QPL Status. Detailed technical information is found on the pages indicated above. To determine their current status consult Siliconix.

LINE DRIVERS AND RECEIVERS

54S140	08101	Dual 4-Input Positive NAND Line Driver	Signetics
55107	10401	Differential Line Receiver	Fairchild TI
55108	10402	Differential Line Receiver	Fairchild TI
55113	10405	Dual Differential Line Driver, Three-State	
55114	10403	Dual Differential Line Driver	Fairchild
55115	10404	Dual Differential Line Receiver	Fairchild

LINEAR

AMPLIFIERS

Device	M38510/	Description	Source
101A	10103	Operational Amplifier	AMD Fairchild National
108A	10104	Operational Amplifier	Fairchild National
118	10107	Operational Amplifier	National
741	10101	Operational Amplifier	AMD Fairchild Intersil National Raytheon
747	10102	Dual Operational Amplifier	AMD Fairchild

COMPARATORS

111	10304	Voltage Comparator	AMD Fairchild National
710	10301	Voltage Comparator	Fairchild
711	10302	Dual Voltage Comparator	Fairchild

TIMERS

555	10901	Timer	Signetics

TRANSISTOR ARRAYS

3045	10802	Transistor Array	Fairchild RCA

VOLTAGE REGULATORS

723	10201	Voltage Regulator	Fairchild

MEMORY

PROM

HPROM0512	20101	512-Bit Programmable Read Only Memory	Harris

RAM

~~2680~~	~~23501~~	~~4096x1 Dynamic RAM~~	~~TI~~
TMS4050	23502	4096x1 Dynamic RAM	TI

SHIFT REGISTERS

4006	05701	18-Bit Static S.R.	National RCA
4014	05702	8-Bit Static S.R. (Synchronous)	National RCA
4015	05703	Dual 4-Bit Static S.R.	National RCA
4021	05704	8-Bit Static S.R. (Asynchronous)	National RCA
4031	05705	64-Bit Static S.R.	National RCA
54L95	02801	4-Bit Parallel Access S.R.	National
5495	00901	4-Bit Parallel Access S.R.	Motorola Signetics
5496	00902	5-Bit S.R.	Motorola Signetics
54164	00903	8-Bit Serial-In Parallel-Out S.R.	ITT Signetics
54165	00904	8-Bit Parallel-Serial S.R.	Motorola
54194	00905	4-Bit Universal S.R.	Motorola
54195	00906	4-Bit Parallel Access S.R.	Motorola
54LS164	30605	8-Bit Serial-In Parallel-Out S.R.	Signetics
9300	15901	Universal 4-Bit S.R.	Motorola
9328	15902	Dual 8-Bit S.R.	Motorola

BASED ON QPL-38510-31, 1 NOVEMBER 1977

SPECIFICATION REQUIREMENTS FOR MICROCIRCUITS, CMOS, ANALOG SWITCH WITH DRIVER, MONOLITHIC, SILICON

1. *SCOPE*

1.1 Scope. This specification covers the detail requirements for silicon, CMOS, monolithic, analog switches. Three product assurance classes and a choice of case outline and lead finish are provided for each type and are reflected in the complete part number.

1.2 Part Number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device Type. The device type shall be as shown in the following:

Device Type	Circuit
01	2x, SPST Switches, TTL Input Compatible
02	1x, SPDT Switch, TTL Input Compatible
03	2x, DPST Switches, TTL Input Compatible
04	2x, SPDT Switches, TTL Input Compatible
05	2x, SPST Switches, CMOS Input Compatible
06	1x, SPDT Switch, CMOS Input Compatible
07	2x, DPST Switches, CMOS Input Compatible
08	2x, SPDT Switches, CMOS Input Compatible

1.2.2 Device Class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case Outline. The case outline shall be designated as follows:

Outline Letter	MIL-M-38510 Appendix C Case Outline
C	D-1 (14-Lead, 1/4" x 3/4", dual-in-line)
D	F-2 (14-Lead, 1/4" x 3/8", flat-pack)
I	A-2 (10-Lead, Can, TO-100)

1.2.4 Absolute Maximum Ratings

V_{IN} to Ground . . . . . V+ + 18, V+ – 36 Vdc
V+ to V– . . . . . +36 Vdc
V+ to Ground . . . . . +36 Vdc
V_S or V_D . . . . . V_1, V_2
Current (Any Terminal) . . . . . 30 mA
Pulsed 1 ms, 10% Duty Cycle (S or D Only) . . . 100 mA
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 60 Sec) . . . . . 300°C
Junction Temperature . . . . . T_J = 150°C

1.2.5 Recommended Operating Conditions

V+ . . . . . +15 Vdc
V– . . . . . –15 Vdc
GND . . . . . 0 Vdc
Ambient Temperature Range . . . . . –55°C to +125°C

1.2.6 Power and Thermal Characteristics

Package	Case Outline	Maximum Allowable Power Dissipation 1/	Thermal Resistance Junction to Case 2/
14 Lead DIP	C	275 mW	0.091°C/mW
14 Lead FP	D	250 mW	0.100°C/mW
10 Lead Can	I	150 mW	0.167°C/mW

NOTES:
1/ All leads welded or soldered to PC board.
2/ Applies only when $T_A \geq 75°C$.

2. *APPLICABLE DOCUMENTS*

2.1 The following document, of the issue in effect on date of invitation for bids or request for proposal, forms a part of this specification to the extent specified herein.

SPECIFICATION
Military
MIL-M-38510—Microcircuits, General Specification for.
STANDARD
Military
MIL-STD-883—Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, drawings, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. *REQUIREMENTS*

3.1 Detail Specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, Construction, and Physical Dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and 1.2.3 herein.

3.2.1 Circuit Diagram and Terminal Connections. The circuit diagram and terminal connections shall be as specified in Figure 1.

3.3 Lead Material and Finish. Lead material and finish shall be in accordance with MIL-M-38510.

3.4 Electrical Performance Characteristics. The following electrical performance characteristics apply over the full operating ambient temperature range of –55°C to +125°C and for supply voltages as indicated in 1.2.5, unless otherwise specified.

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3.4.1 Switch Operation. The analog switches listed below are guaranteed to turn "on" wither a "low" input ($V_{INL} \leq$ 0.8 V for the 01-04 devices and $V_{INL} \leq$ 3.5 V for the 05-08 devices) or "high" input ($V_{INH} \geq$ 4 V for the 01-04 devices and $V_{INH} \geq$ 11 V for the 05-08 devices) as specified in Table A.

3.5 Electrical Test Requirements. Electrical test requirements shall be as specified in Table III for the applicable device type and device class. The subgroups of Table III and the limits of Table IV which constitute the minimum electrical test requirements for screening, qualification and quality conformance, by device class are specified in Table II.

Table A. Switch Function (Truth Table)

Device Types	V_{IN}	Channels ON	Channels OFF	Device Types	V_{IN}	Channels ON	Channels OFF
01 and 05	V_{INL}		1, 2	03 and 07	V_{INL}		1, 2, 3, 4
	V_{INH}	1, 2			V_{INH}	1, 2, 3, 4	
02 and 06	V_{INL}	2	1	04 and 08	V_{INL}	3, 4	1, 2
	V_{INH}	1	2		V_{INH}	1, 2	3, 4

Table I. Electrical Performance Characteristics

Characteristic		Conditions Same as 1.2.5, Unless Otherwise Specified	T_A/°C	Limits 01, 02, 03, 04 Min	Limits 01, 02, 03, 04 Max	Limits 05, 06, 07, 08 Min	Limits 05, 06, 07, 08 Max	Units
R_{DS}	Drain-Source ON Resistance	V_{IN} = (See Table A) V_D = −10 V, I_S = +10 mA	−55, 25		50		50	Ω
			125		75		75	
		V_{IN} = (See Table A) V_D = +10 V, I_S = −10 mA	−55, 25		50		50	
			125		75		75	
$I_{D(on)}$	Channel ON Leakage Current	$V_D = V_S$ = +15 V	−55, 25		1		1	nA
			125		100		100	
		$V_D = V_S$ = −15 V	−55, 25		−2		−2	
			125		−200		−200	
$I_{S(off)}$	Source OFF Leakage Current	V_{IN} = (See Table A) V_D = −15 V, V_S = +15 V	25		1		1	nA
			125		100		100	
		V_{IN} = (See Table A) V_D = +15 V, V_S = −15 V	25		−1		−1	
			125		−100		−100	
$IF_{S(off)}$	Functional Source OFF Leakage Current	V_{IN} = (See Table A), V_D = −15 V, V_S = +15 V	−55		0.1		0.1	μA
		V_{IN} = (See Table A), V_D = +15 V, V_S = −15 V	−55		−0.1		−0.1	
$I_{D(off)}$	Drain OFF Leakage Current	V_{IN} = (See Table A) V_D = +15 V, V_S = −15 V	25		1		1	nA
			125		100		100	
		V_{IN} = (See Table A) V_D = −15 V, V_S = +15 V	25		−1		−1	
			125		−100		−100	
$IF_{D(off)}$	Functional Drain OFF Leakage Current	V_{IN} = (See Table A), V_D = +15 V, V_S = −15 V	−55		0.1		0.1	μA
		V_{IN} = (See Table A), V_D = −15 V, V_S = +15 V	−55		−0.1		−0.1	
I_{INL}	Input Current Input Voltage Low	V_{IN} = 0	−55, 25		−1		−1	
			125		−1		−1	
I_{INH}	Input Current Input Voltage High	V_{IN} = +5 V	−55, 25		−1			μA
			125		−1			
		V_{IN} = +15 V	−55, 25		1		1	
			125		1		1	
$t_{(on)}$	Turn-ON Time	See Switching Circuit, Figure 3	25		300		250	nsec
$t_{(off)}$	Turn-OFF Time		25		250		150	
I+	Positive Supply Current	V_{IN} = 0.8 V (All Inputs)	−55, 25		0.010			mA
			125		0.100			
		V_{IN} = 4.0 V (One Input), 1/	−55		1.000			
			25, 125		0.500			
		V_{IN} = 0 (All Inputs)	−55, 25				0.010	
			125				0.100	
		V_{IN} = 15 V (All Inputs)	−55, 25				0.010	
			125				0.100	
I−	Negative Supply Current	V_{IN} = 0.8 V (All Inputs)	−55, 25		−0.010			
			125		−0.100			
		V_{IN} = 4.0 V (One Input), 1/	−55, 25		−0.010			
			125		−0.100			
		V_{IN} = 0 (All Inputs)	−55, 25				−0.010	
			125				−0.100	
		V_{IN} = 15 V (All Inputs)	−55, 25				−0.010	
			125				−0.100	

Note: 1/ All other inputs = 0 V

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TABLE II. Electrical Test Requirements

MIL-STD-883 Test Requirement	Class A Devices	Class B Devices	Class C Devices
Interim Electrical Parameters (Pre Burn-In) (Method 5004)	1	1	None
Final Electrical Test Parameters (Method 5004)	1*, 2, 3, 9	1*, 2, 3, 9	1
Group A Test Requirements (Method 5005)	1, 2, 3, 7, 8, 9	1, 2, 3, 7, 8, 9	1, 2, 3, 7, 8, 9
Groups B, C and D Endpoint Electrical Parameters (Method 5005)	1, 2, 3 and Table V Delta Limits	Table V Delta Limits and Limits	Table V Delta Limits and Limits

*PDA applies to subgroup 1 (Sec. 4.3(b)).

3.6 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2. At the option of the manufacturer, the following marking may be omitted from the body of the microcircuit, but shall be retained on the initial container.

(a) Country of origin.

3.7 Microcircuit Group Assignment. The devices covered by this specification shall be in technology group C.

4. *PRODUCT ASSURANCE PROVISIONS*

4.1 Sampling and Inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007 of MIL-STD-883, except as modified herein.

Table III. Group A Inspection for Device Types 01 to 08

Subgroup	Symbol	MIL-STD-883 Method	Test	Conditions (V_1 = +15 V, V_2 = −15 V, GND = 0, Unless Otherwise Specified)	Limits Min	Limits Max	Units
	I_+	3005	1	V_{IN} = (low, 1/), 3/		10	μA
	I_+	3005	2	V_{IN} = (high, 1/), 3/		2/	μA
	I_-	3005	3	V_{IN} = (low, 1/), 3/		−10	μA
	I_-	3005	4	V_{IN} = (high, 1/), 3/		−10	μA
	I_{INL}	3009	5	V_{IN} = 0, 3/		−1	μA
	I_{INH}	3010	6	V_{IN} = +5 V, 3/, 4/		1	μA
	I_{INH}	3010	7	V_{IN} = +15 V, 3/		1	μA
1 T_A = 25°C	R_{DS}		8	V_{IN} = 1/, V_D = −10 V, I_S = +10 mA, 5/		50	Ω
	R_{DS}		9	V_{IN} = 1/, V_D = +10 V, I_S = −10 mA, 5/		50	Ω
	$I_{D(off)}$		10	V_{IN} = 1/, V_D = +15 V, V_S = −15 V, 5/		1	nA
	$I_{D(off)}$		11	V_{IN} = 1/, V_D = −15 V, V_S = +15 V, 5/		−1	nA
	$I_{S(off)}$		12	V_{IN} = 1/, V_D = −15 V, V_S = +15 V, 5/		1	nA
	$I_{S(off)}$		13	V_{IN} = 1/, V_D = +15 V, V_S = −15 V, 5/		−1	nA
	$I_{D(on)}$		14	V_{IN} = 1/, V_D = V_S = +15 V		1	nA
	$I_{D(on)}$		15	V_{IN} = 1/, V_D = V_S = −15 V		−2	nA

Table III. Group A Inspection for Device Types 01 to 08 (Continued)

Subgroup	Symbol	MIL-STD-883 Method	Test	Conditions (V_1 = +15 V, V_2 = −15 V, GND = 0, Unless Otherwise Specified)	Limits Min	Limits Max	Units
2 T_A = 125°C	I+	3005	1	V_{IN} = (low, 1/), 3/		100	µA
	I+	3005	2	V_{IN} = (high, 1/), 3/		2/	µA
	I−	3005	3	V_{IN} = (low, 1/), 3/		−100	µA
	I−	3005	4	V_{IN} = (high, 1/), 3/		−100	µA
	I_{INL}	3009	5	V_{IN} = 0, 3/		−1	µA
	I_{INH}	3010	6	V_{IN} = +5 V, 3/, 4/		−1	µA
	I_{INH}	3010	7	V_{IN} = +15 V, 3/		1	µA
	R_{DS}		8	V_{IN} = 1/, V_D = −10 V, I_S = +10 mA, 5/		75	Ω
	R_{DS}		9	V_{IN} = 1/, V_D = +10 V, I_S = −10 mA, 5/		75	Ω
	$I_{D(off)}$		10	V_{IN} = 1/, V_D = +15 V, V_S = −15 V, 5/		100	nA
	$I_{D(off)}$		11	V_{IN} = 1/, V_D = −15 V, V_S = +15 V, 5/		−100	nA
	$I_{S(off)}$		12	V_{IN} = 1/, V_D = −15 V, V_S = +15 V, 5/		100	nA
	$I_{S(off)}$		13	V_{IN} = 1/, V_D = +15 V, V_S = −15 V, 5/		−100	nA
	$I_{D(on)}$		14	V_{IN} = 1/, V_D = V_S = +15 V		100	nA
	$I_{D(on)}$		15	V_{IN} = 1/, V_D = V_S = −15 V		−200	nA
3 T_A = −55°C	I+	3005	1	V_{IN} = (low, 1/), 3/		10	µA
	I+	3005	2	V_{IN} = (high, 1/), 3/		2/	µA
	I−	3005	3	V_{IN} = (low, 1/), 3/		−10	µA
	I−	3005	4	V_{IN} = (high, 1/), 3/		−10	µA
	I_{INL}	3009	5	V_{IN} = 0, 3/		−1	µA
	I_{INH}	3010	6	V_{IN} = +5 V, 3/, 4/		−1	µA
	I_{INH}	3010	7	V_{IN} = +15 V, 3/		1	µA
	R_{DS}		8	V_{IN} = 1/, V_D = −10 V, I_S = +10 mA, 5/		50	Ω
	R_{DS}		9	V_{IN} = 1/, V_D = +10 V, I_S = −10 mA, 5/		50	Ω
7 T_A = +25°C	R_{DS}		1	V_{IN} = 1/, V_D = −10 V, I_S = +10 mA, 5/		50	Ω
	R_{DS}		2	V_{IN} = 1/, V_D = +10 V, I_S = −10 mA, 5/		50	Ω
	$I_{D(off)}$		3	V_{IN} = 1/, V_D = +15 V, V_S = −15 V, 5/		1	nA
	$I_{D(off)}$		4	V_{IN} = 1/, V_D = −15 V, V_S = +15 V, 5/		−1	nA
	$I_{S(off)}$		5	V_{IN} = 1/, V_D = −15 V, V_S = +15 V, 5/		1	nA
	$I_{S(off)}$		6	V_{IN} = 1/, V_D = +15 V, V_S = −15 V, 5/		−1	nA
8 T_A = +125°C	R_{DS}		1	V_{IN} = 1/, V_D = −10 V, I_S = +10 mA, 5/		75	Ω
	R_{DS}		2	V_{IN} = 1/, V_D = +10 V, I_S = −10 mA, 5/		75	Ω
	$I_{D(off)}$		3	V_{IN} = 1/, V_D = +15 V, V_S = −15 V, 5/		100	nA
	$I_{D(off)}$		4	V_{IN} = 1/, V_D = −15 V, V_S = +15 V, 5/		−100	nA
	$I_{S(off)}$		5	V_{IN} = 1/, V_D = −15 V, V_S = +15 V, 5/		100	nA
	$I_{S(off)}$		6	V_{IN} = 1/, V_D = +15 V, V_S = −15 V, 5/		−100	nA
8 T_A = −55°C	R_{DS}		1	V_{IN} = 1/, V_D = −10 V, I_S = +10 mA, 5/		50	Ω
	R_{DS}		2	V_{IN} = 1/, V_D = +10 V, I_S = −10 mA, 5/		50	Ω
	$IF_{D(off)}$		3	V_{IN} = 1/, V_D = +15 V, V_S = −15 V, 5/		0.1	µA
	$IF_{D(off)}$		4	V_{IN} = 1/, V_D = −15 V, V_S = +15 V, 5/		−0.1	µA
	$IF_{S(off)}$		5	V_{IN} = 1/, V_D = −15 V, V_S = +15 V, 5/		0.1	µA
	$IF_{S(off)}$		6	V_{IN} = 1/, V_D = +15 V, V_S = −15 V, 5/		−0.1	µA
9 T_A = +25°C	$t_{(on)}$	3003	1	t_r < 20 nsec, t_f < 20 nsec, See Figure 3, 5/		2/	nsec
	$t_{(off)}$	3003	2	t_r < 20 nsec, t_f < 20 nsec, See Figure 3, 5/		2/	nsec

Notes: 1/ Test conditions are from Table I.
2/ Test limits are from Table I.
3/ Each input is tested individually.
4/ This test is not performed on the 05-08 products.
5/ Each output is measured individually.

Table IV. Groups B, C and D Endpoint Electrical Parameters (Conditions from Group A, Subgroup 1 Testing)

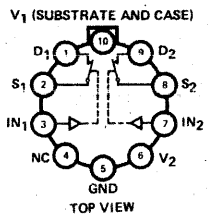
Test	All Products Limit	All Products Delta 1/
R_{DS}	50 Ω	3 Ω or 10%
$I_{D(off)}$	1 nA	0.5 nA
$I_{S(off)}$	1 nA	0.5 nA

Notes: 1/ When two delta limits are specified, only the larger of the two limits shall apply.

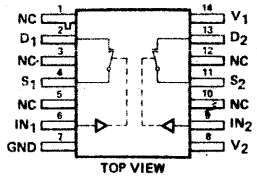
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Device Type –01, –05

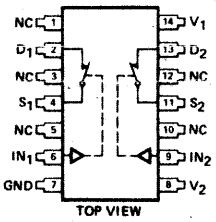
Case I



Case D

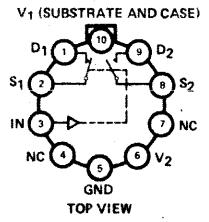


Case C

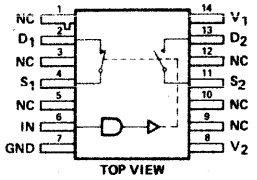


Device Type –02, –06

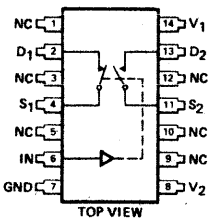
Case I



Case D

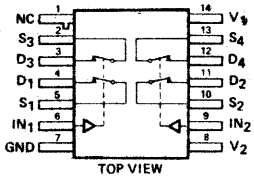


Case C

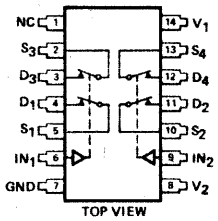


Device Type –03, –07

Case D

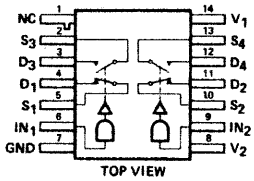


Case C

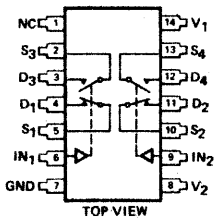


Device Type –04, –08

Case D

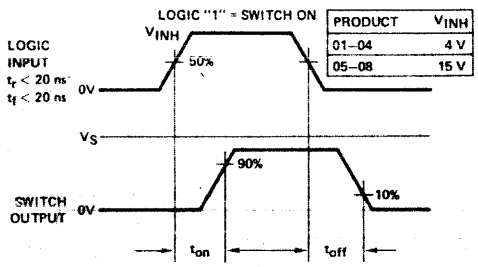


Case C

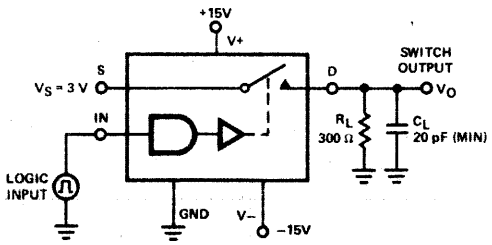


SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

Terminal Connections
Figure 1

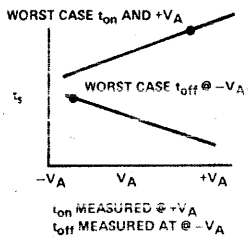


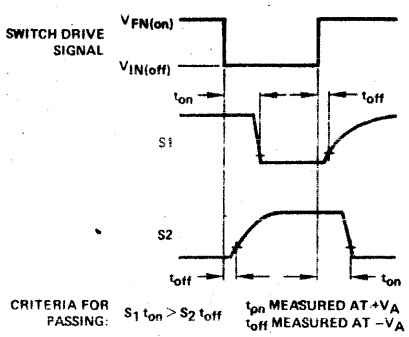
t_{on} AND t_{off} MEASURED AT THE SAME VOLTAGE LEVEL IN ORDER TO GET READINGS FOR THE SAME RESISTANCE.

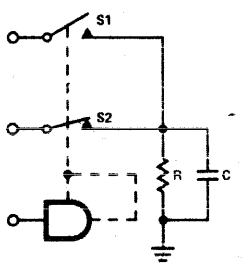


R & C ARE NOT SPECIFIED. C NOT REQUIRED, BUT INEVITABLE. TYPICAL USABLE R'S 300 Ω, 1K Ω.

t_{on} and t_{off} Measurement
Figure 2

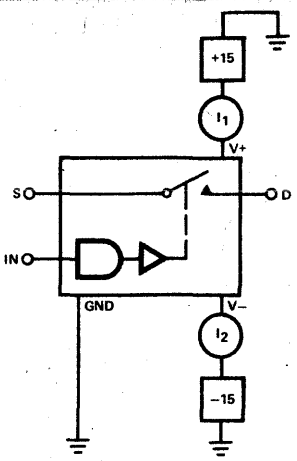




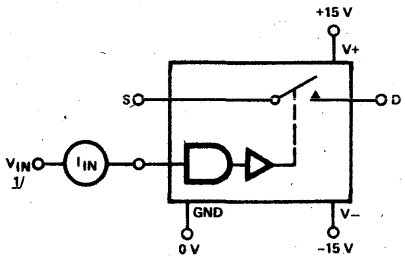


Break Before Make Measurements
Figure 3

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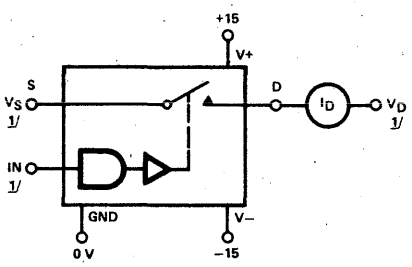


I_1, I_2 Test Circuit
Figure 4



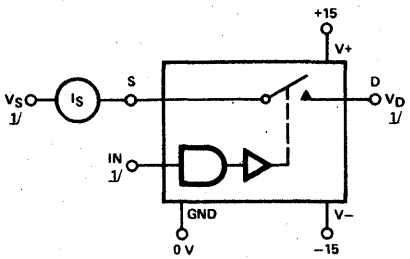
1/ V_{IN} = 0 V FOR I_{INL}
V_{IN} = +5 V AND +15 V FOR I_{INH}

I_{INL}, I_{INH} Test Circuit
Figure 5



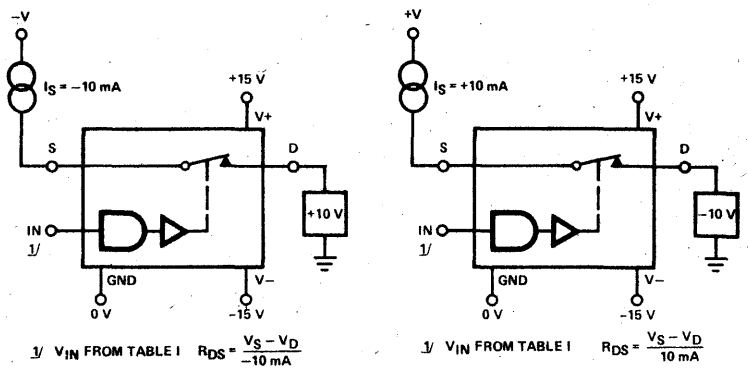
1/ TEST CONDITIONS ARE FROM TABLE I

$I_{D(off)}$, $I_{FD(off)}$ Test Circuit
Figure 6



1/ TEST CONDITIONS ARE FROM TABLE I

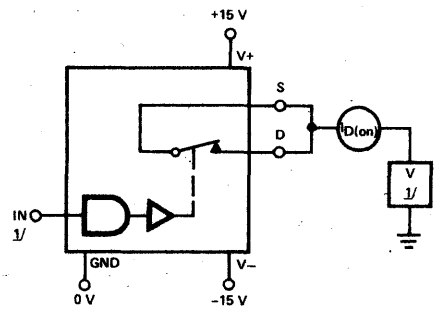
$I_{S(off)}$, $I_{FS(off)}$ Test Circuit
Figure 7



1/ V_{IN} FROM TABLE I $R_{DS} = \frac{V_S - V_D}{-10\text{ mA}}$

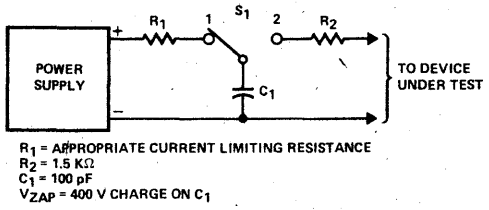
1/ V_{IN} FROM TABLE I $R_{DS} = \frac{V_S - V_D}{10\text{ mA}}$

R_{DS} Test Circuits
Figure 8



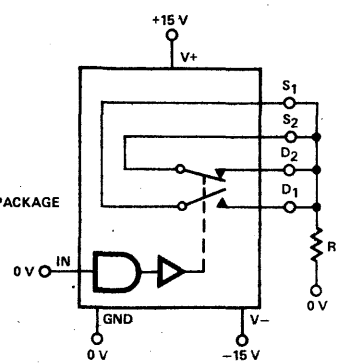
1/ CONDITIONS ARE FROM TABLE I

$I_{D(on)}$ Test Circuit
Figure 9



R_1 = APPROPRIATE CURRENT LIMITING RESISTANCE
R_2 = 1.5 KΩ
C_1 = 100 pF
V_{ZAP} = 400 V CHARGE ON C_1

High Voltage (V_{ZAP}) Test Circuits
Figure 10



NOTES:
1/ R = 10K Ω ±10%
2/ ONE RESISTOR PER PACKAGE

For all device types, burn-in configuration is as follows:
V_1 = +15 V
V_2 = –15 V
GND = 0 V
V_{IN} = 0 V
V_S = GND through 10K Ω
V_D = GND through 10K Ω

Burn-In Configuration (Device Type –02, –06 Shown)
Figure 11

Burn-In Bias Matrix

Case	Device Type/Pin #	1	2	3	4	5	6	7	8	9	10	11	12	13	14
C	01, 05	NC	1/	NC	1/	NC	0 V	0 V	−15	0 V	NC	1/	NC	1/	+15
D	01, 05	NC	1/	NC	1/	NC	0 V	0 V	−15	0 V	NC	1/	NC	1/	+15
I	01, 05	1/	1/	0 V	NC	0 V	−15	0 V	1/	1/	+15				
C	02, 06	NC	1/	NC	1/	NC	0 V	0 V	−15	NC	NC	1/	NC	1/	+15
D	02, 06	NC	1/	NC	1/	NC	0 V	0 V	−15	NC	NC	1/	NC	1/	+15
I	02, 06	1/	1/	0 V	NC	0 V	−15	NC	1/	1/	+15				
C	03, 07	NC	1/	1/	1/	1/	0 V	0 V	−15	0 V	1/	1/	1/	1/	+15
D	03, 07	NC	1/	1/	1/	1/	0 V	0 V	−15	0 V	1/	1/	1/	1/	+15
C	04, 08	NC	1/	1/	1/	1/	0 V	0 V	−15	0 V	1/	1/	1/	1/	+15
D	04, 08	NC	1/	1/	1/	1/	0 V	0 V	−15	0 V	1/	1/	1/	1/	+15

Notes: 1/ Connect to 0 V through 10K Ω
NC Not connected

Burn-In Configuration (Cont'd)
Figure 11

4.2 Qualification Inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified herein for groups A, B, C and D (see 4.4.1, 4.4.2 and 4.4.3). After qualification of one or more electrically and structurally similar types with a single lead finish, other lead finishes of the same case outline may be qualified by submitting a single type in the qualified case outline to the group B, subgroup 3 test and to the group D, subgroups 3 and 5 tests. Other case outlines with identical electrical characteristics and lead finishes may be qualified by submitting each case outline to all group D tests.

4.3 Screening. Screening shall be in accordance with Method 5004 of MIL-STD-883 and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

(a) Final electrical test [(3.1.14(b)) of Method 5004 of MIL-STD-883].
1. Subgroup 4 Testing is not applicable.

(b) Percent defective allowable (PDA) – The PDA is specified as 5 percent for class A devices and 10 percent for class B devices based on failures from group A, subgroup 1 test after cooldown as final electrical test in accordance with Method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

4.4 Quality Conformance Inspection. Quality conformance inspection shall be in accordance with MIL-M-38510.

4.4.1 Group A Inspection. Group A inspection shall consist of the test subgroups and LTPD values shown in Table I of Method 5005 of MIL-STD-883 and as follows:

(a) Subgroups 4, 5, 6, 10 and 11 are not applicable.

(b) Tests shall be as specified in Table III herein.

4.4.2 Group B Inspection. Group B inspection shall consist of the test subgroups and LTPD values shown in Table II of Method 5005 of MIL-STD-883 and as follows:

(a) End point electrical parameters shall be as specified in Table III herein.

(b) Steady state life requirement for group B, subgroup 5 testing of class A devices will be satisfied by testing to LTPD 5, $T_A = 125^{\circ}C$ and t = 1000 hours.

4.4.2.1. Subgroup 4 or 7. Subgroup 4 (for class B devices) or 7 (for class A devices) shall be added to the group B requirements, and shall consist of the test, conditions, and limits specified in 4.5.3. The LTPD shall be 15 for both subgroups.

4.4.3 Group C and D Inspection. Group C and D inspection shall consist of the test subgroups and LTPD values shown in Table III of Method 5005 of MIL-STD-883 and as follows:

(a) End point electrical parameters shall be as specified in Table III herein.

(b) Lead bend in only one direction is required for initial conditioning prior to moisture resistance and salt atmosphere tests.

4.5 Methods of Examination and Test. Methods of examination and test shall be as specified in the appropriate tables. Electrical test circuits as prescribed herein or in the referenced test methods of MIL-STD-883 shall be acceptable. Other test circuits shall require the approval of the qualifying activity.

4.5.1 Voltage and Current. All voltage values given are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Life Test Cooldown Procedure. When devices are measured at 25°C following application of the operating life or burn-in test condition, they shall be cooled to room temperature prior to removal of the bias, except that bias may be removed for up to one minute for the purpose of removing the devices from the oven.

4.5.3 High Voltage (V_{ZAP}) Test of Protection Circuits. Unless otherwise specified, one input and output terminal of the device under test (DUT) shall be subjected to a voltage pulse from a 100 pF source charged to 400 V (see Figure 10). The test shall be conducted in the following sequence:

(a) Measure I_{INL}, I_{INH} and $I_{D(off)}$ at one input and output terminal of the DUT at 25°C. Also measure I_1 and I_2 at 25°C. These measurements shall be made in accordance with Table III herein.

(b) With S_1 in position 1 charge C_1 to 400 V with S_1 in position 2. Apply the test voltage (V_{ZAP}) to the same terminal selected for leakage current measurements. Apply V_{ZAP} in a 4 pulse sequence as follows:

(1) Input (–) to V_1
(2) Input (+) to GND
(3) Drain (+) to V_2
(4) Drain (–) to V_1

(c) Within 24 hours repeat the I_1 and I_2 measurements and the I_{INL}, I_{INH} and $I_{D(off)}$ measurements on the same terminals as performed above. At this time a DUT exhibiting leakage currents in excess of the specified limits is defective.

4.6 Inspection of Preparation for Delivery. Inspection of preparation for delivery shall be in accordance with MIL-M-38510, except that the rough handling test shall not apply.

5. *PREPARATION FOR DELIVERY*

5.1 Preservation-Packaging and Packing. Microcircuits shall be prepared for delivery in accordance with MIL-M-38510.

6. *NOTES*

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended Use. Microcircuits conforming to this specification are intended for use for Government microcircuit applications (original equipment) and logistic purposes.

6.3 Ordering Data. The contract or order should specify the following:

(a) Complete part number (see 1.2).

(b) Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

(c) Requirement for certificate of compliance, if applicable.

(d) Requirements for notification of change of product or process to procuring activity in addition to notification to the qualifying activity, if applicable.

(e) Requirements for packaging and packing.

(f) Requirements for failure analysis (including required test condition of Method 5003), corrective action and reporting of results, if applicable.

(g) Requirements for product assurance options.

(h) Requirements for carriers, special lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

6.4 Abbreviations, symbols and definitions used herein are defined in MIL-STD-1313 and MIL-STD-1331 and as follows:

6.4.1 R_{DS}. The series ON resistance of each switch. $R_{DS} = |(V_D - V_S)/I_S|$.

6.4.2 $I_{D(off)}$, $IF_{D(off)}$. The leakage current into the drain terminal while the switch is off.

6.4.3 $I_{S(off)}$, $IF_{S(off)}$. The leakage current into the source terminals while the switch is off.

6.4.4 $I_{D(on)}$. The leakage current from the switch to the driver circuitry while the switch is on.

6.5 Logistic Support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits procured for Government logistic support will be procured to device class B (see 1.2.2), lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.6 Substitutability. Microcircuits covered by this specification are substitutable for the following commerical device types:

Device Type	Commercial Type	Device Type	Commercial Type
–01	DG300A	–05	DG304A
–02	DG301A	–06	DG305A
–03	DG302A	–07	DG306A
–04	DG303A	–08	DG307A

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MASTER SELECTION GUIDE

The Master Selection Guide is the most comprehensive directory of integrated circuitry available in the United States. It organizes them into categories — digital, interface, linear, memory and microprocessor. Within these categories it classifies the devices by type (i.e., CMOS, ECL, TTC, etc.) and by function (counters, gates, flip-flops, etc.). Furthermore, the guide includes detailed data provided by the manufacturers for those products which they have chosen as particularly important.

how to use the master selection guide

This guide provides sufficient information to make initial product selections, to lead you to a group of device numbers and manufacturers' names. It enables you to find the products which are most apt to fulfill your major requirements and then provides data to help you make your final choice. All devices that appear in this selection, both in the initial selection guide and in the data pages, are included in the Part Number and Product Indexes. These index listings lead to the page and the line on that page where each device appears. Users of the 1977 IC Master will find several new features in the 1978 selection guide. These include an alphabetized topic index which starts on the next page. The coverage of industrial and consumer circuits has been greatly expanded; the guide now identifies these products by model number and covers digital, linear and digital-linear combinations under one heading, Linear & Consumer Circuits. The TTL major families, TTL, TTL-LS, TTL-H and TTL-S have been combined under one heading to facilitate function comparisons. And the Microprocessor section has been enlarged, grouping microprocessor system components together by processor type and adding many new system descriptions.

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Function	Section
A	
AC Detector	Linear—Other Devices
Active Filter	Linear—Other Devices
Active Terminator	Digital—ECL 10000, Miscellaneous
Adders	Digital—CMOS, Arithmetic Functions
	Digital—ECL 10000, Arithmetic Functions
	Digital—TTL, Arithmetic Functions
	Digital—Special
Address Latch Element	Microprocessors—System Components
Address Register	Microprocessors—System Components
Address Selector	Linear—Telecommunication Circuits
Alarm Circuits	Linear—Other Devices
Amplifier/Detector FM IF	Linear—Consumer Circuits
Amplifiers	
AC	Linear—Other Devices
	Linear—Special Purpose
AGC/Squelch	Linear—Amplifiers, Special Purpose
	Linear—Consumer Circuits
AM/FM IF	Linear—Consumer Circuits
AM/FM IF and AF	Linear—Consumer Circuits
Audio, Power	Linear—Consumer Circuits
Current	Linear—Amplifiers, Special Purpose
Differential/Cascade	Linear—Amplifiers, Special Purpose
Differential Input/Output	Linear—Amplifiers, Special Purpose
Followers	Linear—Followers
Hearing Aid	Linear—Consumer Circuits
Instrumentation	Linear—Amplifiers, Special Purpose
	Linear—Operational Amplifier Characteristics
Isolation	Linear—Amplifiers, Special Purpose
Limiting	Linear—Amplifiers, Special Purpose
Linear/Antilog	Linear—Amplifiers, Special Purpose
Log/Antilog	Linear—Amplifiers, Special Purpose
Microphone	Linear—Amplifiers, Special Purpose
Mixer/RF	Linear—Consumer Circuits
Operational	Linear—Operational Amplifier Characteristics
	Linear—Operational Amplifiers, General Purpose
	Linear—Operational Amplifiers, High Output Current
	Linear—Operational Amplifiers, High Voltage
	Linear—Operational Amplifiers, Low Bias Current
	Linear—Operational Amplifiers, Low Drift
	Linear—Operational Amplifiers, Programmable
	Linear—Operational Amplifiers, Single Supply
	Linear—Operational Amplifiers, Wide Band
Preamplifier	Linear—Amplifiers, Special Purpose
	Linear—Consumer Circuits
RF	Linear—Amplifiers, Special Purpose
RF Detector/Video	Linear—Consumer Circuits
Sense	Interface—Sense Amplifiers
Single Ended Input/Output	Linear—Amplifiers, Special Purpose
Tone	Linear—Consumer Circuits
Transconductance	Linear—Amplifiers, Special Purpose
Video, IF and RF	Linear—Amplifiers, Special Purpose
Voltage Controlled	Linear—Amplifiers, Special Purpose
Wideband	Linear—Amplifiers, Special Purpose
Analog Input	Microprocessors—System Components
Analog Output	Microprocessors—System Components
Analog Memories	Linear—Other Devices
Analog Shift Registers	Linear—Other Devices
Analog Switches	Interface—Analog Switches
Arithmetic Logic Element	Digital—TTL, Arithmetic Functions
Arithmetic Logic Register Stack	Digital—CMOS, Arithmetic Functions
	Microprocessors—System Components
Arithmetic Logic Unit	Microprocessors—System Components
	Digital—CMOS, Arithmetic Functions
	Digital—ECL 10000, Arithmetic Functions
	Digital—ECL 100K, Arithmetic Functions
	Digital—TTL, Arithmetic Functions
Arrays	
Bipolar	Linear—Arrays
CMOS	Linear—Arrays, Special Arrays
Custom	Digital—ECL 100K, Miscellaneous
	Digital—Special
	Linear—Other Devices
Thyristor/Transistor	Linear—Arrays, Special Arrays
Transistor	Linear—Arrays, Transistor Arrays
Transistor/Diode	Linear—Arrays, Special Arrays
Asynchronous Communication Controller	Microprocessors—System Components
Audio Noise Reduction Dolby	Linear—Consumer Circuits
B	
Bandpass Filters	Linear—Telecommunication Circuits
Baseband Channel Amplifier	Linear—Telecommunication Circuits
Baud Rate Generator	Digital—Special
	Interface—Serial Transmitters, Receivers
Bidirectional Bus Driver	Microprocessor—System Components
Bidirectional Port	Microprocessor—System Components
Bidirectional Transceiver	Interface—Line Circuits, Line Transceivers
	Microprocessor—System Components
Bit Programmable I/O	Microprocessor—System Components
Bit Rate Generator	Digital—CMOS, Miscellaneous
	Interface—Transmitters-Receivers
	Microprocessor—System Components
Branch Control Unit	Microprocessor—System Components
Bucket Brigade Device	Linear—Other Circuits
Buffers	Digital—CMOS, Buffers/Inverters
	Digital—ECL 10000, Buffers
	Digital—HNIL/HTL, Buffers/Inverters
	Digital—TTL, Buffers/Inverters
	Digital—TTL, Drivers
	Microprocessor—System Components
Bus Interface Circuits	Interface—Line Circuits
	Microprocessor—System Components

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Function	Section
BOART (Bus Oriented ART)	Interface—Transmitters-Receivers
Bus Receiver	Digital—ECL 10000, Miscellaneous
	Interface—Line Circuits
Bus Switch	Digital—TTL, Miscellaneous
Bus Transceiver	Digital—ECL 10000, Miscellaneous
	Digital—TTL, Miscellaneous
	Interface—Line Circuits
	Microprocessor—System Components
Bus Translator	Microprocessor—System Components
C	
Calculator Circuits	Linear—Consumer Circuits
Calculator, Display Interface	Linear—Consumer Circuits
Calculator, Keyboard Entry Sequence Memory	Linear—Consumer Circuits
Calculator, Printing	Linear—Consumer Circuits
Camera Exposure Control	Linear—Consumer Circuits
Camera, Strobe Light Control	Linear—Consumer Circuits
Cassette Controller	Microprocessor—System Components
CB Circuits	Linear—Consumer Circuits
	Linear—Phase Locked Loop Circuits
CCD Memories	Memories—RAMs, CCD Memories
Central Processing Unit	Microprocessor—System Components
Character Generators	Memory—Character Generators
Clock	Digital—CMOS, Oscillators/Dividers
	Linear—Consumer Circuits
Clock Buffer	Interface—Memory and Peripheral Drivers
	Microprocessor—System Components
Clock Generator	Microprocessor—System Components
Code Converters	Memory—Code Converters
Coin Box Circuits	Linear—Telecommunication Circuits
Compander	Linear—Telecommunication Circuits
Comparators, Digital	Digital—CMOS, Arithmetic Functions
	Digital—ECL 10000, Arithmetic Functions
	Digital—ECL III, Arithmetic Functions
	Digital—HNIL/HTL, Arithmetic Functions
	Digital—TTL, Arithmetic Functions
Comparators, Linear	Linear—Comparators, Single Comparators
	Linear—Comparators, Dual Comparators
	Linear—Comparators, Quad Comparators
	Linear—Phase Locked Loop Circuits
Compressor (Compander)	Linear—Telecommunication Circuits
Contact Bounce Eliminator	Digital—CMOS, Miscellaneous
	Digital—TTL, Miscellaneous
Control Element	Microprocessors—System Components
Control ROM	Microprocessors—System Components
Control Sequencer	Microprocessors—System Components
Converters	
Analog to Digital	Interface—Analog to Digital Converters, Binary Output
	Interface—Analog to Digital Converters, Decimal Output
	Linear—Other Devices
BCD to Binary	Digital—TTL, Miscellaneous
Binary to Phone Pulse	Digital—CMOS, Miscellaneous
Digital to Analog	Interface—Digital to Analog Converters
Frequency to Voltage	Linear—Other Devices
Serial to Parallel	Digital—Special
Voltage to Frequency	Linear—Other Devices
Correlation	Digital—Special
	Linear—Other Devices
Counters	Digital—CMOS, Counters
	Digital—ECL III, Counters
	Digital—HNIL/HTL, Counters
	Digital—TTL, Counters
	Digital—Special
Binary	Digital—CMOS, Counters, Binary
	Digital—ECL 10000, Counters, Binary
	Digital—ECL 95000, Counters
	Digital—ECL III, Counters
	Digital—HNIL/HTL, Counters
	Digital—TTL, Binary Counters Up
	Digital—TTL, Binary Counteds Up/Down
	Digital—Special
Decade	Digital—CMOS, Counters, Decade
	Digital—ECL 10000, Counters, Decade
	Digital—ECL 95000, Counters
	Digital—ECL III, Counters
	Digital—HNIL/HTL, Counters
	Digital—TTL, Decade Counters Up
	Digital—TTL, Decade Counters Up/Down
	Digital—TTL, Miscellaneous
	Digital—Special
Counter Time Base	Digital—Special
Counting Register	Digital—ECL 100K, Counters
CRC Generator/ Checker	Interface—Error Checking Circuits
	Microprocessor—System Components
CRT Controller	Microprocessor—System Components
CRT Video Timer Controller	Microprocessor—System Components
Crosspoint Array	Linear—Telecommunications Circuits
D	
Data Access Register	Digital—CMOS, Arithmetic Functions
	Microprocessor—System Components
Data Acquisition System	Linear—Other Devices
Data Encryption	Digital—TTL, Miscellaneous
Data Path Switch	Digital—CMOS, Arithmetic Functions
	Linear—Analog Switches
	Microprocessor—System Components
Data Selector/ Multiplexer	Linear—Analog Switches Multiplexers
	Microprocessor—System Components
Decoders	Digital—CMOS, Decoders
	Digital—ECL 10000, Decoders
	Digital—ECL 100K, Decoders
	Digital—TTL, Decoders
	Digital—CMOS, Drivers
	Digital—Special
	Interface—Display Drivers
	Microprocessor—System Components
FM Stereo	Linear—Consumer Circuits
Keyboard	Interface—Keyboard Encoders, Decoders
Tone	Linear—Phase Locked Loop Circuits
	Linear—Telecommunication Circuits
Delta Modulation System	Linear—Telecommunication Circuits
Deskew FIFO	Memory—FIFO
	Microprocessors—General Purpose

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Function	Section
Dialer Circuits	Linear—Telecommunication Circuits
Digital Filter Switch	Linear—Telecommunication Circuits
Digital Mixer	Linear—Phase Locked Loop Circuits
Digital to Analog Converters	Interface—Digital to Analog Converters
Diode Matrix, Programmable	Digital—Special
Direct Memory Access	Microprocessor—System Components
Disk Memory Drivers	
Fault Detector	Interface—Memory and Peripheral Drivers
Head Selector	Interface—Memory and Peripheral Drivers
Video Amplifier	Interface—Memory and Peripheral Drivers
Display Controller	Microprocessor—System Components
Display Drivers	Interface—Display Drivers
Dividers	Digital—Special
	Digital—CMOS, Oscillators/Dividers
	Digital—TTL, Miscellaneous
	Linear—Phase Locked Loop Circuits
	Linear—Other Devices
DMA Controller	Microprocessor—System Components
Double Balanced Mixer	Linear—Phase Locked Loop Circuits
DPDT Switches	Interface—Analog Switches
DPST Switches	Interface—Analog Switches
Drivers	Digital—CMOS, Drivers
	Digital—CMOS, Miscellaneous
	Digital—ECL 10000, Drivers
	Digital—ECL 100K, Drivers
	Digital—HNIL/HTL, Drivers
	Digital—TTL, Decoders
	Digital—TTL, Drivers
	Digital—TTL, Miscellaneous
	Interface—Display Drivers
	Interface—Line Circuits
	Interface—Memory and Peripheral Drivers
Audio	Linear—Consumer Circuits
Counter Display	Digital—Special
DVMs	Digital—Special
	Interface—Analog to Digital Converters, Decimal Output
Dynamic Memory Interface	Interface—Memory and Perpheral Drivers
	Microprocessor—System Components
Dynamic Memory Refresh Controller	Interface—Memory and Peripheral Drivers
	Microprocessor—System Components

E

Encoders	Digital—CMOS, Miscellaneous
	Digital—ECL 10000, Miscellaneous
	Digital—ECL 100K, Miscellaneous
	Digital—TTL, Miscellaneous
	Digital—Special
Keyboard	Interface—Keyboard Encoder-Decoders
Error Checking Circuits	Interface—Error Checking Circuits
Expander (Compander)	Digital—TTL, Miscellaneous
	Linear—Telecommunication Circuits

F

Field Programmable Logic Array	Memory—PLAs
	Microprocessor—System Components
First In First Out Memory	Memory—FIFO
	Microprocessor—System Components
Flasher	Linear—Other Devices
Flip-Flops	Digital—CMOS, Flip-Flops
	Digital—ECL 10000, Flip-Flops
	Digital—ECL 95000, Flip-Flops
	Digital—ECL 100K, Flip-Flops
	Digital—ECL III, Flip-Flops
	Digital—HNIL/HTL, Flip-Flops
	Digital—TTL, Flip-Flops
	Digital—Special
Floating Point Arithmetic	Microprocessor—System Components
Floppy Disc Controller	Microprocessor—System Components
FM Muting/Tuning Point System	Linear—Consumer Circuits
FM RF/IF Amplifier	Linear—Consumer Circuits
Followers	Linear—Followers
Four Channel Sound	Linear—Consumer Circuits
Frequency Sensitive Switch	Linear—Telecommunication Circuits
Frequency to Voltage Converter	Linear—Other Devices
FSK Modulator/ Demodulator	Linear—Phase Locked Loop Circuits
Function Generator	Linear—Phase Locked Loop Circuits
	Linear—Other Devices

G

Games, T.V.	Linear—Consumer Circuits
Gates	Digital—CMOS, Gates, Miscellaneous
	Digital—HNIL/HTL, Gates, Miscellaneous
	Digital—TTL, Gates, Miscellaneous
AND/NAND	Digital—CMOS, Gates, AND/NAND
	Digital—ECL 10000, Gates, AND/NAND
	Digital—HNIL/HTL, Gates, AND/NAND
	Digital—TTL, Gates, AND/NAND
AND-OR/AND-OR Invert	Digital—CMOS, Gates, AND-OR/ AND-OR Invert
	Digital—ECL 10000, Gates, AND-OR/ AND-OR Invert
	Digital—ECL 100K, Gates, AND-OR/ AND-OR Invert
	Digital—HNIL/HTL, Gates, AND-OR/ AND-OR Invert
	Digital—TTL, Gates, AND-OR/ AND-OR Invert
Complex Gate w/ Persistance Detector	Digital—Special
Exclusive OR/NOR	Digital—CMOS, Gates, Exclusive OR/NOR
	Digital—ECL 10000, Gates, Exclusive OR/NOR
	Digital—ECL 100K, Gates, Exclusive OR/NOR
	Digital—ECL III, Gates, Exclusive OR/NOR
	Digital—HNIL/HTL, Gates, Exclusive OR/NOR
	Digital—TTL, Gates, Exclusive OR/NOR
Majority Logic	Digital—CMOS, Gates, Miscellaneous
	Digital—TTL, Gates, Miscellaneous

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Function	Section
OR/NOR	Digital—CMOS, Gates, OR/NOR
	Digital—ECL 10000, Gates, OR/NOR
	Digital—ECL 95000, Gates, OR/NOR
	Digital—ECL 100K, Gates, OR/NOR
	Digital—ECL III, Gates, OR/NOR
	Digital—TTL, Gates, OR/NOR
	Digital—Special
Gate Expander	Digital—HNIL/HTL, Gates, Miscellaneous
General Interface Circuit	Microprocessor—System Components
General Purpose Input/Output	Microprocessor—System Components
Ground Fault Interrupter	Linear—Consumer Circuits
H	
Hall Effect Devices	Digital—Special
	Linear—Other Devices
Hamming Code Detector and Generator	Digital—TTL, Miscellaneous
	Interface—Error Checking Circuits
I	
Identity Comparator	Digital—TTL, Arithmetic Functions
Image Sensor	Linear—Other Devices
Input/Output Control Unit	Microprocessor—System Components
Interface Latch Element	Microprocessor—System Components
Interrupt Control Unit	Microprocessor—System Components
Interrupter, Ground Fault	Linear—Consumer Circuits
Interval Timer	Linear—Timers
	Microprocessor—System Components
Inverters	Digital—CMOS, Buffers/Inverters
	Digital—HNIL/HTL, Buffers/Inverters
	Digital—HNIL/HTL, Gates, Miscellaneous
	Digital—TTL, Buffers/Inverters
	Digital—Special
K	
Keyboard/Display Controller	Microprocessor—System Components
Keyboard Encoders	Interface—Keyboard Encoders, Decoders
L	
Last In First Out Memory	Memory—LIFOs
Latches	Digital—CMOS, Latches
	Digital—ECL 10000, Latches
	Digital—ECL 95000, Latches
	Digital—ECL 100K, Latches
	Digital—ECL III, Latches
	Digital—HNIL/HTL, Latches
	Digital—TTL, Latches
	Microprocessor—System Components
Level Detector	Linear—Other Devices
Level Meter	Linear—Other Devices
Light Activated Switch	Linear—Other Devices
Light to Current Converter	Linear—Other Devices
Light Detector	Linear—Other Devices
Line Drivers	Interface—Line Circuits, Single Ended
	Interface—Line Circuits, Differential
Line Receivers	Digital—ECL 10000, Miscellaneous
	Digital—ECL 100K, Miscellaneous
	Digital—ECL III, Miscellaneous
	Interface—Line Circuits, Single Ended
	Interface—Line Circuits, Differential
Line Transceiver	Interface—Line Circuits, Transceivers
Logic Processor	Microprocessor—System Components
Look Ahead Carry Generator	Digital—CMOS, Arithmetic Functions
	Digital—ECL 10000, Arithmetic Functions
	Digital—TTL, Arithmetic Functions
	Microprocessor—System Components
Loop Disconnect Dialer	Linear—Telecommunication Circuits
Low Battery Indicator	Linear—Other Devices
M	
Memories	
Active Element	Digital—TTL, Memories
CAM	Digital—CMOS, Memories
	Digital—TTL, Memories
Character Generators	Memory—Character Generators
Code Converters	Memory—Code Converters
FIFO	Digital—CMOS, Memories
	Digital—TTL, Memories
	Memory—FIFO
LIFO	Digital—CMOS, Memories
	Memory—LIFO
PLA	Memory—PLAs
PROM	Digital—ECL 10000, Memories
	Memory—PROMs
	Microprocessor—System Components
RAM	Digital—CMOS, Memories
	Digital—ECL 10000, Memories
	Digital—ECL 95000, Memories
	Digital—ECL 100K, Memories
	Digital—TTL, Memories
	Memory—RAMs, Bubble Memories
	Memory—RAMs, Dynamic
	Memory—RAMs, CCD Memories
	Memory—RAMs, Static
	Microprocessor—System Components
ROM	Digital—CMOS, Memories
	Memory—EAROMs
	Memory—ROMs, Static
	Memory—ROMs, Dynamic
	Microprocessor—System Components
Memory Address Driver	Microprocessor—System Components
Memory Control Unit	Microprocessor—System Components
Memory Drivers	Interface—Memory and Peripheral Drivers
Memory Interface	Interface—Memory and Peripheral Drivers
	Microprocessor—System Components
Memory Refresh Logic Circuits	Digital—TTL, Miscellaneous
	Interface—Memory and Peripheral Drivers
Micro Address Generator	Digital—TTL, Miscellaneous
MICROM	Microprocessor—System Components
Micro Computer	Microprocessor—System Components
Micro Controller	Digital—TTL, Arithmetic Functions
	Microprocessor—System Components

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Function	Section
Microprocessor	Digital—TTL, Arithmetic Functions
	Microprocessor—Selection Tables
	Microprocessor—System Components
Microprocessor Development System	Microprocessor—System Components
Microprogram Control Unit	Microprocessor—System Components
Microprogram Sequencer	Digital—TTL, Miscellaneous
	Microprocessor—System Components
Mixer	Linear—Amplifiers, Special
Modem	Digital—CMOS, Miscellaneous
	Linear—Telecommunication Circuits
	Linear—Other Devices
	Microprocessor—System Components
Modulator	Linear—Other Devices
	Linear—Consumer Circuits
Motor Load Control	Linear—Other Devices
Motor Speed Regulator	Linear—Other Devices
Multiplexers	
Analog	Interface—Analog Switches, Multiplexers
Digital	Digital—CMOS, Multiplexers
	Digital—ECL 10000, Multiplexers
	Digital—ECL 100K, Multiplexers
	Digital—HNIL/HTL, Multiplexers
	Digital—TTL, Multiplexers
	Digital—Special
Multipliers	Digital—ECL 10000, Arithmetic Functions
	Digital—TTL, Arithmetic Functions
	Microprocessor—System Components
	Linear—Other Devices
Binary	Digital—CMOS, Arithmetic Functions
Binary Rate	Digital—CMOS, Miscellaneous
	Digital—TTL, Miscellaneous
Decade Rate	Digital—TTL, Miscellaneous
Multipliers/Dividers	Linear—Other Devices
	Microprocessor—System Components
Multi-Protocol Communications Controller	Microprocessor—System Components
Multivibrators	Digital—CMOS, Multivibrators
	Digital—ECL III, Multivibrators
	Digital—HNIL/HTL, Multivibrators
	Diital—TTL, Multivibrators
	Digital—Special
Monostable/ Astable	Digital—CMOS, Multivibrators
	Digital—ECL 10000, Multivibrators
	Digital—ECL 100K, Multivibrators
	Digital—HNIL/HTL, Multivibrators
	Digital—TTL, Multivibrators
Music Circuits	Linear—Consumer, Organ Circuits

N

Nines Complementer	Digital—CMOS, Arithmetic Functions

O

Organ Circuits	Linear—Consumer Circuits
Oscillators	Digital—CMOS, Oscillators/Dividers
	Linear—Phase Locked Loop Circuits
Overvoltage Protectors	Linear—Other Devices

Function	Section

P

Parallel Data Controller	Microprocessor—System Components
Parallel Interface Element	Microprocessor—System Components
Parity Generator	Digital—CMOS, Miscellaneous
	Digital—ECL 10000, Miscellaneous
	Digital—ECL 100K, Miscellaneous
	Digital—TTL, Miscellaneous
	Interface—Error Checking Circuits
Parity Tree	Digital—CMOS, Miscellaneous
	Digital—TTL, Miscellaneous
Peripheral Drivers	Interface—Memory and Peripheral Drivers
Peripheral Input/Output	Microprocessor—System Components
Peripheral Interface Adapter	Microprocessor—System Components
Phase Comparator	Digital—CMOS, Miscellaneous
	Interface—Phase Locked Loop Circuits
Phase Frequency Detector	Digital—TTL, Miscellaneous
	Linear—Phase Locked Loop Circuits
Phase Locked Loop Circuits	Digital—CMOS, Miscellaneous
	Linear—Phase Locked Loop Circuits
Stereo Decoders	Linear—Consumer Circuits
Phase Sensitive Demodulator	Linear—Other Devices
Phase Shifter	Linear—Other Devices
Plasma Display Controller	Interface—Display Drivers
	Microprocessor—System Components
Polynomial Generator	Digital—TTL, Miscellaneous
	Interface—Error Checking Circuits
Preamplifier	Linear—Amplifiers, Special
Audio	Linear—Consumer Circuits
Prescalers	Digital—Special
	Linear—Phase Locked Loop Circuits
Pressure Transducer	Linear—Other Devices
Printer Controller	Interface—Memory and Peripheral Drivers
	Microprocessor—System Components
Printer Driver	Interface—Memory and Peripheral Drivers
Printer Interface	Microprocessor—System Components
Priority Encoder	Digital—CMOS, Miscellaneous
Priority Interrupt	Microprocessor—System Components
Processing and Control Element	Microprocessor—System Components
Programmable CRT Controller	Microprocessor—System Components
Programmable General Purpose I/O	Microprocessor—System Components
Programmable Interface Controller	Microprocessor—System Components
Programmable Keyboard/ Display Device	Interface—Keyboard Encoders
	Microprocessor—System Components
Programmable Logic Arrays	Digital—CMOS, Miscellaneous
	Digital—TTL, Miscellaneous
	Memory—PLAs

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Function	Section
Programmable Systems Interface	Microprocessor—System Components
Program Memory	Microprocessor—System Components
Program Stack	Microprocessor—System Components
Program Storage Unit	Microprocessor—System Components
PROMs	Memory—PROMs
	Microprocessor—System Components
Protocol Controllers	Microprocessor—System Components
Pulse Stretcher	Digital—HNIL/HTL, Miscellaneous
Pulse Width to Voltage Converter	Linear—Other Devices
Q	
Quad Power Strobe	Digital—TTL, Miscellaneous
R	
Radio Transmitter	Linear—Other Devices
RAM Interface	Interface—Memory and Peripheral Interface
	Microprocessor—System Components
RAMs	Memory—RAMs
	Microprocessor—System Components
RAM and I/O	Microprocessor—System Components
Read Amplifier/ Preamplifier	Linear—Amplifiers, Special Purpose
Receiver AM	Linear—Consumer Circuits
Receiver AM/FM	Linear—Consumer Circuits
Register File	Digital—TTL, Memories
Regulator, Motor Speed	Linear—Consumer Circuits
Regulator, Switching	Linear—Voltage Regulators, Switching
Regulator, Voltage	Linear—Voltage Regulators
Relay Driver	Linear—Consumer Circuits
Remote Control Circuits	Linear—Consumer Circuits, T.V. Remote Control
Resolver Systems	Linear—Other Devices
RMS Converter	Linear—Other Devices
ROMs	Memory—ROMs
	Microprocessor—System Components
S	
Sample and Hold Circuits	Linear—Other Devices
SDLC Protocol Controller	Microprocessor—System Components
Sense Amplifiers	Interface—Sense Amplifiers
Sequence Controller	Microprocessor—System Components
Serial Receiver	Interface—Serial Transmitters-Receivers
Serial Transmitter	Interface—Serial Transmitters-Receivers
Serial Data Controller	Microprocessor—System Components
Servo Driver	Linear—Consumer Circuits
Shift Registers	Digital—CMOS, Shift Registers
	Digital—ECL 10000, Shift Registers
	Digital—ECL 95000, Shift Registers
	Digital—ECL 100K, Shift Registers
	Digital—ECL III, Shift Registers
	Digital—HNIL/HTL, Shift Registers
	Digital—TTL, Shift Registers
	Digital—Special
	Memory—Shift Registers, Dynamic
	Memory—Shift Registers, Static
Analog	Linear—Other Devices
Schmitt Trigger	Digital—CMOS, Miscellaneous
	Digital—HNIL/HTL, Miscellaneous
	Digital—TTL, Miscellaneous
	Digital—Special
Sine Wave Generator	Linear—Other Devices
Smoke Detector	Linear—Consumer Circuits
Sonar Transceiver	Linear—Consumer Circuits
	Linear—Other Devices
Speedometer Circuit	Linear—Consumer Circuits
SPDT Switches	Interface—Analog Switches
SPST Switches	Interface—Analog Switches
SSB Detector	Linear—Consumer Circuits
Static Memory Interface	Microprocessor—System Components
Successive Approximation Register	Digital—CMOS, Miscellaneous
	Digital—TTL, Miscellaneous
Switches	Linear—Consumer Circuits
Analog	Interface—Analog Switches, Drivers
Crosspoint	Interface—Analog Switches, Multiplexers
Drivers	Interface—Analog Switches, Drivers
Frequency	Linear—Other Circuits
Touch Sensing	Linear—Consumer Circuits
Synchronous Communications Controller	Microprocessor—System Components
Synchronous Data Link Controller	Interface—Transmitters-Receivers
Synchronous Receiver/ Transmitter	Interface—Transmitters-Receivers
Synchronous Serial Data Adapter	Microprocessor—System Components
Synthesizer	Linear—Phase Locked Loop Circuits
System Controller and Bus Driver	Microprocessor—System Components
T	
Tachometer	Linear—Consumer Circuits
Tele-communications Data Interface	Microprocessor—System Components
Telephone Circuits	Linear—Telecommunication Circuits
Temperature Transducers	Linear—Other Devices
Thermal Printhead Driver	Interface—Memory and Peripheral Drivers
Threshold Switch	Linear—Other Devices
Timers	Digital—CMOS, Miscellaneous
	Linear—Consumer Circuits
	Linear—Timers
	Microprocessor—System Components
Timing Function	Microprocessor—System Components
Tone Decoder	Linear—Phase Locked Loop Circuits
Tone Operated Switch	Linear—Telecommunication Circuits
Tone Receiver	Linear—Telecommunication Circuits
Tone Ringer	Linear—Telecommunication Circuits
Tone Transmitter	Linear—Telecommunication Circuits

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Function	Section
Translators	Digital—CMOS, Translators
	Digital—ECL 10000, Translators
	Digital—ECL 95000, Translators
	Digital—HNIL/HTL, Translators
	Digital—TTL, Translators
	Microprocessor—System Components
Transmitter	Linear—Consumer Circuits
Transversal Filters	Linear—Other Devices
Tuner Control, AM/FM	Linear—Consumer Circuits
Two Modulus Prescaler	Linear—Phase Locked Loop Circuits
T.V. Circuits	Linear—Consumer Circuits

U

Universal Communications Interface	Interface—Serial Transmitters-Receivers
Universal Peripheral Interface	Microprocessor—System Components
UART	Interface—Serial Transmitters-Receivers
USART	Interface—Serial Transmitters-Receivers
USYNRT	Interface—Serial Transmitters-Receivers

V

Video Display Controller	Microprocessor—System Components
Video Tape Recorder	Linear—Consumer Circuits
Voltage Controlled Oscillators	Digital—ECL III, Miscellaneous
	Digital—TTL, Miscellaneous
	Linear—Consumer Circuits
	Linear—Phase Lock Loop Circuits
Voltage Controlled Transient Generator	Linear—Consumer Circuits
Voltage Detector	Linear—Other Devices
Voltage Reference Source	Linear—Other Devices
Voltage Regulators	Linear—Voltage Regulators, Fixed Positive
	Fixed Negative
	Fixed Dual
	Adjustable Positive
	Adjustable Negative
	Adjustable Dual
	Switching
Automotive	Linear—Consumer Circuits

W/Z

Watch Circuits	Digital—CMOS, Oscillators/Dividers
	Linear—Consumer Circuits
Zero Voltage and Zero Crossing Triggers	Linear—Other Devices

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ABBREVIATIONS OF COMPANY NAMES

AD	Analog Devices
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Analogic	Analogic Corp.
Beckman	Beckman Instruments, Helipot Division
Burr-Brown	Burr-Brown Research
Cermetek	Cermetek
CMA	Consumer Microcircuits of America
Cybernetic	Cybernetic Micro Systems
Data General	Data General
Datel	Datel Systems
DDC	Data Devices Corp.
Delco	Delco Electronics
EA	Electronic Arrays
EMM/Semi	EMM Semi, Div. of Electronic Memories & Magnetics
Essex	Essex International
Exar	Exar Integrated Systems
Fairchild	Fairchild
Ferranti	Ferranti Electric
Fujitsu	Fujitsu
GI	General Instrument
Harris	Harris Semiconductor
Hitachi	Hitachi America Ltd.
Hughes	Hughes Aircraft Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
IMI	International Microcircuits, Inc.
Intech/FMI	Intech/Function Modules Inc.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
IPI	Integrated Photomatrix, Inc.
ITT	ITT Semiconductors
Lambda	Lambda Electronics
LSI	LSI Computer Systems
Master Logic	Master Logic
Micro Comp	Micro Components
Micro Net	Micro Networks
Micropac	Micropac Industries
Micro Power	Micro Power Systems
Micro Tech	Microcircuits Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electric Co.
MMI	Monolithic Memories, Inc.
MOS	MOS Technology
Mostek	Mostek
Motorola	Motorola Semiconductor
National	National Semiconductor
NCR	NCR Corp., Microelectronics Division
NEC	NEC America
NEC	NEC Microcomputers
Nippon	Nippon Electric Co.
Nitron	Nitron
Nortec	Nortec Electronics
Novonics	Novonics
OEI	Optical Electronics, Inc.
Panasonic	Panasonic, Matsushita Electric Corp.
Photo Therm	Photo Therm
Plessey	Plessey Semiconductors
PMI	Precision Monolithics, Inc.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell Microelectronic Division
RTC	Real Time Corp.
Sanken	Sanken Electric
Sanyo	Sanyo Electric
SGS	SGS-Ates Semiconductor
Siemens	Siemens
Signetics	Signetics (Philips)
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys.	Silicon Systems, Inc.
Silitronics	Silitronics
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSM	Solid State Music
SSS	Solid State Scientific
Synertek	Synertek
Tektronix	Tektronix
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	AEG-Telefunken
TI	Texas Instruments
TMX	TMX
Toshiba	Toshiba
Trans-Data	Trans-Data
TRW	TRW
Western	Western Digital
Zilog	Zilog

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INTRODUCTION TO DIGITAL

The Master Selection Guide provides sufficient information to make initial product selections, to lead you to a group of device numbers and manufacturers' names. It enables you to find the products which are most appropriate to fulfill your major requirements and then provides data for many of the more important products.

All devices that appear in this section, both in the initial selection guide and in the data pages, are included in the Part Number and Product Indexes. These index listings lead to the page and the line on that page where each device appears.

The first two pages of the digital section present comparisons of the performance of the major digital families to help you choose between families. These are followed by lists of the devices in each family arranged into functional groups (arithmetic, buffers/inverters, etc.). Within each group you can readily determine all of the various circuits available, surveying the entire IC industry so that you know all your options. The initial selection lists are followed by the device data pages which have been provided for you by the manufacturers. When such data is in the book, the page numbers are given with the initial selection listings.

Some digital circuits — calculator, watch chips, and electronic organ circuits — are not included in this section, but they are covered in detail in the Linear-Consumer section. Digital circuits which do not fall into one of the major logic families are listed at the end of the selection information under the heading Digital-Other Devices.

This section is not complicated by reference to package styles; the package style suffixes are usually deleted. For more information on each companies' suffixes, see the Part Number Guide. Throughout the Master Selection Guide, each full military temperature range (−55°C to 125°C) device is indicated by a dagger (†) before the manufacturer's name. Manufacturers' names are normally spelled out; however, a few are abbreviated and the abbreviations are explained on page 176.

Page Number Index — Digital Devices

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Digital-Special (PMOS, Low voltage CMOS, etc.) 258

Detailed Product Information provided by:

American Microsystems Inc. 261

Raytheon Semiconductor 262

The manufacturers listed above are providing detailed information on their latest and most significant products. They have made this investment to help you. Some chose not to.
If you want to see more data in future editions, tell the manufacturers through their salesmen and distributors.

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WHICH DIGITAL FAMILY?

Edited from material published in Fairchild Progress magazine, Peter Alfke, author.

With several digital families available, the logical question is — which are the best ICs for my particular application?

To answer the question, you need to evaluate the pros and cons of the various logic families. These tradeoffs are listed in Tables I-IV. You will need to establish your speed requirements. Since speeds are characterized by the clock rate of registers and counters, this discussion is divided into four groups based on clock rates.

Very High Speed	Clock Rate	> 100 MHz	ECL
High Speed	Clock Rate	30 to 100 MHz	ECL, S-TTL
Medium Speed	Clock Rate	5 to 50 MHz	LS-TTL, TTL
Low Speed	Clock Rate	< 5 MHz	LS-TTL, CMOS

VERY HIGH SPEED SYSTEMS — Clock Rate > 100 MHz

There is only one reasonable IC logic family for use in very high speed systems — Emitter Coupled Logic, ECL. Originally, this technology presented considerable electrical problems such as voltage and temperature sensitivity and fast edge rates that caused reflection and cross-talk problems. In recent years, however, ECL development has become more user-oriented and there is better compatibility between circuit characteristics and interconnection techniques.

The modern popular ECL line is the 10,000 Series, manufactured in uncompensated, in voltage-compensated, or in both voltage and temperature-compensated forms. The latter form of compensation assures that significant parameters such as logic levels, noise margins and speed remain constant over a wide range of temperature and power supply voltage. These 10K and 95K logic circuits have deliberately slowed-down edge rates to make them easier to use and they can also drive terminated transmission lines whenever required by the interconnection length.

HIGH SPEED SYSTEMS — Clock Rate 30 to 100 MHz (Table II)

Here, you have a choice between ECL and Schottky TTL. H-TTL is really obsolete since it consumes more power than Schottky TTL, has similar interconnection problems and offers only half the speed. Also, it is not significantly faster than the best Low Power Schottky TTL. So, this narrows down your choice to ECL and Schottky TTL.

MEDIUM SPEED SYSTEMS — Clock Rate 5 to 50 MHz (Table III)

Standard TTL has been the obvious choice for medium speed systems for many years. Many designs will increasingly use Low Power Schottky TTL as it becomes more available, multiple sourced, and as the price premium decreases. You can mix standard and LS-TTL to solve most fan-out problems.

SLOW SPEED SYSTEMS — Clock Rate < 5 MHz (Table IV)

If you design slow speed systems you are faced with the largest number of attractive alternatives. Traditionally, TTL and DTL has been used. Now you can save power, cost and avoid heat and reliability problems by changing to LS-TTL, without affecting the logic design and perhaps not even changing the PC board layout.

If the system speed permits, you can switch to CMOS and save even more power and simplify the power supply, but now you must cope with a family of different logic elements and a hodgepodge of MSI elements, far less systems oriented than the better TTL circuits. Also you will notice wide parameter differences between the "same" products from different vendors.

The greatest challenge, however, is to examine the traditional hard-wired system design and decide whether or not it can be implemented with a microprocessor. If the requirements are both complicated and slow enough, this approach might save manufacturing cost, design time, and service time, as well as improve reliability, provide additional flexibility, and perhaps allow additional features at no extra cost.

MOS (p-channel, n-channel, either metal or silicon gate, also silicon on sapphire) does not compete directly with LS-TTL and CMOS. The MOS logic elements (gates and flip-flops) are very small but the input and output buffers are so large and relatively slow that MOS cannot be cost/performance competitive at MSI complexity (below 200 gates). MOS is therefore meaningful only in LSI circuits, where it has proven to be not only competitive, but dominating. These areas are:

- LSI memories, RAMs, ROMs, and shift registers of 500 to 4096 bits at clock rates below 5 MHz.
- Specialized, inherently slow LSI functions produced in very large volume (calculators, clocks, some instrument circuits like DVMs).
- Custom LSI circuits where the manufacturing volume is high enough or the weight/space saving valuable enough to absorb the development cost.
- Microprocessors, where a very carefully designed, standard circuit performs specialized tasks through ROM-stored programming.

SUMMARY

The proliferation of digital circuits and technologies gives you a new degree of freedom, but it also challenges your judgement and imagination. You are faced with an almost overwhelming number of competing technologies, each with its strong and weak points. The basic component speed requirement and the available power will quickly narrow your choice down to two or three different logic families; the tables presented here will make your final decision easier.

You should not forget, however, that the component speed requirement is also affected by your choice of architecture. A parallel approach requires more, but slower components, while a serial architecture requires fewer but faster components. The vesatility of modern MSI circuits makes it easy to explore these alternatives. It is very important to choose the IC logic family at an early stage in the system design, since the full cost, speed and reliability advantages can only be gained by designing in accordance with the device features, taking advantage of their logic and organization.

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TABLE I: COMPARISON OF ELECTRICAL CHARACTERISTICS

	CMOS 5 V SUPPLY	CMOS 10 V SUPPLY	STANDARD TTL	74LS LOW POWER SCHOTTKY	9LS LOW POWER SCHOTTKY	SCHOTTKY TTL	10K ECL
PROPAGATION DELAY	35 ns	25 ns	10 ns	10 ns	5 ns	3 ns	2 ns
FLIP-FLOP TOGGLE FREQUENCY	5 MHz	10 MHz	35 MHz	40 MHz	80 MHz	100 MHz	200 MHz
QUIESCENT POWER[1]	10 nW	10 nW	10 mW	2 mW	2 mW	25 mW	25 mW
NOISE IMMUNITY	2 V	4 V	1 V	0.8 V	0.8 V	0.9 V	0.2 V
FAN OUT (within family)	>50[2]	>50[2]	10	20	20	10	>50

[1]Note the change from nanowatts to milliwatts.
[2]Or as determined by allowable propagation delay.

TABLE II. COMPARISON OF DIGITAL LOGIC FAMILY CHARACTERISTICS FOR HIGH SPEED SYSTEMS (CLOCK RATE 30 TO 100 MHz)

10K AND 95K SERIES ECL	SCHOTTKY TTL
Advantages	**Disadvantages**
Short delays allow propagation through more logic levels in a clock cycle. Compatibility with even faster families currently in development makes future system upgrading easy.	Component delays are about twice as long as with ECL and will not be improved in the foreseeable future.
Low output impedance drives all types of interconnections including terminated transmission lines.	Outputs are not capable of driving terminated transmission lines without causing severe fan-out compromises.
High output drive capability and complementary outputs accommodate differential transmission over tested pairs.	
Slow edge rate minimizes reflection problems.	Has the fastest output transitions of any logic family, causing reflection problems even with relatively short interconnection lengths, and causing cross-talk problems.
Complementary outputs on many elements add design flexibility.	
Wired-OR capability simplifies logic design.	
Compensated circuits simplify power supply and temperature regulation.	Generates fast power supply load changes, requires good decoupling.
High input impedance minimizes loading, allows high fan-out.	Input thresholds and output low levels are slightly offset from conventional TTL, causing some loss of noise immunity.
Disadvantages	**Advantages**
Unfamiliar type of circuitry, logic, nomenclature, and pinouts.	Compatible with popular TTL, same supply voltage, almost identical signal levels, same SSI and MSI logic, nomenclature, pinouts. Ideal to speed up critical paths in standard TTL systems.
Not level-compatible with TTL and CMOS, requires additional interface elements.	
Requires external pull-down resistors on all used outputs.	Outputs require no pull-up (or down) resistors.
Has less absolute noise margin.	Large signal swing and large absolute noise immunity cause less problems with temperature or supply voltage variations and gradients, resistive drops along supply lines, and outside noise.
Higher ground current requires heavier distribution busses.	
Has one less logic pin per package due to double ground.	
Has higher power consumption at low frequencies than equivalent S-TTL circuits.	Has lower system power consumption at moderate speed.

TABLE III. COMPARISON OF DIGITAL LOGIC FAMILY CHARACTERISTICS FOR MEDIUM SPEED SYSTEMS (CLOCK RATE 5 TO 50 MHz)

STANDARD TTL	LOW POWER SCHOTTKY TTL
Advantages	**Disadvantages**
Large number of SSI and MSI functions.	Somewhat fewer devices but this is changing.
Low prices.	Presently higher priced than standard TTL.
Specifications standardized.	Electrical characteristics differ between suppliers.
Disadvantages	**Advantages**
High power consumption (10 mW per gate, 200 to 500 mW per MSI package.)	Saves 75% of the power of equivalent standard TTL.
Large, heavy, expensive, hot power supply and regulator.	Smaller, lighter, cheaper, cooler power supply and regulator.
Heat density problems when using predominantly MSI.	No heat density problem. Cooler, therefore more reliable.
	May eliminate the need for fans and filters.
Not fully compatible with most CMOS and MOS.	Compatible with CMOS and MOS.
	Generates less noise than standard TTL.

TABLE IV. COMPARISON OF DIGITAL LOGIC FAMILY CHARACTERISTICS FOR LOW SPEED SYSTEMS (CLOCK RATE 5 MHz)

STANDARD OR LOW POWER SCHOTTKY TTL	CMOS
Advantages	**Disadvantages**
Well designed, system-oriented MSI.	Some of the original CMOS circuits are poorly defined and not systems oriented.
Adequate speed, tight tolerances.	Low speed, delays depend on supply voltage and capacitive loading.
Low impedance outputs give good immunity against capacitively coupled noise.	Poor current noise immunity (capacitively coupled noise.)
Familiar functions, logic, pinouts.	New functions, logic pinouts.
Standard TTL available from many suppliers, low cost.	Large parameter variations between different vendors.
Disadvantages	**Advantages**
Relatively high static consumption and heat generation.	Extremely low static power consumption, very little heat generated at moderate speed.
Tight power supply voltage requirements (5 V $\pm$5% commercial, $\pm$10% military grade).	Very wide range of supply voltages (theoretically 3 . . . 20 V, practically 5 . . . 12 V).
Not well-suited for portable battery operation.	Ideally suited for battery operation.
More expensive power supply.	Low cost power supply. Less cost, weight, heat, size than for any other family.
Lower voltage noise immunity.	High voltage noise immunity, an advantage with inductively coupled noise.
LS-TTL available from only a few suppliers.	Available from many suppliers.

DIGITAL–CMOS

Function	Device	Source	Line
Arithmetic Functions			
2 x 2 Bit (Parallel) Binary Multiplier	MC14554BA	†Motorola	
	MC14554BC	Motorola	
4 Bit Full Adder	F4008BC	Fairchild	
	F4008BM	†Fairchild	
	HD54C83	†Harris	
	HD74C83	Harris	
	MC14008BA	†Motorola	
	MC14008BC	Motorola	10
	MM54C83	†National	
	MM74C83	National	
	CD4008BC	National	
	CD4008BM	†National	
	CD4008B	†RCA	
	CD4008BE	RCA	
	HBF4008AE	SGS	
	SCL4008B	†SSS	
	SCL4008BE	SSS	
	CM4008A	†Solitron	20
	CM4008AE	Solitron	
	TP4008A/B	TI	
	TC4008	Toshiba	
Triple Serial Adder (Positive Logic) with Internal Carry	MC14032BA	†Motorola	
	MC14032BC	Motorola	
	CD4032B	†RCA	
	CD4032BE	RCA	
	CM4032A	†Solitron	
	CM4032AE	Solitron	30
	TC4032	Toshiba	
Triple Serial Adder (Negative Logic) with Internal Carry	MC14038BA	†Motorola	
	MC14038BE	Motorola	
	CD4038B	†RCA	
	CD4038BE	RCA	
	CM4038A	†Solitron	
	CM4038AE	Solitron	
	TC4038	Toshiba	
4 Bit Arithmetic Array	CD4057B	†RCA	40
4 Bit Arithmetic Logic Unit	MC14581BA	†Motorola	
	MC14581BC	Motorola	
	CD40181B	†RCA	
	CD40181BE	RCA	
	SCL4581B	†SSS	
	SCL4581BE	SSS	
	TP4581A	TI	
Look Ahead Carry Block	F4582BC	Fairchild	50
	F4582BM	†Fairchild	
	MC14582BA	†Motorola	
	MC14582BC	Motorola	
	CD40182B	†RCA	
	CD40182BE	RCA	
	SCL4582B	SSS	
	TP4582A	TI	
4 Bit Magnitude Comparator	F40085BC	Fairchild	
	F40085BM	†Fairchild	60
	HD54C85	†Harris	
	HD74C85	Harris	
	MC14585BA	†Motorola	
	MC14585BC	Motorola	
	MM54C85	†National	
	MM74C85	National	
(Continued)			

Function	Device	Source	Line
Arithmetic Functions (Cont'd)			
4 Bit Magnitude Comparator (Cont'd.)	μPD4063	NEC America	
	CD4063B	†RCA	70
	CD4063BE	RCA	
	SCL4585B	†SSS	
	SCL4585BE	SSS	
	TC4585	Toshiba	
NBCD Adder (Natural Binary Coded Decimal)	MC14560BA	†Motorola	
	MC14560BC	Motorola	
	μPD4560	NEC America	
Nines Complementer	MC14561BA	†Motorola	80
	MC14561BC	Motorola	
	μPD4561	NEC America	
Data Path Switch	F4704BC	Fairchild	
	F4704BM	†Fairchild	
Arithmetic Logic Register Stack	F4705BC	Fairchild	
	F4705BM	†Fairchild	
Data Access Register (for memory address arithmetic)	F4707BC	Fairchild	90
	F4707BM	†Fairchild	
Buffers/Inverters			
Quad Low Impedance Buffer	SCL4441B	†SSS	
	SCL4441BE	SSS	
Hex Buffer/Converter (Non Inverting)	SIL4010B	†Mitel	
	SIL4010BE	Mitel	
	CD4010AC	National	
	CD4010AM	†National	
	CD4010B	†RCA	100
	CD4010BE	RCA	
	HBF4010BE	SGS	
	SCL4010B	†SSS	
	SCL4010BE	SSS	
	CM4010A	†Solitron	
	CM4010AE	Solitron	
	TP4010A/B	†TI	
	TC4010	Toshiba	
Hex Buffer/Converter (Non Inverting) Improved	F4050BC	Fairchild	110
	F4050BM	†Fairchild	
	SIL4050B	†Mitel	
	SIL4050BE	Mitel	
	MC14050BA	†Motorola	
	MC14050BC	Motorola	
	CD4050BC	National	
	CD4050BM	National	
	μPD4050	NEC America	
	CD4050B	†RCA	
	CD4050BE	RCA	120
	HBF4050AE	SGS	
	SCL4050B	†SSS	
	SCL4050BE	SSS	
	CM4050A	†Solitron	
	CM4050AE	Solitron	
	TP4050A/B	TI	
	TC4050	Toshiba	
Hex Buffer, Open Drain (Active pull down)	HD54C906	†Harris	
	HD74C906	Harris	130
(Continued)			

Function	Device	Source	Line
Buffers/Inverters (Cont'd)			
Hex Buffer, Open Drain (Active pull down) (Cont'd.)	MM54C906	†National	
	MM74C906	National	
Hex Buffer, Open Drain (Active pull up)	HD54C907	†Harris	
	HD74C907	Harris	
	MM54C907	†National	
	MM74C907	National	
Hex Buffer, Three State	F40097BC	Fairchild	140
	F40097BM	†Fairchild	
	HD70C95	†Harris	
	HD70C97	†Harris	
	HD80C95	Harris	
	HD80C97	Harris	
	MC14503BA	†Motorola	
	MC14503BC	Motorola	
	CD4503BC	National	
	CD4503BM	†National	
	MM70C95	†National	150
	MM70C97	†National	
	MM80C95	National	
	MM80C97	National	
	μPD4503	NEC America	
Hex TTL Buffer (Non Inverting)(CMOS to TTL)	HD54C902	†Harris	
	HD74C902	Harris	
	MM54C902	†National	
	MM74C902	National	
Hex PMOS Buffer (Non Inverting) (PMOS to CMOS or TTL)	HD54C904	†Harris	160
	HD74C904	Harris	
	MM54C904	†National	
	MM74C904	National	
Hex Buffer/Converter (Inverting)	SIL4009B	†Mitel	
	SIL4009BE	Mitel	
	CD4009AC	National	
	CD4009AM	†National	170
	CD4009UB	†RCA	
	CD4009UBE	RCA	
	HBF4009AE	SGS	
	SCL4009B	†SSS	
	SCL4009BE	SSS	
	SCL4009UBE	SSS	
	CM4009A	†Solitron	
	CM4009AE	Solitron	
	TP4009A/UB	TI	
	TC4009	Toshiba	180
Hex Buffer/Converter (Inverting) Improved	F4049BC	Fairchild	
	F4049BM	†Fairchild	
	SIL4049B	†Mitel	
	SIL4049BE	Mitel	
	MC14049BA	†Motorola	
	MC14049BC	Motorola	
	CD4049UBC	National	
	CD4049UBM	†National	
	μPD4049	NEC America	190
	CD4049UB	†RCA	
	CD4049UBE	RCA	
	HBF4049AE	SGS	
	SCL4049B	†SSS	
	SCL4049BE	SSS	
	SCL4049UB	SSS	
	CM4049A	†Solitron	
(Continued)			

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–CMOS (Cont'd)

Buffers/Inverters (Cont'd)

Function	Device	Source	Line
Hex Buffer/Converter (Inverting) Improved (Cont'd.)			
	CM4049AE	Solitron	
	TP4049A/UB	TI	
	TC4049	Toshiba	
Hex Inverter			
	F4069UBC	Fairchild	
	F4069UBM	† Fairchild	
	HD54C04	† Harris	
	HD74C04	Harris	
	SIL4069B	† Mitel	10
	SIL4069BE	Mitel	
	MC14069BA	† Motorola	
	MC14069BC	Motorola	
	CD4069C	National	
	CD4069M	† National	
	MM54C04	† National	
	MM74C04	† National	
	μPD4069	NEC America	
	CD4069UB	† RCA	
	CD4069UBE	RCA	20
	SCL4069B	† SSS	
	SCL4069BE	SSS	
	SCL4449B	† SSS	
	SCL4069UB	SSS	
	SCL4449BE	SSS	
	CM4069A	† Solitron	
	CM4069AE	Solitron	
	TP4069A/UB	TI	
	TP4315A	TI	
	TC4069	Toshiba	30
	TC7404	Toshiba	
Hex Inverter, Three State			
	F40098BC	Fairchild	
	F40098BM	† Fairchild	
	MM70C96	† National	
	MM80C96	National	
	MM70C98	† National	
	MM80C98	National	
Hex Inverter/Buffer, Three State, Strobed			
	SIL4502B	† Mitel	40
	SIL4502BE	Mitel	
	MC14502BA	† Motorola	
	MC14502BC	Motorola	
	CD4502B	† RCA	
	CD4502BE	RCA	
	SCL4502B	† SSS	
	SCL4502BF	SSS	
Hex TTL Buffer (Inverting)(CMOS to TTL)			
	HD54C901	† Harris	
	HD74C901	Harris	50
	MM54C901	† National	
	MM74C901	National	
Hex PMOS Buffer (Inverting)(PMOS to CMOS or TTL)			
	HD54C903	† Harris	
	HD74C903	Harris	
	MM54C903	† National	
	MM74C903	National	
Hex CMOS Compatible Buffer			
	DS1630	† National	
	DS3630	National	60
Dual Complementary Pair plus Inverter			
	F4007UBC	Fairchild	
	F4007UBM	† Fairchild	
	SIL4007B	† Mitel	
	SIL4007BE	† Mitel	
	MC14007BA	† Motorola	

(Continued)

Buffers/Inverters (Cont'd)

Function	Device	Source	Line
Dual Complementary Pair plus Inverter (Cont'd.)			
	MC14007BC	Motorola	
	CD4007C	National	
	CD4007M	† National	70
	CD4007UB	† RCA	
	CD4007UBE	RCA	
	HBF4007AE	SGS	
	SCL4007B	† SSS	
	SCL4007BE	SSS	
	CM4007A	† Solitron	
	CM4007AE	Solitron	
	TP4007A/UB	TI	
	TC4007	Toshiba	
Quad True/Complement Buffer			80
	F4041BC	Fairchild	
	F4041BM	† Fairchild	
	CD4041C	National	
	CD4041M	National	
	CD4041UB	† RCA	
	CD4041UBE	RCA	
	SCL4041B	† SSS	
	SCL4041BE	SSS	
	CM4041A	† Solitron	
	CM4041AE	Solitron	90

Counters, Binary

Function	Device	Source	Line
Divide by 2, 8 or 16 Counter			
	HD54C93	† Harris	
	HD74C93	Harris	
	MM54C93	† National	
	MM74C93	National	
7 Stage Binary Counter			
	F4024BC	Fairchild	
	F4024BM	† Fairchild	
	SIL4024B	† Mitel	
	SIL4024BE	Mitel	100
	MC14024BA	† Motorola	
	MC14024BC	Motorola	
	CD4024BC	National	
	CD4024BM	† National	
	μPD4024	NEC America	
	CD4024B	† RCA	
	CD4024BE	RCA	
	HBF4024AE	SGS	
	SCL4024B	† SSS	
	SCL4024BE	SSS	110
	CM4024A	† Solitron	
	CM4024AE	Solitron	
	TP4024A/B	TI	
	TC4024	Toshiba	
8 Stage Synchronous Binary Counter			
	SCL4404B	† SSS	
	SCL4404BE	SSS	
12 Stage Binary Counter			
	F4040BC	Fairchild	
	F4040BM	† Fairchild	120
	SIL4040B	† Mitel	
	SIL4040BE	Mitel	
	MC14040BA	† Motorola	
	MC14040BC	Motorola	
	CD4040BC	National	
	CD4040BM	† National	
	μPD4040	NEC America	
	CD4040B	† RCA	
	CD4040BE	RCA	
	CDS4040	† RCA	130
	CDS4040E	RCA	

(Continued)

Counters, Binary (Cont'd)

Function	Device	Source	Line
12 Stage Binary Counter (Cont'd.)			
	SCL4040B	† SSS	
	SCL4040BE	SSS	
	CM4040A	† Solitron	
	CM4040AE	Solitron	
	TF4040A/B	† TI	
	TP4040A/B	TI	
	TC4040	Toshiba	
14 Stage Binary Counter			140
	F4020BC	Fairchild	
	F4020BM	† Fairchild	
	MC14020BA	† Motorola	
	MC14020BC	Motorola	
	SIL4020B	† Mitel	
	SIL4020BE	Mitel	
	CD4020BC	National	
	CD4020BM	† National	
	μPD4020	NEC America	
	CD4020B	† RCA	150
	CD4020BE	RCA	
	CDS4020	† RCA	
	CDS4020E	RCA	
	HBF4020AE	SGS	
	SCL4020B	† SSS	
	SCL4020BE	SSS	
	CM4020A	† Solitron	
	CM4020AE	Solitron	
	TP4020A/B	TI	
	TC4020	Toshiba	160
14 Stage Binary Counter and Oscillator			
	SIL4060B	† Mitel	
	SIL4060BE	Mitel	
	CD4060BC	National	
	CD4060BM	† National	
	CD4060B	† RCA	
	CD4060BE	RCA	
	CDS4060	† RCA	
	CDS4060E	RCA	
	SCL4060B	† SSS	170
	SCL4060BE	SSS	
Presettable Synchronous Binary Counter, Asynchronous Clear			
	F40161BC	Fairchild	
	F40161BM	† Fairchild	
	HD54C161	† Harris	
	HD74C161	Harris	
	MC14161BA	† Motorola	
	MC14161BC	Motorola	
	CD40161BC	National	180
	CD40161BM	† National	
	MM54C161	† National	
	MM74C161	National	
	CD40161B	† RCA	
	CD40161BE	RCA	
	SCL4161B	† SSS	
	SCL4161BE	SSS	
	TP4361A	TI	
Presettable Fully Synchronous Binary Counter, Synchronous Clear			190
	F40163BC	Fairchild	
	F40163BM	† Fairchild	
	HD54C163	† Harris	
	HD74C163	Harris	
	MC14163BA	† Motorola	
	MC14163BC	Motorola	
	CD40163BC	National	
	CD40163BM	† National	
	MM54C163	† National	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–CMOS (Cont'd)

Counters, Binary (Cont'd)

Function	Device	Source	Line
Presettable Fully Synchronous Binary Counter, Synchronous Clear (Cont'd.)			
	MM74C163	National	
	CD40163B	†RCA	
	CD40163BE	RCA	
	SCL4163B	†SSS	
	SCL4163BE	SSS	
	TP4363A	TI	
Dual Synchronous Binary Counter			
	F4520BC	Fairchild	10
	F4520BM	†Fairchild	
	SIL4520B	†Mitel	
	SIL4520BE	Mitel	
	MC14520BA	†Motorola	
	MC14520BC	Motorola	
	CD4520BC	National	
	CD4520BM	†National	
	µPD4520	NEC America	
	CD4520B	†RCA	
	CD4520BE	RCA	20
	CDS4520	†RCA	
	CDS4520E	RCA	
	SCL4520B	†SSS	
	SCL4520BE	SSS	
	CM4520B	†Solitron	
	CM4520BE	Solitron	
	TP4520A	TI	
	TC4520	Toshiba	
Presettable Binary Up/Down Counter			
	F40193BC	Fairchild	30
	F40193BM	†Fairchild	
	F4516BC	Fairchild	
	F4516BM	†Fairchild	
	HD54C193	†Harris	
	HD74C193	Harris	
	SIL4516B	†Mitel	
	SIL4516BE	Mitel	
	MC14516BA	†Motorola	
	MC14516BC	Motorola	
	CD40193BC	National	40
	CD40193BM	†National	
	CD4516BC	National	
	CD4516BM	†National	
	MM54C193	†National	
	MM74C193	National	
	µPD4516	NEC America	
	CD40193B	†RCA	
	CD40193BE	RCA	
	CD4516B	†RCA	
	CD4516BE	RCA	50
	SCL4193B	†SSS	
	SCL4516B	†SSS	
	SCL4516BE	SSS	
	TC4516	Toshiba	
Presettable 8 bit Binary Down Counter			
	CD40103B	†RCA	
	CD40103BE	RCA	
Programmable Binary Divide by N 4 Bit Counter			
	F4526BC	Fairchild	
	F4526BM	†Fairchild	60
	MC14526BA	†Motorola	
	MC14526BC	Motorola	
	CD4526BC	National	
	CD4526BM	†National	
	µPD4526	NEC America	
	SCL4526B	†SSS	
	SCL4526BE	SSS	
	TP4526A	TI	

Counters, Decade

Function	Device	Source	Line
Presettable Decade Counter (Sets to 0 or 9, divides by 2, 5 or 10)			70
	HD54C90	†Harris	
	HD74C90	Harris	
	MM54C90	†National	
	MM74C90	National	
Presettable Synchronous Decade Counter, Asynchronous Clear			
	F40160BC	Fairchild	
	F40160BM	†Fairchild	
	HD54C160	†Harris	
	HD74C160	Harris	80
	MC14160BA	†Motorola	
	MC14160BC	Motorola	
	CD40160BC	National	
	CD40160BM	†National	
	MM54C160	†National	
	MM74C160	National	
	CD40160B	†RCA	
	CD40160BE	RCA	
	SCL4160B	†SSS	
	SCL4160BE	SSS	90
	TP4360A	TI	
Presettable Fully Synchronous Decade Counter, Synchronous Clear			
	F40162BC	Fairchild	
	F40162BM	†Fairchild	
	HD54C162	†Harris	
	HD74C162	Harris	
	MC14162BA	†Motorola	
	MC14162BC	Motorola	
	CD40162BC	National	100
	CD40162BM	†National	
	MM54C162	†National	
	MM74C162	National	
	CD40162B	†RCA	
	CD40162BE	RCA	
	SCL4162B	†SSS	
	SCL4162BE	SSS	
	TP4362A	TI	
Dual Synchronous Decade Counter			
	F4518BC	Fairchild	110
	F4518BM	†Fairchild	
	SIL4518B	†Mitel	
	SIL4518BE	Mitel	
	MC14518BA	†Motorola	
	MC14518BC	Motorola	
	CD4518BC	National	
	CD4518BM	†National	
	µPD4518	NEC America	
	CD4518B	†RCA	
	CD4518BE	RCA	120
	CDS4518	†RCA	
	CDS4518E	RCA	
	SCL4518B	†SSS	
	SCL4518BE	SSS	
	CM4518B	†Solitron	
	CM4518BE	Solitron	
	TP4518A	TI	
	TC4518	Toshiba	
Decade Counter/Divider, 10 line output			
	F4017BC	Fairchild	130
	F4017BM	†Fairchild	
	SIL4017B	†Mitel	
	SIL4017BE	Mitel	
	MC14017BA	†Motorola	
	MC14017BC	Motorola	
	CD4017BC	National	
	CD4017BM	†National	

(Continued)

Counters, Decade (Cont'd)

Function	Device	Source	Line
Decade Counter/Divider, 10 line output (Cont'd.)			
	µPD4017	NEC America	
	CD4017B	†RCA	140
	CD4017BE	RCA	
	CDS4017	†RCA	
	CDS4017E	RCA	
	HBF4017AE	SGS	
	SCL4017B	†SSS	
	SCL4017BE	SSS	
	CM4017A	†Solitron	
	CM4017AE	Solitron	
	TP4017A	TI	
	TC4017	Toshiba	150
Presettable Decade Up/Down Counter			
	F40192BC	Fairchild	
	F40192BM	†Fairchild	
	F4510BC	Fairchild	
	F4510BM	†Fairchild	
	HD54C192	†Harris	
	HD74C192	Harris	
	SIL4510B	†Mitel	
	SIL4510BC	Mitel	
	MC14510BA	†Motorola	160
	MC14510BC	Motorola	
	CD40192BC	National	
	CD40192BM	†National	
	CD4510BC	National	
	CD4510BM	†National	
	MM54C192	†National	
	MM74C192	National	
	µPD4510	NEC America	
	CD40192B	†RCA	
	CD40192BE	RCA	170
	CD4510B	†RCA	
	CD4510BE	RCA	
	CD4192B	†SSS	
	SCL4510B	†SSS	
	SCL4510BE	SSS	
	TC4510	Toshiba	
Presettable 2 Decade Down Counter			
	CD40102A/B	†RCA	
	CD40102A/BE	RCA	
Programmable Decade Divide By N 4 Bit Counter			180
	F4522BC	Fairchild	
	F4522BM	†Fairchild	
	MC14522BA	†Motorola	
	MC14522BC	Motorola	
	CD4522BC	National	
	CD4522BM	†National	
	µPD4522	NEC America	
	SCL4522B	†SSS	
	SCL4522BE	SSS	
	TP4522A	TI	190
4 Decade Divide by N Counter			
	CD4059A	†RCA	
	CD4059AE	RCA	
Presettable Up/Down Decade Counter 7 Segment Display and BCD Output			
	HCTR0200	Hughes	
Decade Counter/Divider 7 Segment Display Output and Display Enable			
	CD4026B	†RCA	
	CD4026BE	RCA	200
	SCL4026B	†SSS	
	SCL4026BE	SSS	
	SCL4426B	†SSS	
	SCL4426BE	SSS	

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† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–CMOS (Cont'd)

Counters, Decade (Cont'd)

Function	Device	Source	Line
Decade Counter/Divider 7 Segment Display Output and Display Enable (Cont'd.)			
	CM4026A	†Solitron	
	CM4026AE	Solitron	
Decade Counter/Divider 7 Segment Display Output and Ripple Blanking			
	CD4033B	†RCA	
	CD4033BE	RCA	
	HBF4033AE	SGS	
	SCL4033B	†SSS	10
	SCL4033BE	SSS	
	SCL4433B	†SSS	
	SCL4433BE	SSS	
	CM4033A	†Solitron	
	CM4033AE	Solitron	
Decade Up/Down Counter, Latch, Decoder, 7 Segment Display Output			
	CD40110B	RCA	
3 1/2 Digit Counter to BCD Driver			
	CM4102	†Solitron	20
	CM4102	Solitron	
3 Decade Counter, Multiplexed Output			
	F4553BC	Fairchild	
	F4553BM	†Fairchild	
	MC14553BA	†Motorola	
	MC14553BC	Motorola	
4 Decade Counter			
	TC5001	Toshiba	
4 Decade Counter, Multiplexed Output (The 926 gives carry at 6000.)			30
	HD54C925	†Harris	
	HD74C925	Harris	
	HD54C926	†Harris	
	HD74C926	Harris	
	MM54C925	†National	
	MM74C925	National	
	MM54C926	†National	
	MM74C926	National	
4 Digit Counter, Multiplexed Output, Second digit counts to 6 (Maximum count 9599.)			40
	HD54C927	†Harris	
	HD74C927	Harris	
	MM54C927	†National	
	MM74C927	National	
4 Digit Counter, Multiplexed Output, Left digit counts to 2 (Maximum count 1999.)			
	HD54C928	†Harris	
	HD74C928	Harris	
	MM54C928	†National	
	MM74C928	National	50
4 1/2 Digit Up Down Counter Oscillator (Maximum count 19999)			
	HCTR4010	Hughes	
	HCTR6010	Hughes	
5 Decade Counter, Multiplexed Output			
	MC14534BA	†Motorola	
	MC14534BC	Motorola	
7 Decade Counter, Multiplexer, Display Driver, 2 6v Supply			
	7208	Intersil	60

Counters, Miscellaneous

Function	Device	Source	Line
See also CMOS Oscillators/Dividers			
Presettable Up/Down Binary or Decade Counter			
	F4029BC	Fairchild	
	F4029BM	†Fairchild	
	SIL4029B	†Mitel	
	SIL4029BE	Mitel	
	CD4029BC	National	
	CD4029BM	†National	
	µPD4029	NEC America	
	CD4029B	†RCA	
	CD4029BE	RCA	70
	HBF4029AE	SGS	
	SCL4029B	†SSS	
	SCL4029BE	SSS	
	CM4029A	†Solitron	
	CM4029AE	Solitron	
	TP4029A	TI	
	TC4029	Toshiba	
Dual Programmable Binary/Decade Counter			
	MC14569BA	†Motorola	
	MC14569BC	Motorola	80
Divide by 8 Counter/Divider, Decoded Output			
	F4022BC	Fairchild	
	F4022BM	†Fairchild	
	SIL4022B	†Mitel	
	SIL4022BE	Mitel	
	MC14022BA	†Motorola	
	MC14022BC	Motorola	
	CD4022BC	National	
	CD4022BM	†National	
	CD4022B	†RCA	90
	CD4022BE	RCA	
	HBF4022AE	SGS	
	SCL4022B	†SSS	
	SCL4022BE	SSS	
	CM4022A	†Solitron	
	CM4022AE	Solitron	
	TP4022A	TI	
	TC4022	Toshiba	
Divide by 60 Counter, BCD Output (Industrial Time Base Generator)			100
	MC14566BA	†Motorola	
	MC14566BC	Motorola	
Presettable Divide by N Counter			
	F4018BC	Fairchild	
	F4018BM	†Fairchild	
	SIL4018B	†Mitel	
	SIL4018BE	Mitel	
	MC14018BA	†Motorola	
	MC14018BC	Motorola	
	CD4018BC	National	110
	CD4018BM	†National	
	CD4018B	†RCA	
	CD4018BE	RCA	
	HBF4018AE	SGS	
	SCL4018B	†SSS	
	SCL4018BE	SSS	
	CM4018A	†Solitron	
	CM4018AE	Solitron	
	TP4018A/B	TI	
	TC4018	Toshiba	120
Phase Comparator and Programmable Counters			
	MC14568BA	†Motorola	
	MC14568BC	Motorola	

Decoders

Function	Device	Source	Line
BCD to Decimal Decoder			
	F4028BC	Fairchild	
	F4028BM	†Fairchild	
	HD54C42	†Harris	
	HD74C42	Harris	
	SIL4028B	†Mitel	
	SIL4028BE	Mitel	130
	MC14028BA	†Motorola	
	MC14028BC	Motorola	
	CD4028BC	National	
	CD4028BM	†National	
	MM54C42	†National	
	MM74C42	National	
	µPD4028	NEC America	
	CD4028B	†RCA	
	CD4028BE	RCA	
	HBF4028AE	SGS	140
	SCL4028B	†SSS	
	SCL4028BE	SSS	
	CM4028A	†Solitron	
	CM4028AE	Solitron	
	TP4028A/B	TI	
	TC4028	Toshiba	
BCD to 7 Segment Decoder			
	HD54C48	†Harris	
	HD74C48	Harris	
	MC14558BA	†Motorola	150
	MC14558BC	Motorola	
	MM54C48	†National	
	MM74C48	National	
	UCN-4102A	Sprague	
	TC5002	Toshiba	
4 bit Latch/4 to 16 Line Decoder (High)			
	F4514BC	Fairchild	
	F4514BM	†Fairchild	
	SIL4514BE	Mitel	
	SIL4514B	†Mitel	160
	MC14514BA	†Motorola	
	MC14514BC	Motorola	
	CD4514BC	National	
	CD4514BM	†National	
	µPD4514	NEC America	
	CD4514B	†RCA	
	CD4514BE	RCA	
	SCL4514B	†SSS	
	CM4514B	†Solitron	
	CM4514BE	Solitron	170
	TC4514	Toshiba	
4 bit Latch/4 to 16 Line Decoder (Low)			
	F4515BC	Fairchild	
	F4515BM	†Fairchild	
	SIL4515B	†Mitel	
	SIL4515BE	Mitel	
	MC14515BA	†Motorola	
	MC14515BC	Motorola	
	CD4515BC	National	
	CD4515BM	†National	180
	µPD4515	NEC America	
	CD4515B	†RCA	
	CD4515BE	RCA	
	SCL4515B	†SSS	
	CM4515B	†Solitron	
	CM4515BE	Solitron	
	TC4515	Toshiba	
Dual Binary to 1 of 4 Decoder/Demultiplexer (High)			
	F4555BC	Fairchild	
	F4555BM	†Fairchild	190
	MC14555BA	†Motorola	
	MC14555BC	Motorola	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–CMOS (Cont'd)

Function	Device	Source	Line
Decoders (Cont'd)			
Dual Binary to 1 of 4 Decoder/Demultiplexer (High) (Cont'd.)			
	µPD4555	NEC America	
	CD4555B	†RCA	
	CD4555BE	RCA	
	SCL4555B	†SSS	
Dual Binary to 1 of 4 Decoder/Demultiplexer (Low)			
	F4556BC	Fairchild	
	F4556BM	†Fairchild	
	MC14556BA	†Motorola	
	MC14556BC	Motorola	10
	µPD4556	NEC America	
	CD4556B	†RCA	
	CD4556BE	RCA	
	SCL4556B	†SSS	
4 Line to 16 Line Decoder/Demultiplexer			
	HD54C154	†Harris	
	HD74C154	Harris	
	MM54C154	†National	
	MM74C154	National	
1 of 8 Strobed Decoder			20
	SCL4428B	†SSS	
	SCL4428BE	SSS	
Drivers			
BCD to 7 Segment Latch/Decoder/Driver			
	F4511BC	Fairchild	
	F4511BM	†Fairchild	
	F4734BC	†Fairchild	
	F4734BM	Fairchild	
	MC14511BA	†Motorola	
	MC14511BC	Motorola	
	MC14513BA	†Motorola	30
	MC14513BC	Motorola	
	SIL4511B	†Mitel	
	SIL4511BE	Mitel	
	CD4511BC	National	
	CD4511BM	†National	
	µPD4511	NEC America	
	CD4511B	†RCA	
	CD4511BE	RCA	
	SCL4511B	†SSS	
	SCL4511BE	SSS	40
	CM4511B	†Solitron	
	CM4511BE	Solitron	
	TP4511B	TI	
BCD(Hexadecimal) to 7 Segment Latch/Decoder/Driver			
	MD4311B	†Mitel	
	MD4311BE	Mitel	
	MD4568B	†Mitel	
	MD4568BE	Mitel	
BCD to 7 Segment Latch/Decoder/Driver (for Liquid Crystal Displays)			50
	MC14543BA	†Motorola	
	MC14543BC	Motorola	
	CD4543BC	National	
	CD4543BM	†National	
	SCL4543B	SSS	
BCD to 7 Segment Liquid Crystal Decoder/Driver with "Display Frequency Output"			
	MD4055B	†Mitel	
	MD4055BE	Mitel	60
	CD4055B	†RCA	
	CD4055BE	RCA	

Function	Device	Source	Line
Drivers (Cont'd)			
BCD to 7 Segment Liquid Crystal Decoder/Driver with Strobed Latch Function			
	MD4056B	†Mitel	
	MD4056BE	Mitel	
	CD4056B	†RCA	
	CD4056BE	RCA	
7 Segment to BCD Converter			
	MM54C915	†National	70
	MM74C915	National	
Display Driver, 4 Digit (stores segment and address data, drives 7 8 segment digits)			
	MM74C911	National	
Display Driver, 6 Digit (stores segment and address data, drives 7 8 segment digits)			
	MM74C912	National	
	MM74C913	National	
4 Line Liquid Crystal Display Driver			
	CD4054B	†RCA	80
	CD4054BE	RCA	
30 Bit Liquid Crystal Display with Register			
	MD4330B	†Mitel	
	MD4330BE	Mitel	
4 Digit Liquid Crystal Display Driver			
	5015	Nortec	
	DF411	**Siliconix**	**(536)**
	SCL5424	SSS	
	SCL5441	SSS	
8 Digit LED Display Driver			
	SCL5440A	†SSS	90
Dual High Voltage Driver, Source 250 ma			
	HD54C908	†Harris	
	HD74C908	Harris	
	MM74C908	National	
	MM74C918	National	
Dual and Quad Line Drivers See Miscellaneous			
Flip-Flops			
Dual "D" Flip Flop			
	F4013BC	Fairchild	
	F4013BM	†Fairchild	100
	HD54C74	†Harris	
	HD74C74	Harris	
	SIL4013B	†Mitel	
	SIL4013BE	Mitel	
	MC14013BA	†Motorola	
	MC14013BC	Motorola	
	CD4013BC	National	
	CD4013BM	†National	
	MM54C74	†National	
	MM74C74	National	110
	µPD4013	NEC America	
	CD4013B	†RCA	
	CD4013BE	RCA	
	HBF4013AE	SGS	
	SCL4013B	†SSS	
	SCL4013BE	SSS	
	CM4013A	†Solitron	
	CM4013AE	Solitron	
	TP4013A/B	TI	
	TC4013	Toshiba	120
Quad "D" Flip Flop			
	F40175BC	Fairchild	
	F40175BM	†Fairchild	
	HD54C175	†Harris	
	HD74C175	Harris	

(Continued)

Function	Device	Source	Line
Flip-Flops (Cont'd)			
Quad "D" Flip Flop (Cont'd.)			
	MC14175BA	†Motorola	
	MC14175BC	Motorola	
	MM54C175	†National	
	MM74C175	National	130
	CD40175B	National	
	µPD4175	NEC America	
Quad "D" Flip Flop, Three State			
	F4076BC	Fairchild	
	F4076BM	†Fairchild	
	HD54C173	†Harris	
	HD74C173	Harris	
	SIL4076B	†Mitel	
	SIL4076BE	Mitel	
	MC14076BA	Motorola	140
	MC14076BC	Motorola	
	MM54C173	†National	
	MM74C173	National	
	CD4076BC	National	
	CD4076BM	†National	
	CD4076B	†RCA	
	CD4076BE	RCA	
	SCL4076B	†SSS	
	SCL4076BE	SSS	
	CM4076A	†Solitron	150
	CM4076AE	Solitron	
Hex "D" Flip Flop			
	F40174BC	Fairchild	
	F40174BM	†Fairchild	
	HD54C174	†Harris	
	HD74C174	Harris	
	MC14174BA	†Motorola	
	MC14174BC	Motorola	
	CD40174BC	National	
	CD40174BM	†National	160
	MM54C174	†National	
	MM74C174	National	
	CD40174B	†RCA	
	CD40174BE	RCA	
	SCL4174B	†SSS	
	TP4370A	TI	
Octal "D" Flip Flop			
	MM54C374	†National	
	MM74C374	National	
Dual "J K" Flip Flop			170
	F4027BC	Fairchild	
	F4027BM	†Fairchild	
	HD54C76	†Harris	
	HD74C76	Harris	
	SIL4027B	†Mitel	
	SIL4027BE	Mitel	
	MC14027BA	†Motorola	
	MC14027BC	Motorola	
	CD4027BC	National	
	CD4027BM	†National	180
	MM54C76	†National	
	MM74C76	National	
	µPD4027	NEC America	
	CD4027B	†RCA	
	CD4027BE	RCA	
	HBF4027AE	SGS	
	SCL4027B	†SSS	
	SCL4027BE	SSS	
	CM4027A	†Solitron	
	CM4027AE	Solitron	190
	TP4027A/B	TI	
	TC4027	Toshiba	
	TC7476	Toshiba	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–CMOS (Cont'd)

Flip-Flops (Cont'd)

Function	Device	Source	Line
Dual "J K" Flip Flop w/o Preset			
	HD54C73	†Harris	
	HD74C73	Harris	
	HD54C107	†Harris	
	HD74C107	Harris	
	MM54C73	†National	
	MM74C73	National	
	MM54C107	†National	
	MM74C107	National	

Gates, AND/NAND

Function	Device	Source	Line
AND Gated "J K" Flip Flop			
	CD4095B	†RCA	10
	CD4095BE	RCA	
	CD4096B	†RCA	
	CD4096BE	RCA	
8 Input AND Gate			
	SIL4968B	†Mitel	
	SIL4968BE	Mitel	
Dual 4 Input AND Gate			
	F4082BC	Fairchild	
	F4082BM	†Fairchild	
	SIL4082B	†Mitel	20
	SIL4082BE	Mitel	
	MC14082BA	†Motorola	
	MC14082BC	Motorola	
	µPD4082	NEC America	
	CD4082B	†RCA	
	CD4082BE	RCA	
	SCL4082B	SSS	
	SCL4082BE	†SSS	
	TP4082B	TI	
	TC4082	Toshiba	30
Triple 3 Input AND Gate			
	F4073BC	Fairchild	
	F4073BM	†Fairchild	
	SIL4073B	†Mitel	
	SIL4073BE	Mitel	
	MC14073BA	†Motorola	
	MC14073BC	Motorola	
	CD4073BC	National	
	CD4073BM	†National	
	µPD4073	NEC America	40
	CD4073B	†RCA	
	CD4073BE	RCA	
	SCL4073B	†SSS	
	SCL4073BE	SSS	
	CM4073A	†Solitron	
	CM4073AE	Solitron	
	TP4073B	TI	
	TC4073	Toshiba	
Quad 2 Input AND Gate			
	F4081BC	Fairchild	50
	F4081BM	†Fairchild	
	HD54C08	†Harris	
	HD74C08	Harris	
	SIL4081B	†Mitel	
	SIL4081BE	Mitel	
	MC14081A	†Motorola	
	MC14081C	Motorola	
	MC14081BA	†Motorola	
	MC14081BC	Motorola	
	CD4081BC	National	60
	CD4081BM	†National	
	MM54C08	†National	
	MM74C08	National	
	µPD4081	NEC America	
	CD4081B	†RCA	

(Continued)

Gates, AND/NAND (Cont'd)

Function	Device	Source	Line
Quad 2 Input AND Gate (Cont'd.)			
	CD4081BE	RCA	
	SCL4081B	†SSS	
	SCL4081BE	SSS	
	CM4081A	†Solitron	70
	CM4081AE	Solitron	
	TP4081B	TI	
	TC4081	Toshiba	
8 Input NAND Gate			
	F4068BC	Fairchild	
	F4068BM	†Fairchild	
	HD54C30	†Harris	
	HD74C30	Harris	
	SIL4068B	†Mitel	
	SIL4068BE	Mitel	80
	MC14068BA	†Motorola	
	MC14068BC	Motorola	
	MM54C30	†National	
	MM74C30	National	
	µPD4068	NEC America	
	CD4068B	†RCA	
	CD4068BE	RCA	
	SCL4068B	†SSS	
	SCL4068BE	SSS	
	SCL4412B	†SSS	90
	SCL4412BE	SSS	
	CM4068A	†Solitron	
	CM4068AE	Solitron	
	TP4068B	TI	
	TC4068	Toshiba	
Dual 4 Input NAND Gate			
	F4012BC	Fairchild	
	F4012BM	†Fairchild	
	HD54C20	†Harris	
	HD74C20	Harris	100
	SIL4012UB	†Mitel	
	SIL4012UBE	Mitel	
	SIL4012B	†Mitel	
	SIL4012BE	Mitel	
	MC14012A	†Motorola	
	MC14012C	Motorola	
	MC14012BA	†Motorola	
	MC14012BC	Motorola	
	CD4012AC	National	
	CD4012AM	†National	110
	MM54C20	†National	
	MM74C20	National	
	µPD4012	NEC America	
	CD4012B	†RCA	
	CD4012BE	RCA	
	CD4012UB	†RCA	
	CD4012UBE	RCA	
	HBF4012AE	SGS	
	SCL4012B	†SSS	
	SCL4012BE	SSS	120
	CM4012A	†Solitron	
	CM4012AE	Solitron	
	TP4012A	TI	
	TC4012	Toshiba	
	TC7420	Toshiba	
Dual 2 Input NAND Gate (Driver)			
	CD40107BE	RCA	
Dual 4 Input Expandable NAND Gate			
	SCL4412B	†SSS	
	SCL4412BE	SSS	130
Triple 3 Input NAND Gate			
	F4023BC	Fairchild	

(Continued)

Gates, AND/NAND (Cont'd)

Function	Device	Source	Line
Triple 3 Input NAND Gate (Cont'd.)			
	F4023BM	†Fairchild	
	HD54C10	†Harris	
	HD74C10	Harris	
	SIL4023UB	†Mitel	
	SIL4023UBE	Mitel	
	SIL4023B	†Mitel	
	SIL4023BE	Mitel	140
	MC14023A	†Motorola	
	MC14023C	Motorola	
	MC14023BA	†Motorola	
	MC14023BC	Motorola	
	µPD4023	NEC America	
	CD4023A/BC	National	
	CD4023A/BM	†National	
	MM54C10	†National	
	MM74C10	National	
	CD4023B	†RCA	150
	CD4023BE	RCA	
	CD4023UB	†RCA	
	CD4023UBE	RCA	
	HBF4023AE	SGS	
	SCL4023B	†SSS	
	SCL4023BE	SSS	
	CM4023A	†Solitron	
	CM4023AE	Solitron	
	TP4023A	TI	
	TC4023	Toshiba	160
	TC7410	Toshiba	
Quad 2 Input NAND Gate			
	F4011BC	Fairchild	
	F4011BM	†Fairchild	
	HD54C00	†Harris	
	HD74C00	Harris	
	SIL4011UB	†Mitel	
	SIL4011UBE	Mitel	
	SIL4011B	†Mitel	
	SIL4011BE	Mitel	170
	MC14011A	†Motorola	
	MC14011C	Motorola	
	MC14011BA	†Motorola	
	MC14011BC	Motorola	
	CD4011AC	National	
	CD4011AM	†National	
	CD4011BC	National	
	CD4011BM	†National	
	MM54C00	†National	
	MM74C00	National	180
	µPD4011	NEC America	
	CD4011B	†RCA	
	CD4011BE	RCA	
	CD4011UB	†RCA	
	CD4011UBE	RCA	
	HBF4011AE	SGS	
	SCL4011B	†SSS	
	SCL4011BE	SSS	
	SCL4011UB	†SSS	
	SCL4011UBE	SSS	190
	CM4011	†Solitron	
	CM4011	Solitron	
	TP4011A/B	TI	
	TP4311A	TI	
	TC4011	Toshiba	
	TC7400	Toshiba	

Gates, AND-OR/AND-OR-Invert

Function	Device	Source	Line
Triple AND OR Bi Phase Pairs			
	CD4037B	†RCA	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–CMOS (Cont'd)

Gates, AND-OR/AND-OR-Invert (Cont'd)

Function	Device	Source	Line
Triple AND OR Bi Phase Pairs (Cont'd.)			
	CD4037BE	RCA	
	CM4037A	† Solitron	
	CM4037AE	Solitron	
Quad AND OR Select Gate			
	F4019BC	Fairchild	
	F4019BM	† Fairchild	
	F4519BC	Fairchild	
	F4519BM	† Fairchild	
	SIL4019B	† Mitel	10
	SIL4019BE	Mitel	
	MC14519BA	† Motorola	
	MC14519BC	Motorola	
	CD4019BC	National	
	CD4019BM	† National	
	CD4519BC	National	
	CD4519BM	† National	
	µPD4019	NEC America	
	CD4019B	† RCA	
	CD4019BE	RCA	20
	HBF4019AE	SGS	
	SCL4019B	† SSS	
	SCL4019BE	SSS	
	CM4019A	† Solitron	
	CM4019AE	Solitron	
	TP4019A/B	TI	
	TP4519A/B	TI	
	TC4019	Toshiba	
Quad AND OR Select Gate, Three State			
	CD40257B	† RCA	30
	CD40257BE	RCA	
Dual 2 Wide 2 Input AND OR Invert Gate			
	F4085BC	Fairchild	
	F4085BM	Fairchild	
	SIL4085B	† Mitel	
	SIL4085BE	Mitel	
	MC14506BA	† Motorola	
	MC14506BC	Motorola	
	CD4085B	† RCA	
	CD4085BE	RCA	40
	SCL4085B	† SSS	
4 Wide 2 Input Expandable AND OR Invert Gate			
	F4086BC	Fairchild	
	F4086BM	† Fairchild	
	CD4086B	† RCA	
	CD4086BE	RCA	
	SCL4086B	† SSS	
Quad 4 2 2 1 Input AND OR Invert Gate			
	TP4302A	TI	
Quad 2 4 4 1 Input AND OR Invert Gate			50
	TP4303A	TI	

Gates, Exclusive OR/NOR

Function	Device	Source	Line
Quad Exclusive OR Gate			
	F4030BC	Fairchild	
	F4030BM	† Fairchild	
	F4070BC	Fairchild	
	F4070BM	† Fairchild	
	HD54C86	† Harris	
	HD74C86	Harris	
	SIL4030B	† Mitel	
	SIL4030BE	Mitel	60
	SIL4070B	† Mitel	
	SIL4070BE	Mitel	
	MC14070BA	† Motorola	
	MC14070BC	Motorola	
	(Continued)		

Gates, Exclusive OR/NOR (Cont'd)

Function	Device	Source	Line
Quad Exclusive OR Gate (Cont'd.)			
	CD4030AC	National	
	CD4030AM	† National	
	CD4070BC	National	
	CD4070BM	† National	
	CD4507BC	National	70
	CD4507BM	† National	
	MM54C86	† National	
	MM74C86	National	
	µPD4030	NEC America	
	CD4030B	† RCA	
	CD4030BE	RCA	
	CD4070B	† RCA	
	CD4070BE	RCA	
	HBF4030AE	SGS	
	SCL4030B	† SSS	80
	SCL4030BE	SSS	
	SCL4070B	† SSS	
	SCL4070BE	SSS	
	CM4030A	† Solitron	
	CM4030AE	Solitron	
	CM4070A	† Solitron	
	CM4070AE	Solitron	
	TP4030A	TI	
	TP4507A	TI	
	TC4030	Toshiba	90
Quad Exclusive NOR Gate			
	F4077BC	Fairchild	
	F4077BM	† Fairchild	
	F4519BC	Fairchild	
	F4519BM	† Fairchild	
	SIL4077B	† Mitel	
	SIL4077BE	Mitel	
	MC14077BA	† Motorola	
	MC14077BC	Motorola	
	CD4519BC	National	100
	CD4519BM	† National	
	CD4077B	† RCA	
	CD4077BE	RCA	
	CM4077A	† Solitron	
	CM4077AE	Solitron	
	SCL4077B	† SSS	
	SCL4077BE	SSS	
	TP4519A/B	TI	

Gates, OR/NOR

Function	Device	Source	Line
8 Input OR Gate			
	SIL4978B	† Mitel	110
	SIL4978BE	Mitel	
Dual 4 Input OR Gate			
	F4072BC	Fairchild	
	F4072BM	† Fairchild	
	SIL4072B	† Mitel	
	SIL4072BC	Mitel	
	MC14072BA	† Motorola	
	MC14072BC	Motorola	
	µPD4072	NEC America	
	CD4072B	† RCA	120
	CD4072BE	RCA	
	SCL4072B	† SSS	
	SCL4072BE	SSS	
	TP4072B	TI	
	TC4072	Toshiba	
Triple 3 Input OR Gate			
	F4075BC	Fairchild	
	F4075BM	† Fairchild	
	SIL4075B	† Mitel	
	(Continued)		

Gates, OR/NOR (Cont'd)

Function	Device	Source	Line
Triple 3 Input OR Gate (Cont'd.)			130
	SIL4075BE	Mitel	
	MC14075BA	† Motorola	
	MC14075BC	Motorola	
	CD4075BC	National	
	CD4075BM	† National	
	µPD4075	NEC America	
	CD4075B	† RCA	
	CD4075BE	RCA	
	SCL4075B	† SSS	
	SCL4075BE	SSS	140
	TP4075B	TI	
	TC4075	Toshiba	
Quad 2 Input OR Gate			
	F4071BC	Fairchild	
	F4071BM	† Fairchild	
	HD54C32	† Harris	
	HD74C32	Harris	
	SIL4071B	† Mitel	
	SIL4071BE	Mitel	
	MC14071A	† Motorola	150
	MC14071C	Motorola	
	MC14071BA	† Motorola	
	MC14071BC	Motorola	
	CD4071BC	National	
	CD4071BM	† National	
	MM54C32	† National	
	MM74C32	National	
	µPD4071	NEC America	
	CD4071B	† RCA	
	CD4071BE	RCA	160
	SCL4071B	† SSS	
	SCL4071BE	SSS	
	CM4071A	† Solitron	
	CM4071AE	Solitron	
	TP4071B	TI	
	TC4071	Toshiba	
8 Input NOR Gate			
	F4078BC	Fairchild	
	F4078BM	† Fairchild	
	SIL4078B	† Mitel	170
	SIL4078BE	Mitel	
	MC14078BA	† Motorola	
	MC14078BC	Motorola	
	µPD4078	NEC America	
	CD4078B	† RCA	
	CD4078BE	RCA	
	SCL4078B	† SSS	
	SCL4078BE	SSS	
	SCL4402B	† SSS	
	SCL4402BE	SSS	180
	CM4078A	† Solitron	
	CM4078AE	Solitron	
	TC4078	Toshiba	
Dual 3 Input NOR Gate plus Inverter			
	SIL4000UB	† Mitel	
	SIL4000UBE	Mitel	
	MC14000A	† Motorola	
	MC14000C	Motorola	
	CD4000C	National	
	CD4000M	† National	190
	CD4000B	† RCA	
	CD4000BE	RCA	
	CD4000UB	† RCA	
	CD4000UBE	RCA	
	SCL4000B	† SSS	
	SCL4000BE	SSS	
	CM4000A	Solitron	
	(Continued)		

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–CMOS (Cont'd)

Gates, OR/NOR (Cont'd)

Function	Device	Source	Line
Dual 3 Input NOR Gate plus Inverter (Cont'd.)			
	CM4000AE	Solitron	
	TP4000A	TI	
Dual 4 Input NOR Gate			
	F4002BC	Fairchild	
	F4002BM	† Fairchild	
	SIL4002UB	† Mitel	
	SIL4002UBE	Mitel	
	SIL4002B	† Mitel	
	SIL4002BC	Mitel	10
	MC14002A	† Motorola	
	MC14002C	Motorola	
	MC14002BA	† Motorola	
	MC14002BC	Motorola	
	CD4002AC	National	
	CD4002AM	† National	
	µPD4002	NEC America	
	CD4002B	† RCA	
	CD4002BE	RCA	
	CD4002UB	† RCA	20
	CD4002UBE	RCA	
	HBF4002AE	SGS	
	SCL4002B	† SSS	
	SCL4002BE	SSS	
	CM4002A	† Solitron	
	CM4002AE	Solitron	
	TP4002A	TI	
	TC4002	Toshiba	
Dual 4 Input Expandable NOR Gate			
	SCL4402B	† SSS	30
	SCL4402BE	SSS	
Triple 3 Input NOR Gate			
	F4025BC	Fairchild	
	F4025BM	† Fairchild	
	SIL4025UB	† Mitel	
	SIL4025UBE	Mitel	
	SIL4025B	† Mitel	
	SIL4025BE	Mitel	
	MC14025A	† Motorola	
	MC14025C	Motorola	40
	MC14025BA	† Motorola	
	MC14025BC	Motorola	
	CD4025AC	National	
	CD4025AM	† National	
	CD4025BC	National	
	CD4025BM	† National	
	µPD4025	NEC America	
	CD4025B	† RCA	
	CD4025BE	RCA	
	CD4025UB	† RCA	50
	CD4025UBE	RCA	
	HBF4025AE	SGS	
	SCL4025B	SSS	
	SCL4025BE	SSS	
	CM4025A	Solitron	
	CM4025AE	Solitron	
	TP4025A	TI	
	TC4025	Toshiba	
Quad 2 Input NOR Gate			
	F4001BC	Fairchild	60
	F4001BM	† Fairchild	
	HD54C02	† Harris	
	HD74C02	Harris	
	SIL4001UB	† Mitel	
	SIL4001UBE	Mitel	
	SIL4001B	† Mitel	
	SIL4001BE	Mitel	
	MC14001A	† Motorola	

(Continued)

Gates, OR/NOR (Cont'd)

Function	Device	Source	Line
Quad 2 Input NOR Gate (Cont'd.)			
	MC14001C	Motorola	70
	MC14001BA	† Motorola	
	MC14001BC	Motorola	
	CD4001AC	National	
	CD4001AM	† National	
	CD4001BC	National	
	CD4001BM	† National	
	MM54C02	† National	
	MM74C02	National	
	µPD4001	NEC America	
	CD4001B	† RCA	80
	CD4001BE	RCA	
	CD4001UB	† RCA	
	CD4001UBE	RCA	
	HBF4001AE	SGS	
	SCL4001B	† SSS	
	SCL4001BE	SSS	
	SCL4001UBE	SSS	
	CM4001A	† Solitron	
	CM4001AE	Solitron	
	TP4001A/B	TI	90
	TP4301A/UB	TI	
	TC4001	Toshiba	

Gates, Miscellaneous

Function	Device	Source	Line
8 Input Expandable Multifunction Gate			
	CD4048BC	National	
	CD4048BM	† National	
	CD4048B	† RCA	
	CD4048BE	RCA	
	SCL4048B	† SSS	
	SCL4402B	† SSS	
	SCL4402BE	SSS	100
	CM4048A	† Solitron	
	CM4048AE	Solitron	
Triple Gate (dual 4 input NAND and 2 input OR/NOR)			
	MC14501A	† Motorola	
	MC14501C	Motorola	
	µPD4501	NEC America	
Hex Function Gate			
	MC14572A	† Motorola	
	MC14572C	Motorola	
Dual 5 Input Majority Logic Gate			110
	MC14530BA	† Motorola	
	MC14530BC	Motorola	
	µPD4530	NEC America	

Latches

Function	Device	Source	Line
8 Bit Latch			
	MM54C373	† National	
	MM74C373	National	
8 bit Addressable Latch (Serial In, Parallel Out)			
	F4724BC	Fairchild	
	F4724BM	† Fairchild	
	MC14099BA	† Motorola	120
	MC14099BC	Motorola	
	CD4099BC	National	
	CD4099BM	† National	
	CD4724BC	National	
	CD4724BM	† National	
	µPD4099	NEC America	
	CD4099B	† RCA	
	CD4099BE	RCA	

Latches (Cont'd)

Function	Device	Source	Line
8 bit Addressable Latch, Three State			
	MC14598BA	† Motorola	130
	MC14598BC	Motorola	
8 bit Addressable Latch, Bidirectional Data Port (Serial In/Out and Parallel Out)			
	MC14599BA	† Motorola	
	MC14599BC	Motorola	
8 bit Latch, Counter Input, Three State			
	MC14597BA	† Motorola	
	MC14597BC	Motorola	
Quad Clocked "D" Latch			
	F4042BC	Fairchild	140
	F4042BM	† Fairchild	
	SIL4042B	† Mitel	
	SIL4042BE	Mitel	
	MC14042BA	† Motorola	
	MC14042BC	Motorola	
	CD4042BC	National	
	CD4042BM	† National	
	µPD4042	NEC America	
	CD4042B	† RCA	
	CD4042BE	RCA	150
	HBF4042AE	SGS	
	SCL4042B	† SSS	
	SCL4042BE	SSS	
	CM4042A	† Solitron	
	CM4042AE	Solitron	
	TP4042A/B	TI	
	TC4042	Toshiba	
Quad NAND R/S Latch			
	F4044BC	Fairchild	
	F4044BM	† Fairchild	160
	SIL4044B	† Mitel	
	SIL4044BE	Mitel	
	MC14044BA	† Motorola	
	MC14044BC	Motorola	
	CD4044AC	National	
	CD4044AM	† National	
	µPD4044	NEC America	
	CD4044A/B	† RCA	
	CD4044A/BE	RCA	
	SCL4044A	† SSS	170
	SCL4044AE	SSS	
	CM4044A	† Solitron	
	TP4044A/B	TI	
	TC4044	Toshiba	
Quad NAND Latch			
	TP4376A	TI	
Quad NOR R/S Latch			
	F4043BC	Fairchild	
	F4043BM	† Fairchild	
	SIL4043B	† Mitel	180
	SIL4043BE	Mitel	
	MC14043BA	† Motorola	
	MC14043BC	Motorola	
	CD4043AC	National	
	CD4043AM	† National	
	µPD4043	NEC America	
	CD4043B	† RCA	
	CD4043BE	RCA	
	SCL4043A	† SSS	
	SCL4043AE	SSS	190
	CM4043A	† Solitron	
	CM4043AE	Solitron	
	TP4043A/B	TI	
	TP4078B	TI	
	TC4043	Toshiba	

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–CMOS (Cont'd)

Latches (Cont'd)

Function	Device	Source	Line
Quad NOR Latch	TP4377A	TI	
Dual 4 bit Latch	SIL4508B	† Mitel	
	SIL4508BE	Mitel	
	MC14508BA	† Motorola	
	MC14508BC	Motorola	
	μPD4508	NEC America	
	CD4508B	† RCA	
	CD4508BE	RCA	
	SCL4508B	† SSS	10
	SCL4508BE	SSS	
	CM4508	Solitron	
	TC4508	Toshiba	
Dual 4 bit Addressable Latch	F4723BC	Fairchild	
	F4723BM	† Fairchild	
	CD4723BC	National	
	CD4723BM	National	

Memories

For additional information see Master Selection Guide Memory Sections. — 20

16 bit FIFO (4x4)	CD40105B	† RCA	
	CD40105BE	RCA	
64 bit FIFO (16x4)	F4703BC	Fairchild	
	F4703BM	† Fairchild	
64 bit Program Stack (16x4 LIFO)	F4706BC	Fairchild	
	F4706BM	† Fairchild	
16 bit Multiport Register File (4x4 Read While Write RAM)	MC14580BA	† Motorola	30
	MC14580BC	Motorola	
	CD40108B	† RCA	
	CD40108BE	RCA	
	CD40208B	† RCA	
	CD40208BE	RCA	
64 bit CAM (8x8 Content Addressable Memory)	SCM5533	† SSS	
1,024 bit PROM (256x4)	HM6610	† Harris	40
	HM6611	**† Harris (1184)**	
	HM6612	† Harris	
32 bit RAM (Direct Word Line Addressing)	CD4039A	† RCA	
	CD4039AE	RCA	
	CM4039A	† Solitron	
	CM4039AE	Solitron	
32 bit RAM (Binary Addressing)	CD4036A	† RCA	50
	CD4036AE	RCA	
	CM4036A	† Solitron	
	CM4036AE	† Solitron	
64 bit RAM (64x1)	MCM14505A	† Motorola	
	MCM14505C	Motorola	
64 bit RAM (16x4)	F4725BC	Fairchild	
	F4725BM	† Fairchild	
	HD54C89	† Harris	60
	HD74C89	Harris	

(Continued)

Memories (Cont'd)

Function	Device	Source	Line
64 bit RAM (16x4) (Cont'd.)	**MM54C89**	**† National (1352)**	
	MM74C89	**National (1352)**	
	SCL5589	† SSS	
64 bit RAM (16x4 clocked RAM, three state output register)	F4710BC	Fairchild	
	F4710BM	† Fairchild	
256 bit RAM (256x1)	F4720C	Fairchild	70
	F4720M	† Fairchild	
	F4720AC	Fairchild	
	F4720AM	† Fairchild	
	HD54C200	† Harris	
	HD74C200	Harris	
	IM6523	† Intersil	
	MCM14537	† Motorola	
	MM54C200	**† National (1355)**	
	MM74C200	**National (1355)**	80
	CD4061A	† RCA	
	CD40061	RCA	
	CD40061A	† RCA	
	SCM5520	† SSS	
	TC4061	Toshiba	
256 bit RAM (64x4)	MCM14552	† Motorola	
	MM54C910	**† National (1358)**	
	MM74C910	**National (1358)**	
	SCM5555	SSS	90
256 bit RAM (32x8)	CDP1824	† RCA	
512 bit RAM (512x1)	S2222	AMI	
	S2222A	AMI	
	2222	Nortec	
	2222A	Nortec	
	SCM5522	SSS	
768 bit RAM (64x12)	IM6512	Intersil	100
	IM6512M	† Intersil	
1,024 bit RAM (128x8)	CDP1823S	RCA	
	MWS5080	RCA	
1,024 bit RAM (256x4)	**S5101**	**AMI (1041)**	
	S5101L	AMI	
	F4721BC	Fairchild	
	F4721BM	Fairchild	
	HM6501	**Harris (1174)**	110
	HM6551	**Harris (1175)**	
	HM6552	Harris	
	HM6561	**Harris (1182)**	
	HM6562	**Harris (1183)**	
	5101	Intel	
	M5101	† Intel	
	IM6551	Intersil	
	IM6551M	† Intersil	
	IM6561	Intersil	
	IM6561M	† Intersil	120
	MM54C920	**† National (1361)**	
	MM74C920	**National (1361)**	
	MM54C921	**† National (1361)**	
	MM74C921	**National (1361)**	
	μPD5101	**NEC Micro (1438)**	
	CDP1822S	RCA	
	MWS5040	RCA	

(Continued)

Memories (Cont'd)

Function	Device	Source	Line
1,024 bit RAM (256x4) (Cont'd.)	MWS5540	RCA	
	SCM5501S	† SSS	130
	SY5101	Synertek	
	SY5111	Synertek	
	SY5112	Synertek	
	TC5007	Toshiba	
	TC5017	Toshiba	
1,024 bit RAM (1024x1)	**S6508**	**AMI (1046)**	
	S6508A	**AMI (1046)**	
	F4736BC	Fairchild	
	F4736BM	† Fairchild	140
	HM6508	**Harris (1180)**	
	HM6518	**Harris (1181)**	
	IM6508	† Intersil	
	IM6518	† Intersil	
	SIL1902A	† Mitel	
	SIL1902AE	Mitel	
	MM54C929	**† National (1363)**	
	MM74C929	**National (1363)**	
	MM54C930	**† National (1363)**	
	MM74C930	**National (1363)**	150
	CDP1821S	RCA	
	MWS5001	RCA	
	MWS5501	RCA	
	SCM5502S	† SSS	
	TC5016	Toshiba	
	TC5006	Toshiba	
1,024 bit ROM (256x4)	MCM14524	† Motorola	
	TC5007	Toshiba	
2,048 bit ROM (256x8)	F4735BC	Fairchild	160
	F4735BM	† Fairchild	
2,048 bit ROM (512x8)	CDP1831	† RCA	
	CDP1832	† RCA	
4,096 bit ROM (1024x8)	CDP1833	† RCA	
	CDP1834	† RCA	
12,228 bit ROM(1024x12)	HM6312	Harris	170
	IM6312	Intersil	

Multiplexers, Digital

See also Interface Analog Switches

Quad 2 Input Multiplexer	F4519BC	Fairchild	
	F4519BM	† Fairchild	
	HD54C157	† Harris	
	HD74C157	Harris	
	MC14519BA	† Motorola	
	MC14519BC	Motorola	
	CD4519BC	National	180
	CD4519BM	† National	
	MM54C157	† National	
	MM74C157	National	
	μPD4519	NEC America	
	TP4519A/B	TI	
Dual 4 Channel Digital Multiplexer	F4539BC	Fairchild	
	F4539BM	† Fairchild	
	MC14539BA	† Motorola	
	MC14539BC	Motorola	190

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–CMOS (Cont'd)

Multiplexers, Digital (Cont'd)

Function	Device	Source	Line
Dual 4 Channel Digital Multiplexer (Cont'd.)			
	µPD4539	NEC America	
	TC4539	Toshiba	
8 Channel Data Selector			
	F4512BC	Fairchild	
	F4512BM	† Fairchild	
	SIL4512B	† Mitel	
	SIL4512BE	Mitel	
	MC14512A	† Motorola	
	MC14512C	Motorola	10
	CD4512BC	National	
	CD4512DM	† National	
	µPD4512	NEC America	
	CD4512B	† RCA	
	CD4512BE	RCA	
	SCL4512B	† SSS	
	SCL4512BE	SSS	
	TP4512A/B	TI	
	TC4512	Toshiba	
8 Channel Digital Multiplexer			20
	HD54C151	† Harris	
	HD74C151	Harris	
	MM54C151	† National	
	MM74C151	National	
Dual 8 Channel Digital Multiplexer			
	TP4321A	TI	
16 Channel Digital Multiplexer			
	MM54C150	† National	
	MM74C150	National	
	TP4320A	TI	30
16 Channel Digital Multiplexer, Three State			
	MM72C19	† National	
	MM82C19	National	

Multivibrators

Function	Device	Source	Line
Monostable/Astable Multivibrator			
	F4047BC	Fairchild	
	F4047BM	† Fairchild	
	CD4047BC	National	
	CD4047BM	† National	
	CD4047B	† RCA	
	CD4047BE	RCA	
	CM4047A	† Solitron	
	CM4047AE	Solitron	
	TC4047	Toshiba	
Dual Monostable Multivibrator			
	F4528BC	Fairchild	
	F4528BM	† Fairchild	
	HD54C221	† Harris	
	HD74C221	Harris	
	SIL4098B	† Mitel	
	SIL4098BE	Mitel	
	SIL4528B	† Mitel	50
	SIL4528BE	Mitel	
	MC14528BA	† Motorola	
	MC14528BC	Motorola	
	MC14538BA	† Motorola	
	MC14538BC	Motorola	
	CD4528BC	National	
	CD4528BM	† National	
	MM54C221	† National	
	MM74C221	National	
	µPD4528	NEC America	60
	CD4098B	† RCA	
	CD4098BE	RCA	
	SCL4528B	† SSS	
	(Continued)		

Multivibrators (Cont'd)

Function	Device	Source	Line
Dual Monostable Multivibrator (Cont'd.)			
	SCL4528BE	SSS	
	SCL4538	† SSS	
	TC4528	Toshiba	

Oscillators/Dividers

Function	Device	Source	Line
See also CMOS Counters			
Oscillator/Divider (Programmable Timer)			70
	MC14541BA	† Motorola	
	MC14541BC	Motorola	
Oscillator/Divider (Industrial Timer) with ÷5, ÷6, ÷10, and ÷4096 counters			
	CD22017	RCA	
Oscillator/2^8 Divider (2 5v supplies)			
	ICM7209	Intersil	
Oscillator/2^9 Divider			
	5801	Intel	
	5016	Nortec	80
Oscillator/2^{11} to 2^{19} Divider, with duty cycle control			
	MC14451	Motorola	
Oscillator/2^{13} to 2^{15} Divider (2 5v supplies)			
	UCN-4105	Sprague	
Oscillator/Divider, Mask Programmable for division by 10,000 to 98,000 (Standard divides 3.579 MHz TV crystal to 60 Hz)			
	MM5369	National	
Oscillator/49,152 Divider			
	UCN-1403	Sprague	90
	UCN-1404	Sprague	
Oscillator/2^{16} Divider/Buffer			
	MC14450	Motorola	
	HBC4700	† SGS	
	HBF4700	SGS	
	UCN-4112	Sprague	
	UCN-4113	Sprague	
	SCL5411	SSS	
Oscillator/2^{16} Divider with 2^{13} Output (Supply 1 2v 7038B, 2 5v 7038A)			100
	ICM7038A	Intersil	
	ICM7038B	Intersil	
Oscillator/2^{16} Divider (also 2^{16} x 10, Supply 2 5v)			
	ICM7027	Intersil	
Oscillator/2^{12} and 2^{17} Divider, also 2^{17} x 10 (3 5v supply)			
	ICM7207	Intersil	
Oscillator/2^{13} and 2^{17} Divider (2 3v supplies)			
	UCN-4111	Sprague	
Oscillator/2^{17} Divider (2.5 6v supplies)			110
	MM53107	National	
Oscillator/2^{17} Divider			
	ICM7038D	Intersil	
Oscillator/2^{18} Divider			
	ICM7038E	Intersil	
Oscillator/2^{19} Divider			
	ICM7039G	Intersil	
Oscillator/2^{12} and 2^{20} Divider, also 2^{20}x10 (0.1 and 1 second output with 5.2 MHz crystal, 5v supply)			
	ICM7207A	Intersil	120

Oscillators/Dividers (Cont'd)

Function	Device	Source	Line
Oscillator/2^{12}, 2^{18}, 2^{21}, and 2^{17} Divider (Also 2^{21} x 60, 2 5v supplies)			
	ICM7213	Intersil	
Oscillator/2^{21} Divider/Buffer			
	CD4045A	† RCA	
	CD4045AE	RCA	
	HBF4045AE	SGS	
	SCL4445B	† SSS	
	SCL4445BE	SSS	
	CM4045A	† Solitron	130
	CM4045AE	Solitron	
	UCN-4114	Sprague	
Oscillator/2^{22} Divider (with 1 second and 1 minute pulses using 4.19 MHz crystal, 2 5v supplies)			
	MC14452	Motorola	
Oscillator/2^{23} Divider			
	SCL5419	SSS	
Oscillator/2^{24} Divider			
	MC14521BA	† Motorola	
	MC14521BC	Motorola	140
Oscillator/2^0 to 2^{24} Divider (Programmable Timer)			
	MC14536BA	† Motorola	
	MC14536BC	Motorola	
Frequency Divider (9 Stage)			
	SCL5425A	SSS	
	SCL5427A	SSS	
	SCL5437A	SSS	
Divider, divide by 5/6			
	RED5/6	LSI Comp	
Divider, divide by 6			150
	D6	LSI Comp	
Divider, divide by 50/60			
	RED50/60	LSI Comp	
Divider, divide by 60			
	D60	LSI Comp	
Divider, divide by 3000/3600			
	RED3000/3600	LSI Comp	
Divider, divide by 3600			
	D3600	LSI Comp	

Shift Registers

Function	Device	Source	Line
4 bit Parallel In/Parallel Out Shift Register			160
	F4035BC	Fairchild	
	F4035BM	† Fairchild	
	SIL4035B	† Mitel	
	SIL4035BE	Mitel	
	MC14035BA	† Motorola	
	MC14035BC	Motorola	
	CD4035BC	National	
	CD4035BM	† National	
	µPD4035	NEC America	
	CD4035B	† RCA	170
	CD4035BE	RCA	
	HBF4035AE	SGS	
	SCL4035B	† SSS	
	SCL4035BE	SSS	
	CM4035A	† Solitron	
	CM4035AE	Solitron	
	TP4035B	TI	
	TC4035	Toshiba	
4 bit Parallel Shift Register			
	F40195BC	Fairchild	180
	F40195BM	† Fairchild	
	HD54C195	† Harris	
	(Continued)		

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–CMOS (Cont'd)

Function	Device	Source	Line
Shift Registers (Cont'd)			
4 bit Parallel Shift Register (Cont'd.)			
	HD74C195	Harris	
	MM54C195	† National	
	MM74C195	National	
4 bit Bidirectional Shift Register			
	F40194BC	Fairchild	
	F40194BM	† Fairchild	
	HD54C95	† Harris	
	HD74C95	Harris	
	MC14194BA	† Motorola	10
	MC14194BC	Motorola	
	MM54C95	National	
	MM74C95	† National	
	µPD4194	NEC America	
	CD40194B	† RCA	
	CD4019BE	RCA	
4 bit Bidirectional Shift Register, Three State			
	CD40104B	† RCA	
	CD40104BE	RCA	
Dual 4 bit Serial In/Parallel Out Shift Register			20
	F4015BC	Fairchild	
	F4015BM	† Fairchild	
	SIL4015B	† Mitel	
	SIL4015BE	Mitel	
	MC14015BA	† Motorola	
	MC14015BC	Motorola	
	CD4015AC	National	
	CD4015AM	† National	
	µPD4015	NEC America	
	CD4015B	† RCA	30
	CD4015BE	RCA	
	HBF4015AE	SGS	
	SCL4015B	† SSS	
	SCL4015BE	SSS	
	CM4015A	† Solitron	
	CM4015AE	Solitron	
	TP4015A/B	TI	
	TC4015	Toshiba	
8 bit Synchronous Parallel In/Serial Out Shift Register			
	F4014BC	Fairchild	40
	F4014BM	† Fairchild	
	SIL4014B	† Mitel	
	SIL4014BE	Mitel	
	MC14014BA	† Motorola	
	MC14014BC	Motorola	
	CD4014AC	National	
	CD4014AM	† National	
	µPD4014	NEC America	
	CD4014B	† RCA	
	CD4014BE	RCA	50
	HBF4014AE	SGS	
	SCL4014B	† SSS	
	SCL4014BE	SSS	
	CM4014A	† Solitron	
	CM4014AE	Solitron	
	TP4014A	TI	
	TC4014	Toshiba	
8 bit (Asynchronous parallel or synchronous serial operation) Parallel In/Serial Out Shift Register			
	F4021BC	Fairchild	60
	F4021BM	† Fairchild	
	SIL4021B	† Mitel	
	SIL4021BE	Mitel	
	MC14021BA	† Motorola	
	MC14021BC	Motorola	
	CD4021AC	National	
	CD4021AM	† National	
(Continued)			

Function	Device	Source	Line
Shift Registers (Cont'd)			
8 bit (Asynchronous parallel or synchronous serial operation) Parallel In/Serial Out Shift Register (Cont'd.)			
	µPD4021	NEC America	70
	CD4021B	† RCA	
	CD4021BE	RCA	
	SCL4021B	† SSS	
	SCL4021BE	SSS	
	CM4021A	† Solitron	
	CM4021AE	Solitron	
	TP4021A	TI	
	TC4021	Toshiba	
8 bit Serial In/Parallel Out Shift Register			
	HD54C164	† Harris	80
	HD74C164	Harris	
	MM54C164	† National	
	MM74C164	National	
8 bit Parallel In/Serial Out Shift Register			
	HD54C165	† Harris	
	HD74C165	Harris	
	MM54C165	† National	
	MM74C165	National	
8 bit Bidirectional Parallel/Serial Input/Output Bus Register			90
	F4034BC	Fairchild	
	F4034BM	† Fairchild	
	MC14034BA	† Motorola	
	MC14034BC	Motorola	
	CD4034BC	National	
	CD4034BM	† National	
	µPD4034	NEC America	
	SCL4034B	† SSS	
	SCL4034BE	SSS	
	CM4034A	† Solitron	100
	CM4034AE	Solitron	
	CD4034B	† RCA	
	CD4034BE	RCA	
	TC4034	Toshiba	
8 bit Bus Register, Shift and Store			
	MC14094BA	† Motorola	
	MC14094BC	Motorola	
	µPD4094	NEC America	
	CD4094B	† RCA	
	CD4094BE	RCA	110
	SCL4094B	† SSS	
	SCL4094BE	SSS	
	SCL4494B	† SSS	
18 bit Static Shift Register			
	MS612	RTC	
18 bit Static Shift Register (4, 5, 8, 9, 10, 12, 13, 14, 16, 17, 18 bits)			
	F4006BC	Fairchild	
	F4006BM	† Fairchild	
	MC14006BA	† Motorola	120
	MC14006BC	Motorola	
	CD4006AC	National	
	CD4006AM	† National	
	µPD4006	NEC America	
	CD4006B	† RCA	
	CD4006BE	RCA	
	SCL4006B	† SSS	
	SCL4006BE	SSS	
	CM4006A	† Solitron	
	CM4006AE	Solitron	130
30 bit Static Shift Register			
	MD4330B	† Mitel	
	MD4330BE	Mitel	

Function	Device	Source	Line
Shift Registers (Cont'd)			
Dual 16 bit Static Shift Register			
	HSSR0321	† Hughes	
	HSSR0351	† Hughes	
32 bit Bidirectional Serial In/Serial Out Shift Register			
	CD40100B	† RCA	
	CD40100BE	RCA	
64 bit Static Shift Register			140
	F4031BC	Fairchild	
	F4031BM	† Fairchild	
	CD4031BC	National	
	CD4031BM	† National	
	µPD4517	NEC America	
	CD4031B	† RCA	
	CD4031BE	RCA	
Dual 64 bit Static Shift Register			
	MC14517BA	† Motorola	
	MC14517BC	Motorola	150
	SCL4517B	SSS	
128 bit Static Shift Register (16 bit increments)			
	MC14562BA	† Motorola	
	MC14562BC	Motorola	
200 bit Dynamic Shift Register			
	CD4062A	† RCA	
	CD4062AE	RCA	
Quad 64 bit Static Shift Register, Separate Clock			
	F4731BC	Fairchild	
	F4731BM	† Fairchild	160
64 bit Variable Length Shift Register			
	F4557BC	† Fairchild	
	F4557BM	Fairchild	
	MC14557BA	† Motorola	
	MC14557BC	Motorola	
96 bit Variable Length Elastic Shift Register			
	MS618	† RTC	
128 bit Static Shift Register, W/Control Logic			
	MS625	† RTC	
Translators			
Quad Voltage Up Level Translator			170
	F4104BE	Fairchild	
	F4104BM	† Fairchild	
Quad Level Shifter (low to high voltage)			
	CD40109B	† RCA	
	CD40109BE	RCA	
Hex TTL Buffer (Inverting) (CMOS To TTL)			
	HD54C901	† Harris	
	HD74C901	Harris	
	MM54C901	† National	
	MM74C901	National	180
Hex TTL Buffer (Non Inverting) (CMOS To TTL)			
	HD54C902	† Harris	
	HD74C902	Harris	
	MM54C902	† National	
	MM74C902	National	
Hex PMOS Buffer (inverting) (PMOS To CMOS or TTL)			
	HD54C903	† Harris	
	HD74C903	Harris	
	MM54C903	† National	190
	MM74C903	National	
Hex PMOS Buffer (Non Inverting) (PMOS To CMOS or TTL)			
	HD54C904	† Harris	
	HD74C904	Harris	
(Continued)			

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–CMOS (Cont'd)

Function	Device	Source	Line
Translators (Cont'd)			
Hex PMOS Buffer (Non Inverting) (PMOS To CMOS or TTL) (Cont'd.)			
	MM54C904	† National	
	MM74C904	National	
HNIL/HTL is suitable for translation/input protection. See HNIL/HTL section			
Miscellaneous			
Microprocessor, 1 bit, Industrial Control Unit			
	MC14500B	Motorola	
Phase Locked Loop			
	F4046BC	Fairchild	10
	F4046BM	† Fairchild	
	SIL4046B	† Mitel	
	SIL4046BE	Mitel	
	MC14046BA	† Motorola	
	MC14046BC	Motorola	
	CD4046BC	National	
	CD4046BM	† National	
	CD4046B	† RCA	
	CD4046BE	RCA	
	SCL4046A	† SSS	
	SCL4046AE	SSS	
	SCL4446	SSS	
CMOS Transistor Array (See also 4007 Dual Complementary Pair and Inverter listed under Buffers/Inverters)			
	CA3600E	† RCA	
Hex Contact Bounce Eliminator			
	MC14490	Motorola	
	MC14490E	† Motorola	
8 bit Priority Encoder			
	F4532BC	Fairchild	
	F4532BM	† Fairchild	
	MC14532BA	† Motorola	
	MC14532BC	Motorola	
	μPD4532	NEC America	
	CD4532B	† RCA	
	CD4532BE	RCA	
	TC4532	Toshiba	
Binary Rate Multiplier			
	CD4089BC	National	
	CD4089BM	† National	
	CD4089B	† RCA	
	CD4089BE	RCA	
BCD Rate Multiplier			
	MC14527BA	† Motorola	
	MC14527BC	Motorola	
	CD4527BC	National	
	CD4527BM	† National	
	CD4527B	† RCA	
	CD4527BE	RCA	
	SCL4527B	† SSS	
	SCL4527BE	SSS	
	MM74C909	National	
Bit Rate Generator			
	F4702BC	Fairchild	
	F4702BM	† Fairchild	
	HD4702-2	**Harris**	**(1634)**
	HD4702-9	**† Harris**	**(1634)**
	HD6405-2	**Harris**	**(1634)**
	HD6405-9	**† Harris**	**(1634)**
	MC14411	Motorola	
Comparator, Linear, Quad			
	HD54C909	† Harris	
	(Continued)		

Function	Device	Source	Line
Miscellaneous (Cont'd)			
Comparator, Linear, Quad (Cont'd.)			
	HD74C909	Harris	
	MM54C909	† National	
Dual Differential Line Driver			
	HD88C30	Harris	
	MM78C30	† National	
	MM88C30	National	
Quad Single Ended Line Driver			
	HD88C29	Harris	
	MM78C29	† National	
	MM88C29	National	
Dual Line Receiver			
	MM78C20	† National	
	MM88C20	National	
Successive Approximation Register			
	HD54C905	† Harris	
	HD74C905	Harris	
	MC14559BA	† Motorola	
	MC14559BC	Motorola	
	MM54C905	† National	
	MM74C905	National	
Successive Approximation Register, Cascadable			
	MC14549BA	† Motorola	
	MC14549BC	Motorola	
Digital Logic (for 3 1/2 digit A/D Systems)			
	MC14435	Motorola	
	MC14435E	† Motorola	
Phase Comparator and Programmable Counters			
	MC14568BA	† Motorola	
	MC14568BC	Motorola	
Synthesizer (Programmable Divider)			
	CRC8100	Rockwell	
Synthesizers, see Linear Phase Locked Loop Circuits			
9 bit Parity Generator and Checker			
	CD40101B	† RCA	
	CD40101BE	RCA	
12 bit Parity Tree			
	F4531BC	Fairchild	
	F4531BM	† Fairchild	
	MC14531BA	† Motorola	
	MC14531BC	Motorola	
	SCL4531B	SSS	
	TP4531A	TI	
Dual Schmitt Trigger			
	F4583BC	Fairchild	
	F4583BM	† Fairchild	
	MC14583BA	† Motorola	
	MC14583BC	Motorola	
	TC4583	Toshiba	
Hex Schmitt Trigger			
	F40014BC	Fairchild	
	F40014AM	† Fairchild	
	HD54C14	† Harris	
	HD74C14	Harris	
	HD54C914	† Harris	
	HD74C914	Harris	
	MC14584BA	† Motorola	
	MC14584BC	Motorola	
	CD40106BC	National	
	CD40106BM	† National	
	CD4584BC	National	
	CD4584BM	† National	
	MM54C14	† National	
	MM74C14	National	
	(Continued)		

Function	Device	Source	Line
Miscellaneous (Cont'd)			
Hex Schmitt Trigger (Cont'd.)			
	MM54C914	† National	
	MM74C914	National	
	μPD4584	NEC America	
	CD40106B	† RCA	
	CD40106BE	RCA	
	SCL4584B	SSS	
	TP4304A	TI	
Quad 2 Input NAND Schmitt Trigger			
	F4093BC	† Fairchild	
	F4093BM	Fairchild	
	MC14093BA	† Motorola	
	MC14093BC	Motorola	
	CD4093BC	National	
	CD4093BM	† National	
	μPD4093	NEC America	
	CD4093B	† RCA	
	CD4093BE	RCA	
	SCL4093B	† SSS	
	SCL4093BE	SSS	
Binary to Phone Pulse Converter			
	MC14408	Motorola	
	MC14409	Motorola	
Modem (0 600 bps)			
	MC14412	Motorola	
Remote Control Transmitter (see also Linear Consumer Circuits, TV Remote Control)			
	MC14422	Motorola	
Tone Encoder (4x4 Input, 2 Outputs)			
	MC14410	Motorola	
2 of 8 Keyboard to Binary Encoder			
	MC14419	Motorola	
Programmable Timer			
	MC14536BA	† Motorola	
	MC14536BC	Motorola	
	MC14541BA	† Motorola	
	MC14541BC	Motorola	
DN			
	MD4301A	Mitel	
Quad Precision Timer/Driver (Inputs cause outputs to switch state for 100 clock pulses)			
	MC14415	Motorola	
	MC14415E	† Motorola	
Standardized CMOS Array, to build custom circuits by changing final metalization			
	MASTERMOS	IMI	
	MonochipM	Interdesign	
	ML200	Master Logic	
Low voltage CMOS devices (Counters, Display Drivers, Counter Timers) not usually mixed with 5 20v CMOS logic are listed under Digital Special or CMOS Oscillators/Dividers			

† Military Temperature Range (−55° to 125°C)

* Typical Values

IC MASTER

DIGITAL–ECL

ECL-10000 Series

Arithmetic Functions

The ECL 10000, 95000, 100K and III Other Series are presented as separate groups in that sequence.

Function	Device	Source	Line
Dual High Speed Adder/Subtractor	F10180	Fairchild	
	F10580	† Fairchild	
	HD10180	Hitachi	
	MC10180	Motorola	
	MC10580	† Motorola	
	μPB10180	NEC America	
	SP10180	Plessey	10
	10180	Signetics	
2 bit Arithmetic Logic Unit/Function Generator	MC10182	Motorola	
4 bit Arithmetic Logic Unit/Function Generator	F10181	Fairchild	
	F10581	† Fairchild	
	HD10181	Hitachi	
	MC10181	Motorola	
	MC10581	† Motorola	
	μPB10181	NEC America	20
	SP10181	Plessey	
	10181	Signetics	
4 bit ALU Slice (Microprocessor)	MC10800	Motorola	
2 bit Multiplier, High Speed	MC10287	Motorola	
4x2 bit Multiplier	MC10183	Motorola	
Look ahead Carry Circuit	F10179	Fairchild	
	F10579	† Fairchild	
	HD10179	Hitachi	
	MC10179	Motorola	
	MC10579	† Motorola	
	SP10179	Plessey	
	10179	Signetics	
5 bit Comparator	F10166	Fairchild	30
	F10566	† Fairchild	
	MC10166	Motorola	

Buffers

Function	Device	Source	Line
Hex Buffer	10188	Signetics	
Hex Inverter	10189	Signetics	
Hex Inverter/Buffer	MC10195	Motorola	

Counters, Binary

Function	Device	Source	Line
4 bit Binary Counter	F10016C	Fairchild	
	F10016M	† Fairchild	
	MC10178	Motorola	50
	SP10178	Plessey	
4 bit Universal Binary Counter	F10136	Fairchild	
	F10536	† Fairchild	
	HD10136	Hitachi	
	MC10136	Motorola	
	MC10536	† Motorola	
	μPB10136	NEC America	
	SP10136	Plessey	
(Cont'd.)	SP10536	† Plessey	60

Counters, Binary (Cont'd)

Function	Device	Source	Line
4 bit Universal Binary Counter (Cont'd.)	10136	Signetics	

Counters, Decade

Function	Device	Source	Line
Bi Quinary Counter	MC10138	Motorola	
	SP10138	Plessey	
Decade Counter	F10010C	Fairchild	
	F10010M	† Fairchild	
Universal Decade Counter	F10137	Fairchild	70
	MC10137	Motorola	
	MC10537	† Motorola	
	SP10137	Plessey	
	SP10537	† Plessey	
	10137	Signetics	

Decoders

Function	Device	Source	Line
Binary to 1 8 Decoder (High)	F10162	Fairchild	
	F10562	† Fairchild	
	HD10162	Hitachi	
	MC10162	Motorola	80
	MC10562	† Motorola	
	μPB10162	NEC America	
	SP10162	Plessey	
	10162	Signetics	
Binary to 1 8 Decoder (Low)	F10161	Fairchild	
	F10561	† Fairchild	
	HD10161	Hitachi	
	MC10161	Motorola	
	MC10561	† Motorola	90
	μPB10161	NEC America	
	SP10161	Plessey	
	10161	Signetics	
Dual Binary to 1 4 Decoder (High)	F10172	Fairchild	
	F10572	† Fairchild	
	MC10172	Motorola	
	MC10572	† Motorola	
	SP10172	Plessey	
	10172	Signetics	100
Dual Binary to 1 4 Decoder (Low)	F10171	Fairchild	
	F10571	† Fairchild	
	MC10171	Motorola	
	MC10571	† Motorola	
	SP10171	Plessey	
	10171	Signetics	

Drivers

Function	Device	Source	Line
Dual TTL/MST Bus Driver	MC10128	Motorola	
	SP10128	Plessey	110
Triple 4 3 3 Input Bus Driver	F10123	Fairchild	
	F10523	† Fairchild	
	MC10123	Motorola	
	SP10123	Plessey	
	10123	Signetics	

Drivers (Cont'd)

Function	Device	Source	Line
Quad Bus Driver	F10192	Fairchild	
	10192	Signetics	

Flip-Flops

Function	Device	Source	Line
Dual "D" Master Slave Flip Flop	F10131	Fairchild	120
	F10231	Fairchild	
	F10531	† Fairchild	
	F10631	† Fairchild	
	HD10131	Hitachi	
	MC10131	Motorola	
	MC10231	Motorola	
	MC10531	† Motorola	
	MC10631	† Motorola	
	μPB10131	NEC America	130
	SP10131	Plessey	
	SP10231	Plessey	
	SP10531	† Plessey	
	10131	Signetics	
	10231	Signetics	
Hex "D" Master Slave Flip Flop	F10176	Fairchild	
	F10576	† Fairchild	
	MC10176	Motorola	
	MC10576	† Motorola	140
	μPB10176	NEC America	
	SP10176	Plessey	
	10176	Signetics	
Hex "D" Master Slave Flip Flop (With Common Reset)	F10186	Fairchild	
	F10586	† Fairchild	
	MC10186	Motorola	
Dual "J &K" Master Slave Flip Flop	F10135	Fairchild	
	F10535	† Fairchild	150
	MC10135	Motorola	
	MC10535	† Motorola	
	μPB10135	NEC America	
	SP10135	Plessey	
	SP10535	† Plessey	
	10135	Signetics	

Gates, AND/NAND

Function	Device	Source	Line
Hex AND Gate	MC10197	Motorola	
Dual 4 Input AND/NAND Gate	10108	Signetics	160
Quad 2 Input Gate (3 AND, 1 AND/NAND)	F10104	Fairchild	
	F10504	† Fairchild	
	HD10104	Hitachi	
	MC10104	Motorola	
	MC10504	† Motorola	
	SP10104	Plessey	
	SP10504	† Plessey	
	10104	Signetics	

Gates, Exclusive OR/NOR

Function	Device	Source	Line
Quad Exclusive OR Gate	F10113	Fairchild	170
	F10513	† Fairchild	
	MC10113	Motorola	
	SP10113	Plessey	
	10113	Signetics	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–ECL (Cont'd)

Gates, Exclusive OR/NOR (Cont'd)

Function	Device	Source	Line
Triple 2 Input Exclusive OR/NOR Gate			
	F10107	Fairchild	
	F10507	† Fairchild	
	HD10107	Hitachi	
	MC10107	Motorola	
	MC10507	† Motorola	
	μPB10107	NEC America	
	SP10107	Plessey	
	SP10507	† Plessey	
	10107	Signetics	

Gates, OR/NOR

Function	Device	Source	Line
Dual 3 Input 3 Output OR Gate (Line Driver)			
	F10110	Fairchild	
	F10210	Fairchild	
	F10510	† Fairchild	
	F10610	† Fairchild	
	HD10110	Hitachi	
	MC10110	Motorola	
	MC10210	Motorola	
	μPB10110	NEC America	
	SP10110	Plessey	20
	SP10210	Plessey	
	10110	Signetics	
Dual 3 Input 3 Output NOR Gate (Line Driver)			
	F10111	Fairchild	
	F10211	Fairchild	
	F10511	† Fairchild	
	F10611	† Fairchild	
	HD10111	Hitachi	
	MC10111	Motorola	
	DM10111	National	30
	μPB10111	NEC America	
	SP10111	Plessey	
	SP10211	Plessey	
	10111	Signetics	
	10211	Signetics	
Triple 4 3 3 Input NOR Gate			
	F10106	Fairchild	
	F10506	† Fairchild	
	HD10106	Hitachi	
	MC10106	Motorola	40
	MC10506	† Motorola	
	DM10106	National	
	μPB10106	NEC America	
	SP10106	Plessey	
	SP10506	† Plessey	
	10106	Signetics	
Quad 3 Input NOR Gate (One Input Common)			
	F10100	Fairchild	
	MC10100	Motorola	
	μPB10100	NEC America	50
	SP10100	Plessey	
	10100	Signetics	
Dual 3 Input 3 Output (1 OR, 2 NOR) Gate (Line Driver)			
	F10212	Fairchild	
	F10612	† Fairchild	
	MC10212	Motorola	
	DM10112	National	
	SP10112	Plessey	
	SP10212	Plessey	60
	10112	Signetics	
Dual 4 5 Input OR/NOR Gate			
	F10109	Fairchild	
	F10509	† Fairchild	
	HD10109	Hitachi	

(Continued)

Gates, OR/NOR (Cont'd)

Function	Device	Source	Line
Dual 4 5 Input OR/NOR Gate (Cont'd.)			
	MC10109	Motorola	
	MC10509	† Motorola	
	DM10109	National	
	μPB10109	NEC America	70
	SP10109	Plessey	
	10109	Signetics	
Triple 2 3 2 Input OR/NOR Gate			
	F10105	Fairchild	
	F10505	† Fairchild	
	HD10105	Hitachi	
	MC10105	Motorola	
	MC10505	† Motorola	
	DM10105	National	
	μPB10105	NEC America	80
	SP10105	Plessey	
	SP10505	† Plessey	
	10105	Signetics	
Quad 2 Input OR/NOR Gate (One Input Common)			
	F10101	Fairchild	
	F10501	† Fairchild	
	HD10101	Hitachi	
	MC10101	Motorola	
	MC10501	† Motorola	
	μPB10101	NEC America	90
	SP10101	Plessey	
	SP10501	† Plessey	
	10101	Signetics	
Quad 2 Input Gate (3 OR, 1 OR/NOR)			
	F10103	Fairchild	
	F10503	† Fairchild	
	MC10103	Motorola	
	μPB10103	NEC America	
	SP10103	Plessey	
	10103	Signetics	100
Quad 2 Input Gate (3 NOR, 1 OR/NOR)			
	F10102	Fairchild	
	F10502	† Fairchild	
	HD10102	Hitachi	
	MC10102	Motorola	
	MC10502	† Motorola	
	μPB10105	NEC America	
	SP10102	Plessey	
	SP10502	† Plessey	
	10102	Signetics	110

Gates, OR-AND/OR-AND-Invert

Function	Device	Source	Line
4 Wide 4 3 3 3 Input OR AND Gate			
	F10119	Fairchild	
	F10519	† Fairchild	
	HD10119	Hitachi	
	MC10119	Motorola	
	MC10519	† Motorola	
	DM10119	National	
	SP10119	Plessey	
	SP10519	† Plessey	
	10119	Signetics	120
Dual 2 Wide 3 Input OR AND Gate			
	F10118	Fairchild	
	F10518	† Fairchild	
	HD10118	Hitachi	
	MC10118	Motorola	
	MC10518	† Motorola	
	DM10118	National	
	μPB10118	NEC America	
	SP10118	Plessey	

(Continued)

Gates, OR-AND/OR-AND-Invert (Cont'd)

Function	Device	Source	Line
Dual 2 Wide 3 Input OR AND Gate (Cont'd.)			
	SP10518	† Plessey	130
	10118	Signetics	
4 Wide 3 Input OR AND/OR AND Invert Gate			
	F10121	Fairchild	
	F10521	† Fairchild	
	HD10121	Hitachi	
	MC10121	Motorola	
	MC10521	† Motorola	
	DM10121	National	
	SP10121	Plessey	140
	SP10521	† Plessey	
	10121	Signetics	
Dual 2 Wide 2 3 Input OR AND/OR AND Invert Gate			
	F10117	Fairchild	
	F10517	† Fairchild	
	HD10117	Hitachi	
	MC10117	Motorola	
	MC10517	† Motorola	
	DM10117	National	
	μPB10117	NEC America	150
	SP10117	Plessey	
	SP10517	† Plessey	
	10117	Signetics	

Latches

Function	Device	Source	Line
Dual "D" Clocked Latch			
	F10130	Fairchild	
	F10530	† Fairchild	
	HD10130	Hitachi	
	MC10130	Motorola	
	MC10530	† Motorola	
	SP10130	Plessey	160
	10130	Signetics	
Quad "D" Latch, Gated Output; Active High Enable			
	F10133	Fairchild	
	F10533	† Fairchild	
	HD10133	Hitachi	
	MC10133	Motorola	
	MC10533	† Motorola	
	μPB10133	NEC America	
	SP10133	Plessey	
	SP10533	† Plessey	170
	10133	Signetics	
Quad "D" Latch, Gated Output; Active Low Enable			
	F10153	Fairchild	
	F10553	† Fairchild	
	MC10153	Motorola	
Quad Latch, Common Clock, Separate Output Enable			
	F10168	Fairchild	
	F10568	† Fairchild	
	MC10168	Motorola	
Quint Latch			180
	F10175	Fairchild	
	F10575	† Fairchild	
	HD10175	Hitachi	
	MC10175	Motorola	
	MC10575	† Motorola	
	μPB10175	NEC America	
	SP10175	Plessey	
	10175	Signetics	
Dual 2 to 1 Multiplexer Latch, Common Reset			
	F10132	Fairchild	190
	F10532	† Fairchild	
	HD10132	Hitachi	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

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DIGITAL–ECL (Cont'd)

Function	Device	Source	Line
Latches (Cont'd)			
Dual 2 to 1 Multiplexer Latch, Common Reset (Cont'd.)	MC10132	Motorola	
	10132	Signetics	
Dual 2 to 1 Multiplexer Latch	F10134	Fairchild	
	F10534	† Fairchild	
	HD10134	Hitachi	
	MC10134	Motorola	
	SP10134	Plessey	
	10134	Signetics	10
Quad 2 Input Multiplexer Latch	F10173	Fairchild	
	F10573	† Fairchild	
	MC10173	Motorola	
	10173	Signetics	
	SP10173	Plessey	
Memories			
For additional information, see Master Selection Guide Memory sections			
CAM (16 bit Content Addressable Memory)	10155	Signetics	20
RAM (8x2) Simultaneous Read Write	MCM10143	Motorola	
RAM (16x1)	HM2101	Hitachi	
RAM (16x4)	F10145AC	Fairchild	
	HD10145	Hitachi	
	MCM10145	Motorola	
	SP10145	Plessey	
	10145	Signetics	30
RAM (64x1)	μPB10142	NEC America	
	SP10142	Plessey	
	10142	Signetics	
	SN10142	TI	
RAM (64x1) 50 Ohm Drive	HD10148	Hitachi	
	μPB10148	NEC America	
	SP10148	Plessey	
	10148	Signetics	40
	SN10148	TI	
RAM (64x1) 90 Ohm Drive	SP10140	Plessey	
	10140	Signetics	
	SN10140	TI	
RAM (64x1) Read while Write	10151	Signetics	
RAM (128x1)	F10405C	Fairchild	
	MB7047	Fujitsu	50
	MCM10147	Motorola	
	SN10147	TI	
RAM (256x1)	F10410C	Fairchild	
	F10411C	Fairchild	
	MBM10410	Fujitsu	
	MB7042	Fujitsu	
	HM2104	Hitachi	
	HM2105	Hitachi	
	MCM10144	Motorola	60
	MCM10152	Motorola	
(Continued)			

Function	Device	Source	Line
Memories (Cont'd)			
RAM (256x1) (Cont'd.)	μPB10144	NEC America	
	SP10144	Plessey	
	10144	Signetics	
	RC10144	Raytheon	
	RI10144	Raytheon	
	SN10144	TI	
RAM (1024x1)	**F10415**	**Fairchild (1128)**	70
	F10415A	**Fairchild (1128)**	
	F100415A	**Fairchild (1128)**	
	MCM10146	Motorola	
	MCM10415A	Motorola	
	MBM10415	Fujitsu	
	MBM10415A	Fujitsu	
PROM (32x8)	MCM10139	Motorola	
	10139	Signetics	
PROM (256x4)	F10416	Fairchild	80
	MCM10149	Motorola	
	GXB10149	Siemens	
	10149	Signetics	
Multivibrators			
Monostable Multivibrator	MC10198	Motorola	
Multiplexers			
8 to 1 Multiplexer	F10164	Fairchild	
	F10564	† Fairchild	
	HD10164	Hitachi	90
	MC10164	Motorola	
	MC10564	† Motorola	
	μPB10164	NEC America	
	SP10164	Plessey	
	10164	Signetics	
	SN10164	TI	
Dual 4 to 1 Multiplexer	F10174	Fairchild	
	F10574	† Fairchild	
	HD10174	Hitachi	100
	MC10174	Motorola	
	μPB10174	NEC America	
	SP10174	Plessey	
	10174	Signetics	
	SN10174	TI	
	MC10574	† Motorola	
Quad 2 to 1 Multiplexer (Non Inverting)	F10158	Fairchild	
	F10558	† Fairchild	
	MC10158	Motorola	110
	μPB10158	NEC America	
	10158	Signetics	
Quad 2 to 1 Multiplexer (Inverting With Enable)	F10159	Fairchild	
	F10559	† Fairchild	
	MC10159	Motorola	
	10159	Signetics	
Shift Registers			
4 bit Shift Register	F10000C	Fairchild	
(Continued)			

Function	Device	Source	Line
Shift Registers (Cont'd)			
4 bit Shift Register (Cont'd.)	F10000M	† Fairchild	120
4 bit Universal Shift Register	F10141	Fairchild	
	F10541	† Fairchild	
	MC10141	Motorola	
	MC10541	† Motorola	
	SP10141	Plessey	
	10141	Signetics	
Translators			
Dual ECL to MOS/TTL Translator	MC75358	Motorola	130
	MC75368	Motorola	
Triple ECL to NMOS Translator	MC10177	Motorola	
	F10177	Fairchild	
Hex ECL to MST Translator	MC10191	Motorola	
	10191	Signetics	
Quad ECL to TTL Translator (Differential Input)	F10125	Fairchild	
	F10525	† Fairchild	140
	HD10125	Hitachi	
	MC10125	Motorola	
	MC10525	† Motorola	
	μPB10125	NEC America	
	SP10125	Plessey	
	SP10525	† Plessey	
	10125	Signetics	
Quad Differential Receiver/MST to ECL Translator	MC10190	Motorola	
	10190	Signetics	150
Quad TTL to ECL OR/NOR Translator	F10124	Fairchild	
	F10524	† Fairchild	
	HD10124	Hitachi	
	MC10124	Motorola	
	MC10524	† Motorola	
	DM10124	National	
	μPB10124	NEC America	
	SP10124	Plessey	
	SP10524	† Plessey	160
	10124	Signetics	
Miscellaneous			
Triple Differential Line Receiver	F10114	Fairchild	
	F10116	Fairchild	
	F10514	† Fairchild	
	F10516	† Fairchild	
	HD10116	Hitachi	
	MC10114	Motorola	
	MC10116	Motorola	
	MC10216	Motorola	170
	MC10514	† Motorola	
	MC10516	† Motorola	
	MC10616	† Motorola	
	DM10116	National	
	SP10114	Plessey	
	SP10116	Plessey	
	SP10216	Plessey	
	SP10514	† Plessey	
	SP10516	† Plessey	
	10114	Signetics	180
(Continued)			

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–ECL (Cont'd)

Miscellaneous (Cont'd)

Triple Differential Line Receiver (Cont'd.)

Device	Source
10116	Signetics
10216	Signetics

Quad Differential Line Receiver

Device	Source
F10115	Fairchild
F10515	† Fairchild
MC10115	Motorola
MC10515	† Motorola
DM10115	National
μPB10115	NEC America
SP10115	Plessey
SP10515	† Plessey
10115	Signetics

Quad Bus Receiver

Device	Source
MC10129	Motorola
SP10129	Plessey
10129	Signetics

Dual Simultaneous Bus Transceiver

Device	Source
MC10194	Motorola

8 Input Priority Encoder

Device	Source
F10165	Fairchild
F10565	† Fairchild
HD10165	Hitachi
MC10165	Motorola
SP10165	Plessey
10165	Signetics

9 bit Parity Circuit (2 Carry Inputs)

Device	Source
F10170	Fairchild
F10570	† Fairchild
MC10170	Motorola
μPB10170	NEC America
10170	Signetics

12 bit Parity Generator/Checker

Device	Source
F10160	Fairchild
F10560	† Fairchild
HD10160	Hitachi
MC10160	Motorola
MC10560	† Motorola
μPB10160	NEC America
SP10160	Plessey
10160	Signetics

Error Detection/Correction Circuit

Device	Source
MC10163	Motorola
MC10193	Motorola

Active Terminator

Device	Source
F10014C	Fairchild
F10014M	† Fairchild

ECL-95000 Series

Counters

Binary Counter

Device	Source
F95016	Fairchild

Decade Counter

Device	Source
F95010	Fairchild

Flip-Flops

"J K" Flip Flop

Device	Source
F95029	Fairchild

Dual "D" Master Slave Flip Flop

Device	Source
F95231	Fairchild

Gates, Exclusive OR/NOR

Triple 2 Input Exclusive OR/NOR Gate

Device	Source
F95107	Fairchild

Gates, OR/NOR

Dual 3 Input 3 Output OR Gate (Line Driver)

Device	Source
F95110	Fairchild

Dual 3 Input 3 Output NOR Gate (Line Driver)

Device	Source
F95111	Fairchild

Triple 4 3 3 Input NOR Gate

Device	Source
F95106	Fairchild

Quad 2 Input NOR (with Enable)

Device	Source
F95004	Fairchild

Dual 4 5 Input OR/NOR Gate

Device	Source
F95109	Fairchild

Dual 4 Input OR/NOR Gate (with Enable)

Device	Source
F95002	Fairchild

Triple 2 3 2 Input OR/NOR Gate

Device	Source
F95105	Fairchild

Triple 2 Input OR/NOR Gate (with Enable)

Device	Source
F95003	Fairchild

Quad 2 Input Gate (3 OR, 1 OR/NOR)

Device	Source
F95103	Fairchild

Quad 2 Input Gate (3 NOR, 1 OR/NOR)

Device	Source
F95102	Fairchild

Quad 2 Input OR/NOR Gate (One Input Common)

Device	Source
F95101	Fairchild

Latches

Dual "D" Clocked Latch

Device	Source
F95130	Fairchild

Shift Registers

4 bit Shift Register

Device	Source
F95000	Fairchild

Translators

Quad TTL to ECL OR/NOR Translator

Device	Source
F95124	Fairchild

Miscellaneous

Triple Differential Line Receiver

Device	Source
F95116	Fairchild

Quad Differential Line Receiver

Device	Source
F95115	Fairchild

ECL-100K Series

Arithmetic Functions

6 bit Adder

Device	Source
F10080	Fairchild

4 bit Binary/Decade Arithmetic Logic Unit

Device	Source
F100181	Fairchild

Look Ahead Carry Circuit

Device	Source
F100179	Fairchild

9 bit Comparator

Device	Source
F100166	Fairchild

Counters

Multipurpose Counting Register

Device	Source
F100136	Fairchild

Decoders

Universal Decoder

Device	Source
F100170	Fairchild

Drivers

Quad Driver

Device	Source
F100112	Fairchild

Hex Bus Driver

Device	Source
F100123	Fairchild

Flip-Flops

Triple D Type

Device	Source
F100131	Fairchild

Hex D Type

Device	Source
F100151	Fairchild

Gates, AND-OR-Invert

Triple AND OR Invert Gate

Device	Source
F100117	Fairchild

5 Wide AND OR Invert Gate

Device	Source
F100118	Fairchild

Gates, Exclusive OR/NOR

Quintuple Exclusive OR/NOR Gate

Device	Source
F100107	Fairchild

Gates, OR/NOR

Triple 5 Input OR/NOR Gate

Device	Source
F100101	Fairchild

Quintuple 2 Input OR/NOR Gate

Device	Source
F100102	Fairchild

Latches

Triple D Latch

Device	Source
F100130	Fairchild

Hex D Latch

Device	Source
F100150	Fairchild

Memories

CAM (4x4)

Device	Source
100142	Fairchild

RAM (16x4 Register File)

Device	Source
F100145	Fairchild

RAM (1024x1)

Device	Source	
F100415	**Fairchild**	**(1128)**

Multiplexers

Dual 8 Input Multiplexer

Device	Source
F100163	Fairchild

16 Input Multiplexer

Device	Source
F100164	Fairchild

Triple 4 Input Multiplexer

Device	Source
F100171	Fairchild

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–ECL (Cont'd)

Function	Device	Source	Line
Multiplexers (Cont'd)			
Quad 2 Input Multiplexer with Latch			
	F100155	Fairchild	
Shift Registers			
8 bit Universal Shift Register			
	F100141	Fairchild	
8 bit Shift Matrix			
	F100158	Fairchild	
Mask Merge			
	F100194	Fairchild	
Miscellaneous			
Quintuple Line Receiver			
	F100114	Fairchild	
Quintuple Transceiver			10
	F100194	Fairchild	
Dual 9 bit Parity Generator/Checker			
	F100160	Fairchild	
Universal Priority Encoder			
	F100165	Fairchild	
Gate Array (Customized in final metalizations)			
	ECL-Array	Fairchild	
ECL-III and Other Series			
Counters			
Binary Counter			
	MC1654	Motorola	
Divide by 4 Counter (1 GHz)			20
	11C05C	Fairchild	
	11C05M	Fairchild	
	MC1699	Motorola	
Divide by 4 Prescaler (1 GHz)			
	MC1697	Motorola	
	MC1699	Motorola	
Bi Quinary Counter			
	MC1678	Motorola	
Divide by 5/6 Prescaler, 650 MHz			
	11C91C	Fairchild	30
	11C91M	† Fairchild	
Divide by 10/11 Prescaler, 650 MHz			
	11C90C	Fairchild	
	11C90M	† Fairchild	
Divide by 248/256 Prescaler, 950 MHz			
	11C83	Fairchild	
Flip-Flops			
Master Slave "D" Flip Flop			
	11C70C	Fairchild	
	MC1670	Motorola	
	µPB606B	NEC America	40
	µPB631B	NEC America	
	SP1670B	Plessey	
	SP1671B	Plessey	
Master Slave "D" Flip Flop (UHF Prescaler)			
	11C06C	Fairchild	
	MC1690	Motorola	
	SP1690B	Plessey	

Function	Device	Source	Line
Flip-Flops (Cont'd)			
Dual, Clocked "R S" Flip Flop			
	MC1666	Motorola	
	µPB604B	NEC America	50
	SP1666	Plessey	
	SP1667B	Plessey	
Gates, Exclusive OR/NOR			
Triple 2 Input Exclusive OR Gate			
	MC1672	Motorola	
	µPB607B	NEC America	
	SP1672B	Plessey	
	SP1673B	Plessey	
Triple 2 Input Exclusive NOR Gate			
	MC1674	Motorola	
	SP1674B	Plessey	60
	SP1675B	Plessey	
Gates, OR/NOR			
Quad 2 Input OR Gate			
	MC1664	Motorola	
	µPB603B	NEC America	
	SP1664B	Plessey	
	SP1665B	Plessey	
Quad 2 Input NOR Gate			
	MC1662	Motorola	
	µPB602B	NEC America	
	SP1662B	Plessey	70
	SP1663B	Plessey	
Dual 4 Input OR/NOR Gate			
	MC1660	Motorola	
	µPB601B	NEC America	
	µPB631B	NEC America	
	SP16F60	Plessey	
	SP1660B	Plessey	
	SP1661B	Plessey	
Dual 4 5 Input OR/NOR Gate			
	11C01C	Fairchild	80
	MC1688	Motorola	
Latches			
Dual Clocked Latch			
	MC1668	Motorola	
	µPB605B	NEC America	
	SP1668	Plessey	
	SP1669	Plessey	
Multivibrators			
Voltage Controlled Multivibrator			
	11C58C	Fairchild	
	MC1658	Motorola	
	SP1658	Plessey	90
Shift Registers			
4 bit Shift Register			
	MC1694	Motorola	
Miscellaneous			
Dual Analog/Digital Comparator			
	MC1650	Motorola	
	MC1651	Motorola	
	SP1650B	Plessey	
	SP1651B	Plessey	

Function	Device	Source	Line
Miscellaneous (Cont'd)			
Quad Line Receiver			
	MC1692	Motorola	
	SP1692B	Plessey	100
Voltage Controlled Oscillator			
	MC1648	† Motorola	
	SP1648B	Plessey	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–HNIL/HTL

Function	Device	Source	Line
Arithmetic Functions			
4 bit Comparator			
	343A/C	Teledyne S	
	343B/M	† Teledyne S	
Buffers/Inverters			
See also: Gates, Miscellaneous			
Hex Inverter			
	MC680	Motorola	
	MC690	Motorola	
	MC697	Motorola	
	H118	SGS	
	332A/C	Teledyne S	10
	332B/M	† Teledyne S	
Hex Inverter, Open Collector			
	MC681	Motorola	
	MC689	Motorola	
	H112	SGS	
Hex Inverter, Strobed			
	MC677	Motorola	
	H119	SGS	
	335A/C	Teledyne S	
	335B/M	† Teledyne S	20
Hex Inverter, Strobed, Open Collector			
	MC678	Motorola	
	H115	SGS	
	334A/C	Teledyne S	
	334B/M	† Teledyne S	
Counters			
Binary Counter			
	MC685	Motorola	
	H156	SGS	
	372A/C	Teledyne S	
	372B/M	† Teledyne S	30
Binary Up/Down Counter			
	374A/C	Teledyne S	
	374B/M	† Teledyne S	
Decade Counter			
	MC684	Motorola	
	H157	SGS	
	371A/C	Teledyne S	
	371B/M	† Teledyne S	
Decade Up/Down Counter			
	373A/C	Teledyne S	40
	373B/M	† Teledyne S	
Decoders/Drivers			
BCD to Seven Segment Decoder/Driver			
	383A/C	Teledyne S	
	383B/M	† Teledyne S	
BCD to Decimal Decoder, Open Collector			
	381A/C	Teledyne S	
	381B/M	† Teledyne S	
BCD to Seven Segment Driver, Gas Discharge Driver			
	384A/C	Teledyne S	
	384B/M	† Teledyne S	50
BCD to Decimal Decoder/Lamp Driver, Open Collector			
	380A/C	Teledyne S	
	380B/M	† Teledyne S	
BCD to Decimal Decoder/Driver (for Gas Discharge Display Tubes)			
	MC676	Motorola	
	(Continued)		

Function	Device	Source	Line
Decoders/Drivers (Cont'd)			
BCD to Decimal Decoder/Driver (for Gas Discharge Display Tubes) (Cont'd.)			
	H158	SGS	60
	382A/C	Teledyne S	
	382B/M	† Teledyne S	
Dual Lamp/Line Driver			
	MC679	Motorola	
Dual Power AND Driver, Open Collector and Open Emitter (Schmitt Trigger)			
	MC699	Motorola	
Dual 4 Input AND Driver, Expandable			
	H109	SGS	
Dual 4 Input NAND Line Driver, Expandable			70
	MC662	Motorola	
Dual 5 Input Power NAND Driver			
	301A/C	Teledyne S	
	301B/M	† Teledyne S	
Dual 4 Input NAND Lamp/Relay Driver, Open Collector (to 30 v)			
	MC679	Motorola	
Quad 2 Input Power NAND Driver, Open Collector			
	302A/C	Teledyne S	
	302B/M	† Teledyne S	80
Flip-Flops			
Quad "D" Flip Flop			
	370A/C	Teledyne S	
	370B/M	† Teledyne S	
Master Slave "R S" Flip Flop			
	MC664	Motorola	
Master Slave "J K" or Set Reset Flip Flop			
	311A/C	Teledyne S	
	311B/M	† Teledyne S	
Dual "J K" Flip Flop with Preset			
	H110	SGS	90
Dual "J K" Flip Flop with Preset and Clear			
	H111	SGS	
Dual "J K" Flip Flop with Reset			
	MC663	Motorola	
Dual "J K" or Set Reset Flip Flop			
	MC688	Motorola	
	312A/C	Teledyne S	
	312B/M	† Teledyne S	
	313A/C	Teledyne S	
	313B/M	† Teledyne S	100
Gates, AND/NAND			
Dual 2 Input AND Interface Buffer			
	391	Teledyne S	
Dual 4 Input AND Interface Buffer			
	390	Teledyne S	
Dual 4 Input NAND Gate			
	MC660	Motorola	
	MC661	Motorola	
Dual 2 Input NAND Interface Buffer			
	392	Teledyne S	
Dual 4 Input NAND Interface Buffer			
	395	Teledyne S	110
Dual 4 Input NAND Gate, Expandable			
	H104	SGS	
	H124	SGS	
	(Continued)		

Function	Device	Source	Line
Gates, AND/NAND (Cont'd)			
Dual 4 Input NAND Gate, Expandable (Cont'd.)			
	396	Teledyne S	
Dual 5 Input NAND Gate			
	301A/C	Teledyne S	
	301B/M	† Teledyne S	
	322A/C	Teledyne S	120
	322B/M	† Teledyne S	
Triple 3 Input NAND Gate			
	MC670	Motorola	
	MC671	Motorola	
	H103	SGS	
4, 3, 4 Input NAND Gate			
	304A/C	Teledyne S	
	304B/M	† Teledyne S	
Quad 2 Input NAND Gate			
	MC668	Motorola	130
	MC672	Motorola	
	H102	SGS	
	H122	SGS	
	303A/C	Teledyne S	
	303B/M	† Teledyne S	
	321A/C	Teledyne S	
	321B/M	† Teledyne S	
	324A/C	Teledyne S	
	324B/M	† Teledyne S	
Quad 2 Input NAND Gate, Open Collector			140
	302A/C	Teledyne S	
	302B/M	† Teledyne S	
	323A/C	Teledyne S	
	323B/M	† Teledyne S	
Quad 2 Input NAND Gate (Schmitt Trigger)			
	MC693	Motorola	
2,2,3,3 Input NAND Gate			
	325A/C	Teledyne S	
	325B/M	† Teledyne S	
	326A/C	Teledyne S	150
	326B/M	Teledyne S	
Gates, OR/NOR			
Dual 2 Input OR Interface Buffer			
	393	Teledyne S	
Dual 2 Input NOR Interface Buffer			
	394	Teledyne S	
Quad 2 Input NOR Gate			
	306A/C	Teledyne S	
	306B/M	† Teledyne S	
Quad 2 Input NOR Gate, Open Collector			
	307A/C	Teledyne S	160
	307B/M	† Teledyne S	
GATES, AND-OR-Invert			
Expandable AND OR Invert			
	344A/C	Teledyne S	
	344B/M	† Teledyne S	
Dual 2 Wide, 2 Input AND OR Invert Gate			
	MC673	Motorola	
	MC674	Motorola	
	341A/C	Teledyne S	
	341B/M	† Teledyne S	
Dual 2 Wide, 2 Input AND OR Invert Gate, Expandable			170
	H105	SGS	

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–HNIL/HTL (Cont'd)

Gates, Exclusive OR

Quad 2 Input Exclusive OR Gate
- MC683 — Motorola

Gates, Miscellaneous

Hex Inverter/Gate (Quad Inverter, Dual NAND Gate)
- 333A/C — Teledyne S
- 333B/M — † Teledyne S

Hex Inverter/Gate (Quad Inverter, Dual NAND Gate) Open Collector
- 332A/C — Teledyne S
- 332B/M — † Teledyne S

Dual 4 Input Gate Expander (for 600 Series)
- MC669 — Motorola

Dual 5 Input Gate Expander (for 300 Series)
- 331A/C — Teledyne S
- 331B/M — † Teledyne S
- CA3094 — † RCA
- CA3094A — † RCA
- CA3094B — † RCA

Latches

Quad Latch
- MC682 — Motorola

Multiplexers

8 Bit Multiplexer
- 350A/C — Teledyne S
- 350B/M — † Teledyne S

Dual 4 Bit Multiplexer
- 351A/C — Teledyne S
- 351B/M — † Teledyne S

Multivibrators

Monostable Multivibrator
- H117 — SGS
- 346 — Teledyne S

Dual Monostable Multivibrator
- MC667 — Motorola
- 342A/C — Teledyne S
- 342B/M — † Teledyne S

Dual Retriggerable Monostable Multivibrator
- 347A/C — Teledyne S
- 347B/M — † Teledyne S

Shift Registers

4 bit Parallel In Parallel Out Shift Register
- MC686 — Motorola
- 375A/C — Teledyne S
- 375B/M — † Teledyne S

Translators

Dual Low to High Interface (TTL to HNIL)
- 362A/C — Teledyne S
- 362B/M — † Teledyne S

Triple Low to High Translator (TTL to HTL)
- MC666 — Motorola

Quad Low to High Interface (TTL to HNIL)
- H114 — SGS
- 363A/C — Teledyne S
- 363B/M — † Teledyne S

Translators (Cont'd)

Dual High to Low Interface (HNIL to DTL, TTL)
- 361A/C — Teledyne S
- 361B/M — † Teledyne S

Dual Interface Element, (Line Driver, Receiver, ECL to TTL, MOS to TTL, Schmitt Trigger)
- MC696 — Motorola

Triple High to Low Translator (HTL to TTL)
- MC665 — Motorola

Quad High to Low Converter (Open Collector)
- H113 — SGS

Hex Inverter/Interface (Low to High: TTL, CMOS to HTL, CMOS)
- MC691 — Motorola

Miscellaneous

Pulse Stretcher
- 348 — Teledyne S

Dual Pulse Stretcher
- MC675 — Motorola
- 349A/C — Teledyne S
- 349B/M — † Teledyne S

Quad Schmitt Trigger/Line Receiver
- 367A/C — Teledyne S
- 367B/M — † Teledyne S

Quad Schmitt Trigger/Line Receiver, Open Collector
- MC693 — Motorola
- 368A/C — Teledyne S
- 368B/M — † Teledyne S

Timer (See also Linear Timers)
- 355A/C — Teledyne S
- 355B/M — Teledyne S

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL

Arithmetic Functions

Function	Device	Source	Line
Gated Full Adder			
TTL	5480	† Fairchild	
	7480	Fairchild	
	ITT5480	† ITT	
	ITT7480	ITT	
	M53280	Mitsubishi	
	MC5480	† Motorola	
	MC7480	Motorola	
	μPB7480	NEC America	
	5480	† Signetics	10
	7480	Signetics	
	N8268	Signetics	
	SN5480	† TI	
	SN7480	TI	
2 bit Binary Full Adder			
TTL	5482	† Fairchild	
	7482	Fairchild	
	ZN5482	† Ferranti	
	ZN7482	Ferranti	
	HD2513	Hitachi	20
	ITT5482	† ITT	
	ITT7482	ITT	
	MC5482	† Motorola	
	MC7482	Motorola	
	SN5482	† TI	
	SN7482	TI	
4 bit Binary Full Adder, Look Ahead Carry			
TTL	5483	† Fairchild	
	7483	Fairchild	
	54283	† Fairchild	30
	74283	Fairchild	
	ZN5483A	† Ferranti	
	ZN7483A	Ferranti	
	HD2535	Hitachi	
	ITT5483	† ITT	
	ITT7483	ITT	
	M53283	Mitsubishi	
	M53483	Mitsubishi	
	MC5483	† Motorola	
	MC7483	Motorola	40
	DM5483	† National	
	DM7483	National	
	μPB74283	NEC America	
	5483	† Raytheon	
	7483	Raytheon	
	54283	† Raytheon	
	74283	Raytheon	
	5483	† Signetics	
	7483	Signetics	
	SN5483A	† TI	50
	SN7483A	TI	
	SN54283	† TI	
	SN74283	TI	
TTL-LS	9LS83C	Fairchild	
	9LS83M	† Fairchild	
	9LS283C	Fairchild	
	9LS283M	† Fairchild	
	54LS83	† Fairchild	
	74LS83	Fairchild	
	54LS283	† Fairchild	60
	74LS283	Fairchild	
	ITT74LS83A	ITT	
	ITT74LS283	ITT	
	SN54LS83	† Motorola	
	SN74LS83	Motorola	
	SN54LS283	† Motorola	
	SN74LS283	Motorola	
	DM54LS83A	† National	
	DM74LS83A	National	

(Continued)

Arithmetic Functions (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)			70
	DM54LS283	† National	
	DM74LS283	National	
	9LS83AC	Raytheon	
	9LS83AM	† Raytheon	
	54LS83A	† Raytheon	
	74LS83A	Raytheon	
	9LS283C	Raytheon	
	9LS283M	† Raytheon	
	54LS283	† Raytheon	
	74LS283	Raytheon	80
	74LS83A	Signetics	
	74LS283	Signetics	
	SN54LS83A	† TI	
	SN74LS83A	TI	
	SN54LS283	† TI	
	SN74LS283	TI	
TTL-S	SN54S283	† TI	
	SN74S283	TI	
4 bit Full Adder with Output Latch			
TTL	AM2506C	AMD	90
	AM2506M	† AMD	
	RC2506	Raytheon	
	RM2506	† Raytheon	
NBCD Adder (Natural Binary Coded Decimal)			
TTL	MC4056	Motorola	
	MC4356	† Motorola	
	MC54456	† Motorola	
	MC74456	Motorola	
4 bit BCD Adder			
TTL-S	N82S83	Signetics	100
Dual Full Adder			
TTL	9304C	AMD	
	9304M	† AMD	
	9304C	Fairchild	
	9304M	† Fairchild	
	ITT9304-1	† ITT	
	ITT9304-5	ITT	
	M54304	Mitsubishi	
	MC8304	Motorola	
	MC9304	Motorola	110
	RC9304	Raytheon	
	RM9304	† Raytheon	
	9304	Signetics	
TTL-LS	SN54LS183	† TI	
	SN74LS183	TI	
TTL-H	54H183	† Fairchild	
	74H183	Fairchild	
	SN54H183	† TI	
	SN74H183	TI	
Dual Full Adder/Full Subtractor			120
TTL	M54401	Mitsubishi	
Quad Serial Adder/Subtractor			
TTL-LS	AM25LS15C	AMD	
	AM25LS15M	† AMD	
	SN54LS385	† AMD	
	SN74LS385	AMD	
	25LS15C	**Raytheon (295)**	
	25LS15M	**† Raytheon (295)**	
	SN54LS385	† TI	
	SN74LS385	TI	130
4 bit BCD Arithmetic Unit (add, subtract, compare)			
TTL-S	N82S82	Signetics	
Binary Multiplier (2x4) Parallel, Serial Output			
TTL-LS	ITT74LS261	ITT	

(Continued)

Arithmetic Functions (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)			
	9LS261C	**Raytheon (284)**	
	9LS261M	**† Raytheon (284)**	
	54LS261	**† Raytheon (284)**	
	74LS261	**Raytheon (284)**	
	54LS261	† Signetics	140
	74LS261	Signetics	
	SN54LS261	† TI	
	SN74LS261	TI	
Binary Multiplier (4x2)			
TTL	9344C	Fairchild	
	9344M	† Fairchild	
Binary Multiplier (4x4) Three State			
TTL-S	SN74S274	TI	
4 bit Multiplier, Three State (two ICs to a set, 7875A and 7875B)			150
TTL	DM7875	† National	
	DM8875	National	
Binary Multiplier (4x4) Parallel (used with 54/74285)			
TTL	DM54284	† National	
	SN54284	† TI	
	SN74284	TI	
Binary Multiplier (4x4) Parallel (used with 54/74284)			
TTL	SN54285	† TI	
	SN74285	TI	
Multiplier (8x1) Serial/Parallel 2's Complement			160
TTL-LS	AM25LS14C	AMD	
	AM25LS14M	† AMD	
	SN54LS384	† AMD	
	SN74LS384	AMD	
	25LS14C	**Raytheon (293)**	
	25LS14M	**† Raytheon (293)**	
	SN54LS384	† TI	
	SN74LS384	TI	
8 Bit Serial/Parallel Register (for use with 25LS14/74LS384)			170
TTL-LS	AM25LS22C	AMD	
	AM25LS22M	† AMD	
	SN54LS322	† AMD	
	SN74LS322	AMD	
	25LS22C	**Raytheon (297)**	
	25LS22M	**† Raytheon (297)**	
	SN54LS322	TI	
	SN74LS322	TI	
2's Complement Multiplier (4x2)			
TTL	AM2505C	AMD	180
	AM2505M	† AMD	
	RC2505	Raytheon	
	RM2505	† Raytheon	
TTL-S	AM25S05C	AMD	
	AM25S05M	† AMD	
	93S43C	Fairchild	
	93S43M	† Fairchild	
2's Complement Multiplier (8x8)			
TTL-S	**57558**	**† MMI (1652)**	
	67558	**MMI (1652)**	190
	MPY8AJ	TRW	
	MPY8AJM	† TRW	
2's Complement Multiplier (12x12)			
TTL-S	MPY12AJ	TRW	
	MPY12AJM	† TRW	
2's Complement Multiplier (12x12) with Accumulator			
TTL-S	TDC1003J	TRW	

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Arithmetic Functions (Cont'd)

Function	Device	Source	Line
2's Complement Multiplier (16x16)			
TTL-S	MPY16AJ	TRW	
	MPY16AJM	† TRW	
7 bit Slice Wallace Tree (to build multipliers)			
TTL-LS	SN54LS275	† TI	
	SN74LS275	TI	
TTL-S	SN54S275	† TI	
	SN74S275	TI	
4 bit ALU with Look ahead Carry			
TTL	9340C	AMD	
	9340M	† AMD	10
	9340C	Fairchild	
	9340M	† Fairchild	
Arithmetic Logic Unit/Function Generator			
TTL	9341C	AMD	
	9341M	† AMD	
	AM2506C	AMD	
	AM2506M	† AMD	
	SN54181	† AMD	
	SN74181	AMD	
	9341C	Fairchild	20
	9341M	† Fairchild	
	54181	† Fairchild	
	74181	† Fairchild	
	ZN54181	† Ferranti	
	ZN74181	Ferranti	
	HD2547	Hitachi	
	M53381	Mitsubishi	
	MC54181	Motorola	
	MC74181	Motorola	
	DM54181	† National	30
	DM74181	National	
	μPB74181	NEC America	
	54181	† Raytheon	
	74181	Raytheon	
	RC2506	Raytheon	
	RM2506	† Raytheon	
	RC9341	Raytheon	
	RM9341	† Raytheon	
	54181	† Signetics	
	74181	Signetics	40
	SN54181	† TI	
	SN74181	TI	
TTL-LS	AM25LS181C	AMD	
	AM25LS181M	† AMD	
	SN54LS181	† AMD	
	SN74LS181	AMD	
	9LS181C	Fairchild	
	9LS181M	† Fairchild	
	74LS181	Fairchild	
	SN54LS181	† Motorola	50
	SN74LS181	Motorola	
	9LS181C	Raytheon	
	9LS181M	† Raytheon	
	54LS181	† Raytheon	
	74LS181	Raytheon	
	25LS181C	Raytheon	
	25LS181M	† Raytheon	
	54LS181	† Signetics	
	74LS181	Signetics	
	SN54LS181	† TI	60
	SN74LS181	TI	
TTL-H	54R181	† Raytheon	
	74R181	Raytheon	
TTL-S	SN54S181	† AMD	
	SN74S181	AMD	
	54S181	† Fairchild	

(Continued)

Arithmetic Functions (Cont'd)

Function	Device	Source	Line
TTL-S (Cont'd.)			
	74S181	Fairchild	
	93S41C	Fairchild	
	93S41M	† Fairchild	70
	HD74S181	Hitachi	
	M5S181	Mitsubishi	
	54S181	† Signetics	
	74S181	Signetics	
	SN54S181	† TI	
	SN74S181	TI	
Arithmetic Logic Unit/Function Generator			
TTL-LS	AM25LS2517C	AMD	
	AM25LS2517M	AMD	
	AM25LS381C	AMD	80
	AM25LS381M	† AMD	
	SN54LS381	† AMD	
	SN74LS381	AMD	
	ITT74LS381	ITT	
	SN54LS381	† TI	
	SN74LS381	TI	
TTL-S	SN54S381	† TI	
	SN74S381	TI	
Look ahead Carry Generator			
TTL	9342C	AMD	90
	9342M	† AMD	
	SN54182	† AMD	
	SN74182	AMD	
	9342C	Fairchild	
	9342M	† Fairchild	
	54182	† Fairchild	
	74182	Fairchild	
	HD2562	Hitachi	
	ITT54182	† ITT	
	ITT74182	ITT	100
	M53382	Mitsubishi	
	MC54182	† Motorola	
	MC74182	Motorola	
	μPB74182	NEC America	
	DM54182	† National	
	DM74182	National	
	RC9342	Raytheon	
	RM9342	† Raytheon	
	54182	† Raytheon	
	74182	Raytheon	110
	54182	† Signetics	
	74182	Signetics	
	SN54182	† TI	
	SN74182	TI	
TTL-H	54R182	† Raytheon	
	74R182	Raytheon	
TTL-S	54S182	† Fairchild	
	74S182	Fairchild	
	93S42C	Fairchild	
	93S42M	† Fairchild	120
	M5S182	Mitsubishi	
	DM74S182	National	
	74S182	Signetics	
	SN54S182	† TI	
	SN74S182	TI	
Register/Arithmetic Logic Unit			
TTL-LS	AM25LS281C	AMD	
	AM25LS281M	† AMD	
	SN54LS281	† AMD	
	SN74LS281	AMD	130
TTL-S	DM74S281	National	
	SN54S281	† TI	

(Continued)

Arithmetic Functions (Cont'd)

Function	Device	Source	Line
TTL-S (Cont'd.)			
	SN74S281	TI	
Arithmetic Logic Element			
TTL	MC7260	Motorola	
	MC8260	† Motorola	
	RC8260	Raytheon	
	RM8260	† Raytheon	
	N8260	Signetics	140
	S8260	† Signetics	
Fast Carry Extender (for 8260)			
TTL	MC7261	Motorola	
	MC8261	† Motorola	
	RC8261	Raytheon	
	RM8261	† Raytheon	
	N8261	Signetics	
	S8261	† Signetics	
Arithmetic and Logic Shift Matrix, Bit and Byte Masking			
TTL-S	**9405AC**	**Fairchild (1620)**	150
	9405AM	**† Fairchild (1620)**	
4 bit Microprocessor Slice (ALU)			
TTL-S	AM2901C	AMD	
	AM2901M	† AMD	
	AM2901AC	AMD	
	AM2901AM	† AMD	
	AM2903C	AMD	
	AM2903M	† AMD	
	9405AC	**Fairchild (1620)**	
	F2901AC	Fairchild	160
	F2901AM	† Fairchild	
	9405AM	**† Fairchild (1620)**	
	3002	Intel	
	M3002	† Intel	
	5701	**† MMI (1654)**	
	6701	**MMI (1654)**	
	MC2901	Motorola	
	IDM2901AC	**National (1680)**	
	IDM2901AM	**† National (1680)**	
	μPB2901	**NEC Micro (1850)**	170
	AM2901C	Raytheon	
	AM2901M	† Raytheon	
	AM2901AC	Raytheon	
	AM2901AM	† Raytheon	
	N2901-1	**Signetics (1851)**	
	N3002	**Signetics (1868)**	
	S3002	**† Signetics (1868)**	
	SN54LS481	† TI	
	SN74LS481	TI	
	SN74S481	TI	180
4 bit Magnitude Comparator			
TTL	DM7200	† National	
	DM8200	National	
	N8269	Signetics	
	S8269	† Signetics	
4 bit Magnitude Comparator, Separate A=B Output			
TTL	9324C	AMD	
	9324M	† AMD	
	5485	† Fairchild	
	7485	Fairchild	190
	9324C	Fairchild	
	9324M	† Fairchild	
	ZN5485	† Ferranti	
	ZN7485	Ferranti	
	HD7485	Hitachi	
	M53285	Mitsubishi	
	MC5485	† Motorola	
	MC7485	Motorola	
	MC8324	Motorola	

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† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Arithmetic Functions (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	MC9324	† Motorola	
	DM5485	† National	
	DM7485	National	
	μPB7485	NEC America	
	5485	† Signetics	
	7485	Signetics	
	N9324	Signetics	
	SN5485	† TI	
	SN7485	TI	10
	7485	TRW	
TTL-LS	9LS85C	Fairchild	
	54LS85	† Fairchild	
	74LS85	Fairchild	
	ITT74LS85	TI	
	SN74LS85	Motorola	
	DM54LS85	† National	
	DM74LS85	National	
	9LS85C	Raytheon	
	9LS85M	† Raytheon	20
	54LS85	† Raytheon	
	74LS85	Raytheon	
	54LS85	† Signetics	
	74LS85	Signetics	
	SN54LS85	† TI	
	SN74LS85	TI	
TTL-S	M5S085	Mitsubishi	
	54S85	† Signetics	
	74S85	Signetics	
	SN54S85	† TI	30
	SN74S85	TI	
Dual 4 bit Magnitude Comparator			
TTL	MC4021	Motorola	
	MC4022	Motorola	
	MC4321	† Motorola	
	MC4322	† Motorola	
6 bit, Unified Bus Comparator, Active Pull Up			
TTL	DM7131	† National	
	DM8131	National	
6 bit Unified Bus Comparator, Open Collector			40
TTL	DM7136	† National	
	DM8136	National	
6 bit Identity Comparator			
TTL	DM7160	† National	
	DM8160	National	
TTL-S	93S46C	Fairchild	
	93546M	† Fairchild	
6 bit Identity Comparator, Open Collector			
TTL-S	93S47C	Fairchild	
	93S47M	† Fairchild	50
8 bit Comparator			
TTL-LS	AM25LS2521C	AMD	
	AM25LS2521M	† AMD	
10 bit Identity Comparator			
TTL	DM7130	† National	
	DM8130	National	

Buffers/Inverters

Function	Device	Source	Line
Quad Gated Buffer, Three State			
TTL	54125	† Fairchild	
	74125	Fairchild	
	HD74125	Hitachi	60
	M53325	Mitsubishi	
	DM7093	† National	
	(Continued)		

Buffers/Inverters (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	DM8093	National	
	DM54125	† National	
	DM74125	National	
	54125	† Signetics	
	74125	Signetics	
	SN54125	† TI	
	SN74125	TI	70
	SN54425	† TI	
	SN74425	TI	
TTL-LS	9LS125C	Fairchild	
	9LS125M	Fairchild	
	54LS125	† Fairchild	
	74LS125	Fairchild	
	ITT74LS125	ITT	
	DM54LS125	† National	
	DM74LS125	National	
	9LS125C	Raytheon	80
	9LS125M	† Raytheon	
	54LS125	† Raytheon	
	74LS125	Raytheon	
	54LS125	† Signetics	
	74LS125	Signetics	
	SN54LS125A	† TI	
	SN74LS125A	TI	
Quad Gated Buffer, Three State (Inverted Control)			
TTL	54126	† Fairchild	
	74126	Fairchild	90
	HD74126	Hitachi	
	M53326	Mitsubishi	
	DM7094	† National	
	DM8094	National	
	DM54126	† National	
	DM74126	National	
	54126	† Signetics	
	74126	Signetics	
	SN54126	† TI	
	SN74126	TI	100
	SN54426	† TI	
	SN74426	TI	
TTL-LS	9LS126C	Fairchild	
	9LS126M	† Fairchild	
	54LS126	† Fairchild	
	74LS126	Fairchild	
	ITT74LS126	ITT	
	SN54LS126	† Motorola	
	SN74LS126	Motorola	
	DM54LS126	† National	110
	DM74LS126	National	
	9LS126C	Raytheon	
	9LS126M	† Raytheon	
	54LS126	† Raytheon	
	74LS126	Raytheon	
	54LS126	† Signetics	
	74LS126	Signetics	
	SN54LS126A	† TI	
	SN74LS126A	TI	
Hex Buffer, Three State			
TTL	DM7095	† National	120
	DM7097	† National	
	DM8097	National	
	DM8095	National	
	DM54365	† National	
	DM74365	National	
	DM54367	† National	
	DM74367	National	
	74365	Signetics	
	74367	Signetics	130
	(Continued)		

Buffers/Inverters (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	SN54365	† TI	
	SN74365	TI	
	SN54367	† TI	
	SN74367	TI	
TTL-LS	9LS365C	Fairchild	
	9LS365M	† Fairchild	
	9LS367C	Fairchild	
	9LS367M	† Fairchild	
	54LS365	† Fairchild	140
	74LS365	Fairchild	
	54LS367	† Fairchild	
	74LS367	Fairchild	
	ITT74LS365	ITT	
	ITT74LS367	ITT	
	SN54LS365	† Motorola	
	SN74LS365	Motorola	
	SN54LS367	† Motorola	
	SN74LS367	Motorola	
	DM54LS365	† National	150
	DM74LS365	National	
	DM54LS367	† National	
	DM74LS367	National	
	μPB74LS365	NEC America	
	μPB74LS367	NEC America	
	9LS365C	**Raytheon (286)**	
	9LS365M	**† Raytheon (286)**	
	54LS365	**† Raytheon (286)**	
	74LS365	**Raytheon (286)**	
	9LS367C	**Raytheon (286)**	160
	9LS367M	**† Raytheon (286)**	
	54LS367	**† Raytheon (286)**	
	74LS367	**Raytheon (286)**	
	54LS365	† Signetics	
	74LS365	Signetics	
	54LS367	† Signetics	
	74LS367	Signetics	
	SN54LS365A	† TI	
	SN74LS365A	TI	
	SN54LS367A	† TI	170
	SN74LS367A	TI	
TTL-S	MB485	Fujitsu	
	MB487	Fujitsu	
	MC8T95	Motorola	
	MC8T97	Motorola	
	N8T95	Signetics	
	N8T97	Signetics	
Octal Buffer, Three State			
TTL-LS	DM71LS95	† National	
	DM81LS95	National	180
	DM71LS97	† National	
	DM81LS97	National	
Octal (Dual Quad), Buffer (Driver), Hysteresis, Three State. See Octal Bus Drivers under Miscellaneous			
Hex Inverter			
TTL	5404	† Fairchild	
	7404	Fairchild	
	9016C	Fairchild	
	9016M	† Fairchild	
	ZN5404	† Ferranti	190
	ZN7404	Ferranti	
	HD2522	Hitachi	
	HD7404	Hitachi	
	ITT5404	† ITT	
	ITT7404	ITT	
	ITT9016-1	† ITT	
	ITT9016-5	ITT	
	(Continued)		

† Military Temperature Range (−55° to 125°C)

* Typical Values

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DIGITAL–TTL (Cont'd)

Buffers/Inverters (Cont'd)

Function	Device	Source
TTL (Cont'd.)	M53204	Mitsubishi
	MC5404	† Motorola
	MC7404	Motorola
	DM5404	† National
	DM7404	National
	DM9016C	National
	μPB7404	NEC America
	5404	† Raytheon
	7404	Raytheon
	7404	Signetics
	5404	† Signetics
	SN5404	† TI
	SN7404	TI
	TD3404	Toshiba
	7404	TRW
TTL-LS	9LS04C	Fairchild
	9LS04M	† Fairchild
	54LS04	† Fairchild
	74LS04	Fairchild
	ITT74LS04	ITT
	SN54LS04	† Motorola
	SN74LS04	Motorola
	DM54LS04	† National
	DM74LS04	National
	μPB74LS04	NEC America
	9LS04C	Raytheon
	9LS04M	† Raytheon
	54LS04	† Raytheon
	74LS04	Raytheon
	54LS04	† Signetics
	74LS04	Signetics
	SN54LS04	† TI
	SN74LS04	TI
TTL-H	54H04	† Fairchild
	74H04	Fairchild
	HD2563	Hitachi
	ITT54H04	† ITT
	ITT74H04	ITT
	MC3008	Motorola
	MC3108	† Motorola
	DM54H04	† National
	DM74H04	National
	μPB74H04	NEC America
	54H04	† Raytheon
	74H04	Raytheon
	54R04	† Raytheon
	74R04	Raytheon
	54H04	† Signetics
	74H04	Signetics
	SN54H04	† TI
	SN74H04	TI
TTL-S	54S04	† Fairchild
	74S04	Fairchild
	9S04AC	Fairchild
	9S04AM	† Fairchild
	HD74S04	Hitachi
	M5S004	Mitsubishi
	DM74S04	National
	54S04	† Signetics
	74S04	Signetics
	N8T93	Signetics
	SN54S04	† TI
	SN74S04	TI
Hex Inverter, Open Collector TTL	5405	† Fairchild
	7405	Fairchild
	9017C	Fairchild

(Continued)

Buffers/Inverters (Cont'd)

Function	Device	Source
TTL (Cont'd.)	9017M	† Fairchild
	ZN5405	Ferranti
	ZN7405	Ferranti
	HD2523	Hitachi
	HD7405	Hitachi
	ITT5405	† ITT
	ITT7405	ITT
	M53205	Mitsubishi
	MC5405	† Motorola
	MC7405	Motorola
	DM5405	† National
	DM7405	National
	μPB7405	NEC America
	5405	† Raytheon
	7405	Raytheon
	5405	† Signetics
	N8T90	Signetics
	S8T90	† Signetics
	7405	Signetics
	SN5405	† TI
	SN7405	TI
	TD3405	Toshiba
	7405	TRW
TTL-LS	9LS05C	Fairchild
	9LS05M	† Fairchild
	54LS05	† Fairchild
	74LS05	Fairchild
	ITT74LS05	ITT
	SN54LS05	† Motorola
	SN74LS05	Motorola
	DM54LS05	† National
	DM74LS05	National
	μPB74LS05	NEC America
	9LS05C	Raytheon
	9LS05M	† Raytheon
	54LS05	† Raytheon
	74LS05	Raytheon
	54LS05	† Signetics
	74LS05	Signetics
	SN54LS05	† TI
	SN74LS05	TI
TTL-H	54H05	† Fairchild
	74H05	Fairchild
	ITT54H05	† ITT
	ITT74H05	ITT
	MC3009	Motorola
	MC3109	† Motorola
	DM54H05	† National
	DM74H05	National
	54H05	† Raytheon
	74H05	Raytheon
	54R05	† Raytheon
	74R05	Raytheon
	54H05	† Signetics
	74H05	Signetics
	SN54H05	† TI
	SN74H05	TI
TTL-S	54S05	† Fairchild
	74S05	Fairchild
	9S05AC	Fairchild
	9S05AM	† Fairchild
	HD74S05	Hitachi
	M5S005	Mitsubishi
	DM74S05	National
	54S05	† Signetics
	74S05	Signetics
	N8T94	Signetics

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Buffers/Inverters (Cont'd)

Function	Device	Source
TTL-S (Cont'd.)	SN54S05	† TI
	SN74S05	TI
Hex Inverter, Three State TTL	DM7096	† National
	DM8096	National
	DM7098	† National
	DM8098	National
	DM54366	† National
	DM74366	National
	DM54368	† National
	DM74368	National
	74366	Signetics
	74368	Signetics
	SN54366	† TI
	SN54368	† TI
	SN74366	TI
	SN74368	TI
TTL-LS	9LS366C	Fairchild
	9LS366M	† Fairchild
	9LS368C	Fairchild
	9LS368M	† Fairchild
	54LS366	† Fairchild
	74LS366	Fairchild
	54LS368	† Fairchild
	74LS368	Fairchild
	ITT74LS368	ITT
	SN54LS366	† Motorola
	SN74LS366	Motorola
	SN54LS368	† Motorola
	SN74LS368	Motorola
	DM54LS366	† National
	DM74LS366	National
	DM54LS368	† National
	DM74LS368	National
	μPB74LS366	NEC America
	μPB74LS368	NEC America
	9LS366C	**Raytheon (286)**
	9LS366M	**† Raytheon (286)**
	54LS366	**† Raytheon (286)**
	74LS366	**Raytheon (286)**
	9LS368C	**Raytheon (286)**
	9LS368M	**† Raytheon (286)**
	54LS368	**† Raytheon (286)**
	74LS368	**Raytheon (286)**
	54LS366	† Signetics
	74LS366	Signetics
	54LS368	† Signetics
	74LS368	Signetics
	SN54LS366A	† TI
	SN74LS366A	TI
	SN54LS368A	† TI
	SN74LS368A	TI
TTL-S	MB486	Fujitsu
	MB488	Fujitsu
	MC8T96	Motorola
	MC8T98	Motorola
	N8T96	Signetics
	N8T98	Signetics
Octal Inverter, Three State TTL-LS	DM71LS96	† National
	DM81LS96	National
	DM71LS98	† National
	DM81LS98	National

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Counters, Binary Count Up

Octal (Dual Quad) Inverter (Driver) Hysteresis, Three State. See Octal Bus Drivers under Miscellaneous (Cont'd.)

Function	Device	Source	Line
TTL	5493	† Fairchild	
	7493	Fairchild	
	9305C	Fairchild	
	9305M	† Fairchild	
	9356C	Fairchild	
	54293	† Fairchild	
	74293	Fairchild	
	ZN5493	† Ferranti	
	ZN7493	Ferranti	
	HD2520	Hitachi	
	HD7493	Hitachi	10
	ITT5493	† ITT	
	ITT7493	ITT	
	M5393	Mitsubishi	
	M53293	Mitsubishi	
	M53493	Mitsubishi	
	MC5493	† Motorola	
	MC7493	Motorola	
	MC54293	† Motorola	
	MC74293	Motorola	
	DM5493	† National	20
	DM7493	National	
	5493	† Signetics	
	7493	Signetics	
	SN5493A	† TI	
	SN7493A	TI	
	SN54293	† TI	
	SN74293	TI	
	TD3493	Toshiba	
	7493	TRW	
	74293	TRW	30
TTL-LS	9LS93C	Fairchild	
	9LS93M	† Fairchild	
	9LS293C	Fairchild	
	9LS293M	† Fairchild	
	54LS93	† Fairchild	
	74LS93	Fairchild	
	54LS293	† Fairchild	
	74LS293	Fairchild	
	ITT74LS93	ITT	
	ITT74LS293	ITT	40
	SN54LS93	† Motorola	
	SN74LS93	Motorola	
	SN54LS293	† Motorola	
	SN74LS293	Motorola	
	9LS93C	**Raytheon (268)**	
	9LS93M	**† Raytheon (268)**	
	54LS93	**† Raytheon (268)**	
	74LS93	**Raytheon (268)**	
	54LS93	† Signetics	
	74LS93	Signetics	50
	54LS293	† Signetics	
	74LS293	Signetics	
	SN54LS93	† TI	
	SN74LS93	TI	
	SN54LS293	† TI	
	SN74LS293	TI	

Dual 4 bit Binary Counter, Ripple (Dual 54/7493A)

TTL	SN54393	† TI	
	SN74393	TI	
TTL-LS	9LS393C	Fairchild	
	9LS393M	† Fairchild	
	54LS393	† Fairchild	
	74LS393	Fairchild	
	SN54LS393	† TI	60

(Continued)

Counters, Binary Count Up (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)	SN74LS393	TI	

Binary Counter/Latch (Divide by 2, 4, 8, 16), Preset Input

TTL	54177	† Fairchild	
	74177	Fairchild	70
	54197	Fairchild	
	74197	Fairchild	
	ZN54197	† Ferranti	
	ZN74197	Ferranti	
	HD2573	Hitachi	
	M53377	Mitsubishi	
	MC7281	Motorola	
	MC8281	Motorola	
	MC54177	† Motorola	
	MC74177	Motorola	80
	MC54197	† Motorola	
	MC74197	Motorola	
	DM7281	† National	
	DM8281	National	
	DM7291	† National	
	DM8291	National	
	DM54197	† National	
	DM74197	National	
	DM54177	† National	
	DM74177	National	90
	RC8281	Raytheon	
	RC8291	Raytheon	
	RM8281	† Raytheon	
	RM8291	† Raytheon	
	N8281	Signetics	
	S8281	† Signetics	
	N8291	Signetics	
	S8291	† Signetics	
	74177	Signetics	
	74197	Signetics	100
	SN54177	† TI	
	SN74177	TI	
	SN54197	† TI	
	SN74197	TI	
TTL-LS	9LS197C	Fairchild	
	9LS197M	† Fairchild	
	54LS197	† Fairchild	
	74LS197	Fairchild	
	ITT74LS197	ITT	
	SN54LS197	† Motorola	110
	SN74LS197	Motorola	
	DM54LS197	† National	
	DM74LS197	National	
	9LS197C	Raytheon	
	9LS197M	† Raytheon	
	54LS197	† Raytheon	
	74LS197	Raytheon	
	74LS197	Signetics	
	SN54LS197	† TI	
	SN74LS197	TI	120
TTL-S	74S197	Signetics	
	N82S91	Signetics	
	SN54S197	† TI	
	SN74S197	TI	

Dual Binary Counter, Synchronous

TTL	MC4053	Motorola	
	MC4353	† Motorola	
	MC54453	† Motorola	
	MC74453	Motorola	

Counters, Binary Count Up (Cont'd)

Function	Device	Source	Line

Binary Counter, Synchronous, Preset Input (Synchronous Clear)

TTL	SN54163	† AMD	130
	SN74163	AMD	
	54163	† Fairchild	
	74163	Fairchild	
	ZN54163	† Ferranti	
	ZN74163	Ferranti	
	HD74163	Hitachi	
	ITT54163	† ITT	
	ITT74163	ITT	140
	M53363	Mitsubishi	
	MC54163	† Motorola	
	MC74163	Motorola	
	DM54163	† National	
	DM74163	National	
	54163	† Raytheon	
	74163	Raytheon	
	54163	Signetics	
	74163	Signetics	
	SN54163	† TI	150
	SN74163	TI	
	74163	TRW	
TTL-LS	AM25LS163C	AMD	
	AM25LS163M	† AMD	
	SN54LS163	† AMD	
	SN74LS163	AMD	
	9LS163C	Fairchild	
	9LS163M	† Fairchild	
	54LS163	† Fairchild	
	74LS163	Fairchild	160
	ITT74LS163A	ITT	
	SN54LS163	† Motorola	
	SN74LS163	Motorola	
	DM54LS163	† National	
	DM74LS163	National	
	9LS163C	Raytheon	
	9LS163M	† Raytheon	
	25LS163C	Raytheon	
	25LS163M	† Raytheon	
	54LS163	† Raytheon	170
	74LS163	Raytheon	
	54LS163	† Signetics	
	74LS163	Signetics	
	SN54LS163A	† TI	
	SN74LS163A	TI	

Binary Counter, Synchronous, Preset Input (Asynchronous Clear)

TTL	SN54161	† AMD	
	SN74161	AMD	
	9316C	AMD	180
	9316M	† AMD	
	9316C	Fairchild	
	9316M	† Fairchild	
	54161	† Fairchild	
	74161	Fairchild	
	ZN54161	† Ferranti	
	ZN74161	Ferranti	
	HD74161	Hitachi	
	ITT9316	ITT	
	ITT54161	† ITT	190
	ITT74161	ITT	
	M53361	Mitsubishi	
	MC8316	Motorola	
	MC9316	† Motorola	
	MC54161	† Motorola	
	MC74161	Motorola	
	DM54161	† National	
	DM74161	National	
	DM8316	† National	

(Cont'd.)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Counters, Binary Count Up (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	DM9316	National	
	μPB74161	NEC America	
	RC9316	Raytheon	
	RM9316	† Raytheon	
	54161	† Raytheon	
	74161	Raytheon	
	54161	† Signetics	
	74161	Signetics	10
	9316	Signetics	
	SN29316	TI	
	SN39316	† TI	
	SN54161	† TI	
	SN74161	TI	
	74161	TRW	
TTL-LS	AM25LS161C	AMD	
	AM25LS161M	† AMD	
	SN54LS161	† AMD	
	SN74LS161	AMD	20
	9LS161C	Fairchild	
	9LS161M	† Fairchild	
	54LS161	† Fairchild	
	74LS161	Fairchild	
	ITT74LS161A	ITT	
	SN54LS161	† Motorola	
	SN74LS161	Motorola	
	μPB74LS161	NEC America	
	DM54LS161	† National	
	DM74LS161	National	30
	9LS161C	Raytheon	
	9LS161M	† Raytheon	
	25LS161C	Raytheon	
	25LS161M	† Raytheon	
	54LS161	† Raytheon	
	74LS161	Raytheon	
	54LS161	† Signetics	
	74LS161	Signetics	
	SN54LS161A	† TI	
	SN74LS161A	TI	40
TTL-S	SN54S161	† AMD	
	SN74S161	AMD	
	93S16C	AMD	
	93S16M	† AMD	
	93S16C	Fairchild	
	93S16M	† Fairchild	
	SN54S163	† TI	
	SN74S163	TI	
Binary Counter, Synchronous, Preset Input, Low Power			
TTL	N8293	Signetics	50
	S8293	† Signetics	
Binary Counter, Synchronous (both conventional and three state outputs) Preset Input			
TTL	DM7556	† National	
	DM8556	National	

Counters, Binary, Count Up/Down

Binary Up/Down Counter, Synchronous with mode control			
TTL	N8284	AMD	
	S8284	† AMD	
	AM2501C	AMD	60
	AM2501M	† AMD	
	RC8284	Raytheon	
	RM8284	† Raytheon	
	N8284	Signetics	
	S8284	† Signetics	

Counters, Binary, Count Up/Down (Cont'd)

Binary Up/Down, Synchronous, Preset Input with mode control			
TTL	54191	† Fairchild	
	74191	Fairchild	
	ZN54191	† Ferranti	70
	ZN74191	Ferranti	
	HD74191	Hitachi	
	ITT54191	† ITT	
	ITT74191	ITT	
	M53391	Mitsubishi	
	MC54191	† Motorola	
	MC74191	Motorola	
	DM54191	† National	
	DM74191	National	
	54191	† Raytheon	80
	74191	Raytheon	
	54191	† Signetics	
	74191	Signetics	
	SN54191	† TI	
	SN74191	TI	
TTL-LS	AM25LS191C	AMD	
	AM25LS191M	† AMD	
	SN54LS191	† AMD	
	SN74LS191	AMD	
	9LS191C	Fairchild	90
	9LS191M	† Fairchild	
	54LS191	† Fairchild	
	74LS191	Fairchild	
	ITT74LS191	ITT	
	SN54LS191	† Motorola	
	SN74LS191	Motorola	
	DM54LS191	† National	
	DM74LS191	National	
	9LS191C	Raytheon	
	9LS191M	† Raytheon	100
	25LS191C	Raytheon	
	25LS191M	† Raytheon	
	54LS191	† Raytheon	
	74LS191	Raytheon	
	54LS191	† Signetics	
	74LS191	Signetics	
	SN54LS191	† TI	
	SN74LS191	TI	
Binary Up/Down, Synchronous, Preset Input (2 Clocks)			110
TTL	9366C	AMD	
	9366M	† AMD	
	SN54193	† AMD	
	SN74193	AMD	
	9366C	Fairchild	
	9366M	† Fairchild	
	54193	† Fairchild	
	74193	Fairchild	
	ZN54193	† Ferranti	
	ZN74193	Ferranti	120
	HD2542	Hitachi	
	ITT54193	† ITT	
	ITT74193	ITT	
	M53393	Mitsubishi	
	MC54193	† Motorola	
	MC74193	Motorola	
	DM7563	† National	
	DM8563	National	
	DM54193	† National	
	DM74193	National	130
	μPB74193	NEC America	
	RC9366	Raytheon	
	RM9366	† Raytheon	
	54193	† Raytheon	
	74193	Raytheon	

(Continued)

Counters, Binary, Count Up/Down (Cont'd)

TTL (Cont'd.)			
	54193	† Signetics	
	74193	Signetics	
	SW74193	SW	140
	SN54193	† TI	
	SN74193	TI	
	TD34193	Toshiba	
TTL-LS	AM25LS193C	AMD	
	AM25LS193M	† AMD	
	SN54LS193	† AMD	
	SN74LS193	AMD	
	9LS193C	Fairchild	
	9LS193M	† Fairchild	
	54LS193	† Fairchild	150
	74LS193	Fairchild	
	ITT74LS193	ITT	
	SN54LS193	† Motorola	
	SN74LS193	Motorola	
	DM54LS193	† National	
	DM74LS193	National	
	μPB74LS193	NEC America	
	9LS193C	Raytheon	
	9LS193M	† Raytheon	
	25LS193C	Raytheon	160
	25LS193M	† Raytheon	
	54LS193	† Raytheon	
	74LS193	Raytheon	
	54LS193	Signetics	
	74LS193	Signetics	
	SN54LS193	† TI	
	SN74LS193	TI	
Binary Up/Down Counter, Synchronous, Preset Input, Mode Control, Look ahead Carry			
TTL-LS	AM25LS169C	AMD	170
	AM25LS169M	† AMD	
	SN54LS169	† AMD	
	SN74LS169	AMD	
	9LS169C	Fairchild	
	54LS169	† Fairchild	
	74LS169	Fairchild	
	DM54LS169	† National	
	DM74LS169	National	
	SN54LS169A	† TI	
	SN74LS169A	TI	180
TTL-S	SN54S169	† TI	
	SN74S169	TI	
Binary Up/Down Counter, Three State			
TTL-LS	AM25LS2569C	AMD	
	AM25LS2569M	† AMD	
Dual Binary Up/Down Counter, Synchronous, Preset Input			
TTL	MC4055	Motorola	
	MC4355	† Motorola	
	MC54455	† Motorola	190
	MC74455	Motorola	
4 bit Universal Shift Register, Binary Up/Down Counter, Synchronous			
TTL-S	SN74S291	TI	

Counters, Decade, Count Up

Decade Counter, Divide by 2 and by 5			
TTL	9350C	Fairchild	
	9350M	† Fairchild	
	5490	† Fairchild	
	7490	Fairchild	
	54290	† Fairchild	200

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† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Counters, Decade, Count Up (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)	74290	Fairchild	
	ZN5490	†Ferranti	
	ZN7490	Ferranti	
	HD2519	Hitachi	
	HD7490	Hitachi	
	ITT5490	†ITT	
	ITT7490	ITT	
	M53290	Mitsubishi	
	M53490	Mitsubishi	10
	MC5490	†Motorola	
	MC7490	Motorola	
	MC54290	†Motorola	
	MC74290	Motorola	
	DM5490	†National	
	DM7490	National	
	5490	†Signetics	
	7490	Signetics	
	TL7490S1	Telefunken	
	SN5490A	†TI	20
	SN7490A	TI	
	SN54290	†TI	
	SN74290	TI	
	TD3490	Toshiba	
	7490	TRW	
	74290	TRW	
TTL-LS	9LS90C	Fairchild	
	9LS90M	†Fairchild	
	9LS290C	Fairchild	
	9LS290M	†Fairchild	30
	54LS90	†Fairchild	
	74LS90	Fairchild	
	54LS290	†Fairchild	
	74LS290	Fairchild	
	ITT74LS90	ITT	
	ITT74LS290	ITT	
	SN54LS90	†Motorola	
	SN74LS90	Motorola	
	SN54LS290	†Motorola	
	SN74LS290	Motorola	40
	DM54LS90	†National	
	DM74LS90	National	
	9LS90C	**Raytheon (268)**	
	9LS90M	**†Raytheon (268)**	
	54LS90	**†Raytheon (268)**	
	74LS90	**Raytheon (268)**	
	54LS90	†Signetics	
	74LS90	Signetics	
	54LS290	†Signetics	
	74LS290	Signetics	50
	SN54LS90	†TI	
	SN74LS90	TI	
	SN54LS290	†TI	
	SN74LS290	TI	
Decade (Divide by 2 and Divide by 5) Counter/Latch, Ripple, Preset Input			
TTL	54176	†Fairchild	
	74176	Fairchild	
	54196	†Fairchild	
	74196	Fairchild	60
	M53376	Mitsubishi	
	MC7280	†Motorola	
	MC54176	†Motorola	
	MC74176	Motorola	
	MC54196	†Motorola	
	MC74196	Motorola	
	DM7280	†National	
	DM8280	National	
	DM7290	†National	

(Continued)

Counters, Decade, Count Up (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)	DM8290	National	
	DM54176	†National	
	DM74176	National	
	DM54196	†National	
	DM74196	National	
	RC8280	Raytheon	
	RC8290	Raytheon	
	RM8280	†Raytheon	
	RM8290	†Raytheon	80
	N8280	Signetics	
	N8290	Signetics	
	74176	Signetics	
	74196	Signetics	
	S8280	†Signetics	
	S8290	†Signetics	
	SN54176	†TI	
	SN74176	TI	
	SN54196	†TI	
	SN74196	TI	90
TTL-LS	9LS196C	Fairchild	
	9LS196M	†Fairchild	
	54LS196	†Fairchild	
	74LS196	Fairchild	
	ITT74LS196	ITT	
	SN54LS196	†Motorola	
	SN74LS196	Motorola	
	DM54LS196	†National	
	DM74LS196	National	
	9LS196C	Raytheon	100
	9LS196M	†Raytheon	
	54LS196	†Raytheon	
	74LS196	Raytheon	
	74LS196	†Signetics	
	SN54LS196	†TI	
	SN74LS196	TI	
	N82S90	Signetics	
	SN54S196	†TI	
	SN74S196	TI	
Decade Counter, Synchronous, Preset Input (Asynchronous Clear)			110
TTL	9310C	AMD	
	9310M	†AMD	
	SN54160	†AMD	
	SN74160	AMD	
	9310C	Fairchild	
	9310M	†Fairchild	
	54160	†Fairchild	
	74160	Fairchild	
	HD74160	Hitachi	120
	ITT54160	†ITT	
	ITT74160	ITT	
	M53360	Mitsubishi	
	MC8310	Motorola	
	MC9310	Motorola	
	MC54160	†Motorola	
	MC74160	Motorola	
	DM54160	†National	
	DM74160	National	
	DM8310	National	130
	DM9310	†National	
	54160	†Raytheon	
	74160	Raytheon	
	RC9310	Raytheon	
	RM9310	†Raytheon	
	54160	†Signetics	
	74160	Signetics	
	9310	Signetics	
	SN29310	TI	

(Continued)

Counters, Decade, Count Up (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)	SN39310	TI	
	SN54160	†TI	
	SN74160	TI	
	74160	TRW	
TTL-LS	AM25LS160C	AMD	
	AM25LS160M	†AMD	
	SN54LS160	†AMD	
	SN74LS160	AMD	
	9LS160C	Fairchild	150
	9LS160M	†Fairchild	
	54LS160	†Fairchild	
	74LS160	Fairchild	
	ITT74LS160A	ITT	
	SN54LS160	†Motorola	
	SN74LS160	Motorola	
	DM54LS160	†National	
	DM74LS160	National	
	9LS160C	Raytheon	
	9LS160M	†Raytheon	160
	25LS160C	Raytheon	
	25LS160M	†Raytheon	
	54LS160	†Raytheon	
	74LS160	Raytheon	
	74LS160	Signetics	
	SN54LS160A	†TI	
	SN74LS160A	TI	
TTL-S	SN54S160	†AMD	
	SN74S160	AMD	
	93S10C	AMD	170
	93S10M	†AMD	
	93S10C	Fairchild	
	93S10M	†Fairchild	
Decade Counter, Synchronous, Preset Input (Synchronous Clear)			
TTL	SN54162	†AMD	
	SN74162	AMD	
	54162	†Fairchild	
	74162	Fairchild	
	HD74162	Hitachi	180
	ITT54162	†ITT	
	ITT74162	ITT	
	M53362	Mitsubishi	
	MC54162	†Motorola	
	MC74162	Motorola	
	DM54162	†National	
	DM74162	National	
	54162	†Raytheon	
	74162	Raytheon	
	54162	†Signetics	190
	74162	Signetics	
	SN54162	†TI	
	SN74162	TI	
	74162	TRW	
TTL-LS	AM25LS162C	AMD	
	AM25LS162M	†AMD	
	SN54LS162	†AMD	
	SN74LS162	AMD	
	9LS162C	Fairchild	
	9LS162M	†Fairchild	200
	54LS162	†Fairchild	
	74LS162	Fairchild	
	ITT74LS162A	ITT	
	SN54LS162	†Motorola	
	SN74LS162	Motorola	
	DM54LS162	†National	
	DM74LS162	National	
	9LS162C	Raytheon	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Counters, Decade, Count Up (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)			
	9LS162M	† Raytheon	
	25LS162C	Raytheon	
	25LS162M	† Raytheon	
	54LS162	† Raytheon	
	74LS162	Raytheon	
	74LS162	Signetics	
	SN54LS162A	† TI	
	SN74LS162A	TI	10
TTL-S	SN54S162	† TI	
	SN74S162	TI	
Decade Counter, Synchronous, Preset Input Low Power			
TTL	N8292	Signetics	
	S8292	† Signetics	
Decade Counter, Synchronous (both conventional and three state outputs), Preset Inputs			
TTL	DM7555	† National	
	DM8555	National	20
Decade Counter, 10 line Output (resettable 2 10)			
TTL	9319C	Fairchild	
	9319M	† Fairchild	
	9320C	Fairchild	
	9320M	† Fairchild	
Dual Decade Counter, Synchronous			
TTL	MC54452	† Motorola	
	MC74452	Motorola	
Dual Decade Counter, Ripple (Dual 54/7490A)			
TTL	MC4052	Motorola	30
	MC4352	† Motorola	
	SN54390	† TI	
	SN54490	† TI	
	SN74390	TI	
	SN74490	TI	
TTL-LS	9LS390C	Fairchild	
	54LS390	† Fairchild	
	74LS390	Fairchild	
	9LS490C	Fairchild	
	54LS490	† Fairchild	40
	74LS490	Fairchild	
	74LS390	Signetics	
	SN54LS390	† TI	
	SN74LS390	TI	
	SN54LS490	† TI	
	SN74LS490	TI	

Counters, Decade, Count Up/Down

Function	Device	Source	Line
Decade Up/Down Counter, Synchronous			
TTL	N8285	AMD	
	S8285	† AMD	
	RC8285	Raytheon	50
	RM8285	† Raytheon	
	N8285	Signetics	
	S8285	† Signetics	
Decade Up/Down Counter, Synchronous, Preset, with Mode Control			
TTL	9306C	AMD	
	9306M	† AMD	
	54190	† Fairchild	
	74190	Fairchild	
	HD74190	Hitachi	
	ITT54190	† ITT	
	ITT74190	ITT	60
	M53390	Mitsubishi	
	MC54190	† Motorola	

(Continued)

Counters, Decade, Count Up/Down (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	MC74190	Motorola	
	DM54190	† National	
	DM74190	National	
	54190	† Raytheon	70
	74190	Raytheon	
	54190	† Signetics	
	74190	Signetics	
	SN54190	† TI	
	SN74190	TI	
TTL-LS	AM25LS190C	AMD	
	AM25LS190M	† AMD	
	SN54LS190	† AMD	
	SN74LS190	AMD	
	9LS190C	Fairchild	80
	9LS190M	† Fairchild	
	54LS190	† Fairchild	
	74LS190	Fairchild	
	ITT74LS190	ITT	
	SN54LS190	† Motorola	
	SN74LS190	Motorola	
	DM54LS190	† National	
	DM74LS190	National	
	9LS190C	Raytheon	
	9LS190M	† Raytheon	90
	25LS190C	Raytheon	
	25LS190M	† Raytheon	
	54LS190	† Raytheon	
	74LS190	Raytheon	
	54LS190	† Signetics	
	74LS190	Signetics	
	SN54LS190	† TI	
	SN74LS190	TI	
Decade Up/Down Counter, Synchronous, Preset Input (2 clocks)			100
TTL	9360C	AMD	
	9360M	† AMD	
	SN54192	† AMD	
	SN74192	AMD	
	9360C	Fairchild	
	9360M	† Fairchild	
	54192	† Fairchild	
	74192	Fairchild	
	ZN54192	† Ferranti	
	ZN74192	Ferranti	110
	HD2541	Hitachi	
	ITT54192	† ITT	
	ITT74192	ITT	
	M53392	Mitsubishi	
	MC54192	† Motorola	
	MC74192	Motorola	
	DM7560	† National	
	DM8560	National	
	DM54192	† National	
	DM74192	National	120
	µPB74192	NEC America	
	54192	† Raytheon	
	74192	Raytheon	
	RC9360	Raytheon	
	RM9360	† Raytheon	
	54192	Signetics	
	74192	† Signetics	
	SN54192	† TI	
	SN74192	TI	
	TD34192	Toshiba	130
TTL-LS	AM25LS192C	AMD	
	AM25LS192M	† AMD	
	SN54LS192	† AMD	

(Continued)

Counters, Decade, Count Up/Down (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)			
	SN74LS192	AMD	
	9LS192C	Fairchild	
	9LS192M	† Fairchild	
	54LS192	† Fairchild	
	74LS192	Fairchild	140
	ITT74LS192	ITT	
	SN54LS192	† Motorola	
	SN74LS192	Motorola	
	DM54LS192	† National	
	DM74LS192	National	
	µPB74LS192	NEC America	
	9LS192C	Raytheon	
	9LS192M	† Raytheon	
	25LS192C	Raytheon	
	25LS192M	† Raytheon	150
	54LS192	† Raytheon	
	74LS192	Raytheon	
	54LS192	† Signetics	
	74LS192	Signetics	
	SN54LS192	† TI	
	SN74LS192	TI	
Decade Up/Down Counter, Three State			
TTL-LS	AM25LS2568C	AMD	
	AM25LS2568M	† AMD	
Dual Decade Up/Down Counter, Synchronous, Preset Input			160
TTL	MC4054	Motorola	
	MC4354	† Motorola	
	MC54454	Motorola	
	MC74454	Motorola	
Decade Up/Down Counter, Counter, Synchronous, Preset Input, Mode Control, Look ahead Carry			
TTL-LS	AM25LS168C	AMD	
	AM25LS168M	† AMD	
	SN54LS168	† AMD	170
	SN74LS168	AMD	
	9LS168C	Fairchild	
	54LS168	† Fairchild	
	74LS168	Fairchild	
	DM54LS168	National	
	DM74LS168	National	
	SN54LS168	† TI	
	SN74LS168	TI	
	SN54LS668	† TI	
	SN74LS668	TI	180
TTL-S	SN54S168A	† TI	
	SN74S168A	TI	
Four Decade Counter/Latch/Display Driver (Synchronous, BCD and segment drives)			
TTL	ZN1040E	Ferranti	

Counters, Miscellaneous

Function	Device	Source	Line
4 bit Universal Counter			
TTL	MC4023	Motorola	
Divide By 12 Counter (Divide by 2 and 6), Ripple			
TTL	5492	† Fairchild	
	7492	Fairchild	190
	ZN5492	† Ferranti	
	ZN7492	Ferranti	
	HD2521	Hitachi	
	HD7492	Hitachi	
	ITT5492	† ITT	
	ITT7492	ITT	
	M53292	Mitsubishi	
	MC5492	† Motorola	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Counters, Miscellaneous (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)	MC7492	Motorola	
	DM5492	† National	
	DM7492	National	
	5492	† Signetics	
	7492	Signetics	
	SN5492A	† TI	
	SN7492A	TI	
	TD3492	Toshiba	
	7492	TRW	10
TTL-LS	9LS92C	Fairchild	
	9LS92M	† Fairchild	
	54LS92	† Fairchild	
	74LS92	Fairchild	
	SN54LS92	† Motorola	
	SN74LS92	Motorola	
	DM54LS92	† National	
	DM74LS92	National	
	9LS92C	**Raytheon (268)**	
	9LS92M	**† Raytheon (268)**	20
	54LS92	**† Raytheon (268)**	
	74LS92	**Raytheon (268)**	
	54LS92	† Signetics	
	74LS92	Signetics	
	SN54LS92	† TI	
	SN74LS92	TI	
Divide By 12 Counter (Divide by 2 and 6), Preset Input			
TTL	DM7288	† National	
	DM8288	National	
	N8288	Signetics	30
	S8288	† Signetics	
Programmable Modulo N Binary Counter			
TTL	MC4018	Motorola	
	MC4318	† Motorola	
	MC4019	Motorola	
	MC4319	† Motorola	
Programmable Modulo N Decade Counter			
TTL	MC4016	Motorola	
	MC4316	† Motorola	
	MC4017	Motorola	40
	MC4317	† Motorola	
Binary Counter/Latch, Three State			
TTL	DM7554	† National	
	DM8554	National	
Decade Counter/Latch, Three State			
TTL	DM7552	† National	
	DM8552	National	
Programmable Modulo N Divider (Divide by 2 to 15, Cascadable)			
TTL	DM7520	† National	50
	DM8520	National	
4 bit Variable Modulo Counter (2 and 5, 6, 7, 8, or 10, 12, 14, 16)			
TTL	9305C	Fairchild	
	9305M	† Fairchild	
TTL-S	93S05C	Fairchild	
	93S05M	† Fairchild	
Decade Counter/Latch/7 Segment Decoder			
TTL	MC4050	Motorola	
	MC4350	† Motorola	60
	MC4051	Motorola	
Decade Counter/Latch/Decoder (Nixie Driver)			
TTL	SN74142	TI	

Counters, Miscellaneous (Cont'd)

Function	Device	Source	Line
Decade Counter/Latch LED/Lamp Driver (High Current Output)			
TTL	SN54144	† TI	
	SN74144	TI	
Decade Counter/Latch, LED/Lamp Driver (Constant Current Output)			
TTL	SN54143	† TI	70
	SN74143	TI	
TTL-LS	SN54LS143	† TI	
	SN74LS143	TI	

Decoders

Function	Device	Source	Line
Excess 3 to Decimal (1 of 10) Decoder			
TTL	5443	† Fairchild	
	7443	Fairchild	
	HD2537	Hitachi	
	HD7443	Hitachi	
	ITT5443	† ITT	
	ITT7443	ITT	80
	M53243	Mitsubishi	
	MC5443	† Motorola	
	MC7443	Motorola	
	5443	† Raytheon	
	7443	Raytheon	
	5443	† Signetics	
	7443	Signetics	
	SN5443A	† TI	
	SN7443A	TI	
TTL-LS	**9LS43C**	**Raytheon (266)**	90
	9LS43M	**† Raytheon (266)**	
	54LS43	**† Raytheon (266)**	
	74LS43	**Raytheon (266)**	
Excess 3 Gray to Decimal (1 of 10) Decoder			
TTL	5444	† Fairchild	
	7444	Fairchild	
	HD2538	Hitachi	
	HD7444	Hitachi	
	ITT5444	† ITT	
	ITT7444	ITT	100
	M53244	Mitsubishi	
	MC5444	† Motorola	
	MC7444	Motorola	
	5444	† Raytheon	
	7444	Raytheon	
	5444	† Signetics	
	7444	Signetics	
	SN5444A	† TI	
	SN7444A	TI	
TTL-LS	**9LS44C**	**Raytheon (266)**	110
	9LS44M	**† Raytheon (266)**	
	54LS44	**† Raytheon (266)**	
	74LS44	**Raytheon (266)**	
BCD to Decimal (1 of 10) Decoder			
TTL	9301M	† AMD	
	9301C	AMD	
	5442	† Fairchild	
	7442	Fairchild	
	9301C	Fairchild	
	9301M	† Fairchild	120
	9302C	Fairchild	
	9302M	† Fairchild	
	ZN5442	† Ferranti	
	ZN7442	Ferranti	
	HD2536	Hitachi	
	HD7442	Hitachi	
	ITT5442	† ITT	
	ITT7442	ITT	

(Continued)

Decoders (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)	ITT9301-1	† ITT	130
	ITT9301-5	ITT	
	M53262	Mitsubishi	
	M53242	Mitsubishi	
	MC5442	† Motorola	
	MC7442	Motorola	
	MC8301	Motorola	
	MC9301	† Motorola	
	DM5442	† National	
	DM7442	National	
	DM8301	National	140
	DM9301	† National	
	μPB7442	NEC America	
	5442	† Raytheon	
	7442	Raytheon	
	RC8251	Raytheon	
	RC8252	Raytheon	
	RM8251	† Raytheon	
	RM8252	† Raytheon	
	5442	† Signetics	
	7442	Signetics	150
	N8251	Signetics	
	N8252	Signetics	
	S8251	† Signetics	
	S8252	† Signetics	
	SN29301	TI	
	SN39301	† TI	
	SN5442A	† TI	
	SN7442A	TI	
	TD3441	Toshiba	
	TD3442	Toshiba	160
TTL-LS	9LS42C	Fairchild	
	9LS42M	† Fairchild	
	54LS42	† Fairchild	
	74LS42	Fairchild	
	ITT74LS42	ITT	
	SN54LS42	† Motorola	
	SN74LS42	Motorola	
	DM54LS42	† National	
	DM74LS42	National	
	μPB74LS42	NEC America	170
	9LS42C	**Raytheon (266)**	
	9LS42M	**† Raytheon (266)**	
	54LS42	**† Raytheon (266)**	
	74LS42	**Raytheon (266)**	
	54LS42	† Signetics	
	74LS42	Signetics	
	SN54LS42	† TI	
	SN74LS42	TI	
TTL-S	N82S52	Signetics	
BCD to Decimal (1 of 10) Decoder, Three State			180
TTL-LS	AM25LS2537C	AMD	
	AM25LS2537M	† AMD	
BCD to Binary and Binary to BCD Converter, Open Collector			
TTL	MC4001	Motorola	
BCD to Decimal Decoder/Driver, Open Collector, 15v			
TTL	54145	† Fairchild	
	74145	Fairchild	
	93145C	Fairchild	
	93145M	† Fairchild	190
	HD2555	† Hitachi	
	ITT54145	† ITT	
	ITT74145	ITT	
	M53345	Mitsubishi	
	MC54145	† Motorola	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Decoders (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)	MC74145	Motorola	
	DM54145	† National	
	DM74145	National	
	54145	† Raytheon	
	74145	Raytheon	
	54145	† Signetics	
	74145	Signetics	
	SN54145	† TI	
	SN74145	TI	10
	74145	TRW	
TTL-LS	54LS145	† Fairchild	
	74LS145	Fairchild	
	74LS145	Signetics	
	SN54LS145	† TI	
	SN74LS145	TI	
	SN54LS445	† TI	
	SN74LS445	TI	
BCD to Decimal/Decoder Driver, Open Collector to 30v Output			
TTL	5445	† Fairchild	20
	7445	Fairchild	
	HD2531	Hitachi	
	ITT5445	† ITT	
	ITT7445	ITT	
	M53245	Mitsubishi	
	MC5445	† Motorola	
	MC7445	Motorola	
	DM5445	† National	
	DM7445	National	30
	μPB7445	NEC America	
	5445	† Raytheon	
	7445	Raytheon	
	5445	† Signetics	
	7445	Signetics	
	SN5445	† TI	
	SN7445	TI	
	7445	TRW	
Dual 1 of 4 Decoder/Demultiplexer (Independent Address)			
TTL	9321C	AMD	40
	9321M	† AMD	
	9321C	Fairchild	
	9321M	† Fairchild	
Dual Binary to One Of Four Line Gated Decoder			
TTL	MC4007	Motorola	
	MC4307	† Motorola	
Demultiplexer, (2 Lines In 2 of 4 Out) Three State			
TTL	DM7230	† National	
	DM8230	National	50
Dual 2 Line To 4 Line Decoder/Demultiplexer, Totem Pole Output (or 3 Line to 8 Line Decoder/Demultiplexer)			
TTL	54155	† Fairchild	
	74155	Fairchild	
	ZN54155	† Ferranti	
	ZN74155	Ferranti	
	HD74155	Hitachi	
	ITT54155	† ITT	
	ITT74155	ITT	
	M53355	Mitsubishi	
	MC54155	† Motorola	
	MC74155	Motorola	
	DM54155	† National	
	DM74155	National	
	μPB74185	NEC America	
	54155	† Raytheon	60

(Continued)

Decoders (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)	74155	Raytheon	
	54155	† Signetics	
	74155	Signetics	
	SN54155	† TI	
	SN74155	TI	
	74155	TRW	
TTL-LS	9LS155C	Fairchild	
	9LS155M	† Fairchild	
	54LS155	† Fairchild	
	74LS155	Fairchild	80
	ITT74LS155	ITT	
	SN54LS155	† Motorola	
	SN74LS155	Motorola	
	DM54LS155	† National	
	DM74LS155	National	
	μPB74LS155	NEC America	
	9LS155C	Raytheon	
	9LS155M	† Raytheon	
	54LS155	† Raytheon	
	74LS155	Raytheon	90
	74LS155	Signetics	
	SN54LS155	† TI	
	SN74LS155	TI	
Dual 2 Line to 4 Line Decoder/Demultiplexer, Open Collector (or 3 Line to 8 Line Decoder/Demultiplexer)			
TTL	54156	† Fairchild	
	74156	Fairchild	
	HD74156	Hitachi	
	ITT54156	† ITT	
	ITT74156	ITT	100
	M53356	Mitsubishi	
	MC54156	† Motorola	
	MC74156	Motorola	
	DM54156	† National	
	DM74156	National	
	μPB74156	NEC America	
	54156	† Raytheon	
	74156	Raytheon	
	54156	† Signetics	
	74156	Signetics	110
	SN54156	† TI	
	SN74156	TI	
	74156	TRW	
TTL-LS	9LS156C	Fairchild	
	9LS156M	† Fairchild	
	54LS156	† Fairchild	
	74LS156	Fairchild	
	ITT74LS156	ITT	
	SN54LS156	† Motorola	
	SN74LS156	Motorola	120
	DM54LS156	† National	
	DM74LS156	National	
	9LS156C	Raytheon	
	9LS156M	† Raytheon	
	54LS156	† Raytheon	
	74LS156	Raytheon	
	74LS156	Signetics	
	SN54LS156	† TI	
	SN74LS156	TI	
Dual 2 Line to 4 Line Decoder/Demultiplexer (or 3 Line to 8 Line Decoder/Demultiplexer) Three State			130
TTL-LS	54255	† Raytheon	
	74255	Raytheon	
	9LS255C	Raytheon	
	9LS255M	† Raytheon	
	54LS255	† Raytheon	
	74LS255	Raytheon	

Decoders (Cont'd)

Function	Device	Source	Line
Dual 2 Line to 4 Line Decoder/Demultiplexer			70
TTL-LS	AM25LS139C	AMD	
	AM25LS139M	AMD	140
	SN54LS139	† AMD	
	SN74LS139	AMD	
	9LS139C	Fairchild	
	9LS139M	† Fairchild	
	54LS139	† Fairchild	
	74LS139	Fairchild	
	ITT74LS139	ITT	
	SN54LS139	† Motorola	
	SN74LS139	Motorola	
	DM54LS139	† National	150
	DM74LS139	National	
	μPB74LS139	NEC America	
	9LS139C	Raytheon	
	9LS139M	† Raytheon	
	25LS139C	Raytheon	
	25LS139M	† Raytheon	
	54LS139	† Raytheon	
	74LS139	Raytheon	
	54LS139	† Signetics	
	74LS139	Signetics	160
	SN54LS139	† TI	
	SN74LS139	TI	
TTL-S	93S21C	AMD	
	93S21M	† AMD	
	SN54S139	† AMD	
	SN74S139	AMD	
	54S139	† Fairchild	
	74S139	Fairchild	
	DM74S139	National	
	54S139	† Signetics	170
	74S139	Signetics	
	SN54S139	† TI	
	SN74S139	TI	
Dual 2 Line to 4 Line Decoder/Demultiplexer, Three State			
TTL-LS	AM25LS2539C	AMD	
	AM25LS2539M	† AMD	
3 Line to 8 Line Decoder/Demultiplexer with Input Latches			
TTL-S	93S137C	Fairchild	180
	93S137M	† Fairchild	
3 Line to 8 Line Decoder/Demultiplexer			
TTL-LS	AM25LS138C	AMD	
	AM25LS138M	AMD	
	SN54LS138	† AMD	
	SN74LS138	AMD	
	9LS138C	Fairchild	
	9LS138M	† Fairchild	
	54LS138	† Fairchild	
	74LS138	Fairchild	190
	ITT74LS138	ITT	
	SN54LS138	† Motorola	
	SN74LS138	Motorola	
	DM54LS138	† National	
	DM74LS138	National	
	μPB74LS138	NEC America	
	9LS138C	Raytheon	
	9LS138M	† Raytheon	
	25LS138C	Raytheon	
	25LS138M	† Raytheon	200
	54LS138	† Raytheon	
	74LS138	Raytheon	
	54LS138	† Signetics	
	74LS138	Signetics	
	SN54LS138	† TI	
	SN74LS138	TI	

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† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Decoders (Cont'd)

Function	Device	Source	Line
3 Line to 8 Line Decoder/Demultiplexer (Cont'd.)			
TTL-S	SN54S138	† AMD	
	SN74S138	AMD	
	54S138	† Fairchild	
	74S138	Fairchild	
	3205	Intel	
	M5S138	Mitsubishi	
	DM74S138	National	
	74S138	† Signetics	
	SN54S138	† TI	10
	SN74S138	TI	
3 Line to 8 Line Decoder/Demultiplexer, Control Storage, Three State			
TTL-LS	AM25LS2538C	AMD	
	AM25LS2538M	† AMD	
3 Line to 8 Line Decoder/Demultiplexer, Inverting/Non Inverting, Control Storage			
TTL-LS	AM25LS2536C	AMD	
	AM25LS2536M	† AMD	
Binary to Octal (1 of 8) Decoder			
TTL	9301C	Fairchild	20
	9301M	† Fairchild	
	M54402	Mitsubishi	
	MC4006	Motorola	
	MC4306	† Motorola	
	MC7250	Motorola	
	MC8250	† Motorola	
	AN852	Panasonic	
	RC8250	Raytheon	
	RM8250	† Raytheon	30
	N8250	Signetics	
	S8250	† Signetics	
	9301	Signetics	
TTL-S	N82S50	Signetics	
Binary to Octal Decoder, Non Inverting			
TTL	MC4048	Motorola	
Binary to Octal Decoder, Inverting/Non Inverting, Open Collector			
TTL	MC4038	Motorola	
1 Line to 8 Line Demultiplexer			
TTL	DM7223	† National	40
	DM8223	National	
Binary to 2 of 8 Decoder, Open Collector			
TTL	MC4040	Motorola	
4 Line to 16 Line Decoder/Demultiplexer			
TTL	9311C	AMD	
	9311M	† AMD	
	SN54154	† AMD	
	SN74154	AMD	
	9311C	Fairchild	50
	9311M	† Fairchild	
	54154	† Fairchild	
	74154	Fairchild	
	ZN54154	† Ferranti	
	ZN74154	Ferranti	
	HD2580	Hitachi	
	M53354	Mitsubishi	
	MC8311	Motorola	
	MC9311	† Motorola	
	MC54154	† Motorola	60
	MC74154	Motorola	
	DM54154	† National	
	DM74154	National	
	DM8311	National	
	DM9311	† National	
	μPB74154	NEC America	

(Continued)

Decoders (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	RC9311	Raytheon	
	RM9311	† Raytheon	
	54154	† Raytheon	70
	74154	Raytheon	
	54154	† Signetics	
	74154	Signetics	
	SN29311	TI	
	SN39311	† TI	
	SN54154	† TI	
	SN74154	TI	
	74154	TRW	
TTL-LS	DM54LS154	† National	
	DM74LS154	National	80
	54LS154	† Signetics	
	74LS154	Signetics	
4 Line to 16 Line Decoder/Demultiplexer, Open Collector Output			
TTL	54159	† Raytheon	
	74159	Raytheon	
	SN54159	† TI	
	SN74159	TI	

Drivers

Function	Device	Source	Line
Quad Predriver, Open Collector			
TTL	MC4042	Motorola	90
Quad 2 Input AND Buffer, Open Collector, to 15v Output (High Voltage 54/74109)			
TTL	DS7819	† National	
	DS8819	National	
Hex Buffer/Driver, Open Collector High Voltage Output, to 15v			
TTL	5417	† Fairchild	
	7417	Fairchild	
	HD7417	Hitachi	
	ITT5417	† ITT	100
	ITT7417	ITT	
	M53217	Mitsubishi	
	MC5417	† Motorola	
	MC7417	Motorola	
	DM5417	† National	
	DM7417	National	
	5417	† Signetics	
	7417	Signetics	
	SN5417	† TI	
	SN7417	TI	110
	TD3417	Toshiba	
	7417	TRW	
Hex Buffer/Driver, Open Collector High Voltage Output, to 30v			
TTL	5407	† Fairchild	
	7407	Fairchild	
	HD7407	Hitachi	
	ITT5407	† ITT	
	ITT7407	ITT	
	M53207	Mitsubishi	120
	MC5407	† Motorola	
	MC7407	Motorola	
	DM5407	† National	
	DM7407	National	
	5407	† Signetics	
	7407	Signetics	
	SN5407	† TI	
	SN7407	TI	
	TD3407	Toshiba	
	7407	TRW	130

Drivers (Cont'd)

Function	Device	Source	Line
Hex Inverter Buffer/Driver Open Collector High Voltage Output, to 15v			
TTL	5416	† Fairchild	
	7416	Fairchild	
	HD7416	Hitachi	
	ITT5416	† ITT	
	ITT7416	ITT	
	M53216	Mitsubishi	
	MC5416	† Motorola	
	MC7416	Motorola	140
	DM5416	† National	
	DM7416	National	
	DS7812	† National	
	DS8812	National	
	5416	† Signetics	
	7416	Signetics	
	SN5416	† TI	
	SN7416	TI	
	TD3416	Toshiba	
	7416	TRW	150
Hex Inverter Buffer/Driver, Open Collector High Voltage Output, to 30v			
TTL	5406	† Fairchild	
	7406	Fairchild	
	HD7406	Hitachi	
	ITT5406	† ITT	
	ITT7406	ITT	
	M53206	Mitsubishi	
	MC5406	† Motorola	
	MC7406	Motorola	160
	DM5406	† National	
	DM7406	National	
	5406	† Signetics	
	7406	Signetics	
	SN5406	† TI	
	SN7406	TI	
	TD3406	Toshiba	
	7406	TRW	
Hex High Voltage Interface Driver, Open Collector, to 35v			170
TTL	HD235	† Harris	
	HD535	Harris	
Quad 2 Input NAND Buffer, Open Collector, to 15v Output			
TTL	5426	† Fairchild	
	7426	Fairchild	
	HD2560	Hitachi	
	HD7426	Hitachi	
	ITT5426	† ITT	
	ITT7426	ITT	180
	MC5426	† Motorola	
	MC7426	Motorola	
	DM5426	† National	
	DM7426	National	
	DS7810	† National	
	DS8810	National	
	DS7811	† National	
	DS8811	National	
	5426	† Signetics	
	7426	Signetics	190
	SN5426	† TI	
	SN7426	TI	
	TD3426	Toshiba	
	7426	TRW	
Quad 2 Input NAND Buffer, Open Collector, to 30v Output			
TTL	N8T80	Signetics	
	S8T80	† Signetics	

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Drivers (Cont'd)

Function	Device	Source
4 Input NAND High Voltage, High Current Driver (40 to 50v, sinks 150 to 500ma)		
TTL	SH2001C	Fairchild
	SH2001M	† Fairchild
	SH2002C	Fairchild
	SH2002M	† Fairchild
	SH2200C	Fairchild
	SH2200M	† Fairchild
Quad 2 Input AND Power Driver (to 70v, sinks 300ma)		
TTL	MN204	Micro Net
	MN304	Micro Net
	MN304H	† Micro Net
	UDN-5706A	Sprague
Quad 2 Input AND Power Driver, Open Collector (to 100v, sinks 500ma)		
TTL	UHC/D-400	† Sprague
	UHC/D-406	† Sprague
	UHC/D-500	† Sprague
	UHC/D-506	† Sprague
	UHP-400	Sprague
	UHP-406	Sprague
	UHP-500	Sprague
	UHP-506	Sprague
Quad 2 Input NAND Power Driver, Open Collector (to 100v, sinks 500ma)		
TTL	UHC/D-407	† Sprague
	UHC/D-408	† Sprague
	UHC/D-507	† Sprague
	UHC/D-508	† Sprague
	UHP-407	Sprague
	UHP-408	Sprague
	UHP-507	Sprague
	UHP-508	Sprague
Quad 2 Input NAND Bus Driver, Open Collector, 80ma		
TTL	96101	Fairchild
Quad 2 Input OR Power Driver, Open Collector (to 100v, sinks 500ma)		
TTL	UHC/D-402	† Sprague
	UHC/D-403	† Sprague
	UHC/D-502	† Sprague
	UHC/D-503	† Sprague
	UHP-402	Sprague
	UHP-403	Sprague
	UHP-502	Sprague
	UHP-503	Sprague
Quad 2 Input NOR Power Driver, Open Collector (to 100v, sinks 500ma)		
TTL	UHC/D-432	† Sprague
	UHC/D-433	† Sprague
	UHC/D-532	† Sprague
	UHC/D-533	† Sprague
	UHP-432	Sprague
	UHP-433	Sprague
	UHP-532	Sprague
	UHP-533	Sprague
Quad 2 Input NOR 75 Ohm/50 Ohm Line Driver		
TTL	74128	Signetics
	SN54128	† TI
	SN74128	TI
Hex Interface Inverter, Open Collector, to 30v		
TTL	N8T90	Signetics
	S8T90	† Signetics
Hex Interface Inverter, Open Collector, to 50v or to 50ma)		
TTL	HD234	† Harris
	HD334	† Harris
	HD534	Harris

Drivers (Cont'd)

Function	Device	Source
Quad Bus Driver, Three State		
TTL	RC8T09	Raytheon
	RM8T09	† Raytheon
	N8T09	Signetics
	S8T09	† Signetics
Hex Bus Driver, Gated Enable, Three State		
TTL	DM54365	† National
	DM74365	National
	74365	Signetics
	SN54365	† TI
	SN74365	TI
Hex Bus Driver, Gated Enable, Inverted Three State Output		
TTL	DM54366	† National
	DM74366	National
	74366	Signetics
	SN54366	† TI
	SN74366	TI
Hex Bus Driver, 2 Line and 4 Line Enable, Three State		
TTL	DM54367	† National
	DM74367	National
	74367	Signetics
	SN54367	† TI
	SN74367	TI
Hex Bus Driver, 2 Line and 4 Line Enable, Inverted Three State Output		
TTL	DM54368	† National
	DM74368	National
	74368	Signetics
	SN54368	† TI
	SN74368	TI
Dual 3 Input 3 Output AND Series Terminated Line Driver		
TTL-H	MC3028	Motorola
	MC3128	† Motorola
Dual 3 Input 3 Output NAND Series Terminated Line Driver		
TTL-H	MC3029	Motorola
	MC3129	† Motorola
Dual 4 Input Positive NAND 50 Ohm Line Driver		
TTL-S	54S140	† Fairchild
	74S140	† Fairchild
	HD74S140	Hitachi
	DM74S140	National
	54S140	† Signetics
	74S140	Signetics
	SN54S140	† TI
	SN74S140	TI

Flip-Flops

Function	Device	Source
See Also Interface Memory and Peripheral Drivers		
TTL	9000C	Fairchild
	9000M	† Fairchild
	9001C	Fairchild
	9001M	† Fairchild
	54104	† Fairchild
	74104	Fairchild
	54105	† Fairchild
	74105	Fairchild
	ITT9001	ITT
	μPB74105	NEC America
AND Gated "J K" Master Slave Flip Flop with Preset and Clear		
TTL	5472	† Fairchild
	7472	Fairchild
	ZN5472	† Ferranti

(Continued)

Flip-Flops (Cont'd)

Function	Device	Source
TTL (Cont'd.)		
	ZN7472	Ferranti
	HD2529	Hitachi
	HD7472	Hitachi
	ITT5472	† ITT
	ITT7472	ITT
	M5375	Mitsubishi
	M53272	Mitsubishi
	MC5472	† Motoroia
	MC7472	Motorola
	DM5472	† National
	DM7472	National
	7472	Signetics
	5472	† Signetics
	SN5472	† TI
	SN7472	TI
	TD3472	Toshiba
	7472	TRW
TTL-H	54H72	† Fairchild
	74H72	Fairchild
	ITT54H72	† ITT
	ITT74H72	ITT
	MC3051	Motorola
	MC3151	† Motorola
	DM54H72	† National
	DM74H72	National
	54H72	† Signetics
	74H72	Signetics
	SN54H72	† TI
	SN74H72	TI
AND Gated "J K" Master Slave Flip Flop with Data Lockout		
TTL	SN54110	† TI
	SN74110	TI
AND Gated, Edge Triggered "J K" Flip Flop with Preset and Clear		
TTL	5470	† Fairchild
	7470	Fairchild
	ZN5470	† Ferranti
	ZN7470	Ferranti
	HD2539	Hitachi
	ITT5470	† ITT
	ITT7470	ITT
	M53270	Mitsubishi
	MC5470	† Motorola
	MC7470	Motorola
	DM5470	† National
	DM7470	National
	5470	† Signetics
	7470	Signetics
	N8270	Signetics
	S8270	† Signetics
	SN5470	† TI
	SN7470	TI
"J K" Negative Edge Triggered Flip Flop, AND Input		
TTL-H	54H102	† Fairchild
	74H102	Fairchild
	54H102	† Signetics
	74H102	Signetics
	SN54H102	† TI
	SN74H102	TI
"J K" Master Slave Flip Flop, AND OR Input		
TTL-H	54H71	† Fairchild
	74H71	Fairchild
	DM54H71	† National
	DM74H71	National
	54H71	† Signetics

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Flip-Flops (Cont'd)

Function	Device	Source	Line
TTL-H (Cont'd.)	74H71	Signetics	
	SN54H71	† TI	
	SN74H71	TI	
"J K" Negative Edge Triggered Flip Flop, AND OR Input			
TTL-H	54H101	† Fairchild	
	74H101	Fairchild	
	54H101	† Signetics	
	74H101	Signetics	10
	SN54H101	† TI	
	SN74H101	TI	
Dual "J K" Negative Edge Triggered Flip Flop, with Clear			
TTL-H	54H103	† Fairchild	
	74H103	Fairchild	
	DM54H103	† National	
	DM74H103	National	
	54H103	† Signetics	
	74H103	Signetics	20
	SN54H103	† TI	
	SN74H103	TI	
Dual "J K" Negative Edge Triggered Flip Flop, Preset, Common Clear, Common Clock			
TTL-H	54H108	† Fairchild	
	74H108	Fairchild	
	DM54H108	† National	
	DM74H108	National	
	54R114	† Raytheon	
	74R114	Raytheon	30
	54H108	† Signetics	
	74H108	Signetics	
	SN54H108	† TI	
	SN74H108	TI	
AND "–J–J –K–K" Flip Flop			
TTL-H	MC3052	Motorola	
	MC3152	† Motorola	
Dual "J &K" Flip Flop with Preset, Common Clock and Common Clear			
TTL-LS	ITT74LS78	ITT	40
	DM54LS78	† National	
	DM74LS78	National	
	9LS78C	Raytheon	
	9LS78M	† Raytheon	
	54LS78	Raytheon	
	74LS78	Raytheon	
	54LS78	† Signetics	
	74LS78	Signetics	
	SN54LS78A	† TI	
	SN74LS78A	TI	50
TTL-H	54H78	† Fairchild	
	74H78	Fairchild	
	DM54H78	† National	
	DM74H78	National	
	SN54H78	† TI	
	SN74H78	TI	
Dual "J &K" Positive Edge Triggered Flip Flop, Preset and Clear			
TTL	9024C	Fairchild	
	9024M	† Fairchild	60
	74109	Fairchild	
	ITT9024-1	† ITT	
	ITT9024-5	ITT	
	DM54109	† National	
	DM74109	National	
	54109	† Signetics	

(Continued)

Flip-Flops (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)	74109	Signetics	
	SN54109	† TI	70
	SN74109	TI	
TTL-LS	9LS109C	Fairchild	
	9LS109M	† Fairchild	
	54LS109	† Fairchild	
	74LS109	Fairchild	
	ITT74LS109A	ITT	
	SN54LS109	† Motorola	
	SN74LS109	Motorola	
	DM54LS109	† National	
	DM74LS109	National	80
	μPB74LS109	NEC America	
	9LS109C	Raytheon	
	9LS109M	† Raytheon	
	54LS109	† Raytheon	
	74LS109	Raytheon	
	54LS109	† Signetics	
	74LS109	Signetics	
	SN54LS109A	† TI	
	SN74LS109A	TI	
TTL-S	54S109	† Fairchild	90
	74S109	Fairchild	
Dual "J K" Negative Edge Triggered Flip Flop, Separate Preset and Clock, (no Clear)			
TTL-LS	9LS113C	Fairchild	
	9LS113M	† Fairchild	
	54LS113	† Fairchild	
	74LS113	Fairchild	
	ITT74LS113	ITT	
	DM54LS113	† National	
	DM74LS113	National	100
	μPB74LS113	NEC America	
	9LS113C	Raytheon	
	9LS113M	† Raytheon	
	54LS113	† Raytheon	
	74LS113	Raytheon	
	54LS113	† Signetics	
	74LS113	Signetics	
	SN54LS113A	† TI	
	SN74LS113A	TI	
TTL-S	54S113	† Fairchild	110
	74S113	Fairchild	
	HD74S113	Hitachi	
	M5S113	Mitsubishi	
	SN54S113	† Motorola	
	SN74S113	Motorola	
	DM74S113	National	
	54S113	† Signetics	
	74S113	Signetics	
	SN54S113	† TI	
	SN74S113	TI	120
TTL-H	54R113	† Raytheon	
	74R113	Raytheon	
Dual "J K" Negative Edge Triggered Flip Flop with Preset, Common Clock and Common Clear			
TTL-LS	9LS114C	Fairchild	
	9LS114M	† Fairchild	
	54LS114	† Fairchild	
	74LS114	Fairchild	
	ITT74LS114	ITT	
	SN54LS114	† Motorola	130
	SN74LS114	Motorola	
	DM54LS114	† National	
	DM74LS114	National	
	9LS114C	Raytheon	

(Continued)

Flip-Flops (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)	9LS114M	† Raytheon	
	54LS114	† Raytheon	
	74LS114	Raytheon	
	54LS114	† Signetics	140
	74LS114	Signetics	
	SN54LS114A	† TI	
	SN74LS114A	TI	
TTL-S	54S114	† Fairchild	
	74S114	Fairchild	
	HD74S114	Hitachi	
	M5S114	Mitsubishi	
	DM74S114	National	
	54S114	† Signetics	
	74S114	Signetics	150
	SN54S114	† TI	
	SN74S114	TI	
Dual "J K" Negative Edge Triggered Flip Flop with Preset and Clear			
TTL-LS	9LS112C	Fairchild	
	9LS112M	† Fairchild	
	54LS112	† Fairchild	
	74LS112	Fairchild	
	ITT74LS112	ITT	
	DM54LS112	† National	160
	DM74LS112	National	
	μPB74LS122	NEC America	
	9LS112C	Raytheon	
	9LS112M	† Raytheon	
	54LS112	† Raytheon	
	74LS112	Raytheon	
	54LS112	Signetics	
	74LS112	Signetics	
	SN54LS112A	† TI	
	SN74LS112A	TI	170
TTL-S	54S112	† Fairchild	
	74S112	Fairchild	
	HD74S112	Hitachi	
	M5S112	Mitsubishi	
	SN54S112	† Motorola	
	SN74S112	Motorola	
	DM74S112	National	
	54S112	† Signetics	
	74S112	Signetics	
	SN54S112	† TI	180
	SN74S112	TI	
TTL-H	54H106	† Fairchild	
	74H106	Fairchild	
	DM54H106	† National	
	DM74H106	National	
	54R112	† Raytheon	
	74R112	Raytheon	
	54H106	† Signetics	
	74H106	Signetics	
	SN54H106	† TI	190
	SN74H106	TI	
Dual "J K" Master Slave Flip Flop			
TTL	9020C	Fairchild	
	9020M	† Fairchild	
	ITT9020-1	† ITT	
	ITT9020-5	ITT	
Dual "J K" Master Slave Flip Flop with Clear			
TTL	5473	† Fairchild	
	7473	Fairchild	
	54107	† Fairchild	200
	74107	Fairchild	
	ZN5473	† Ferranti	

(Continued)

† Military Temperature Range (–55° to 125°C)

* Typical Values

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DIGITAL–TTL (Cont'd)

Flip-Flops (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	ZN7473	Ferranti	
	ZN54107	† Ferranti	
	ZN74107	Ferranti	
	HD2530	Hitachi	
	HD74107	Hitachi	
	ITT5473	† ITT	
	ITT7473	ITT	
	ITT54107	† ITT	
	ITT74107	ITT	10
	M5373	Mitsubishi	
	M53273	Mitsubishi	
	M53307	Mitsubishi	
	MC5473	† Motorola	
	MC7473	Motorola	
	MC54107	† Motorola	
	MC74107	Motorola	
	DM5473	† National	
	DM7473	National	
	DM54107	† National	20
	DM74107	National	
	µPB7473	NEC America	
	µPB74107	NEC America	
	5473	† Signetics	
	7473	Signetics	
	54107	† Signetics	
	74107	Signetics	
	SN5473	† TI	
	SN7473	† TI	
	SN54107	† TI	30
	SN74107	TI	
	TD3473	Toshiba	
	TD34107	Toshiba	
TTL-LS	9LS73C	Fairchild	
	9LS73M	† Fairchild	
	54LS73	† Fairchild	
	74LS73	Fairchild	
	54LS107	† Fairchild	
	74LS107	Fairchild	
	ITT74LS73	ITT	40
	ITT74LS107	ITT	
	SN54LS73	† Motorola	
	SN74LS73	Motorola	
	DM54LS73	† National	
	DM74LS73	National	
	DM54LS107	† National	
	DM74LS107	National	
	9LS73C	Raytheon	
	9LS73M	† Raytheon	
	54LS73	† Raytheon	50
	74LS73	Raytheon	
	9LS107C	Raytheon	
	9LS107M	† Raytheon	
	54LS107	† Raytheon	
	74LS107	Raytheon	
	54LS73	† Signetics	
	74LS73	Signetics	
	54LS107	† Signetics	
	74LS107	Signetics	
	SN54LS73A	† TI	60
	SN74LS73A	TI	
	SN54LS107A	† TI	
	SN74LS107A	TI	
TTL-H	54H73	† Fairchild	
	74H73	Fairchild	
	ITT54H73	† ITT	
	ITT74H73	ITT	
	MC3061	Motorola	
	MC3062	Motorola	

(Continued)

Flip-Flops (Cont'd)

Function	Device	Source	Line
TTL-H (Cont'd.)			
	MC3161	† Motorola	70
	MC3162	† Motorola	
	DM54H73	† National	
	DM74H73	National	
	54H73	† Signetics	
	74H73	Signetics	
	SN54H73	† TI	
	SN74H73	TI	
Dual "J K" Master Slave Flip Flop with Preset and Clear			
TTL	5476	† Fairchild	80
	7476	Fairchild	
	9022C	Fairchild	
	9022M	† Fairchild	
	ZN5476	† Ferranti	
	ZN7476	Ferranti	
	HD2516	Hitachi	
	ITT5476	† ITT	
	ITT7476	ITT	
	ITT9022-1	ITT	90
	ITT9022-5	ITT	
	M5376	Mitsubishi	
	M53276	Mitsubishi	
	MC5476	† Motorola	
	MC7476	Motorola	
	DM5476	† National	
	DM7476	National	
	µPB7476	NEC America	
	7476	Signetics	
	5476	† Signetics	100
	SN5476	† TI	
	SN7476	TI	
	TD3476	Toshiba	
	7476	TRW	
TTL-LS	ITT74LS76	ITT	
	DM54LS76	† National	
	DM74LS76	National	
	9LS76C	Raytheon	
	9LS76M	† Raytheon	
	54LS76	† Raytheon	110
	74LS76	Raytheon	
	54LS76	† Signetics	
	74LS76A	Signetics	
	SN54LS76A	† TI	
	SN74LS76	TI	
TTL-H	54H76	† Fairchild	
	74H76	Fairchild	
	DM54H76	† National	
	DM74H76	National	
	54H76	† Signetics	120
	74H76	Signetics	
	SN54H76	† TI	
	SN74H76	TI	
Dual "J K" Master Slave Flip Flop with Data Lockout			
TTL	SN74111	TI	
	74111	TRW	
Dual Gated Master Slave "J K/D" Flip Flop			
TTL	DM7512	† National	
	DM8512	National	
Quad "J &K" Edge Triggered Flip Flop with Clear			130
TTL	SN54376	† TI	
	SN74376	TI	
Quad "J &K" Edge Triggered Flip Flop with Preset and Clear			
TTL	SN74276	TI	

Flip-Flops (Cont'd)

Function	Device	Source	Line
Dual D Type Flip Flop			
TTL	MC5479	† Motorola	
	MC7479	Motorola	
Dual D Type Positive Edge Triggered Flip Flop with Preset and Clear			140
TTL	5474	† Fairchild	
	7474	Fairchild	
	ZN5474	† Ferranti	
	ZN7474	Ferranti	
	HD2510	Hitachi	
	HD7474	Hitachi	
	ITT5474	† ITT	
	ITT7474	ITT	
	M5374	Mitsubishi	
	M53274	Mitsubishi	150
	MC5474	† Motorola	
	MC7474	Motorola	
	DM5474	† National	
	DM7474	National	
	µPB7474	NEC America	
	5474	† Raytheon	
	7474	Raytheon	
	5474	† Signetics	
	7474	Signetics	
	SN5474	† TI	160
	SN7474	TI	
	TD3474	Toshiba	
	7474	TRW	
TTL-LS	9LS74C	Fairchild	
	9LS74M	† Fairchild	
	54LS74	† Fairchild	
	74LS74	Fairchild	
	ITT74LS74	ITT	
	SN54LS74	† Motorola	
	SN74LS74	Motorola	170
	DM54LS74	† National	
	DM74LS74	National	
	µPB74LS74	NEC America	
	9LS74C	Raytheon	
	9LS74M	† Raytheon	
	54LS74	† Raytheon	
	74LS74	Raytheon	
	54LS74	† Signetics	
	74LS74	Signetics	
	SN54LS74A	† TI	180
	SN74LS74A	TI	
TTL-H	54H74	† Fairchild	
	74H74	Fairchild	
	ITT54H74	† ITT	
	ITT74H74	ITT	
	MC3060	Motorola	
	MC3160	† Motorola	
	DM54H74	† National	
	DM74H74	National	
	54H74	† Raytheon	190
	74H74	Raytheon	
	54R74	† Raytheon	
	74R74	Raytheon	
	54H74	† Signetics	
	74H74	Signetics	
	SN54H74	† TI	
	SN74H74	TI	
TTL-S	54S74	† Fairchild	
	74S74	Fairchild	
	HD74S74	Hitachi	200
	M5S074	Mitsubishi	
	DM74S74	National	
	54S74	† Signetics	
	74S74	Signetics	

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† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Flip-Flops (Cont'd)

Function	Device	Source	Line
TTL-S (Cont'd.)	SN54S74	† TI	
	SN74S74	TI	
Dual Gated D Flip Flop			
TTL	DM7511	† National	
	DM8511	National	
Quad Gated D Flip Flop			
TTL	DM7613	† National	
	DM8613	National	10
Quad D Type Flip Flop, Common Clock			
TTL	MC4015	Motorola	
Quad D Type Flip Flop, Three State			
TTL	54173	† Fairchild	
	74173	Fairchild	
	DM54173	† National	
	DM74173	National	
	DM7551	† National	
	DM8551	National	
	RC8T10	Raytheon	20
	RM8T10	† Raytheon	
	N8T10	Signetics	
	S8T10	† Signetics	
	74173	Signetics	
	SN54173	† TI	
	SN74173	TI	
TTL-LS	9LS173C	Fairchild	
	9LS173M	† Fairchild	
	54LS173	† Fairchild	
	74LS173	Fairchild	30
	DM54LS173	† National	
	DM74LS173	National	
	54LS173	† Signetics	
	74LS173	Signetics	
	SN54LS173	† TI	
	SN74LS173	TI	
Quad D Type Edge Triggered Flip Flop with Clear, Complementary Output			
TTL	SN54175	† AMD	
	SN74175	AMD	40
	54175	† Fairchild	
	74175	Fairchild	
	ZN54175	† Ferranti	
	ZN74175	Ferranti	
	HD74175	Hitachi	
	M53375	Mitsubishi	
	MC54175	† Motorola	
	MC74175	Motorola	
	DM54175	† National	
	DM74175	National	50
	μPB74175	NEC America	
	54175	† Raytheon	
	74175	Raytheon	
	54175	† Signetics	
	74175	Signetics	
	SN54175	† TI	
	SN74175	TI	
TTL-LS	AM25LS175C	AMD	
	AM25LS175M	AMD	
	SN54LS175	† AMD	60
	SN74LS175	AMD	
	9LS175C	Fairchild	
	9LS175M	† Fairchild	
	54LS175	† Fairchild	
	74LS175	Fairchild	
	ITT74LS175	ITT	
	SN54LS175	† Motorola	

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Flip-Flops (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)	SN74LS175	Motorola	70
	DM54LS175	† National	
	DM74LS175	National	
	μPB74LS175	NEC America	
	9LS175M	† Raytheon	
	9LS175C	Raytheon	
	25LS175C	Raytheon	
	25LS175M	† Raytheon	
	54LS175	† Raytheon	
	74LS175	Raytheon	
	54LS175	† Signetics	80
	74LS175	Signetics	
	SN54LS175	† TI	
	SN74LS175	TI	
TTL-S	SN54S175	† AMD	
	SN74S175	AMD	
	54S175	† Fairchild	
	74S175	Fairchild	
	HD74S175	Hitachi	
	M5S175	Mitsubishi	
	DM74S175	National	90
	74S175	Signetics	
	SN74S175	TI	
	SN54S175	† TI	
Quad D Type Flip Flop with Common Clock Enable			
TTL-LS	AM25LS08C	AMD	
	AM25LS08M	† AMD	
	SN54LS379	† AMD	
	SN74LS379	AMD	
	SN54LS379	† TI	
	SN74LS379	TI	100
TTL-S	AM25S08C	AMD	
	AM25S08M	† AMD	
Quad D Type Flip Flop, Standard TTL and Three State Outputs			
TTL	AM2918C	AMD	
	AM2918M	† AMD	
	μPB2918	**NEC Micro (1850)**	
	AM2918C	Raytheon	
	AM2918M	† Raytheon	
TTL-LS	AM25LS2518C	AMD	110
	AM25LS2518M	† AMD	
	SN54LS388	† AMD	
	SN74LS388	AMD	
TTL-S	AM25S18C	AMD	
	AM25S18M	† AMD	
Quad D type Flip Flop, Dual Three State Outputs			
TTL-LS	AM25LS2519C	AMD	
	AM25LS2519M	† AMD	
Quad D Type Flip Flop with Multiplexed Dual Inputs			
TTL	54298	† Fairchild	120
	74298	Fairchild	
	MC54298	† Motorola	
	MC74298	Motorola	
	54298	† Signetics	
	74298	Signetics	
	SN54298	† TI	
	SN74298	TI	
TTL-LS	AM25LS09C	AMD	
	AM25LS09M	† AMD	
	SN54LS399	† AMD	130
	SN74LS399	AMD	
	9LS298C	Fairchild	
	9LS298M	† Fairchild	
	54LS298	† Fairchild	

(Continued)

Flip-Flops (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)	74LS298	Fairchild	
	SN54LS298	† Motorola	
	SN74LS298	Motorola	
	9LS298C	Raytheon	
	9LS298M	† Raytheon	140
	54LS298	† Raytheon	
	74LS298	Raytheon	
	74LS298	Signetics	
	SN54LS298	† TI	
	SN74LS298	TI	
	SN54LS398	† TI	
	SN74LS398	TI	
	SN54LS399	† TI	
	SN74LS399	TI	
TTL-S	AM25S09C	AMD	150
	AM25S09M	† AMD	
Hex D Type Flip Flop with Common Enable			
TTL-LS	AM25LS07C	AMD	
	AM25LS07M	† AMD	
	SN54LS378	† AMD	
	SN74LS378	AMD	
	ITT74LS378	ITT	
	74LS378	Signetics	
	SN54LS378	† TI	
	SN74LS378	TI	160
TTL-S	AM25S07C	AMD	
	AM25S07M	† AMD	
Hex D Type Edge Triggered Flip Flop with Clear			
TTL	SN54174	† AMD	
	SN74174	AMD	
	54174	† Fairchild	
	74174	Fairchild	
	93174C	Fairchild	
	ZN54174	† Ferranti	
	ZN74174	Ferranti	170
	HD74174	Hitachi	
	M53374	Mitsubishi	
	MC54174	† Motorola	
	MC74174	Motorola	
	DM54174	† National	
	DM74174	National	
	54174	† Raytheon	
	74174	Raytheon	
	54174	† Signetics	
	74174	Signetics	180
	SN54174	† TI	
	SN74174	TI	
TTL-LS	AM25LS174C	AMD	
	AM25LS174M	† AMD	
	SN54LS174	† AMD	
	SN74LS174	AMD	
	9LS174C	Fairchild	
	9LS174M	† Fairchild	
	54LS174	† Fairchild	
	74LS174	Fairchild	190
	ITT74LS174	ITT	
	SN74LS174	Motorola	
	DM54LS174	† National	
	DM74LS174	National	
	9LS174C	Raytheon	
	9LS174M	† Raytheon	
	25LS174C	Raytheon	
	25LS174M	† Raytheon	
	54LS174	† Raytheon	
	74LS174	Raytheon	200
	54LS174	† Signetics	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

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DIGITAL–TTL (Cont'd)

Flip-Flops (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)	74LS174	Signetics	
	SN54LS174	† TI	
	SN74LS174	TI	
TTL-S	SN54S174	† AMD	
	SN74S174	AMD	
	54S174	† Fairchild	
	74S174	Fairchild	
	HD74S174	Hitachi	
	M5S174	Mitsubishi	10
	DM74S174	National	
	54S174	† Signetics	
	74S174	Signetics	
	SN54S174	† TI	
	SN74S174	TI	
Octal D Type, Edge Triggered Flip Flop, with Clear			
TTL	SN74273	TI	
TTL-LS	AM25LS273C	AMD	
	AM25LS273M	† AMD	
	SN54LS273	† AMD	20
	SN74LS273	AMD	
	ITT74LS273	ITT	
	74LS273	Signetics	
	SN54LS273	† TI	
	SN74LS273	TI	
Octal D Type Edge Triggered Flip Flop, Three State			
TTL-LS	AM25LS374C	AMD	
	AM25LS374M	† AMD	
	SN54LS374	† AMD	
	SN74LS374	AMD	30
	74LS374	**Raytheon** (288)	
	54LS374	MMI	
	74LS374	MMI	
	57LS376	† MMI	
	67LS376	MMI	
	SN54LS364	† TI	
	SN74LS364	TI	
	SN54LS374	† TI	
	SN74LS374	TI	
TTL-S	**54S374**	**† MMI** (460)	40
	74S374	**MMI** (460)	
	54S374	**† MMI** (460)	
	74S374	**MMI** (460)	
	57S376	**† MMI** (460)	
	67S376	**MMI** (460)	
	57S378	**† MMI** (460)	
	67S378	**MMI** (460)	
	SN54S374	† TI	
	SN74S374	TI	
Octal D Type Flip Flop with Enable			50
TTL-LS	AM25LS377C	AMD	
	AM25LS377M	† AMD	
	SN54LS377	† AMD	
	SN74LS377	AMD	
	ITT74LS377	ITT	
	54LS377	† Fairchild	
	74LS377	Fairchild	
	54LS377	**† Raytheon** (288)	
	74LS377	**Raytheon** (288)	
	SN54LS377	† TI	60
	SN74LS377	TI	
Octal D type Flip Flop, Common Clear and Enable, Three State			
TTL-LS	AM25LS2520C	AMD	
	AM25LS2520M	† AMD	

Flip-Flops (Cont'd)

Function	Device	Source	Line
Quad I/O Register, Three State (two terminals per flip flop can be used as input or output)			
TTL	DM7542	† National	
	DM8542	National	

Gates, AND/NAND

Dual 4 Input AND Gate			
TTL	5421	† Fairchild	70
	7421	Fairchild	
	ITT5421	† ITT	
	ITT7421	ITT	
	5421	† Raytheon	
	7421	Raytheon	
	5421	† Signetics	
	7421	Signetics	
	TD3421	Toshiba	
TTL-LS	9LS21C	Fairchild	80
	9LS21M	† Fairchild	
	54LS21	† Fairchild	
	74LS21	Fairchild	
	ITT74LS21	ITT	
	SN54LS21	† Motorola	
	SN74LS21	Motorola	
	DM54LS21	† National	
	DM74LS21	National	
	µPB74LS21	NEC America	
	9LS21C	Raytheon	90
	9LS21M	† Raytheon	
	54LS21	† Raytheon	
	74LS21	Raytheon	
	54LS21	† Signetics	
	74LS21	Signetics	
	SN54LS21	† TI	
	SN74LS21	TI	
TTL-H	54H21	† Fairchild	
	74H21	Fairchild	
	ITT54H21	† ITT	100
	ITT74H21	ITT	
	MC3011	Motorola	
	MC3111	† Motorola	
	DM54H21	† National	
	DM74H21	National	
	54H21	† Signetics	
	74H21	Signetics	
	SN74H21	† TI	
	SN74H21	TI	
Dual 4 Input AND Power Gate			110
TTL-H	MC3026	Motorola	
	MC3126	† Motorola	
Triple 3 Input AND Gate			
TTL	5411	† Fairchild	
	7411	Fairchild	
	ITT5411	† ITT	
	ITT7411	ITT	
	DM5411	† National	
	DM7411	National	
	5411	† Raytheon	120
	7411	Raytheon	
	5411	† Signetics	
	7411	Signetics	
TTL-LS	9LS11C	Fairchild	
	9LS11M	† Fairchild	
	54LS11	† Fairchild	
	74LS11	Fairchild	
	ITT74LS11	ITT	
	SN54LS11	† Motorola	
	SN74LS11	Motorola	130

(Continued)

Gates, AND/NAND (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)	DM54LS11	† National	
	DM74LS11	National	
	µPB74LS11	NEC America	
	9LS11C	Raytheon	
	9LS11M	† Raytheon	
	54LS11	† Raytheon	
	74LS11	Raytheon	
	54LS11	† Signetics	
	74LS11	Signetics	140
	SN54LS11	TI	
	SN74LS11	† TI	
TTL-H	54H11	† Fairchild	
	74H11	Fairchild	
	ITT54H11	† ITT	
	ITT74H11	ITT	
	MC3006	Motorola	
	MC3106	† Motorola	
	DM54H11	† National	
	DM74H11	National	150
	54H11	† Raytheon	
	74H11	Raytheon	
	54R11	† Raytheon	
	74R11	Raytheon	
	54H11	† Signetics	
	74H11	Signetics	
	SN54H11	† TI	
	SN74H11	TI	
TTL-S	54S11	† Fairchild	
	74S11	Fairchild	160
	HD74S11	Hitachi	
	M5S011	Mitsubishi	
	DM74S11	National	
	54S11	† Signetics	
	74S11	Signetics	
	SN54S11	† TI	
	SN74S11	TI	
Triple 3 Input AND Gate, Open Collector			
TTL	5415	† Raytheon	
	7415	Raytheon	170
TTL-LS	9LS15C	Fairchild	
	9LS15M	† Fairchild	
	54LS15	† Fairchild	
	74LS15	Fairchild	
	ITT74LS15	ITT	
	SN54LS15	† Motorola	
	SN74LS15	Motorola	
	DM54LS15	† National	
	DM74LS15	National	
	9LS15C	Raytheon	180
	9LS15M	† Raytheon	
	54LS15	† Raytheon	
	74LS15	Raytheon	
	54LS15	† Signetics	
	74LS15	Signetics	
	SN54LS15	† TI	
	SN74LS15	TI	
TTL-H	54H15	† Fairchild	
	74H15	Fairchild	
	54H15	† Raytheon	190
	74H15	Raytheon	
	54R15	† Raytheon	
	74R15	Raytheon	
	SN54H15	† TI	
	SN74H15	TI	
TTL-S	54S15	† Fairchild	
	74S15	Fairchild	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Gates, AND/NAND (Cont'd)

Function	Device	Source	Line
TTL-S (Cont'd.)			
	HD74S15	Hitachi	
	M5S015	Mitsubishi	
	DM74S15	National	
	54S15	† Signetics	
	74S15	Signetics	
	SN54S15	† TI	
	SN74S15	TI	
Quad 2 Input AND Gate			
TTL	5408	† Fairchild	10
	7408	Fairchild	
	ZN5408	† Ferranti	
	ZN7408	Ferranti	
	HD2550	Hitachi	
	ITT5408	† ITT	
	ITT7408	ITT	
	M53208	Mitsubishi	
	MC5408	† Motorola	
	MC7408	Motorola	
	DM5408	† National	20
	DM7408	National	
	5408	† Raytheon	
	7408	Raytheon	
	5408	† Signetics	
	7408	Signetics	
	SN5408	† TI	
	SN7408	TI	
	TD3408	Toshiba	
	7408	TRW	
TTL-LS	9LS08C	Fairchild	30
	9LS08M	† Fairchild	
	54LS08	† Fairchild	
	74LS08	Fairchild	
	ITT74LS08	ITT	
	SN54LS08	† Motorola	
	SN74LS08	Motorola	
	DM54LS08	† National	
	DM74LS08	National	
	μPB74LS08	NEC America	
	9LS08C	Raytheon	40
	9LS08M	† Raytheon	
	54LS08	† Raytheon	
	74LS08	Raytheon	
	54LS08	† Signetics	
	74LS08	Signetics	
	SN54LS08	† TI	
	SN74LS08	TI	
TTL-H	54H08	† Fairchild	
	74H08	Fairchild	
	MC3001	Motorola	50
	MC3101	† Motorola	
	DM54H08	† National	
	DM74H08	National	
	54H08	† Signetics	
	74H08	Signetics	
TTL-S	54S08	† Fairchild	
	74S08	Fairchild	
	54S08	† Signetics	
	74S08	Signetics	
	SN54S08	† TI	60
	SN74S08	TI	
Quad 2 Input AND Gate, Open Collector			
TTL	5409	† Fairchild	
	7409	Fairchild	
	ZN5409	Ferranti	
	ZN7409	Ferranti	
	HD2551	Hitachi	

(Continued)

Gates, AND/NAND (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	ITT5409	† ITT	
	ITT7409	ITT	70
	M53209	Mitsubishi	
	MC5409	† Motorola	
	MC7409	Motorola	
	DM5409	† National	
	DM7409	National	
	5409	† Raytheon	
	7409	Raytheon	
	5409	† Signetics	
	7409	Signetics	
	SN5409	† TI	80
	SN7409	TI	
	TD3409	Toshiba	
	7409	TRW	
TTL-LS	9LS09C	Fairchild	
	9LS09M	† Fairchild	
	54LS09	† Fairchild	
	74LS09	Fairchild	
	ITT74LS09	ITT	
	SN54LS209	† Motorola	
	SN74LS209	Motorola	90
	DM54LS09	† National	
	DM74LS09	National	
	9LS09C	Raytheon	
	9LS09M	† Raytheon	
	54LS09	† Raytheon	
	74LS09	Raytheon	
	54LS09	† Signetics	
	74LS09	Signetics	
	SN54LS09	† TI	
	SN74LS09	† TI	100
TTL-H	54H09	† Fairchild	
	74H09	Fairchild	
TTL-S	54S09	† Fairchild	
	74S09	Fairchild	
	54S09	† Signetics	
	74S09	Signetics	
	SN54S09	† TI	
	SN74S09	TI	
2 2 3 3 Input AND Gate			
TTL-S	9S41C	Fairchild	110
	9S41M	† Fairchild	
8 Input NAND Gate			
TTL	5430	† Fairchild	
	7430	Fairchild	
	9007C	Fairchild	
	9007M	† Fairchild	
	ZN5430	† Ferranti	
	ZN7430	Ferranti	
	HD2508	Hitachi	
	HD7430	Hitachi	120
	ITT5430	† ITT	
	ITT7430	ITT	
	M53230	Mitsubishi	
	MC5430	† Motorola	
	MC7430	Motorola	
	DM5430	† National	
	DM7430	National	
	μPB7430	NEC America	
	5430	† Signetics	
	7430	Signetics	130
	SN5430	† TI	
	SN7430	TI	
	TD3430	Toshiba	
	7430	TRW	

(Continued)

Gates, AND/NAND (Cont'd)

Function	Device	Source	Line
8 Input NAND Gate (Cont'd.)			
TTL-LS	9LS30C	Fairchild	
	9LS30M	† Fairchild	
	54LS30	† Fairchild	
	74LS30	Fairchild	
	ITT74LS30	ITT	140
	SN54LS30	† Motorola	
	SN74LS30	Motorola	
	DM54LS30	† National	
	DM74LS30	National	
	μPB74LS30	NEC America	
	9LS30C	Raytheon	
	9LS30M	† Raytheon	
	54LS30	† Raytheon	
	74LS30	Raytheon	
	54LS30	† Signetics	150
	74LS30	Signetics	
	SN54LS30	† TI	
	SN74LS30	TI	
TTL-H	54H30	† Fairchild	
	74H30	Fairchild	
	ITT54H30	† ITT	
	ITT74H30	ITT	
	MC3015	Motorola	
	MC3016	Motorola	
	MC3115	† Motorola	160
	MC3116	† Motorola	
	DM54H30	† National	
	DM74H30	National	
	μPB74H30	NEC America	
	54H30	† Signetics	
	74H30	Signetics	
	SN54H30	† TI	
	SN74H30	TI	
TTL-S	54S30	† Fairchild	
	74S30	Fairchild	170
	M5S030	Mitsubishi	
	DM74S30	National	
	SN54S30	† TI	
	SN74S30	TI	
12 Input NAND Gate, Three State			
TTL-S	54S134	† Fairchild	
	74S134	Fairchild	
	HD74S134	Hitachi	
	DM74S134	National	
	54S134	† Signetics	180
	74S134	Signetics	
	SN54S134	† TI	
	SN74S134	TI	
13 Input NAND Gate			
TTL-LS	9LS133C	Fairchild	
	9LS133M	† Fairchild	
	54LS133	† Fairchild	
	74LS133	Fairchild	
	ITT74LS133	ITT	
TTL-S	54S133	† Fairchild	190
	HD74S133	Hitachi	
	74S133	Fairchild	
	M5S133	Mitsubishi	
	DM74S133	National	
	54S133	† Signetics	
	74S133	Signetics	
	SN54S133	† TI	
	SN74S133	TI	
Dual 4 Input NAND Gate			
TTL	5420	† Fairchild	200
	7420	Fairchild	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Gates, AND/NAND (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)	9004C	Fairchild	
	9004M	† Fairchild	
	ZN7420	Ferranti	
	ZN5420	† Ferranti	
	HD2504	Hitachi	
	HD7420	Hitachi	
	ITT5420	† ITT	
	ITT7420	ITT	
	ITT9004-1	ITT	10
	ITT9004-5	† ITT	
	M53220	Mitsubishi	
	MC5420	† Motorola	
	MC7420	Motorola	
	DM5420	† National	
	DM7420	National	
	DM9004C	National	
	μPB7420	NEC America	
	5420	† Raytheon	
	7420	Raytheon	20
	5420	† Signetics	
	7420	Signetics	
	SN5420	† TI	
	SN7420	TI	
	TD3420	Toshiba	
	7420	TRW	
TTL-LS	9LS20C	Fairchild	
	9LS20M	† Fairchild	
	54LS20	† Fairchild	
	74LS20	Fairchild	30
	ITT74LS20	ITT	
	SN54LS20	† Motorola	
	SN74LS20	Motorola	
	DM54LS20	† National	
	DM74LS20	National	
	μPB74LS20	NEC America	
	9LS20C	Raytheon	
	9LS20M	† Raytheon	
	54LS20	† Raytheon	
	74LS20	Raytheon	40
	54LS20	† Signetics	
	74LS20	Signetics	
	SN54LS20	† TI	
	SN74LS20	TI	
TTL-H	54H20	† Fairchild	
	74H20	Fairchild	
	ITT54H20	† ITT	
	ITT74H20	ITT	
	MC3010	Motorola	
	MC3110	† Motorola	50
	DM54H20	† National	
	DM74H20	National	
	μPB74H20	NEC America	
	54H20	† Raytheon	
	74H20	Raytheon	
	54R20	† Raytheon	
	74R20	Raytheon	
	54H20	† Signetics	
	74H20	Signetics	
	SN54H20	† TI	60
	SN74H20	TI	
TTL-S	54S20	† Fairchild	
	74S20	Fairchild	
	ZN54S20	† Ferranti	
	ZN74S20	Ferranti	
	HD74S20	Hitachi	
	M5S020	Mitsubishi	
	DM74S20	National	

(Continued)

Gates, AND/NAND (Cont'd)

Function	Device	Source	Line
TTL-S (Cont'd.)	54S20	† Signetics	70
	74S20	Signetics	
	SN54S20	† TI	
	SN74S20	TI	
Dual 4 Input NAND Buffer			
TTL	5440	† Fairchild	
	7440	Fairchild	
	9009C	Fairchild	
	9009M	† Fairchild	
	ZN5440	† Ferranti	
	ZN7440	Ferranti	80
	HD2501	Hitachi	
	HD7440	Hitachi	
	ITT5440	† ITT	
	ITT7440	ITT	
	ITT9009-1	† ITT	
	ITT9009-5	ITT	
	M53240	Mitsubishi	
	MC5440	† Motorola	
	MC7440	Motorola	
	DM5440	† National	90
	DM7440	National	
	DM9009C	National	
	μPB7440	NEC America	
	5440	† Signetics	
	7440	Signetics	
	SN5440	† TI	
	SN7440	TI	
	TD3440	Toshiba	
	7440	TRW	
TTL-LS	9LS40C	Fairchild	100
	9LS40M	† Fairchild	
	54LS40	† Fairchild	
	74LS40	Fairchild	
	ITT74LS40	ITT	
	SN54LS40	† Motorola	
	SN74LS40	Motorola	
	DM54LS40	† National	
	DM74LS40	National	
	μPB74LS40	NEC America	
	9LS40C	Raytheon	110
	9LS40M	† Raytheon	
	54LS40	† Raytheon	
	74LS40	Raytheon	
	54LS40	Signetics	
	74LS40	Signetics	
	SN54LS40	† TI	
	SN74LS40	TI	
TTL-H	54H40	† Fairchild	
	74H40	Fairchild	
	ITT54H40	† ITT	120
	ITT74H40	ITT	
	MC3024	Motorola	
	MC3025	Motorola	
	MC3124	† Motorola	
	MC3125	† Motorola	
	DM54H40	† National	
	DM74H40	National	
	μPB74H40	NEC America	
	54H40	† Raytheon	
	74H40	Raytheon	130
	54R40	† Raytheon	
	74R40	Raytheon	
	54H40	† Signetics	
	74H40	Signetics	
	SN54H40	† TI	
	SN74H40	TI	

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Gates, AND/NAND (Cont'd)

Function	Device	Source	Line
Dual 4 Input NAND Buffer (Cont'd.)			
TTL-S	54S40	† Fairchild	
	74S40	Fairchild	
	HD74S40	Hitachi	140
	M5S040	Mitsubishi	
	DM74S40	National	
	54S40	† Signetics	
	74S40	Signetics	
	SN54S40	† TI	
	SN74S40	TI	
Dual 4 Input NAND Gate, Open Collector			
TTL	5422	† Fairchild	
	7422	Fairchild	
	HD7422	Hitachi	150
	5422	† Raytheon	
	7422	Raytheon	
	SN5422	† TI	
	SN7422	TI	
TTL-LS	9LS22C	Fairchild	
	9LS22M	† Fairchild	
	54LS22	† Fairchild	
	74LS22	Fairchild	
	ITT74LS22	ITT	
	SN54LS22	† Motorola	160
	SN74LS22	Motorola	
	DM54LS22	† National	
	DM74LS22	National	
	9LS22C	Raytheon	
	9LS22M	† Raytheon	
	54LS22	† Raytheon	
	74LS22	Raytheon	
	54LS22	† Signetics	
	74LS22	Signetics	
	SN54LS22	† TI	170
	SN74LS22	TI	
TTL-H	54H22	† Fairchild	
	74H22	Fairchild	
	MC3012	Motorola	
	MC3112	† Motorola	
	DM54H22	† National	
	DM74H22	National	
	54H22	† Raytheon	
	74H22	Raytheon	
	54R22	† Raytheon	180
	74R22	Raytheon	
	54H22	† Signetics	
	74H22	Signetics	
	SN54H22	† TI	
	SN74H22	TI	
Dual 4 Input NAND Gate, Open Collector			
TTL-S	54S22	† Fairchild	
	74S22	Fairchild	
	ZN54S22	† Ferranti	
	ZN74S22	Ferranti	190
	HD74S22	Hitachi	
	M5S022	Mitsubishi	
	DM74S22	National	
	54S22	† Signetics	
	74S22	Signetics	
	SN54S22	† TI	
	SN74S22	TI	
Dual 5 Input NAND Gate			
TTL	DM7092	† National	
	DM8092	National	200
Triple 3 Input NAND Gate			
TTL	5410	† Fairchild	
	7410	Fairchild	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Gates, AND/NAND (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)	9003C	Fairchild	
	9003M	† Fairchild	
	ZN5410	† Ferranti	
	ZN7410	Ferranti	
	HD2507	Hitachi	
	HD7410	Hitachi	
	ITT5410	† ITT	
	ITT7410	ITT	
	ITT9003-1	† ITT	10
	ITT9003-5	ITT	
	M5330	Mitsubishi	
	M53210	Mitsubishi	
	MC5410	† Motorola	
	MC7410	Motorola	
	DM5410	† National	
	DM7410	National	
	DM9003C	National	
	μPB7410	NEC America	
	5410	† Raytheon	20
	7410	Raytheon	
	5410	† Signetics	
	7410	Signetics	
	SN5410	† TI	
	SN7410	TI	
	TD3410	Toshiba	
	7410	TRW	
TTL-LS	9LS10C	Fairchild	
	9LS10M	† Fairchild	
	54LS10	† Fairchild	30
	74LS10	Fairchild	
	ITT74LS10	ITT	
	SN54LS10	† Motorola	
	SN74LS10	Motorola	
	DM54LS10	† National	
	DM74LS10	National	
	μPB74LS10	NEC America	
	9LS10C	Raytheon	
	9LS10M	† Raytheon	
	54LS10	† Raytheon	40
	74LS10	Raytheon	
	54LS10	† Signetics	
	74LS10	Signetics	
	SN54LS10	† TI	
	SN74LS10	TI	
TTL-H	54H10	† Fairchild	
	74H10	Fairchild	
	ITT54H10	† ITT	
	ITT74H10	ITT	
	MC3005	Motorola	50
	MC3105	† Motorola	
	DM54H10	† National	
	DM74H10	National	
	μPB74H10	NEC America	
	54H10	† Raytheon	
	74H10	Raytheon	
	54R10	† Raytheon	
	74R10	Raytheon	
	54H10	† Signetics	
	74H10	Signetics	60
	SN54H10	† TI	
	SN74H10	TI	
TTL-S	54S10	† Fairchild	
	74S10	Fairchild	
	HD74S10	Hitachi	
	M5S010	Mitsubishi	
	DM74S10	National	
	54S10	† Signetics	

(Continued)

Gates, AND/NAND (Cont'd)

Function	Device	Source	Line
TTL-S (Cont'd.)	74S10	Signetics	70
	SN54S10	† TI	
	SN74S10	TI	
Triple 3 Input NAND Gate, Open Collector			
TTL	5412	† Fairchild	
	7412	Fairchild	
	ZN5412	† Ferranti	
	ZN7412	Ferranti	
	HD7412	Hitachi	
	ITT5412	† ITT	
	ITT7412	ITT	80
	5412	† Raytheon	
	7412	Raytheon	
	5412	† Signetics	
	7412	Signetics	
	SN5412	† TI	
	SN7412	TI	
	7412	TRW	
TTL-LS	54LS12	† Fairchild	
	74LS12	Fairchild	
	DM54LS12	† National	90
	DM74LS12	National	
	9LS12C	Raytheon	
	9LS12M	† Raytheon	
	54LS12	† Raytheon	
	74LS12	Raytheon	
	54LS12	† Signetics	
	74LS12	Signetics	
	SN54LS12	† TI	
	SN74LS12	TI	
TTL-H	MC3007	Motorola	100
	MC3107	† Motorola	
Quad 2 Input NAND Gate			
TTL	5400	† Fairchild	
	7400	Fairchild	
	9002C	Fairchild	
	9002M	† Fairchild	
	ZN5400	† Ferranti	
	ZN7400	Ferranti	
	HD2503	Hitachi	
	HD7400	Hitachi	110
	ITT5400	† ITT	
	ITT7400	ITT	
	ITT9002-1	† ITT	
	ITT9002-5	ITT	
	M5340	Mitsubishi	
	M53200	Mitsubishi	
	MC5400	† Motorola	
	MC7400	Motorola	
	DM5400	† National	
	DM7400	National	120
	DM9002C	National	
	μPB7400	NEC America	
	5400	† Raytheon	
	7400	Raytheon	
	5400	† Signetics	
	7400	Signetics	
	SN5400	† TI	
	SN7400	TI	
	TD3400	Toshiba	
	7400	TRW	130
TTL-LS	9LS00C	Fairchild	
	9LS00M	† Fairchild	
	54LS00	† Fairchild	
	74LS00	Fairchild	
	ITT74LS00	ITT	

(Continued)

Gates, AND/NAND (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)	SN54LS00	† Motorola	
	SN74LS00	Motorola	
	DM54LS00	† National	
	DM74LS00	National	140
	μPB74LS00	NEC America	
	9LS00C	Raytheon	
	9LS00M	† Raytheon	
	54LS00	† Raytheon	
	74LS00	Raytheon	
	54LS00	† Signetics	
	74LS00	Signetics	
	SN54LS00	† TI	
	SN74LS00	TI	
TTL-H	54H00	† Fairchild	150
	74H00	Fairchild	
	ITT54H00	† ITT	
	ITT74H00	ITT	
	MC3000	Motorola	
	MC3100	† Motorola	
	DM54H00	† National	
	DM74H00	National	
	μPB74H00	NEC America	
	54H00	† Raytheon	
	74H00	Raytheon	160
	54R00	† Raytheon	
	74R00	Raytheon	
	54H00	† Signetics	
	74H00	Signetics	
	SN54H00	† TI	
	SN74H00	TI	
TTL-S	54S00	† Fairchild	
	74S00	† Fairchild	
	ZN54S00	† Ferranti	
	ZN74S00	Ferranti	170
	HD74S00	Hitachi	
	M5S000	Mitsubishi	
	DM74S00	National	
	54S00	† Signetics	
	74S00	Signetics	
	SN54S00	† TI	
	SN74S00	TI	
Quad 2 Input NAND Buffer			
TTL	5437	† Fairchild	
	7437	Fairchild	180
	ZN5437	† Ferranti	
	ZN7437	Ferranti	
	HD2552	Hitachi	
	ITT5437	† ITT	
	ITT7437	ITT	
	M53237	Mitsubishi	
	MC5437	† Motorola	
	MC7437	Motorola	
	DM5437	† National	
	DM7437	National	190
	DM7091	† National	
	DM8091	National	
	μPB7437	NEC America	
	5437	† Raytheon	
	7437	Raytheon	
	5437	† Signetics	
	7437	Signetics	
	SN5437	† TI	
	SN7437	TI	
	TD3437	Toshiba	200
	7437	TRW	
TTL-LS	9LS37C	Fairchild	
	9LS37M	† Fairchild	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

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DIGITAL–TTL (Cont'd)

Gates, AND/NAND (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)			
	54LS37	† Fairchild	
	74LS37	Fairchild	
	ITT74LS37	ITT	
	SN54LS37	† Motorola	
	SN74LS37	Motorola	
	DM54LS37	† National	
	DM74LS37	National	
	μPB74LS37	NEC America	
	9LS37C	Raytheon	10
	9LS37M	† Raytheon	
	54LS37	† Raytheon	
	74LS37	Raytheon	
	54LS37	† Signetics	
	74LS37	Signetics	
	SN54LS37	† TI	
	SN74LS37	TI	
TTL-S	74S37	Signetics	
	SN54S37	† TI	
	SN74S37	TI	20
Quad 2 Input NAND Gate, Open Collector			
TTL	5401	† Fairchild	
	7401	Fairchild	
	5403	† Fairchild	
	7403	Fairchild	
	9012C	Fairchild	
	9012M	† Fairchild	
	ZN5401	† Ferranti	
	ZN7401	Ferranti	
	HD2509	Hitachi	30
	HD2528	Hitachi	
	HD7403	Hitachi	
	ITT5401	† ITT	
	ITT7401	ITT	
	ITT5403	† ITT	
	ITT7403	ITT	
	M53201	Mitsubishi	
	M53203	Mitsubishi	
	MC5401	† Motorola	
	MC7401	Motorola	40
	MC5403	† Motorola	
	MC7403	Motorola	
	DM5401	† National	
	DM7401	National	
	DM5403	† National	
	DM7403	National	
	DM9012C	National	
	5401	† Raytheon	
	7401	Raytheon	
	5403	† Raytheon	50
	7403	Raytheon	
	5401	† Signetics	
	7401	Signetics	
	5403	† Signetics	
	7403	Signetics	
	SN5401	† TI	
	SN7401	TI	
	SN5403	† TI	
	SN7403	TI	
	TD3401	Toshiba	60
	TD3403	Toshiba	
	7401	TRW	
	7403	TRW	
TTL-LS	9LS03C	Fairchild	
	9LS03M	† Fairchild	
	54LS01	† Fairchild	
	74LS01	Fairchild	
	54LS03	† Fairchild	

(Continued)

Gates, AND/NAND (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)			
	74LS03	Fairchild	70
	ITT74LS01	ITT	
	ITT74LS03	ITT	
	SN54LS03	† Motorola	
	SN74LS03	Motorola	
	DM54LS01	† National	
	DM74LS01	National	
	DM54LS03	† National	
	DM74LS03	National	
	μPB74LS03	NEC America	
	9LS01C	Raytheon	80
	9LS01M	† Raytheon	
	54LS01	† Raytheon	
	74LS01	Raytheon	
	9LS03C	Raytheon	
	9LS03M	† Raytheon	
	54LS03	† Raytheon	
	74LS03	Raytheon	
	54LS01	† Signetics	
	74LS01	Signetics	
	54LS03	† Signetics	90
	74LS03	Signetics	
	SN54LS01	† TI	
	SN74LS01	TI	
	SN54LS03	† TI	
	SN74LS03	TI	
TTL-H	54H01	† Fairchild	
	74H01	Fairchild	
	ITT54H01	† ITT	
	ITT74H01	ITT	
	MC3004	Motorola	100
	MC3104	† Motorola	
	DM54H01	† National	
	DM74H01	National	
	μPB74H01	NEC America	
	54H01	† Raytheon	
	74H01	Raytheon	
	54H03	† Raytheon	
	74H03	Raytheon	
	54H01	† Signetics	
	74H01	Signetics	110
	SN54H01	† TI	
	SN74H01	TI	
TTL-S	54S03	† Fairchild	
	74S03	Fairchild	
	ZN54S03	† Ferranti	
	ZN74S03	Ferranti	
	HD74S03	Hitachi	
	M5S003	Mitsubishi	
	DM74S03	National	
	54S03	† Signetics	120
	74S03	Signetics	
	SN54S03	† TI	
	SN74S03	TI	
Quad 2 Input NAND Buffer, Open Collector			
TTL	5438	† Fairchild	
	7438	Fairchild	
	7439	Fairchild	
	ZN5438	† Ferranti	
	ZN7438	Ferranti	
	HD2544	Hitachi	130
	ITT5438	† ITT	
	ITT7438	ITT	
	M53238	Mitsubishi	
	MC5438	† Motorola	
	MC7438	Motorola	
	DM5438	† National	

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Gates, AND/NAND (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	DM7438	National	
	μPB7438	NEC America	
	5438	† Raytheon	140
	7438	Raytheon	
	5438	† Signetics	
	7438	Signetics	
	5439	† Signetics	
	7439	Signetics	
	SN5438	† TI	
	SN7438	TI	
	TD3438	Toshiba	
	7438	TRW	
TTL-LS	9LS38C	Fairchild	150
	9LS38M	† Fairchild	
	54LS38	† Fairchild	
	74LS38	Fairchild	
	ITT74LS38	ITT	
	SN54LS38	† Motorola	
	SN74LS38	Motorola	
	9LS38C	Raytheon	
	9LS38M	† Raytheon	
	54LS38	† Raytheon	
	74LS38	Raytheon	160
	DM54LS38	† National	
	DM74LS38	National	
	μPB74LS38	NEC America	
	74LS38	Signetics	
	54LS38	† Signetics	
	SN54LS38	† TI	
	SN74LS38	TI	
TTL-S	74S38	Signetics	
	SN54S38	† TI	
	SN74S38	TI	170
Quad 2 Input NAND Buffer, Open Collector, to 15v			
TTL-LS	9LS26C	Fairchild	
	9LS26M	† Fairchild	
	54LS26	† Fairchild	
	74LS26	Fairchild	
	DM54LS26	† National	
	DM74LS26	National	
	9LS26C	Raytheon	
	9LS26M	† Raytheon	
	54LS26	† Raytheon	180
	74LS26	Raytheon	
	54LS26	† Signetics	
	74LS26	Signetics	
	SN54LS26	† TI	
	SN74LS26	TI	
Quad 2 Input NAND Buffer, Three State			
TTL	DM7099	† National	
	DM8099	National	

Gates, AND-OR/AND-OR-Invert

Function	Device	Source	Line
Dual 2 4 Input AND/OR Gate			
TTL-S	9S42C	Fairchild	190
	9S42M	Fairchild	
2 2 2 3 Input AND OR Gate, Expandable			
TTL-H	54H52	† Fairchild	
	74H52	Fairchild	
	MC3031	Motorola	
	MC3131	† Motorola	
	DM54H52	† National	
	DM74H52	National	
	54H52	† Signetics	
	74H52	Signetics	200

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† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Gates, AND-OR/AND-OR-Invert (Cont'd)

Function	Device	Source	Line
TTL-H (Cont'd.)			
	SN54H52	† TI	
	SN74H52	TI	
2 2 2 3 Input AND OR Invert Gate, Expandable			
TTL	9008C	Fairchild	
	9008M	† Fairchild	
	ITT9008-1	† ITT	
	ITT9008-5	ITT	
	DM9008C	National	
4 Wide 2 Input AND OR Invert Gate			10
TTL	5454	† Fairchild	
	7454	Fairchild	
	ZN5454	† Ferranti	
	ZN7454	Ferranti	
	HD2514	Hitachi	
	HD7454	Hitachi	
	ITT5454	† ITT	
	ITT7454	ITT	
	MC5454	† Motorola	
	MC7454	Motorola	20
	DM5454	† National	
	DM7454	National	
	μPB7454	NEC America	
	5454	† Signetics	
	7454	Signetics	
	SN5454	† TI	
	SN7454	TI	
	7454	TRW	
4 Wide 2 2 3 3 Input AND OR Invert Gate			
TTL-LS	9LS54C	Fairchild	30
	9LS54M	† Fairchild	
	54LS54	† Fairchild	
	74LS54	Fairchild	
	ITT74LS54	ITT	
	SN54LS54	† Motorola	
	SN74LS54	Motorola	
	DM54LS54	† National	
	DM74LS54	National	
	μPB74LS54	NEC America	
	9LS54C	Raytheon	40
	9LS54M	† Raytheon	
	54LS54	† Raytheon	
	74LS54	Raytheon	
	54LS54	† Signetics	
	74LS54	Signetics	
	SN54LS54	† TI	
	SN74LS54	TI	
2 2 2 3 Input AND OR Invert Gate			
TTL-H	54H54	† Fairchild	
	74H54	Fairchild	50
	ITT54H54	† ITT	
	ITT74H54	ITT	
	DM54H54	† National	
	DM74H54	National	
	54H54	† Signetics	
	74H54	Signetics	
	SN54H54	† TI	
	SN74H54	TI	
4 Wide 2 Input AND OR Invert Gate, Expandable			
TTL	5453	† Fairchild	60
	7453	Fairchild	
	ZN5453	† Ferranti	
	ZN7453	Ferranti	
	HD2512	Hitachi	
	HD2578	Hitachi	
	HD7453	Hitachi	
	ITT5453	† ITT	

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Gates, AND-OR/AND-OR-Invert (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	ITT7453	ITT	
	M53253	Mitsubishi	70
	MC5453	† Motorola	
	MC7453	Motorola	
	DM5453	† National	
	DM7453	National	
	μPB7453	NEC America	
	5453	† Signetics	
	7453	Signetics	
	SN5453	† TI	
	SN7453	TI	
	7453	TRW	80
2 2 2 3 Input AND OR Invert Gate, Expandable			
TTL-H	54H53	† Fairchild	
	74H53	Fairchild	
	ITT54H53	† ITT	
	ITT74H53	ITT	
	MC3032	Motorola	
	MC3132	† Motorola	
	DM54H53	† National	
	DM74H53	National	
	54H53	† Signetics	90
	74H53	Signetics	
	SN54H53	† TI	
	SN74H53	TI	
4 2 3 2 Input AND OR Invert Gate			
TTL-H	54R64	† Raytheon	
	74R64	Raytheon	
TTL-S	54S64	† Fairchild	
	74S64	† Fairchild	
	HD74S64	Hitachi	
	DM74S64	National	100
	54S64	† Signetics	
	74S64	† Signetics	
	SN54S64	TI	
	SN74S64	TI	
4 2 3 2 Input AND OR Invert Gate, Open Collector			
TTL-H	54R65	† Raytheon	
	74R65	Raytheon	
TTL-S	54S65	† Fairchild	
	74S65	† Fairchild	
	HD74S65	Hitachi	110
	DM74S65	National	
	54S65	† Signetics	
	74S65	Signetics	
	SN54S65	† TI	
	SN74S65	TI	
Dual 2 Wide 2 Input AND OR Invert Gate			
TTL	5451	† Fairchild	
	7451	Fairchild	
	ZN7451	Ferranti	
	ZN5451	† Ferranti	120
	HD2505	Hitachi	
	HD7451	Hitachi	
	ITT5451	† ITT	
	ITT7451	ITT	
	MC5451	† Motorola	
	MC7451	Motorola	
	DM5451	† National	
	DM7451	National	
	μPB7451	NEC America	
	5451	† Signetics	130
	7451	Signetics	
	SN5451	† TI	
	SN7451	TI	
	TD3451	Toshiba	

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Gates, AND-OR/AND-OR-Invert (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	7451	TRW	
TTL-H	54H51	† Fairchild	
	74H51	Fairchild	
	ITT54H51	† ITT	
	ITT74H51	ITT	140
	MC3023	Motorola	
	MC3123	† Motorola	
	DM54H51	† National	
	DM74H51	National	
	μPB74H51	NEC America	
	54H51	† Signetics	
	74H51	Signetics	
	SN54H51	† TI	
	SN74H51	TI	
TTL-S	54S51	† Fairchild	150
	74S51	Fairchild	
	DM74S51	National	
	54S51	† Signetics	
	74S51	Signetics	
	SN54S51	† TI	
	SN74S51	TI	
Dual 2 Wide 2/3 Input AND OR Invert Gate			
TTL-LS	9LS51C	Fairchild	
	9LS51M	† Fairchild	
	54LS51	† Fairchild	160
	74LS51	Fairchild	
	ITT74LS51	ITT	
	SN54LS51	† Motorola	
	SN74LS51	Motorola	
	DM54LS51	† National	
	DM74LS51	National	
	μPB74LS51	NEC America	
	9LS51C	Raytheon	
	9LS51M	† Raytheon	
	54LS51	† Raytheon	170
	74LS51	Raytheon	
	54LS51	† Signetics	
	74LS51	Signetics	
	SN54LS51	† TI	
	SN74LS51	TI	
2 Wide, 4 Input AND OR Invert Gate			
TTL-LS	9LS55C	Fairchild	
	9LS55M	† Fairchild	
	54LS55	† Fairchild	
	74LS55	Fairchild	180
	SN54LS55	† Motorola	
	SN74LS55	Motorola	
	DM54LS55	† National	
	DM74LS55	National	
	μPB74LS55	NEC America	
	9LS55C	Raytheon	
	9LS55M	† Raytheon	
	54LS55	† Raytheon	
	74LS55	Raytheon	
	54LS55	† Signetics	190
	74LS55	Signetics	
	SN54LS55	† TI	
	SN74LS55	TI	
2 Wide, 4 Input AND OR Invert Gate, Expandable			
TTL-H	54H55	† Fairchild	
	74H55	Fairchild	
	DM54H55	† National	
	DM74H55	National	
	54H55	† Signetics	
	74H55	Signetics	200
	SN54H55	† TI	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Gates, AND-OR/AND-OR-Invert (Cont'd)

Function	Device	Source	Line
TTL-H (Cont'd.)			
	SN74H55	TI	
Dual 2 Wide 2 input AND OR Invert Gate (one gate is expandable)			
TTL	5450	† Fairchild	
	7450	Fairchild	
	9005C	Fairchild	
	9005M	† Fairchild	
	ZN5450	† Ferranti	
	ZN7450	Ferranti	10
	HD2506	Hitachi	
	HD7450	Hitachi	
	ITT5450	† ITT	
	ITT7450	ITT	
	ITT9005-1	† ITT	
	ITT9005-5	ITT	
	M5352	Mitsubishi	
	M53250	Mitsubishi	
	MC5450	† Motorola	
	MC7450	Motorola	20
	DM5450	† National	
	DM7450	National	
	DM9005C	National	
	μPB7450	NEC America	
	5450	† Signetics	
	7450	Signetics	
	SN5450	† TI	
	SN7450	TI	
	TD3450	Toshiba	
	7450	TRW	30
TTL-H	54H50	† Fairchild	
	74H50	Fairchild	
	ITT54H50	† ITT	
	ITT74H50	ITT	
	MC3020	Motorola	
	MC3120	† Motorola	
	DM54H50	† National	
	DM74H50	National	
	54H50	† Signetics	
	74H50	Signetics	40
	SN54H50	† TI	
	SN74H50	TI	
Dual 4 input Expander (for 54/7423, 54/7450, 54/7453)			
TTL	5460	† Fairchild	
	7460	Fairchild	
	ZN5460	† Ferranti	
	ZN7460	Ferranti	
	HD2502	Hitachi	
	HD7460	Hitachi	50
	M5304	Mitsubishi	
	M53260	Mitsubishi	
	MC5460	† Motorola	
	MC7460	Motorola	
	DM5460	† National	
	DM7460	National	
	μPB7460	NEC America	
	5460	† Signetics	
	7460	Signetics	
	SN5460	† TI	60
	SN7460	TI	
	TD3460	Toshiba	
	7460	TRW	
Dual 4 Input Extender (for 9005, 9006)			
TTL	9006C	Fairchild	
	9006M	† Fairchild	
	DM9006C	National	

Gates, Exclusive OR/NOR

Function	Device	Source	Line
Quad 2 Input Exclusive OR Gate			
TTL	5486	† Fairchild	
	7486	Fairchild	70
	ZN5486	† Ferranti	
	ZN7486	Ferranti	
	HD2526	Hitachi	
	HD7486	Hitachi	
	DM74LS386	National	
	ITT5486	† ITT	
	ITT7486	ITT	
	M53286	Mitsubishi	
	MC5486	† Motorola	
	MC7486	Motorola	80
	MC7241	Motorola	
	MC8241	† Motorola	
	DM5486	National	
	DM7486	National	
	μPB7486	NEC America	
	5486	† Raytheon	
	7486	Raytheon	
	RC8241	Raytheon	
	RM8241	† Raytheon	
	5486	† Signetics	90
	7486	Signetics	
	N8241	Signetics	
	S8241	† Signetics	
	SN5486	† TI	
	SN7486	TI	
	7486	TRW	
TTL-LS	9LS86C	Fairchild	
	9LS86M	† Fairchild	
	54LS86	† Fairchild	
	74LS86	Fairchild	100
	ITT74LS86	ITT	
	ITT74LS386	ITT	
	SN54LS86	† Motorola	
	SN74LS86	Motorola	
	DM54LS386	† National	
	μPB74LS86	NEC America	
	9LS86C	Raytheon	
	9LS86M	† Raytheon	
	54LS86	† Raytheon	
	74LS86	Raytheon	110
	9LS386C	Raytheon	
	9LS386M	† Raytheon	
	54LS386	† Raytheon	
	74LS386	Raytheon	
	54LS86	† Signetics	
	74LS86	Signetics	
	54LS386	† Signetics	
	74LS386	Signetics	
	SN54LS86	† TI	
	SN74LS86	TI	120
	SN54LS386	† TI	
	SN74LS386	TI	
TTL-H	MC3021	Motorola	
	MC3121	† Motorola	
TTL-S	54S86	† Fairchild	
	74S86	Fairchild	
	HD74S86	Hitachi	
	DM74S86	National	
	N82S41	Signetics	
	54S86	† Signetics	130
	74S86	Signetics	
	SN54S86	† TI	
	SN74S86	TI	
Quad 2 Input Exclusive OR Gate (two of the outputs are complemented)			
TTL	9014C	Fairchild	

(Continued)

Gates, Exclusive OR/NOR (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	9014M	† Fairchild	
Quad 2 Input Exclusive OR Gate, Open Collector			140
TTL	HD74136	Hitachi	
	MC54136	† Motorola	
	MC74136	Motorola	
	54136	† Raytheon	
	74136	Raytheon	
	SN54136	† TI	
	SN74136	TI	
	74136	TRW	
TTL-LS	9LS136C	Fairchild	
	9LS136M	† Fairchild	150
	54LS136	Fairchild	
	74LS136	Fairchild	
	ITT74LS136	ITT	
	SN54LS136	† Motorola	
	SN74LS136	Motorola	
	DM54LS136	† National	
	DM74LS136	National	
	9LS136C	Raytheon	
	9LS136M	† Raytheon	
	54LS136	† Raytheon	160
	74LS136	Raytheon	
	54LS136	† Signetics	
	74LS136	Signetics	
	SN54LS136	† TI	
	SN74LS136	TI	
TTL-S	DM74S136	National	
Quad 2 Input Exclusive NOR Gate			
TTL-H	MC3022	Motorola	
	MC3122	† Motorola	
Quad 2 Input Exclusive NOR Gate, Open Collector			170
TTL	9386C	Fairchild	
	9386M	† Fairchild	
	MC7242	Motorola	
	MC8242	† Motorola	
	RC8242	Raytheon	
	RM8242	† Raytheon	
	N8242	Signetics	
	S8242	† Signetics	
TTL-LS	9LS266C	Fairchild	
	9LS266M	† Fairchild	180
	54LS266	† Fairchild	
	74LS266	Fairchild	
	ITT74LS266	ITT	
	SN54LS266	† Motorola	
	SN74LS266	Motorola	
	DM54LS266	† National	
	DM74LS266	National	
	9LS266C	Raytheon	
	9LS266M	† Raytheon	
	54LS266	† Raytheon	190
	74LS266	Raytheon	
	54LS266	† Signetics	
	74LS266	Signetics	
	SN54LS266	† TI	
	SN74LS266	TI	
TTL-S	N82S42	Signetics	
Quad 2 Input OR/NOR Gate			
TTL-S	54S135	† Fairchild	
	74S135	Fairchild	
	HD74S135	Hitachi	200
	DM74S135	National	
	74S135	Signetics	
	SN54S135	† TI	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Gates, Exclusive OR/NOR (Cont'd)

Function	Device	Source	Line
TTL-S (Cont'd.)			
	SN74S135	TI	

Gates, OR/NOR

Function	Device	Source	Line
Quad 2 Input OR Gate			
TTL	5432	† Fairchild	
	7432	Fairchild	
	ZN5432	† Ferranti	
	ZN7432	Ferranti	
	HD7432	Hitachi	
	ITT5432	† ITT	
	ITT7432	ITT	10
	DM5432	† National	
	DM7432	National	
	5432	† Signetics	
	7432	Signetics	
	SN5432	† TI	
	SN7432	TI	
TTL-LS	9LS32C	Fairchild	
	9LS32M	† Fairchild	
	54LS32	† Fairchild	
	74LS32	Fairchild	20
	ITT74LS32	ITT	
	SN54LS32	† Motorola	
	SN74LS32	Motorola	
	DM54LS32	† National	
	DM74LS32	National	
	μPB74LS32	NEC America	
	9LS32C	Raytheon	
	9LS32M	† Raytheon	
	54LS32	† Raytheon	
	74LS32	Raytheon	30
	54LS32	† Signetics	
	74LS32	Signetics	
	SN54LS32	† TI	
	SN74LS32	TI	
TTL-S	54S32	† Fairchild	
	74S32	Fairchild	
	54S32	† Signetics	
	74S32	Signetics	
	SN54S32	† TI	
	SN74S32	TI	40
2 2 2 4 Input NOR Gate			
TTL	9015C	Fairchild	
	9015M	† Fairchild	
Dual 4 Input NOR Gate, with Strobe			
TTL	5425	† Fairchild	
	7425	Fairchild	
	ZN5425	† Ferranti	
	ZN7425	Ferranti	
	ITT5425	† ITT	
	ITT7425	ITT	50
	M53225	Mitsubishi	
	MC5425	† Motorola	
	MC7425	Motorola	
	DM5425	† National	
	DM7425	National	
	7425	Signetics	
	SN5425	† TI	
	SN7425	TI	
Dual 4 Input NOR Gate, with Strobe, Expandable (see 54/7460 Expander)			
TTL	5423	† Fairchild	
	7423	Fairchild	
	MC5423	† Motorola	
	MC7423	Motorola	60

(Continued)

Gates, OR/NOR (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	DM5423	† National	
	DM7423	National	
	7423	Signetics	
	SN5423	† TI	70
	SN7423	TI	
Dual 5 Input NOR Gate			
TTL-LS	9LS260C	Fairchild	
	9LS260M	† Fairchild	
	54LS260	† Fairchild	
	74LS260	Fairchild	
	54LS260A	† Signetics	
	74LS260A	Signetics	
TTL-S	DM74S260	National	
	54S260	† Signetics	80
	74S260	Signetics	
	SN54S260	† TI	
	SN74S260	TI	
Triple 3 Input NOR Gate			
TTL	5427	† Fairchild	
	7427	Fairchild	
	ZN5427	† Ferranti	
	ZN7427	Ferranti	
	HD7427	Hitachi	
	M53227	Mitsubishi	90
	MC5427	† Motorola	
	MC7427	Motorola	
	DM5427	† National	
	DM7427	National	
	5427	† Signetics	
	7427	Signetics	
	SN5427	† TI	
	SN7427	TI	
TTL-LS	9LS27C	Fairchild	
	9LS27M	† Fairchild	100
	54LS27	† Fairchild	
	74LS27	Fairchild	
	ITT74LS27	ITT	
	SN54LS27	† Motorola	
	SN74LS27	Motorola	
	DM54LS27	† National	
	DM74LS27	National	
	μPB74LS27	NEC America	
	9LS27C	Raytheon	
	9LS27M	† Raytheon	110
	54LS27	† Raytheon	
	74LS27	Raytheon	
	54LS27	† Signetics	
	74LS27	Signetics	
	SN54LS27	† TI	
	SN74LS27	TI	
Quad 2 Input NOR Gate (54/7428 devices are also buffers)			
TTL	5402	† Fairchild	
	7402	Fairchild	120
	ZN5428	† Ferranti	
	ZN7428	Ferranti	
	HD2511	Hitachi	
	HD7402	Hitachi	
	ITT5402	† ITT	
	ITT7402	ITT	
	M53202	Mitsubishi	
	MC5402	† Motorola	
	MC7402	Motorola	
	DM5402	† National	130
	DM7402	National	
	μPB7402	NEC America	

(Continued)

Gates, OR/NOR (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	5402	† Signetics	
	7402	Signetics	
	5428	† Signetics	
	7428	Signetics	
	SN5402	† TI	
	SN7402	TI	140
	SN5428	† TI	
	SN7428	TI	
	7402	TRW	
TTL-LS	9LS02C	Fairchild	
	9LS02M	† Fairchild	
	54LS02	† Fairchild	
	74LS02	Fairchild	
	9LS28C	Fairchild	
	74LS28	Fairchild	
	ITT74LS02	ITT	150
	ITT74LS28	ITT	
	SN54LS02	† Motorola	
	SN74LS02	Motorola	
	DM54LS02	† National	
	DM74LS02	National	
	μPB74LS02	NEC America	
	9LS02C	Raytheon	
	9LS02M	† Raytheon	
	54LS02	† Raytheon	
	74LS02	Raytheon	160
	9LS28C	Raytheon	
	9LS28M	† Raytheon	
	54LS28	† Raytheon	
	74LS28	Raytheon	
	54LS02	† Signetics	
	74LS02	Signetics	
	54LS28	† Signetics	
	74LS28	Signetics	
	SN54LS02	† TI	
	SN74LS02	TI	170
	SN54LS28	† TI	
	SN74LS28	TI	
TTL-S	54S02	† Fairchild	
	74S02	Fairchild	
	DM74S02	National	
	54S02	† Signetics	
	74S02	Signetics	
	SN54S02	† TI	
	SN74S02	TI	
Quad 2 Input NOR Buffer, Open Collector			180
TTL	5433	† Signetics	
	7433	Signetics	
	SN5433	† TI	
	SN7433	TI	
TTL-LS	9LS33C	Fairchild	
	54LS33	† Fairchild	
	74LS33	Fairchild	
	9LS33C	Raytheon	
	9LS33M	† Raytheon	
	54LS33	† Raytheon	190
	74LS33	Raytheon	
	54LS33	† Signetics	
	74LS33	Signetics	
	SN54LS33	† TI	
	SN74LS33	TI	
Quad 2 Input OR Gate			
TTL-H	MC3003	Motorola	
	MC3103	† Motorola	
Quad 2 Input NOR Gate			
TTL-H	MC3002	Motorola	200

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

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DIGITAL–TTL (Cont'd)

Gates, OR/NOR (Cont'd)

Function	Device	Source
TTL-H (Cont'd.)		
	MC3102	† Motorola
	54R02	† Raytheon
	74R02	Raytheon

Gates Miscellaneous

Function	Device	Source
Quad Inverter and Dual 2 Input NAND Gate		
TTL	DM7090	† National
	DM8090	National
Dual Majority Logic Gate		
TTL	MC4062	Motorola

Latches

Function	Device	Source
8 bit Addressable Latch, with Clear		
TTL	9334C	AMD
	9334M	† AMD
	SN54259	† AMD
	SN74259	AMD
	9334C	Fairchild
	9334M	† Fairchild
	DM8334	National
	DM9334	† National
	N9334	Signetics
	SN54259	† TI
	SN74259	TI
TTL-LS	9LS259C	Fairchild
	9LS259M	† Fairchild
	54LS259	† Fairchild
	74LS259	Fairchild
	ITT74LS259	ITT
	SN54LS259	† Motorola
	SN74LS259	Motorola
	SN54LS259	† TI
	SN74LS259	TI
Dual 4 bit Addressable Latch		
TTL-LS	54LS256	† Fairchild
	74LS256	Fairchild
8 bit Latch, Three State (input and output through the same pins)		
TTL	DM7553	† National
	DM8553	National
8 bit Latch, Transparent, D Type, Three State		
TTL-LS	AM25LS373C	AMD
	AM25LS373M	† AMD
	SN54LS373	† AMD
	SN74LS373	AMD
	ITT74LS373	ITT
	54LS373	† MMI
	74LS373	MMI
	57LS380	† MMI
	67LS380	MMI
	25LS373C	Raytheon
	25LS373M	† Raytheon
	54LS373	**† Raytheon (288)**
	74LS373	**Raytheon (288)**
	SN54LS363	† Ti
	SN74LS363	TI
	SN54LS373	† TI
	SN74LS373	TI
TTL-S	**54S373**	**† MMI (460)**
	74S373	**MMI (460)**
	57S373	**† MMI (460)**
	67S373	**MMI (460)**
	57S380	**† MMI (460)**
	67S380	**MMI (460)**

(Continued)

Latches (Cont'd)

Function	Device	Source
TTL-S (Cont'd.)		
	57S382	**† MMI (460)**
	67S382	**MMI (460)**
	SN54S373	† TI
	SN74S373	TI
	SN54S412	† TI
	SN74S412	TI
6 bit Latch (Independent 2 and 4 bit)		
TTL-S	3404	Intel
Dual 4 bit Latch		
TTL	MC54100	† Motorola
	MC74100	Motorola
	54100	† Signetics
	74100	Signetics
	SN54100	† TI
	SN74100	TI
Dual 4 bit Latch with Clear		
TTL	9308C	AMD
	9308M	† AMD
	9308C	Fairchild
	9308M	† Fairchild
	54116	† Fairchild
	74116	Fairchild
	MC8308	Motorola
	MC9308	† Motorola
	μPB9308	NEC America
	RM9308	† Raytheon
	RC9308	Raytheon
	54116	† Signetics
	74116	Signetics
	N9308	Signetics
	SN29308	TI
	SN39308	† TI
	SN54116	† TI
	SN74116	TI
Quad Multifunction Latch		
TTL	9314C	AMD
	9314M	† AMD
	9314C	Fairchild
	9314M	† Fairchild
	MC8314	Motorola
	MC9314	† Motorola
	N9314	Signetics
Quad Bistable Latch, Single Output		
TTL	5477	† Fairchild
	7477	Fairchild
	MC5477	† Motorola
	MC7477	Motorola
	5477	† Signetics
	7477	Signetics
	SN5477	† TI
TTL-LS	54LS77	† Fairchild
	74LS77	Fairchild
	DM74LS77	National
	9LS77C	Raytheon
	9LS77M	† Raytheon
	54LS77	† Raytheon
	74LS77	Raytheon
	SN54LS77	† TI
Quad Bistable Latch, Complementary Outputs		
TTL	5474	† Fairchild
	7474	Fairchild
	5475	† Fairchild
	7475	Fairchild
	ZN5474	† Ferranti
	ZN7475	Ferranti

(Continued)

Latches (Cont'd)

Function	Device	Source
TTL (Cont'd.)		
	HD2517	Hitachi
	HD7475	Hitachi
	ITT5475	† ITT
	ITT7475	ITT
	M53275	Mitsubishi
	MC5475	† Motorola
	MC7475	Motorola
	DM5475	† National
	DM7475	National
	5474	† Signetics
	7474	Signetics
	5475	† Signetics
	7475	Signetics
	SN5474	† TI
	SN7475	TI
	TD3475	Toshiba
	7475	TRW
TTL-LS	54LS75	† Fairchild
	74LS75	Fairchild
	ITT74LS75	ITT
	ITT74LS375	ITT
	DM54LS75	† National
	DM74LS75	National
	μPB74LS375	NEC Amenca
	9LS75C	Raytheon
	9LS75M	† Raytheon
	54LS75	† Raytheon
	74LS75	Raytheon
	54LS75	† Signetics
	74LS75	Signetics
	54LS375	† Signetics
	74LS375	Signetics
	SN54LS75	† TI
	SN74LS75	TI
	SN54LS375	† TI
	SN74LS375	TI
Quad Set Reset Latch		
TTL	54279	† Fairchild
	74279	Fairchild
	54279	† Signetics
	74279	Signetics
	SN54279	† TI
	SN74279	TI
TTL-LS	9LS279C	Fairchild
	9LS279M	† Fairchild
	54LS279	† Fairchild
	74LS279	Fairchild
	ITT74LS279	ITT
	SN54LS279	† Motorola
	SN74LS279	Motorola
	DM54LS279	† National
	DM74LS279	National
	μPB74LS279	NEC Amenca
	9LS279C	Raytheon
	9LS279M	† Raytheon
	54LS279	† Raytheon
	74LS279	Raytheon
	54LS279	† Signetics
	74LS279	Signetics
	SN54LS279	† TI
	SN74LS279	TI
Hex Set Reset Latch (Common Reset)		
TTL	ZN54118	† Ferranti
	ZN74118	Ferranti
	ZN54119	† Ferranti
	ZN74119	Ferranti

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Memories

For additional information on these and larger TTL compatible memories, see the Master Selection Guide Memory section

8 bit Multiport Register (RAM with simultaneous Read/Write)

Function	Device	Source
TTL	9338C	AMD
	9338M	† AMD
	9338C	Fairchild
	9338M	† Fairchild

Octal Storage Register (two stage, 4 bit wide shift register)

Function	Device	Source
TTL-LS	SN54LS396	† TI
	SN74LS396	TI

Dual Rank 8 bit Shift Register (8 Bit I/O Buffer, "D" Register, and Serial "B" Register)

Function	Device	Source	Line
TTL-LS	DM76LS52	† National	
	DM86LS52	National	
	DM76LS62	† National	10
	DM86LS62	National	

16 bit Active Element Memory

Function	Device	Source	Line
TTL	93407C	Fairchild	
	93407M	† Fairchild	
	HM2501	Hitachi	
	MC4004	Motorola	
	MC4005	Motorola	
	MC4304	† Motorola	
	MC4305	† Motorola	
	SN5481A	† TI	20
	SN7481A	TI	
	7481	TRW	

16 bit Active Element Memory, Gated Write

Function	Device	Source
TTL	M53284	Mitsubishi
	μPB7484	NEC America
	SN5484A	† TI
	SN7484A	TI

16 bit (4x4) Register File, Simultaneous Read/Write, Open Collector

Function	Device	Source	Line
TTL	54170	† Fairchild	30
	74170	Fairchild	
	ZN54170	† Ferranti	
	ZN74170	Ferranti	
	HD2540	Hitachi	
	M53370	Mitsubishi	
	DM74170	National	
	μPB74170	NEC America	
	54170	† Raytheon	
	74170	Raytheon	
	54170	† Signetics	40
	74170	Signetics	
	SN54170	† TI	
	SN74170	TI	
TTL-LS	AM25LS170C	AMD	
	AM25LS170M	† AMD	
	SN54LS170	† AMD	
	SN74LS170	AMD	
	9LS170C	Fairchild	
	9LS170M	† Fairchild	
	54LS170	† Fairchild	50
	74LS170	Fairchild	
	ITT74LS170	ITT	
	SN54LS170	† Motorola	
	SN74LS170	Motorola	
	DM54LS170	† National	
	DM74LS170	National	
	9LS170C	Raytheon	
	9LS170M	† Raytheon	
	54LS170	† Raytheon	
	74LS170	Raytheon	60

(Continued)

Memories (Cont'd)

TTL-LS (Cont'd.)

Function	Device	Source
	25LS170C	Raytheon
	25LS170M	† Raytheon
	54LS170	† Signetics
	74LS170	Signetics
	SN54LS170	† TI
	SN74LS170	TI

16 bit (4x4) Register File, Simultaneous Read/Write, Three State

Function	Device	Source	Line
TTL-LS	AM25LS670C	AMD	70
	AM25LS670M	† AMD	
	SN54LS670	† AMD	
	SN74LS670	AMD	
	9LS670C	Fairchild	
	9LS670M	† Fairchild	
	54LS670	† Fairchild	
	74LS670	Fairchild	
	ITT74LS670	ITT	
	SN54LS670	† Motorola	80
	SN74LS670	Motorola	
	DM54LS670	† National	
	DM74LS670	National	
	9LS670C	Raytheon	
	9LS670M	† Raytheon	
	25LS670C	Raytheon	
	25LS670M	† Raytheon	
	54LS670	† Raytheon	
	74LS670	Raytheon	
	54LS670	† Signetics	90
	74LS670	Signetics	
	SN54LS670	† TI	
	SN74LS670	TI	

16 bit (8x2) Multiport Register File, Simultaneous Read/Write, Three State

Function	Device	Source
TTL	SN74172	TI

Function	Device	Source
TTL-S	74S172	Signetics

16 bit (4x4) Content Addressable Memory

Function	Device	Source
TTL	3104	Intel

32 bit (8x4) Multiport RAM

Function	Device	Source	Line
TTL-S	N82S12	Signetics	100
	N82S112	Signetics	

64 Bit (16x4) Register File with Latch, Three State

Function	Device	Source
TTL-S	**DM85S68**	**National (1295)**

64 Bit (32x2) Simultaneous Read/Write RAM

Function	Device	Source
TTL-S	DM86S21	National
	N82S21	Signetics

64 Bit (16x4) Simultaneous Read/Write RAM with output register

Function	Device	Source	Line
TTL	9410C	Fairchild	110
	9410M	† Fairchild	

64 Bit (16x4) RAM with two output ports

Function	Device	Source
TTL	AM29704C	AMD
	AM29704M	† AMD
	AM29705C	AMD
	AM29705M	† AMD

80 bit (16x5) First In/First Out Memory, Asynchronous, Three State

Function	Device	Source
TTL-S	SN74S225	TI

Multiplexers

Quad 2 Input Multiplexer, Non Inverting

Function	Device	Source	Line
TTL	9322C	AMD	120
	9322M	† AMD	
	SN54157	† AMD	

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Multiplexers (Cont'd)

TTL (Cont'd.)

Function	Device	Source	Line
	SN74157	AMD	
	9322C	Fairchild	
	9322M	† Fairchild	
	54157	† Fairchild	
	74157	Fairchild	
	ZN54157	† Ferranti	130
	ZN74157	Ferranti	
	HD74157	Hitachi	
	ITT9322-1	ITT	
	ITT9322-5	ITT	
	ITT54157	† ITT	
	ITT74157	ITT	
	M53357	Mitsubishi	
	MC8322	Motorola	
	MC9322	† Motorola	
	MC54157	† Motorola	140
	MC74157	Motorola	
	DM8322	National	
	DM9322	† National	
	DM54157	† National	
	DM74157	National	
	μPB74157	NEC America	
	RC8233	Raytheon	
	RM8233	† Raytheon	
	RC9322	Raytheon	
	RM9322	† Raytheon	150
	54157	† Raytheon	
	74157	Raytheon	
	N8233	Signetics	
	S8233	† Signetics	
	54157	† Signetics	
	74157	Signetics	
	N9322	Signetics	
	SN54157	† TI	
	SN74157	TI	
TTL-LS	AM25LS157C	AMD	160
	AM25LS157M	AMD	
	SN54LS157	† AMD	
	SN74LS157	AMD	
	9LS157C	Fairchild	
	9LS157M	† Fairchild	
	54LS157	† Fairchild	
	74LS157	Fairchild	
	ITT74LS157	ITT	
	SN54LS157	† Motorola	
	SN74LS157	Motorola	170
	DM54LS157	† National	
	DM74LS157	National	
	μPB74LS157	NEC America	
	9LS157C	Raytheon	
	9LS157M	† Raytheon	
	25LS157C	Raytheon	
	25LS157M	† Raytheon	
	54LS157	† Raytheon	
	74LS157	Raytheon	
	54LS157	Signetics	180
	74LS157	Signetics	
	SN54LS157	† TI	
	SN74LS157	TI	
TTL-S	SN54S157	† AMD	
	SN74S157	AMD	
	93S22C	AMD	
	93S22M	† AMD	
	54S157	† Fairchild	
	74S157	Fairchild	
	M5S157	Mitsubishi	190
	DM74S157	National	
	54S157	† Signetics	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

IC MASTER

DIGITAL–TTL (Cont'd)

Multiplexers (Cont'd)

Function	Device	Source	Line
TTL-S (Cont'd.)			
	74S157	Signetics	
	N82S33	Signetics	
	SN54S157	† TI	
	SN74S157	TI	
Quad 2 Input Multiplexer, (Three State 54/74157)			
TTL	DM7123	National	
	DM8123	† National	
Quad 2 Input Multiplexer with Storage			
TTL	54298	† Fairchild	10
	74298	Fairchild	
	MC54298	† Motorola	
	MC74298	Motorola	
	54298	† Signetics	
	74298	Signetics	
	SN54298	† TI	
	SN74298	TI	
Quad 2 Input Digital Multiplexer (Suitable for Driving Adders, Registers)			
TTL	MC7266	Motorola	20
	MC8266	† Motorola	
	RC8266	Raytheon	
	RM8266	† Raytheon	
	N8266	Signetics	
	S8266	† Signetics	
TTL-S	N82S33	Signetics	
	N82S66	Signetics	
Quad 2 Input Multiplexer, Open Collector (for adder, register input)			
TTL	MC7267	Motorola	30
	MC8267	† Motorola	
	RC8267	Raytheon	
	RM8267	† Raytheon	
	N8267	Signetics	
	S8267	† Signetics	
TTL-S	N82S34	Signetics	
	N82S67	Signetics	
Quad 2 Input Multiplexer, Inverting			
TTL	M53358	Mitsubishi	
	54158	† Raytheon	40
	74158	Raytheon	
	54158	† Signetics	
	74158	Signetics	
TTL-LS	AM25LS158C	AMD	
	AM25LS158M	† AMD	
	SN54LS158	† AMD	
	SN74LS158	AMD	
	9LS158C	Fairchild	
	9LS158M	† Fairchild	
	54LS158	† Fairchild	50
	74LS158	Fairchild	
	ITT74LS158	ITT	
	SN54LS158	† Motorola	
	SN74LS158	Motorola	
	DM54LS158	† National	
	DM74LS158	National	
	9LS158C	Raytheon	
	25LS158C	Raytheon	
	25LS158M	† Raytheon	
	9LS158M	† Raytheon	60
	54LS158	† Raytheon	
	74LS158	Raytheon	
	54LS158	† Signetics	
	74LS158	Signetics	
	SN54LS158	† TI	
	SN74LS158	TI	

(Continued)

Multiplexers (Cont'd)

Function	Device	Source	Line
Quad 2 Input Multiplexer, Inverting (Cont'd.)			
TTL-S	SN54S158	† AMD	
	SN74S158	AMD	
	54S158	† Fairchild	70
	74S158	Fairchild	
	M5S158	Mitsubishi	
	DM74S158	National	
	54S158	† Signetics	
	74S158	Signetics	
	N82S66	Signetics	
	SN54S158	† TI	
	SN74S158	TI	
Quad 2 Input Multiplexer, Inverting Three State			
TTL-LS	AM25LS258C	AMD	80
	AM25LS258M	† AMD	
	SN54LS258	† AMD	
	SN74LS258	AMD	
	9LS258C	Fairchild	
	9LS258M	† Fairchild	
	54LS258	† Fairchild	
	74LS258	Fairchild	
	ITT74LS258	ITT	
	SN54LS258	† Motorola	
	SN74LS258	Motorola	90
	DM54LS258	† National	
	DM74LS258	National	
	μPB74LS258	NEC America	
	9LS258C	Raytheon	
	9LS258M	† Raytheon	
	25LS258C	Raytheon	
	25LS258M	† Raytheon	
	54LS258	† Raytheon	
	74LS258	Raytheon	
	74LS258	Signetics	100
	SN54LS258	† TI	
	SN74LS258	TI	
TTL-S	SN54S258	† AMD	
	SN74S258	AMD	
	54S258	† Fairchild	
	74S258	Fairchild	
	M5S258	Mitsubishi	
	54S258	† Signetics	
	74S258	Signetics	
	SN54S258	† TI	110
	SN74S258	TI	
Quad 2 Input Multiplexer, Non Inverting, Three State			
TTL-LS	AM25LS257C	AMD	
	AM25LS257M	† AMD	
	SN54LS257	† AMD	
	SN74LS257	AMD	
	9LS257C	Fairchild	
	9LS257M	† Fairchild	
	54LS257	† Fairchild	
	74LS257	Fairchild	120
	ITT74LS257	ITT	
	SN54LS257	† Motorola	
	SN74LS257	Motorola	
	DM54LS257	† National	
	DM74LS257	National	
	μPB74LS57	NEC America	
	9LS257C	Raytheon	
	9LS257M	† Raytheon	
	25LS257C	Raytheon	
	25LS257M	† Raytheon	130
	54LS257	† Raytheon	
	74LS257	Raytheon	
	54LS257	† Signetics	
	74LS257	Signetics	

(Continued)

Multiplexers (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)			
	SN54LS257	† TI	
	SN74LS257	TI	
TTL-S	SN54S257	† AMD	
	SN74S257	AMD	
	54S257	† Fairchild	140
	74S257	Fairchild	
	M5S257	Mitsubishi	
	DM74S257	National	
	74S257	Signetics	
	SN54S257	† TI	
	SN74S257	TI	
Quad 2 Input Multiplexer, Inverting, Open Collector			
TTL	RC8234	Raytheon	
	RM8234	† Raytheon	
	N8234	Signetics	150
	S8234	† Signetics	
Quad 2 Input Multiplexer, Conditional Complementing, Open Collector			
TTL	RC8235	Raytheon	
	RM8235	† Raytheon	
	N8235	Signetics	
	S8235	† Signetics	
Quad 3 Input Multiplexer, Conditional Complementing			
TTL	RC8263	Raytheon	
	RM8263	† Raytheon	160
	N8263	Signetics	
	S8263	† Signetics	
Quad 3 Input Multiplexer, Open Collector, Conditional Complementing, Output Enable			
TTL	RC8264	Raytheon	
	RM8264	† Raytheon	
	N8264	Signetics	
	S8264	Signetics	
Quad 2 Input Multiplexer with Storage			
TTL-LS	9LS298C	AMD	170
	9LS298M	† AMD	
	AM25LS09C	AMD	
	AM25LS09M	† AMD	
	SN54LS399	† AMD	
	SN74LS399	AMD	
	9LS298C	Fairchild	
	9LS298M	† Fairchild	
	54LS298	† Fairchild	
	74LS298	Fairchild	
	SN54LS298	† Motorola	180
	SN74LS298	Motorola	
	9LS298C	Raytheon	
	9LS298M	† Raytheon	
	54LS298	† Raytheon	
	74LS298	Raytheon	
	74LS298	Signetics	
	SN54LS298	† TI	
	SN74LS298	TI	
	SN54LS398	† TI	
	SN74LS398	TI	190
	SN54LS399	† TI	
	SN74LS399	TI	
TTL-S	AM25S09C	AMD	
	AM25S09M	† AMD	
Dual 4 Input Multiplexer			
TTL	54153	† Fairchild	
	74153	Fairchild	
	ZN54153	† Ferranti	
	ZN74153	Ferranti	
	HD2564	Hitachi	200

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† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Multiplexers (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	ITT54153	†ITT	
	ITT74153	ITT	
	M53353	Mitsubishi	
	MC4000	Motorola	
	MC4300	†Motorola	
	MC54153	†Motorola	
	MC74153	Motorola	
	DM54153	†National	
	DM74153	National	10
	μPB74153	NEC America	
	54153	†Raytheon	
	74153	Raytheon	
	54153	†Signetics	
	74153	Signetics	
	SN54153	†TI	
	SN74153	TI	
	74153	TRW	
TTL-LS	AM25LS153C	AMD	
	AM25LS153M	†AMD	20
	SN54LS153	†AMD	
	SN74LS153	AMD	
	9LS153C	Fairchild	
	9LS153M	†Fairchild	
	54LS153	†Fairchild	
	74LS153	Fairchild	
	ITT74LS153	ITT	
	SN54LS153	†Motorola	
	SN74LS153	Motorola	
	DM54LS153	†National	30
	DM74LS153	National	
	μPB74LS153	NEC America	
	9LS153C	Raytheon	
	9LS153M	†Raytheon	
	25LS153C	Raytheon	
	25LS153M	†Raytheon	
	54LS153	†Raytheon	
	74LS153	Raytheon	
	54LS153	†Signetics	
	74LS153	Signetics	40
	SN54LS153	†TI	
	SN74LS153	TI	
TTL-S	SN54S153	†AMD	
	SN74S153	AMD	
	54S153	†Fairchild	
	74S153	Fairchild	
	DM74S153	National	
	M5S153	Mitsubishi	
	54S153	†Signetics	
	74S153	Signetics	50
	SN54S153	†TI	
	SN74S153	TI	
Dual 4 Input Multiplexer (Three State 54/75153)			
TTL	DM7214	†National	
	DM8214	National	
Dual 4 Input Multiplexer, Three State			
TTL-LS	AM25LS253C	AMD	
	AM25LS253M	†AMD	
	SN54LS253	†AMD	
	SN74LS253	AMD	60
	9LS253C	Fairchild	
	9LS253M	†Fairchild	
	54LS253	†Fairchild	
	74LS253	Fairchild	
	ITT74LS253	ITT	
	SN54LS253	†Motorola	
	SN74LS253	Motorola	
	DM54LS253	†National	

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Multiplexers (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)			
	DM74LS253	National	70
	μPB74LS253	NEC America	
	9LS253C	Raytheon	
	9LS253M	†Raytheon	
	25LS253C	Raytheon	
	25LS253M	†Raytheon	
	54LS253	†Raytheon	
	74LS253	Raytheon	
	54LS253	†Signetics	
	74LS253	Signetics	
	SN54LS253	†TI	80
	SN74LS253	TI	
TTL-S	SN54S253	†AMD	
	SN74S253	AMD	
	54S253	†Fairchild	
	74S253	Fairchild	
	DM74S253	National	
	54S253	†Signetics	
	74S253	Signetics	
Dual 4 Input Multiplexer, Inverting			
TTL-LS	54LS352	†Fairchild	90
	74LS352	Fairchild	
	DM54LS352	†National	
	DM74LS352	National	
	SN54LS352	†TI	
	SN74LS352	TI	
Dual 3 Input Multiplexer, Inverting, Three State			
TTL-LS	54LS353	†Fairchild	
	74LS353	Fairchild	
	DM54LS353	†National	
	DM74LS353	National	100
	SN54LS353	†TI	
	SN74LS353	TI	
Dual 4 Input Multiplexer, Complementary Output			
TTL	9309C	AMD	
	9309M	†AMD	
	9309C	Fairchild	
	9309M	†Fairchild	
	ITT9309-1	†ITT	
	ITT9309-5	ITT	
	MC8309	Motorola	110
	MC9309	†Motorola	
	DM8309	National	
	DM9309	National	
	μPB9309	NEC America	
	N9309	Signetics	
	S9309	†Signetics	
	SN29309	TI	
	SN39309	†TI	
8 Input Multiplexer, Inverted Output			
TTL	54152	†Fairchild	120
	74152	Fairchild	
	MC54152	†Motorola	
	MC74152	Motorola	
	DM7210	†National	
	DM7211	†National	
	DM8210	National	
	DM8211	National	
	54152	†Raytheon	
	74152	Raytheon	
	54152	†Signetics	130
	SN54152A	†TI	
	74152	TRW	
TTL-LS	9LS152C	Fairchild	
	9LS152M	†Fairchild	
	54LS152	†Fairchild	

(Continued)

Multiplexers (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)			
	74LS152	Fairchild	
	SN54LS152	†Motorola	
	SN74LS152	Motorola	
	9LS152C	Raytheon	140
	9LS152M	†Raytheon	
	54LS152	†Raytheon	
	74LS152	Raytheon	
	SN54LS152	†TI	
8 Input Multiplexer, Complementary Output			
TTL	9312C	AMD	
	9312M	†AMD	
	9312C	Fairchild	
	9312M	†Fairchild	
	ITT9312-1	†ITT	150
	ITT9312-5	ITT	
	MC8312	Motorola	
	MC9312	†Motorola	
	DM8312	National	
	DM9312	†National	
	μPB9312	NEC America	
	RC8230	Raytheon	
	RC8232	Raytheon	
	RC9312	Raytheon	
	RM8230	†Raytheon	160
	RM8232	†Raytheon	
	RM9312	†Raytheon	
	N8230	Signetics	
	S8230	†Signetics	
	N9312	Signetics	
	N8232	Signetics	
	S8232	†Signetics	
	SN29312	TI	
	SN39312	†TI	
TTL-S	N82S30	Signetics	170
	N82S31	Signetics	
	N82S32	Signetics	
8 Input Multiplexer, Complementary Output, Strobe			
TTL	54151	†Fairchild	
	74151	Fairchild	
	ZN54151	†Ferranti	
	ZN74151	Ferranti	
	HD2549	Hitachi	
	HD2571	Hitachi	
	HD74151	Hitachi	180
	ITT54151	†ITT	
	ITT74151	ITT	
	M53351	Mitsubishi	
	MC54151	†Motorola	
	MC74151	Motorola	
	DM54151A	†National	
	DM74151A	National	
	μPB74151	NEC America	
	54151	†Raytheon	
	74151	Raytheon	190
	54151	†Signetics	
	74151	Signetics	
	SN54151A	†TI	
	SN74151A	TI	
	74151	TRW	
TTL-LS	AM25LS151C	AMD	
	AM25LS151M	†AMD	
	SN54LS151	†AMD	
	SN74LS151	AMD	
	9LS151C	Fairchild	200
	9LS151M	†Fairchild	
	54LS151	†Fairchild	
	74LS151	Fairchild	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

IC MASTER

DIGITAL–TTL (Cont'd)

Multiplexers (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)			
	ITT74LS151	ITT	
	SN54LS151	† Motorola	
	SN74LS151	Motorola	
	DM54LS151	† National	
	DM74LS151	National	
	μPB74LS151	NEC America	
	9LS151C	Raytheon	
	9LS151M	Raytheon	
	25LS151C	Raytheon	10
	25LS151M	† Raytheon	
	54LS151	† Raytheon	
	74LS151	Raytheon	
	54LS151	† Signetics	
	74LS151	Signetics	
	SN54LS151	† TI	
	SN74LS151	TI	
TTL-S	SN54S151	† AMD	
	SN74S151	AMD	
	54S151	† Fairchild	20
	74S151	Fairchild	
	93S12C	Fairchild	
	93S12M	† Fairchild	
	HD74S151	Hitachi	
	M5S151	Mitsubishi	
	DM74S151	National	
	54S151	† Signetics	
	74S151	Signetics	
	SN54S151	† TI	
	SN74S151	TI	30
8 Input Multiplexer, Complementary Output (Three State 54/74151)			
TTL	DM7121	† National	
	DM8121	National	
8 Input Multiplexer, Complementary Output, Open Collector			
TTL	9313C	Fairchild	
	9313M	† Fairchild	
	RC8231	Raytheon	
	RM8231	† Raytheon	40
	N8231	Signetics	
	S8231	† Signetics	
	N9313	Signetics	
8 Input Multiplexer, Strobe, Complementary Output, Three State			
TTL	DM54251	† National	
	DM74251	National	
	SN54251	† TI	
	SN74251	TI	
TTL-LS	AM25LS251C	AMD	50
	AM25LS251M	† AMD	
	SN54LS251	† AMD	
	SN74LS251	AMD	
	9LS251C	Fairchild	
	9LS251M	† Fairchild	
	54LS251	† Fairchild	
	74LS251	Fairchild	
	ITT74LS251	ITT	
	SN54LS251	† Motorola	
	SN74LS251	Motorola	60
	μPB74LS151	NEC America	
	9LS251C	Raytheon	
	9LS251M	† Raytheon	
	25LS251C	Raytheon	
	25LS251M	† Raytheon	
	54LS251	† Raytheon	
	74LS251	Raytheon	

(Continued)

Multiplexers (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)			
	54LS251	† Signetics	70
	74LS251	Signetics	
	SN54LS251	† TI	
	SN74LS251	TI	
TTL-S	SN54S251	† AMD	
	SN74S251	AMD	
	54S251	† Fairchild	
	74S251	Fairchild	
	HD74S251	Hitachi	
	M5S251	Mitsubishi	
	DM74S251	National	80
	74S251	Signetics	
	SN54S251	† TI	
	SN74S251	TI	
8 Input Multiplexer, Inverting/Non Inverting, Control Storage			
TTL-LS	AM25LS2535C	AMD	
	AM25LS2535M	† AMD	
	AM2922C	AMD	
	AM2922M	† AMD	
Dual 8 Input Multiplexer (two 8 to 1 sections)			90
TTL	SN74351	TI	
16 Input Multiplexer, Inverted Output, Strobe			
TTL	54150	† Fairchild	
	74150	Fairchild	
	ZN54150	† Ferranti	
	ZN74150	Ferranti	
	HD2548	Hitachi	
	HD74150	Hitachi	
	M53350	Mitsubishi	
	MC54150	† Motorola	100
	MC74150	Motorola	
	DM54150	† National	
	DM74150	National	
	μPB74150	NEC America	
	54150	† Raytheon	
	74150	Raytheon	
	54150	† Signetics	
	74150	Signetics	
	SN54150	† TI	
	SN74150	TI	110
	74150	TRW	
16 Input Multiplexer (Three State 54/74150)			
TTL	DM7219	† National	
	DM8219	National	
10 Input, Quad, 8 to 1 Programmable Multiplexer, Three State.			
TTL	**29693C**	**Raytheon (1494)**	
	29693M	**† Raytheon (1494)**	

Multivibrators

Function	Device	Source	Line
Monostable Multivibrator, Schmitt Trigger Input			
TTL	54121	† Fairchild	120
	74121	Fairchild	
	ZN54121	† Ferranti	
	ZN74121	Ferranti	
	HD2543	Hitachi	
	HD74121	Hitachi	
	ITT54121	† ITT	
	ITT74121	ITT	
	M53321	Mitsubishi	
	MC54121	† Motorola	
	MC74121	Motorola	130
	DM54121	† National	
	DM74121	National	

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Multivibrators (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	54121	† Signetics	
	74121	Signetics	
	SN54121	† TI	
	SN74121	TI	
	TD34121	Toshiba	
	74121	TRW	
Retriggerable Monostable Multivibrator			140
TTL	9601C	AMD	
	9601M	† AMD	
	9601C	Fairchild	
	9601M	† Fairchild	
	ITT9601-1	ITT	
	ITT9601-5	† ITT	
	MC8601	Motorola	
	MC9601	† Motorola	
	DM8601	National	
	DM9601	† National	150
	RF8601	Raytheon	
	RF9601	† Raytheon	
	N8T22	Signetics	
	SN29601	TI	
Retriggerable Monostable Multivibrator, with Reset			
TTL	9600C	AMD	
	9600M	† AMD	
	AM2600C	AMD	
	AM2600M	† AMD	
	9600C	Fairchild	160
	9600M	† Fairchild	
Retriggerable Monostable Multivibrator with Clear			
TTL	54122	† Fairchild	
	74122	Fairchild	
	ZN54122	† Ferranti	
	ZN74122	Ferranti	
	ITT54122	† ITT	
	ITT74122	ITT	
	M53322	Mitsubishi	
	MC54122	† Motorola	170
	MC74122	Motorola	
	74122	Signetics	
	SN54122	† TI	
	SN74122	TI	
TTL-LS	DM54LS122	† National	
	DM74LS122	National	
	9LS122C	**Raytheon (275)**	
	9LS122M	**† Raytheon (275)**	
	54LS122	**† Raytheon (275)**	
	74LS122	**Raytheon (275)**	180
	SN54LS122	† TI	
	SN74LS122	TI	
Bidirectional Monostable Multivibrator (Low Level Input)			
TTL	RC8T20	Raytheon	
	RM8T20	† Raytheon	
	N8T20	Signetics	
Dual Monostable Multivibrator, Schmitt Trigger Input (Dual 54/74121)			
TTL	SN54221	† AMD	190
	SN74221	AMD	
	74221	Signetics	
	SN54221	† TI	
	SN74221	TI	
TTL-LS	ITT74LS221	ITT	
	DM54LS221	† National	
	DM74LS221	National	
	9LS221C	**Raytheon (275)**	

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† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Multivibrators (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)			
	9LS221M	**† Raytheon (275)**	
	54LS221	**† Raytheon (275)**	
	74LS221	**Raytheon (275)**	
	54LS221	† Signetics	
	74LS221	Signetics	
	SN54LS221	TI	
	SN74LS221	TI	
Dual Retriggerable Monostable Multivibrator with Reset (OR Triggered)			10
TTL	AM2602C	AMD	
	AM2602M	† AMD	
	9602C	AMD	
	9602M	† AMD	
	96L02C	Fairchild	
	96L02M	† Fairchild	
	9602C	Fairchild	
	9602M	† Fairchild	
	ITT9602-1	† ITT	20
	ITT9602-5	ITT	
	MC8602	Motorola	
	MC9602	† Motorola	
	DM8602	National	
	DM9602	† National	
	µPB9602	NEC America	
	RF8602	Raytheon	
	RF9602	† Raytheon	
	N9602	Signetics	
	S9602	† Signetics	30
TTL-S	AM26S02C	AMD	
	AM26S02M	† AMD	
	96S02C	Fairchild	
	96S02M	† Fairchild	
Dual Retriggerable Monostable Multivibrator with Clear (AND Triggered)			
TTL	AM26123C	AMD	
	AM26123M	† AMD	
	SN54123	† AMD	
	SN74123	AMD	40
	54123	† Fairchild	
	74123	Fairchild	
	ZN54123	† Ferranti	
	ZN74123	Ferranti	
	HD2561	Hitachi	
	ITT54123	† ITT	
	ITT74123	ITT	
	M53323	Mitsubishi	
	MC54123	† Motorola	
	MC74123	Motorola	50
	DM54123	† National	
	DM74123	National	
	µPB74123	NEC America	
	54123	† Raytheon	
	74123	Raytheon	
	54123	† Signetics	
	74123	Signetics	
	SN54123	† TI	
	SN74123	TI	
	74123	TRW	60
TTL-LS	AM25LS123C	AMD	
	AM25LS123M	† AMD	
	SN54LS123	† AMD	
	SN74LS123	AMD	
	ITT74LS123	ITT	
	DM54LS123	† National	
	DM74LS123	National	
	9LS123C	**Raytheon (275)**	
	9LS123M	**† Raytheon (275)**	

(Continued)

Multivibrators (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)			
	54LS123	**† Raytheon (275)**	
	74LS123	**Raytheon (275)**	
	SN54LS123	† TI	
	SN74LS123	TI	
Dual Monostable Multivibrator (Double Edge)			
TTL	DM7853	† National	
	DM8853	National	
Dual Voltage Controlled Multivibrator			
TTL	11C24C	Fairchild	80
	MC4024	Motorola	
	MC4324	† Motorola	

Shift Registers

Function	Device	Source	Line
4 Bit Parallel Input, Parallel Output Shift Register			
TTL	9300C	AMD	
	9300M	† AMD	
	SN54195	† AMD	
	SN74195	AMD	
	9300C	Fairchild	
	9300M	† Fairchild	
	54195	† Fairchild	90
	74195	Fairchild	
	ITT9300-1	† ITT	
	ITT9300-5	ITT	
	ITT54195	† ITT	
	ITT74195	ITT	
	MC8300	Motorola	
	MC9300	† Motorola	
	MC54195	† Motorola	
	MC74195	Motorola	
	DM8300	National	100
	DM9300	† National	
	DM54195	† National	
	DM74195	National	
	µPB74195	NEC America	
	RC9300	Raytheon	
	RM9300	† Raytheon	
	54195	† Raytheon	
	74195	Raytheon	
	54195	† Signetics	
	74195	Signetics	110
	N9300	Signetics	
	SN29300	TI	
	SN39300	† TI	
	SN54195	† TI	
	SN74195	TI	
TTL-LS	AM25LS195AC	AMD	
	AM25LS195AM	† AMD	
	SN54LS195A	† AMD	
	SN74LS195A	AMD	
	9LS195C	Fairchild	120
	9LS195M	† Fairchild	
	54LS195	† Fairchild	
	74LS195	Fairchild	
	ITT74LS195A	ITT	
	SN54LS195	† Motorola	
	SN74LS195	Motorola	
	µPB74LS195	NEC America	
	9LS195AC	Raytheon	
	9LS195AM	† Raytheon	
	25LS195AC	Raytheon	130
	25LS195AM	† Raytheon	
	54LS195A	† Raytheon	
	74LS195A	Raytheon	
	54LS195A	† Signetics	
	74LS195A	Signetics	

(Continued)

Shift Registers (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)			
	SN54LS195A	† TI	
	SN74LS195A	TI	
TTL-S	SN54S195	† AMD	
	SN74S195	AMD	140
	93S00C	Fairchild	
	93S00M	† Fairchild	
	54S195	Fairchild	
	74S195	Fairchild	
	DM74S195	National	
	74S179	Signetics	
	74S195	Signetics	
	N82S70	Signetics	
	N82S71	Signetics	
	SN54S195	† TI	150
	SN74S195	TI	
4 bit Parallel In, Parallel Out, Right/Left Shift Register			
TTL	5495	† Fairchild	
	7495	Fairchild	
	ZN5495A	† Ferranti	
	ZN7495A	Ferranti	
	HD2534	Hitachi	
	ITT5495	† ITT	
	ITT7495	ITT	
	M5395	Mitsubishi	160
	M53295	Mitsubishi	
	MC4012	Motorola	
	MC5495	† Motorola	
	MC7495	Motorola	
	DM5495	† National	
	DM7495	National	
	5495	† Signetics	
	7495	Signetics	
	SN5495A	† TI	
	SN7495A	TI	170
	TD3495	Toshiba	
TTL-LS	9LS95C	Fairchild	
	9LS95M	† Fairchild	
	54LS95	† Fairchild	
	74LS95	Fairchild	
	ITT74LS95B	ITT	
	SN54LS95	† Motorola	
	SN74LS95	Motorola	
	9LS95BC	Raytheon	
	9LS95BM	† Raytheon	180
	54LS95B	† Raytheon	
	74LS95B	Raytheon	
	74LS95B	Signetics	
	SN54LS95B	† TI	
	SN74LS95B	TI	
4 bit Universal Bidirectional Shift Register			
TTL	SN54194	† AMD	
	SN74194	AMD	
	54194	† Fairchild	
	74194	Fairchild	190
	ZN54194	† Ferranti	
	ZN74194	Ferranti	
	HD74194	Hitachi	
	ITT54194	† ITT	
	ITT74194	ITT	
	MC54194	† Motorola	
	MC74194	Motorola	
	DM54194	† National	
	DM74194	National	
	54194	† Raytheon	200
	74194	Raytheon	
	54194	† Signetics	
	74194	Signetics	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Shift Registers (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	SN54194	† TI	
	SN74194	TI	
TTL-LS	AM25LS194AC	AMD	
	AM25LS194AM	† AMD	
	SN54LS194A	† AMD	
	SN74LS194A	AMD	
	9LS194C	Fairchild	
	9LS194M	† Fairchild	
	54LS194	† Fairchild	10
	74LS194	Fairchild	
	ITT74LS194A	ITT	
	SN54LS194	† Motorola	
	SN74LS194	Motorola	
	μPB74LS194	NEC America	
	9LS194AC	Raytheon	
	9LS194AM	† Raytheon	
	25LS194AC	Raytheon	
	25LS194AM	† Raytheon	
	54LS194A	† Raytheon	20
	74LS194A	Raytheon	
	74LS194A	Signetics	
	SN54LS194A	† TI	
	SN74LS194A	TI	
TTL-S	SN54S194	† AMD	
	SN74S194	AMD	
	54S194	† Fairchild	
	74S194	Fairchild	
	74S194	Signetics	
	SN54S194	† TI	30
	SN74S194	TI	
4 bit Parallel In, Parallel Out, Right/Left Shift Register, Three State			
TTL-LS	9LS295C	Fairchild	
	9LS295M	† Fairchild	
	54LS295	† Fairchild	
	74LS295	Fairchild	
	SN54LS295	† Motorola	
	SN74LS295	Motorola	
	μPB74LS295	NEC America	
	9LS295AC	Raytheon	
	9LS295AM	† Raytheon	
	54LS295A	† Raytheon	
	74LS295A	Raytheon	
	74LS295	Signetics	
	SN54LS295B	† TI	
	SN74LS295B	TI	
4 bit Parallel In, Parallel Out, Cascadable Shift Register, Three State			
TTL-LS	9LS395C	Fairchild	50
	54LS395	† Fairchild	
	74LS395	Fairchild	
	DM54LS395	† National	
	DM74LS395	National	
	μPB74LS395	NEC America	
	9LS395C	**Raytheon (291)**	
	9LS395M	**† Raytheon (291)**	
	54LS395	**† Raytheon (291)**	
	74LS395	**Raytheon (291)**	
	54LS395	† Signetics	60
	74LS395	Signetics	
	SN54LS395A	† TI	
	SN74LS395A	TI	
4 bit Parallel In, Serial Out, Shift Register			
TTL	5494	† Fairchild	
	7494	Fairchild	
	ZN5494	† Ferranti	

(Continued)

Shift Registers (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	ZN7494	Ferranti	
	HD2533	Hitachi	70
	MC5494	† Motorola	
	MC7494	Motorola	
	5494	† Signetics	
	7494	Signetics	
	SN5494	† TI	
	SN7494	TI	
4 bit Parallel In, Serial Out, Shift Register, (with load, shift, hold control)			
TTL	54178	† Fairchild	
	74178	Fairchild	80
	MC7270	Motorola	
	MC8270	† Motorola	
	RC8270	Raytheon	
	RM8270	† Raytheon	
	S8270	† Signetics	
	N8270	Signetics	
	SN54178	† TI	
	SN74178	TI	
4 bit Parallel In, Serial Out, Shift Register, with Reset, Complementary Output for last bit			90
TTL	54179	† Fairchild	
	74179	Fairchild	
	MC7271	Motorola	
	MC8271	† Motorola	
	RC8271	Raytheon	
	RM8271	† Raytheon	
	N8271	Signetics	
	S8271	† Signetics	
	SN54179	† TI	
	SN74179	TI	100
TTL-S	74S179	Signetics	
4 bit Universal Shift Register, Binary Up/Down Counter, Synchronous			
TTL-S	SN74S291	TI	
5 bit Parallel In, Parallel Out, Shift Register			
TTL	5496	† Fairchild	40
	7496	Fairchild	
	ZN5496	† Ferranti	
	ZN7496	Ferranti	
	HD2546	Hitachi	110
	HD7496	Hitachi	
	ITT5496	† ITT	
	ITT7496	ITT	
	M53296	Mitsubishi	
	MC5496	† Motorola	
	MC7496	Motorola	
	DM5496	† National	
	DM7496	National	
	5496	† Signetics	
	7496	Signetics	120
	SN5496	† TI	
	SN7496	TI	
	7496	TRW	
TTL-LS	ITT74LS96	ITT	
	54LS96	† Signetics	
	74LS96	Signetics	
	SN54LS96	† TI	
	SN74LS96	TI	
5 bit Right/Left Shift Register with Clear			
TTL	M54403	Mitsubishi	130
8 bit Parallel In, Parallel Out, Unidirectional Shift Register			
TTL	54199	† Fairchild	

(Continued)

Shift Registers (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)			
	74199	Fairchild	
	HD74199	Hitachi	
	M53399	Mitsubishi	
	DM54199	† National	
	DM74199	National	140
	54199	† Raytheon	
	74199	Raytheon	
	54199	† Signetics	
	74199	Signetics	
	SN54199	† TI	
	SN74199	TI	
8 bit Parallel In, Parallel Out, Right/Left Shift Register			
TTL	54198	† Fairchild	
	74198	Fairchild	
	HD74198	Hitachi	150
	M53398	Mitsubishi	
	DM54198	† National	
	DM74198	National	
	μPB74198	NEC America	
	54198	† Raytheon	
	74198	Raytheon	
	54198	† Signetics	
	74198	Signetics	
	SN54198	† TI	
	SN74198	TI	160
8 bit Universal Shift Register, Three State			
TTL	DM7546	† National	
	DM8546	National	
TTL-LS	AM25LS23C	AMD	
	AM25LS23M	† AMD	
	AM25LS299C	AMD	
	AM25LS299M	† AMD	
	SN54LS299	† AMD	
	SN74LS299	AMD	
	SN54LS323	† AMD	170
	SN74LS323	AMD	
	ITT74LS299	ITT	
	ITT74LS323	ITT	
	9LS299C	Raytheon	
	9LS299M	† Raytheon	
	25LS23C	**Raytheon (300)**	
	25LS23M	**† Raytheon (300)**	
	25LS299C	**Raytheon (302)**	
	25LS299M	**† Raytheon (302)**	
	54LS299	† Raytheon	180
	74LS299	Raytheon	
	SN54LS299	† TI	
	SN74LS299	TI	
	SN54LS323	† TI	
	SN74LS323	TI	
TTL-S	SN54S299	† TI	
	SN74S299	TI	
8 bit Parallel In, Serial Out Shift Register, Complementary Output			
TTL	54165	† Fairchild	190
	74165	Fairchild	
	ZN54165	† Ferranti	
	ZN74165	Ferranti	
	M53365	Mitsubishi	
	MC54165	† Motorola	
	MC74165	Motorola	
	DM54165	† National	
	DM74165	National	
	54165	† Raytheon	
	74165	Raytheon	200
	54165	† Signetics	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Shift Registers (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)	74165	Signetics	
	SN54165	† TI	
	SN74165	TI	
TTL-LS	54LS165	† Fairchild	
	74LS165	Fairchild	
	SN54LS165	† TI	
	SN74LS165	TI	
8 bit Parallel In, Serial Out Shift Register with Clear			
TTL	54166	† Fairchild	10
	74166	Fairchild	
	ZN54166	† Ferranti	
	ZN74166	Ferranti	
	HD74166	Hitachi	
	M53366	Mitsubishi	
	DM54166	† National	
	DM74166	National	
	54166	† Raytheon	
	74166	Raytheon	20
	54166	† Signetics	
	74166	Signetics	
	SN54166	† TI	
	SN74166	TI	
TTL-LS	SN54LS166	† TI	
	SN74LS166	TI	
8 bit Gated Serial In, Parallel Out Shift Register			
TTL	SN54164	† AMD	
	SN74164	AMD	
	54164	† Fairchild	30
	74164	Fairchild	
	ZN54164	† Ferranti	
	HD74164	Hitachi	
	ZN74164	Ferranti	
	ITT54164	† ITT	
	ITT74164	ITT	
	M53364	Mitsubishi	
	DM7570	† National	
	DM8570	National	
	DM54164	† National	40
	DM74164	National	
	μPB74164	NEC America	
	54164	† Raytheon	
	74164	Raytheon	
	54164	† Signetics	
	74164	Signetics	
	SN54164	† TI	
	SN74164	TI	
	TD3503	Toshiba	
TTL-LS	AM25LS164C	AMD	50
	AM25LS164M	AMD	
	SN54LS164	† AMD	
	SN74LS164	AMD	
	ITT74LS164	ITT	
	9LS164C	Fairchild	
	9LS164M	† Fairchild	
	54LS164	† Fairchild	
	74LS164	Fairchild	
	SN54LS164	† Motorola	
	SN74LS164	Motorola	60
	DM54LS164	† National	
	DM74LS164	National	
	μPB74LS164	NEC America	
	9LS164C	**Raytheon (272)**	
	9LS164M	**† Raytheon (272)**	
	54LS164	**† Raytheon (272)**	
	74LS164	**Raytheon (272)**	
	54LS164	† Signetics	

(Continued)

Shift Registers (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)	74LS164	Signetics	70
	SN54LS164	† TI	
	SN74LS164	TI	
8 bit Serial In, Serial Out Shift Register			
TTL	5491	† Fairchild	
	7491	Fairchild	
	ZN5491	† Ferranti	
	ZN7491	Ferranti	
	HD2524	Hitachi	
	ITT5491A	† ITT	
	ITT7491A	ITT	80
	M5391	Mitsubishi	
	M53291	Mitsubishi	
	MC5491	† Motorola	
	MC7491	Motorola	
	DM5491A	† National	
	DM7491A	National	
	μPB7491	NEC America	
	N8276	Signetics	
	5491	† Signetics	
	7491	Signetics	90
	SN5491A	† TI	
	SN7491A	TI	
	TD3491	Toshiba	
TTL-LS	**9LS91C**	**Raytheon (272)**	
	9LS91M	**† Raytheon (272)**	
	54LS91	**† Raytheon (272)**	
	74LS91	**Raytheon (272)**	
	SN54LS91	† TI	
	SN74LS91	TI	
8 bit Serial/Parallel In Register with Sign Extend (for use with 25LS14/74LS384 Multiplier)			100
TTL-LS	AM25LS22C	AMD	
	AM25LS22M	† AMD	
	SN54LS322	† AMD	
	SN74LS322	AMD	
	25LS22C	**Raytheon (297)**	
	25LS22M	**† Raytheon (297)**	
	SN54LS322	† TI	
	SN74LS322	TI	
Octal Storage Register, two stage 4 bit wide shift register			110
TTL-LS	SN54LS396	† TI	
	SN74LS396	TI	
Dual Rank 8 bit Shift Register (8 bit I/O buffer, "A" register, and serial "B" register)			
TTL-LS	DM76LS52	† National	
	DM86LS52	National	
	DM76LS62	† National	
	DM86LS62	National	
10 bit Parallel In, Parallel Out Buffer Register, with Reset (clocked flip flops)			120
TTL	RC8202	Raytheon	
	RM8202	† Raytheon	
	N8202	Signetics	
	S8202	† Signetics	
10 bit Parallel In, Parallel Out Buffer Register, with Reset, Inverting Output (clocked flip flops)			
TTL	RC8203	Raytheon	
	RM8203	† Raytheon	
	N8203	Signetics	
	S8203	† Signetics	130
10 bit Parallel In, Serial Out Shift Register			
TTL	RC8274	Raytheon	
	RM8274	† Raytheon	

(Continued)

Shift Registers (Cont'd)

Function	Device	Source	Line
TTL (Cont'd.)	N8274	Signetics	
	S8274	Signetics	
10 bit Serial In, Parallel Out Shift Register			
TTL	RC8273	Raytheon	
	RM8273	† Raytheon	140
	N8273	Signetics	
	S8273	† Signetics	
Dual 5 bit Parallel In, Parallel Out Buffer Register, (clocked flip flops)			
TTL	RC8200	Raytheon	
	RM8200	† Raytheon	
	N8200	Signetics	
	S8200	† Signetics	
Dual 5 bit Parallel In, Parallel Out, Buffer Register, Inverting Output (clocked flip flops)			150
TTL	RC8201	Raytheon	
	RM8201	† Raytheon	
	N8201	Signetics	
	S8201	† Signetics	
Dual 8 bit Serial In, Serial Out, Shift Register			
TTL	9328C	AMD	
	9328M	† AMD	
	9328C	Fairchild	
	9328M	† Fairchild	
	ITT9328-1	† ITT	160
	ITT9328-5	ITT	
	MC8328	Motorola	
	MC9328	† Motorola	
	RC8277	Raytheon	
	RM8277	† Raytheon	
	N8277	Signetics	
4 bit Shifter, Three State (Shifts 0, 1, 2, or 3 bits under 2 Line Select Control)			
TTL-S	AM25S10C	AMD	
	AM25S10M	† AMD	170
	N25S10	Signetics	

Translators

Function	Device	Source	Line
Hex DTL to TTL Inverter			
TTL	9109C	Fairchild	
	9109M	† Fairchild	
Hex TTL to DTL Inverter			
TTL	9112C	Fairchild	
	9112M	† Fairchild	
Dual MOS to TTL Level Converter			
TTL	9625C	Fairchild	
	9625M	† Fairchild	180
Dual MOS to TTL Level Translator, Three State			
TTL	MC4068	Motorola	
	MC4368	† Motorola	
	MC54468	† Motorola	
	MC74468	Motorola	
7 Unit MOS to TTL Level Converter			
TTL	SN75270	TI	
Dual 2 Input NAND Gate, High Voltage to TTL Interface, to 30v Input			
TTL	N8T18	Signetics	190
	S8T18	† Signetics	
Dual TTL to MOS Voltage Translator			
TTL	D130A	† Siliconix	
	D130B	Siliconix	
	D139A	† Siliconix	
	D139B	Siliconix	

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Function	Device	Source	Line
Translators (Cont'd)			
Dual 2 Input NAND TTL to MOS Voltage Translator			
TTL	9624C	Fairchild	
	9624M	† Fairchild	
	DH0034	† National	
	DH0034C	National	
	DS7800	† National	
	DS8800	National	
	SN55180	† TI	
	SN75180	TI	
Hex TTL to MOS Voltage Translator			
TTL	DS7812	† National	10
	DS8812	National	
	DS78L12	† National	
	DS88L12	National	
	D123A	† Siliconix	
	D123B	Siliconix	
	D125A	† Siliconix	
	D125B	Siliconix	
Quad 2 Input NAND TTL to MOS Voltage Translators			
TTL	DS7810	† National	
	DS8810	National	20
	DS7811	† National	
	DS8811	National	
Quad 2 Input AND TTL to MOS Voltage Translators			
TTL	DS7819	† National	
	DS8819	National	
Dual ECL to MOS Driver (also ECL to TTL)			
TTL	MC75358	Motorola	
	MC75368	Motorola	
	SN75368	TI	
Quad TTL to MOS Inverter/Driver, Three State			30
TTL	ITT75367	ITT	
	SN75357	TI	
	SN75367	TI	
For other translators, see Interface Sense Amplifiers and also Memory and Peripheral Drivers			
Miscellaneous			
Programmable Logic Array, Mask Programmed (See also Memory PLAs)			
TTL	DM7575	† National	
	DM7576	**† National**	**(1285)**
	DM8575	**National**	**(1285)**
	DM8576	**National**	**(1285)**
TTL-S	N82S200	Signetics	40
	N82S201	Signetics	
Programmable Logic Arrays, Field Programmable (See also Memory PLAs)			
TTL	IM5200	Intersil	
	HM7660	Harris	
	HM7661	Harris	
TTL-S	82S100	MMI	
	82S101	MMI	50
	N82S100	Signetics	
	S82S100	† Signetics	
	N82S101	Signetics	
	S82S101	† Signetics	
	SN54S330	† TI	
	SN74S330	TI	
	SN54S331	† TI	
	SN74S331	TI	
4 bit True/Complement Zero/One Element			
TTL-H	54H87	† Fairchild	60
	74H87	Fairchild	
	MC54H87	† Motorola	

(Continued)

Function	Device	Source	Line
Miscellaneous (Cont'd)			
TTL-H (Cont'd.)			
	MC74H87	Motorola	
	SN54H87	† TI	
	SN74H87	TI	
Dual 4 Input Expander (for H50, H53, H55)			
TTL-H	54H60	† Fairchild	
	74H60	Fairchild	
	ITT54H60	† ITT	70
	ITT74H60	ITT	
	DM54H60	† National	
	DM74H60	National	
	54H60	† Signetics	
	74H60	Signetics	
	SN54H60	† TI	
	SN74H60	TI	
Triple 3 Input Expander (for H52)			
TTL-H	54H61	† Fairchild	
	74H61	Fairchild	80
	DM54H61	National	
	54H61	† Signetics	
	74H61	Signetics	
	SN54H61	† TI	
	SN74H61	TI	
3 2 2 3 Input AND OR Expander (for H50, H53, H55)			
TTL-H	54H62	† Fairchild	
	74H62	Fairchild	
	DM54H62	† National	
	DM74H62	National	90
	54H62	† Signetics	
	74H62	Signetics	
	SN54H62	† TI	
	SN74H62	TI	
8 bit Successive Approximation Register			
TTL	AM2502C	AMD	
	AM2502M	† AMD	
	AM2503C	AMD	
	AM2503M	† AMD	
	2502	Intersil	100
	2503	Intersil	
	DM2502	† National	
	DM2502C	National	
	DM2503	† National	
	DM2503C	National	
12 bit Successive Approximation Register			
TTL	AM2504C	AMD	
	AM2504M	† AMD	
	2504	Intersil	
	DM2504	† National	110
	DM2504C	National	
8 bit Position Scaler (The output is shifted with respect to the input up to 8 positions as determined by a 3 bit selector code.)			
TTL	RC8243	Raytheon	
	RM8243	† Raytheon	
	N8243	Signetics	
	S8243	† Signetics	
6 bit Synchronous Binary Rate Multiplier			
TTL	5497	† Fairchild	120
	7497	Fairchild	
	MC5497	† Motorola	
	MC7497	Motorola	
	SN5497	† TI	
	SN7497	TI	
Synchronous Decade Rate Multiplier			
TTL	54167	† Fairchild	
	74167	Fairchild	

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Function	Device	Source	Line
Miscellaneous (Cont'd)			
TTL (Cont'd.)			
	MC54167	† Motorola	130
	MC74167	Motorola	
	SN54167	† TI	
	SN74167	TI	
TTL-S	54S167	† Fairchild	
	74S167	Fairchild	
4 bit Priority Register, Cascadable			
TTL	M53478	Mitsubishi	
	SN54278	† TI	
	SN74278	TI	
TTL-LS	SN54LS278	† TI	140
	SN74LS278	TI	
8 Input Priority Encoder			
TTL	9318C	AMD	
	9318M	† AMD	
	9318C	Fairchild	
	9318M	† Fairchild	
	HD74148	Hitachi	
	M53348	Mitsubishi	
	MC8318	Motorola	
	MC9318	† Motorola	150
	DM8318	National	
	DM9318	† National	
	DM54148	† National	
	DM74148	National	
	μPB74148	NEC America	
	54148	† Signetics	
	74148	Signetics	
	SN29318	TI	
	SN39318	† TI	
	SN54148	† TI	160
	SN74148	TI	
TTL-LS	AM2913C	AMD	
	AM2913M	† AMD	
	AM25LS148C	AMD	
	AM25LS148M	† AMD	
	SN54LS148	† AMD	
	SN74LS148	AMD	
	AM25LS2513C	AMD	
	AM25LS2513M	† AMD	
	SN54LS148	† TI	170
	SN74LS148	TI	
	SN54LS348	† TI	
	SN74LS348	TI	
10 Input Priority Encoder			
TTL	HD74147	Hitachi	
	M53347	Mitsubishi	
	DM54147	† National	
	DM74147	National	
	μPB74147	NEC America	
	54147	† Signetics	180
	74147	Signetics	
	SN54147	† TI	
	SN74147	TI	
TTL-LS	SN54LS147	† TI	
	SN74LS147	TI	
8 bit Parity Tree			
TTL	MC4008	Motorola	
	MC4308	† Motorola	
	MC54408	† Motorola	
	MC74408	Motorola	190
Dual 4 bit Parity Tree			
TTL	MC4010	Motorola	
	MC4310	† Motorola	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Miscellaneous (Cont'd)

Function	Device	Source	Line
9 bit Parity Generator/Checker			
TTL	DM7220	† National	
	DM8220	National	
9 bit Odd/Even Parity Generator/Checker			
TTL	54180	† Fairchild	
	74180	Fairchild	
	ZN54180	† Ferranti	
	ZN74180	Ferranti	
	HD2525	Hitachi	
	HD74180	Hitachi	
	ITT54180	† ITT	10
	ITT74180	ITT	
	M53380	Mitsubishi	
	MC54180	† Motorola	
	MC74180	Motorola	
	DM54180	† National	
	DM74180	National	
	µPB8262	NEC America	
	µPB74180	NEC America	
	54180	† Raytheon	
	74180	Raytheon	20
	RC8262	Raytheon	
	RM8262	† Raytheon	
	N8262	Signetics	
	S8262	† Signetics	
	54180	† Signetics	
	74180	Signetics	
	SN54180	† TI	
	SN74180	TI	
	74180	TRW	
TTL-LS	54LS280	† Fairchild	
	74LS280	Fairchild	30
	SN54LS280	† TI	
	SN74LS280	TI	
TTL-S	82S62C	AMD	
	82S62M	† AMD	
	93S62C	Fairchild	
	93S62M	† Fairchild	
	DM74S280	National	
	74S280	Signetics	
	N82S62	Signetics	40
	SN54S280	† TI	
	SN74S280	TI	
12 Input Odd/Even Parity Checker/Generator			
TTL	9348C	Fairchild	
	9348M	† Fairchild	
TTL-S	93S48C	AMD	
	93S48M	† AMD	
Cyclic Redundancy Checker			
TTL	9401C	Fairchild	
	9401M	† Fairchild	50
4 bit Universal Presettable Polynomial Generator			
TTL	MC8504	Motorola	
Polynomial Generator			
TTL	MC8506	Motorola	
Single Error Hamming Code Detector and Generator			
TTL	MC4041	Motorola	
BCD To Binary/Binary To BCD Number Converter			
TTL	MC4001	Motorola	
BCD To Binary Converter			
TTL	ZN54184	† Ferranti	
	ZN74184	Ferranti	60
	DM54184	† National	
	DM74184	National	
	SN54184	† TI	
	SN74184	TI	

Miscellaneous (Cont'd)

Function	Device	Source	Line
BCD To Binary Converter (Three State 54/74184)			
TTL	DM8898	National	
Binary To BCD Converter			
TTL	M53385	Mitsubishi	
	DM54185A	† National	70
	DM74185A	National	
	DM8899	National	
	SN54185A	† TI	
	SN74185A	TI	
Dual Pulse Synchronizer/Driver			
TTL	MC54120	† Motorola	
	MC74120	Motorola	
	SN54120	† TI	
	SN74120	TI	
Quad Power Strobe (Vcc strobe or digit driver)			80
TTL	HD6600-2	† Harris	
	HD6600-5	Harris	
	HD6605-2	† Harris	
	HD6605-5	Harris	
Phase Frequency Detector			
TTL	11C44C	Fairchild	
	MC4044	Motorola	
	MC4344	† Motorola	
Contact Bounce Eliminator			
TTL	DM7544	† National	90
	DM8544	National	
Quad Complementary Output Elements (for symmetrical generation of complementary outputs)			
TTL	SN54265	† TI	
	SN74265	TI	
Dual Zero Crossing Detector			
TTL	N8T363	Signetics	
MOS Dynamic Memory Refresh Logic Circuit			
TTL	MC8505	Motorola	
Data Encryption, 4 Device Set			100
I^2L	9414	Fairchild	
	9415	Fairchild	
	9416	Fairchild	
	9417	Fairchild	
Dual 4 Input NAND Schmitt Trigger			
TTL	5413	† Fairchild	
	7413	Fairchild	
	ZN5413	† Ferranti	
	ZN7413	Ferranti	
	HD2545	Hitachi	110
	ITT5413	† ITT	
	ITT7413	ITT	
	M53213	Mitsubishi	
	MC5413	† Motorola	
	MC7413	Motorola	
	DM5413	† National	
	DM7413	National	
	µPB7413	NEC America	
	5413	† Signetics	
	7413	Signetics	120
	SN5413	† TI	
	SN7413	TI	
	7413	TRW	
TTL-LS	9LS13C	Fairchild	
	9LS13M	† Fairchild	
	54LS13	† Fairchild	
	74LS13	Fairchild	
	ITT74LS13	ITT	
	SN74LS13	Motorola	
	DM54LS13	† National	130
	DM74LS13	National	

(Continued)

Miscellaneous (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)			
	9LS13C	**Raytheon (264)**	
	9LS13M	**† Raytheon (264)**	
	54LS13	**† Raytheon (264)**	
	74LS13	**Raytheon (264)**	
	54LS13	† Signetics	
	74LS13	Signetics	
	SN54LS13	† TI	
	SN74LS13	TI	140
Quad 2 Input NAND Schmitt Trigger			
TTL	54132	† Fairchild	
	74132	Fairchild	
	HD74132	Hitachi	
	M53332	Mitsubishi	
	MC54132	† Motorola	
	MC74132	Motorola	
	DM54132	† National	
	DM74132	National	
	54132	† Signetics	150
	74132	Signetics	
	SN54132	† TI	
	SN74132	TI	
TTL-LS	9LS132C	Fairchild	
	9LS132M	† Fairchild	
	54LS132	† Fairchild	
	74LS132	Fairchild	
	ITT74LS132	ITT	
	SN54LS132	† Motorola	
	SN75LS132	Motorola	160
	DM54LS132	† National	
	DM74LS132	National	
	9LS132C	**Raytheon (264)**	
	9LS132M	**† Raytheon (264)**	
	54LS132	**† Raytheon (264)**	
	74LS132	**Raytheon (264)**	
	74LS132	Signetics	
	54LS132	† Signetics	
	SN54LS132	† TI	
	SN74LS132	TI	170
TTL-S	54S132	† Fairchild	
	74S132	Fairchild	
	SN54S132	† TI	
	SN74S132	TI	
Hex Schmitt Trigger, Inverting			
TTL	5414	† Fairchild	
	7414	Fairchild	
	HD7414	Hitachi	
	M53214	Mitsubishi	
	MC5414	† Motorola	180
	MC7414	Motorola	
	DM5414	† National	
	DM7414	National	
	5414	† Signetics	
	7414	Signetics	
	SN5414	† TI	
	SN7414	TI	
TTL-LS	9LS14C	Fairchild	
	9LS14M	† Fairchild	
	54LS14	† Fairchild	190
	74LS14	Fairchild	
	ITT74LS14	ITT	
	SN54LS14	† Motorola	
	SN74SL14	Motorola	
	DM54LS14	† National	
	DM74LS14	National	
	9LS14C	**Raytheon (264)**	
	9LS14M	**† Raytheon (264)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Miscellaneous (Cont'd)

Function	Device	Source	Line
TTL-LS (Cont'd.)			
	54LS14	**† Raytheon (264)**	
	74LS14	**Raytheon (264)**	
	54LS14	† Signetics	
	74LS14	Signetics	
	SN54LS14	† TI	
	SN74LS14	TI	
Voltage Controlled Oscillator (or Crystal Controlled)			
TTL-LS	SN54LS324	† TI	
	SN74LS324	TI	10
Voltage Controlled Oscillator			
TTL-LS	SN74LS320	TI	
Dual Voltage Controlled Oscillator (or Crystal Controlled)			
TTL-LS	SN54LS124	† TI	
	SN74LS124	TI	
	SN54LS325	† TI	
	SN74LS325	TI	
	SN54LS326	† TI	
	SN74LS326	TI	20
	SN54LS327	† TI	
	SN74LS327	TI	
TTL-S	SN54S124	† TI	
	SN74S124	TI	
Voltage Comparator (Analog Input Digital Output)			
TTL-S	686C	AMD	
	686M	**† AMD**	
Decade Sequencer (sequential 1 of 10 Decoder), adjustable sequence length			
TTL	9319C	Fairchild	30
	9319M	† Fairchild	
	9320C	Fairchild	
	9320M	† Fairchild	
Bus Transfer Switch (transmit receive connections to 4 bus terminals)			
TTL	MC4060	Motorola	
	MC4363	† Motorola	
	MC54460	† Motorola	
	MC74460	Motorola	
Triple Bidirectional Bus Switch, Three State (Connects any 2 of 3 inputs together)			40
TTL-S	MC6881	Motorola	
	MC3449	Motorola	
Quad Bus Transceiver			
TTL-LS	ITT74LS242	ITT	
	ITT74LS243	ITT	
	54LS242	**† Raytheon (282)**	
	74LS242	**Raytheon (282)**	
	54LS243	**† Raytheon (282)**	
	74LS243	**Raytheon (282)**	50
	74LS242	Signetics	
	74LS243	Signetics	
	SN54LS242	† TI	
	SN74LS242	TI	
	SN54LS243	† TI	
	SN74LS243	TI	
TTL-S	SN54S242	† AMD	
	SN74S242	AMD	
	SN54S243	† AMD	
	SN74S243	AMD	60
4 bit Parallel Bus Transceiver, Non Inverting, Three State			
TTL-S	N8T28	AMD	
	MC8T28	Motorola	
	MC6889	Motorola	

(Continued)

Miscellaneous (Cont'd)

Function	Device	Source	Line
TTL-S (Cont'd.)			
	N8T28	Signetics	
4 bit Parallel Universal Bus Transceiver, Storage, Three State			70
TTL-S	SN54S226	† TI	
	SN74S226	TI	
4 bit Parallel Bus Transceiver, Inverting Three State			
TTL-S	N8T26	AMD	
	S8T26	† AMD	
	MB424	Fujitsu	
	MC8T26	Motorola	
	N8T26	Signetics	
	SN75136	TI	
4 bit Parallel Bus Transceiver, Open Collector Drivers			80
TTL-S	AM26S10C	AMD	
	AM26S10M	† AMD	
	AM26S11C	AMD	
	AM26S11M	† AMD	
	AM26S12C	AMD	
	AM26S12M	† AMD	
	AM26S12AC	AMD	
	AM26S12AM	† AMD	
	9640C	Fairchild	
	9640M	† Fairchild	90
	9641C	Fairchild	
	9641M	† Fairchild	
	MC26S10	Motorola	
	MC26S11	Motorola	
	26S10C	Raytheon	
	26S10M	Raytheon	
	26S11C	Raytheon	
	26S11M	Raytheon	
	AM26S10C	† TI	
	AM26S10M	† TI	100
	AM26S11C	TI	
	AM26S11M	† TI	
8 bit Bidirection I/O Port			
TTL-S	**N8T31**	**Signetics (1898)**	
8 bit Bidirectional I/O Port, Latched, Addressable			
TTL-S	**N8T32**	**Signetics (1898)**	
	N8T33	**Signetics (1898)**	
	N8T35	**Signetics (1898)**	
	N8T36	**Signetics (1898)**	
	N8T39	**Signetics (1909)**	110
Octal Bus Driver (Schmitt Trigger), Inverting, Three State			
TTL-LS	AM25LS240C	AMD	
	AM25LS240M	† AMD	
	SN54LS240	† AMD	
	SN74LS240	AMD	
	54LS240	† Fairchild	
	74LS240	Fairchild	
	ITT74LS240	ITT	
	54LS240	† MMI	120
	74LS240	MMI	
	57LS300	† MMI	
	67LS300	MMI	
	25LS240C	Raytheon	
	25LS240M	† Raytheon	
	54LS240	**† Raytheon (279)**	
	74LS240	**Raytheon (279)**	
	74LS240	Signetics	
	SN54LS240	† TI	
	SN74LS240	TI	130
TTL-S	SN54S240	† AMD	
	SN74S240	AMD	

(Continued)

Miscellaneous (Cont'd)

Function	Device	Source	Line
TTL-S (Cont'd.)			
	54S240	**† MMI (462)**	
	74S240	**MMI (462)**	
	57S300	† MMI	
	67S300	MMI	
	54S240	† Raytheon	
	74S240	Raytheon	140
	SN54S240	† TI	
	SN74S240	TI	
Octal Bus Driver (Schmitt Trigger), Non Inverting, Three State, Symmetrical Controls			
TTL-LS	AM25LS241C	AMD	
	AM25LS241M	† AMD	
	SN54LS241	† AMD	
	SN74LS241	AMD	
	54LS241	† Fairchild	
	74LS241	Fairchild	150
	ITT74LS241	ITT	
	54LS241	† MMI	
	74LS241	MMI	
	57LS301	† MMI	
	67LS301	MMI	
	25LS241C	Raytheon	
	25LS241M	† Raytheon	
	54LS241	**† Raytheon (279)**	
	74LS241	**Raytheon (279)**	
	74LS241	Signetics	160
	SN54LS241	† TI	
	SN74LS241	TI	
TTL-S	SN54S241	† AMD	
	SN74S241	AMD	
	54S241	**† MMI (462)**	
	74S241	**MMI (462)**	
	57S301	† MMI	
	67S301	MMI	
	54S241	† Raytheon	
	74S241	Raytheon	170
	SN54S241	† TI	
	SN74S241	TI	
Octal Bus Driver (Schmitt Trigger), Non Inverting, Three State, Complementary Controls			
TTL-LS	ITT74LS244	ITT	
	54LS244	† MMI	
	74LS244	MMI	
	57LS304	† MMI	
	67LS304	MMI	
	54LS244	**† Raytheon (279)**	180
	74LS244	**Raytheon (279)**	
	74LS244	Signetics	
	SN54LS244	† TI	
	SN74LS244	TI	
	SN74LS244	AMD	
TTL-S	SN54S244	† AMD	
	SN74S244	AMD	
	54S244	**† MMI (462)**	
	74S244	**MMI (462)**	
	57S304	† MMI	190
	67S304	MMI	
	54S244	† Raytheon	
	74S244	Raytheon	
Octal Bus Transceiver			
TTL-LS	54LS245	† MMI	
	74LS245	MMI	
	57LS305	† MMI	
	67LS305	MMI	
	SN54LS245	† TI	
	SN74LS245	TI	200

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Miscellaneous (Cont'd)

Function	Device	Source	Line
Hex Current Sensing Interface Gate			
TTL-LS	SN54LS63	†TI	
	SN74LS63	TI	
Microprogram Sequencer			
TTL-LS	AM2909C	AMD	
	AM2909M	†AMD	
	AM2911C	AMD	
	AM2911M	†AMD	
	3001	Intel	
	M3001	Intel	
	MC2909C	Motorola	10
	MC2909M	†Motorola	
	MC2911C	Motorola	
	MC2911M	†Motorola	
	IDM2909AC	National	
	IDM2909AM	†National	
	IDM2911AC	National	
	IDM2911AM	†National	
	μPB2909	**NEC Micro (1850)**	
	μPB2911	**NEC Micro (1850)**	
	AM2909C	Raytheon	20
	AM2909M	†Raytheon	
	AM2911C	Raytheon	
	AM2911M	†Raytheon	
	8X02	**Signetics (1877)**	
	N3001	**Signetics (1860)**	
	S3001	**†Signetics (1860)**	
Micro Address Generator (for bit slice microprocessor)			
TTL-S	SN54S482	†TI	
	SN74S482	TI	

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–Special

Other Digital Devices

Function	Device	Source
Arithmetic Processor (supply 5 12v)		
TTL-S	9511	AMD
	9511-4	AMD
	MM5863	National
Arithmetic Processor, 4 functions, ASCII Floating Point Computations (Supply 5v)		
TTL-S	CY-450	Cybernetic
Baud Rate Generator/Programmable Divider (ROM controlled divider)		
TTL-S	MM5307	National
	COM5016T	SMC
	COM5016	SMC
Baud Rate Generator/Programmable Divider, Dual (ROM controlled divider)		
TTL-S	COM5036	SMC
	COM5036T	SMC
	BR1941	Western
Correlator (Continually compares two independently clocked serial inputs and gives correlation output)		
TTL-S	R5401	Reticon
	TCD1004J	TRW
Custom Arrays (Digital and Linear circuits customized in final metalization)		
TTL-S	XR-IIL-CHIP	Exar
	XR-CHIP	Exar
	XR400	Exar
	ECL-Array	Fairchild
	ULA	Ferranti
	MONOCHIP	Interdesign
	MASTERMOS	IMI
	ML200	Master Logic
	707	Micro Tech
	XC160	Motorola
	XC177	Motorola
	XC400	Motorola
	ECL-ARRAY	NEC America
	ECL-ARRAY	Plessey
	ILL-ARRAY	Plessey
	RTL-ARRAY	Plessey
Calculators: See Linear Consumer		
Counter, 16 Bit, Non Volatile Storage, Parallel Input/Output, 500KHz (Supply 29,5v)		
TTL-S	NCR2900	NCR
Counter, 4 Decade (Counts and stores, BCD Output, 0.5 MHz; supply 12,5v)		
TTL-S	AY5-4057	GI
Counter/Display Decoder, 4 Decade (7 Segment and BCD outputs, 0.25 MHz; supply 5v)		
TTL-S	MK5002	Mostek
	MK5005	Mostek
	MK5007	Mostek
Counter, 5 Decade (includes storage, multiplexed BCD output, 0.6 MHz, supply 12,5v)		
TTL-S	3815	Fairchild
Dual Counter (two 3 decade up/down counters with latch, BCD output. 0.5 MHz., supply 5 15 v)		
TTL-S	LS7040	LSI Comp
Counter/Display Driver, 1 Decade Up/Down, (7 segment and BCD output, 0.5 MHz; supply 12, 27v)		
TTL-S	MCS1003	†MOS
Counter/Display Driver, 1 Decade Up/Down, Preset (7 segment and BCD output, 1 MHz)		
TTL-S	HCTR0107	Hughes

Other Digital Devices (Cont'd)

Function	Device	Source
Counter/Display Driver, 4 Decade Up/Down (7 segment output, 0.6 M Hz, supply 12, 5v; BCD; and serial output versions available)		
TTL-S	AY5-4007	GI
	AY5-4007A	GI
	AY5-4007D	GI
Counter/Display Driver, 6 Decade Up/Down (7 segment and BCD output, 1 MHz, presettable compare register, latched output, LED drive maximum count 999999, 995959, or 595999 versions, supply 10 15 v)		
TTL-S	MK50395	Mostek
	MK50396	Mostek
	MK50397	Mostek
	MK50398	Mostek
	MK50399	Mostek
Counter, 6 Decade, BCD output, 5 MHz, 8 latches (supply 5 15v)		
TTL-S	LS7031	LSI Comp
Counter/Display Driver, 7 Decade (7 segment output, supply 2 6v)		
TTL-S	ICM7208	Intersil
Counter, 8 Decade, BCD and 7 segment outputs, 5 MHz, latches (supply 5 15v)		
TTL-S	LS7030	LSI Comp
Counter Time Base (Oscillator, programmable divider, 10^1 to 10^8, $2x10^7$, $6x10^7$, $6x10^8$ and $36x10^8$, (supply 12,5v)		
TTL-S	MK5009	Mostek
Dual Counter/Timer		
TTL-S	MM5865	National
	DF215	**Siliconix (981)**
Down/Up Timer (0.1 and 1 second. Keyboard Entry)		
TTL-S	DF216	Siliconix
Elapsed Time Counter (0.01 seconds to 1 hour, supply 2 5v)		
TTL-S	ICM7205	Intersil
Elapsed Time Counter (0.01 seconds to 24 hours, supply 2 5v)		
TTL-S	ICM7045	Intersil
Elapsed Time Counter, Decimal, 0.1 seconds to 10 hours, maximum count 2399999 (supply 2.5 4.5v)		
TTL-S	ICM7045A	Intersil
Programmable Diode Matrix, 5x5		
TTL-S	HM074	†Harris
	HM075	†Harris
	HM076	†Harris
Programmable Diode Matrix, 5x8		
TTL-S	HM010	†Harris
	HM012	†Harris
	HM013	†Harris
Programmable Diode Matrix, 8x5		
TTL-S	HM080	†Harris
	HM081	†Harris
	HM084	†Harris
Programmable Diode Matrix, 4x10		
TTL-S	HM090	†Harris
	HM091	†Harris
	HM093	†Harris
	HM0110	Harris
Programmable Diode Matrix,10x4		
TTL-S	HM050	†Harris
	HM051	†Harris
	HM055	†Harris

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Other Digital Devices (Cont'd)

Function	Device	Source
TTL-S (Cont'd.)		
	HM0104	Harris
Programmable Diode Matrix,6x8		
TTL-S	HM030	†Harris
	HM031	†Harris
	HM034	†Harris
	HM0168	Harris
Programmable Diode Matrix, 8x6		
TTL-S	HM040	†Harris
	HM041	†Harris
	HM044	†Harris
	HM0186	Harris
Programmable Diode Matrix, 18x5		
TTL-S	M54510	Mitsubishi
Programmable Diode Matrix, 10x16		
TTL-S	S353	Siemens
Divider, divide by 2, 525, supply 12v		
TTL-S	MN115	Panasonic
Divider, divide by 2, 625, supply 12v		
TTL-S	MN116	Panasonic
Programmable Divider (any modulo from 3 to 262,145, supply 12,5)		
TTL-S	3816	Fairchild
Divider, divide by 2, 0.2 to 1 GHz		
TTL-S	MC1690	Motorola
	SP1690B	Plessey
	SP8602A	†Plessey
	SP8602B	Plessey
	SP8602M	Plessey
	SP8603A	†Plessey
	SP8603B	Plessey
	SP8603M	Plessey
	SP8604A	†Plessey
	SP8604B	Plessey
	SP8604M	Plessey
	SP8607A	†Plessey
	SP8607B	Plessey
	SP8607M	Plessey
Divider, divide by 3/4, 40 to 300 MHz		
TTL-S	SP8720	Plessey
Divider, divide by 4, 0.15 to 1 GHz		
TTL-S	MC1697	Motorola
	MC1699	Motorola
	SP8600A	†Plessey
	SP8600B	Plessey
	SP8600M	Plessey
	SP8601A	†Plessey
	SP8601B	Plessey
	SP8601M	Plessey
	SP8613B	Plessey
	SP8613M	Plessey
	SP8614B	Plessey
	SP8614M	Plessey
	SP8615B	Plessey
	SP8615M	Plessey
	SP8616B	Plessey
Divider, divide by 4, above 1 GHz		
TTL-S	11C05C	Fairchild
	11C05M	†Fairchild
	SP8616B	Plessey
	SP8617B	Plessey
	SP8619B	Plessey
Divider, divide by 5, 0.2 to 1 GHz		
TTL-S	SP8620A	†Plessey

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–Special (Cont'd)

Other Digital Devices (Cont'd)

Function	Device	Source	Line
TTL-S (Cont'd.)			
	SP8620B	Plessey	
	SP8620M	Plessey	
	SP8621A	†Plessey	
	SP8621B	Plessey	
	SP8621M	Plessey	
	SP8622B	Plessey	
	SP8622M	Plessey	
Divider, divide by 5/6, 0.2 to 1 GHz			
TTL-S	11C91C	Fairchild	10
	11C91M	†Fairchild	
	95H91C	Fairchild	
	MC12009	Motorola	
	MC12509	†Motorola	
	SP8740A	†Plessey	
	SP8740B	Plessey	
	SP8740M	Plessey	
	SP8745A	†Plessey	
	SP8745B	Plessey	
	SP8745M	Plessey	20
Divider, divide by 6/7, 0.2 to 1 GHz			
TTL-S	SP8741A	†Plessey	
	SP8741B	Plessey	
	SP8741M	Plessey	
	SP8746A	†Plessey	
	SP8746B	Plessey	
	SP8746M	Plessey	
Divider, divide by 8, 0.25 to 1 GHz			
TTL-S	SP8670A	†Plessey	
	SP8670B	Plessey	30
	SP8670M	Plessey	
	SP8671A	†Plessey	
	SP8671B	Plessey	
	SP8671M	Plessey	
	SP8672A	†Plessey	
	SP8672B	Plessey	
	SP8672M	Plessey	
	SP8735B	Plessey	
	SP8736B	Plessey	
Divider, divide by 8, above 1 GHz			40
TTL-S	SP8675B	Plessey	
	SP8675M	Plessey	
	SP8676B	Plessey	
	SP8676M	Plessey	
	SP8677B	Plessey	
	SP8677M	Plessey	
Divider, divide by 8/9, 0.25 to 1 GHz			
TTL-S	MC12011	Motorola	
	MC12511	†Motorola	
	SP8743B	Plessey	50
	SP8743M	Plessey	
	SP8748B	Plessey	
	SP8748M	Plessey	
Divider, divide by 10, 0.2 to 1 GHz			
TTL-S	SP8505	Plessey	
	SP8515	Plessey	
	SP8630A	†Plessey	
	SP8630B	Plessey	
	SP8630M	Plessey	
	SP8631A	†Plessey	60
	SP8631B	Plessey	
	SP8631M	†Plessey	
	SP8632A	Plessey	
	SP8632B	Plessey	
	SP8632M	Plessey	
	SP8634B	Plessey	
	SP8635B	Plessey	

(Continued)

Other Digital Devices (Cont'd)

Function	Device	Source	Line
TTL-S (Cont'd.)			
	SP8636B	Plessey	
	SP8637B	Plessey	70
	SP8660A	†Plessey	
	SP8660B	Plessey	
	SP8660M	Plessey	
Divider, divide by 10, above 1 GHz			
TTL-S	SP8665B	Plessey	
	SP8666B	Plessey	
	SP8667B	Plessey	
Divider, divide by 10/11, 0.2 to 1 GHz			
TTL-S	11C90C	Fairchild	
	11C90M	†Fairchild	80
	95H90C	Fairchild	
	95H90M	†Fairchild	
	MC12013	Motorola	
	MC12513	†Motorola	
	SP8640A	†Plessey	
	SP8640B	Plessey	
	SP8640M	Plessey	
	SP8641A	†Plessey	
	SP8641B	Plessey	
	SP8641M	Plessey	90
	SP8642A	†Plessey	
	SP8642B	Plessey	
	SP8642M	Plessey	
	SP8643B	Plessey	
	SP8643M	Plessey	
	SP8646A	†Plessey	
	SP8646B	Plessey	
	SP8646M	Plessey	
	SP8647A	†Plessey	
	SP8647B	Plessey	100
	SP8647M	Plessey	
	SP8685A	†Plessey	
	SP8685B	Plessey	
	SP8685M	Plessey	
	SP8690A	†Plessey	
	SP8690B	Plessey	
	SP8690M	Plessey	
	SP8695A	†Plessey	
	SP8695B	Plessey	
	SP8695M	Plessey	110
Divider, divide by 16, 0.2 to 1 GHz			
TTL-S	SP8650A	†Plessey	
	SP8650B	Plessey	
	SP8650M	Plessey	
	SP8651A	†Plessey	
	SP8651B	Plessey	
	SP8651M	Plessey	
	SP8652A	†Plessey	
	SP8652B	Plessey	
	SP8652M	Plessey	120
	SP8659A	†Plessey	
	SP8659B	Plessey	
	SP8659M	Plessey	
Divider, divide by 20, 0.2 to 1 GHz			
TTL-S	SP8657A	†Plessey	
	SP8657B	Plessey	
	SP8657M	Plessey	
Divider, divide by 32, 0.2 to 1 GHz			
TTL-S	SP8655A	†Plessey	
	SP8655B	Plessey	130
	SP8655M	Plessey	
Divider, divide by 64, 0.2 to 1 GHz			
TTL-S	SP4020	Plessey	

Other Digital Devices (Cont'd)

Function	Device	Source	Line
Divider, divide by 64, above 1 GHz			
TTL-S	SP8750B	Plessey	
	SP8750M	Plessey	
	SP8751B	Plessey	
	SP8751M	Plessey	
	SP8752B	Plessey	
Divider, divide by 100, to 150MHz			140
TTL-S	DS8629	National	
	SP8627	Plessey	
	SP8628	Plessey	
	SP8629	Plessey	
Divider, divide by 256, above 1 GHz			
TTL-S	SP8770B	Plessey	
	SP8771B	Plessey	
	SP8772B	Plessey	
Divider Extender, divide by 4, to extend division ratios of two modulus counters while maintaining the difference (ie 5/6 to 20/21)			150
TTL-S	SP8790A	†Plessey	
	SP8790B	Plessey	
	SP8790M	Plessey	
Divider Extender, divide by 8 (ie extends 5/6 to 40/41)			
TTL-S	SP8794A	†Plessey	
	SP8794B	Plessey	
	SP8794M	Plessey	
DVM Logic, 3 1/2 Decade (for dual ramp integration DVM, BCD or 7 Segment Output; supply 12 to 18 or 18 to 24v)			160
TTL-S	AY5-3507	GI	
	AY5-3510	GI	
DVM Logic 3 3/4 Digit (ramp integration BCD or 7 segment output, supply 7.5, 15)			
TTL-S	AY5-3500	GI	
DVM Logic, 4 Digits (supply 17v)			
TTL-S	MN6032	Panasonic	
DVM Logic, 4 1/2 Digit, (dual slope integration, supply 15,5)			170
TTL-S	ADB4500	National	
DVM Logic, 4 1/2 Decade (Multiplexed BCD output; supply 12,5v)			
TTL-S	3814C	Fairchild	
DVM Logic, 4 3/4 Digit, (dual ramp integration, BCD and 7 segment output, supply 5v)			
TTL-S	AY3-3550	GI	
DVM Logic: See also Interface Analog to Digital Converters, Decimal Output			
Electronic Organ Circuits: See Linear Consumer			180
Flip Flop, D Type (750 MHz, ECL or TTL supplies)			
TTL-S	11C06C	Fairchild	
Flip Flop, D Type Master Slave (ECL or TTL supplies)			
TTL-S	11C70C	Fairchild	
Frequency Synthesizers: See Linear Phase Locked Loop Circuits			
Frequency to Voltage: See Linear Other Devices			
Gate, Dual OR/NOR (5/4 Input, 700ns delay, ECL or TTL supplies)			
TTL-S	11C01C	Fairchild	190
Gate, Dual OR/NOR (4 Input, 0.5 ns delay, ECL supply)			
TTL-S	SP16F60	Plessey	

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–Special (Cont'd)

Other Digital Devices (Cont'd)

Function	Device	Source	Line
Hall Effect Switch (senses magnetic field)			
TTL-S	DN830	Panasonic	
	DM831	Panasonic	
	DN834	Panasonic	
	DN835	Panasonic	
	DN837	Panasonic	
	DN838	Panasonic	
	DN839	Panasonic	
	SAS211	Siemens	
	ULN-3006	Sprague	
	ULN-3008	Sprague	10
	ULS-3006	Sprague	
	TL170	TI	
Inverter, Triple PMOS			
TTL-S	LM8942	Sanyo	
Latch, Quad with non volatile memory			
TTL-S	MN9102	Plessey	
Multiplexer/Demultiplexer, 8 channel latched, binary addressable(Supply 5 to 70v)			
TTL-S	LS7110	LSI Comp	
Multivibrator, astable (programmable pulse width, current controlled pulse rep. rate, supply 3 7v)			20
TTL-S	MC3380	Motorola	
Pulse Group Encoder (2141) and Decoder (2151) for pulse width code systems (25^3 codes programmed by RC networks)			
TTL-S	TMX2141	TMX	
	TMX2151	TMX	
Regulators, Switching: See Linear Other Devices			
Schmitt Trigger, Complementary Open Collector Output (supply 2.2 to 6v)			30
TTL-S	ULN-3303	Sprague	
Schmitt Trigger (Supply 8 to 16v)			
TTL-S	LB8015	Sanyo	
Schmitt Trigger, Programmable			
TTL-S	CA3098	†RCA	
	CA3099	†RCA	
Schmitt Trigger, Zener Clamped Output (supply 2.2 to 6v)			
TTL-S	MCC102	Micro Comp	
	ULN-3304	Sprague	40
Schmitt Trigger, Dual, Complementary Open Collector Outputs (supply 2.2 to 6v)			
TTL-S	MCC122	Micro Comp	
	ULN-3305	Sprague	
Schmitt Trigger, Dual one Open Collector Output, one Zener Clamped Output (supply 2.2 to 6v)			
TTL-S	ULN-3306	Sprague	
Schmitt Trigger, Dual, Low voltage; 3.5v			
TTL-S	SN76811	TI	
Sequential Boolean Analyzer, microprogrammable			50
TTL-S	SBA	GI	
Serial to Parallel Converter, 33 bits (shift register with output latch)			
TTL-S	MM5559	National	
Shift Register, 8 bit with 8 corresponding analog switches			
TTL-S	SD5350	Signetics	
Timers: See Linear Timers			
Voltage to Frequency: See Linear Other Devices			
Watch Circuits See Linear Consumer Circuits			60

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

Consumer Circuits

Part No.	Description	Digits	Power Supplies	Process	Packages
S1424A	Five Function LCD Watch with alternating time/date mode and voltage tripler display options	3½	+1.5V	CMOS	Die
S1424C	Five Function LCD Watch Circuit	3½	+1.5V	CMOS	Die
S1425A	Five Function LCD Watch Circuit	3½	+1.5V	CMOS	Chip Carrier
S1427A	Five Function LCD Watch Circuit	3½	+1.5V	CMOS	40 Pin DIP
S1856	Digital Clock Circuit — LED/Gas Discharge Auto Clock	3½	+6V to +16V	P-I^2	40 Pin DIP
S1998A	50/60Hz Line LED Clock Circuit	4	+8V to +26V	P-I^2	40 Pin DIP
S1998B	50/60Hz Line Clock — Gas Discharge	4	+8V to +33V	P-I^2	40 Pin DIP
S1998C	50/60Hz Line Clock — Fluorescent	4	+8V to +16V	P-I^2	40 Pin DIP
S2709	Fluorescent Automotive Digital Clock	4	+12V	P-I^2	22 Pin Plastic
S2733	Six Function LCD Watch Circuit	4	+1.5V	CMOS	40 Pin Plastic

Organ Circuits

Part No.	Description	Process	Power Supplies	Power Dissipation	Packages
S10110	Analog Shift Register	P-I^2	-24V	—	8 Pin Plastic
S10111	Analog Shift Register	P-I^2	-24V	—	8 Pin Plastic
S10129	Six-Stage Frequency Divider	P-I^2	-14V, -27V	350mW	14 Pin Plastic
S10130	Six-Stage Frequency Divider	P-I^2	-14V, -27V	350mW	14 Pin Plastic
S10131	Six-Stage Frequency Divider	P-I^2	-14V, -27V	350mW	14 Pin Plastic
S2193	Seven-Stage Frequency Divider	P-I^2	-14V, -28V	300mW	14 Pin Plastic
S2567	Rhythm Counter	HI V_T	-15V, -27V	400mW	14 Pin Plastic
S50240	Top Octave Synthesizer	P-I^2	-11V, -16V	360mW	16 Pin Plastic
S50241	Top Octave Synthesizer	P-I^2	-11V, -16V	360mW	16 Pin Plastic
S50242	Top Octave Synthesizer	P-I^2	-11V, -16V	360mW	16 Pin Plastic
S50243	Top Octave Synthesizer	P-I^2	-11V, -16V	360mW	16 Pin Plastic
S50244	Top Octave Synthesizer	P-I^2	-11V, -16V	360mW	16 Pin Plastic
S50145	Top Octave Synthesizer	P-I^2	-11V, -16V	360mW	16 Pin Plastic
S8890	Rhythm Generator	P-I^2	-12V	400mW	40 Pin Plastic
S9660	Rhythm Generator	P-I^2	-12V	400mW	28 Pin Plastic

Remote Control Circuits

Part No.	Description	Process	Power Supplies	I/O Bits	Packages
S2600	Remote Control Transmitter	CMOS	+7V to +10V	11	16 Pin Plastic
S2601	Remote Control Receiver	P-I^2	+10V to +18V	5	22 Pin Plastic

Also available from AMI is the S2742/S2743/S2744 three-chip set for serial data encoding, decoding, and sequencing. The S2742 is the serial data decoder; the S2743 is the serial data encoder; the S2744 is the sequencer. The circuits are designed for coded remote control applications. Very few external parts are needed for most applications.

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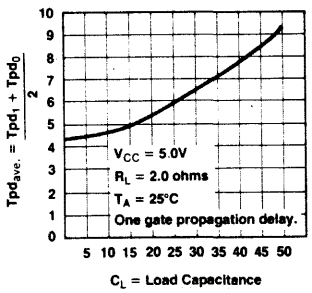
Total Low-Power Schottky From Raytheon 25LS/9LS/54LS/74LS

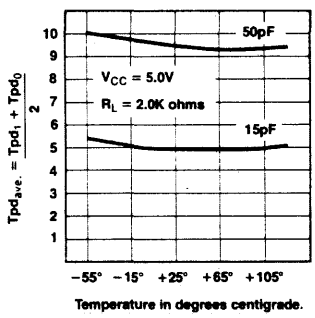
Raytheon offers the full performance range of low-power Schottky devices: The new military standard 9LS, the high-performance 25LS, the old military standard 54LS and the industrial/commercial standard 74LS.

Raytheon specifies the more stringent JAN 38510 AC load measurements, as well as the standard 15pF and 2K ohms load. The AC parameters for both loads are specified across the full operating temperature range. Raytheon has compiled the most comprehensive specifications available in the industry. See for yourself that Raytheon standard products will meet or exceed your most demanding requirements.

Development Plan Raytheon is one of the largest suppliers of both flat packs and dual-in-line ceramic packages to the military market. We have 99 types available now, including 34 JAN qualified devices, with an additional 25 new products in development.

	NOW	1978	TOTAL
GATES	40	0	40
FLIP-FLOPS	9	0	9
MSI	50	25	75
TOTAL	99	25	124





For your own full digital product catalog, contact your local distributor or Raytheon Company, Semiconductor Division, Dept. LS, 350 Ellis Street, Mountain View, California 94042, (415) 968-9211.

Low-Power Schottky Families

Parameter	Old Military Standard 54LS	New Military Standard 9LS	High-Permormance 25LS
I_{OL}	4mA($V_{OL(MAX)}$=0.4V)	4mA($V_{OL(MAX)}$=0.4V)	8mA($V_{OL(MAX)}$=0.45V)
I_{OSL}	15mA-100mA	15mA-100mA	15mA-100mA
t_{PLH}	20nS Max.	10nS Max.	10nS Max.
t_{PHL}	20nS Max.	10nS Max.	10nS Max.
Fanout	11	11	22

RAYTHEON

SEMICONDUCTOR DIVISION

1-1

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RAYTHEON
Your source for low-power Schottky

9LS/54LS/74LS LOW-POWER SCHOTTKY

Type	Description
LS00	Quad 2-input NAND gate
LS01	Quad 2-input NAND gate, OC
LS02	Quad 2-input NOR gate, OC
LS03	Quad 2-input NAND gate, OC
LS04	Hex inverter
LS05	Hex inverter, OC
LS08	Quad 2-input AND gate
LS09	Quad 2-input AND gate, OC
LS10	Triple 3-input NAND gate
LS11	Triple 3-input AND gate
LS12	Triple 3-input NAND gate, OC
LS13	Dual 4-input Schmitt trigger
LS14	Hex Schmitt trigger
LS15	Triple 3-input AND gate, OC
LS20	Dual 4-input NAND gate
LS21	Dual 4-input AND gate
LS22	Dual 4-input NAND gate, OC
LS26	Quad 2-input NAND, 15V, OC
LS27	Triple 3-input NOR gate
LS28	Quad 2-input NOR buffer
LS30	8-input NAND gate
LS32	Quad 2-input OR gate
LS33	Quad 2-input NOR buffer, OC
LS37	Quad 2-input NAND buffer
LS38	Quad 2-input NAND buffer, OC
LS40	Dual 4-input NAND buffer
LS42	1-of-10 decoder
LS43	Excess 3 to decimal decoder
LS44	Excess gray to decimal decoder
LS51	Dual AOI gate
LS54	2-3-3-2-input AOI gate
LS55	2-wide, 4-input AOI gate
LS73	Dual J-K flip-flop
LS74	Dual D flip-flop
LS75	Quad transparent latch
LS76	Dual J-K flip-flop
LS77	Quad transparent latch
LS78	Dual J-K flip-flop
LS83A	4-bit full adder
LS85	4-bit magnitude comparator
LS86	Quad exclusive OR gate
LS90	Decade counter
LS91	8-bit shift register
LS92	Divide by 12 counter
LS93	4-bit binary counter
LS95B	4-bit shift register
LS107	Dual J-K flip-flop
LS109	Dual J-K flip-flop
LS112	Dual J-K edge-triggered flip-flop
LS113	Dual J-K edge-triggered flip-flop
LS114	Dual J-K edge-triggered flip-flop
LS122	Retriggerable one-shot
LS123	Dual one-shot
LS125	Quad 3-state buffer, low enable
LS126	Quad 3-state buffer, high enable
LS132	Quad 2-input Schmitt trigger
LS136	Quad exclusive OR gate, OC
LS137	Decoder/demultiplexer
LS138	3-to-8 decoder/demultiplexer
LS139	Dual 2-to-4 decoder/demultiplexer
LS151	8-to-1 line multiplexer
LS152	8-to-1 line multiplexer
LS153	Dual 4-to-1 multiplexer
LS155	Dual 2-to-4 decoder/demultiplexer
LS156	Dual 2-to-4 decoder/demultiplexer, OC
LS157	Quad 2-to-1 line multiplexer
LS158	Quad 2-to-1 line multiplexer, inverting
LS160	Decade counter, async clear
LS161	Binary counter, async clear
LS162	Decade counter, sync clear
LS163	Binary counter, sync clear
LS164	8-bit shift register (SIPO)
LS170	4 x 4 register file, OC
LS174	Hex D-type flip-flop
LS175	Quad D-type flip-flop
LS181	4-bit arithmetic logic unit
LS190	BCD decade counter, mode control
LS191	4-bit binary counter, mode control
LS192	BCD decade counter, up/down
LS193	4-bit binary counter, up/down
LS194A	4-bit universal shift register
LS195A	4-bit parallel shift register
LS196	4-bit presettable decade counter
LS197	4-bit presettable binary counter
LS221	Dual one-shot (very stable)
LS240	Octal inverting bus driver
LS241	Octal non-inverting bus driver
LS242	Quad transceiver
LS243	Quad transceiver
LS244	Octal 3-state driver
LS251	8-to-1 line multiplexer, TS
LS253	Dual 4-to-1 multiplexer, TS
LS254	1-of-16 decoder, TS
LS255	Dual 2-to-4 decoder/demultiplexer, TS
LS257	Quad 2-to-1 line multiplexer, TS
LS258	Quad 2-to-1 line multiplexer, inverting, TS
LS261	2 x 4 binary multiplier
LS266	Quad exclusive NOR gate, OC
LS279	Quad set/reset latch
LS283	4-bit full adder, fast carry
LS295A	4-bit shift register, TS
LS298	Quad 2-multiplexer with output register
LS299	8-bit universal shift register
LS322	8-bit serial/parallel register with sign extender
LS323	8-bit shift/storage register with sync clear
LS365	Hex buffer, common enable, TS
LS366	Hex inverter, common enable, TS
LS367	Hex buffer, 4-bit and 2-bit, TS
LS368	Hex inverter, 4-bit and 2-bit, TS
LS373	Octal transparent latch
LS374	Octal D flip-flop
LS377	Octal D flip-flop with enable
LS384	8-bit serial/parallel two's compliment multiplier
LS385	Quad serial adder/subtractor
LS395A	4-bit shift register, TS
LS670	4 x 4 register file, TS

25LS HIGH-PERFORMANCE LOW-POWER SCHOTTKY

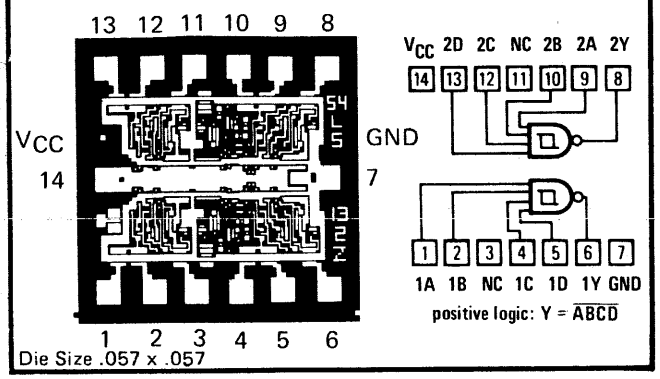
LS14	8-bit serial/parallel two's complement multiplier
LS15	Quad serial adder/subtractor
LS22	8-bit serial/parallel register with sign extender
LS23	8-bit shift/storage register with sync clear
LS122	Single retriggerable monostable multivibrator with clear
LS123	Dual retriggerable monostable multivibrator with clear
LS138	3-to-8 line decoder/demultiplexer
LS139	Dual 2-to-4 line decoder/demultiplexer
LS151	8-to-1 line multiplexer, complementary outputs
LS153	Dual 4-to-1 line multiplexer
LS157	Quad 2-to-1 line multiplexer
LS158	Quad 2-to-1 line multiplexer, inverting
LS160	BCD decade counter, async clear
LS161	4-bit binary counter, async clear
LS162	BCD decade counter, sync clear
LS163	4-bit binary counter, sync clear
LS170	4 x 4 register file, OC
LS174	Hex D-type flip-flop with clear
LS175	Quad D-type flip-flop with clear
LS181	4-bit arithmetic logic unit
LS190	BCD decade up/down counter, sync
LS191	4-bit binary up/down counter, sync
LS192	BCD decade up/down counter, sync
LS193	4-bit binary up/down counter, sync
LS194A	4-bit bidirectional universal shift register
LS195A	4-bit parallel access shift register
LS251	8-to-1 line multiplexer, TS
LS253	Dual 4-to-1 line data selectors/multiplexers, TS
LS257	Quad 2-to-1 line multiplexer, TS
LS258	Quad 2-to-1 line multiplexer, TS
LS299	8-bit universal shift/storage register
LS670	4 x 4 register file, TS

TS = tri-state outputs

OC = open collectors

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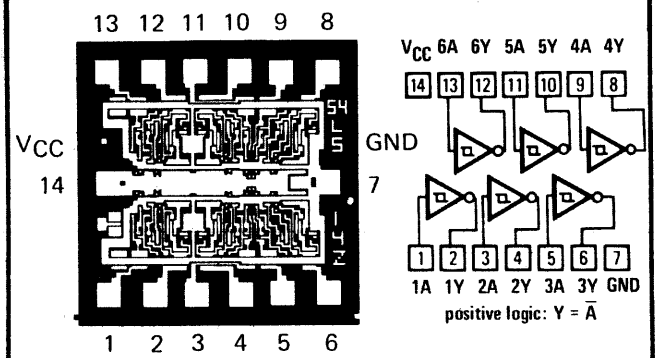
LS13
DUAL 4-INPUT SCHMITT TRIGGER



Die Size .057 x .057

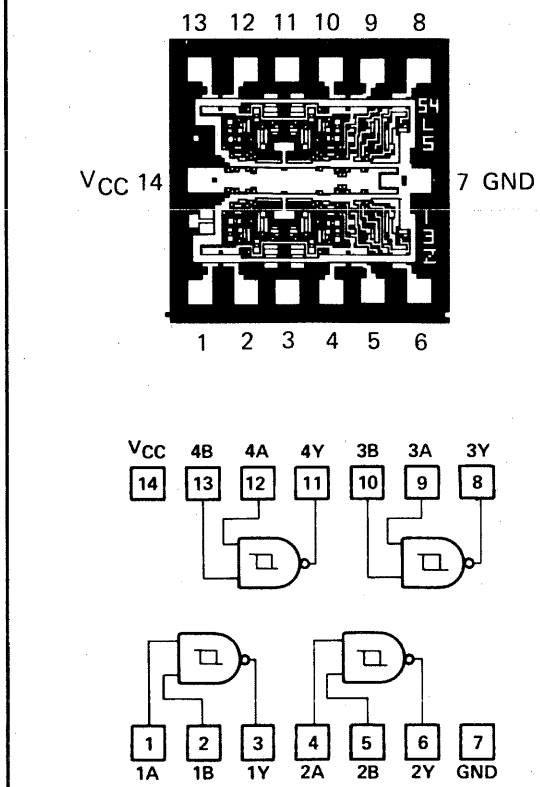
NC- No internal connection

LS14
HEX SCHMITT TRIGGER



Die Size .057 x .057

LS132
QUAD 2-INPUT SCHMITT TRIGGER



Die Size .057 x .057

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

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Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{T+}	V_{CC} = 5V		1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	V_{CC} = 5V		.5	.8	1.0	.5	.8	1.0	V
$V_{T+} - V_{T-}$	V_{CC} = 5V		0.4	0.8		0.4	0.8		V
V_I	V_{CC} = MIN, I_I = -18 mA			-0.65	-1.5		-0.65	-1.5	V
V_{OH}	V_{CC} = MIN, I_{OH} = -400μA, V_I = 0.6V		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_I = 2V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_{T+}	V_{CC} = 5V $V_I = V_{T+}$			-0.14			-0.14		mA
I_{T-}	V_{CC} = 5V $V_I = V_{T-}$			-0.18			-0.18		mA
I_I	V_{CC} = MAX, V_I = 7V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7V				20			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4V				-0.4			-0.4	mA
I_{OS}	V_{CC} = MAX		-15		-100	-15		-100	mA
I_{CCH}	V_{CC} = MAX, V_I = 0V	LS13		2.9	6		2.9	6	mA
		LS14, LS132		8.6	16		8.6	16	
I_{CCL}	V_{CC} = MAX, V_I = 4.5V	LS13		4.1	7		4.1	7	mA
		LS14, LS132		12	21		12	21	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter		−55°C			+25°C			+125°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ											
t_{PLH}	LS13	16	28			15	22		16	30	ns
	LS14	16	28			15	22		16	30	
	LS132	16	24			13	20		16	24	
t_{PLH}	LS13	22	38			18	27		20	38	ns
	LS14	17	32			15	22		16	30	
	LS132	16	24			13	20		16	24	
Test Conditions: C_L = 50 pF, R_L = 2kΩ											
t_{PLH}	LS13	20	38			20	27		20	38	ns
	LS14	20	38			20	27		21	38	
	LS132	20	29			17	25		20	29	
t_{PHL}	LS13	25	42			25	33		25	42	ns
	LS14	21	38			20	27		21	38	
	LS132	20	29			17	25		20	29	

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

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FEATURES

- All Outputs Are High for Invalid Input Conditions
- Also for Application as
  - 4-Line to 16-Line Decoders
  - 3-Line to 8-Line Decoders

DESCRIPTION

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The LS42 BCD-to-decimal decoders, the LS43 excess-3-to-decimal decoders, and the LS44 excess-3-gray-to-decimal decoders feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits.

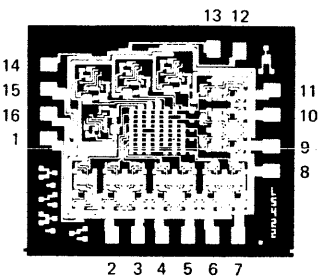
54LS circuits are characterized for operation over the full military temperature range of −55°C to 125°C; 74LS circuits are characterized for operation from 0°C to 70°C.

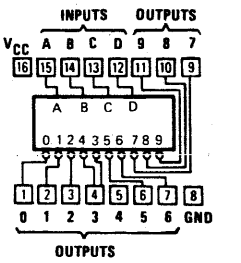
NO.	LS42 BCD INPUT				LS43 EXCESS 3-INPUT				LS44 EXCESS 3-GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
	D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	L	H	L	L	L	H	H	L	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	L	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	L	H	H	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	L	L	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

PIN-OUT DIAGRAM

LS42
BCD-TO-DECIMAL DECODER

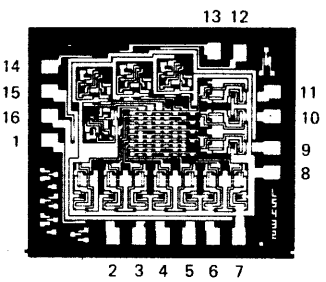


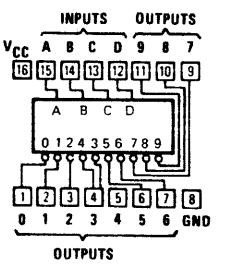


positive logic: see function table

Die Size .077 x .065

LS43
EXCESS-3-TO-DECIMAL DECODER

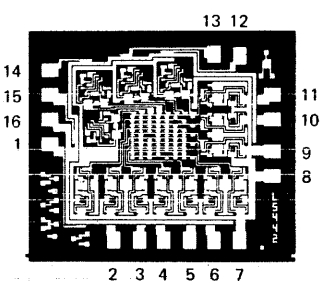


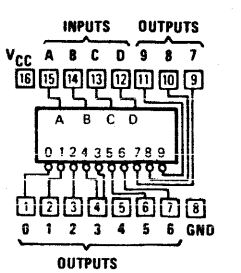


positive logic: see function table

Die Size .077 x .065

LS44
EXCESS-3-GRAY-TO-DECIMAL DECODER





positive logic: see function table

Die Size .077 x .065

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Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max I_{OH}=-400μA		2.5	3.5		2.7	3.5		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††	V_{CC}=MAX,			7	13		7	13	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††I_{CC} is measured with all outputs open and inputs grounded.

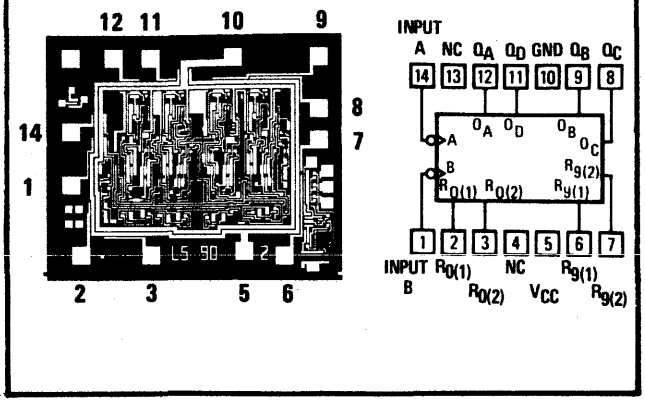
Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (Input)	To (Output)	-55°C			+25°C			+125°C			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2kΩ												
t_{PHL}	A,B,C or D	Any output 2 gate delay		15	26		14	25		15	26	ns
t_{PHL}	A,B,C or D	Any Output 3 gate delay		17	31		17	30		18	31	ns
t_{PLH}	A,B,C or D	Any output 2 gate delay		11	27		10	25		11	26	ns
t_{PLH}	A,B,C or D	Any output 3 gate delay		22	35		17	30		20	34	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ												
t_{PHL}	A,B,C or D	Any Output 2 gate delay		18	32		18	31		19	33	ns
t_{PHL}	A,B,C or D	Any Output 3 gate delay		21	35		22	35		23	36	ns
t_{PHL}	A,B,C or D	Any Output 2 gate delay		21	33		20	32		21	33	ns
t_{PLH}	A,B,C or D	Any Output 3 gate delay		29	36		25	38		28	40	ns

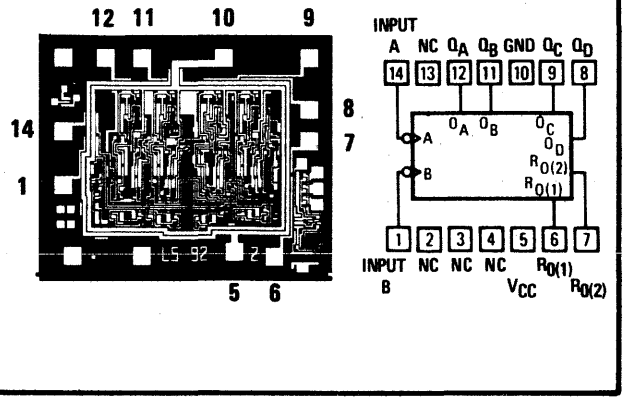
Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

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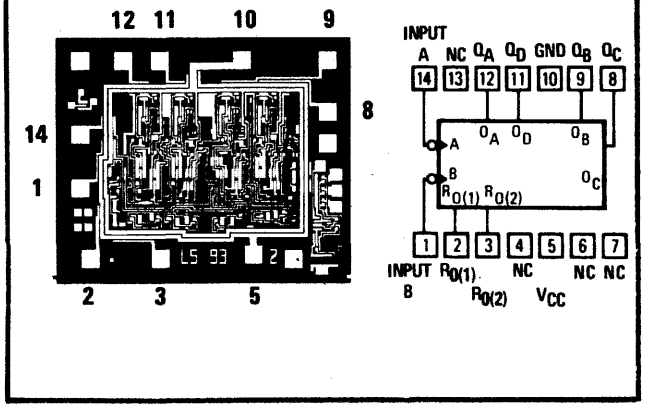
LS90
DECADE COUNTER



LS92



LS93
4-BIT BINARY COUNTER



Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Count frequency, f_{count} (see Figure 1 on 2-46)	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	15			15			
Reset inactive-state setup time, t_{setup}		25			25			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

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Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS90/92			9LS/74LS90/92			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=−400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max,	I_{OL}=4mA¶		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA¶					0.35	0.5	
I_I	Any reset	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
	A input	V_{CC}=MAX, V_I=5.5V				0.2			0.2	
	B input					0.4			0.4	
I_{IH}	Any reset	V_{CC}=MAX, V_I=2.7V				20			20	μA
	A input					40			40	
	B input					80			80	
I_{IL}	Any reset	V_{CC}=MAX, V_I=0.4V				−0.4			−0.4	mA
	A input					−2.4			−2.4	
	B input					−3.2			−3.2	
I_{OS}†		V_{CC}=MAX		−15		−100	−15		−100	mA
I_{CC}††		V_{CC}=MAX,	LS90		9	15		9	15	mA
			LS92		9	15		9	15	

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS93			9LS/74LS93			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=−400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA¶		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA¶					0.35	0.5	
I_I	Any reset	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
	A or B input	V_{CC}=MAX, V_I=5.5V				0.2			0.2	
I_{IH}	Any reset	V_{CC}=MAX, V_I=2.7V				20			20	μA
	A or B input					40			40	
I_{IL}	Any reset	V_{CC}=MAX, V_I=0.4V				−0.4			−0.4	mA
	A input					−2.4			−2.4	
	B input					−1.6			−1.6	
I_{OS}†		V_{CC}=MAX		−15		−100	−15		−100	mA
I_{CC}††		V_{CC}=MAX,			9	15		9	15	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

†† I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

¶ Outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

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Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter		From (input)	To (output)	−55°C			+25°C			+125°C			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ													
f_{max}	LS90	A	Q_A				32	42					MHz
		B	Q_B				16						
f_{max}	LS92	A	Q_A				32	42					MHz
		B	Q_B				16						
f_{max}	LS93	A	Q_A				32	42					MHz
		B	Q_B				16						
t_{PLH}	LS90	A	Q_A		13	20		10	16		13	20	ns
t_{PHL}					15	22		12	18		15	22	
t_{PLH}	LS92	A	Q_A		13	20		10	16		13	20	ns
t_{PHL}					15	22		12	18		15	22	
t_{PLH}	LS93	A	Q_A		13	20		10	16		13	20	ns
t_{PHL}					15	22		12	18		15	22	
t_{PLH}	LS90	A	Q_D		35	51		32	48		35	51	ns
t_{PHL}					37	56		34	50		37	56	
t_{PLH}	LS92	A	Q_D		35	54		32	48		35	54	ns
t_{PHL}					37	56		34	50		37	56	
t_{PLH}	LS93	A	Q_D		49	76		46	70		49	76	ns
t_{PHL}					49	76		46	70		49	76	
t_{PLH}	LS90	B	Q_B		13	20		10	16		13	20	ns
t_{PHL}					17	27		14	21		17	27	
t_{PLH}	LS92	B	Q_B		13	20		10	16		13	20	ns
t_{PHL}					17	27		14	21		17	27	
t_{PLH}	LS93	B	Q_B		13	20		10	16		13	20	ns
t_{PHL}					17	27		14	21		17	27	
t_{PLH}	LS90	B	Q_C		24	39		21	32		24	39	ns
t_{PHL}					27	42		23	35		27	42	
t_{PLH}	LS92	B	Q_C		13	20		10	16		13	20	ns
t_{PHL}					17	27		14	21		17	27	
t_{PLH}	LS93	B	Q_C		24	39		21	32		24	39	ns
t_{PHL}					27	41		23	35		27	41	
t_{PLH}	LS90	B	Q_D		24	39		21	32		24	39	ns
t_{PHL}					27	41		23	35		27	41	
t_{PLH}	LS92	B	Q_D		24	39		21	32		24	39	ns
t_{PHL}					27	41		23	35		27	41	
t_{PLH}	LS93	B	Q_D		38	57		34	51		38	57	ns
t_{PHL}					38	57		34	51		38	57	
t_{PHL}	LS90	Set-to-0	Any		30	47		26	40		30	47	ns
t_{PHL}	LS92	Set-to-0	Any		30	47		26	40		30	47	ns
t_{PHL}	LS93	Set-to-0	Any		30	47		26	40		30	47	ns
t_{PLH}	LS90	Set-to-9	Q_A, Q_D		24	35		20	30		24	35	ns
t_{PHL}			Q_B, Q_C		24	47		26	24		24	47	

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

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Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter		From (input)	To (output)	−55°C			+25°C			+125°C			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 50pF, R_L = 2kΩ													
t_{PLH}	LS90	A	Q_A		17	25		14	21		17	25	ns
t_{PHL}					19	27		16	23		19	27	
t_{PLH}	LS92	A	Q_A		17	25		14	21		17	25	ns
t_{PHL}					19	27		16	23		19	27	
t_{PLH}	LS93	A	Q_A		17	25		14	21		17	25	ns
t_{PHL}					19	27		16	23		19	27	
t_{PLH}	LS90	A	Q_D		39	56		36	52		39	56	ns
t_{PHL}					41	58		38	54		41	58	
t_{PLH}	LS92	A	Q_D		39	56		36	52		39	56	ns
t_{PHL}					41	58		38	54		41	58	
t_{PLH}	LS93	A	Q_D		53	82		50	78		53	82	ns
t_{PHL}					53	82		50	78		53	82	
t_{PLH}	LS90	B	Q_B		17	25		14	21		17	25	ns
t_{PHL}					19	27		16	23		19	27	
t_{PLH}	LS92	B	Q_B		17	25		14	21		17	25	ns
t_{PHL}					19	27		16	23		19	27	
t_{PLH}	LS93	B	Q_B		17	25		14	21		17	25	ns
t_{PHL}					41	27		16	23		19	27	
t_{PLH}	LS90	B	Q_C		29	41		26	37		29	41	ns
t_{PHL}					30	42		27	38		30	42	
t_{PLH}	LS92	B	Q_C		17	25		14	21		17	25	ns
t_{PHL}					19	27		16	23		19	27	
t_{PLH}	LS93	B	Q_C		29	41		26	37		29	41	ns
t_{PHL}					30	42		27	38		30	42	
t_{PLH}	LS90	B	Q_D		29	41		26	37		29	41	ns
t_{PHL}					30	42		27	38		30	42	
t_{PLH}	LS92	B	Q_D		29	41		26	37		29	41	ns
t_{PHL}					30	42		27	38		30	42	
t_{PLH}	LS93	B	Q_D		43	63		40	58		43	62	ns
t_{PHL}					43	62		40	58		43	62	
t_{PHL}	LS90	Set-to-0	Any		33	50		30	46		33	50	ns
t_{PHL}	LS92	Set-to-0	Any		33	50		30	46		33	50	ns
t_{PHL}	LS93	Set-to-0	Any		33	50		30	46		33	50	ns
t_{PLH}	LS90	Set-to-9	Q_A, Q_D		28	40		25	36		28	40	ns
t_{PHL}			Q_B, Q_C		33	49		30	45		33	49	

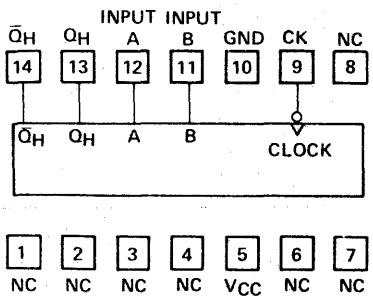
Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

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Shift Register — LS91, LS164

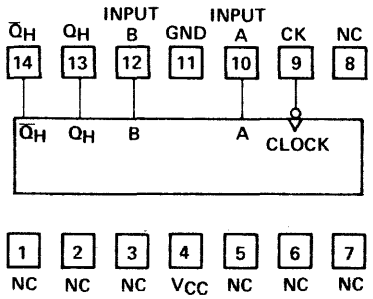
LS91
8-BIT SHIFT REGISTER

DUAL-IN-LINE PACKAGE



positive logic: see function table

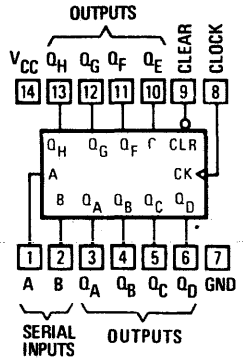
FLAT PACKAGE



positive logic: see function table

NC—No Internal Connection

LS164
8-BIT SHIFT REGISTER (SIPO)



Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			–400			–400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear input pulse, t_w	20			20			ns
Data setup time, t_{setup}	15			15			ns
Data hold time, t_{hold}	5			5			ns
Operating free-air temperature, T_A	–55		125	0		70	°C

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Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

Parameter	Test Conditions†		9LS/54LS			9LS/74LS			Unit
			Min.	Typ.‡	Max.	Min.	Typ.‡	Max.	
V_{IH} High-level input voltage			2			2			V
V_{IL} Low-level input voltage					0.7			0.8	V
V_{IK} Input clamp voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
V_{OH} High-level output voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = V_{IL} max, I_{OH} = −400μA		2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	V_{CC} = Min, V_{IH} = 2V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{IL} = V_{IL} max	I_{OL} = 8 mA					0.35	0.5	
I_I Input current at maximum input voltage	V_{CC} = Max, V_I = 7V				0.1			0.1	mA
I_{IH} High-level input current	V_{CC} = Max, V_I = 2.7V				20			20	μA
I_{IL} Low-level input current	V_{CC} = Max, V_I = 0.4V				−0.4			−0.4	mA
I_{OS} Short-circuit current∮	V_{CC} = Max		15		−100	15		−100	mA
I_{CC} Supply current	V_{CC} = Max, See Note 1			12	20		12	20	mA

†For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
∮Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 1. I_{CC} is measured after the eighth clock pulse with the output open and A and B inputs grounded.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=−400μA		2.5	3.5		2.7	3.5		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V,	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
	V_{IL}=V_{IL}max	I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				−0.4			−0.4	mA
I_{OS}†	V_{CC}=MAX		−15		−100	−15		−100	mA
I_{CC}††	V_{CC}=MAX			16	27		16	27	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4V, and a momentary ground, then 4.5V applied to clear.

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Switching Characteristics V_{CC} = 5.0V Over Recommended Free-Air Temperature Range.

Parameter	From (Input)	To (Output)	9LS/54LS									Unit
			−55°C			+25°C			+125°C			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2.0kΩ												
f(max)						10	18					MHz
T_{PLH}	clock	Q_H		26	42		24	40		26	42	ns
T_{PHL}	clock	Q_H		28	45		27	40		28	45	ns
Test Conditions: C_L = 50pF, R_L = 2.0kΩ												
T_{PLH}	clock	Q_H		30	47		27	45		30	47	ns
T_{PHL}	clock	Q_H		33	52		30	48		33	52	ns

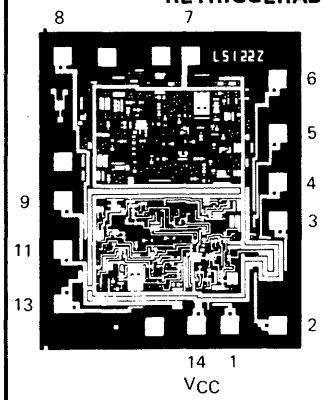
Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

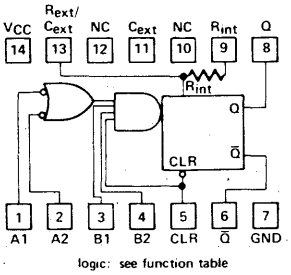
Parameter	−55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ										
f_{max}				25	36					MHz
t_{PHL}		26	38		24	36		26	38	ns
t_{PLH}		20	30		17	27		20	30	ns
t_{PHL}		24	35		21	32		24	35	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ										
t_{PHL}		29	42		27	40		29	42	ns
t_{PLH}		23	34		20	31		23	34	ns
t_{PHL}		27	39		24	36		27	39	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

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LS122
RETRIGGERABLE ONE-SHOT



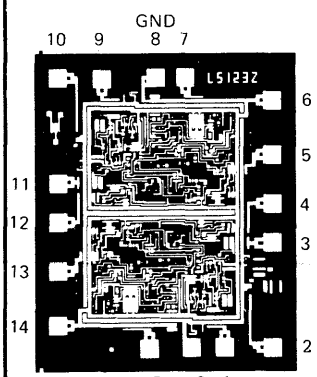


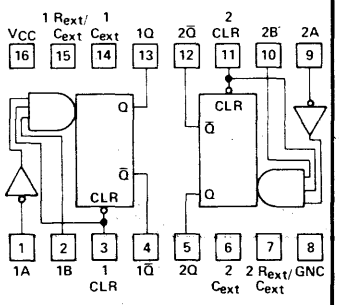
logic: see function table

NC–No internal connection.

Die Size .085 x .071

LS123
DUAL ONE-SHOT

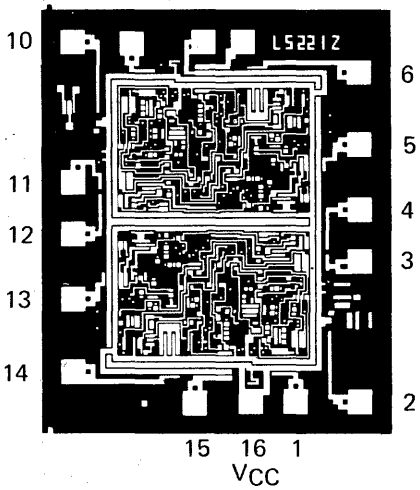


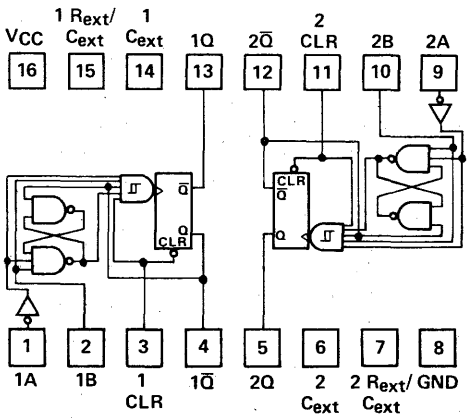


logic: see function table

Die Size .085 x .071

LS221 DUAL ONE-SHOT





Positive Logic: Low input to clear resets Q low and Q̄ high regardless of d-c levels at A or B inputs.

Die Size .085 x .071

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LS122, LS123
Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min.	Nom.	Max.	Min.	Nom.	Max.	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Pulse width, t_w	A or B inputs high	40			40			ns
	A or B inputs low	40			40			
	Clear low	40			40			
External timing resistance, R_{ext}		5		225	5		360	kΩ
External capacitance, C_{ext}		No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal				50			50	pF
Operating free-air temperature, T_A		−55		125	0		70	°C

LS221
Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min.	Nom.	Max.	Min.	Nom.	Max.	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt, B	1			1			V/s
	Logic input, A	1			1			V/μs
Input pulse width	A or B, $t_{w(in)}$	40			40			ns
	Clear, $t_{w(clear)}$	40			40			
Clear-inactive-state setup time, t_{setup}		15			15			ns
External timing resistance, R_{ext}		1.4		70	1.4		100	kΩ
External timing capacitance, C_{ext}		0		1000	0		1000	μF
Output duty cycle	R_T = 2 kΩ			67			67	%
	R_T = MAX R_{ext}			90			90	
Operating free-air temperature, T_A		−55		125	0		70	°C

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LS122, LS123

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions†			9LS/54LS			9LS/74LS			Unit
					Min.	Typ.‡	Max.	Min.	Typ.‡	Max.	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2V, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−30		−150	−30		−150	mA
I_{CC}	Supply current (quiescent or triggered)	V_{CC} = MAX,	See Note 2	'LS122		6	11		6	11	mA
				'LS123		12	20		12	20	

LS221

Parameter			Test Conditions†		9LS/54LS			9LS/74LS			Unit
					Min.	Typ.‡	Max.	Min.	Typ‡	Max.	
V_{T+}	Positive-going threshold voltage at A input		V_{CC} = MIN			1.0	2		1.0	2	V
V_{T-}	Negative-going threshold voltage at A input		V_{CC} = MIN		0.7	1.0		0.8	1.0		V
V_{T+}	Positive-going threshold voltage at B input		V_{CC} = MIN			1.0	2		1.0	2	V
V_{T-}	Negative-going threshold voltage at B input		V_{CC} = MIN		0.7	0.9		0.8	0.9		V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20			20	μA
I_{IL}	Low-level input current	Input A	V_{CC} = MAX, V_I = 0.4V				−0.36			−0.36	mA
		Input B					−0.44			−0.44	
		Clear					−0.54			−0.54	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−30		−100	−15		−100	mA
I_{CC}	Supply current		V_{CC} = MAX	Quiescent		4.7	11		4.7	11	mA
				Triggered		19	27		19	27	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5V, T_A = 25°C.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

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LS122, LS123

Switching Characteristics V_{CC} = 5.0V Over Recommended Free-Air Temperature Range.

Parameter	From (Input)	To (Output)	-55°C			+25°C			+125°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2.0k C_{ext} = 0pf, R_{ext} = 5.0kΩ												
t_{PLH}	A	Q		25	37		22	33		25	37	ns
	B			32	48		29	44		32	48	
t_{PHL}	A	$\overline{Q}$		33	49		30	45		33	49	ns
	B			40	61		37	56		40	61	
t_{PHL}	clear	Q		21	31		18	27		21	31	ns
t_{PLH}		$\overline{Q}$		33	50		30	45		33	50	ns
$tw_{Q(min)}$	A or B	Q		140	250		116	200		140	250	ns
*tw_Q	A or B	Q	—	—	—	4.0	4.5	5.0	—	—	—	μs
Test Conditions: C_L = 50pF, R_L = 2.0k, C_{ext} = 0pf, R_{ext} = 5.0kΩ												
t_{PLH}	A	Q		30	43		26	38		30	43	ns
	B			37	54		33	49		37	54	
t_{PHL}	A	$\overline{Q}$		38	55		34	50		38	55	ns
	B			45	67		41	62		45	67	
t_{PHL}	clear	Q		26	37		22	32		26	37	ns
t_{PLH}		$\overline{Q}$		39	55		35	50		39	55	ns
$tw_{Q(min)}$	A or B	Q		155	270		127	240		155	270	ns

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

*For this test R_{ext} = 10kΩ, C_{ext} = 1000pF.

LS221

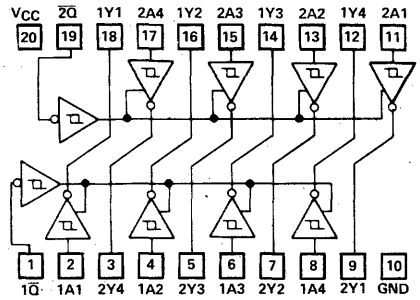
Switching Characteristics V_{CC} = 5.0V Over Recommended Free-Air Temperature Range.

Parameter	From (Input)	To (Output)	-55°C			+25°C			+125°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: R_L = 2.0k, C_L = 15pF, C_{ext} = 80pF, R_{ext} = 2.0kΩ												
$TW_{(out)}$	A or B	Q or $\overline{Q}$	77	138	175	70	120	150	77	138	175	ns
Test Conditions: R_L = 2.0k, C_L = 15pF, C_{ext} = 0, R_{ext} = 2.0kΩ												
$TW_{(out)}$	A or B	Q or $\overline{Q}$	22	50	80	20	47	70	22	50	80	ns
Test Conditions: R_L = 2.0k, C_L = 15pF, C_{ext} = 100pF, R_{ext} = 10kΩ												
$TW_{(out)}$	A or B	Q or $\overline{Q}$	600	725	870	600	670	750	620	750	870	ns
Test Conditions: R_L = 2.0k, C_L = 15pF, C_{ext} = 1pF, R_{ext} = 10kΩ												
$TW_{(out)}$	A or B	Q or $\overline{Q}$	6.0	7.7	8.5	6.0	6.7	7.5	6.0	7.7	8.5	ms
Test Conditions: R_L = 2.0k, C_L = 15pF, C_{ext} = 80pF, R_{ext} = 2.0kΩ												
t_{PLH}	A	Q		48	74		45	70		48	74	ns
	B			38	59		35	55		38	59	
t_{PHL}	A	$\overline{Q}$		53	84		50	80		53	84	ns
	B			43	69		40	65		43	69	
t_{PHL}	Clear	Q		38	59		35	55		38	59	ns
t_{PLH}	Clear	$\overline{Q}$		47	69		44	65		47	69	ns

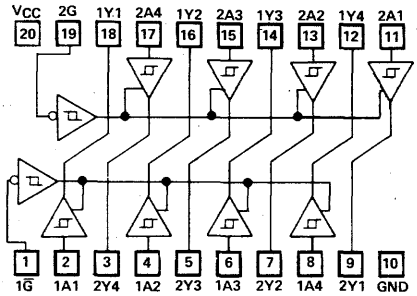
Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

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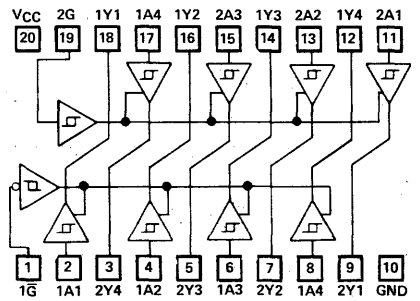
LS240
OCTAL INVERTING BUS DRIVER



LS244
TRI-STATE OCTAL BUS DRIVER



LS241
OCTAL NON-INVERTING BUS DRIVER



Recommended Operating Conditions

PARAMETER	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-12			-15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Note 1: Voltage values are with respect to network ground terminal.

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Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_{IK}		V_{CC} = MIN, I_I = -18 mA				-1.5			-1.5	V
Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = MAX		2.4	3.4		2.4	3.4		V
		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.5V, I_{OH} = MAX		2			2			
V_{OL}		V_{CC} = MIN, V_{IH} = 2V,	I_{OL} = 12 mA			0.4			0.4	V
		V_{IL} = V_{IL}max	I_{OL} = 24 mA						0.5	
I_{OZH}		V_{CC} = MAX, V_{IH} = 2V, V_{IL} = V_{IL}max	V_O = 2.7V			20			20	μA
I_{OZL}		V_{CC} = MAX, H_{IH} = 2V, V_{IL} = V_{IL}max	V_O = 0.4V			-20			-20	μA
I_I		V_{CC} = MAX, V_I = 7V				0.1			0.1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7V				20			20	μA
I_{IL}		V_{CC} = MAX, V_{IL} = 0.4V				-0.2			-0.2	mA
I_{OS}		V_{CC} = MAX		-50		-225	-50		-275	mA
I_{CC}	Outputs high	V_{CC} = MAX, Outputs open	All		13	23		13	23	mA
	Outputs low		'LS240		26	44		26	44	
			'LS241, 'LS244		27	46		27	46	
	All outputs disabled		'LS240		29	50		29	50	
			'LS241, 'LS244		32	54		32	54	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

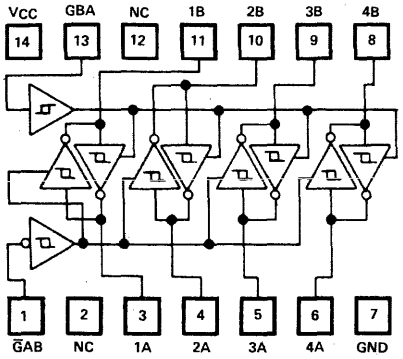
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Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

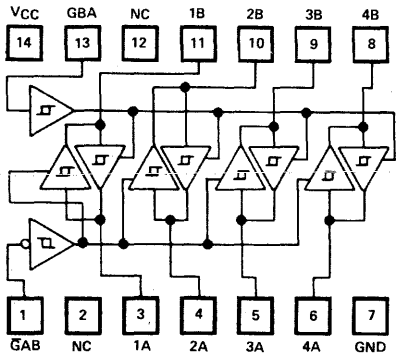
Parameter	LS240			LS241 LS244			Unit
	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 45 pF, R_L = 667Ω							
t_{PLH}		9	14		12	18	ns
t_{PHL}		12	18		12	18	ns
t_{PZL}		20	30		20	30	ns
t_{PZH}		15	23		15	23	ns
Test Conditions: C_L = 5 pF, R_L = 667Ω							
t_{PLZ}		15	25		15	25	ns
t_{PHZ}		10	18		10	18	ns

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LS242
QUAD BUS TRANSCEIVER



LS243
QUAD BUS TRANSCEIVER



Recommended Operating Conditions

PARAMETER	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-12			-15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Note: Voltage values are with respect to network ground terminal.

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Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_{IK}		V_{CC} = MIN, I_I = -18 mA				-1.5			-1.5	V
Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = V_{IL}max, I_{OH} = -3 mA		2.4	3.1		2.4	3.1		V
		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.5V, I_{OH} = MAX		2			2			
V_{OL}		V_{CC} = MIN, V_{IH} = 2V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{IL} = V_{IL}max	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = MAX, V_{IH} = 2V, V_{IL} = V_{IL}max	V_O = 2.7V			20			20	μA
I_{OZL}		V_{CC} = MAX, V_{IH} = 2V, V_{IL} = V_{IL}max	V_O = 0.4V			-200			-200	μA
I_I		V_{CC} = MAX, V_I = 7V				0.1			0.1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7V				20			20	μA
I_{IL}	A inputs	V_{CC} = MAX, V_I = 0.4V, GAB and GBA at V_{IL}max				-0.2			-0.2	mA
	B inputs	V_{CC} = MAX, V_I = 0.4V, GAB and GBA at 2V				-0.2			-0.2	
	GAB and GBA	V_{CC} = MAX, V_I = 0.4V				-0.2			-0.2	
I_{OS}†		V_{CC} = MAX		-50		-225	-50		-225	mA
I_{CC}	Outputs high	V	LS242, LS243		22	38		22	38	mA
	Outputs low	V_{CC} = MAX, Outputs open,	LS242, LS243		29	50		29	50	
	All outputs disabled	See Note 2	LS242		29	50		29	50	
			LS243		32	54		32	54	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
NOTE 1:

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	LS242			LS243			Unit
	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 45 pF, R_L = 667Ω							
t_{PLH}		9	14		12	18	ns
t_{PHL}		12	18		12	18	ns
t_{PZL}		20	30		20	30	ns
t_{PZH}		15	23		15	23	ns
Test Conditions: C_L = 5 pF, R_L = 667Ω							
t_{PLZ}		15	25		15	25	ns
t_{PHZ}		10	18		10	18	ns

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Binary Multiplier — LS261

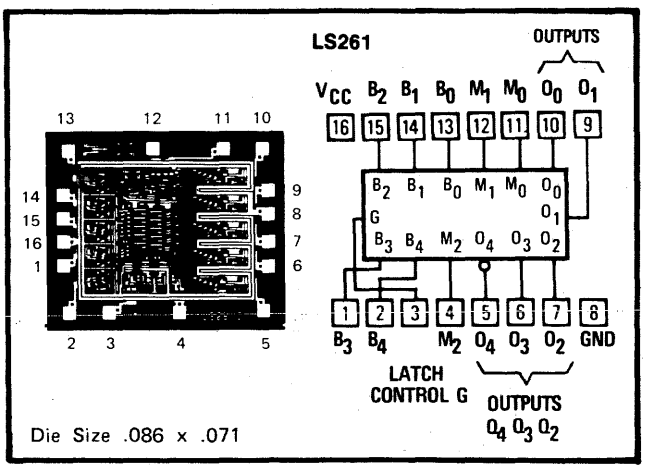
FUNCTION TABLE

INPUTS				OUTPUTS				
LATCH CONTROL G	MULTIPLIER M2	M1	M0	$\bar{Q}4$	Q3	Q2	Q1	Q0
L	X	X	X	$Q4_0$	$Q3_0$	$Q2_0$	$Q1_0$	$Q0_0$
H	L	L	L	H	L	L	L	L
H	L	L	H	$\bar{B}4$	B4	B3	B2	B1
H	L	H	L	$\bar{B}4$	B4	B3	B2	B1
H	L	H	H	$\bar{B}4$	B3	B2	B1	B0
H	H	L	L	B4	$\bar{B}3$	$\bar{B}2$	$\bar{B}1$	$\bar{B}0$
H	H	L	H	B4	$\bar{B}4$	$\bar{B}3$	$\bar{B}2$	$\bar{B}1$
H	H	H	L	B4	$\bar{B}4$	$\bar{B}3$	$\bar{B}2$	$\bar{B}1$
H	H	H	H	H	L	L	L	L

H = high level, L = low level, X = irrelevant

$\bar{Q}4_0 \ldots Q0_0$ = The logic level of the same output before the high-to-low transition of G.

B4 . . . B0 = The logic level of the indicated multiplicand (B) input



Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−1	mA
Low-level output current, I_{OL}				4			8	mA
Width of enable pulse, t_w		25			25			ns
Setup time, t_{setup}	Any M input	17↓			17↓			ns
	Any B input	15↓			15↓			
Hold time, t_{hold}	Any M input	0↓			0↓			ns
	Any B input	0↓			0↓			
Operating free-air temperature, T_A		−55		125	0		70	°C

↓The arrow indicates that the falling edge of the enable pulse is used for reference.

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Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.2	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-1mA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}	V_{CC}=MAX, All inputs at 0V, Outputs open			22	38		22	40	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

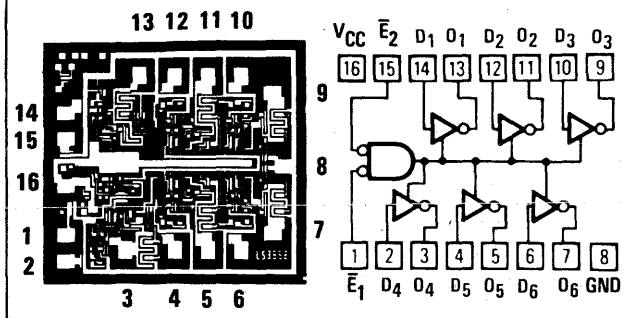
Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (input)	To (output)	−55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ												
t_{PLH}	Enable G	Any Q		25	39		22	35		25	39	ns
t_{PHL}				23	34		20	30		23	34	
t_{PLH}	Any M input	Any Q		28	44		25	40		28	44	ns
t_{PHL}				25	39		22	35		25	39	
t_{PLH}	Any B input	Any Q		30	46		27	42		30	46	ns
t_{PHL}				27	41		24	37		27	41	
Test Conditions: C_L = 50pF, R_L = 2kΩ												
t_{PLH}	Enable G	Any Q		30	44		26	40		30	44	ns
t_{PHL}				28	39		24	35		28	39	
t_{PLH}	Any M input	Any Q		33	49		29	45		33	49	ns
t_{PHL}				30	44		26	40		30	44	
t_{PLH}	Any B input	Any Q		35	51		31	47		35	51	ns
t_{PHL}				32	46		28	42		32	46	

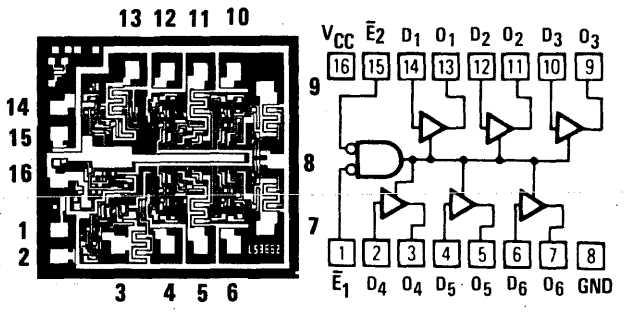
Note: AC specification shown under −55°C and +125°C are for 9LS devices only.
All 50pF specifications are for 9LS only.

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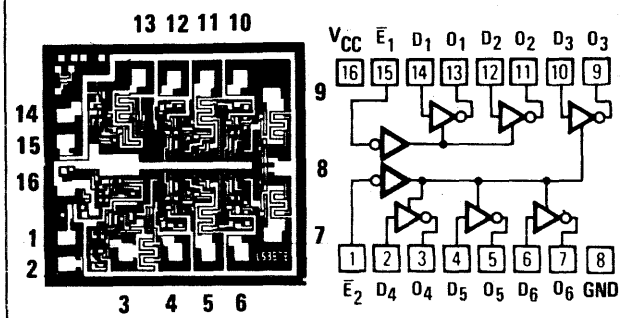
LS365
HEX 3-STATE BUFFER WITH COMMON 2-INPUT NOR ENABLE



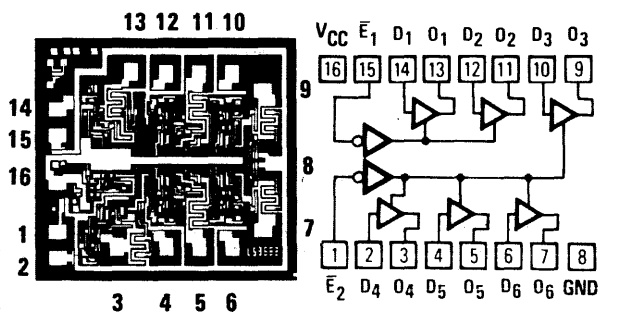
LS366
HEX 3-STATE INVERTER BUFFER WITH COMMON 2-INPUT NOR ENABLE



LS367
HEX 3-STATE BUFFER SEPARATE 2-BIT AND 4-BIT SECTIONS



LS368
HEX 3-STATE INVERTER BUFFER SEPARATE 2-BIT AND 4-BIT SECTIONS



Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-Level Output Current, I_{OH}			-1			-2.6	mA
Low-Level Output Current, I_{OL}			12			24	mA
Operating Free-Air Temperature, T_A	-55		125	0		75	°C

TRUTH TABLES

LS365

INPUTS			OUTPUTS
$\overline{E}_1$	$\overline{E}_2$	D	
L	L	L	L
L	L	H	H
H	X	X	(Z)
X	H	X	(Z)

LS366

INPUTS			OUTPUTS
$\overline{E}_1$	$\overline{E}_2$	D	
L	L	L	H
L	L	H	L
H	X	X	(Z)
X	H	X	(Z)

LS367

INPUTS		OUTPUTS
$\overline{E}$	D	
L	L	L
L	H	H
H	X	(Z)

LS368

INPUTS		OUTPUTS
$\overline{E}$	D	
L	L	H
L	H	L
H	X	(Z)

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Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}	Guaranteed Input HIGH Voltage for All Inputs		2.0			2.0			V
V_{IL}	Guaranteed Input LOW Voltage for All Inputs				.7	2.0		.8	V
V_{CD}	V_{CC}=MIN, I_{IN}=−18mA			−0.65	−1.5		−0.65	−1.5	V
V_{OH}	V_{CC}=MIN, V_{IN}=V_{IH} or V_{IL} per Truth Table	I_{OH}=−1.0mA	2.4	3.4					V
		I_{OH}=−2.6mA				2.4	3.1		
V_{OL}	V_{CC}=MIN, V_{IN}=V_{IH} or V_{IL} per Truth Table	I_{OL}=12mA		0.25	0.4		0.25	0.40	V
		I_{OL}=24mA					0.35	0.5	
I_{OZH}	V_{CC}=MAX, V_{out}=2.4V, $V_{\overline{E}}$=2.0V				20			20	μA
I_{OZL}	V_{CC}=MAX, V_{out}=0.4V, $V_{\overline{E}}$=2.0V				−20			−20	μA
I_{IH}	V_{CC}=MAX, V_{IN}=2.7V				20			20	μA
	V_{CC}=MAX, V_{IN}=7.0V				−.1			−.1	mA
I_{IL}	V_{CC}=MAX, V_{IN}=0.4V				−0.4			−0.4	mA
I_{OS}†	V_{CC}=MAX, V_{OUT}=0V		−30		−100	−30		−100	mA
I_{CC}	V_{CC}=MAX, V_{IN}=0V, $V_{\overline{E}}$=4.5V	LS365/367		13.5	24		13.5	24	mA
		LS366/368		11.8	21		11.8	21	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

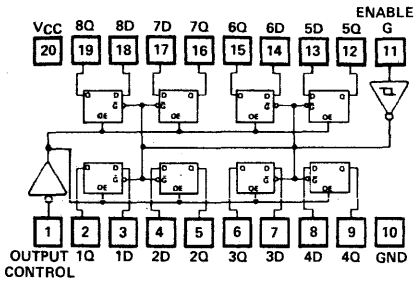
Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (Input)	To (Output)	−55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 45pF												
t_{PLH} (LS365/367)	D_i	O_i		9	14		7	10		9	14	ns
t_{PHL} (LS365/367)				12	20		10	16		12	20	
t_{PLH} (LS366/368)	D_i	O_i		9	14		7	10		9	14	ns
t_{PHL} (LS366/368)				12	20		10	16		12	20	
t_{ZH}	$\overline{E}$	O_i		12	20		10	16		12	20	ns
t_{ZL}				20	36		18	30		20	36	
Test Conditions: C_L = 5pF, R_L = 667Ω												
t_{LZ}	$\overline{E}$	O_i		12	20		10	15		12	20	ns
t_{HZ}				19	27		17	23		19	27	
Test Conditions: C_L = 125pF,												
t_{PLH} (LS365/367)	D_i	O_i		12	20		10	15		12	20	ns
t_{PHL} (LS365/367)				15	26		15	21		15	26	
t_{PLH} (LS366/368)	D_i	O_i		12	20		10	15		12	20	ns
t_{PHL} (LS366/368)				15	26		15	21		15	20	
t_{ZH}	$\overline{E}$	O		16	26		13	20		16	26	ns
t_{ZL}				24	42		21	35		24	40	

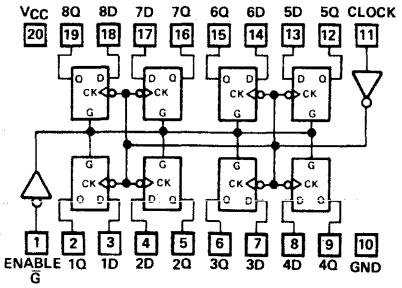
Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

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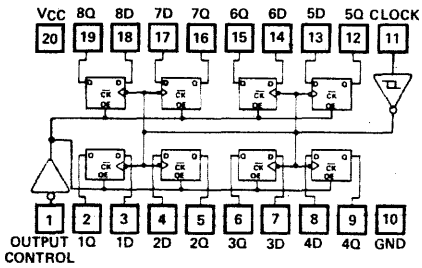
LS373
OCTAL TRANSPARENT LATCH



LS377
OCTAL D FLIP-FLOP WITH ENABLE



LS374
OCTAL D FLIP-FLOP



Recommended Operating Conditions (LS373, LS374)

PARAMETER		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				-1			-2.6	mA
Width of clock/enable pulse, t_w	High	15			15			ns
	Low	15			15			
Data setup time, t_{su}	LS373	0↓			0↓			ns
	LS374	20↑			20↑			
Data hold time, t_h	LS373	10↓			10↓			ns
	LS374	0↑			0↑			
Operating free-air temperature, T_A		-55		125	0		70	°C

↑↓ The arrow indicates the transistion of the clock/enable input used for reference:
↑ for the low-to-high transition,
↓ for the high-to-low transition.

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Recommended Operating Conditions (LS377)

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-400			-400	μA
Low-level output current, I_{OH}				4			8	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{su}	Data input	20↑			20↑			ns
	Enable active-state	25↑			25↑			
	Enable inactive-state	10↑			10↑			
Hold time, t_h		5↑			5↑			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

↑ The arrow indicates that the rising edge of the clock pulse is used for reference.

LS373, LS374

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_{IK}	V_{CC} = MIN, I_I = -18 mA				-1.5			-1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = V_{IL}max, I_{OH} = MAX		2.4	3.4		2.4	3.1		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = MAX, V_{IH} = 2V, V_O = 2.7V				20			20	μA
I_{OZL}	V_{CC} = MAX, V_{IH} = 2V, V_O = 0.4V				-20			-20	μA
I_I	V_{CC} = MAX, V_I = 7V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7V				20			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4V				-0.4			-0.4	mA
I_{OS}	V_{CC} = MAX		-30		-130	-30		-130	mA
I_{CC}	V_{CC} = MAX, Output control at 4.5V	LS373		24	40		24	40	mA
		LS374		27	45		27	45	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
NOTE 1:

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Electrical Characteristics Over Recommended Free-Air Temperature Range LS373, LS374

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_{IK}	V_{CC} = MIN, I_I = -18 mA				-1.5			-1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = V_{IL}max, I_{OH} = -400μA		2.5	3.5		2.7	3.5		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = MAX, V_I = 7V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7V				20			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4V				-0.4			-0.4	mA
I_{OS}	V_{CC} = MAX		-20		-100	-20		-100	mA
I_{CC}	V_{CC} = MAX			17	28		17	28	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

LS377
Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

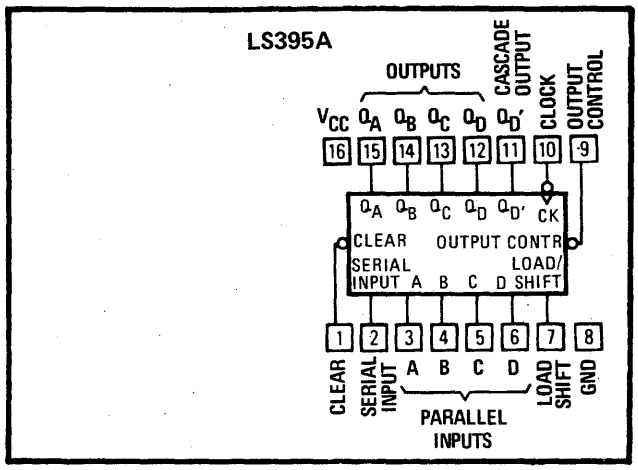
Parameter	From (Input)	To (Output)	LS373			LS374			Unit
			Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 45 pF, R_L = 667Ω (see Note 1)									
f_{max}						35	50		MHz
t_{PLH}	Data	Any Q		10	18				ns
t_{PHL}				18	27				
t_{PLH}	Clock or enable	Any Q		14	25		16	28	ns
t_{PHL}				24	36		22	34	
t_{PZH}	Output Control	Any Q		16	28		16	28	ns
t_{PZL}				22	36		22	36	
Test Conditions: C_L = 5 pF, R_L = 667Ω									
t_{PHZ}	Output Control	Any Q		12	20		10	18	ns
t_{PLZ}				16	25		14	24	

Note 1: Maximum clock frequency is tested with all outputs loaded.

LS377
Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	LS377			Unit
	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ				
t_{max}	30	40		MHz
t_{PLH}		17	27	ns
t_{PHL}		18	27	ns

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FUNCTION TABLE

INPUTS					3-STATE OUTPUTS				CASCADE OUTPUT
CLEAR	LOAD/SHIFT CONTROL	CLOCK	SERIAL	PARALLEL A B C D	Q_A	Q_B	Q_C	Q_D	Q_D
L	X	X	X	X X X X	L	L	L	L	L
H	H	H	X	X X X X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	H	↓	X	a b c d	a	b	c	d	d
H	L	H	X	X X X X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	L	↓	H	X X X X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	L	↓	L	X X X X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}

When the output control is high, the 3-state outputs are disabled to the high-impedance state; however, sequential operation of the registers and the output at Q_D are not affected.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent ↓ transition of the clock.

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-2.6	mA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$	25			25			ns
Setup time, high-level or low-level data, t_{setup}	20			20			ns
Hold time, high-level or low-level data, t_{hold}	10			10			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

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Tri-State Shift Register — LS395A

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*			9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I	V_{CC}=MIN,	I_I=−18mA				−1.5			−1.5	V
V_{OH}	V_{CC}=MIN, V_{IL}=V_{IL}max,	V_{IH}=2V, I_{OH}=MAX		2.4	3.4		2.4	3.1		V
V_{OL}	V_{CC}=MIN V_{IL}=V_{IL} max, V_{IH}=2V	Q_A, Q_B Q_C, Q_D	I_{OL}=12mA		0.25	0.4		0.25	0.40	V
			I_{OC}=24mA					0.35	0.50	
		Q_D	I_{OL}=4mA		0.25	0.4		0.25	0.40	V
			I_{OL}=8mA					0.35	0.50	
I_{OZH}	V_{CC}=MAX, V_O=2.7V	V_{IH}=2V,	Q_A, Q_B Q_C, Q_D			20			20	μA
I_{OZL}	V_{CC}=MAX, V_O=0.4V	V_{IH}=2V,	Q_A, Q_B Q_C, Q_D			−20			−20	μA
I_I	V_{CC}=MAX,	V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX,	V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX,	V_I=0.4V				−0.4			−0.4	mA
I_{OS}†	V_{CC}=MAX			−15		−100	−15		−100	mA
I_{CC}††	V_{CC}=MAX,		Condition A		18	29		18	29	mA
			Condition B		15	25		15	25	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

††I_{CC} is measured with the outputs open, the serial input and mode control at 4.5V, and the data inputs grounded under the following conditions: A. Output control at 4.5V and a momentary 3V, then ground, applied to clock input.
B. Output control and clock input grounded.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameters	−55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ										
f_{max}				25	35					MHz
t_{PHL} Clear to output		27	40		23	35		27	40	ns
t_{PLH}		27	40		23	35		27	40	ns
t_{PHL}		24	35		20	30		24	35	ns
t_{PZH}		17	25		13	20		17	25	ns
t_{PZL}		28	41		24	36		28	41	ns
t_{PHZ}		15	22		11	17		15	22	ns
t_{PLZ}		19	27		15	23		19	27	ns
Test Conditions: C_L = 5.0pF, R_L = 2kΩ										
t_{HZ}		13	22		11	17		13	22	ns
t_{LZ}		18	27		15	23		18	27	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ										
t_{PHL}		30	44		26	39		30	44	ns
t_{PLH}		30	44		26	39		30	44	ns
t_{PHL}		27	38		23	34		27	38	ns
t_{PZH}		20	29		18	24		22	27	ns
t_{PZL}		31	45		27	40		30	45	ns
t_{PHZ}		18	26		14	20		19	26	ns
t_{PLZ}		22	32		18	27		22	32	ns

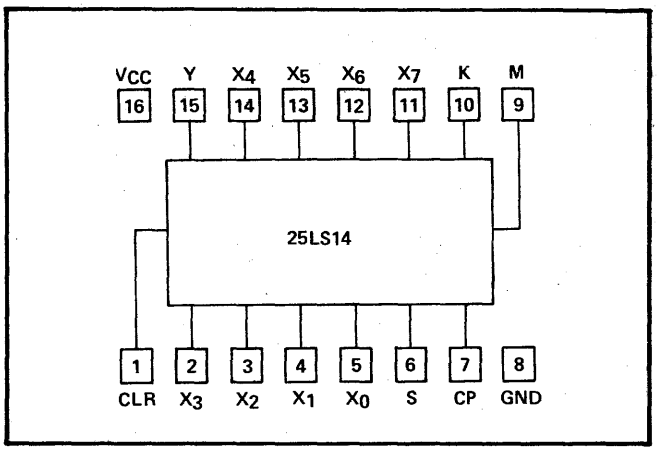
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Note: AC specification shown under −55°C and +125°C are for 9LS devices only.
All 50pF specifications are for 9LS devices only.

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FEATURES

- Two's Complement Multiplication Without Correction
- Magnitude Only Multiplication
- Cascadable for any Number of Bits
- 8-Bit Parallel Multiplicand Data Input
- Serial Multiplier Data Input
- Serial Data Output for Multiplication Product
- 25 MHz Minimum Clock Frequency
- 100% Reliability Assurance Testing in Compliance With MIL-STD-883



FUNCTIONAL DESCRIPTION

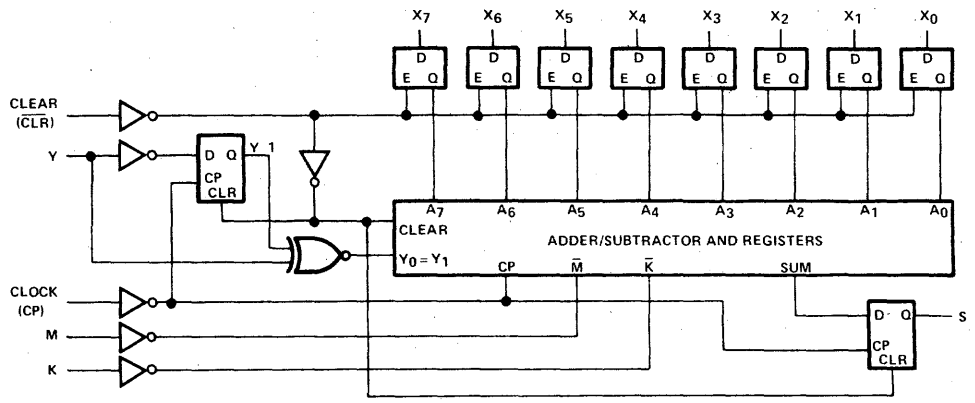
The 25LS14 is an 8-bit by 1-bit sequential logic element that performs digital multiplication of two numbers represented in two's complement form to produce a two's complement product without correction by using Booth's algorithm internally. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. The X latches are controlled via the clear input. When the clear input is LOW, all internal flip-flops are cleared and the X latches are opened to accept new multiplicand data. When the clear input is HIGH, the latches are closed and are insensitive to X input changes.

The multiplier word data is passed by the Y input in a serial bit stream—least significant bit first. The product is clocked out the S output least significant bit first.

The multiplication of an m-bit multiplicand by an n-bit multiplier results in an m + n bit product. The 25LS14 must be clocked for m + n clock cycles to produce this two's complement product. Likewise, the n-bit multiplier (Y-input) sign bit data must be extended for the remaining m-bits to complete the multiplication cycle.

The device also contains a K input so that devices can be cascaded for longer length X words. The sum (S) output of one device is connected to the K input of the succeeding device when cascading. Likewise, a mode input (M) is used to indicate which device contains the most significant bit. The mode input is wired HIGH or LOW depending on the position of the 8-bit slice in the total X word length.

LOGIC DIAGRAM



Recommended Operating Conditions

	Military			Commercial			Units
	Min.	Nom	Max.	Min.	Nom.	Max.	
Supply Voltage, V_{CC}	4.75	5	5.25	4.5	5	5.5	V
High-level Output Current, I_{OH}			−1			−1	mA
Low-level Output Current, I_{OL}		8	12		8	12	mA
Operating Free-Air Temperature, T_A	−55		125	0		70	°C

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8-Bit Serial/Parallel Two's Complement Multiplier 25LS14

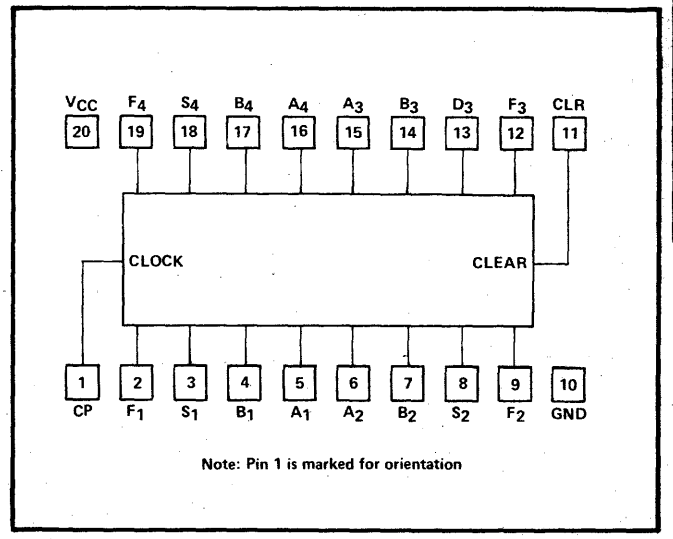
Electrical Characteristics Over Operating Temperature Range (Unless Otherwise Noted)

Parameters		Test Conditions (Note 1)		Military			Commercial			Units
				Min.	Typ. (2)	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = 1.0mA V_{IN} = V_{IH} or V_{IL}		2.5	3.4		2.7	3.4		V
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0mA			0.4			0.40	V
			I_{OL} = 12mA			0.45			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2			−1.2	V
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	X, M			−0.48			−0.48	mA
			K' $\overline{CLR}$			−1.2			−1.2	
			CP			−1.6			−1.6	
			Y			−3.2			−3.2	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	X, M			20			20	µA
			K, $\overline{CLR}$			30			30	
			CP			40			40	
			Y			80			80	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0			1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.		−40		−100	−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			91	155		91	155	mA

Switching Characteristics, V_{cc} = 5V

Parameter	From (Input)	To (Output)	+25°C			Units
			Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2kΩ						
t_{PLH}	Clock	Y		13	20	ns
t_{PHL}	Clock	Y		13	20	ns
t_{PHL}	Clear	X		17	25	ns
t_s	Set up time	Y to Clock	32			ns
t_h	Hold time		0			ns
t_s	Set up time	K to Clock	18			ns
t_h	Hold time		0			ns
t_s	Set up time	Xi to Clear	13			ns
t_h	Hold time		0			ns
t_{pw}	Clock Pulse Width	Clock Hi	15			ns
		Clock Low	15			ns
t_{pw}	Clear Pulse Width		20			ns
t_s	Clear Recovery Time		18			ns
f_{max}	Max. Clock Frequency		25	40		MHz

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Note: Pin 1 is marked for orientation

Recommended Operating Conditions

	Military			Commercial			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5.0	5.25	V
High-Level Output Current I_{OH}			–440			–440	μA
Low Level Output Current I_{OL}			8			8	mA
Operating Free Air Temperature	–55		+125	0		+70	°C

Electrical characteristics Over Operating Temperature Range (Unless Otherwise Noted)

Parameters	Description	Test Conditions (Note 1)		Military Min.	Military Typ. (Note 2)	Military Max.	Commercial Min.	Commercial Typ.	Commercial Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = –440μA V_{IN} = V_{IH} or V_{IL}		2.5			2.7			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4			0.4	Volts
			I_{OL} = 8.0mA			0.45			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.7			0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = –18mA				1.5			1.5	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				–0.36			–0.36	Volts
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20			20	Volts
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V				0.1			0.1	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.		–30		–85	–30		–85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.			48	75		48	75	mA

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Input Load Current x Input Load Factor (See Loading Rultes).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. All inputs HIGH, measured after a LOW-to-HIGH clock transition.

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Quad Serial Adder/Subtractor 25LS15

Switch Characteristics V_{CC} = 5.0V, T_A = +25°C

Parameters	From (Input)	To (Output)		+25°C Min.	+25°C Typ.	+25°C Max.	Units
Test Conditions: C_L = 15pF, R_L = 2kΩ							
t_{PLH}	Clock	F			14	22	ns
t_{PHL}					14	22	
t_{PHL}	Clear	F			20	30	ns
t_s	Set up time	A, B, S		10			ns
t_h	Hold time			0			
t_s	Clear Recovery time			25			ns
t_h	Clear Hold time			0			
t_{pw}	Clock Pulse Width	Clock	HIGH	17			ns
			LOW	17			
t_{pw}	Clear Pulse Width			20			ns
f_{MAX}	Max. Clock Frequency			30	40		MHz

FUNCTION TABLE

External Inputs					Internal Point		Output	
CP	CLR	S	A	B	C	C_1	F	Function
X	L	L	X	X	L	L	L	Clear
X	L	H	X	X	H	H	L	
L	H	X	X	X	NC	NC	NC	
H	H	X	X	X	NC	NC	NC	
↑	H	L	L	L	L	L	L	Add
↑	H	L	L	L	H	L	H	
↑	H	L	L	H	L	L	H	
↑	H	L	L	H	H	H	L	
↑	H	L	H	L	L	L	H	
↑	H	L	H	L	H	H	L	
↑	H	L	H	H	L	H	L	
↑	H	L	H	H	H	H	H	
↑	H	H	L	L	L	L	H	Subtract
↑	H	H	L	L	H	H	L	
↑	H	H	L	H	L	L	L	
↑	H	H	L	H	H	L	H	
↑	H	H	H	L	L	H	L	
↑	H	H	H	L	H	H	H	
↑	H	H	H	H	L	L	H	
↑	H	H	H	H	H	H	L	

C = Data In the Carry Flip-Flop Before the Clock Transition
C_1 = Data In the Carry Flip-Flop After the Clock
X = Don't Care
NC = No Change
H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition

DEFINITION OF FUNCTIONAL TERMS

A_1,A_2,A_3,A_4 The "A" input into each adder/subtractor

B_1,B_2,B_3,B_4 The "B" input into each adder/subtractor

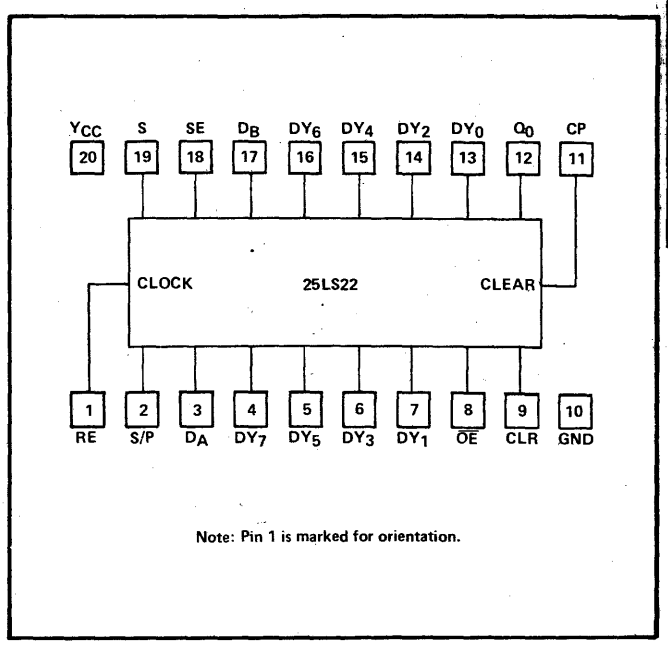
S_1,S_2,S_3,S_4 The add subtract control for each adder/subtractor. When S is LOW, the F function is A+B. When S is HIGH, the F function is A–B.

F_1,F_2,F_3,F_4 The four independent serial outputs of the adder/subtractor.

CP Clock The clock input for the device. All internal flip-flops change state on the LOW-to-HIGH transition.

CLR Clear When the clear input is LOW, the four independent adder/subtractors are asynchronously reset. The sum flip-flop is always set to logic "0". The carry flip-flop is set to logic "0" in the add mode and logic "1" in the subtract mode.

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Note: Pin 1 is marked for orientation.

Recommended Operating Conditions

		Military			Commercial			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	V
High Level Output Current I_{OH}	Q_0			-0.44			-0.44	mA
	D_{Yi}			-1.0			-2.6	
Low Level Output Current I_{OL}			4	8		4	8	mA
Operating Free Air Temperature		-55		+125	0		70	°C

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Electrical Characteristics Over Operating Temp. Range (Unless Otherwise Noted)

	Description	Test Conditions (Note 1)		Military			Commercial			Unit
				Min.	Typ. (2)	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Q_0, I_{OH} = −440μA	2.5			2.7			V
			DY_i, I_{OH} = −1.0mA	2.4			2.4			
			DY_i, I_{OH} = −2.6mA	2.4			2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4			0.4	V
			I_{OL} = 8.0mA			0.45			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.7			0.8	V
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5			−1.5	V
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	$\overline{SE}$			−1.08			−1.08	mA
			S			−0.72			−0.72	
			Others			−0.36			−0.36	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V (Except DY_i)	$\overline{SE}$			60			60	μA
			S			40			40	
			Others			20			20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V (Except DY_i)	SE			0.3			0.3	mA
			S			0.2			0.2	
			Others			0.1			0.1	
I_O	Off State (High Impedance) Output Current (DY_i)	V_{CC} = MAX.	V_O = 2.4V			40			40	μA
			V_O = 0.4V			−100			−100	
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.		−30		−85	−30		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			40	65		40	65	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

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Switching Characteristics V_{CC} = 5V, T_A = +25°C

Parameters	From (Input)	To (Output)	+25°C Min.	+25°C Typ.	+25°C Max.	Units
Test Conditions: C_L = 50pF, R_L = 2kΩ						
t_{PLH}	Clock	DY_i		16.5	24	ns
t_{PHL}				18	26	
t_{PHL}	Clear	DY_i		23	30	ns
t_{PLH}	Clock	Q_0		16.5	24	ns
t_{PHL}				18	26	
t_{PHL}	Clear	Q_0		23	30	ns
Test Conditions: C_L = 15pF, R_L = 2kΩ						
t_{ZH}	$\overline{OE}$	DY_i		13	21	ns
t_{ZL}				18	26	
t_{HZ}				13	21	
t_{LZ}				18	26	
t_{ZH}	SER/PAR	DY_i		18	26	ns
t_{ZL}				23	32	
t_{HZ}				18	26	
t_{LZ}				23	32	
t_s	Set Up Time RE To Clock		20			ns
t_s	Set Up Time SE To Clock		10			
t_s	Set Up Time S To Clock		15			
t_s	Set Up Time DA/DB to Clock		15			
t_s	Set Up Time DY_i To Clock		15			
t_s	Clear to Recovery To Clock		8.0			
t_s	Set Up Time S/P To Clock		15			ns
t_h	Hold Time Any Input		0			
t_h	Clear Hold Time		0			ns
t_{pw}	Clock Pulse Width	HIGH	8.0			ns
		LOW	8.0			
t_{pw}	Clear Pulse Width		20			ns
f_{max}	Max. Clock Frequency		50	70		MHz

FUNCTION TABLE

Mode	INPUTS Clear	Register Enable	Serial/ Parallel	Sign Extend	Mux Select	$\overline{OE}$*	Clock	OUTPUTS DY_7	DY_6	DY_5	DY_4	DY_3	DY_2	DY_1	DY_0	Q_0
Clear	L	X	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	X	X	X	X	H	X	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel Load	H	L	L	X	X	X	↑	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_0
Shift Right	H	L	H	H	L	L	↑	D_A	Y_{7n}	Y_{6n}	Y_{5n}	Y_{4n}	Y_{3n}	Y_{2n}	Y_{1n}	Y_{1n}
	H	L	H	H	H	L	↑	D_B	Y_{7n}	Y_{6n}	Y_{5n}	Y_{4n}	Y_{3n}	Y_{2n}	Y_{1n}	Y_{1n}
Sign Extend	H	L	H	L	X	L	↑	Y_{7n}	Y_{7n}	Y_{6n}	Y_{5n}	Y_{4n}	Y_{3n}	Y_{2n}	Y_{1n}	Y_{1n}
Hold	H	H	X	X	X	L	↑	NC	NC	NC	NC	NC	NC	NC	NC	NC

L = LOW
H = HIGH
↑ = Clock LOW-to-HIGH Transition
NC = No Change
X = Don't Care
Z = High-Impedance Output State

*When the OE input is HIGH, all input/output terminals are at the high-impedance state; sequential operation or clearing of the register is not affected.

D_7, D_6 . . . D_0 = the level of the steady-state input at the respective DY_n terminal is loaded into the flip-flop while the flip-flop outputs (except Q_0) are isolated from the DY_n terminal.

D_A, D_B = the level of the steady state inputs to the serial multiplexer input.

Y_{7n}, Y_{6n} . . . Y_{0n} = the level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.

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8-Bit Shift/Storage Register with Synchronous Clear 25LS23

FEATURES

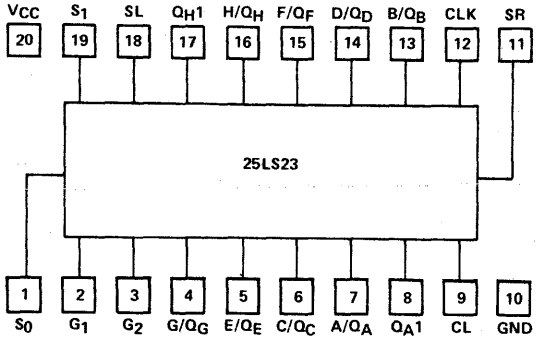
- Synchronous Clear
- Three-State Outputs
- Common Input/Output Pins
- Advanced Low-Power Schottky Processing
- 100% Reliability Assurance Testing in Compliance With MIL-STD-883

DESCRIPTION

The 25LS23 is an 8-bit universal shift/storage register with 3-state outputs. The function is similar to the 25LS299 with the exception of a synchronous clear function. Parallel load inputs and register outputs are multiplexed to allow the use of a 20-pin package. Separate continuous outputs are also provided for flip-flops A and H.

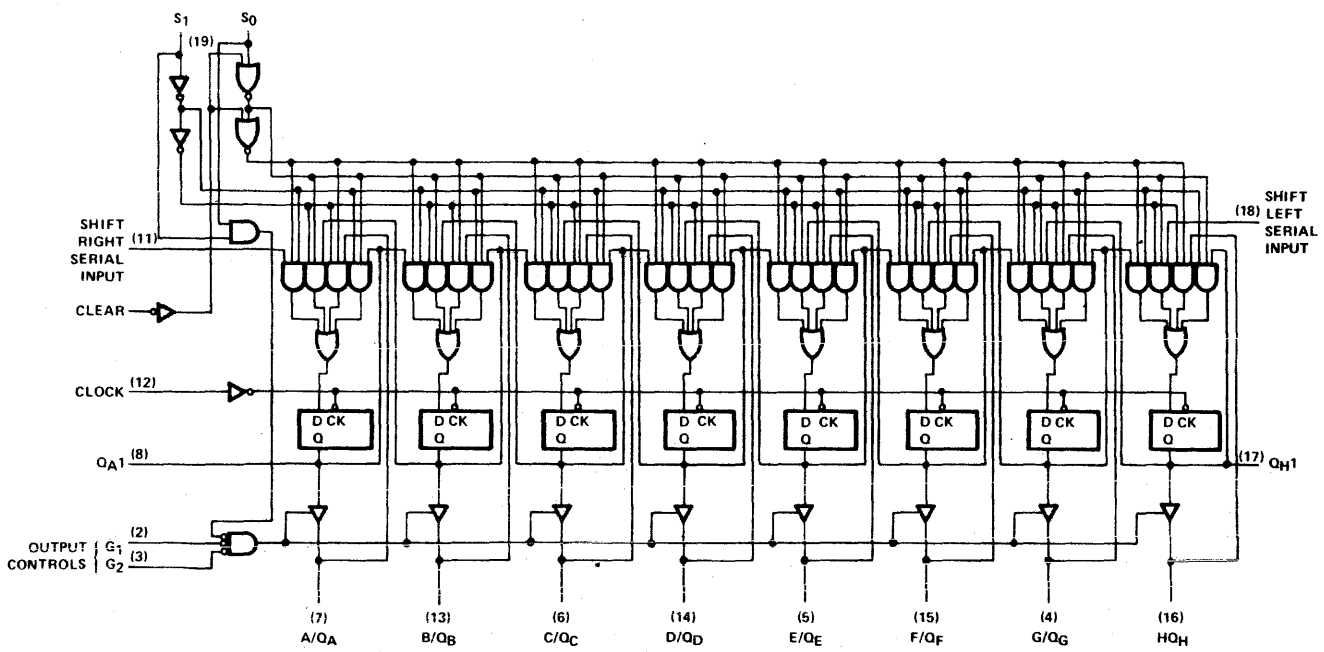
Four modes of operation are possible—Hold (store), Shift-left, Shift-right and Load Data. The 25LS23 has a typical shift frequency of 50MHz. The 25LS23 is packaged in a standard 20-pin package.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

LOGIC DIAGRAM



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Recommended Operating Conditions

		Military			Commercial			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	V
High Level Output Current I_{OH}	Q_0–Q_7			-0.44			-0.44	mA
	DY_0–DY_7			-1.0			-2.6	
Low-Level Output Current I_{OH}			4.0	8.0		4.0	8.0	mA
Operating Free Air Temperature T_A		-55		+125	0°		70	°C

Electrical Characteristics Over Operating Temperature Range (Unless Otherwise Noted)

	Description	Test Conditions (Note 1)			Military			Commercial			Units
					Min.	(2)	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{OL}	Q_0, Q_7	I_{OH} = -440μA	2.5			2.7			V
			DY_0–DY_7	I_{OH} = -1.0mA	2.4						
				I_{OH} = -2.6mA				2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}		I_{OL} = 4.0mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8.0mA		0.35	0.45		0.35	0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.7			0.8	V
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = -18mA					-1.5			-1.5	V
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V		S_0, S_1			-0.8			-0.8	mA
				All others			-0.4			-0.4	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V (Except DY_i)		S_0, S_1			40			40	μA
				All others			20			20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V (Except DY_i)		S_0, S_1			0.2			0.2	mA
				All others			0.1			0.1	
I_O	Off-State (High Impedance) Output Current	V_{CC} = MAX.		V_O = 0.4V			-100			-100	μA
				V_O = 2.4V			40			400	
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.			-30		-85	-30		-85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)				38	57		38	57	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).

4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

5. I_{CC}–measured with clock input HIGH and output controls HIGH.

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8-Bit Shift/Storage Register with Synchronous Clear 25LS23

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0V)

Parameters	From (Input)	To (Output)	+25°C Min.	+25°C Typ.	+25°C Max.	Units
Test Conditions: C_L = 15pF, R_L = 2kΩ						
t_{PLH}	Clock	Q_0 or Q_7		19		ns
t_{PHL}				23		
t_{PLH}	Clock	DY_i		18		
t_{PHL}				21		
t_s	S_i, S_0 Setup Prior to Clock		20			ns
t_s	S_R, S_L Setup Prior to Clock		20			
t_{pw}	Clock Pulse Width		25			
t_h	Hold Time		3.0			
t_s	Clear Setup Prior to Clock		20			
t_{ZH}	S_i, S_0	DY_i		20		ns
t_{ZL}				19		
t_{ZH}	$\overline{G}_1$, G_2	DY_i		20		
t_{ZL}				18		
f_{max}	Maximum Frequency			50		mHz
Test Conditions: C_L = 5pF, R_L = 2kΩ						
t_{LZ}	S_1, S_0	DY_i		22		ns
t_{HZ}				20		
t_{LZ}	G_1, G_2	DY_i		20		
t_{HZ}				16		

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FEATURES

- Four operational modes
- Three-state outputs
- Common input/output pins
- Cascadable shifting
- Advanced Low-Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

DESCRIPTION

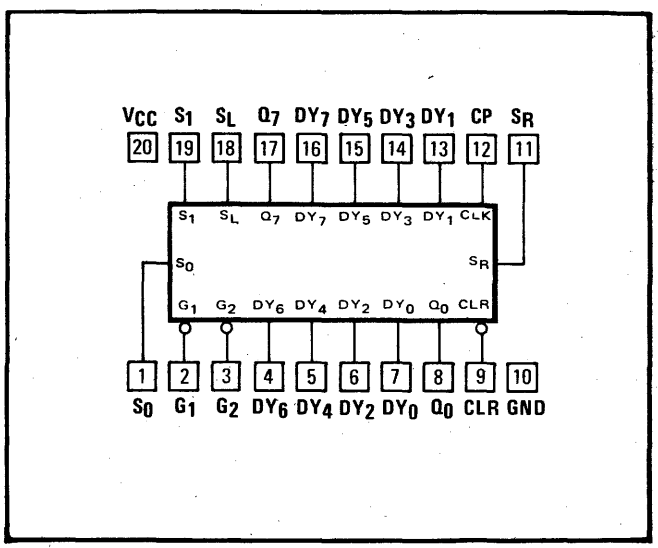
The 25LS299 is an 8-bit universal shift/storage register with 3-state outputs. Four modes of operation are possible—Hold (store), shift left, shift right and load data.

Parallel load inputs and register outputs are multiplexed to reduce the number of package pins. Separate continuous outputs are also provided for flip-flop Q_0 and Q_7. These devices can be cascaded to N-Bit words.

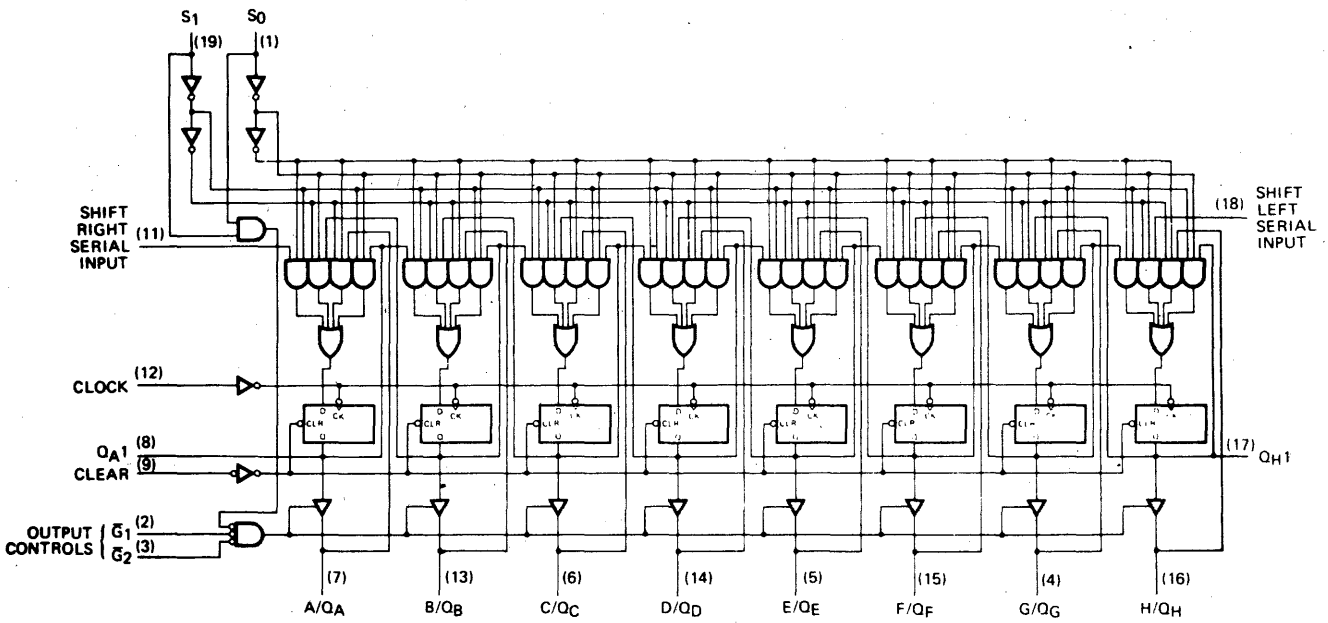
The 25LS299 has a typical shift frequency of 50 MHz; and is packaged in the standard 20-pin DIP package.

A separate active-LOW asynchronous clear input forces all flip-flops to the LOW state whenever this clear input is LOW.

PIN-OUT DIAGRAM



LOGIC DIAGRAM



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8-Bit Universal Shift/Storage Register 25LS299

Recommended Operating Conditions

	Military			Commercial			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-Level Output Current, I_{OH}		-0.44	-1.0		-0.44	-2.6	mA
Low-Level Output Current, I_{OL}	4		8	4		8	mA
Operating Free-Air Temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*			Military			Commercial			Unit
					Min	Typ**	Max	Min	Typ**	Max	
V_{IH}		Guaranteed input logical HIGH voltage for all inputs			2			2			V
V_{IL}		Guaranteed input logical LOW voltage for all inputs					0.7			0.8	V
V_I		V_{CC}=MIN., I_{IN}= -18mA					-1.5			-1.5	V
V_{OH}		V_{CC}=MIN. V_{IN}=V_{IH} or V_{IL}	Q_0,Q_7	I_{OH}=-0.44mA	2.5			2.7			V
			DY_0,DY_7	I_{OH}=-1.0mA	2.4						V
				I_{OH}=-2.6mA				2.4			
V_{OL}		V_{CC}=MIN. V_{IN}=V_{IH} or V_{IL}		I_{OL} = 4.0mA		0.25	0.40		0.25	0.40	V
				I_{OL} = 8.0mA		0.30	0.45		0.30	0.45	
I_I	S_0, S_1	V_{CC}=MAX., V_{IN} = 5.5V					0.2			0.2	mA
	All others						0.1			0.1	
I_H	S_0, S_1	V_{CC}=MAX., V_{IN} = 2.7V					40			40	μA
	All others						20			20	
I_{IL}	S_0, S_1	V_{CC}=MAX., V_{IN} = 0.4V					-0.8			-0.8	mA
	All others						-0.4			-0.4	
I_O		V_{CC} = MAX.		V_0= 0.4V			-100			-100	μA
				V_0= 2.7V			40			40	
I_{OS}		V_{CC} = MAX., See Note 3			-30		-85	-30		-85	mA
I_{CC}		V_{CC} = MAX., See Note 4				38	57		38	57	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.

3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

4. I_{CC} – measured with clock input HIGH and output controls HIGH.

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Switching Characteristics, V_{CC} = 5V, T_A = +25°C

Parameter	From (input)	To (output)	+25°C Min	+25°C Typ	+25°C Max	Unit
Test Conditions: C_L = 15pF, R_L = 2kΩ						
t_{PLH}	Clock	Q_i		19		ns
t_{PHL}				23		
t_{PLH}	Clock	DY_i		18		ns
t_{PHL}				21		
t_{PHL}	Clear	DY_0-DY_7		25		ns
t_{PHL}	Clear	Q_0 or Q_7		27		ns
t_{ZH}	S_1, S_0	DY_i		20		ns
t_{ZL}				19		
t_{ZH}	$\overline{G}_1$, $\overline{G}_2$	DY_i		20		ns
t_{ZL}				18		
t_s	S_1, S_0 Set-up Prior to Clock		20			ns
t_s	S_R, S_L Set-up Prior to Clock		20			ns
t_{pw}	Pulse Width (Clock)		25			ns
t_n	Hold Time		3			ns
f_{max}				50		MHz
Test Conditions: C_L = 5pF, R_L = 2kΩ						
t_{LZ}	S_1, S_0	DY_i		22		ns
t_{HZ}				20		
t_{LZ}	$\overline{G}_1$, $\overline{G}_2$	DY_i		20		ns
t_{HZ}				16		

TRUTH TABLE

FUNCTION		INPUTS S_R	S_L	CLEAR	CLOCK	S_0	S_1	$\overline{G}_1$ $\overline{G}_2$	OUTPUTS Q_0	Q_7	INPUTS/OUTPUTS DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7
Clear		X	X	L	X	(Note 1)		L L	L	L	L	L	L	L	L	L	L	L
Output Control		X	X	X	X	X	X	H L	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
		X	X	X	X	X	X	L H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
		X	X	X	X	X	X	H H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
M O D E	Hold	X	X	H	X	L	L	L L	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	Load (Note 2)	X	X	H	↑	H	H	L L	A	A	A	B	C	D	E	F	G	H
	Shift Right	L	X	H	↑	H	L	L L	L	DY_6	L	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6
	Shift Right	H	X	H	↑	H	L	L L	H	DY_6	H	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6
	Shift Left	X	L	H	↑	L	H	L L	DY_1	L	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7	L
	Shift Left	X	H	H	↑	L	H	L L	DY_1	H	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7	H

L = LOW Z = High Impedence ↑ = Transition LOW-to-HIGH
H = HIGH X = Don't Care NC = No Change

Notes: 1. Either LOW to observe outputs.
2. In this mode DY_i are inputs.

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INTRODUCTION TO INTERFACE

INTERFACE.....

The Master Selection Guide provides sufficient information to make initial product selections, to lead you to a group of device numbers and manufacturers' names. It enables you to find the products which are most appropriate to fulfill your major requirements and then provides data for many of the more important products.

All devices that appear in this section, both in the initial selection guide and in the data pages, are included in the Part Number and Product Indexes. These index listings lead to the page and the line on that page where each device appears.

In the Interface Section the selection parameters differ drastically for each category; therefore, each has its own format. The analog to digital converter category has two formats: one for binary output devices and another for decimal units. Some of the products in this section, primarily analog to digital and digital to analog converters, are hybrids; the ones listed are those packaged to be compatible with IC's.

This section is not complicated by reference to package styles; the package style suffixes are usually deleted. For more information on each companies' suffixes, see the Part Number Guide. Throughout the Master Selection Guide, each full military temperature range (−55°C to 125°C) device is indicated by a dagger (†) before the manufacturer's name. Manufacturers' names are normally spelled out; however, a few are abbreviated and the abbreviations are explained on page 176.

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National Semiconductor	465
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The manufacturers listed above are providing detailed information on their latest and most significant products. They have made this investment to help you.
chose not to.

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INTERFACE–Analog Switches

Switches with Drivers

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
SPST	CMOS	75	±11	±15,5	**HI5040-2**	**† Harris** (410)	
					HI5040-5	**Harris** (410)	
					IH5040C	Intersil	
					IH5040M	† Intersil	
	JFET	6	-5 to 4	±15,5	CAG10A	† Teledyne C	
			-5 to 10	±15	CAG6	† Teledyne C	
		10	-5 to 4	±15,5	CAG10C	† Teledyne C	
			-5 to 10	±15	CAG6-10	† Teledyne C	
		15	-10 to 5	±15,5	CAG10D	† Teledyne C	
		30	±5	±5,5	CAG10	† Teledyne C	10
			±8	-18,12	IH5001	Intersil	
		50	±8	-18,12	IH5002	Intersil	
			-10 to 4	±15,5	CAG10B	† Teledyne C	
			-10 to 5	-15,5	CAG14	† Teledyne C	
			±10	±15	2110BE	† Teledyne C	
		60	±10	±18,5	CAG30	† Teledyne C	
		100	±5	±15	2107BE	† Teledyne C	
	PMOS	80-300	±10	-20,10	TL610I	TI	
					TL610M	† TI	
		100-400	±10	-20,10	TL610C	TI	20
2xSPST	CMOS	30	±11	±15,5	IH5048C	Intersil	
					IH5048M	† Intersil	
		50	±15	±15,5	**HI5048-2**	**† Harris** (410)	
					HI5048-5	**Harris** (410)	
				±15	**DG300A**	**† Siliconix** (528)	
					DG300B	**Siliconix** (528)	
					DG300C	**Siliconix** (528)	
					DG304A	**† Siliconix** (528)	
					DG304B	**Siliconix** (528)	
					DG304C	**Siliconix** (528)	30
					DG381A	**† Siliconix** (530)	
					DG381B	**† Siliconix** (530)	
					DG381C	**† Siliconix** (530)	
		70	±15	±15	AD7513S	† AD	
					AD7513T	† AD	
					HI200-2	**† Harris** (394)	
					MP7513S	Micro Power	
					DG200A	† Siliconix	
		75	±10	±15,5	IH200M	† Intersil	
			±15	±15,5	**HI5041-2**	**† Harris** (410)	40
					HI5041-5	**Harris** (410)	
					IH5041C	Intersil	
					IH5041M	† Intersil	
		80	±10	±15,5	IH200C	Intersil	
			±15	±15	AD7513J	AD	
					AD7513K	AD	
					HI200-5	**Harris** (394)	
					MPS7513J	Micro Power	
					MPS7513K	Micro Power	
					DG200B	Siliconix	50
					DG200C	Siliconix	
	JFET	6	-6 to 10	-18,15	CAG27	† Teledyne C	
		10	-6 to 10	-18,15	CAG27-10	† Teledyne C	
			-7.5 to 15	±15,5	DG180A	† Intersil	
					DG180B	Intersil	
					DG180A	† Siliconix	
					DG180B	Siliconix	
			±10	-18,12	DG141A	† Intersil	

(Continued)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
2xSPST	JFET	10	±10	-18,12	(Cont'd.)		
					IH5005	† Intersil	60
					AH0141	† National	
					AH0141C	National	
					DG141A	† Siliconix	
				-20,10,5	DG180A	† Intersil	
					DG180B	Intersil	
					DG180A	† Siliconix	
					DG180B	Siliconix	
		15	±7.5	±15	DG151A	† Intersil	
					AH0151	† National	
					AH0151C	National	70
					DG151A	† Siliconix	
			±8	-18,12	DG141B	Intersil	
					DG441A	Intersil	
					DG141B	Siliconix	
		20	±5.5	±15	DG151B	Intersil	
					DG451A	Intersil	
					DG151B	Siliconix	
		30	-6 to 10	-18,15	CAG24	† Teledyne C	
			-7.5 to 15	±15,5	DG181A	† Intersil	
					IH181M	† Intersil	80
					AM181	† National	
					DG181A	† Siliconix	
			±10	-18,12	DG133A	† Intersil	
					IH5003	† Intersil	
					IH5006	† Intersil	
					AH0133	† National	
					AH0133C	National	
					DG133A	† Siliconix	
			-12.5 to 10	-20,10,5	DG181A	† Intersil	
					IH181M	† Intersil	90
					AM181	† National	
					DG181A	† Siliconix	
			for D/A ±10	-20	CDA2-3	† Teledyne C	
		35	±8	-18,12	DG433A	† Intersil	
		50	±7.5	±15	DG152A	† Intersil	
					AH0152	† National	
					AH0152C	National	
					DG152A	† Siliconix	
			-7.5 to 15	±15,5	DG181B	Intersil	100
					IH181C	Intersil	
					DG181B	Siliconix	
			±8	-18,12	DG133B	Intersil	
					DG133B	Siliconix	
			±10	-18,15	CAG13	† Teledyne C	
					CAG42	† Teledyne C	
					CAG45A	† Teledyne C	
				-18,12	IH5004	Intersil	
			-10 to 15	±15,5	AM281	National	
			-12.5 to 10	-20,10,5	DG181B	Intersil	110
					IH181C	Intersil	
					DG181B	Siliconix	
			-15 to 10	-20,10,5	AM281	National	
		75	-7.5 to 15	±15,5	AM182	† National	
			-15 to 10	-20,10,5	AM281	National	
			±10	±15	TL182M	† TI	
			-10 to 15	±15,5	DG182A	† Intersil	

(Continued)

DT¹ means four terminals with a pair of normally open and normally closed contacts.

INTERFACE–Analog Switches (Cont'd)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
2xSPST	JFET	75	-10 to 15	±15,5	(Cont'd.)		
					IH182M	† Intersil	
					DG182A	† Siliconix	
			-12.5 to 10	-20,10,5	AM182	† National	
			-15 to 10	-20,10,5	DG182A	† Intersil	
					IH182M	† Intersil	
					DG182A	† Siliconix	
		80	±8	-18,12	DG434A	Intersil	
			±10	-18,12	DG134A	† Intersil	
					IH5007	Intersil	10
					AH0134	† National	
					AH0134C	National	
					DG134A	† Siliconix	
		100	±5.5	±15	DG452	Intersil	
					DG152B	Siliconix	
			±8	-18,12	DG134B	Intersil	
					DG134B	Siliconix	
			±10	±15,5	TL182I	TI	
					TL182C	TI	
			-10 to 15	±15,5	DG182B	Intersil	20
					IH182C	Intersil	
					AM282	National	
					DG182B	Siliconix	
			-15 to 10	-20,10,5	DG182B	Intersil	
					IH182C	Intersil	
					AM282	National	
					DG182B	Siliconix	
	PMOS	75-200	-5 to 10	±15,5	DGM111A	† Siliconix	
			±10	-20,10,5	DGM111A	† Siliconix	
		75-250	-5 to 10	±15	DGM111B	Siliconix	30
			±10	-20,10,5	DGM111B	Siliconix	
		100-450	±10	-20,10,5	DG111	† Intersil	
					DG112	† Intersil	
4xSPST	CMOS	80	±15	±15	**HI201-2**	**† Harris**	**(400)**
		80*	±5	±5	CDS4016	† RCA	
					CDS4016E	RCA	
		100	±15	±15	**HI201-5**	**Harris**	**(400)**
					AD7510DJ	AD	
					AD7510DK	AD	
					AD7510DS	† AD	40
					AD7511DJ	AD	
					AD7511DK	AD	
					AD7511DS	† AD	
					AD7511DT	† AD	
					MPS7510DJ	Micro Power	
					MPS7510DK	Micro Power	
					MPS7510DS	† Micro Power	
					MPS7511DJ	Micro Power	
					MPS7511DK	Micro Power	
					MPS7511DS	† Micro Power	50
					MPS7511DT	† Micro Power	
		175	±15	±15	DG201A	† Siliconix	
		200	±7.5	±7.5	SCL4066S	SSS	
			±15	±15	DG201B	Siliconix	
					DG201C	Siliconix	
		280	±7.5	±7.5	AD7516K	AD	
					AD7516T	† AD	
					F4066BC	Fairchild	
					F4066BM	† Fairchild	

(Continued)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
4xSPST	CMOS	280	±7.5	±7.5	(Cont'd.)		60
					MPS7516K	Micro Power	
					MPS7516T	† Micro Power	
					SIL4066B	† Mitel	
					SIL4066BE	Mitel	
					MC14066BA	† Motorola	
					MC14066BC	Motorola	
					CD4066BC	National	
					CD4066BM	† National	
					µPD4066	NEC America	
					CD4066B	† RCA	70
					CD4066BE	RCA	
					HBF4066AE	SGS	
					N4066A	Signetics	
					SCL4066B	† SSS	
					SCL4066BE	SSS	
					TC4066	Toshiba	
		400	±7.5	±7.5	AD7516J	AD	
					AD7516S	† AD	
					MPS7516J	Micro Power	
					MPS7516S	† Micro Power	80
					SIL4016B	† Mitel	
					SIL4016BE	Mitel	
					MC14016BA	† Motorola	
					MC14016BC	Motorola	
					SCL4016B	† SSS	
					SCL4016BE	SSS	
					CM4016A	† Solitron	
					CM4016AE	Solitron	
					TP4016A/UB	† TI	
					TP4316A	† TI	90
					TC4016	Toshiba	
		800	±7.5	±7.5	F4016C	Fairchild	
					F4016M	† Fairchild	
		850	±7.5	±7.5	CD4016AC	National	
					CD4016AM	† National	
					CD4016B	† RCA	
					CD4016BE	RCA	
					SCL4016A	† SSS	
					SCL4016AE	SSS	
					CM4016A	† Solitron	100
					CM4016AE	Solitron	
					CM4116A	† Solitron	
					CM4116AE	Solitron	
			Inverted control				
					SCL4416A	† SSS	
					SCL4416AE	SSS	
	JFET	10	±10	-18,2.8	CAM604A	† Teledyne C	
		30	±7.5	±15,5	AM193	National	
		50	-10 to 5	-15,5	CAG49	† Teledyne C	
		60	±10	-18,5	CAG49	† Teledyne C	110
				±18,-7	CAG50	† Teledyne C	
		75	±10	±15,5	AM194	National	
4xSPST	Various Combinations of normally on/off						
	JFET	100	±10	-18,15	CAG48A	† Teledyne C	
		200	±10	±15,0	LF11201	† National	
					LF11202	† National	
					LF11331	† National	
					LF11332	† National	
					LF11333	† National	
		250	±10	±15,0	LF12201	National	120
					LF13201	National	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog Switches (Cont'd)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
4xSPST Various Combinations of normally on/off							
	JFET	250	±10	±15,0	(Cont'd.)		
					LF12202	National	
					LF13202	National	
					LF12331	National	
					LF13331	National	
					LF12332	National	
					LF13332	National	
					LF12333	National	
					LF13333	National	10
	PMOS	200-600	±10	-20,10,5	AH0015	† National	
					AH0015C	National	
4xSPST Common Output							
	PMOS	100-450	±10	-20,10	DG116	† Intersil	
				-20,10,5	DG118	† Intersil	
		150-250	±10	-20,10,5	DG172A	† Siliconix	
		150-500	±10	-20,10,5	DG172B	Siliconix	
		200-600	±10	-20,10,5	DG172C	Siliconix	
5xSPST Common Output							
	PMOS	100-450	±10	-20,10	DG123	† Intersil	
					DG123A	† Siliconix	20
				-20,10,5	DG125	† Intersil	
					DG125A	† Siliconix	
		125-500	±10	-20,10	DG123B	Intersil	
					DG123B	Siliconix	
				-20,10,5	DG125B	Intersil	
					DG125B	Siliconix	
16xSPST							
	CMOS	60	±9	±9	7507-01	Telenetics	
SPDT[1]	CMOS	30	±11	±15,5	IH5050C	Intersil	
					IH5050M	† Intersil	30
		50	±15	±15,5	**HI5050-2**	**† Harris**	**(410)**
					HI5050-5	**Harris**	**(410)**
				±15	**DG301A**	**† Siliconix**	**(528)**
					DG301B	**Siliconix**	**(528)**
					DG301C	**Siliconix**	**(528)**
					DG305A	**† Siliconix**	**(528)**
					DG305B	**Siliconix**	**(528)**
					DG305C	**Siliconix**	**(528)**
					DG387A	**† Siliconix**	**(530)**
					DG387B	**Siliconix**	**(530)**
					DG387C	**Siliconix**	**(530)**
		75	±15	±15,5	**HI5042-2**	**† Harris**	**(410)**
					HI5042-5	**Harris**	**(410)**
					IH5042C	Intersil	
					IH5042M	† Intersil	
	JFET	6	-5 to 10	±15	CAG7	† Teledyne C	
		10	-5 to 10	±15	CAG7-10	† Teledyne C	
			-7.5 to 15	±15,5	DG186A	† Intersil	
					DG186B	Intersil	
					DG186A	† Siliconix	
					DG186B	Siliconix	50
			±10	-18,12	DG146A	† Intersil	
					AH0146	† National	
					AH0146C	National	
					DG146A	Siliconix	
			-12.5 to 10	-20,10,5	DG186A	† Intersil	
					DG186B	Intersil	

(Continued)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
SPDT[1]	JFET	10	-12.5 to 10	-20,10,5	(Cont'd.)		
					DG186A	† Siliconix	60
					DG186B	Siliconix	
		15	±7.5	±15	DG161A	† Intersil	
					AH0161	† National	
					AH0161C	National	
					DG161A	Siliconix	
			±8	-18,12	DG146B	Intersil	
					DG446A	Intersil	
					DG146B	Siliconix	
		20	±5.5	±15	DG461A	Intersil	
					DG161B	Siliconix	70
		30	-7.5 to 15	±15,5	DG187A	† Intersil	
					IH187M	† Intersil	
					AM187	† National	
					DG187A	† Siliconix	
			±10	-18,12	DG144A	† Intersil	
					AH0144	† National	
					AH0144C	National	
					DG144A	† Siliconix	
			-12.5 to 10	-20,10,5	DG187A	† Intersil	
					IH187M	† Intersil	80
					AM187	† National	
					DG187A	† Siliconix	
		35	±8	±8,12	DG444A	Intersil	
		50	±7.5	±15	DG162A	† Intersil	
					AH0162	† National	
					AH0162C	National	
					DG162A	† Siliconix	
			-7.5 to 15	±15,5	DG187B	Intersil	
					IH187C	Intersil	
					DG187B	Siliconix	90
			±8	-18,12	DG144B	Intersil	
					DG144B	Siliconix	
				±15	2126BG	† Teledyne C	
			-10 to 15	±15,5	AM287	National	
			-12.5 to 10	-20,10,5	DG187B	Intersil	
					IH187C	Intersil	
					DG187B	Siliconix	
			-15 to 10	-20,10,5	AM287	National	
		75	-7.5 to 15	±15,5	AM188	† National	
			±10	±15,5	TL188M	† TI	100
			-10 to 15	±15,5	DG188A	† Intersil	
					IH188M	† Intersil	
					DG188A	† Siliconix	
			-12.5 to 10	-20,10,5	AM188	† National	
			-15 to 10	-20,10,5	DG188A	† Intersil	
					IH188M	† Intersil	
					DG188A	† Siliconix	
		80	±8	-18,12	DG443A	Intersil	
			±10	-18,12	DG143	† Intersil	
					AH0143	† National	110
					AH0143C	National	
					DG143A	† Siliconix	
		100	±5.5	±15	DG162B	Siliconix	
			±8	±15	DG462A	Intersil	
			±10	±15,5	TL188I	TI	
					TL188C	TI	

(Continued)

DT[1] means four terminals with a pair of normally open and normally closed contacts.

INTERFACE–Analog Switches (Cont'd)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
SPDT[1]	JFET	100	±10	(Cont'd.)			
				±15	AH2114	† National	
				-18,12	DG143B	Siliconix	
			-10 to 15	±15,5	DG188B	Intersil	
					IH188C	Intersil	
					AM288	National	
					DG188B	Siliconix	
			-15 to 10	-20,10,5	DG188B	Intersil	
					IH188C	Intersil	
					AM288	National	10
					DG188B	Siliconix	
		125	±10	±15	AH2114C	National	
	NPN PNP						
		10	±10	-5,5	CDA23	† Teledyne C	
SPDT	JFET	50	-10 to 5	-15,5	CDA18	† Teledyne C	
SPDT for D/A							
	NPN PNP						
		10	10	10	CDA4A	† Teledyne C	
			0 to -10	-15	CDA1-3	† Teledyne C	
			±10	-15,5	CDA23	† Teledyne C	20
				±15	CDA6	† Teledyne C	
SPDT[1]	PMOS	75-200	-5 to 15	±15	DG175A	† Siliconix	
			±10	-20,10,5	DG175A	† Siliconix	
		75-250	-5 to 15	±15	DG175B	Siliconix	
			±10	-20,10,5	DG175B	Siliconix	
		100-400	±10	-20,10	TL604I	TI	
					TL604M	† TI	
		200-600	±10	-20,10	TL604C	TI	
SPDT	PMOS	100-400	±10	-20,10	SI3002A	† Siliconix	
					SI3002B	Siliconix	
					TL601I	TI	30
					TL601M	† TI	
					TL607I	TI	
					TL607M	† TI	
		200-600	±10	-20,10	TL601C	TI	
					TL607C	TI	
		200*	±10	-20,10	SH3002C	Fairchild	
					SH3002M	† Fairchild	
2xSPDT[1]	CMOS	30	±11	±15,5	IH5051C	Intersil	
					IH5051M	† Intersil	40
		50	±15	±15,5	**HI5051-2**	**† Harris**	**(410)**
					HI5051-5	**Harris**	**(410)**
				±15	**DG303A**	**† Siliconix**	**(528)**
					DG303B	**Siliconix**	**(528)**
					DG303C	**Siliconix**	**(528)**
					DG307A	**† Siliconix**	**(528)**
					DG307B	**Siliconix**	**(528)**
					DG307C	**Siliconix**	**(528)**
					DG390A	**† Siliconix**	**(530)**
					DG390B	**Siliconix**	**(530)** 50
					DG390C	**Siliconix**	**(530)**
		75	±15	±15,5	**HI5043-2**	**† Harris**	**(410)**
					HI5043-5	**Harris**	**(410)**
					IH5043C	Intersil	
					IH5043M	† Intersil	
2xSPDT	CMOS	100	±15	±15	AD7512DIJ	AD	
					AD7512DIK	AD	
					AD7512DIS	† AD	

(Continued)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
2xSPDT	CMOS	100	±15	±15	(Cont'd.)		
					AD7512DIT	† AD	60
					MPS7512DIJ	Micro Power	
					MPS7512DIK	Micro Power	
					MPS7512DIS	† Micro Power	
	PNP	10	±10	±15	CDA29A	† Teledyne C	
2xSPDT[1]	DMOS	50	±10	±15,5	SD5600	Signetics	
	JFET	10	-7.5 to 15	±15,5	DG189A	† Intersil	
					DG189B	Intersil	
					DG189A	† Siliconix	
					DG189B	Siliconix	
			-12.5 to 15	-20,15,5	DG189A	† Intersil	70
					DG189B	Intersil	
					DG189A	† Siliconix	
					DG189B	Siliconix	
		30	-7.5 to 15	±15,5	DG190A	† Intersil	
					IH190M	† Intersil	
					AM190	† National	
					DG190A	† Siliconix	
			-12 to 15	-20,15,5	DG190A	† Intersil	
					IH190M	† Intersil	
					AM190	† National	80
					DG190A	† Siliconix	
		50	-7.5 to 15	±15,5	DG190B	Siliconix	
			-10 to 15	±15,5	AM290	National	
			-12.5 to 15	-20,10,5	DG190B	Siliconix	
			-15 to 10	-20,10,5	AM290	National	
		75	-7.5 to 15	±15,5	AM191	† National	
			-10 to 15	±15,5	DG191A	† Intersil	
					IH191M	† Intersil	
					DG191A	† Siliconix	
			-12.5 to 15	-20,10,5	AM191	† National	90
			-15 to 10	-20,10,5	DG191A	† Intersil	
					IH191M	† Intersil	
					DG191A	† Siliconix	
		100	-10 to 15	±15,5	DG191B	Intersil	
					IH191C	Intersil	
					AM291	National	
					DG191B	Siliconix	
			-15 to 10	-20,10,5	DG191B	Intersil	
					IH191C	Intersil	
					AM291	National	100
					DG191B	Siliconix	
		125	±10	±15,5	TL191M	† TI	
		150	±10	±15,5	TL191I	TI	
					TL191C	TI	
3xSPDT	CMOS	280	±7.5	±7.5	F4053BC	Fairchild	
					F4053BM	† Fairchild	
					SIL4053B	† Mitel	
					SIL4053BE	Mitel	
					MC14053BA	† Motorola	
					MC14053BC	Motorola	110
					CD4053C	National	
					CD4053M	† National	
					µPD4053	NEC America	
					CD4053B	† RCA	
					CD4053BE	RCA	
					SCL4053A	† SSS	
					SCL4053AE	SSS	
					CM4053A	† Solitron	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog Switches (Cont'd)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
3xSPDT	CMOS	280	±7.5	±7.5	(Cont'd.)		
					CM4053AE	Solitron	
					TP4053A/B	TI	
					TC4053	Toshiba	
	PMOS	200-800	±10	-20,10,5	DG170A	† Siliconix	
		250-850	±10	-20,10,5	DG170B	Siliconix	
					DG170C	Siliconix	
4xSPDT for D/A							
	CMOS	100	0.1	8	AD7519J	AD	
					MPS7519J	Micro Power	10
4xSPDT	JFET	35	±10	-15,5	HCS310	HyComp	
	NMOS	—	—	8	DG515A	† Siliconix	
					DG515B	Siliconix	
					DG515C	Siliconix	
	NPN	—	-10 to -3	±15	ULN-2140	Sprague	
					ULN-2141	Sprague	
					ULN-2142	Sprague	
					ULS-2140	† Sprague	
					ULS-2141	† Sprague	
					ULS-2142	† Sprague	20
			—	—	AD550	† AD	
					AD555	AD	
	PNP	7	0 to -10	-15	CDA11-S12	Teledyne C	
		10	0 to -10	-15	CDA11	Teledyne C	
8xSPDT	CMOS	60	±9	±9	7507-02	Telenetics	
10xSPDT for D/A							
	NMOS	—	—	8	DG516A	† Siliconix	
					DG516B	Siliconix	
					DG516C	Siliconix	
DPST	CMOS	75	±15	±15,5	**HI5044-2**	**† Harris** (410)	30
					HI5044-5	**Harris** (410)	
					IH5044C	Intersil	
					IH5044M	† Intersil	
2xDPST	CMOS	30	±11	±15,5	IH5049C	Intersil	
					IH5049M	† Intersil	
		50	±15	±15,5	**HI5049-2**	**† Harris** (410)	
					HI5049-5	**Harris** (410)	
				±15	**DG302A**	**† Siliconix** (528)	
					DG302B	**Siliconix** (528)	
					DG302C	**Siliconix** (528)	40
					DG306A	**† Siliconix** (528)	
					DG306B	**Siliconix** (528)	
					DG306C	**Siliconix** (528)	
					DG384A	**† Siliconix** (530)	
					DG384B	**Siliconix** (530)	
					DG384C	**Siliconix** (530)	
		75	±15	±15,5	**HI5045-2**	**† Harris** (410)	
					HI5045-5	**Harris** (410)	
					IH5045C	Intersil	
					IH5045M	† Intersil	50
2xDPST Three Control Input							
	CMOS	200	±15	±15,5	**HI1800A-2**	**† Harris** (406)	
					HI1800A-5	**Harris** (406)	
2xDPST	JFET	10	-7.5 to 15	±15,5	DG183A	† Intersil	
					DG183B	Intersil	
					DG183A	† Siliconix	
					DG183B	Siliconix	
			±10	-18,12	DG140A	† Intersil	
					AH0140	† National	
					AH0140C	National	60

(Continued)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
2xDPST	JFET	10	±10	-18,12	(Cont'd.)		
					DG140A	† Siliconix	
			-12.5 to 10	-20,10,5	DG183A	† Intersil	
					DG183B	Intersil	
					DG183A	† Siliconix	
					DG183B	† Siliconix	
		15	±7.5	±15	DG153A	† Intersil	
					AH0153	† National	
					AH0153C	National	
					DG153A	† Siliconix	70
			±8	-18,12	DG440A	Intersil	
					DG140B	Siliconix	
		20	±5.5	±15	DG153B	Intersil	
					DG453A	Intersil	
					DG153B	Siliconix	
		30	-7.5 to 15	±15,5	DG184A	† Intersil	
					IH184M	† Intersil	
					AM184	† National	
					DG184A	† Siliconix	
			±10	-18,12	DG129A	† Intersil	80
					AH0129	† National	
					AH0129C	National	
					DG129A	† Siliconix	
			-12.5 to 10	-20,10,5	DG184A	† Intersil	
					IH184M	† Intersil	
					AM184	† National	
					DG184A	† Siliconix	
		35	±8	-18,12	DG429A	Intersil	
		50	±7.5	±15	DG154A	† Intersil	
					AH0154	† National	90
					AH0154C	National	
					DG154A	† Siliconix	
			-7.5 to 15	±15,5	DG184B	Intersil	
					IH184C	Intersil	
					DG184B	Siliconix	
			±8	-18,12	DG129B	Siliconix	
			-10 to 15	±15,5	AM284	National	
			-12.5 to 15	-20,10,5	DG184B	Intersil	
					IH184C	Intersil	
					DG184B	Siliconix	100
			-15 to 10	-20,10,5	AM284	National	
		60	±10	-18,15	CS4R101A	† Teledyne C	
		75	-7.5 to 15	±15,5	AM185	† National	
			-10 to 15	±15,5	DG185A	† Intersil	
					IH185M	† Intersil	
					DG185A	† Siliconix	
			-12.5 to 10	-20,10,5	AM185	† National	
			-15 to 10	-20,10,5	DG185A	Intersil	
					IH185M	† Intersil	
					DG185A	† Siliconix	110
		80	±8	-18,12	DG426A	Intersil	
			±10	-18,12	DG126A	† Intersil	
					AH0126	† National	
					AH0126C	National	
					DG126A	† Siliconix	
		100	±5.5	±15	DG154B	Intersil	
					DG454A	Intersil	
					DG154B	Siliconix	

(Continued)

DT¹ means four terminals with a pair of normally open and normally closed contacts.

INTERFACE–Analog Switches (Cont'd)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
2xDPST	JFET	100	(Cont'd.)				
			±8	-18,12	DG126B	Siliconix	
			-10 to 15	±15,5	DG185B	Intersil	
					IH185C	Intersil	
					AM285	National	
					DG185B	Siliconix	
			-15 to 10	-20,10,5	DG185B	Intersil	
					IH185C	Intersil	
					AM285	National	
					DG185B	Siliconix	10
		125	±10	±15,5	TL185M	† TI	
		150	±10	±15,5	TL185I	TI	
					TL185C	TI	
2xDPST Common Output							
	PMOS	100-450	±10	-20,10,5	DGM122A	† Siliconix	
		125-500	±10	-20,10,5	DGM122B	Siliconix	
		200-600	±10	-20,10,5	AH0019	† National	
					AH0019C	National	
3xDPST Common Output							
	PMOS	100-450	±10	-20,10	DG120	† Intersil	20
				-20,10,5	DG121	† Intersil	
DPDT[1]	CMOS	50	±15	±15,5	**HI5046A-2**	**† Harris (410)**	
					HI5046A-5	**Harris (410)**	
		75	±15	±15,5	1115	† DDC	
					HI5046-2	**† Harris (410)**	
					HI5046-5	**Harris (410)**	
					IH5046C	Intersil	
					IH5046M	† Intersil	
	JFET	10	±10	-18,12	DG145A	† Intersil	
					AH0145	† National	30
					AH0145C	National	
					DG145A	† Siliconix	
		15	±7.5	±15	DG163A	† Intersil	
					AH0163	† National	
					AH0163C	National	
					DG163A	† Siliconix	
			±8	-18,12	DG445A	Intersil	
					DG145B	Siliconix	
		20	±5.5	±15	DG163B	Intersil	
					DG463A	Intersil	40
					DG163B	Siliconix	
		30	±10	-18,12	DG139A	† Intersil	
					AH0139	† National	
					AH0139C	National	
					DG139A	† Siliconix	
		35	±8	-18,12	DG439A	Intersil	
		50	±7.5	±15	DG164A	† Intersil	
					AH0164	† National	
					AH0164C	National	
					DG164A	† Siliconix	50
			±8	-18,12	DG139B	Siliconix	
		80	±8	-18,12	DG442A	Intersil	
			±10	-18,12	DG142A	† Intersil	
					AH0142	† National	
					AH0142C	National	
					DG142A	† Siliconix	
		100	±5.5	±15	DG164B	Intersil	
					DG464A	Intersil	
					DG164B	Siliconix	

(Continued)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
DPDT[1]	JFET	100	(Cont'd.)				60
			±10	-18,12	DG142B	Siliconix	
2xDPDT	PMOS	—	±7	-5,-21	TDA1195	Siemens	
DPDT	PMOS	150-450	±10	-20,10,5	DG173A	† Siliconix	
		150-500	±10	-20,10,5	DG173B	Siliconix	
		200-600	±10	-20,10,5	AH0014	† National	
					AH0014C	National	
		200-275	±10	-28,5,12	CRC9505	Rockwell	
4PST	CMOS	50	±15	±15,5	**HI5047A-2**	**† Harris (410)**	
					HI5047A-5	**Harris (410)**	
		75	±15	±15,5	**HI5047-2**	**† Harris (410)**	70
					HI5047-5	**Harris (410)**	
					IH5047C	Intersil	
					IH5047M	† Intersil	
8PST with shift register							
	DMOS	100	7	12	SD5350	Signetics	
4PDT for D/A							
	PNP	10	±10	±15,5	CDA28A	† Teledyne C	
2x4PDT[1]	CMOS	60	±9	±9	7509-01	Telenetics	

Switches without Drivers

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
SPST	JFET	30	±10		AM1000	† National	
		50	±15		AM1001	† National	80
		100	±0.2		IH5021C	Intersil	
					IH5021M	† Intersil	
					IH5023C	Intersil	
					IH5023M	† Intersil	
			0 to (Drive-4)		IH5037C	Intersil	
					IH5037M	† Intersil	
			±10		AM1002	† National	
		150	±0.2		IH5022C	Intersil	
					IH5022M	† Intersil	
					IH5024C	Intersil	90
					IH5024M	† Intersil	
			0 to (Drive-4)		IH5038C	Intersil	
					IH5038M	† Intersil	
2xSPST	JFET	100	±0.2		IH5017C	Intersil	
					IH5017M	† Intersil	
			0 to (Drive-4)		IH5033C	Intersil	
					IH5033M	† Intersil	
		150	±0.2		IH5020C	Intersil	
					IH5020M	† Intersil	
			0 to (Drive-4)		IH5036C	Intersil	100
					IH5036M	† Intersil	
2xSPST Common Output							
	JFET	100	±0.2		IH5019C	Intersil	
					IH5019M	† Intersil	
			0 to (Drive-4)		IH5035C	Intersil	
					IH5035M	† Intersil	
		150	±0.2		IH5018C	Intersil	
					IH5018M	† Intersil	
			0 to (Drive-4)		IH5034C	Intersil	
					IH5034M	† Intersil	110
3xSPST	JFET	100	±0.2		IH5015C	Intersil	
					IH5015M	† Intersil	
					AH5015C	National	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog Switches (Cont'd)

Switches without Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
3xSPST	JFET	100	(Cont'd.)				
			0 to (Drive-4)		IH5031C	Intersil	
					IH5031M	† Intersil	
		150	±0.2		IH5016C	Intersil	
					IH5016M	† Intersil	
					AH5016C	National	
			0 to (Drive-4)		IH5032C	Intersil	
					IH5032M	† Intersil	
3xSPST	Common Output						
	JFET	100	±0.2		IH5013C	Intersil	10
					IH5013M	† Intersil	
					AH5013C	National	
			0 to (Drive-4)		IH5029C	Intersil	
					IH5029M	† Intersil	
		150	±0.2		IH5014C	Intersil	
					IH5014M	† Intersil	
					AH5014C	National	
			0 to (Drive-4)		IH5030C	Intersil	
					IH5030M	† Intersil	
3xSPST	PMOS	200-600			MM455	† Intersil	20
					MM555	Intersil	
					MM455	† National	
					MM555	National	
					Si455A	† Siliconix	
					Si555B	Siliconix	
4xSPST	DMOS	45	±5		SD5001	Signetics	
			±10		SD5000	Signetics	
	JFET	100	±0.2		IH5011C	Intersil	
					IH5011M	† Intersil	
					AH5011C	National	30
					AM97C11C	National	
					AM9711C	National	
			0 to (Drive-4)		1108C-1	DDC	
					1108M-1	† DDC	
					IH5027C	Intersil	
					IH5027M	† Intersil	
		150	±0.2		1104C-2	DDC	
					1104M-2	† DDC	
					IH5012C	Intersil	
					IH5012M	† Intersil	40
					AH5012C	National	
					AM97C12C	National	
					AM9712C	National	
			0 to (Drive-4)		1108C-2	DDC	
					1108M-2	† DDC	
					IH5028C	Intersil	
					IH5028M	† Intersil	
		—			G125	† Intersil	
					G126	† Intersil	
					G127	† Intersil	
					G128	† Intersil	
					G129	Intersil	
					G1330	Intersil	
					G1340	Intersil	
					G125A	† Siliconix	
					G125B	Siliconix	
					G126A	† Siliconix	
					G126B	Siliconix	
					G127A	† Siliconix	
					G127B	Siliconix	60
					G128A	† Siliconix	
					G128B	Siliconix	

Switches without Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
4xSPST	Common Output						
	DMOS	45	±5		SD5101	Signetics	
			±10		SD5100	Signetics	
	JFET	100	±0.2		IH5009C	Intersil	
					IH5009M	† Intersil	
					AH5009C	National	
					AM97C09C	National	
					AM9709C	National	70
			0 to (Drive-4)		IH5025C	Intersil	
					IH5025M	† Intersil	
		150	±0.2		IH5010C	Intersil	
					IH5010M	† Intersil	
					AH5010C	National	
					AM97C10C	National	
					AM9710C	National	
			0 to (Drive-4)		IH5026C	Intersil	
					IH5026M	† Intersil	
					G129	† Intersil	80
					G130	† Intersil	
					G131	† Intersil	
					G132	† Intersil	
					G1350	Intersil	
					G1360	Intersil	
					G129A	† Siliconix	
					G129B	Siliconix	
					G130A	† Siliconix	
					G130B	Siliconix	
					G131A	† Siliconix	90
					G131B	Siliconix	
					G132A	† Siliconix	
					G132B	Siliconix	
4xSPST	Two Outputs						
	JFET	—			G123	Intersil	
	PMOS	—			G123A	† Siliconix	
					G123B	Siliconix	
4xSPST	PMOS	200-600			MM452	† Intersil	
					MM552	Intersil	
					MM452	† National	100
					MM552	National	
					Si452A	† Siliconix	
					Si552B	Siliconix	
		—			MBM851	GI	
					MEM851	GI	
4xSPST	Common Output						
	PMOS	—			MM451	† Intersil	
					MM551	Intersil	
					MM451	† National	
					MM551	National	110
					G124A	† Siliconix	
					G124B	Siliconix	
4xSPST	(current switch for D/A)						
	—	—			LM11340	National	
					LM11341	National	
5xSPST	Common Output						
	PMOS	—			G116A	† Intersil	
					G116B	Intersil	
					G116A	† Siliconix	
					G116B	Siliconix	120
5xSPST	Common Output plus output switch						
	PMOS	—			G117A	† Intersil	
					G117B	Intersil	
					G117A	† Siliconix	
					G117B	Siliconix	

DT[1] means four terminals with a pair of normally open and normally closed contacts.

INTERFACE–Analog Switches (Cont'd)

Switches without Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
6xSPST Common Output							
	PMOS	—			CRC9509	Rockwell	
					MEM855	GI	
					MEM856	GI	
					G115	Intersil	
					G115A	† Intersil	
					G118A	† Intersil	
					G118B	Intersil	
					AM2009	† National	
					AM2009C	National	
					MM5504	† National	10
					MM4504	National	
					G115A	† Siliconix	
					G115B	Siliconix	
					G118A	† Siliconix	
					G118B	Siliconix	
8xSPST Two Outputs							
	PMOS	—			MEM857	GI	
10xSPST							
	PMOS	—			CRC9510	Rockwell	
10xSPST Three Outputs							20
	NMOS	—			NMX5010	SMC	
	PMOS	—		Null	MEM853	GI	
2xDPST Common Output							
	PMOS	—			G122A	† Siliconix	
					G122B	Siliconix	
					MM450	† Intersil	
					MM550	Intersil	
					MM450	† National	
					MM550	National	
3xDPST Common Output							30
	PMOS	—			G119C	Intersil	
					G119M	† Intersil	
					G119A	† Siliconix	
					G119B	Siliconix	

Multiplexers

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
4 channel. See Switches 4xSPST							
4 channel differential							
	CMOS	270	±7.5	±7.5	MC14529BA	† Motorola	
					MC14529BC	Motorola	
					CD4529BC	National	
					CD4529BM	† National	40
		280	±7.5	±7.5	F4052BC	Fairchild	
					F4052BM	† Fairchild	
					SIL4052B	† Mitel	
					SIL4052BE	Mitel	
					MC14052BA	† Motorola	
					MC14052BC	Motorola	
					CD4052BC	National	
					CD4052BM	† National	
					µPD4052	NEC America	
					CD4052B	† RCA	50
					CD4052BE	RCA	
					SCL4052B	† SSS	
					SCL4052BE	SSS	
					CM4052B	† Solitron	
					CM4052BE	Solitron	
					TP4052A/B	TI	
					TC4052	Toshiba	
		300	±15	±15	AD7502J	AD	
					AD7502K	AD	
					AD7502S	† AD	60
					MPS7502J	Micro Power	

(Continued)

Multiplexers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
4 channel differential							
	CMOS	300	±15	±15	(Cont'd.)		
					MPS7502K	Micro Power	
					MPS7502S	† Micro Power	
		400	±15	±15	**HI1828A-2**	**† Harris (436)**	
					HI1828A-5	**Harris (436)**	
					DG509A	† Siliconix	
		450	±15	±15	DG509B	Siliconix	
					DG509C	Siliconix	70
		1300	±15	±15	MPC-4D	Burr-Brown	
		1500	±15	±15	HI509A-2	† Harris	
					MXD-409	Datel	
					MXD-409M	† Datel	
		1800	±15	±15	HI509A-5	Harris	
	JFET	260	-15 to 11.5	±15	**MUX-24A**	**† PMI (960)**	
					MUX-24E	**PMI (960)**	
		300	±10	±15,5	LF11306	† National	
					LF12306	National	
					LF13306	National	80
		350*	-15 to 12	±15	LF11509	† National	
					LF12509	National	
					LF13509	National	
		370	-15 to 12	±15	**MUX-24B**	**† PMI (960)**	
					MUX-24F	**PMI (960)**	
4 channel Sequential Commutator							
	PMOS	200-600	±10	-24,12	MM454	† National	
					MM554	National	
6 channel							
	JFET	60	±10	-18,2.8	CAM601A	† Teledyne C	90
8 channel							
	CMOS	150	±8	±8	MS504	RTC	
		270	±7.5	±7.5	MC14529BA	† Motorola	
					MC14529BC	Motorola	
					CD4529BC	National	
					CD4529BM	† National	
		280	±7.5	±7.5	F4051BC	Fairchild	
					F4051BM	† Fairchild	
					SIL4051B	† Mitel	
					SIL4051BE	Mitel	100
					MC14051BA	† Motorola	
					MC14051BC	Motorola	
					CD4051BC	National	
					CD4051BM	† National	
					µPD4051	NEC America	
					CD4051B	† RCA	
					CD4051BE	RCA	
					SCL4051B	† SSS	
					SCL4051BE	SSS	
					CM4051A	† Solitron	110
					CM4051AE	Solitron	
					TP4051A/B	TI	
					TC4051	Toshiba	
		300	±15	±15	AD7501J	AD	
					AD7501K	AD	
					AD7501S	† AD	
					AD7503J	AD	
					AD7503K	AD	
					AD7503S	† AD	
					MPS7501J	Micro Power	120
					MPS7501K	Micro Power	
					MPS7501S	† Micro Power	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog Switches (Cont'd)

Multiplexers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
8 channel							
	CMOS	300	±15	±15	(Cont'd.)		
					MPS7503J	Micro Power	
					MPS7503K	Micro Power	
					MPS7503S	† Micro Power	
		400	±15	±15,5	**HI1818A-2**	**† Harris (436)**	
					HI1818A-5	**Harris (436)**	
				±15	DG508A	† Siliconix	
		450	±15	±15	DG508B	Siliconix	
					DG508C	Siliconix	10
		1300	±15	±15	MPC-8S	Burr-Brown	
		1500	±15	±15	MN4708	Analogic	
					MX-808	Datel	
					MX-808M	† Datel	
					HI508A-2	**† Harris (430)**	
					MUX202	Hybrid Sys.	
					MUX203M	† Hybrid Sys.	
		1800	±15	±15	**HI508A-5**	**Harris (430)**	
	JFET	260	-15 to 11.5	±15	**MUX-08A**	**† PMI (958)**	
					MUX-08E	**PMI (958)**	20
					MUX-88A	**† PMI (962)**	
					MUX-88E	**PMI (962)**	
		300	±10	±15,5	LF11305	† National	
					LF12305	National	
					LF13305	National	
		350*	-15 to 12	±15	LF11508	† National	
					LF12508	National	
					LF13508	National	
		370	-15 to 12	±25	**MUX-08B**	**† PMI (958)**	
					MUX-08F	**PMI (958)**	30
					MUX-88B	**† PMI (962)**	
					MUX-88F	**PMI (962)**	
	PMOS	150-250	±5	-20,5	DG501A	† Siliconix	
					DG501B	Siliconix	
					DG501C	Siliconix	
		150-400	±5	-20,5	3705	Fairchild	
					SI3705	Siliconix	
		150-800	±10	-20,10	DG503A	† Siliconix	
					DG503B	Siliconix	
		200-600	±5	-15,5	DG501A	† Siliconix	40
		200-800	±5	-15,5	DG501B	Siliconix	
					DG501C	Siliconix	
		250-400	±5	-15,5	AM3705	† National	
					AM3705	National	
		450	-15	-20	3708	Fairchild	
8 channel with shift register							
	DMOS	120	0-7	12	SD5350	Signetics	
8 channel, BCD input, latch							
	PMOS	—	60	0-70	LS7110	LSI Comp	
8 channel differential							50
	CMOS	60	±9	±9	7508-02	Telenetics	
		270	±15	±15	MVD-807	Datel	
					MVD-807M	† Datel	
		280	±7.5	±7.5	CD4097B	† RCA	
					CD4097BE	RCA	
		400	±15	±15	AD7507S	† AD	
					AD7507T	† AD	

(Continued)

Multiplexers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
8 channel differential							
	CMOS	400	±15	±15	(Cont'd.)		
					HI507-2	**† Harris (418)**	60
					HI507-5	**Harris (418)**	
					IH5070M	† Intersil	
					MPS7507S	† Micro Power	
					MPS7507T	† Micro Power	
					DG507A	† Siliconix	
		450	±15	±15	AD7507J	AD	
					AD7507K	AD	
					IH5070C	Intersil	
					MPS7507J	Micro Power	
					MPS7507K	Micro Power	70
					DG507B	Siliconix	
					DG507C	Siliconix	
		1300	±15	±15	MPC-8D	Burr-Brown	
		1500	±15	±15	MXD-807	Datel	
					MXD-807M	† Datel	
					HI507A-2	**† Harris (424)**	
		1800	±15	±15	MN4708D	Analogic	
					HI507A-5	**Harris (424)**	
					4551	Teledyne P	
	JFET	300	-15 to 11	±15	**MUX-28A**	**† PMI (961)**	80
					MUX-28E	**PMI (961)**	
		350	-15 to 12	±15	LF11507	National	
		450	-15 to 11.5	±15	**MUX-28B**	**† PMI (961)**	
					MUX-28F	**PMI (961)**	
8 channel (DPST) with ring counter							
	PMOS	500,6800	±5,±4	-12,5	CRC2002	Rockwell	
8 channel differential with storage, counter							
	PMOS	750	±5	-12,5	AY5-1016	GI	
					AY6-4016	† GI	
16 channel							90
	CMOS	60	±9	±9	7508-01	Telenetics	
		270	±15	±15	MV-1606	Datel	
					MV-1606M	† Datel	
		280	±7.5	±7.5	F4067BC	Fairchild	
					F4067BM	Fairchild	
					CD4067B	† RCA	
					CD4067BE	RCA	
		400	±15	±15	AD7506S	† AD	
					AD7506T	† AD	
					HI506-2	**† Harris (418)**	100
					HI506-5	**Harris (418)**	
					IH5060M	† Intersil	
					MPS7506S	† Micro Power	
					MPS7506T	† Micro Power	
					DG506A	† Siliconix	
		450	±15	±15	AD7506J	AD	
					AD7506K	AD	
					IH5060C	Intersil	
					MPS7506J	Micro Power	
					MPS7506K	Micro Power	110
					DG506B	Siliconix	
					DG506C	Siliconix	
		1300	±15	±15	MPC-16S	Burr-Brown	
		1500	±15	±15	MX-1606	Datel	
					MX-1606M	† Datel	
					HI506A-2	**† Harris (424)**	
					MUX204	Hybrid Sys.	

(Continued)

DT[1] means four terminals with a pair of normally open and normally closed contacts.

INTERFACE–Analog Switches (Cont'd)

Multiplexers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
16 channel							
	CMOS	(Cont'd.)					
		1800	±15	±15	MN4716	Analogic	
					HI506A-5	**Harris**	**(424)**
	PMOS	5K	-5 to 15	±15, 5	**HI1840-2**	**† Harris**	**(440)**
					4552	Teledyne P	
	JFET	300	-15 to 11	±15	**MUX-16A**	**† PMI**	**(959,961)**
					MUX-16E	**PMI**	**(959)**
		350	-15to12	±15	LF1106	National	10
		450	-15 to 11.5	±15	**MUX-16B**	**† PMI**	**(959)**
					MUX-16F	**PMI**	**(959)**
16 channel with storage counter							
	PMOS	750	±5	-12,5	AY5-1016	GI	
					AY6-4016	† GI	
18 channel with address latch							
	NMOS	600	0 to 6	12	MUX1600	GI	
32 channel with memory							
	CMOS	50	±9	±9	MT8804B	† Mitel	
					MT8804BE	Mitel	20
4 x 4 channel							
	CMOS	60	±9	±9	7507-03	Telenetics	
Crosspoint Switches							
					MT8804B	† Mitel	
					MT8804BE	Mitel	
					MC3466	Motorola	
					RC4444	Raytheon	
					RM4444	† Raytheon	
					CD22100	RCA	
					SD5300	Signetics	30

Drivers

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
High Current Switch Driver (to drive power transistor switches)							
					SG1629	† Silicon G	
					SG3629	Silicon G	
2 channel							
					D112C	Intersil	
					D112M	† Intersil	
					D113C	Intersil	
					D113M	† Intersil	
					D120C	Intersil	40
					D120M	† Intersil	
					D121C	Intersil	
					D121M	† Intersil	
					D130A	† Siliconix	
					D130B	Siliconix	
					D139A	† Siliconix	
					D139B	Siliconix	
					D139C	Siliconix	
4 channel							
					D129	Intersil	50
					D129A	† Siliconix	
					D129B	Siliconix	
4 channel for DMOS							
					SD5200	Signetics	
4 channel with Decoder							
					D132A	† Siliconix	
					D132B	Siliconix	

Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
6 channel							
					D123C	Intersil	
					D123M	† Intersil	60
					D125C	Intersil	
					D125M	† Intersil	
					D123A	† Siliconix	
					D123B	Siliconix	
					D125A	† Siliconix	
					D125B	Siliconix	
					CDR125A	† Teledyne C	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog to Digital Converters

Binary Output

In this section devices with multiple codes follow those with single codes rather than repeating under each heading. Also devices are listed by the number of output bits even though their linearity corresponds to lower accuracy. Therefore when looking for devices to fill particular requirements, it is necessary to review all possibilities.

Bits-Code	Conversion Time µs	Linearity Error ±%FS	Supply Voltage	Device	Source	Line
3 Bit Expandable 8 Line/Binary/Offset Binary						
	16/20 ns	0.1	±5	ADC-HU3B	Datel	
8-Bit Binary	0.4	0.2	±5	TDC1001J	TRW	10
	1	0.2	±5	TDC1002J	TRW	
	2.5	0.2	±12,5	MN5143	Micro Net	
				MN5143H	† Micro Net	
				MN5133	Micro Net	
				MN5133H	† Micro Net	
	Multiplex input for Microprocessors					
	5	0.2	±15,5	MP20	Burr-Brown	
				MP21	Burr-Brown	
	6	0.2	±15,5	MN5123	Micro Net	
				MN5123H	† Micro Net	20
	12	0.2	±15,5	MN502	Micro Net	
				MN502H	† Micro Net	
				MN510	Micro Net	
				MN510H	Micro Net	
			±12,5	MN508	Micro Net	
				MN508H	† Micro Net	
	40	0.2	-12,5	MM4357	† National	
				MM5357	National	
				ME5034	Signetics	
	50	0.4	-12,5	ADC0800C	National	30
	80	0.4	-12,5	ADC0800	† National	
	100	0.2	12	MN5061	Micro Net	
				MN5061H	† Micro Net	
	Integrating					
	1800	0.2	±5	ADC-EK8B	Datel	
				ADC586-8	Hybrid Sys.	
				8700	Teledyne S	
				8703	Teledyne S	
8 Bit Complementary Binary						
	1.5	0.2	±15,5	MN5100	Micro Net	40
				MN5100H	† Micro Net	
	2.5	0.2	±12,5	MN5140	Micro Net	
				MN5140H	† Micro Net	
				MN5130	Micro Net	
				MN5130H	† Micro Net	
	6	0.2	±15,5	MN5120	Micro Net	
				MN5120H	† Micro Net	
	12	0.2	±15,5	MN504	Micro Net	
				MN504H	† Micro Net	
	100	0.2	12,5-12	MN5066	Micro Net	50
				MN5066H	† Micro Net	
8 Bit Complementary Offset Binary						
	12	0.2	±15,5	MN503	Micro Net	
				MN503H	† Micro Net	
				MN507	Micro Net	
				MN507H	† Micro Net	
				MN511	Micro Net	
				MN511H	† Micro Net	
			±12,5	MN509	Micro Net	
				MN509H	† Micro Net	60

(Continued)

Binary Output (Cont'd)

Bits-Code	Conversion Time µs	Linearity Error ±%FS	Supply Voltage	Device	Source	Line
8 Bit Complementary Offset Binary (Cont'd.)						
	100	0.2	12,5-12	MN5065	Micro Net	
				MN5065H	† Micro Net	
8 Bit Offset Binary						
	2.5	0.2	±15,5	MN5131	Micro Net	
				MN5131H	† Micro Net	
				MN5132	Micro Net	
				MN5132H	† Micro Net	
			±12,5	MN5141	Micro Net	70
				MN5141H	† Micro Net	
				MN5142	Micro Net	
				MN5142H	† Micro Net	
	6	0.2	±15,5	MN5121	Micro Net	
				MN5121H	† Micro Net	
				MN5122	Micro Net	
				MN5122H	† Micro Net	
	100	0.2	12	MN5060	Micro Net	
				MN5060H	† Micro Net	
8 Bit Binary/Offset Binary						80
	1	0.2	±15,5	ADH-8512-8	DDC	
		0.4	±15,5	ADH-8512-7	DDC	
8 Bit Binary/Offset Binary/Two's Complement						
	10*	0.2	±15,5	ADC541-8	Hybrid Sys.	
				ADC541B-8	† Hybrid Sys.	
8 Bit Complementary Binary/Comp. Offset Binary/Comp. Two's Complement						
	0.9	0.2	±15,5	MN5101	Micro Net	
				MN5101H	† Micro Net	
	2.8	0.2	±15,5	ADC82A	Burr-Brown	90
8 Bit Binary/Complementary Offset Binary						
	2.5	0.2	±15,5	MN5150	Micro Net	
8 Bit Binary, Integrating						
	2000	0.2	5	NE5030	Signetics	
8 Bit Binary, Microcomputer Input System						
				MP20	Burr-Brown	
				MP21	Burr-Brown	
8 Bit Binary/Offset Binary with Counter, D/A A/D						
	500	0.2	5	ADC-MC8BC	Datel	
				ADC-MC8BM	† Datel	100
				ZN425	Ferranti	
8 Bit Binary, with 8 channel analog multiplexer						
	—	0.2	5	MM74C949	National	
8 Bit Binary, with 8 channel analog multiplexer, sample and hold						
	—	0.2	5	MM74C950	National	
8 Bit Binary, with 16 channel analog multiplexer						
	114	0.2	5	ADC0186	National	
				MM74C948	National	
		0.4	5	ADC0817	National	110
8 Bit Complementary Offset Binary, with 8 channel analog multiplexer, sample and hold						
	7	0.2	±15,5	MN7120	Micro Net	
				MN7120H	† Micro Net	
10-Bit Binary	16*	0.2	15,5-15	AD7570J	AD	
				MPS7570J	Micro Power	
	20*	0.05	15,5-15	AD7570L	AD	
				MPS7570L	Micro Power	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Analog to Digital Converters (Cont'd)

Bits-Code	Conversion Time µs	Linearity Error ±%FS	Supply Voltage	Device	Source	Line
Binary Output (Cont'd)						
10-Bit Binary	(Cont'd.)					
	Integrating					
	6000	0.05	±5	ADC-EK10B	Datel	
				ADC586-10	Hybrid Sys.	
				8701	Teledyne S	
				8704	Teledyne S	
10 Bit Binary/Two's Complement Stochastic						
	200ms	0.2	-12,5	AY5-5053	GI	
				AY5-5054	GI	
10 Bit Complementary Binary/Comp. Offset Binary/Comp. Two's Complement						
	6	0.05	±15,5	ADC84-10	Burr-Brown	10
				ADC85-10	Burr-Brown	
				ADC85C-10	Burr-Brown	
	18	0.05	±15,5	ADC80A-10	Burr-Brown	
				ADC80A-10	Micro Net	
12-Bit Binary	13	0.0125	±15,5	MN5210	Micro Net	
				MN5210H	† Micro Net	
				MN5213	Micro Net	
				MN5213H	† Micro Net	
	25	0.012	±15,5	AD572A	AD	
				AD572B	AD	20
				AD572S	† AD	
	50	0.0125	±15,5	MN5200	Micro Net	
				MN5200H	† Micro Net	
				MN5203	Micro Net	
				MN5203H	† Micro Net	
			5-15	ADC1210	† National	
				ADC1210C	National	
		0.048	5-15	ADC1211	† National	
				ADC1211C	National	
	175	0.0125	±12,5-12	MN5250	Micro Net	30
				MN5250H	† Micro Net	
	24ms integrating					
		0.0125	±5	ADC-EK12B	Datel	
				ADC586-12	Hybrid Sys.	
				8702	Teledyne S	
				8705	Teledyne S	
	20 ms Dual Slope, 2 Devices					
		0.0125	±15,5	LF13300	National	
			-15,5	MM5863	National	
12 Bit Binary/Offset Binary/Two's Complement						40
	2	0.012	±15	**ADC-HF12B**	**Datel**	**(384)**
			±15,5	ADH-8516-12	DDC	
				ADH-8516-11	DDC	
	300	0.012	±(9-15)	**ADC-HC12B**	**Datel**	**(383)**
				ADC-HC12BMM	**† Datel**	**(383)**
12 Bit Binary/Offset Binary with 8 channel analog multiplexer, sample and hold						
	9*	0.012	±15,5	**HDAS-8M**	**Datel**	**(382)**
12 Bit Binary/Offset Binary with 16 channel analog multiplexer, sample and hold						50
	9*	0.012	±15,5	**HDAS-16M**	**Datel**	**(382)**
12 Bit Complementary Binary						
	13	0.0125	±15,5	MN5216	Micro Net	
				MN5216H	† Micro Net	
	50	0.0125	±15,5	MN5206	Micro Net	
				MN5206H	† Micro Net	
	175	0.0125	±12,5-12	MN5253	Micro Net	

(Continued)

Bits-Code	Conversion Time µs	Linearity Error ±%FS	Supply Voltage	Device	Source	Line
Binary Output (Cont'd)						
12 Bit Complementary Binary						
	175	0.0125	±12,5-12	(Cont'd.)		
				MN5253H	† Micro Net	60
12 Bit Complementary Offset Binary						
	13	0.0125	±15,5	MN5211	Micro Net	
				MN5211H	† Micro Net	
				MN5212	Micro Net	
				MN5212H	† Micro Net	
				MN5214	Micro Net	
				MN5214H	† Micro Net	
				MN5215	Micro Net	
				MN5215H	† Micro Net	
	50	0.0125	±15,5	MN5201	Micro Net	70
				MN5201H	† Micro Net	
				MN5202	Micro Net	
				MN5202H	† Micro Net	
				MN5204	Micro Net	
				MN5204H	† Micro Net	
				MN5205	Micro Net	
				MN5205H	† Micro Net	
	175	0.0125	±15,5	MN5251	Micro Net	
				MN5251H	† Micro Net	
				MN5252	Micro Net	80
				MN5252H	† Micro Net	
12 Bit Complementary Binary/Comp. Offset Binary						
	30	0.012	±15,5	873-15	† Beckman	
	40	0.012	±15,5	873-88	Beckman	
	50	0.012	±15,5	873-78	Beckman	
12 Bit Complementary Binary/Comp. Offset Binary with sample and hold						
	8	0.012	±15,5	**ADC-HS12B**	**Datel**	**(385)**
12 Bit Complementary Binary/Comp. Offset Binary/Comp. Two's Complement						90
	8	0.0125	±15,5	**ADC-HZ12B**	**Datel**	**(387)**
				ADC-HZ12BMM	**Datel**	**(387)**
	10	0.012	±15,5	ADC85-12	Burr-Brown	
				ADC85C-12	Burr-Brown	
				ADC84-12	Burr-Brown	
	20	0.0125	±15,5	**ADC-HX12B**	**Datel**	**(386)**
				ADC-HX12BMM	**Datel**	**(386)**
	25	0.0125	±15,5	ADC80A-12	Burr-Brown	
				ADC80A-12	Micro Net	
	30	0.012	±15,5	ADC581-12	Hybrid Sys.	100
12 Bit plus sign, Ramp						
	36 ms	0.0125	-15.5	ADB1200	National	
				LF13300	National	
13 Bit Two's Complement, Multiple Integration, 5 and 8 Bit Serial Output						
	40ms*	0.006	±5,12	AD7550B	AD	
				MPS7550B	Micro Power	
14 Bit Binary, Serial/Parallel Output						
	250	0.003	±15,5	MN5210	Micro Net	
16 Bit Binary, Dual Slope, 2 devices						110
	250ms	—	±15,5	7104	Intersil	
				8052	Intersil	
16 Bit Various Codes, Building Block						
	—	—	±15,5	8052	Intersil	
				8053	Intersil	

† Military Temperature Range (–55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog to Digital Converters (Cont'd)

Decimal Output

Digits	Device	Source	Line
Bargraph (Analog Output)	UAA170	Siemens	
	UAA180	Siemens	
2½ Digits, v to f Converter	ADD2500	National	
3 Digits, Integrating	**LD130**	**Siliconix (537)**	
3 Digits, Dual Slope, Building Block, for microprocessor systems, e.g. TMS1000	TL505	TI	10
3 1/3 Digits, Dual Slope	**LD131**	**Siliconix (537)**	
3½ Digits, Dual Slope	MN2301	Analogic	
	ZNA1116E	Ferranti	
	ICL7106	Intersil	
	ICL7107	Intersil	
	MC904	IPI	
	MPS7138	Micro Power	
3½ Digits, Integrating	ADC-EK12D	Datel	20
	MC14433	Motorola	
	ADC3511	National	
	ADD3500	National	
	ADD3501	National	
	MM74C935	National	
	MM74C937	National	
	8750	Teledyne S	
3½ Digits, Dual Slope, 2 device sets	ICL7101	Intersil	30
	ICL7103	Intersil	
	ICL7103A	Intersil	
	ICL8052	Intersil	
	ICL8052A	Intersil	
	ICL8053	Intersil	
	ICL8053A	Intersil	
	TL500	TI	
	TL502	TI	
3½ Digits, Integrating, 2 device sets	LD110	Intersil	40
	LD111	Intersil	
	LD114	Intersil	
	LD110	**Siliconix (535)**	
	LD111	**Siliconix (535)**	
	LD111A	Intersil	
	LD114	**Siliconix (535)**	
3½ Digits, 2 device sets	MPS7104	Micro Power	
	MPS5007	Micro Power	
3¾ Digits, Integrating	ADC3701	National	50
	ADD3711	National	
	MM74C936	National	
	MM74C938	National	
3¾ Digits, Dual Slope	S190	Siemens	
3½ 4½ Digits, Ramp Type, 2 device sets	MC1405	Motorola	
	MC1505	†Motorola	
	MC14435	Motorola	60
	MC14435E	†Motorola	
4½ Digits, Dual Slope, 2 device sets	7103	Intersil	

(Continued)

Decimal Output (Cont'd)

Digits	Device	Source	Line
4½ Digits, Dual Slope, 2 device sets	(Cont'd.)		
	7103A	Intersil	
	8052A	Intersil	
	8055A	Intersil	
	LF12300	National	
	LF13300	National	
	ADB4500	National	70
	ADB4510	National	
	LD120	**Siliconix (537)**	
	LD121	**Siliconix (539)**	

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Digital to Analog Converters

D/A Converters

In this section devices with multiple codes follow those with single codes rather than repeating under each heading. Also devices are listed by the number of input bits even if their linearity corresponds to less accuracy. Therefore when looking for devices to fill particular requirements, it is necessary to review all possibilities.

Bits-Code	Setting Time (±½LSB) µs	Linearity Error %FPS	Supply Voltage	Device	Source	Line
4 Bit 16 Lines/Binary, external reference						
	25*	0.1	-5	DAC-HU4B	Datel	
				DAC-HU4BMM	†Datel	
6 Bit Binary, Multiplying						
	0.25*	0.78	-(5-15),5	SSS1408A-6	AMD	
				SSS1408A-6	**PMI** (919)	
	0.3*	0.78	-(5-15),5	1408-6	AMD	
				µA0802CC	Fairchild	
				MC1408A-6	Motorola	
				DAC0806LC	National	
				LM1408-6	National	
				MC1408-6	Signetics	
6 Bit Complementary Binary/Complementary Offset Binary, Multiplying						
	0.3	0.78	-(5-15),5	MC1406	Motorola	
				MC1506	†Motorola	
6 Bit Complementary Binary/Complementary Offset Binary						
	3	0.4	±(12-18)	**DAC-01**	**†PMI** (909)	
				DAC-01B	**†PMI** (909)	
				DAC-01C	**PMI** (909)	
				DAC-01F	**†PMI** (909)	
				DAC-01H	**PMI** (909)	
		0.78	±(12-18)	µPC603	NEC America	
				DAC-01D	**PMI** (909)	
	23*	0.78	±15,5	MN301	Micro Net	
				MN301H	†Micro Net	
7 Bit Binary, Multiplying						
	0.25*	0.39	-(5-15),5	SSS1408A-7	AMD	
				SSS1408A-7	**PMI** (919)	
	0.3*	0.39	-(5-15),5	1408-7	AMD	
				µA0802BC	Fairchild	
				MC1408-7	Motorola	
				DAC0807LC	National	
				LM1408-7	National	
				MC1408-7	Signetics	
8 Bit BCD (2 BCD Digits)						
	0.135	0.25	(5-18)	**DAC-20A**	**†PMI** (931)	
				DAC-20E	**PMI** (931)	
	0.150	0.5	(5-18)	**DAC-20**	**†PMI** (931)	
				DAC-20C	**PMI** (931)	
	23	0.5	±15	MN3010	Micro Net	
				MN3010H	†Micro Net	
8 Bit Binary, Multiplying						
	0.25*	0.2	-(5-15),5	SSS1408A-8	AMD	
				SSS1508-8	†AMD	
				SSS1408A-8	**PMI** (919)	
				SSS1508A-8	**†PMI** (919)	
	0.3*	0.2	-(12-15),5	AD559K	AD	
				AD559S	†AD	
			-(5-15),5	1408-8	AMD	
				1508-8	†AMD	
				DAC-IC8BC	Datel	
				DAC-IC8BM	†Datel	
				µA0802AC	Fairchild	
				µA0802AM	†Fairchild	
				MC1408-8	Motorola	

(Continued)

D/A Converters (Cont'd)

Bits-Code	Setting Time (±½LSB) µs	Linearity Error %FPS	Supply Voltage	Device	Source	Line
8 Bit Binary, Multiplying						
	0.3*	0.2	-(5-15),5	(Cont'd.)		
				MC1508-8	†Motorola	
				DAC0808L	†National	
				DAC0808LC	National	
				LM1408-8	National	
				LM1508-8	†National	
				MC1408-8	Signetics	
				MC1508-8	†Signetics	
	1.5	0.2	5-10/15	DAC331C-08	Hybrid Sys.	
				DAC331M-08	†Hybrid Sys.	
		0.5	-(5-15),5	MC3408	Motorola	
8-Bit Binary	0.135	0.2	±15	MN3015	Micro Net	
				MN3015H	†Micro Net	
	0.2/1.0	0.2	±15	DAC-82B	Burr-Brown	
				DAC-82S	†Burr-Brown	
	1	0.2	±15	MN3008	Micro Net	
				MN3008H	†Micro Net	
				MN3009	Micro Net	
				MN3009H	†Micro Net	
	1.5	0.2	5-10/15	DAC331C-08	Hybrid Sys.	
				DAC331M-08	Hybrid Sys.	
	2.5	0.2	±15	MN3014	Micro Net	
				MN3014H	†Micro Net	
				MN3002	Micro Net	
				MN3002H	†Micro Net	
8 Bit Offset Binary						
	23	0.2	±15	MN3001	Micro Net	
				MN3001H	†Micro Net	
				DAC337C-1	Hybrid Sys.	
				DAC337M-1	Hybrid Sys.	
	45	0.2	±15	MN3006	Micro Net	
				MN3006H	†Micro Net	
				DAC337C-6	Hybrid Sys.	
				DAC337M-6	†Hybrid Sys.	
8 Bit Binary with latches						
	2*	0.2	±(12-18)	**NE5018**	**Signetics** (1913)	
				SE5018	**†Signetics** (1913)	
	23	0.2	±15,5	MN328	Micro Net	
				MN328H	†Micro Net	
8 Bit Binary with counter						
	2.0*	0.2	5	ZN4258	Ferranti	
8 Bit Complementary Binary						
	0.1	0.2	5,15	MN333	Micro Net	
	0.225	0.2	±(6-18)	**DAC-100C**	**PMI** (950)	
				DAC-100C	**†PMI** (950)	
		0.3	±(6-18)	**DAC-100D**	**PMI** (950)	
				DAC-100D	**†PMI** (950)	
	23	0.2	±15	MN3000	Micro Net	
				MN3000H	†Micro Net	
				MN3001	Micro Net	
				MN3001H	†Micro Net	
	45	0.2	±15	MN3006	Micro Net	
				MN3006H	†Micro Net	
8 Bit Complementary Binary with latch						
	23	0.2	±15, 5	MN328B	Micro Net	
				MN328BH	†Micro Net	
	45	0.2	±15, 5	MN335	Micro Net	
				MN335H	†Micro Net	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits-Code	Setting Time (±½LSB) µs	Linearity Error %FPS	Supply Voltage	Device	Source		Line
8 Bit Binary/Complementary Binary/Offset, Multiplying							
	0.135	0.1	±(5-18)	DAC-08A	† AMD		
				µA0801AM	† Fairchild		
				DAC-08A	**† PMI**	(919)	
				DAC-08H	**PMI**	(919)	
				NE5009	Signetics		
				SE5009	† Signetics		
		0.19	±(5-18)	DAC-08	† AMD		
				µA0801M	† Fairchild		
				DAC0800L	† National		
				DAC-08	**† PMI**	(919)	10
				SE5008	† Signetics		
	0.015	0.19	±(5-18)	DAC-08E	AMD		
				DAC-08BC	Datel		
				DAC-08BM	† Datel		
				µA0801E	Fairchild		
				DAC-0800LC	National		
				DAC-08E	**PMI**	(919)	
				NE5008	Signetics		
		0.39	±(5-18)	DAC-08C	AMD		
				µA0801CC	Fairchild		20
				DAC0801LC	National		
				DAC-08C	NEC America		
				DAC-08C	**PMI**	(919)	
				NE5007	Signetics		
8 Bit Binary/Offset Binary							
	0.025	0.2	±15	DAC-HF8B	Datel		
	35	0.2	±15	MN3013	Micro Net		
				MN3013H	† Micro Net		
8 Bit Complementary Binary/Complementary Offset Binary							30
	0.2	0.2	±15	DAC90B	Burr-Brown		
				DAC90S	† Burr-Brown		
8 Bit Complementary Binary/Complementary Offset Binary with latches							
	3	0.2	±15,5	MN3020	Micro Net		
				MN3020H	† Micro Net		
8 Bit Binary/Offset Binary/Comp, Binary with latches							
	4*	0.2	±15	DAC336	Hybrid Sys.		
8 Bit (7 Bits plus Sign) Companding							
	0.5	—	±15	AM6070C	AMD		40
				AM6070M	† AMD		
				AM6071M	† AMD		
				AM6072M	† AMD		
				AM6073C	AMD		
				AM6073M	† AMD		
	0.5*	—	±15	**DAC-76**	**† PMI**	(935)	
				DAC-76B	**† PMI**	(935)	
				DAC-76C	**PMI**	(935)	
				DAC-76D	PMI		
				DAC-76E	**PMI**	(935)	50
				DAC-87C	**PMI**	(935)	
				DAC-87E	**PMI**	(935)	
8 Bit Binary Ladder							
	1.5*	—	—	**HI1085**	**Harris**	(449)	
	3	—	—	**HI1080**	**† Harris**	(449)	
Dual 8 Bit Binary, data latches, addressable							
	—	0.4	±15,5	MP10	Burr-Brown		
				MP11	Burr-Brown		
9 Bit (8 Bits plus sign), Multiplying							
	23	0.2	±15	MN380	Micro Net		60
				MN380H	† Micro Net		

D/A Converters (Cont'd)

Bits-Code	Setting Time (±½LSB) µs	Linearity Error %FPS	Supply Voltage	Device	Source		Line
9 Bit plus sign. Offset Binary, Multiplying							
	15	0.1	±15,5	MN411	Micro Net		
				MN411H	† Micro Net		
	45	0.1	±15,5	MN410	Micro Net		
				MN410H	† Micro Net		
10 Bit Binary, Multiplying							
	0.25	0.05	-15,5	DAC-IC10B	Datel		
				MC3410	Motorola		
				MC3510	† Motorola		70
		0.1	-15,5	MC3410C	Motorola		
	50	0.05	±15	MN3100	Micro Net		
10-Bit Binary	0.25*	0.025	-15,5	AD561K	AD		
				AD561T	† AD		
		0.05	-15,5	AD561J	AD		
				AD561S	† AD		
		0.1	±(12-18)	**DAC-03AD**	**PMI**	(911,913)	
				DAC-03BD	**PMI**	(911,913)	80
		0.2	±(12-18)	**DAC-03CD**	**PMI**	(911,913)	
		0.4	±(12-18)	**DAC-03DD**	**PMI**	(911,913)	
	23	0.05	±15	DAC337C-5	Hybrid Sys.		
				DAC337M-5	† Hybrid Sys.		
				MN3005	Micro Net		
				MN3005H	† Micro Net		
10 Bit Complementary Binary							
	0.375	0.05	±(6-18)	**DAC-100A**	**PMI**	(950)	90
				DAC-100A	**† PMI**	(950)	
		0.1	±(6-18)	**DAC-100B**	**PMI**	(950)	
				DAC-100B	**† PMI**	(950)	
	2*	0.05	±15	DAC345I	Hybrid Sys.		
	5*	0.05	±15	DAC346V	Hybrid Sys.		
				DAC346V	† Hybrid Sys.		
	23	0.05	±15	MN3003	Micro Net		
				MN3003H	† Micro Net		
10 Bit Binary/Complementary Binary, Multiplying							
	0.3*	0.025	±(5-18)	**DAC-10A**	**† PMI**	(929)	100
		0.05	±(5-18)	**DAC-10B**	**† PMI**	(929)	
				DAC-10E	**PMI**	(929)	
		0.1	±(5-18)	**DAC-10F**	**PMI**	(929)	
10 Bit Offset Binary, Multiplying							
	30	0.05	-15,5	M/D2005-1	HyComp		
10 Bit Offset Binary							
	23	0.05	±15	DAC337C-4	Hybrid Sys.		
				DAC337M-4	† Hybrid Sys.		
				MN3004	Micro Net		
				MN3004H	† Micro Net		110
	45	0.05	±15	DAC337C-7	Hybrid Sys.		
				DAC337M-7	† Hybrid Sys.		
				MN3007	Micro Net		
				MN3007H	† Micro Net		
10 Bit Binary/Offset Binary, Multiplying							
	0.5*	0.05	5/15	DAC-HA10B	Datel		
				DAC-HA10BM	† Datel		
10 Bit Binary/Offset Binary							
	0.025	0.05	±15	DAC-HF10B	Datel		

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits-Code	Setting Time (±½LSB) µs	Linearity Error %FPS	Supply Voltage	Device	Source	Line
10 Bit Binary/Offset Binary and Complements, Multiplying						
	0.5*	0.05	5-15	AD7520L	AD	
				AD7520U	†AD	
				AD7530L	AD	
				AD7520L	Intersil	
				AD7520U	†Intersil	
				AD7530L	Intersil	
		0.1	5-15	AD7520K	AD	
				AD7520T	†AD	
				MPS7520K	Micro Power	
				MPS7520T	† Micro Power	10
				AD7530K	AD	
				AD7520K	Intersil	
				AD7520T	†Intersil	
				AD7530K	Intersil	
		0.2	5-15	AD7520J	AD	
				AD7520S	†AD	
				AD7530J	AD	
				AD7520J	Intersil	
				AD7520S	†Intersil	
				AD7530J	Intersil	20
				MPS7520J	Micro Power	
				MPS7520S	† Micro Power	
	1.5	0.05	5-10/15	DAC331C-10	Hybrid Sys.	
				DAC331M-10	† Hybrid Sys.	
10 Bit Binary/Offset Binary and Complements, Multiplying, with latches						
	0.5*	0.05	15,5-15	AD7522L	AD	
				AD7522U	†AD	
				MPS7522L	Micro Power	
				MPS7522U	† Micro Power	30
		0.1	15,5-15	AD7522K	AD	
				AD7522T	†AD	
				MPS7522K	Micro Power	
				MPS7522T	† Micro Power	
		0.2	15,5-15	AD7522J	AD	
				AD7522S	†AD	
				MPS7522J	Micro Power	
				MPS7522S	† Micro Power	
10 Bit Binary/Two's Complement, Stochastic						
	6800	0.2	-12,5	AY5-5053	GI	40
10 Bit Two's Complement						
	1.5*	0.1	±(12-18)	**DAC-04AC**	**PMI** (916)	
				DAC-04BC	**PMI** (916)	
				DAC-06A	**†PMI** (916)	
				DAC-06E	**PMI** (916)	
		0.2	±(12-18)	**DAC-04CC**	**PMI** (916)	
				DAC-06B	**†PMI** (916)	
				DAC-06F	**PMI** (916)	
		0.4	±(12-18)	**DAC-06C**	**†PMI** (916)	
				DAC-06G	**PMI** (916)	50
	2.5*	0.4	±(12-18)	**DAC-04DD**	**PMI** (916)	
11 Bit (10 Bit plus Sign)						
	1.5*	0.1	±(12-18)	**DAC-02AC**	**PMI** (913)	
				DAC-02BC	**PMI** (913)	
				DAC-05A	**†PMI** (913)	
				DAC-05E	**PMI** (913)	
		0.2	±(12-18)	**DAC-02CC**	**PMI** (913)	
				DAC-05B	**†PMI** (913)	
				DAC-05F	**PMI** (913)	
		0.4	±(12-18)	µPC610	NEC America	60
				DAC-02DD	**PMI** (913)	
				DAC-05C	**†PMI** (913)	

(Continued)

D/A Converters (Cont'd)

Bits-Code	Setting Time (±½LSB) µs	Linearity Error %FPS	Supply Voltage	Device	Source	Line
11 Bit (10 Bit plus Sign)						
	1.5*	0.4	±(12-18)	(Cont'd.)		
				DAC-05G	**PMI** (913)	
11 Bit (10 Bit plus sign) Offset Binary, Multiplying						
	15*	0.05	±15,5	MN413	Micro Net	
				MN413H	† Micro Net	
	45*	0.05	±15,5	MN412	Micro Net	
				MN412H	† Micro Net	70
11 Bit plus sign dynamic range (7 Bit plus Sign Format)						
	0.5	—	±15	AM6071C	AMD	
				AM6071M	†AMD	
				AM6073C	AMD	
				AM6073M	†AMD	
	5*	—	±15	**DAC-87C**	**PMI** (935)	
				DAC-87E	**PMI** (935)	
12 Bit BCD, Multiplying						
	0.5*	0.02	-(10-18), 5-18	**DAC-30A**	**†PMI** (930)	
		0.05	-(10-18),5-18	**DAC-30B**	**†PMI** (930)	80
				DAC-30E	**PMI** (930)	
			5/15	DAC-HA12D	Datel	
				DAC-HA12DM	†Datel	
		0.1	-(10-18),5-18	**DAC-30F**	**PMI** (930)	
	1.5	0.01	-15,5-15	**SSS562S/BCD**	**†PMI** (930,955)	
		0.05	-15,5-15	**SSS562A/BCD**	**PMI** (930,955)	
				SSS562K/BCD	**PMI** (930,955)	90
	3.0	0.01	-15,5-15	AD562A/BCD	AD	
				AD562K/BCD	AD	
				AD562S/BCD	†AD	
				AN562I/BCD	Analogic	
				AN562S/BCD	†Analogic	
		0.05	-15,5-15	AN562A/BCD	Analogic	
				AN562K/BCD	Analogic	
12-Bit BCD	0.15/5*	0.05	±15,5	DAC-S-CCD	DDC	
	0.3/3*	0.025	±15	**DAC-HZ12D**	**Datel** (392)	
				DAC-HZ12DMM	**†Datel** (392)	100
		0.05	±15,5	DAC80/CCD	Burr-Brown	
				DAC85/CCD	Burr-Brown	
				DAC85C/CCD	Burr-Brown	
				DAC335-3D	† Hybrid Sys.	
				DAC80/CCD	Micro Net	
				DAC85/CCD	Micro Net	
				DAC1286	†National	
				DAC1286C	National	
		0.1	±15,5	DAC1287C	National	
	0.5	0.05	±15	MN311	Micro Net	110
				MN311H	† Micro Net	
	15	0.05	±15	DAC349C-3D	Hybrid Sys.	
				DAC349B-3D	† Hybrid Sys.	
	1.2	0.025	-15,5-15	AD563K/BCD	AD	
				AD563S/BCD	†AD	
				AD563T/BCD	†AD	
		0.05	-15,5-15	AD563J/BCD	AD	
	5	0.01	±15,5	DA1202	† National	
				DA1202C	National	
				DA1203	†National	120

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits-Code	Setting Time (±½LSB) µs	Linearity Error %FPS	Supply Voltage	Device	Source	Line
12-Bit BCD	5	0.01	±15,5	(Cont'd.) DA1203C	National	
	23	0.05	±15	MN3212	Micro Net	
12 Bit BCD with latches	4	0.025	±15,5	**DAC-HK12D**	**Datel (390)**	
				DAC-HK12DMM	**† Datel (390)**	
12 Bit Binary, Multiplying	0.4	0.006	-15,5-15	**HI562-2**	**† Harris (444)**	
				HI562-8	**† Harris (444)**	
				HI562-4	**Harris (444)**	10
				HI562-5	**Harris (444)**	
	0.5*	0.05	5-15	AD7531L	AD	
		0.1	5-15	AD7531K	AD	
		0.2	5-15	AD7531J	AD	
	1.5	0.006	-15,5-15	**SSS562S/BIN**	**† PMI (930,955)**	
		0.0125	-15,5-15	**SSS562A/BIN**	**PMI (930,955)**	
				SSS562K/BIN	**PMI (930,955)**	20
				DAC331M-12	† Hybrid Sys.	
	3.5	0.006	-15,5-15	AD562S/BIN	† AD	
				AN562S/BIN	† Analogic	
		0.012	-15,5-15	AD562A/BIN	AD	
				AD562K/BIN	AD	
				AN562A/BIN	Analogic	
12-Bit Binary	0.5	0.0125	±15	MN312	Micro Net	
				MN312H	† Micro Net	
	1	0.025	±5	MN312R	Micro Net	
	1.2*	0.006	-15,5-15	AD563K/BIN	AD	30
				AD563S/BIN	† AD	
				AD563T/BIN	† AD	
		0.012	-15,5-15	AD563J/BIN	AD	
	70	0.05	±15	MN371	Micro Net	
				MN371H	† Micro Net	
12 Bit Binary, Pulse Output	4ms	0.0125	±10	6202	Intersil	
12 Bit Binary/Offset Binary, Multiplying	0.2	0.012	±15	DAC391-12	Hybrid Sys.	
				DAC391B-12	Hybrid Sys.	40
			5/15	DAC-HA12B	Datel	
				DAC-HA12BM	† Datel	
12 Bit Binary/Offset Binary	0.05	0.01	±15	**DAC-HF12B**	**Datel (389)**	
	0.2/2	0.0125	±15	4058	† Teledyne P	
	15	0.0125	±15	DAC349-12	Hybrid Sys.	
				DAC349B-12	† Hybrid Sys.	
	30*	0.012	±15	DA4000	HyComp	
	75	0.024	±15	872-D1	† Beckman	
		0.05	±15	872-D2	† Beckman	50
12 Bit Binary/Offset Binary/Two's Complement with latches	4	0.012	±15,5	**DAC-HK12B**	**Datel (390)**	
				DAC-HK12BMM	**† Datel (390)**	
12 Bit Binary/Offset Binary and Complements, Multiplying	0.5*	0.05	5-15	AD7521L	AD	
				AD7521U	† AD	

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D/A Converters (Cont'd)

Bits-Code	Setting Time (±½LSB) µs	Linearity Error %FPS	Supply Voltage	Device	Source	Line
12 Bit Binary/Offset Binary and Complements, Multiplying	0.5*	0.05	5-15	(Cont'd.) AD7521L	Intersil	60
				AD7521U	† Intersil	
				AD7531L	Intersil	
				MPS7521L	Micro Power	
				MPS7521U	† Micro Power	
		0.1	5-15	AD7521K	AD	
				AD7521T	† AD	
				AD7521K	Intersil	
				AD7521T	† Intersil	
				AD7531K	Intersil	
				MPS7521K	Micro Power	70
				MPS7521T	† Micro Power	
		0.2	5-15	AD7521J	AD	
				AD7521S	† AD	
				AD7521J	Intersil	
				AD7521S	† Intersil	
				AD7531J	Intersil	
				MPS7521J	Micro Power	
				MPS7521S	† Micro Power	
	3	0.012	5-10/15	DAC331C-12	Hybrid Sys.	
				DAC331M-12	† Hybrid Sys.	80
12 Bit Complementary Binary	2*	0.0125	±15	DAC345I-12	Hybrid Sys.	
	3	0.0125	±15,10	MN366	Micro Net	
				MN366H	† Micro Net	
	5*	0.0125	±15	DAC346V-12	Hybrid Sys.	
	7	0.0125	±15,10	MN362	Micro Net	
				MN362H	† Micro Net	
	35	0.0125	±15	MN3210	Micro Net	
12 Bit Binary/Complementary Binary, Multiplying	0.75*	0.006	-(10-18),5-18	**DAC-12A**	**† PMI (930)**	90
		0.01	-(10-18),5-18	**DAC-12B**	**† PMI (930)**	
				DAC-12F	**PMI (930)**	
		0.02	-(10-18),5-18	**DAC-12F**	**† PMI (930)**	
	5	0.01	-15,5	M/DA2000	HyComp	
		0.05	-15,5	M/DA2005	HyComp	
12 Bit Complementary Binary/Offset Binary	5*	0.0125	±15	MN3850	Micro Net	
				MN3850H	† Micro Net	
12 Bit Complementary Offset Binary	1*	0.0125	±15	DAC345I-12	Hybrid Sys.	100
	3	0.0125	±15,10	MN364	Micro Net	
				MN364H	† Micro Net	
	7	0.0125	±5,10	MN360	Micro Net	
				MN360H	† Micro Net	
	35	0.0125	±15	MN3211	Micro Net	
12 Bit Complementary Binary/Comp. Offset Binary/Comp. Two's Complement	0.3/3*	0.012	±15,5	877-15I	Beckman	
				877-15V	Beckman	
				877-80I	Beckman	110
				877-80V	Beckman	
				877-85I	Beckman	
				877-85V	Beckman	
				DAC80/CBI	Burr-Brown	
				DAC85/CBI	Burr-Brown	
				DAC85LD/CBI	Burr-Brown	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits-Code	Setting Time (±½LSB) µs	Linearity Error %FPS	Supply Voltage	Device	Source	Line
12 Bit Complementary Binary/Comp. Offset Binary/Comp. Two's Complement						
	0.3/3*	0.012	±15,5	(Cont'd.)		
				DAC335-12	† Hybrid Sys.	
				DAC80/CBI	Micro Net	
				DAC85/CBI	† Micro Net	
				DAC1285	† National	
				DAC1285C	National	
				DAC-HZ12B	**Datel** (392)	
				DAC-HZ12BMM	**† Datel** (392)	10
		0.024	±15,5	DAC1280C	National	
			±12	DAC80/CBI	Burr-Brown	
12 Bit Complementary Binary/Comp. Offset Binary						
	0.15/5*	0.0122	±15,5	DAC-S-CBI	DDC	
	0.05	0.0125	-1.3,±15	ADH-030-12	DDC	
		0.025	-1.3,±15	ADH-030-11	DDC	
		0.05	-1.3±15	ADH-030-10	DDC	
		0.2	-1.3±15	ADH-030-8	DDC	
	5	0.0122	±15,5	DA1200	† National	
				DA1200C	National	20
		0.048	±15,5	DA1201	† National	
				DA1201C	National	
12 Bit Complementary Binary/Comp. Offset Binary with latches						
	5*	0.0125	±15,5	MN3860	Micro Net	
				MN3860H	† Micro Net	
12 Bit Offset Binary						
	5*	0.0125	±15	DAC346V-12	Hybrid Sys.	
	70	0.0125	±15	MN370	Micro Net	
				MN370H	† Micro Net	30
12 Bit Two's Complement						
	4	0.012	±15,5	**DAC-HK12B-2**	**Datel** (390)	
				DAC-HK12BM-2	**† Datel** (390)	
12 Bit plus sign dynamic range (7 Bit plus Sign format)						
	0.5	—	±15	AM6070C	AMD	
				AM6070M	† AMD	
				AM6072C	AMD	
				AM6072M	† AMD	
	0.5*	—	±15	**DAC-76**	**† PMI** (935)	
				DAC-86	**PMI** (935)	40
13 Bit Binary, Multiplying						
	20	—	-25,±15,5	877-69C	Beckman	
				877-69M	† Beckman	
13 Bit Modified Two's Complement						
	1.6	0.0125	±15,5	SDAC-12	DDC	
		0.025	±15,5	SDAC-11	DDC	
		0.05	±15,5	SDAC-10	DDC	
14 Bit Binary/Offset Binary, Multiplying						
	0.5*	0.006	5/15	**DAC-HA14B**	**Datel** (388)	
				DAC-HA14BM	**† Datel** (388)	50
	8	0.0125	±15	DAC-U-12	DDC	
		0.025	±15	DAC-U-11	DDC	
16-Bit BCD	8*	0.07	±15,5	DAC327	Hybrid Sys.	
	15*	0.005	±15	**DAC-HP16D**	**Datel** (391)	
				DAC-HP16DMM	**† Datel** (391)	

(Continued)

D/A Converters (Cont'd)

Bits-Code	Setting Time (±½LSB) µs	Linearity Error %FPS	Supply Voltage	Device	Source	Line
16-Bit BCD	(Cont'd.)					
	30	0.01	±15,5	DAC327-4-BCD	Hybrid Sys.	
	35	0.005	±15	MN3300	Micro Net	
	50/100*	0.003	±15,5	DAC70/CCD	Burr-Brown	
		0.005	±15,5	DAC70C/CCD	Burr-Brown	60
16-Bit Binary	35	0.003	±15	MN3310	Micro Net	
16 Bit Complementary Binary						
	50/100*	0.003	±15,5	DAC70/CSB	Burr-Brown	
		0.005	±15,5	DAC70C/CSB	Burr-Brown	
16 Bit Complementary Offset Binary						
	50/100*	0.003	±15,5	DAC70/COB	Burr-Brown	
		0.005	±15,5	DAC70C/COB	Burr-Brown	
16 Bit Complementary Binary/Comp. Offset Binary						
	35*	0.003	±15	**DAC-HP16B**	**Datel** (391)	
				DAC-HP16BMM	**† Datel** (391)	70

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Display Drivers

Function	Device	Source	Line
Display Drivers			
Display Driver, 4 Digit (Stores segment and address data, drives 7 8 segment digits)	MM74C911	National	
Display Driver, 6 Digit (Stores segment and address data, drives 7 8 segment digits)	MM74C912	National	
	MM74C913	National	
BCD to 7 Segment LED Driver Adjustable Current	DD700	Beckman	
	DS7858	National	10
	DS8858	National	
BCD to 7 Segment LED Decoder/Driver, Constant Current	NE586	Signetics	
	NE587	Signetics	
	DS8857	National	
BCD to 7 Segment LED Latch/Decoder/Driver, with ripple blanking	F4734BC	Fairchild	
	F4734BM	† Fairchild	20
BCD (Hexadecimal) to 7 Segment LED Decoder/Driver, Constant Current, with Latch	9368C	Fairchild	
	MD4368B	† Mitel	
	MD4368BE	Mitel	
BCD (Hexadecimal) to 7 Segment LED Decoder/Driver	M54405	Mitsubishi	
BCD (Hexadecimal) to 7 Segment LED Decoder/Driver, with Latch	MD4311B	† Mitel	
	MD4311E	Mitel	30
	DS8673	National	
BCD to 7 Segment LED Decoder/Driver with Latch, output 0 9, , E, H, L, P	9374C	Fairchild	
	DS8674	National	
BCD to 7 Segment Decoder/Driver, Active High, Resistive Pull Up	54LS48	† Fairchild	
	74LS48	Fairchild	40
	5448	† Fairchild	
	7448	Fairchild	
	9307C	Fairchild	
	9307M	† Fairchild	
	ITT5448	† ITT	
	ITT7448	ITT	
	M53248	Mitsubishi	
	MC5448	† Motorola	
	MC7448	Motorola	50
	MC8307	Motorola	
	MC9307	† Motorola	
	DM5448	† National	
	DM7448	National	
	DM54LS48	† National	
	DM74LS48	National	
	DM54LS248	† National	
	DM74LS248	National	
	DS7856	† National	
	DS8856	National	60
	5448	† Signetics	
	7448	Signetics	
	N8T05	Signetics	
	S8T05	† Signetics	
	SN5448	† TI	
	SN7448	TI	
	SN54248	† TI	
(Continued)			

Function	Device	Source	Line
Display Drivers (Cont'd)			
BCD to 7 Segment Decoder/Driver, Active High, Resistive Pull Up (Cont'd.)	SN74248	TI	70
	SN54LS48	† TI	
	SN74LS48	TI	
	SN54LS248	† TI	
	SN74LS248	TI	
BCD to 7 Segment Decoder/Driver, Active High, Open Collector	5449	† Fairchild	
	7449	Fairchild	
	54LS49	† Fairchild	
	74LS49	Fairchild	80
	MC5449	† Motorola	
	MC7449	Motorola	
	DM54LS49	† National	
	DM74LS49	National	
	DM54LS249	† National	
	DM74LS249	National	
	N8T06	Signetics	
	S8T06	† Signetics	
	SN5449	† TI	
	SN7449	TI	90
	SN54249	† TI	
	SN74249	TI	
	SN54LS49	† TI	
	SN74LS49	TI	
	SN54LS249	† TI	
	SN74LS249	TI	
BCD (Hexadecimal) to 7 Segment Decoder/Driver with Latch Active Low, Open Collector	9370C	Fairchild	
BCD to 7 Segment Decoder/Driver Active Low, Open Collector	MC4039	Motorola	100
	N8T04	Signetics	
	S8T04	† Signetics	
BCD to 7 Segment Decoder/Driver, Active Low, Open Collector, 15v Output	54LS47	† Fairchild	
	74LS47	Fairchild	
	5447	† Fairchild	
	7447	Fairchild	110
	9317BC	Fairchild	
	9317BM	† Fairchild	
	HD2532	Hitachi	
	ITT5447A	† ITT	
	ITT7447A	ITT	
	M53247	Mitsubishi	
	M54406	Mitsubishi	
	MC5447	† Motorola	
	MC7447	Motorola	120
	DM5447A	† National	
	DM7447A	National	
	DM54LS47	† National	
	DM74LS47	National	
	DM54LS247	† National	
	DM74LS247	National	
	µPB7447	NEC America	
	5447	† Signetics	
	7447	Signetics	
	383A/C	Teledyne S	
	383B/M	† Teledyne S	130
	SN5447A	† TI	
	SN7447A	TI	
	SN54247	† TI	
	SN74247	TI	
	SN54LS47	† TI	
	SN74LS47	TI	
(Continued)			

Function	Device	Source	Line
Display Drivers (Cont'd)			
BCD to 7 Segment Decoder/Driver, Active Low, Open Collector, 15v Output (Cont'd.)	SN54LS247	† TI	
	SN74LS247	TI	140
	SN54LS347	† TI	
	SN74LS347	TI	
BCD to 7 Segment Decoder/Driver, Active Low, Open Collector, 30v Output	5446	† Fairchild	
	7446	Fairchild	
	9317CC	Fairchild	
	9317CM	† Fairchild	
	HD2553	Hitachi	
	ITT5446A	† ITT	150
	ITT7446A	ITT	
	MC5446	† Motorola	
	MC7446	Motorola	
	DM5446A	† National	
	DM7446A	National	
	µPB7446	NEC America	
	5446	† Signetics	
	7446	Signetics	
	SN5446A	† TI	
	SN7446A	TI	160
	SN54246	† TI	
	SN74246	TI	
BCD to 7 Segment Decoder/Driver, for gas discharge displays	384A/C	Teledyne S	
	384B/M	† Teledyne S	
BCD to 7 Segment Decoder, Driver for lamps and relays	CD2500	RCA	
	CD2501	RCA	170
	CD2502	RCA	
	CD2503	RCA	
BCD to 7 Segment Latch/Decoder/Driver (CMOS with Bipolar Output)	F4511BC	Fairchild	
	F4511BM	† Fairchild	
	SIL4511B	† Mitel	
	SIL4511BE	Mitel	
	MC14511BA	† Motorola	
	MC14513BA	† Motorola	180
	MC14513BC	Motorola	
	MC14511BC	Motorola	
	CD4511BC	National	
	CD4511BM	† National	
	CD4511B	† RCA	
	CD4511BE	RCA	
	SCL4511B	† SSS	
	SCL4511BE	SSS	
	CM4511B	† Solitron	
	CM4511BE	Solitron	190
	TP4511B	TI	
BCD to 7 Segment Decoder/Driver, for Liquid Crystal Displays	SIL4055B	† Mitel	
	SIL4055BE	Mitel	
	CD4055B	† RCA	
	CD4055BE	RCA	
BCD to 7 Segment Latch/Decoder/Driver, for Liquid Crystal Displays	MC14543BA	† Motorola	200
	MC14543BC	Motorola	

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Display Drivers (Cont'd)

Function	Device	Source	Line
Display Drivers (Cont'd)			
BCD to 7 Segment Latch/Decoder/Driver (Strobed Latch), for Liquid Crystal Displays			
	LS7100	LSI Comp	
	SIL4056B	†Mitel	
	SIL4056BE	Mitel	
	MC14543BA	†Motorola	
	MC14543BC	Motorola	
	CD4056B	†RCA	
	CD4056BE	RCA	
	SCL4543A	SSS	
BCD to 7 Segment Decoder/Driver, for Liquid Crystal Displays			10
	SIL4055B	†Mitel	
	SIL4055BE	Mitel	
	CD4055B	†RCA	
	CD4055BE	RCA	
4 Digit Liquid Crystal Display Driver			
	SCL5424	SSS	
	SCL5441	SSS	
4 Digit Liquid Crystal Display Driver, Multiplexed BCD to LCD Decoder/Driver, AC Drive			20
	HMUX0190	†Hughes	
	DF411	**Siliconix** (536)	
30 Bit LCD Driver/Register			
	MD4330B	†Mitel	
	MD4330BE	Mitel	
Hex High Voltage Indicator Driver Open Collector (to 55v)			
	HD536	Harris	
Hex TTL to LED Bulb Driver, with Latch			30
	DS8859	National	
	DS8869	National	
7 Digit/Segment MOS to Fluorescent Display Driver			
	XR2271	Exar	
8 Digit/Segment Fluorescent Display Driver			
	μPB249	NEC America	
	UDN-6118A	Sprague	
	UDN-6128A	Sprague	
4 Digit Gas Discharge Display Anode Driver			
	UDN-6144A	Sprague	
5 Digit Gas Discharge Display Anode Driver			40
	UHP-490	Sprague	
6 Digit Gas Discharge Display Anode Driver			
	DS7891	†National	
	DS8891	National	
	UDN-6164A	Sprague	
	UHP-491	Sprague	
	UHP-495	Sprague	
	SN75481	TI	
7 Digit Gas Discharge Display Anode Driver			
	MC3490	Motorola	50
	MC3494	Motorola	
8 Digit Gas Discharge Display Anode Driver			
	DS7887	†National	
	DS8887	National	
	DS7897	†National	
	DS8897	National	
	UDN-6184A	Sprague	
9 Digit Gas Discharge Display Anode Driver			
	NE585	Signetics	
5 Segment Gas Discharge Display Cathode Driver			60
	UHP-480	Sprague	
7 Segment Gas Discharge Display Cathode Driver			
	DS7885	†National	
	(Continued)		

Function	Device	Source	Line
Display Drivers (Cont'd)			
7 Segment Gas Discharge Display Cathode Driver (Cont'd.)			
	DS8885	National	
	UHP-481	Sprague	
7 Segment Gas Discharge Display Cathode Driver, with BCD Decoder			
	DS7880	†National	
	DS8880	National	70
	DS8884A	National	
	DS8880	Signetics	
	SN75480	TI	
	SN75484	TI	
8 Segment Gas Discharge Display Cathode Driver			
	SN75484	TI	
	MC3491	Motorola	
	MC3492	Motorola	
	DS7889	†National	
	DS8889	National	80
	UDN-7180A	Sprague	
	UDN-7183A	Sprague	
	UDN-7184A	Sprague	
	UDN-7186A	Sprague	
	UHP-482	Sprague	
9 Segment (Panaplex) Display Cathode Driver			
	NE584	Signetics	
12 Digit Digitron Driver			
	EA7050	EA	
	EA7052	EA	90
Plasma Display Controller and ASCII Keyboard Interface			
	CY-300	Cybernetic	
4 Digit CMOS to LED Cathode Driver			
	MCC1486	Motorola	
	MCC1487	Motorola	
	DS8650	National	
	DS8658	National	
7 Segment CMOS to LED Driver			
	DS8651	National	100
	DS8659	National	
6 Digit MOS to LED Cathode Driver			
	9664C	Fairchild	
	9664AC	Fairchild	
	9664BC	Fairchild	
	75492C	Fairchild	
	75492AC	Fairchild	
	75492BC	Fairchild	
	ITT492	ITT	
	ITT500	ITT	110
	MC75492	Motorola	
	DS75492	National	
	DS8870	National	
	DS8877	National	
	DS8892	National	
	NE582	Signetics	
	D140	**Siliconix** (962)	
	SN75492	TI	
	SN75492A	TI	
	SN75494	TI	120
7 Digit MOS to LED Cathode Driver			
	ITT546A	ITT	
	DS8844	National	
	SN75497	TI	
7 Digit MOS TO LED Cathode Driver, with low battery indicator			
	DS8866	National	
	DS8977	National	

Function	Device	Source	Line
Display Drivers (Cont'd)			
8 Digit MOS to LED Cathode Driver			
	HD2903	Hitachi	130
	ITT508	ITT	
	ITT514	ITT	
	DS8863	National	
	DS8865	National	
	DS8871	National	
	DS8963	National	
9 Digit MOS to LED Cathode Driver			
	ITT548	ITT	
	ITT558	ITT	
	DS8855	National	140
	DS8872	National	
	DS8973	National	
	DS8974	National	
	DS8976	National	
	SN75498	TI	
9 Digit MOS to LED Cathode Driver, with low battery indicator			
	DS8864	National	
	DS8873	National	
9 Digit MOS to LED Cathode Driver with shift register decoding			150
	DS8874	National	
	DS8876	National	
	DS8879	National	
12 Digit MOS to LED Cathode Driver (for National Calculators)			
	DS8868	National	
14 Digit Decoder/Driver			
	DS8665	National	
	DS8666	National	160
14 Digit Decoder/Driver, with low battery indicator			
	DS7664	†National	
	DS8664	National	
4 Segment MOS to LED Anode Driver			
	75491C	Fairchild	
	75491AC	Fairchild	
	75491BC	Fairchild	
	ITT491	ITT	
	ITT501	ITT	
	MC75491	Motorola	170
	DS7895	†National	
	DS8895	†National	
	DS75491	National	
	DS75493	National	
	SN75491	TI	
	SN75493	TI	
5 Segment MOS to LED Anode Driver			
	DS8861	National	
8 Segment MOS to LED Anode Driver			
	HD2902	Hitachi	180
	MC676	Motorola	
	DS8867	National	
Bargraph LED Display Driver			
	LB1405	Sanyo	
	UAA170	Siemens	
	UAA180	Siemens	
Bargraph (Gas Discharge) Display Driver			
	NE580	Signetics	
BCD To Decimal Decoder/Driver (Nixie Driver)			
	5441	†Fairchild	190
	7441	Fairchild	
	HD2518	Hitachi	
	M53241	Mitsubishi	
	(Continued)		

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Display Drivers (Cont'd)

Function	Device	Source	Line
Display Drivers (Cont'd)			
BCD To Decimal Decoder/Driver (Nixie Driver) (Cont'd.)			
	MC676	Motorola	
	DM5441A	† National	
	DM7441A	National	
	H158	SGS	
	382A/C	Teledyne S	
	382B/M	† Teledyne S	
BCD To Decimal Decoder/Driver with Blanking (for cold cathode indicator tubes)			
	74141	Fairchild	10
	HD2558	Hitachi	
	MC54141	† Motorola	
	MC74141	Motorola	
	DM54141	† National	
	DM74141	National	
	μPB74141	NEC America	
	SN74141	TI	
Quad Plasma Display Axis Driver			
	SN75426	TI	
	SN75427	TI	20
BCD To Decimal Decoder/Driver (for lamps)			
	380A/C	Teledyne S	
	380B/M	† Teledyne S	
	381A/C	Teledyne S	
	381B/M	† Teledyne S	
Lamp Driver; See below and various high current drivers under Interface Memory and Peripheral Drivers			
Lamp Drivers (to 90v, 2.0a)			
	S55V01	† Siliconix	
	S55V02	† Siliconix	30
	S55V11	† Siliconix	
	S55V12	† Siliconix	
	S55V21	† Siliconix	
	S55V22	† Siliconix	
	S75V01	Siliconix	
	S75V02	Siliconix	
	S75V03	**Siliconix** (542)	
	S75V11	Siliconix	
	S75V12	Siliconix	
	S75V21	Siliconix	40
	S75V22	Siliconix	
Lamp Driver			
	CSR301	Teledyne C	
4 Channel Incandescent Lamp Driver			
	CLD4	Teledyne C	

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Error Checking Circuits

Function	Max. Serial Data Rate MHz	Supply Voltage	Device	Source
Error Checking Circuits				
CRCC Generator	10	5	9401C 9401M	Fairchild † Fairchild
		10/5	9411C	Fairchild
	3	5	MC8500	Motorola
	10	60ma, 5v	8X01	Signetics
Deskew-Queue Register	3*	5	MC8520	Motorola
	10*	200ma	8X03 8X04	Signetics Signetics
Error Detection/Correction Circuit (ECL)	—	-5.2	MC10163 MC10193	Motorola Motorola
Error Pattern Register	3	5	MC8501	Motorola
LRCC Data Register	3	5	MC8502	Motorola
Single Error Hamming Code Detector and Generator	—	5	MC4041	Motorola
Polynominal Generator	4*	5	MC8506	Motorola
Universal Polynomial Generator	3.5*	5	MC8503	Motorola
Universal Polynomial 4 Bit Generator	17*	5	MC8504	Motorola

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Keyboard Encoder-Decoders

No. of Keys	No. of Output Bits	Code	Max. Clock Rate KHz	Supply Voltage	Comments	Device	Source
Keyboard Encoder-Decoders							
16	4	1 of 16	—	5	Strobe output, Key rollover output, 2 of 8 keyboard to binary encoder, one of four row inputs and column inputs (telephone key pads) give binary output, strobe.	**HD0165** MC14419	**Harris (453)** Motorola
		Binary	—	3-15	2 key rollover, 3 state output	HD54C922 HD74C922 MM54C922 MM74C922	†Harris Harris †National National
20	5	Binary	—	3-15	2 key rollover, 3 state output	HD54C923 HD74C923 MM54C923 MM74C923	†Harris Harris †National National
28	8 plus Parity	Mask, Programmable	50	-12,5	4 x 8 matrix, N Key rollover, 2 Levels. Independent or expander for MCS1007. Repeat.	MCS1008	MOS
64	8 plus Parity	Mask, Programmable	50	-12,5	Odd Parity, N Key Rollover, 9 x 8 matrix, 4 levels Repeat.	MCS1007	MOS
76	9	Mask Programmable	—	-(12-18), 5	To 4 independent 9 Bit codes per switch	MM5746	National
	10	Mask Programmable	—	-(12-18), 5	To 4 independent 10 Bit codes per switch	MM5745	National
88	8 plus Parity	Mask, Programmable	100	-12,5	Programmable parity, strobe width, strobe delay. Two key rollover. 8 x 11 matrix, 3 levels.	AY5-2376 KR2376	GI SMC
90	9	Mask, Programmable	200	-12,5	Programmable strobe width. 9 x 10 matrix. N or two key rollover. 4 levels. Repeat.	MM5740	National
	10	Mask, Programmable	50	-12,5	Two units give 180 keys. 9 x 10 matrix, N key rollover, 4 levels. Repeat.	MCS1009	MOS
			100	-12,5	9 x 10 matrix, 4 Mode, 2 or N key rollover	AY5-3600 KR3600	GI SMC
		ARS33/Baudot/Logical Bit Pairing/Typewriter Pairing	100	-12,5	9x10 matrix, N key rollover or lockout	TMS5001	TI
		ASCII	100	±5,12	—	μPD364-02	NEC Micro

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Line Circuits

No. Per Device	Output	Party Line	Power Supply	Comments	Device	Source
Line Drivers-Single Ended						
2	±4 to 6v	No	±9 to ±15	RS232, RS432, CCITT V.26, V.28	9636C	Fairchild
					9636M	† Fairchild
	±6v	No	±12	4 Input; RS232B, C; MIL188	N8T15	Signetics
	±8v	No	±12	RS232C; MIL188; CCITT V.24	55150M	† Fairchild
					75150	Fairchild
					M54650	Mitsubishi
					DS75150	National
					RC75150	Raytheon
					RM55150	† Raytheon
					SN75150	TI
	TTL	No	5,12	130 Ohm Twisted Pair	9621C	AMD
					9621M	† AMD
					9621	Fairchild
					9621M	† Fairchild
					RC9621	Raytheon
					RM9621	† Raytheon
	High Current	Yes	5	Emitter Follower for Coax/Twisted Pair	μA8T13C	Fairchild
					μA8T13M	† Fairchild
					55121M	† Fairchild
					75121	Fairchild
					MC8T13	Motorola
					DS55121	† National
					DS75121	National
					N8T13	Signetics
					S8T13	† Signetics
					N8T13	TI
					SN55121	† TI
					SN75121	TI
				Coax/Twisted Pair; IBM360, 370	μA8T23C	Fairchild
					μA8T23M	† Fairchild
					55123M	† Fairchild
					75123	Fairchild
					MC8T23	Motorola
					DS75123	National
					N8T23	Signetics
					N8T23	TI
					S8T23	† TI
					SN75123	TI
3	±6v	No	±12	RS232B/C, CCITT, MIL188	9616C	AMD
					9616M	† AMD
					9616	Fairchild
					9616E	Fairchild
					9616M	† Fairchild
4	±6 to 9v	No	±9 to ±15	RS232C, CCITT V.24	1488	AMD
					XR1488	Exar
					μA1488	Fairchild
					HD1488	Harris
					ITT1488	ITT
					MC1488	Motorola
					DS1488	National
					RC1488	Raytheon
					MC1488	Signetics
					SG1488	Silicon G
					MC1488	TI
					SN75188	TI
	±5 to ±7	No	±12	RS232C, CCITT V.24	AM2616C	AMD
					AM2616M	† AMD
	TTL	No	5	Active Pull-Up	AM2614C	AMD
					AM2614M	† AMD
		Yes	5	Three-State	RC8T09	Raytheon
					RM8T09	† Raytheon
					N8T09	Signetics
					S8T09	† Signetics
				2-Input NAND, 80 ma	96101C	Fairchild

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Common Mode Voltage	Supply Voltage	Comments	Device	Source
Line Receivers - Differential (Cont'd)						
2	±0.5/2	(Cont'd.)				
		±0/12	5,12	±12 v CMV	9620C	AMD
					9620C	Fairchild
	±0.3/0.3	±10/15	5	±15v CMV, Response Control	DS78L20	† National
					DS88L20	National
	±0.5/1	±0/15	5	15 v CMV, Response Control	9615C	AMD
					9615M	† AMD
					9615C	Fairchild
					9615M	† Fairchild
					ITT9615-1	† ITT
					ITT9615-5	ITT
					9615C	TI
				Twisted Pair, ±15v CMV, Response Control	DM7820	† AMD
					DM8820	AMD
					DS78C20	† National
					DS88C20	National
					DS7820	† National
					DS8820	National
					DS7820	† Signetics
					DS8820	Signetics
		±5/15	5	±15v CMV	9613C	Fairchild
					9613M	† Fairchild
		±3/15	5	Twisted Pair, ±3/15 v CMV, Response Control	DM7820A	† AMD
					DM8820A	AMD
					DS7820A	† National
					DS8820A	National
					DS7820A	† Signetics
					DS8820A	Signetics
					DS7820	† TI
					DS8820	TI
					SN55182	† TI
					SN75182	TI
	±0.5/3	±25	±12	Adjusts RS232C/MIL-188, ±25 v CMV, Hysteresis	9627C	Fairchild
					9627M	† Fairchild
					SN75152	TI
	±2	±10	-10,5	130 Ohm Termination	9622C	Fairchild
					9622M	† Fairchild
					RC9622	Raytheon
					RM9622	† Raytheon
	±0.010	±3	±5	10 mv, MOS Sense, Active Pull-up	SN75207	AMD
					55207M	† Fairchild
					75207C	Fairchild
					ITT75207	ITT
					DS75207	**National (504)**
					75S207	Signetics
					SN75207	TI
				75207 with Diode Protected Input Stage	SN75207B	TI
				10 mv, MOS Sense, Three-State	DS3604	AMD
					DS3604	**National (504)**
				10 mv, MOS Sense, Open Collector	SN75208	AMD
					55208M	† Fairchild
					75208C	Fairchild
					ITT75208	ITT
					DS75208	**National (504)**
					75S208	Signetics
					SN75208	TI
				75208 with Diode Protected Input Stage	SN75208B	TI
	±0.025	±3	±5	25 mv, Active Pull-up	55107AM	† Fairchild
					75107AC	Fairchild
					ITT55107A	† ITT
					ITT75107A	ITT
					MC55107	† Motorola

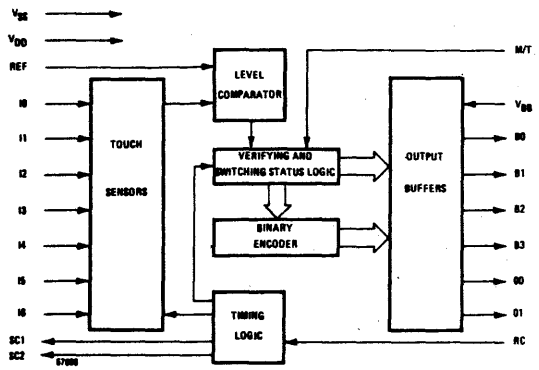
(Continued)

† Military Temperature Range (−55° to 125°C)

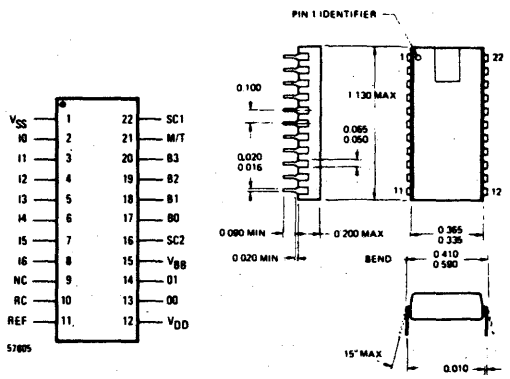
* Typical Values

Multiplexed TouchControl™ Interface

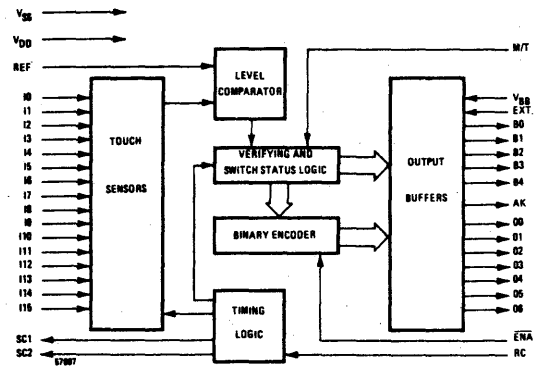
ADVANCED PRODUCT DESCRIPTION



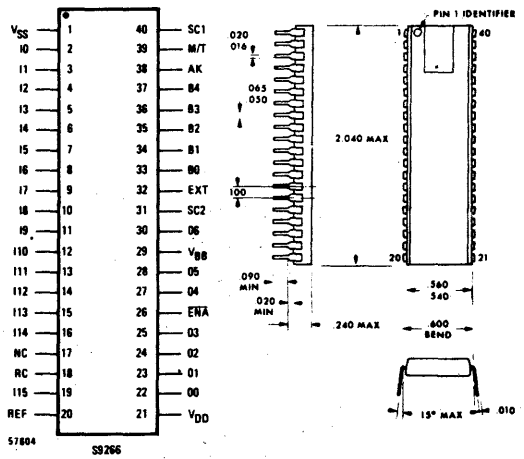
BLOCK DIAGRAM – S9262 (14 SWITCHES)



PIN/PACKAGE CONFIGURATION – S9262



BLOCK DIAGRAM – S9266 (32 SWITCHES)



PIN/PACKAGE CONFIGURATION – S9266

FEATURES

- Simplifies design of Touch-sensitive switches
- Interfaces with up to 32 touch switches
- Eliminates contact noise
- Comparator sensing permits use with wide variety of touch switch configurations
- Binary outputs provided
- Outputs are TTL compatible
- Permits design of totally isolated touch surfaces, facilitating UL approval

FUNCTIONAL DESCRIPTION

Both circuits multiplex the inputs to increase the number of TouchControl switches to which each circuit can connect. All scanning is performed by the internal circuitry with an external RC network used to establish the frequency. The S9262 can connect to a 2x7 switch matrix to interface with 14 TouchControl switches. The S9262 outputs are encoded in binary on four pins. The S9266 can connect to a 2x16 switch matrix to interface with 32 TouchControl switches. Outputs are encoded in binary on five pins. An enable input is provided to allow use of several circuits in one system. All outputs are open drain with the sources connected to the V_{BB} input. This allows easy driving of TTL, CMOS, PMOS or discrete circuitry.

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INTERFACE–Line Circuits (Cont'd)

No. Per Device	Output	Party Line	Power Supply	Comments	Device	Source	
Line Drivers-Single Ended (Cont'd)							
4	TTL	Yes	5	2-Input NAND, 80 ma	(Cont'd.)		
					96101M	† Fairchild	
				4-Input AND, NAND; Three-State	DM7831	† AMD	
					DM8831	AMD	
					DS7831	† National	
					DS8831	National	
					DS7831	† TI	
					DS8831	TI	
				DS7831 w/o Vcc Clamp	DS7832	† National	
					DS8832	National	10
					DS7832	† TI	
					DS8832	TI	
8	· TTL	Yes	5	Three-State (Also see index for 74S244, 74LS244, 67S304, 67LS304)	AM25LS241C	AMD	
					AM25LS241M	† AMD	
					SN54LS241	† AMD	
					SN74LS241	AMD	
					SN54S241	† AMD	
					SN74S241	AMD	
					54LS241	† Fairchild	
					74LS241	Fairchild	20
					ITT74LS241	ITT	
					54LS241	† MMI	
					74LS241	MMI	
					54S241	**† MMI (462)**	
					74S241	**MMI (462)**	
					57LS301	† MMI	
					67LS301	MMI	
					57S301	† MMI	
					67S301	MMI	
					9LS241C	**Raytheon (279)**	
					9LS241M	**† Raytheon (279)**	30
					25LS241C	† Raytheon	
					25LS241M	Raytheon	
					54LS241	**† Raytheon (279)**	
					74LS241	**Raytheon (279)**	
					54S241	† Raytheon	
					74S241	Raytheon	
					74LS241	Signetics	
					SN54LS241	† TI	
					SN74LS241	TI	
					SN54S241	† TI	
					SN74S241	TI	
					SN54LS244	† TI	
					SN74LS244	TI	40
				Three-State, Inverting	AM25LS240C	AMD	
					AM25LS240M	† AMD	
					SN54LS240	† AMD	
					SN74LS240	AMD	
					SN54S240	AMD	
					SN74S240	AMD	
					54LS240	† Fairchild	
					74LS240	Fairchild	
					ITT74LS240	ITT	
					54LS240	† MMI	50
					74LS240	MMI	
					54S240	**† MMI (462)**	
					74S240	**MMI (462)**	
					57LS300	† MMI	
					67LS300	MMI	
					57S300	† MMI	
					67S300	MMI	
					9LS240C	**Raytheon (279)**	
					9LS240M	**† Raytheon (279)**	
					25LS240C	† Raytheon	60
					25LS240M	† Raytheon	
					54LS240	**† Raytheon (279)**	

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Line Circuits (Cont'd)

No. Per Device	Output	Party Line	Power Supply	Comments	Device	Source
Line Drivers-Single Ended (Cont'd)						
8	TTL	Yes	5	Three-State, Inverting	(Cont'd.)	
					74LS240	**Raytheon (279)**
					54S240	† Raytheon
					74S240	Raytheon
					74LS240	Signetics
					SN54LS240	† TI
					SN74LS240	TI
					SN54S240	† TI
					SN74S240	TI
Line-Drivers - Differential						
2	High Current TTL					
		No	5	40 ma, Active Pull-up/Pull-down	9612C	Fairchild
					9612M	† Fairchild
				50 ma, Active Pull-up/Pull-down	9612EC	Fairchild
				40 ma, Open Collector/Active Pull-up	9614C	AMD
					9614M	† AMD
					9614C	Fairchild
					9614M	† Fairchild
					ITT9614-1	† ITT
					ITT9614-5	ITT
					9614C	TI
					SN55114	† TI
					SN75114	TI
		Yes	5	40 ma, Open Collector/Active Pull-up, Three-State	SN55113	† TI
					SN75113	TI
		No	5	40 ma, 4-Input AND, NAND	DM7830	† AMD
					DM8830	AMD
					54S140	† Fairchild
					74S140	Fairchild
					HD74S140	Hitachi
					DM74S140	National
					DS7830	† National
					DS8830	National
					DS7830	† Signetics
					DS8830	Signetics
					54S140	† Signetics
					74S140	Signetics
					DS7830	† TI
					DS8830	TI
					SN54S140	† TI
					SN74S140	TI
					SN55183	† TI
					SN75183	TI
		Yes	5	40 ma, 4-Input AND, NAND; Three-State	DM7831	† AMD
					DM8831	AMD
					DS7831	† National
					DS8831	National
					DS7831	† TI
					DS8831	TI
				DS7831 w/o Vcc Clamp	DM7832	† AMD
					DM8832	AMD
					DS7832	† National
					DS7832	† TI
					DS8832	TI
		No	5	40 ma, RS422	μA9638C	Fairchild
					μA9638M	† Fairchild
					μA9638C	TI
					μA9638M	† TI
					SN75158	TI
		Yes	5	40 ma, RS422, Three-State	SN75159	TI
					DS8832	National

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

INTERFACE-Line Circuits (Cont'd)

No. Per Device	Output	Party Line	Power Supply	Comments	Device	Source
Line-Drivers - Differential (Cont'd)						
2	(Cont'd.)					
	High Current CMOS					
		No	3-15	CMOS 50 ma, 4-Input AND, NAND	MM78C30	† National
					MM88C30	National
	3.5 ma	Yes	±5	Twisted Pair; Level Shifting	SN55109	† AMD
					SN75109	AMD
					55109M	† Fairchild
					75109C	Fairchild
					ITT55109	† ITT
					ITT75109	ITT
					MC75109	Motorola
					DS55109	† National
					DS75109	National
					RC75109	Raytheon
					RM55109	† Raytheon
					SN55109A	† TI
					SN75109A	TI
	6.5ma	Yes	±5	Twisted Pair Level Shifting	SN55110	† AMD
					SN75110	AMD
					55110M	† Fairchild
					75110C	Fairchild
					ITT55110	† ITT
					ITT75110	ITT
					MC75110	Motorola
					DS55110	† National
					DS75110	National
					RM55110	† Raytheon
					RC75110	Raytheon
					SN55110A	† TI
					SN75110A	TI
	18 ma	Yes	±5	Higher current 75110	55112M	† Fairchild
					75112C	Fairchild
					SN75112	TI
3	2 ma	Yes	5	Constant Current	**HD245**	**† Harris (456)**
					HD545	**Harris (456)**
4	11 ma	Yes	±5	Quad 75110	MC3453	Motorola
	High Current TTL					
		No	5	50 ohm lines	74128	Signetics
					SN74128	TI
				75 ohm lines	54128	† Signetics
					SN54128	† TI
		Yes	5	Three-State	DS1688	† National
					DS3688	National
					N8T100	Signetics
					N8T101	Signetics
				RS-422, RS-423, Three-State	MC3487	Motorola
	20 ma	Yes	5	RS-422, Three-State	AM26LS31C	AMD
					AM26LS31M	† AMD
					AM26LS31C	TI
					AM26LS31M	† TI
	High Current CMOS					
		No	3-15	CMOS, 25 ma	MM78C29	† National
					MM88C29	National

See also Drivers under digital logic families

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Common Mode Voltage	Supply Voltage	Comments	Device	Source
Line Receivers - Single Ended						
2	Ref ±0.1v		5	Ext. Reference Adjustable from 1.5 to 3.5v	MC75140	Motorola
					SN55140	†TI
					SN75140	TI
					SN55141	†TI
					SN75141	TI
				Ext. Ref. Adj. 1.5 to 3.5v with optional internal 2.5v Reference	SN55142	†TI
					SN75142	TI
					SN55143	†TI
					SN75143	TI
	0.4 to 2.4	±15	5	Differential Input, Single Ended Data	AM2615C	AMD
					AM2615M	†AMD
	±2.0		5	RS232B	DS7822	†National
					DS8822	National
3	0.7 to 1.7		5	Hysteresis, IBM 360/370	µA8T24C	Fairchild
					µA8T24M	†Fairchild
					55124M	Fairchild
					75124C	Fairchild
					MC8T24	Motorola
					DS75124	National
					N8T24	Signetics
					N8T24	TI
	0.75 to 2.25		5	Hysteresis, RS232C, CCITT V.24	9617C	AMD
					9617M	†AMD
					9617C	Fairchild
	0.8 to 2.0 v		5	Hysteresis, High-Speed	µA8T14C	Fairchild
					µA8T14M	†Fairchild
					55122M	†Fairchild
					75122C	Fairchild
					MC8T14	Motorola
					DS55122	†National
					DS75122	National
					N8T14	Signetics
					S8T14	†Signetics
					N8T14	TI
4	±3/0.8 to 3		5 or 12	RS232C, Hysteresis, Fail Safe Option	55154M	†Fairchild
					75154C	Fairchild
					M54654	Mitsubishi
					DS75154	National
					RM55154	†Raytheon
					RC75154	Raytheon
					SG55154	†Silicon G
					S875154	Silicon G
					SN75154	TI
	0.75 to 1.5v		5	RS232C, Programmable Threshold, Hysteresis	1489	AMD
					µA1489	Fairchild
					HD1489	Harris
					ITT1489	ITT
					MC1489	Motorola
					DS1489	National
					RC1489	Raytheon
					MC1489	Signetics
					SG1489	Silicon G
					SN75189	TI
	0.75 to 2.25		5	RS232C, Programmable Threshold, wider hysteresis than 1489	1489A	AMD
					XR1489A	Exar
					µA1489A	Fairchild
					ITT1489A	ITT
					HD1489A	Harris
					MC1489A	Motorola
					DS1489A	National
					RC1489A	Raytheon
					MC1489A	Signetics
					SG1489A	Silicon G
					MC1489A	TI
	0.97 to 2.65		5	Hysteresis, 120 Ohm System	DS7836	†National

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Common Mode Voltage	Supply Voltage	Comments	Device	Source
Line Receivers - Differential (Cont'd)						
2	±0.025	±3	±5	25 mv, Active Pull-up	(Cont'd.)	
					MC75107	Motorola
					DS55107	**† National (504)**
					DS75107	**National (504)**
					RC75107A	Raytheon
					RM55107A	† Raytheon
					75S107	Signetics
					SN55107A	† TI
					SN75107A	TI
				25 mv, Three-State 55107	DS1603	† AMD
					DS3603	AMD
					DS1603	**† National (504)**
					DS3603	**National (504)**
				25 mv, Open Collector	55108AM	Fairchild
					75108AC	Fairchild
					ITT55108A	† ITT
					ITT75108A	ITT
					MC55108	† Motorola
					MC75108	Motorola
					DS55108	**† National (504)**
					DS75108	**National (504)**
					RC75108A	Raytheon
					RM55108A	† Raytheon
					75S108	Signetics
					SN55108A	† TI
					SN75108A	TI
				55107A with Diode Protected Input Stage	SN55107B	† AMD
					SN75107B	AMD
					55107BM	† Fairchild
					75107BC	Fairchild
					ITT55107B	† ITT
					ITT75107B	ITT
					DS55107	**† National (504)**
					DS75107	**National (504)**
					SN55107B	† TI
					SN75107B	TI
				55108A with Diode Protected Input Stage	SN55108B	† AMD
					SN75108B	AMD
					55108BM	† Fairchild
					75108BC	Fairchild
					ITT55108B	† ITT
					ITT75108B	ITT
					DS55108	**† National (504)**
					DS75108	**National (504)**
					SN55108B	† TI
					SN75108B	TI
3	±0.075		±5	100 Ohm Twisted Pair, Shielded	**HD248**	**† Harris (456)**
					HD548	**Harris (456)**
	±1.5 ma		±5	100 Ohm Twisted Pair, Shielded	**HD246**	**† Harris (456)**
					HD249	**† Harris (456)**
					HD546	**Harris (456)**
					HD549	**Harris (456)**
4	±0.025	±3	±5	Four 75107, Active Pull-Up	MC3450	Motorola
					DS3650	National
				Four 75108, Open Collector	MC3452	Motorola
					DS3652	National
	±0.2	±3	5	Three-state, RS422/423	MC3486	Motorola
		±7	5	Three-State, RS-422/423	AM26LS32C	AMD
					AM26LS32M	† AMD
					AM26LS32C	TI
					AM26LS32M	† TI
		±15	5	50 mv Hysteresis	DS1689	† National
					DS3689	National

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Common Mode Voltage	Supply Voltage	Comments	Device	Source
Line Receivers - Differential (Cont'd)						
4	±0.2	±15	5	50 mv Hysteresis	(Cont'd.)	
					DS1690	†National
					DS3690	National
					DS3651	**National (517)**
				Three-State	N8T110	Signetics
					N8T111	Signetics
	±0.5	±15	5	Three-State	AM26LS33C	AMD
					AM26LS33M	†AMD
See also Receivers listed under Digital ECL and Digital HNIL/HTL Miscellaneous sections						

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Output	Supply Voltage	Comments	Device	Source
Line Transceivers - Single Ended						
2	MOS/TTL	MOS/TTL	5	Transceiver/Port Controller	N8T30	Signetics
4	0.6 to 2.0	TTL	5	General Purpose Interface Bus, Open Collector, for MOS input	MC3446	Motorola
					MC3446	TI
		0.7 to 2.0	TTL	Three-State, Hysteresis	SN54S242	† AMD
					SN54S243	† AMD
					SN54LS242	† AMD
					9LS242M	**† Raytheon (282)**
					54LS242	**† Raytheon (282)**
					9LS243M	**† Raytheon (282)**
					54LS243	**† Raytheon (282)**
					SN54LS242	† TI
					SN54LS243	† TI
				Three-State, Bus Transceiver	AM2915M	† AMD
					MC2915M	† Motorola
				Three-State, Bus Transceiver, Parity Generator/Checker	AM2916M	† AMD
					AM2917M	† AMD
					MC2916M	† Motorola
					MC2917M	† Motorola
	0.8 to 2.0	TTL	5	Three-State, Bus Transceiver	AM2915C	AMD
					MC2915C	Motorola
					μPB2915	**NEC Micro (1850)**
				Three-State, Bus Transceiver, Parity Generator/Checker	AM2916C	AMD
					AM2917C	AMD
					MC2916C	Motorola
					MC2917C	Motorola
					μPB2916	**NEC Micro (1850)**
					μPB2917	**NEC Micro (1850)**
				General Purpose Interface Bus, Open Collector, 100 ma output	MC3440	Motorola
					MC3441	Motorola
					MC3443	Motorola
					DS8641	Motorola
					DS7641	† National
					DS8641	National
				General Purpose Bus, Open Collector, 100 ma,for 50 ohm system	DS8642	National
				Three-State (Inverting)	N8T26	AMD
					S8T26	† AMD
					9626	Fairchild
					MC6880	Motorola
					MC8T26	Motorola
					N8T26A	Signetics
					SN75136	TI
				Three-State(Non-Inverting)	N8T28	AMD
					S8T28	† AMD
					9628	Fairchild
					MC6889	Motorola
					MC8T28	Motorola
					N8T28	Signetics
				Three-State, Hysteresis	AM74S242	AMD
					AM74S243	AMD
					SN54LS242	† AMD
					SN74LS243	AMD
					ITT74LS242	ITT
					ITT74LS243	ITT
					9LS242C	**Raytheon (282)**
					74LS242	**Raytheon (282)**
					9LS243C	**Raytheon (282)**
					74LS243	**Raytheon (282)**
					74LS242	Signetics
					74LS243	Signetics
					SN74LS242	TI
					SN74LS243	TI
				Three-State, dual rank latches	SN54S266	† TI
					SN74S226	TI

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Output	Supply Voltage	Comments	Device	Source
Line Transceivers - Single Ended (Cont'd)						
4	(Cont'd.)					
	0.97 to 2.65	TTL	5	Open Collector, 1 v Hysteresis	DS7838	†AMD
					DS7838	†National
	1.05 to 2.50	TTL	5	Open Collector, 1 v Hysteresis	DS8838	AMD
					MC3438	Motorola
					DS8838	National
					N8T38	Signetics
	1.4 to 2.05	TTL	5	Open Collector, Hysteresis	AM26S12AM	†AMD
					AM26S12AC	AMD
	1.5 to 2.4	TTL	5	2-Input, Open Collector 100ma Drivers	AM2905M	†AMD
				2-Input, Open Collector 100ma Drivers, Parity Generator/Checker	AM2906M	†AMD
				Open Collector, 100ma output, Parity Generator/Checker	AM2907M	†AMD
	1.5 to 3.2	TTL	5	Open Collector, 100 ma output	SG55138	†Silicon G
					SN55138	†TI
	1.6 to 1.8	TTL	5	Open Collector, Hysteresis	AM26S12M	†AMD
					AM26S12C	AMD
	1.6 to 2.3	TTL	5	2-Input, Open Collector 100 ma Drivers	AM2905C	AMD
					MC2905	Motorola
					μPB2905	NEC Micro (1850)
					AM2905	Raytheon
				2-Input, Open Collector, 100 ma Drivers, Parity Generator/Checker	AM2906C	AMD
					MC2906	Motorola
					μPB2906	NEC Micro (1850)
					AM2906	Raytheon
				Open Collector, 100 ma output, Parity Generator/Checker	AM2907C	AMD
					MC2907	Motorola
					μPB2907	NEC Micro (1850)
					AM2907	Raytheon
	1.6 to 2.4	TTL	5	Open Collector, 100 ma output	AM26S10M	†AMD
					AM26S11M	†AMD
					9640M	†Fairchild
					9641M	†Fairchild
					AM26S10M	†TI
					AM26S11M	†TI
				Open Collector, 100 ma, Hysteresis	9642M	†Fairchild
	1.75 to 2.25	TTL	5	Open Collector, 100 ma output	AM26S10C	AMD
					AM26S11C	AMD
					9640C	Fairchild
					9641C	Fairchild
					MC26S10	Motorola
					MC26S11	Motorola
					AM26S10C	TI
					AM26S11C	TI
				Open Collector, 100 ma, Hysteresis	9642C	Fairchild
	1.8 to 2.9	TTL	5	Open Collector, 100 ma output	ITT55138	†ITT
					ITT75138	ITT
					SG75138	Silicon G
					SN75138	TI
	1.05 to 2.50	TTL	5	Three-State, T/R Disables, Hysteresis	DS7833	†National
					DS8833	National
				Inverting 7833/8833	DS7835	†National
					DS8835	National
				Three-State, NOR Gate, Transmit Disable, Hysteresis	DS7839	†National
					DS8839	National
				Inverting 7839/8839	DS7834	†National
					DS8834	National
					N8T34	Signetics
8	TTL	TTL	5	Bidirectional Bus Transceiver, Three-State	**DP8304**	**National (501)**
	0.7 to 2.0	TTL	5	Bidirectional Bus Transceiver, Three State	54LS245	†MMI

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Output	Supply Voltage	Comments	Device	Source
Line Transceivers - Single Ended (Cont'd)						
8	0.7 to 2.0	TTL	5	Bidirectional Bus Transceiver, Three State	(Cont'd.)	
					57LS305	†MMI
					54LS245	†TI
	0.8 to 2.0	TTL	5	Bidirectional Bus Transceiver, Three State	74LS245	MMI
					67LS305	MMI
					SN74LS245	TI
Line Transceivers - Differential						
1	±0.5/±1v	TTL	5	Independent Three-State 55113 Driver and 55115 Receiver	SN55116	†TI
					SN75116	TI
				Three-State 8 Pin, 40 ma	SN55117	†TI
					SN75117	TI
				Same as 55116 with Three-State Receiver	SN55118	†TI
					SN75118	TI
				Same as 55117 with Three-State Receiver	SN55119	†TI
					SN75119	TI

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Memory and Peripheral Drivers

Memory & Peripheral Drivers

Function	Device	Source	
MOS Dynamic Memory, Address Refresh Logic Circuitry			
	3222	Intel	
	MC8505	Motorola	
MOS Dynamic Memory, 4k Address Multiplexer and Refresh Counter			
	3232	Intel	
	MC3232A	Motorola	
MOS Dynamic Memory Interface, Microprocessor to 16K RAM			
	MC3480	Motorola	
MOS Dynamic Memory, 16k Address Multiplexer and Refresh Counter			
	3242	Intel	
Clock Generator/Oscillator, to 10 MHz, 8½1 Divider, for Microprocessors			
	ICM7209	†Intersil	
MNOS Memory Controller (for TMM141/2 EAROMS)			
	T3541	Toshiba	
MOS Clock Driver			
	MH0007	†National	
	MH0012	†National	
	MH0007C	National	
	MH0012C	National	
Dual MOS Clock Driver			
	0026	†AMD	
	0026C	AMD	
	0056	†AMD	
	0056C	AMD	
	SH013C	Fairchild	
	SH013M	†Fairchild	
	9646	Fairchild	
	MMH0026	†Motorola	
	MMH0026C	Motorola	
	MH0009	†National	
	MH0009C	National	
	MH0013	†National	
	MH0013C	National	
	DS0025	**†National**	**(502)**
	DS0025C	**National**	**(502)**
	DS0026	**†National**	**(503)**
	DS0026C	National	
	DS0056	**†National**	**(503)**
	DS0056C	National	
	SN75369	TI	
Two Phase Oscillator/Clock Driver (for MOS systems)			
	DS7803	**†National**	**(518)**
	DS8803	**National**	**(518)**
	DS7807	†National	
	DS8807	National	
	DS8813	**National**	**(518)**
	DS8817	National	
Two Phase Oscillator Driver (for CCD Shift Register Memories)			
	MCC233	Micro Comp	
Quad NMOS Memory Driver			
	MC3459	Motorola	
	MC3460	Motorola	
	DS1644	†National	
	DS3644	**National**	**(516)**
	DS1674	†National	
	DS3674	National	
	DS36144	National	
	DS36174	National	

Memory & Peripheral Drivers (Cont'd)

Function	Device	Source	
Quad MOS Driver (for clock inputs 2416 and 2444 CCD Memories)			
	5244	Intel	
Quad Port Driver, for 5270 RAM			
	DS1640	**†National**	**(506)**
	DS3640	**National**	**(506)**
	DS1670	**†National**	**(506)**
	DS3670	**National**	**(506)**
Dual MOS Clock Driver, bootstrapped for single supply systems			
	DS1642	**†National**	**(507)**
	DS3642	**National**	**(507)**
	DS1671	**†National**	**(513)**
	DS3671	**National**	**(513)**
	DS1672	**†National**	**(507)**
	DS3672	**National**	**(507)**
Quad MOS Clock Driver, decodes input address			
	DS3643	**National**	**(515)**
	DS3673	National	
Quad, MOS Memory Decoder/Clock Driver			
	DS36143	National	
	DS36173	National	
6 Bit MOS Refresh Counter/Driver			
	DS1646	**†National**	**(509)**
	DS3646	**National**	**(509)**
	DS1676	**†National**	**(509)**
	DS3676	**National**	**(509)**
Quad TTL to MOS Driver, Three State			
	ITT75367	ITT	
	SN75357	TI	
	SN75367	TI	
Quad TTL to NMOS Memory Driver (for 7001, etc.)			
	MC3466	Motorola	
Quad TTL to NMOS Memory Driver (for 2105, 2107, etc.)			
	9645	Fairchild	
	3245	Intel	
	5235	Intel	
	MC3245	Motorola	
Dual TTL to MOS Driver (MOS Memory Interface)			
	9644	**Fairchild**	**(652)**
	ITT75361A	ITT	
	DS75361	**National**	**(523)**
	DS75362	**National**	**(524)**
	DS75364	**National**	**(525)**
	MH8805	National	
	75361A	Signetics	
	SN75350	TI	
	SN75361A	TI	
Dual AND TTL to MOS Driver (NMOS Memory Interface)			
	9643	**Fairchild**	**(652)**
	DS75322	**National**	**(521)**
	SN75322	TI	
	SN75363	TI	
Dual Channel TTL to MOS Memory Interface (for TMS4062, AMS6002, etc.)			
	SN75370	TI	
Quad NAND TTL to MOS Driver (MOS Memory Interface clock driver)			
	3207A	Intel	
	3207A-1	Intel	
	ITT75365	ITT	
	MC75365	Motorola	
	DS75365	**National**	**(526)**

(Continued)

Memory & Peripheral Drivers (Cont'd)

Function	Device	Source	
Quad NAND TTL to MOS Driver (MOS Memory Interface clock driver) (Cont'd.)			
	3207A	Signetics	
	3207A-1	Signetics	
	SN75355	TI	
	SN75365	TI	
	SN75366	TI	
	SN75375	TI	
Quad TTL to MOS Shifter/Driver; Schottky			
	MB8901	Fujitsu	
	MB8902	Fujitsu	
	MB8907P	Fujitsu	
TTL to MOS Shifter; See also Digital TTL Translators			
Dual ECL to MOS Driver			
	SN75320	TI	
	SN75321	TI	
Dual 2 input ECL to MOS Level Shifter/Driver			
	MB8909	Fujitsu	
Quad 2 input ECL to TTL Level Shifter/Driver			
	MB8903	Fujitsu	
Dual Channel ECL to MOS Driver (MOS Memory Interface; also ECL to TTL driver)			
	ITT75368	ITT	
	MC75358	Motorola	
	MC75368	Motorola	
	SN75368	TI	
Dual MOS Logic to MOS Memory Driver			
	SN75364	TI	
Dual ECL to TTL/MOS Driver			
	SN75441	TI	
Hex MOS to Power Transistor Level Shifter/Driver			
	M54520	Mitsubishi	
Hex Latch/Driver, for MOS Memories			
	DS3645	Motorola	
	DS3675	Motorola	
	DS1645	**†National**	**(508)**
	DS3645	**National**	**(508)**
	DS1675	**†National**	**(508)**
	DS3675	**National**	**(508)**
Quad MOS Memory I/O Register			
	DS3647	Motorola	
	DS3677	Motorola	
	DS36147	Motorola	
	DS36177	Motorola	
	DS1647	**†National**	**(510)**
	DS3647	**National**	**(510)**
	DS1677	**†National**	**(510)**
	DS3677	**National**	**(510)**
	DS16147	**†National**	**(510)**
	DS36147	**National**	**(510)**
	DS16177	**†National**	**(510)**
	DS36177	**National**	**(510)**
Disc Memory Video Amplifer, for magnetic servo head			
	SSI101A	Silicon Sys.	
Disc Memory Fault Detector			
	SSI103	Silicon Sys.	
Disc Memory Head Selector			
	SSI102	Silicon Sys.	
Disc Memory Head Control Circuit, for moving heads			
	SSI104	Silicon Sys.	
Disc Memory Head Control Circuit, for fixed heads			
	SSI105	Silicon Sys.	

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Memory and Peripheral Drivers (Cont'd)

Memory & Peripheral Drivers (Cont'd)

Function	Device	Source	Line
Gated Decoder, for SSI104/5	SSi106	Silicon Sys.	
Quad Predriver, Open Collector, 50 ma Sink (for magnetic memories)	MC4042	Motorola	
Dual Memory Driver, 400 ma Sink (for magnetic memories)	MC4043	Motorola	
Memory Driver Dual, 400 ma Sink/Source, Decode (for magnetic memories)	75324	Fairchild	10
	DS3629	National	
	DS75324	**National (522)**	
	RC75324	Raytheon	
	RM55324	† Raytheon	
	75324	Signetics	
	SN75324	TI	
Memory Driver, Quad, 600 ma Sink	55326M	† Fairchild	
	75326C	Fairchild	
	ITT75326	ITT	20
	SN55326	† TI	
	SN75326	TI	
Memory Driver, Quad, 600 ma Source	55327M	† Fairchild	
	75327C	Fairchild	
	ITT75327	ITT	
	SN55327	† TI	
	SN75327	TI	
Memory Switch, Quad, 600mA Sink/Source	SN75328	TI	30
	SN75330	TI	
Memory Driver, Dual 600 ma Sink/Source	SN55325	† AMD	
	SN75325	AMD	
	55325M	† Fairchild	
	75325	Fairchild	
	ITT55325	ITT	
	ITT75325	ITT	
	MC55325	† Motorola	
	MC75325	Motorola	40
	DS55325	**† National (520)**	
	DS75325	**National (520)**	
	RM55325	† Raytheon	
	RC75325	Raytheon	
	55325	† Signetics	
	75325	Signetics	
	SG55325	† Silicon G	
	SG75325	Silicon G	
	SN55325	† TI	
	SN75325	TI	50
Quad Multiplexer/Driver, for MOS systems	9647	Fairchild	
	DS1648	**† National (511)**	
	DS3648	**National (511)**	
	DS1678	**† National (511)**	
	DS3678	**National (511)**	
Hex Inverter/MOS Driver, Three State	9648	Fairchild	
	DS1649	**† National (512)**	
	DS3649	**National (512)**	
	DS1679	**† National (512)**	60
	DS3679	**National (512)**	
Hex Inverter/MOS Driver, disable causes logic 1 state	**DS16149**	**† National (519)**	
	DS36149	**National (519)**	

(Continued)

Memory & Peripheral Drivers (Cont'd)

Function	Device	Source	Line
Hex Inverter/MOS Driver, disable causes logic 1 state (Cont'd.)	**DS16179**	**† National (519)**	
	DS36179	**National (519)**	
Dual AND Driver, HNIL, 250 ma, Open Collector	391	Teledyne S	70
Dual Peripheral AND Driver	55450A/B	† Fairchild	
	55451A/B	† Fairchild	
	55460	† Fairchild	
	55461	† Fairchild	
	55470	† Fairchild	
	55471	† Fairchild	
	75450	Fairchild	
	75451	Fairchild	
	75460	Fairchild	80
	75461	Fairchild	
	75470B	Fairchild	
	75471B	Fairchild	
	HD2574	Hitachi	
	HD2575	Hitachi	
	ITT55450	† ITT	
	ITT55460	† ITT	
	ITT75450	ITT	
	ITT75451	ITT	
	ITT75460	ITT	90
	ITT75461	ITT	
	M54504	Mitsubishi	
	M54600	Mitsubishi	
	M54601	Mitsubishi	
	MC75450	Motorola	
	MC75451	Motorola	
	SN75451B	Motorola	
	MC75461	Motorola	
	DS55450	† National	
	DS55451	† National	100
	DS55460	† National	
	DS55461	† National	
	DS75450	National	
	DS75451	National	
	DS75460	National	
	DS75461	National	
	RC75450	Raytheon	
	RC75451	Raytheon	
	RM55450	† Raytheon	
	RM55451	† Raytheon	110
	PBD3513	RIFA	
	75450B	Signetics	
	75451B	Signetics	
	SG55450	† Silicon G	
	SG55451	† Silicon G	
	SG55460	† Silicon G	
	SG55461	† Silicon G	
	SG75450	Silicon G	
	SG75451	Silicon G	
	SG75460	Silicon G	120
	SG75461	Silicon G	
	SN55450B	† TI	
	SN55451B	† TI	
	SN55460	† TI	
	SN55461	† TI	
	SN55470	† TI	
	SN55471	† TI	
	SN75401	TI	
	SN75411	TI	
	SN75430	TI	130
	SN75431	TI	
	SN75450B	TI	
	SN75451B	TI	
	SN75460	TI	

(Continued)

Memory & Peripheral Drivers (Cont'd)

Function	Device	Source	Line
Dual Peripheral AND Driver (Cont'd.)	SN75461	TI	
	SN75470	TI	
	SN75471	TI	
Dual Peripheral AND Driver, to 70v 300ma	MC1471	Motorola	140
	SN75476	TI	
Dual Peripheral AND Driver, to 70v 500ma	SN75416	TI	
Dual Peripheral AND Driver, to 80v, 300 ma	DS1611	† National	
	DS3611	National	
	DS3611	Signetics	
	UDN5711	Signetics	
	UDN-3611	Sprague	
	UDN-5711	Sprague	150
Dual Peripheral AND Driver, for CMOS	DS1631	† National	
	DS3631	National	
Dual 4 Input AND Driver, HNIL 250 ma Open Collector	390	Teledyne S	
4 Input AND Current Driver (45v, to 1.5A peak)	DH0006	† National	
	DH0006C	National	
4 Input AND High Voltage High Current Driver (4.5v, to 3A peak)	DH0008	† National	160
	DH0008C	National	
Quad 2 Input AND Driver (to 70v, sinks 300 ma)	MN304	Micro Net	
	MN304H	† Micro Net	
	UDN-5706A	Sprague	
Quad 2 Input AND Power Driver, Open Collector (to 100v, sinks 500ma)	UHC/D-400	† Sprague	
	UHC/D-406	† Sprague	170
	UHC/D-500	Sprague	
	UHC/D-506	Sprague	
	UHP-400	Sprague	
	UHP-406	Sprague	
	UHP-500	Sprague	
	UHP-506	Sprague	
Quad 2 Input NAND Driver (to 70v, sinks 300 ma)	UDN-5707A	Sprague	
Dual NAND Driver, HNIL, 250 ma, Open Collector	392	Teledyne S	180
4 Input NAND High Voltage, High Current Driver (40 to 50v, sinks 150 to 500 ma)	SH2001C	Fairchild	
	SH2001M	† Fairchild	
	SH2002C	Fairchild	
	SH2002M	† Fairchild	
	SH2200C	Fairchild	
	SH2200M	† Fairchild	
4 Input NAND High Voltage, High Current Drivers (40v, 0.15 to 0.25A)	DH0011	† National	190
	DH0011C	National	
4 Input NAND High Voltage, High Current Drivers (50, 70 or 100v, 0.25 to 0.5A)	DH0016C	National	
	DH0017C	National	
	DH0018C	National	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Memory and Peripheral Drivers (Cont'd)

Function	Device	Source	Line
Memory & Peripheral Drivers (Cont'd)			
Dual Peripheral NAND Driver			
	55452A	† Fairchild	
	55462	† Fairchild	
	55472B	† Fairchild	
	75452	Fairchild	
	75462	Fairchild	
	75472B	Fairchild	
	HD2577	Hitachi	
	ITT75452	ITT	
	ITT75462	ITT	
	M54501	Mitsubishi	10
	M54502	Mitsubishi	
	M54602	Mitsubishi	
	M54605	Mitsubishi	
	MC75452	Motorola	
	MC75462	Motorola	
	SN75452B	Motorola	
	DS55452	† National	
	DS55462	† National	
	DS75452	National	
	DS75462	National	20
	RC75452	Raytheon	
	RM55452	† Raytheon	
	75452B	Signetics	
	SG55452	† Silicon G	
	SG55462	† Silicon G	
	SG75452	Silicon G	
	SG75462	Silicon G	
	SN75402	TI	
	SN75412	TI	
	SN75432	TI	30
	SN55452B	† TI	
	SN75452B	TI	
	SN55462	† TI	
	SN75462	TI	
	SN55472	† TI	
	SN75472	TI	
	SN75475	TI	
Dual 4 Input NAND Driver, HNIL, 250 ma Open Collector			
	395	Teledyne S	40
Dual Peripheral NAND Driver, to 70v, 300ma			
	MC1472	Motorola	
	SN75477	TI	
Dual Peripheral NAND Driver, to 70v, 500ma			
	SN75417	TI	
Dual Peripheral NAND Driver, to 80v, 300ma			
	DS1612	† National	
	DS3612	National	
	DS3612	Signetics	
	UDN5712	Signetics	50
	UDN-3612	Sprague	
	UDN-5712	Sprague	
Dual Peripheral NAND Driver, for CMOS			
	DS1632	† National	
	DS3632	National	
Quad 2 Input NAND Driver, to 30v, sinks 250ma			
	MC693	Motorola	
Quad 2 Input NAND Driver, to 30v, sinks 100ma			
	M54503	Mitsubishi	
Quad 2 Input NAND Power Driver, Open Collector, to 100v, sinks 500 ma			
	UHC/D-407	† Sprague	
	UHC/D-408	† Sprague	
	UHC/D-507	† Sprague	
	UHC/D-508	† Sprague	
	UHP-407	Sprague	
	(Continued)		

Function	Device	Source	Line
Memory & Peripheral Drivers (Cont'd)			
Quad 2 Input NAND Power Driver, Open Collector, to 100v, sinks 500 ma (Cont'd.)			
	UHP-408	Sprague	
	UHP-507	Sprague	70
	UHP-508	Sprague	
Power Peripheral Driver/Logic Switch, to 90v, 2.0a (relay, solenoid, and hammer driver)			
	S55V01	† Siliconix	
	S55V02	† Siliconix	
	S55V11	† Siliconix	
	S55V12	† Siliconix	
	S55V21	† Siliconix	
	S55V22	† Siliconix	
	S75V01	Siliconix	80
	S75V02	Siliconix	
	S75V03	**Siliconix** **(542)**	
	S75V11	Siliconix	
	S75V12	Siliconix	
	S75V21	Siliconix	
	S75V22	Siliconix	
Relay Driver, to 70v, 500ma			
	CSR301	Teledyne C	
Relay Driver, to 65v, sinks 300 ma, OR Input for 48v telephone relays			
	DS1686	† National	
	DS1687	† National	
	DS3686	National	90
	DS3687	National	
Dual Relay Driver, to 60v, sinks 1a			
	831	Beckman	
Dual OR Driver, HNIL, 250 ma, Open Collector			
	393	Teledyne S	
Dual Peripheral OR Driver			
	55453A/B	† Fairchild	100
	55463	† Fairchild	
	55473B	† Fairchild	
	75453	Fairchild	
	75463	Fairchild	
	75473B	Fairchild	
	55453	† Hitachi	
	55463	Hitachi	
	75453	Hitachi	
	75463	Hitachi	
	ITT75453	ITT	110
	ITT75463	ITT	
	M54603	Mitsubishi	
	MC75453	Motorola	
	MC75463	Motorola	
	SN75453B	Motorola	
	DS55453	† National	
	DS55463	† National	
	DS75453	National	
	DS75463	National	
	RC75453	Raytheon	120
	RM55453	† Raytheon	
	75453B	Signetics	
	SG55453	Silicon G	
	SG55463	Silicon G	
	SG75453	Silicon G	
	SG75463	Silicon G	
	SN55453B	† TI	
	SN55463	† TI	
	SN55473	† TI	
	SN75403	TI	130
	SN75413	TI	
	SN75433	TI	
	SN75453B	TI	
	SN75463	TI	
	(Continued)		

Function	Device	Source	Line
Memory & Peripheral Drivers (Cont'd)			
Dual Peripheral OR Driver (Cont'd.)			
	SN75473	TI	
Dual Peripheral OR Driver, to 30v, 300ma			
	MC1473	Motorola	
	SN75478	TI	
Dual Peripheral OR Driver, to 30v, 500ma			140
	SN75418	TI	
Dual Peripheral OR Driver, to 80v, 300ma			
	DS1613	† National	
	DS3613	Signetics	
	DS3613	National	
	UDN5713	Signetics	
	UDN-3613	Sprague	
	UDN-5713	Sprague	
Dual Peripheral OR Driver, ECL Input			
	SN75441	TI	150
Dual Peripheral OR Driver, for CMOS			
	DS1633	† National	
	DS3633	National	
Quad 2 Input OR Driver, to 70v, sinks 300ma			
	UDN-5703A	Sprague	
Quad 2 Input OR Power Driver, Open Collector, to 100v, sinks 500ma			
	UHC/D-402	† Sprague	
	UHC/D-403	† Sprague	
	UHC/D-502	Sprague	160
	UHC/D-503	Sprague	
	UHP-402	Sprague	
	UHP-403	Sprague	
	UHP-502	Sprague	
	UHP-503	Sprague	
Dual NOR Driver, HNIL, 250 ma, Open Collector			
	394	Teledyne S	
Dual Peripheral NOR Driver			
	55454A/B	† Fairchild	
	55464	† Fairchild	170
	55474	† Fairchild	
	75454	Fairchild	
	75464	Fairchild	
	75474B	Fairchild	
	HD2579	Hitachi	
	ITT75454	ITT	
	ITT75464	ITT	
	M54604	Mitsubishi	
	MC75454	Motorola	
	SN75454B	Motorola	180
	MC75464	Motorola	
	DS55454	† National	
	DS55464	† National	
	DS75454	National	
	DS75464	National	
	RC75454	Raytheon	
	RM55454	† Raytheon	
	75454B	Signetics	
	SG55454	† Silicon G	
	SG55464	† Silicon G	190
	SG75454	Silicon G	
	SG75464	Silicon G	
	SN55454B	† TI	
	SN55464	† TI	
	SN55474	† TI	
	SN75404	TI	
	SN75414	TI	
	SN75434	TI	
	SN75454B	TI	
	SN75464	TI	200
	(Continued)		

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Memory and Peripheral Drivers (Cont'd)

Function	Device	Source	Line
Memory & Peripheral Drivers (Cont'd)			
Dual Peripheral NOR Driver (Cont'd.)	SN75474	TI	
Dual Peripheral NOR Driver, to 30v, 300ma	MC1479	Motorola	
	SN75479	TI	
Dual Peripheral NOR Driver, to 30v, 500ma	SN75419	TI	
Dual Peripheral NOR Driver, to 80v, 300ma	DS1614	†National	
	DS3614	National	10
	DS3614	Signetics	
	UDN5714	Signetics	
	UDN-3614	Sprague	
	UDN-5714	Sprague	
Dual Peripheral NOR Driver, for CMOS	DS1634	†National	
	DS3634	National	
Quad 2 Input NOR Driver, to 70v, sinks 300ma	UDN-5733A	Sprague	
Quad 2 Input NOR Power Driver, Open Collector, to 100v, sinks 500ma	UHC/D-432	†Sprague	20
	UHC/D-433	†Sprague	
	UHC/D-532	†Sprague	
	UHC/D-533	†Sprague	
	UHP-432	Sprague	
	UHP-433	Sprague	
	UHP-532	Sprague	
	UHP-533	Sprague	
High Current Switch Driver (to drive high power, high speed NPN switching transistors)	SG1629	†Silicon G	30
	SG3629	Silicon G	
Driver, Open Collector/Emitter, for 150mA (load connected to negative supply)	PBD3520	RIFA	
Driver, single, 125mA, for relays, motors, lamps	PBD3510	RIFA	
	PBD3511	RIFA	
Dual Darlington Switch, to 50v, 1.5a	ULN-2061M	Sprague	40
Quintuple High Voltage Interface (Outputs can accept high negative voltages in "off" state)	SP1404	Plessey	
	SP1406	Plessey	
Driver, dual, 2 input, Sink or Source 500mA	SG1627	†Silicon G	
	SG3627	Silicon G	
Quad Darlington Switch, to 50v, 1.5a	ULN-2064B	Sprague	50
	ULN-2074B	Sprague	
Hammer Driver (to 6A pulsed output)	DH0028C	National	
Driver, 5 channel Darlington, to 400ma	LB1287	Sanyo	
	LB1288	Sanyo	
	XR2200	Exar	
	XR2200M	†Exar	
Driver, 5 channel, CMOS/TTL Input (lamp, relay driver, load to negative supply)	UDN-2957A	Sprague	60
Driver, 5 channel, CMOS/PMOS Input (lamp, relay driver, load to negative supply)	UDN-2956A	Sprague	
Hex Universal Driver (400 ma)	NE582	Signetics	
Driver, 7 Channel, CMOS/TTL Input (hammer, lamp, relay driver)	XR2203	Exar	
	XR2203M	†Exar	70
	9667	Fairchild	
	MC1413	Motorola	
	PBD352303	RIFA	
	ULN2003	Signetics	
	L203	SGS	
	SG2003	Silicon G	
	SG3853	Silicon G	
	ULN-2003A	Sprague	
	ULN-2005A	Sprague	
	ULN-2013A	Sprague	80
	ULN-2015A	Sprague	
	ULN-2023A	Sprague	
	ULN-2025A	Sprague	
	SN75468	TI	
	ULN2003A	TI	
Driver, 7 Channel, CMOS/PMOS Input (hammer, lamp, relay driver)	XR2204	Exar	
	XR2204M	†Exar	
	9668	Fairchild	90
	MC1416	Motorola	
	PBD352304	RIFA	
	ULN2004	Signetics	
	ULN-2004A	Sprague	
	ULN-2014A	Sprague	
	ULN-2024A	Sprague	
	SN75469	TI	
	ULN2004A	TI	
Driver, 7 Channel, MOS/TTL Input (hammer, lamp, relay driver)	XR2201	Exar	
	XR2201M	†Exar	100
	9665	Fairchild	
	MC1411	Motorola	
	PBD352301	RIFA	
	ULN2001	Signetics	
	L201	SGS	
	SG2001	Silicon G	
	SG3851	Silicon G	
	ULN-2001A	Sprague	110
	ULN-2011A	Sprague	
	ULN-2021A	Sprague	
	SN75466	TI	
	ULN2001A	TI	
Driver, 7 Channel, PMOS Input (hammer, lamp, relay driver)	XR2202	Exar	
	XR2202M	†Exar	
	9666	Fairchild	
	MC1412	Motorola	120
	PBD352302	RIFA	
	ULN2002	Signetics	
	L202	SGS	
	SG2002	Silicon G	
	SG3852	Silicon G	
	ULN-2002A	Sprague	
	ULN-2012A	Sprague	
	ULN-2022A	Sprague	
	SN75467	TI	
Driver, 7 Channel, PMOS Input (hammer, lamp, relay driver) (Cont'd.)	ULN2002A	TI	130
Addressable Peripheral Driver (Latched, 8 Output Driver)	NE590	Signetics	
	NE592	Signetics	
Printer Driver, 7 Channel	FD1021	Hitachi	
Driver, 8 Channel, CMOS/TTL Input (hammer, lamp, relay driver)	ULN-2803A	Sprague	140
	ULN-2805A	Sprague	
	ULN-2813A	Sprague	
	ULN-2815A	Sprague	
	ULN-2823A	Sprague	
	ULN-2825A	Sprague	
Driver, 8 Channel, CMOS/PMOS Input (hammer, lamp, relay driver)	ULN-2804A	Sprague	
	ULN-2814A	Sprague	150
	ULN-2824A	Sprague	
Driver, 8 Channel, MOS/TTL Input (hammer, lamp, relay driver)	ULN-2801A	Sprague	
	ULN-2811A	Sprague	
	ULN-2821A	Sprague	
Driver, 8 Channel, PMOS Input (hammer, lamp, relay driver)	ULN-2802A	Sprague	
	ULN-2812A	Sprague	160
	ULN-2822A	Sprague	
Driver, 8 Channel, CMOS/TTL Input (lamps, relay driver)	UDN-2981A	Sprague	
	UDN-2983A	Sprague	
Driver, 8 Channel, CMOS/PMOS Input (lamp, relay driver)	UDN-2982A	Sprague	
	UDN-2984A	Sprague	
Printer Controller, for Seiko CR 330 or M 310	**μPD764**	**NEC Micro (1799)**	170
Printer Controller, for 5 x 7 dot matrix printers	CY-480	Cybernetic	
Printer Driver, 5 Channel	LB1287	Sanyo	
	LB1288	Sanyo	
Printer Driver, 10 Channel	FD1018	Hitachi	
Thermal Print Head Driver	SN75270	TI	180
	SN75490	TI	
Printing Calculator Circuits	DS8654	National	
	DS8655	National	
	DS8656	National	
	DS8692	National	
	DS8693	National	
	DS8694	National	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Sense Amplifiers

Sense Amplifiers

Function	Device	Source	Line
One Channel Sense Amplifier (for core memories)	MC1440	Motorola	
Dual Channel Gated Sense Amplifier (for core memories)	CA1541	†RCA	
Dual Core Memory Sense Amplifier, Separate Outputs	SN5524	†AMD	
	SN7524	AMD	
	SN5525	†AMD	
	SN7525	AMD	10
	5524M	†Fairchild	
	5525M	†Fairchild	
	55224M	†Fairchild	
	55225M	†Fairchild	
	7524C	Fairchild	
	7525C	Fairchild	
	75224C	Fairchild	
	75225C	Fairchild	
	ITT5524	†ITT	
	ITT7524	ITT	20
	MC5524	†Motorola	
	MC5525	†Motorola	
	MC7524	Motorola	
	MC7525	Motorola	
	DS5524	†National	
	DS5525	†National	
	DS7524	National	
	DS7525	National	
	7524	Signetics	
	SG5524	†Silicon G	30
	SG5525	†Silicon G	
	SG7524	Silicon G	
	SG7525	Silicon G	
	SN5524	†TI	
	SN7524	TI	
Dual Core Memory Sense Amplifier, Complemetary Output, Latch Capability	SN5520	†AMD	
	SN7520	AMD	
	SN5521	†AMD	40
	SN7521	AMD	
	ITT5520	†ITT	
	ITT7520	ITT	
	DS5520	†National	
	DS5521	†National	
	DS7520	National	
	DS7521	National	
	7520	Signetics	
	SG5520	†Silicon G	
	SG5521	†Silicon G	50
	SG7520	Silicon G	
	SG7521	Silicon G	
	SN5520	†TI	
	SN7520	TI	
Dual Core Memory Sense Amplifier, Single Open Collector Output	ITT5522	†ITT	
	ITT7522	ITT	
	ITT7523	ITT	
	DS5522	†National	60
	DS5523	†National	
	DS7522	National	
	7522	Signetics	
	SG5522	†Silicon G	
	SG5523	Silicon G	
	SG7522	Silicon G	
	SG7523	Silicon G	
	SN5522	†TI	
	SN7522	TI	

Sense Amplifiers (Cont'd)

Function	Device	Source	Line
Dual Core Memory Sense Amplifier, Output Register	SN7526	TI	70
Dual Core Memory Sense Amplifier, Separate Outputs, Test Points	5528M	†Fairchild	
	5529M	†Fairchild	
	7528C	Fairchild	
	7529C	Fairchild	
	ITT5528	†ITT	
	ITT7528	ITT	
	MC5528	†Motorola	80
	MC5529	†Motorola	
	MC7528	Motorola	
	MC7529	Motorola	
	DS5529	†National	
	DS7528	National	
	DS7529	National	
	7528	Signetics	
	SG7528	Silicon G	
	SG7529	Silicon G	
	SN7528	TI	90
Dual Core Memory Sense Amplifier, Separate Inverted Outputs	SN55234	†AMD	
	SN55235	†AMD	
	SN75234	AMD	
	SN75235	AMD	
	55234M	†Fairchild	
	55235M	†Fairchild	
	75234C	Fairchild	
	75235C	Fairchild	100
	ITT55234	†ITT	
	ITT75234	ITT	
	75234	Signetics	
	SN55234	†TI	
	SN75234	TI	
Dual Core Memory Sense Amplifier, Separate Inverted Outputs, Test Points	SN55238	†AMD	
	SN75238	AMD	
	SN55239	†AMD	110
	SN75239	AMD	
	55238M	†Fairchild	
	55239M	†Fairchild	
	75238C	Fairchild	
	75239C	Fairchild	
	SN55238	†TI	
	SN75238	TI	
Dual Core Memory Sense Amplifier, Separate Open Collector Outputs	5534M	†Fairchild	
	5535M	†Fairchild	120
	55232M	†Fairchild	
	55233M	†Fairchild	
	7534C	Fairchild	
	7535C	Fairchild	
	75232C	Fairchild	
	75233C	Fairchild	
	ITT5534	†ITT	
	ITT7534	ITT	
	MC5534	†Motorola	130
	MC5535	†Motorola	
	MC7534	Motorola	
	MC7535	Motorola	
	DS5534	†National	
	DS5535	†National	
	DS7534	National	
	DS7535	National	
	75232	Signetics	

(Continued)

Sense Amplifiers (Cont'd)

Function	Device	Source	Line
Dual Core Memory Sense Amplifier, Separate Open Collector Outputs (Cont'd.)	SG5534	†Silicon G	140
	SG5535	†Silicon G	
	SG7534	Silicon G	
	SG7535	Silicon G	
	SN55232	†TI	
	SN75232	TI	
Dual Core Memory Sense Amplifier, Separate Open Collector Outputs, Test Points	5538M	†Fairchild	
	5539M	†Fairchild	150
	7538C	Fairchild	
	7539C	Fairchild	
	ITT5538	†ITT	
	ITT7538	ITT	
	MC5538	†Motorola	
	MC5539	†Motorola	
	MC7538	Motorola	
	MC7539	Motorola	
	DS5538	†National	
	DS5539	†National	160
	DS7538	National	
	DS7539	National	
	SG5538	†Silicon G	
	SG5539	†Silicon G	
	SG7538	Silicon G	
	SG7539	Silicon G	
Dual Sense Amplifier/Data Register (for core memories)	ITT55236	†ITT	
	ITT75236	ITT	170
	ITT55237	†ITT	
	ITT75237	ITT	
MOS to TTL Level Converter, High Speed, Three State	MC4000	Motorola	
	MC4300	†Motorola	
Dual Sense Amplifier (for MOS Memory or line receiver)	DS163	†AMD	
	DS363	AMD	180
	DS1603	†AMD	
	DS3603	AMD	
	DS3604	AMD	
	SN75207	AMD	
	SN75208	AMD	
	75207C	Fairchild	
	75208C	Fairchild	
	ITT75207	ITT	
	ITT75208	ITT	
	DS3604	**National** (504)	190
	DS1603	**†National** (504)	
	DS3603	**National** (504)	
	DS75207	**National** (504)	
	DS75208	**National** (504)	
	75S207	Signetics	
	75S208	Signetics	
	SN75207	TI	
	SN75208	TI	
Dual Sense Amplifier (NMOS memories to ECL 10K)	MC3461	Motorola	200
Dual MOS to TTL Level Converter, Latch, Three State (Sense Amp)	MC4068	Motorola	
	MC4368	†Motorola	
	MC54468	†Motorola	
	MC74468	Motorola	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Sense Amplifiers (Cont'd)

Function	Device	Source	Line
Sense Amplifiers (Cont'd)			
Dual MOS to TTL Level Converter, Latch, Three State (Sense Amp) (Cont'd.)			
	DS3625	**National** (514)	
	DS7802	† National	
	DS7806	† National	
	DS8802	National	
	DS8806	National	
	N8T25	Signetics	
Translators: See also Digital TTL (Translators)			
Quad Sense Amplifier, Three State			10
	MC3430	Motorola	
	MC3431	Motorola	
	MC3432	Motorola	
	MC3433	Motorola	
	DS3651	**National** (517)	
	DS3653	National	
Hex MOS Sense Amplifier (MOS to TTL Converter) Three State			
	DS1605	**† National** (505)	
	DS1606	**† National** (505)	20
	DS1607	**† National** (505)	
	DS1608	**† National** (505)	
	DS3605	**National** (505)	
	DS3606	**National** (505)	
	DS3607	**National** (505)	
	DS3608	**National** (505)	
Hex MOS Sense Amplifier, Open Collector (for 1103)			
	3208A	Intel	
Hex MOS Sense Amplifiers with Latches, Three State			
	3408A	Intel	30
4 Input Sense Amplifier (for plated wire or thick/thin film memories)			
	MC1444	Motorola	
	MC1544	† Motorola	
Dual Digit Driver, Sense Amplifier, for MD8201 RAM			
	MB8912	Fujitsu	
	MB8915	Fujitsu	
Dual Sense Amplifier with Read Strobe, ECL for MB8215 RAM			
	MB8916	Fujitsu	40

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Transmitters-Receivers

Serial Transmitters-Receivers

Function	Max Serial Data Rate in KHZ	Supply Voltage	Device	Source	Line
(ACIA) Asynchronous Communications Interface Adapter (Links 8 Bit bidirectional data bus to serial asynchronous data communications, including to 6860)	50	5	**S6850**	**AMI (1567)**	
			MC6850	Motorola	
Digital Modem (Modulation, demodulation and supervisory control, up to 600bps.)	0.6	5	MC6860	Motorola	
PSAR (Programmable Synchronous Asynchronous Receiver) Synchronous/Asynchronous serial to parallel converter with programmable character length and programmable serial data rate.	100	-12,5	AY8-1472B	GI	10
			PT1472B	Western	
	640	-12,±5	NC2259	Nitron	
		-12,5	PT1472B-01	Western	
PSAT (Programmable Synchronous Asynchronous Transmitter) Synchronous/Asynchronous parallel to serial converter that has programmable character length and programmable serial data rate.	100	-12,5	AY8-1482B	GI	20
			PT1482B	Western	
	200	-12,±5	NC2257	Nitron	
			NC2260	Nitron	
	640	-12,5	PT1482B-01	Western	
PSART (Programmable Synchronous Asynchronous Receiver Transmitter) Serial to parallel and parallel to serial converter that can operate in Full Duplex Mode.	50	5	8251	Intel	
			μPD8251	**NEC Micro (1814)**	30
	320	5,12	**3843**	**Fairchild (1098)**	
BOART (Bus Orientated Programmable Asynchronous Receiver/Transmitter	9.6	5	TR1983	Western	
SDLC (Synchronous Data Link Controller)	1500	5	SD1933	Western	
Synchronous Receiver/Transmitter (Bi Sync/SDLC)	800	±5,12	**μPD379**	**NEC Micro (1788)**	
UART (Universal Asynchronous Receiver Transmitter) complete serial to parallel and parallel to serial interface)	1.2	-12,5	10371	Rockwell	40
	10	-12,±5	S1757	AMI	
	12.5	-12.5	**S1883**	**AMI (354,1587)**	
	20	-12,5	AY6-1013	†GI	
			TR1402	Western	
			TR1602	Western	
	25	-12,5	COM2017	SMC	
			COM2502	SMC	
	30	5	AY3-1015	GI	50
		5 to 14	AY3-1014A	GI	
		-12,5	MM5303	National	
			TR1602-03	Western	
	40	-12,5	AY5-1013A	GI	
			COM2017H	SMC	
			COM2502H	SMC	
			TR1602-04	Western	
	50	±5,12	μPD369	NEC Micro	
		-12,5	TR1602-05	Western	

(Continued)

Serial Transmitters-Receivers (Cont'd)

Function	Max Serial Data Rate in KHZ	Supply Voltage	Device	Source	Line
UART (Universal Asynchronous Receiver Transmitter) complete serial to parallel and parallel to serial interface)	60	5	TR1863	Western	60
	100	5	HCMP1854C	†Hughes	
			CDP1854C	†RCA	
	200	5	HM6402-2	†Harris	
			HM6402-9	Harris	
			HM6403-2	†Harris	
			HM6403-9	Harris	
			IM6402	Intersil	
			IM6402M	†Intersil	70
			IM6403	Intersil	
			IM6403M	†Intersil	
		-12,5	TMS6011	TI	
	400	5	HM6402A-2	†Harris	
			HM6402A-9	Harris	
			HM6403A-2	†Harris	
			HM6403A-9	Harris	
		3–12	HCMP1854	†Hughes	
			CDP1854	†RCA	
USRT (Universal Synchronous Receiver Transmitter) Complete serial to parallel and parallel to serial interface.	250	-12,5	COM2601	SMC	80
	500	5	**S2350**	**AMI (368,1589)**	
USART (Universal Synchronous/Asynchronous Receiver/Transmitter)	56	5	TR1953	Western	
	256	5,12	**3843**	**Fairchild (1098)**	
USYNRT (Universal Synchronous Receiver/Transmitter) Multi Protocol, Bit and Byte Oriented	256	5,12	COM5025	SMC	90
MPCC (Multi Protocol Communications Controller) Bit and Byte Oriented	500	5	2652	Signetics	
Universal Communications Interface (receives or transmits data to serial data bus when addressed and commanded by bus. Links the bus to serial or parallel I/O devices)	500	5	UMC-16	Trans-Data	
ASTRO (Asynchronous/Synchronous Receiver/Transmitter) to interface serial communications channel with a parallel digital system (i.e. microprocessors)	1000	12,±5	INS1671	National	100
			COM1671	SMC	
			UC1671	Western	
			UC1971	Western	
Baud Rate Generator (Programmable Divider)	1000	12,±5	F4702BC	Fairchild	
			F4702BM	†Fairchild	
			HD4702-2	**†Harris (1634)**	110
			HD4702-9	**Harris (1634)**	
			HD6405-2	**†Harris (1634)**	
			HD6405-9	**Harris (1634)**	
			MC14411	Motorola	
			MM5307	National	
			COM5026	SMC	
			COM5026T	SMC	
			COM5046	SMC	
			COM5046T	SMC	
			BR1941	Western	120
			BR1941-06	Western	

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Transmitters-Receivers (Cont'd)

Serial Transmitters-Receivers (Cont'd)

Function	Max Serial Data Rate in KHZ	Supply Voltage	Device	Source	Line
Baud Rate Generator (Programmable Divider), Dual					
	1000	12,±5	COM5016	SMC	
			COM5016T	SMC	
			COM5036	SMC	
			COM5036T	SMC	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

Communications Circuits

Part No.	Description	Process	Power Supplies	Input/ Output	Package
S1883	Universal Asynchronous Receiver/Transmitter (UART)	P-I^2	-12V, ± 5V	TTL	40 Pin Plastic, 40 Pin SLAM
S2350	Universal Synchronous Receiver/Transmitter (USRT)	N-SiGate	+5V	TTL	40 Pin Plastic 40 Pin SLAM
S2559	Digital Tone Generator	CMOS	+3.5V to +13V	TTL-CMOS	16 Pin Plastic
S2560	Key Pulser	CMOS	—	—	18 Pin Package 24 Pin Package
S2561	Tone Ringer	CMOS	—	—	18 Pin Package
S2562	Repertory Dialer	CMOS	—	—	40 Pin Package
S2563	Single Channel PCM CODEC	CMOS	—	—	24 Pin Package

TouchControl™ Interface Circuits

Part No.	Description	Process	Power Supplies	Input/ Output	Packages
S9260/61	Seven-Switch Interface	P-I^2	-13.5V to -18V	MOS/TTL	22 Pin Plastic
S9262	Fourteen-Switch Interface	P-I^2	-13.5V to -18V	MOS/TTL	22 Pin Plastic
S9263/64/65	Sixteen Switch Interface	P-I^2	-13.5V to -18V	MOS/TTL	40 Pin Plastic
S9266	32-Switch Interface	P-I^2	-13.5V to -18V	MOS/TTL	40 Pin Plastic

TCK-100 TouchControl™ Kit

The AMI TouchControl kit demonstrates the ease with which this unique system of capacitive switching may be implemented. Included in the kit are a printed circuit board and AMI's S9263 TouchControl circuit. The printed wiring board, which has sixteen touch switches etched into its top surface, contains on its reverse side all the interconnection necessary to interface the S9263 outputs with sixteen light emitting diodes. Additional components required for the kit are readily available, and assembly of the kit should take less than an hour's time.

The TouchControl™ Concept

TouchControl™ panels replace mechanical switches with non-moving electronically sensitive glass (or other material panels that respond to the touch of a finger. The most apparent advantage of TouchControl is the visual appeal of a flat keyboard, which may be designed in a wide variety of patterns and colors. In addition to the advanced styling features, TouchControl also offers several practical benefits, such as the reliability of non-moving electronic controls and electrical isolation of the entire switch area. TouchControl also provides safety advantages, complete moisture proofing and ease of cleaning. Contact your nearest AMI Sales Office for additional information about the TouchControl concept.

Typical Applications

- Appliance Control Panels
- Home Entertainment Systems
- Power Tool Controls
- Television Sets
- Automotive Controls
- Telephones
- Games
- Industrial Controllers
- Computer Terminals
- Keyboards
- Instrumentation
- 16-to01 Multiplexers
- Microprocessor Interface

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TouchControl™ Kit

FEATURES

- 16 TouchControl Switches can Operate in Different Modes
- Quick and Convenient for Demonstrating TouchControl Concept
- Interfaces Easily to External Logic for Prototype Development
- Can Drive up to 16 LED Indicators
- Provisions for Adding Power Supply Components (for 115 VAC Operation)

PARTS LIST FOR AMI TOUCHCONTROL KIT:

QUANTITY REQUIRED	DESCRIPTION
1	S9263 TouchControl circuit (Included)
1	Printed wiring board (Included)
1	Transformer, 12.6 volt 300mA Radio Shack P/N 273-1385 or equivalent
1	Line cord
1	Diode IN920 or equivalent
2	100KΩ Resistor ¼ Watt
1	60KΩ Resistor ¼ Watt
1	15KΩ Resistor ¼ Watt
1	10KΩ Resistor ¼ Watt
16	3.3KΩ Resistor ¼ Watt
1	Transistor 2N3569 or equivalent
1	500μF capacitor/20 volts
1	0.33μF capacitor
1	270 pF capacitor
16	Light emitting diode — MV5023 or equivalent
1	Aluminum chassis box–15" x 9" Bud No. AC1421 or equivalent (optional)

ASSEMBLY

The circuit board may be assembled easily by referring to Figure 2, a view of the reverse side of the board. For appearance, it is recommended that all components except the LED's and the S9263 be mounted on the reverse side of the board, with all leads cut off flush with the board's top surface.

For convenience, a 15 volt power supply is provided on the circuit board, so that the system may be plugged into a standard 110 volt outlet. If desired, an external DC supply of 15 volts may be used, connecting the positive and negative outputs to the corresponding holes designated for C1. If a DC supply is used, the transformer, diode, and C1 may be eliminated.

INTRODUCTION

The AMI TouchControl kit demonstrates the ease with which this unique system of capacitive switching may be implemented. Included in the kit are a printed circuit board and AMI's newly developed S9263 TouchControl circuit. The printed wiring board, which has 16 touch switches etched onto its top surface, contains on its reverse side all the interconnection necessary to interface the S9263 inputs with the 16 touch switches and the S9263 outputs with 16 light emitting diodes. As the touch switches are activated, the corresponding diodes are lighted to indicate the output states of the S9263. If desired, external logic may be operated by connecting a cable directly to the S9263 outputs.

Additional components required for the kit are readily available, and assembly of the kit should take less than an hour's time. The circuit board may be mounted either on standoffs or on a standard aluminum chassis box.

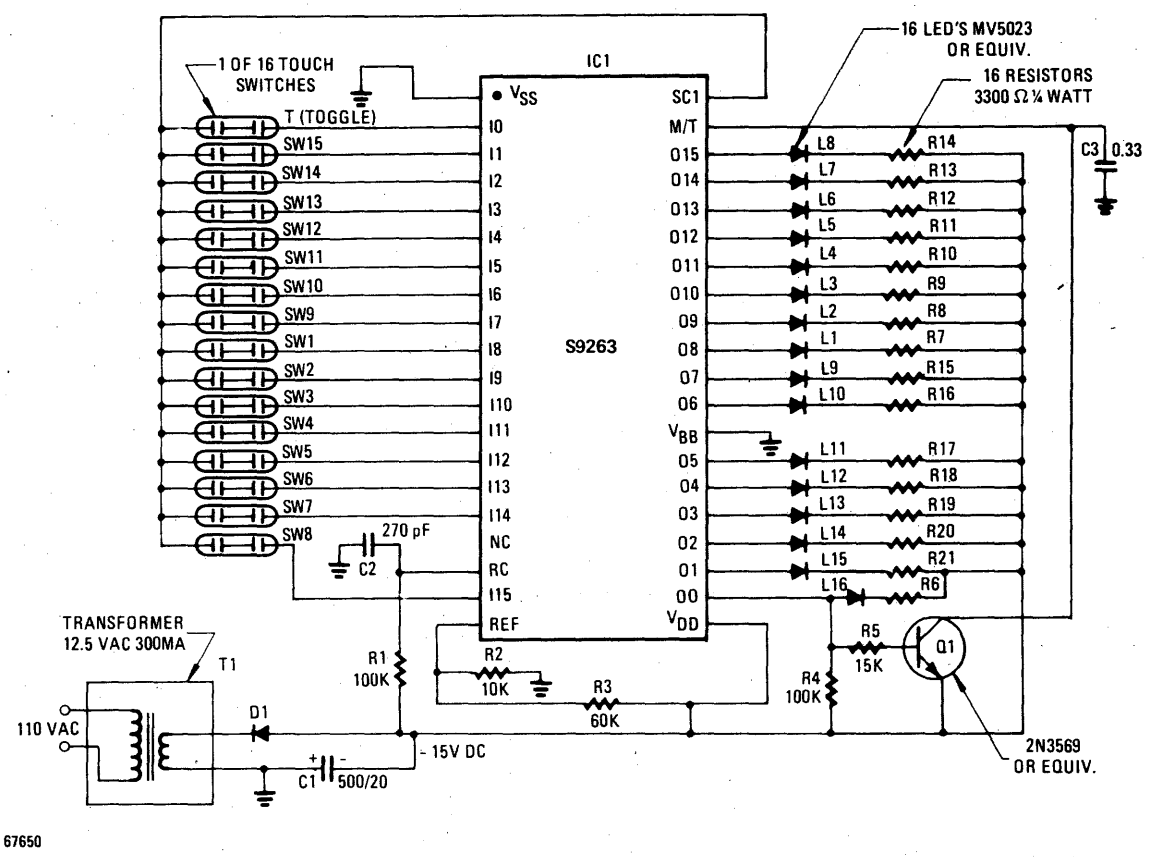
OPERATION

The AMI TouchControl kit provides sixteen touch switches that interface with the S9263 to activate sixteen light emitting diodes. Each of the switches numbered from one to fifteen has a light associated with it which is labeled with the same number. The switch labeled "T" is used to select the mode of operation of the S9263, either momentary or toggle. When the LED labeled "T" is off, touch pads one through fifteen operate as momentary switches, and any switch's corresponding LED will turn on when the switch is touched, remaining on only for the duration of touching the switch. If "T" is touched, the "T" LED will turn on and stay on even after "T" is untouched. The S9263 is now operating in a toggle mode, and the brief touch of any switch from one through fifteen will cause its corresponding LED to turn on and latch. Subsequent activations of the switch will turn the LED off and on alternately. Touching "T" once again causes the "T" LED to turn off, and the S9263 once again operates in the momentary mode. By removing the 0.33μF capacitor, it is possible to use the "T" pad as a clear switch. In this mode, all numbered pads function as "push on, push off"

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switches. Touching the "T" pad turns off all LED's corresponding to the numbered switches.

To operate external logic systems with the Touch-Control kit, a cable may be soldered, using a grounded soldering iron, directly to the outputs of the S9263. The voltage on an output that is turned off (corresponding LED is off) is - 15 volts (or V_{DD}). When turned on, the output will rise towards ground (V_{SS}). Appropriate loading conditions are specified in the advanced product description for this part.



67650

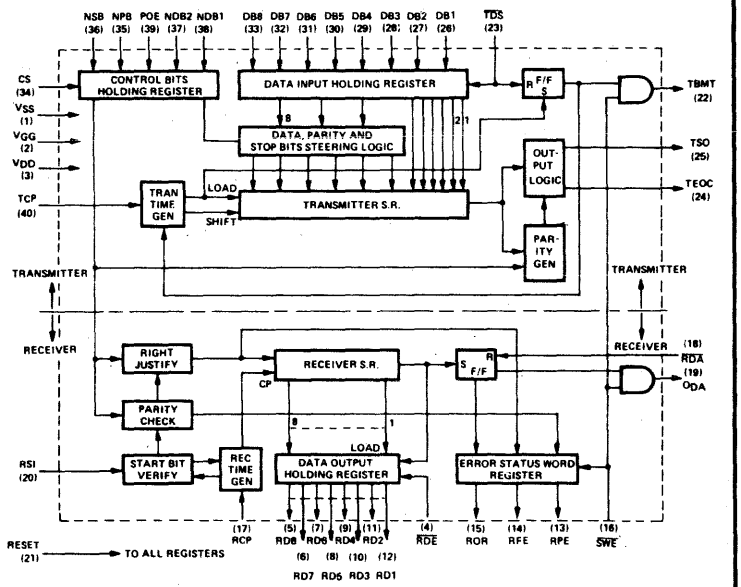
SCHEMATIC DIAGRAM OF TCK-100

PARTS LIST FOR ASSEMBLING TCK — 100 KIT:

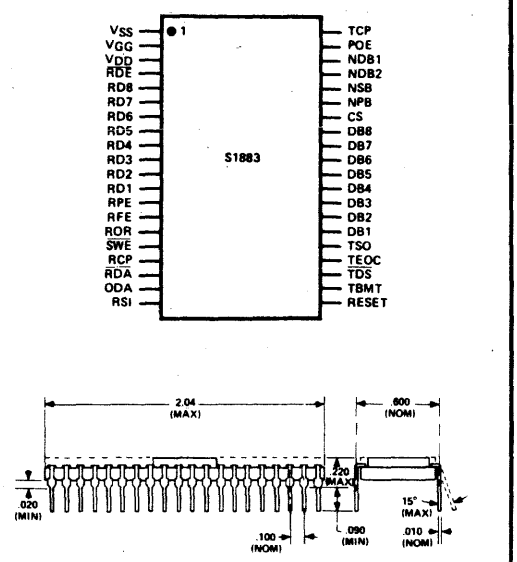
PART NUMBER	PART DESCRIPTION	PART NUMBER	PART DESCRIPTION
R1, R4	100 KΩ ¼ Watt resistor	Q1	NPN transistor 2N3569 or equivalent
R2	10 KΩ ¼ Watt resistor	D1	Diode IN920 or equivalent
R3	60 KΩ ¼ Watt resistor	L1 thru L16	Light emitting diode — MV5023 or equivalent
R5	15 KΩ ¼ Watt resistor		
R6 thru R21	3.3 KΩ ¼ Watt resistor	IC1	AMI integrated circuit S9263
C1	500 μF capacitor 20 Volts	T1	Transformer 12. 6 VAC @ 300 mA. Radio Shack P/N 273-1385 or equivalent
C2	270 pF capacitor		
C3	0.33 μF capacitor		

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Universal Asynchronous Receiver/Transmitter (UART)



S1883 BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- 12.5 K Baud Data Rates
- 5-8 Bit Word Length
- Parity Generation/Checking Odd, Even, None
- Framing and Overflow Error Detection
- 1, 1.5, or 2 Stop Bits
- Double Buffered Input/Output
- Independent Transmit/Receive Rates
- Start and Stop Bits Generated and Detected
- Interchangeable with TMS6011, COM2017, TR1602, AY-5-1013
- Tri-State Outputs

FUNCTIONAL DESCRIPTION

The S1883 Universal Asynchronous Receiver Transmitter (UART) is a single chip MOS/LSI device that totally replaces the asynchronous parallel to serial and serial to parallel conversion logic required to interface a word parallel controller or data terminal to a bit serial communication network.

For asynchronous data transmission with a non-contiguous data bit stream, the UART automatically inserts a START bit preceding each character and under program control 1, 1.5, or 2 stop bits at the end of each character. To detect incoming characters in a noisy environment the UART employs a START bit detection network and allows errorless recovery of data with up to 42% distortion.

The UART will transmit or receive data characters of 5, 6, 7, or 8 bit length. Options allow the generation and checking of odd, even parity or no parity. The odd or even parity bit is automatically added to the character length for transmission. The parity bit is removed, checked and an error flag set if incorrectly received.

The data or baud rate at the receiver input and transmitter output are determined independently by external clock inputs. The clock inputs must be 16 times the data rate required at the serial input and output. The independent clocks allow for either half or full duplex operation.

The UART provides a buffer register in both the transmitter and receiver to allow a full character time for responding to a received data ready or transmit data request signal. The UART generates a MARK signal if the transmit register is not loaded with a data character and also indicates an overflow error if two characters are received without a RDA input.

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TYPICAL APPLICATIONS

- Computer Peripherals
- Communication Concentrators
- Integrated Modems
- Industrial Data Transmission
- TTY Terminals
- Time Division Multiplexing

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Positive Voltage on Any Pin with Respect to V_{SS}	+.3 Volt
Negative Voltage on Any Pin with Respect to V_{SS}	−20.0 Volt

NOTE: Stresses greater than those listed as Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operation section of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC (STATIC) CHARACTERISTICS

$T_A = 0° - +70°C$, $V_{SS} = +5$ Volt ±5%, $V_{GG} = -12$ Volt ±5%

Symbol	Parameter	Min	Max	Unit	Condition
V_{IH}	Input High Voltage	V_{SS} -1.0	V_{SS} +0.3	Volt	Internal Pull-up
V_{IL}	Input Low Voltage	V_{GG}	0.8	Volt	Resistor Provided
I_{LI}	Input Load Current		-1.2	mamp	V_{IN} = 0 Volt
V_{OH}	Output High Voltage	2.4		Volt	I_{OH} = - 100 uamp
V_{OL}	Output Low Voltage		.4	Volt	I_{OL} = 1.6 mamp
C_{IN}	Input Capacitance		20	pf	$V_{IN} = V_{SS}$
C_{OUT}	Output Capacitance		10	pf	$V_{OUT} = V_{SS}$
I_{SS}	V_{SS} Supply Current		30	mamp	$\overline{SWE} = \overline{RDE} = V_{IL}$
I_{GG}	V_{GG} Supply Current		40	mamp	ITTL Load

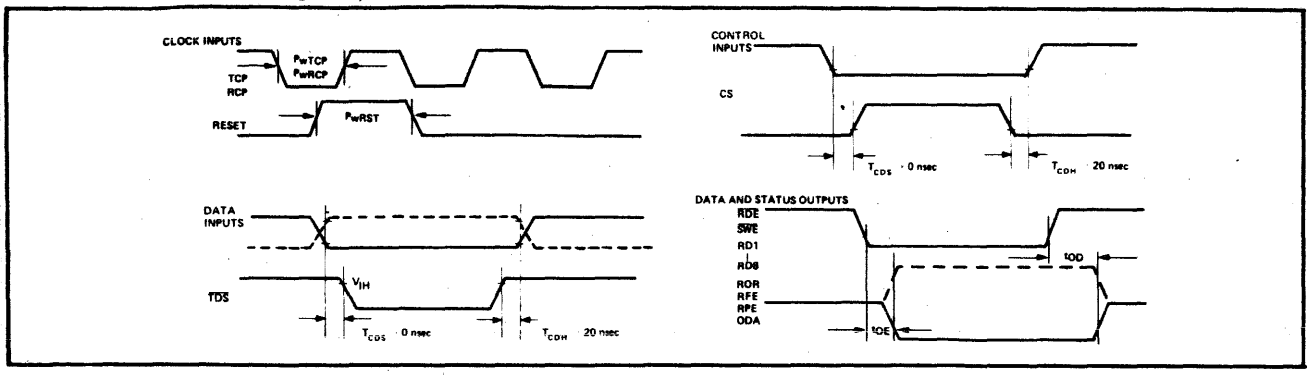
AC (DYNAMIC) CHARACTERISTICS

$T_A = 0°C - +70°C$; $V_{SS} = +5$ Volt ±5%; $V_{GG} = -12$ Volt ±5%

Symbol	Parameter	Min	Max	Unit	Condition
TCP, RCP	Clock Frequency	DC	200	KHz	
Input Pulse Widths					
PWTCP	Transmit Clock	2.5		usec	C_L = 20pf
PWRCP	Receive Clock	2.5		usec	1 TTL Load
PWCS	Control Strobe	250		nsec	
PWTDS	Transmit Data Strobe	250		nsec	
PWRST	RESET	1.0		μsec	
PWSWE	Status Word Enable	500		nsec	
PWRDA	Reset Data Available	500		nsec	
PWRDE	Receive Data Enable	250		nsec	
Switching Characteristics					
t_{CDS}	Control Set Up Time	0		nsec	Figure 1
t_{CDH}	Control Hold Time	20		nsec	Figure 1
t_{OE}	Output Enable Time		500	nsec	
t_{OD}	Output Disable Time		500	nsec	

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TIMING WAVEFORMS (Figure 1)



PIN DEFINITIONS

Pin	Label	Function
(1)	V_{SS}	+5 Volt ± 5%
(2)	V_{GG}	−12 Volt ± 5%
(3)	V_{DD}	Ground
(21)	RESET	The transmitter status outputs TBMT and TEOC are set to V_{OH} indicating the input transmitter buffer register is empty. The TSO output generates V_{OH} or MARK until a valid data character has been loaded into the transmitter and valid data transmission begins. The receiver status output ODA, is reset to the V_{OL} state.
(38)	NDB1	Number Data Bits/Character
(37)	NDB2	Number Data Bits/Character
(36)	NSB	Number Stop Bits The bit length of each data character and the number of stop bits added to each transmitted character are defined by these three inputs. The character word length does not include the parity bit and is common to both the transmitter and receiver if operating in the full duplex mode.

NSB	NDB2	NDB1	BITS/CHARACTER	STOP BITS
V_{IL}	V_{IL}	V_{IL}	5	1
V_{IL}	V_{IL}	V_{IH}	6	1
V_{IL}	V_{IH}	V_{IL}	7	1
V_{IL}	V_{IH}	V_{IH}	8	1
V_{IH}	V_{IL}	V_{IL}	5	1.5
V_{IH}	V_{IL}	V_{IH}	6	2
V_{IH}	V_{IH}	V_{IL}	7	2
V_{IH}	V_{IH}	V_{IH}	8	2

(35)	NPB	NO PARITY BIT. A V_{IH} eliminates the PARITY bit from being transmitted causing the STOP bit(s) to immediately follow the last data bit. The receiver assumes the bit(s) following the last data bit to be STOP bits. The RPE output is also forced to a V_{OL} condition.
(39)	POE	PARITY ODD/EVEN. If the NPB input is V_{IL}, the parity mode is ODD if POE is V_{IL} and EVEN if POE is V_{IH}. The parity mode is the same for both the transmitter and receiver.
(34)	CS	CONTROL STROBE. A V_{IH} loads POE, NDB1, NDB2, NPB, NSB into the CONTROL HOLDING REGISTER. To load the control inputs for static operation CS can be hard-wired to V_{IH}.
(26)	DB1	TRANSMITTER DATA BITS. Input data on DB1-DB8 are strobed into the DATA INPUT
(27)	DB2	HOLDING REGISTER by $\overline{TDS}$.
(28)	DB3	Input data is assumed right justified so DB1 is always the least significant bit and is the bit
(29)	DB4	
(30)	DB5	

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Pin	Label	Function
(31) (32) (33)	DB6 DB7 DB8	transmitted following the START bit. For data words less than eight bits, the unused bits are don't care inputs.
(23)	$\overline{TDS}$	TRANSMITTER DATA STROBE. A V_{IL} enters data on the DB1-DB8 inputs into the INPUT HOLDING REGISTER. If the transmitter is in the idle state with both TBMT and TEOC at V_{OH}, the START bit will be generated on the first negative transition of the input clock TCP following the return of $\overline{TDS}$ to a V_{IH} state.
(25)	TSO	TRANSMITTER SERIAL OUTPUT. Data entered on DB1-DB8 are serially transmitted on TSO. A START (SPACE) bit precedes each character. A PARITY bit, if selected, and the correct number of STOP bits follow the last valid data bit. The TSO output is V_{OH} (MARK) when a valid character is not being transmitted.
(22)	TBMT	TRANSMITTER BUFFER EMPTY. A V_{OH} indicates the character in the INPUT HOLDING REGISTER has been transferred into the transmitter and a new character may be loaded into the INPUT HOLDING REGISTER. One complete character time (START BIT, DATA BITS, PARITY BIT, AND STOP BIT(S)) is available to load the next character. If a $\overline{TDS}$ is not generated within the time allotted, the TSO output will go into an idle state of V_{OH} or a MARK condition. TBMT will remain in the tri state mode unless $\overline{SWE}$ is a U_{ZL}.
(24)	TEOC	TRANSMITTER END OF CHARACTER. A V_{OL} to V_{OH} transition indicates the transmission of the character and stop bits have been completed. The V_{OH} is maintained until the leading edge of the next START bit (MARK to SPACE transition) is generated.
(40)	TCP	TRANSMITTER CLOCK PULSE. The transmitter input clock must be 16 times faster than the desired baud rate at TSO.
(17)	RCP	RECEIVER CLOCK PULSE. The receiver input clock must be 16 times the baud rate of data received on RSI.
(20)	RSI	RECEIVER SERIAL INPUT. Serial input data is received on RSI at a baud rate 1/16th the rate of RCP. The V_{IH} to V_{IL} (MARK to SPACE) transition beginning each START bit synchronizes the receiver to the incoming data. Data is assumed to be received least significant bit first.
(12) (11) (10) (9) (8) (7) (6) (5)	RD1 RD2 RD3 RD4 RD5 RD6 RD7 RD8	RECEIVER DATA. Data outputs from the DATA OUTPUT HOLDING REGISTER are active only when $\overline{RDE}$ is a V_{IL}. The eight data outputs are in a tri-state mode if $\overline{RDE}$ is a V_{IH}. Data is presented at the outputs right justified with RD1 the least significant bit. For data word lengths less than 8 bits the unused bits will appear as V_{OL}.
(4)	$\overline{RDE}$	RECEIVER DATA ENABLE. A V_{IL} enables data in the DATA OUTPUT HOLDING REGISTER to the RECEIVER DATA output pins. For an output configuration not requiring a tri-state condition for RD1-RD8 the RDE input can be tied directly to ground enabling the data outputs at all times.
(19)	ODA	OUTPUT DATA AVAILABLE. A V_{OH} indicates a complete character has been received and transferred to the DATA OUTPUT HOLDING REGISTER. The ODA output will be in the tri-state mode unless $\overline{SWE}$ is a V_{IL}. For contiguous data inputs on RSI data will remain in the holding register one character time before being lost.
(18)	$\overline{RDA}$	RESET DATA AVAILABLE. A V_{IL} resets the ODA to a V_{OL}. If ODA is not reset by $\overline{RDA}$ the ROR will be set when the next complete character is received and transferred to the DATA OUTPUT HOLDING REGISTER.
(15)	ROR	RECEIVER OVERRUN. A V_{OH} indicates a second character has been received and transferred to the DATA OUTPUT HOLDING REGISTER without an intervening $\overline{RDA}$. If the previously received character has not been unloaded from the register the next character will be loaded and the first character lost. ROR will remain in the tri-state mode unless $\overline{SWE}$ is a V_{IL}.
(14)	RFE	RECEIVER FRAMING ERROR. A V_{OH} indicates a correct STOP bit was not received following the START bit and correct number of data bits. RFE will remain in the tri-state mode unless $\overline{SWE}$ is a V_{IL}.

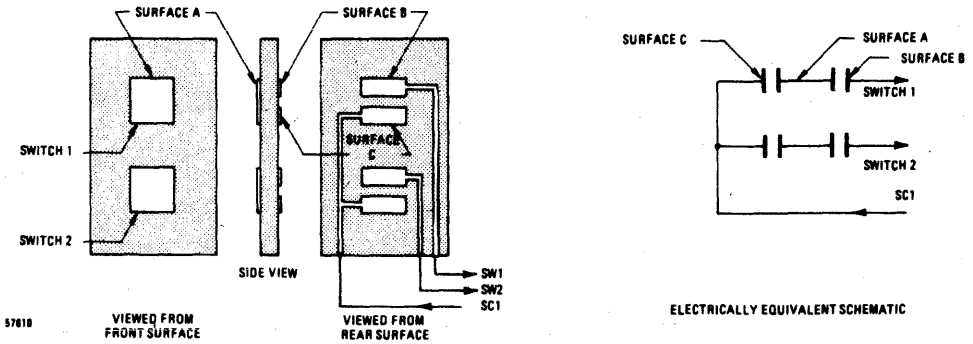


FIGURE 3. CONSTRUCTION OF A TWO SWITCH TOUCHCONTROL PANEL WITH EQUIVALENT ELECTRICAL CIRCUIT.

The application of the conductive surfaces depends on selection of the panel materials. If glass is used, for example, it is common to apply a coating of tin oxide, which is then fired on for durability; rear surface conductors may be screened on with a conductive ink. Touch panels may be made more simply from double-sided printed circuit boards in which the conductive TouchControl surfaces are created by standard etching. For breadboarding purposes, a number of conductive tapes and paints are available and may be applied to a variety of touch panel materials.

ELECTRICAL OPERATION

The three conductive surfaces in a TouchControl switch combine to form two capacitors connected in series, as shown in the schematic diagram of Figure 3. An AC signal generated in the MOS circuit is applied to the rear conductive surface labeled C. This signal is coupled through to surface A by the capacitor formed by C and A. The signal is then coupled to surface B by the capacitor formed by A and B and applied to one of the inputs of the MOS circuit, which detects the signal's presence. When surface A is touched, the amplitude of the signal is significantly decreased because of body capacitance. This is sensed by the MOS circuit, and the appropriate switching function is performed.

TOUCH SWITCH LAYOUT GUIDELINES

AMI TouchControl circuits have been designed to interface with a variety of touch switch configurations. However, there are several guidelines that must be observed to insure a satisfactory TouchControl system.

The size of a TouchControl switch is dependent on the amount of capacitance needed to couple the clock signal to the "I" inputs of the MOS circuits. Because the input capacitance associated with the circuit input is typically five picofarads, it is advisable that each of the two series capacitors formed by the three conductive TouchControl panel surfaces be no less than seven picofarads. Since the capacitance in picofarads can be calculated by $C = 0.22 \in A \div d$, where $\in$ is the dielectric constant, A is area, and d is the material's thickness, it is apparent that minimum switch size is dependent on the thickness and dielectric constant of the panel material. If, for example, the panel is made from 1/8" thick glass with a dielectric constant of 8, then the minimum area of each of the two rear surface conductors is 0.5 sq. inches. Since the touch surface must cover the entire area of the two rear conductors, it must, then, be at least 1.0 sq. inch. It is desirable to separate the two rear-surface conductors by at least 0.125 inches, so the touch surface would be somewhat larger than 1.0 sq. inch. Higher capacitance, and thus smaller touch switches, can be obtained by using epoxy printed circuit material; though the dielectric constant is lower (around 5.0) the thickness can be decreased substantially.

CIRCUIT TO PANEL CONNECTIONS

There are a number of ways to make the necessary connections between TouchControl circuits and panels. A simple approach is to use a printed circuit board for the touch panel. In this case, the connections to the circuit are made by the etched copper pattern. In laying out a printed circuit, it is important to keep the copper traces running to the individual touch pads separated from each other as much as possible. In most instances a minimum spacing of 0.125" between traces is acceptable, though wider spacing might be necessary in cases where traces will run parallel to each other for distances of over six inches. It is also important to keep the clock output (SC1) at least 0.75 inches away from any input trace. These spacing requirements are guidelines to be followed regardless of the touch panel material.

With glass touch panels, a simple method for breadboarding systems is to fasten individual wires onto the conductive surfaces with a conductive epoxy. For production situations, it is possible to locate the electronic circuitry on a separate printed circuit board. Contact to the glass touch panel can be made through spring contacts mounted in the appropriate locations on the circuit board. An alternate approach is to route the traces on the glass to an edge of the glass, making connection through an edge connector, keeping in mind the spacing requirements between traces.

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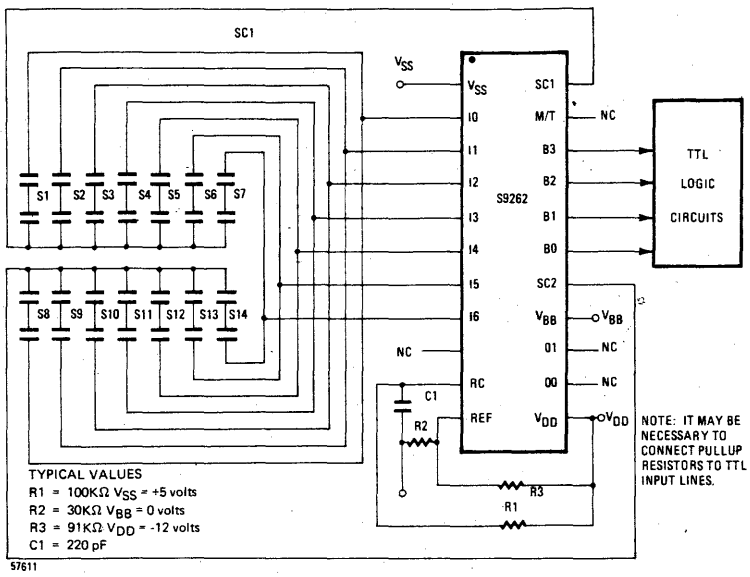


FIGURE 2. 14 SWITCH APPLICATION USING S9262

TABLE 1. OUTPUT ENCODING (V_{BB} = 0 VOLTS)

SCAN OUTPUT	TOUCHED INPUT	"B" OUTPUTS B0 B1 B2 B3 B4	"O" OUTPUTS O0 O1 O2 O3 O4 O5 O6	AK OUTPUT
SC1	I0	0 0 0 0 0	1 0 0 0 0 0 0	1
SC1	I1	1 0 0 0 0	0 1 0 0 0 0 0	1
SC1	I2	0 1 0 0 0	0 0 1 0 0 0 0	1
SC1	I3	1 1 0 0 0	0 0 0 1 0 0 0	1
SC1	I4	0 0 1 0 0	0 0 0 0 1 0 0	1
SC1	I5	1 0 1 0 0	0 0 0 0 0 1 0	1
SC1	I6	0 1 1 0 0	0 0 0 0 0 0 1	1
SC1	I7	1 1 1 0 0	0 0 0 0 0 0 0	1
SC1	I8	0 0 0 1 0	0 0 0 0 0 0 0	1
SC1	I9	1 0 0 1 0	0 0 0 0 0 0 0	1
SC1	I10	0 1 0 1 0	0 0 0 0 0 0 0	1
SC1	I11	1 1 0 1 0	0 0 0 0 0 0 0	1
SC1	I12	0 0 1 1 0	0 0 0 0 0 0 0	1
SC1	I13	1 0 1 1 0	0 0 0 0 0 0 0	1
SC1	I14	0 1 1 1 0	0 0 0 0 0 0 0	1
SC1	I15	1 1 1 1 0	0 0 0 0 0 0 0	1
SC2	I0	0 0 0 0 1	0 0 0 0 0 0 0	1
SC2	I1	1 0 0 0 1	0 0 0 0 0 0 0	1
SC2	I2	0 1 0 0 1	0 0 0 0 0 0 0	1
SC2	I3	1 1 0 0 1	0 0 0 0 0 0 0	1
SC2	I4	0 0 1 0 1	0 0 0 0 0 0 0	1
SC2	I5	1 0 1 0 1	0 0 0 0 0 0 0	1
SC2	I6	0 1 1 0 1	0 0 0 0 0 0 0	1
SC2	I7	1 1 1 0 1	0 0 0 0 0 0 0	1
SC2	I8	0 0 0 1 1	0 0 0 0 0 0 0	1
SC2	I9	1 0 0 1 1	0 0 0 0 0 0 0	1
SC2	I10	0 1 0 1 1	0 0 0 0 0 0 0	1
SC2	I11	1 1 0 1 1	0 0 0 0 0 0 0	1
SC2	I12	0 0 1 1 1	0 0 0 0 0 0 0	1
SC2	I13	1 0 1 1 1	0 0 0 0 0 0 0	0
SC2	I14	0 1 1 1 1	0 0 0 0 0 0 0	1
SC2	I15	1 1 1 1 1	0 0 0 0 0 0 0	1
–	None	1 1 1 1 1	0 0 0 0 0 0 0	0

ENA INPUT

Available on the S9266, the $\overline{ENA}$ input allows the outputs to be bussed and may be gated off by application of a logic 1 level. V_{SS} applied to the input enables all five outputs and AK.

EXT

The EXT pin is available on the S9266 and is used to supply a higher clock voltage to the TouchControl panel whenever that may be necessitated by smaller touch switch size. When the higher clock voltage level for SC1 and SC2 is not required, this pin should be connected to V_{DD}.

TOUCHCONTROL APPLICATION NOTES

PANEL CONSTRUCTION

A TouchControl switch panel consists of a single sheet of a rigid material with conductive surfaces applied on both sides as shown in Figure 3.

A number of materials may be used for touch panels, the selection of the material most suited for a particular application being dependent on such things as durability, appearance, ease of assembly, cost, and dielectric constant of the material.

Regardless of the selected panel material, a touch switch is formed by applying a single conductive surface to its front surface with two other conductive surfaces applied directly in line on the reverse side of the panel. Figure 3 shows three views of a typical touch panel containing two TouchControl switches. On switch one, conductive surface A is applied to the front of the panel and is the surface to be touched to effect a switch closure. Surfaces B and C are applied directly in line with A on the opposite side of the panel. A should cover completely and may overlap surfaces B and C.

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V_{BB} SUPPLY

The sources of all output devices (both "O" and "B" outputs) are common and connected to pin V_{BB}. This allows TTL compatibility as shown in Figure 1, as well as the ability to drive higher level signals. For instance, if V_{SS} = 0 volts, V_{DD} = - 16 volts, and V_{BB} = V_{SS}, then active outputs would drive a load connected to V_{DD} towards V_{SS}.

M/T INPUT

The M/T input pin selects the mode of switch operation, either momentary or toggle. Applying V_{SS} to the M/T pin selects momentary operation in which appropriate outputs are active only for the duration of touching a switch. In this mode, no output is active when no switch is touched. A V_{DD} level applied to M/T causes the circuit to operate in the toggle mode for "push-on, push-off" operation. Subsequent activation of the switch will toggle the corresponding output on and off alternately. It should be noted that each input should be cleared to the off state before selecting a new input to obtain meaningful data from the binary outputs. To reset all outputs when the toggle mode is selected, a pulse of V_{SS} level may be applied to the M/T input.

SC1 and SC2 OUTPUTS

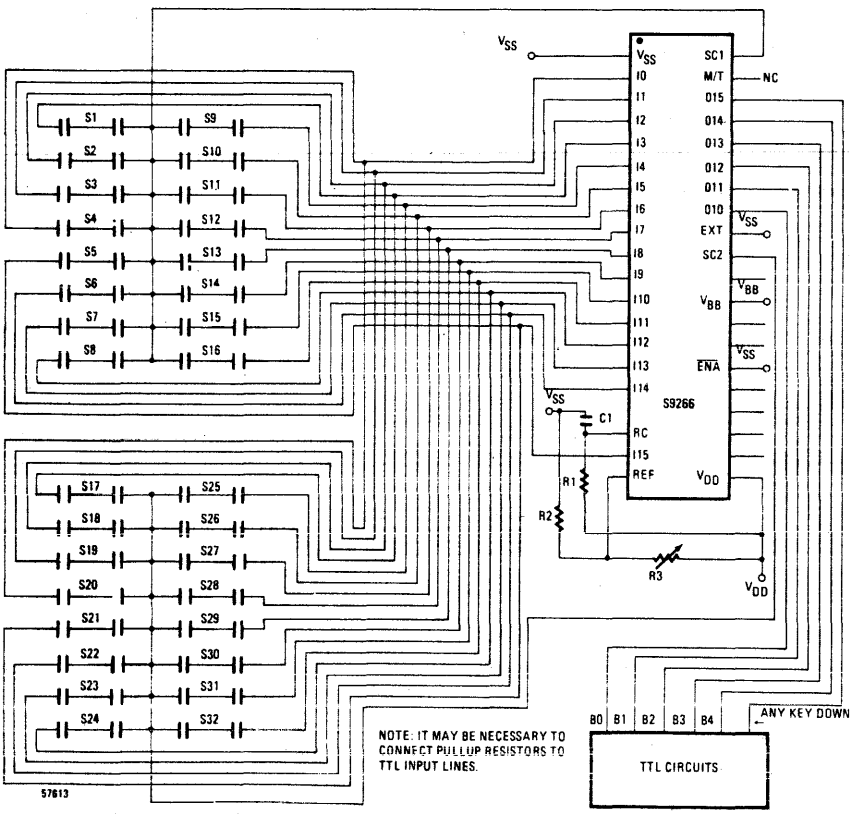
The S9262 and S9266 have multiplexed inputs, using 2 x 7 and 2 x 16 matrices, respectively, to provide 14 and 32 input states. Clock signals SC1 and SC2 are used along with the "I" inputs to form these matrices as connected in the schematic of Figure 1.

O OUTPUTS

Each output pin labeled "O" corresponds to an input pin labeled "I". Whenever an input is selected, the output becomes active and will drive an external load toward supply voltage V_{BB}. This is true for momentary operation only; toggle operation is described in the section labeled "M/T input." When "O" outputs are not active, they are high impedance open drain.

B AND AK OUTPUTS

The S9262 has four and the S9266 has five outputs labeled "B." These supply a binary code relating to the state of the inputs. Fourteen unique states are available on S9262 and thirty-two on S9266. The output configuration is identical to the "O" outputs. An extra output labeled AK is available on the S9266 and is active whenever any key is selected.



TYPICAL VALUES:
R1 = 100KΩ V_{SS} = +5 volts
R2 = 30KΩ V_{SS} = 0 volts
R3 = 91KΩ V_{SS} = -12 volts
C1 = 220 pF

FIGURE 1. 32 SWITCH APPLICATION USING S9266

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ABSOLUTE MAXIMUM RATINGS

Voltage on any pin except EXT relative to V_{SS}:	+ 0.3V to - 20V	Operating temperature range:	0°C to + 50°C
Voltage on EXT pin relative to V_{SS}:	+ 0.3V to - 27V	Storage temperature (Ambient)	- 65°C to + 150°C

**For non-multiplexed TouchControl circuits see AMI S9260, S9261, S9263, S9264, S9265*

ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 50°C; V_{SS} = 0V; V_{DD} = - 13.5V to - 18.0V unless otherwise specified.)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IL}	Input logic 0 level – all except "I" inputs.	+ 0.3	0	- 1.5	Volts	Note: M/T and $\overline{ENA}$ inputs are internally pulled up to V_{SS}.
V_{IH}	Input logic 1 level – all except "I" inputs.	- 10.0	- 12.0	- 18.0	Volts	
f_{RC}	Internal oscillator frequency measured at RC input.	50		100	kHz	
T_S	Switch delay time	50		200	msec	Frequency measured at RC Input = 50 kHz.
T_{RST}	Time to reset all latches using M/T input.		100		msec	
V_{OL}	Output low voltage.	V_{SS}		- 1.0	Volts	V_{BB} = V_{SS}; 10K resistive load to V_{DD}.
V_{OH}	Output high voltage			V_{DD}		
V_{OL}	Output low voltage.	V_{SS}		V_{SS} - 0.5	Volts	V_{SS} = + 5V; V_{BB} = 0V V_{DD} = - 12V; 2800Ω resistive load to V_{SS}.
V_{OH}	Output high voltage	V_{BB} + 0.4		V_{BB}		
SC1, SC2	Scan clock output.					Max. capacitive loading ≤ 150 pF.
	Output low voltage	V_{SS}		- 1.5		
	Output high voltage.			V_{DD}		

OPERATION

Device operation can be understood by referring to Figure 1, depicting a typical application of the S9266. Each of the 32 pairs of series capacitors labeled S1 – S32 is one touch switch located on a TouchControl panel constructed of glass, printed circuit board, epoxy, or other dielectric material. (For details on touch panel configuration and operation, see the TouchControl application note included in this APD.) In each capacitor pair, the two common plates represent the conductive area on the control panel surface that is to be touched. The other two plates are formed by two conductive surfaces parallel to the touched surface and located directly under it on the reverse side of the panel. Referring again to Figure 1, the S9266 generates a clock signal on output SC1 and a similar signal on output SC2. The SC1 clock output is connected to the common conductors of 16 of the 32 touch switches; the SC2 clock connects to the remaining 16 switches. For each touch switch the clock signal passes through the two series capacitors and is detected in the MOS circuit. When a panel switch surface is touched, the signal level into the chip diminishes, and the on-chip differential amplifier senses the change and performs the appropriate switching function.

I INPUTS

Inputs from the touch switch pads to the TouchControl circuit are labeled I0 through I15 (S9266), or I0 through I6 (S9262). The I inputs in conjunction with SC1 and SC2 outputs form a touch switch matrix of 2 x 16 or 2 x 7, respectively. In both these parts the outputs are binary coded and will be described later.

RC INPUT

A resistor connected to V_{DD} and a capacitor connected to V_{SS} are connected to the RC input pin to establish the on-chip clock frequency that controls the rate of multiplexing and the touch switch delay time. Nominal values for these components are suggested in Figure 1, but they may be varied to change clock frequency over a range of 50kHz to 100 kHz.

REF INPUT

In order to allow flexibility in the choice of TouchControl panel materials, switch layout, and switch size, AMI TouchControl inputs have been designed to detect a differential change rather than an absolute change in level. To obtain a reference level, two resistors are connected to input REF, one connected to input REF, one connected to V_{SS} and the other to V_{DD}.

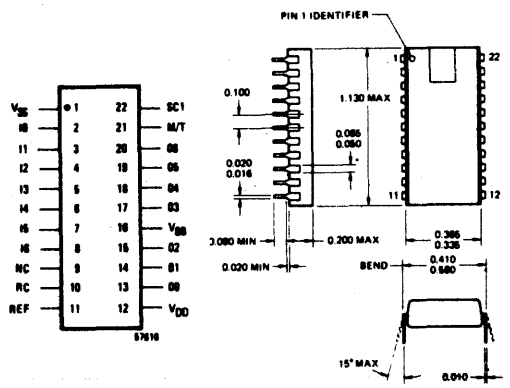
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S9263/S9264/S9265
TouchControl™ Interface

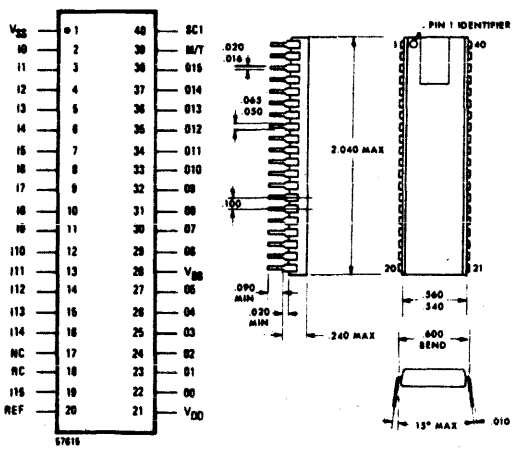
Features

- Interfaces with up to 16 Touch Switches
- Eliminates Contact Noise
- Comparator Sensing Permits Use with Wide Variety of Touch Switch Configurations
- Momentary or Toggle Operation Electrically Selectable
- Outputs are TTL/CMOS/MOS Compatible
- Simplifies Design of Touch-Sensitive Switches

ADVANCED PRODUCT DESCRIPTION



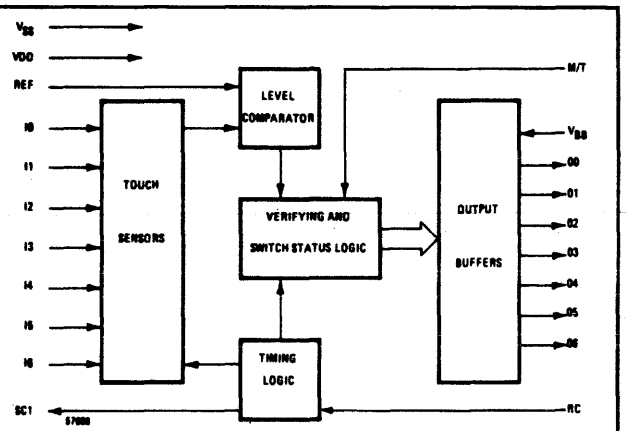
PIN/PACKAGE CONFIGURATION
S9260/S9261



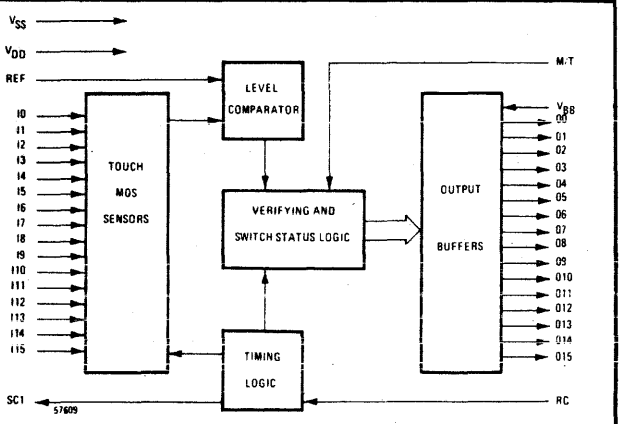
PIN/PACKAGE CONFIGURATION
S9263/S9264/S9265

General Description

These TouchControl interface circuits can be connected to either seven (S9260/S9261) or sixteen (S9263/S9264/S9265) touch switches. For each switch input, there is a corresponding separate output. The outputs are open drain with their sources connected in common to supply input V_{BB}. This permits the driving of TTL as well as MOS circuits, by varying the V_{BB} voltage. The M/T input controls operation of the outputs. In the momentary mode (M) output is active only while the touch switch is being activated (touched by the operator). In the toggle mode (T), alternate actuations of a touch switch will cause its associated output to latch either on or off. On the S9260 and S9263, the M/T input affects all outputs. On the S9261, S9264, and S9265, several switch inputs are permanently fixed in the momentary mode, thus allowing both momentary and toggle switch actuation to be implemented simultaneously.



BLOCK DIAGRAM – S9260/S9261 (7 SWITCHES)



BLOCK DIAGRAM – S9263/S9264/S9265 (16 SWITCHES)

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ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS}:	+ 0.3V to - 20V	Storage temperature (Ambient)	- 65°C to + 150°C
Operating temperature range:	0°C to + 50°C		

**FOR MULTIPLEXED TOUCHCONTROL CIRCUITS SEE AMI S9262 and S9266.*

ELECTRICAL CHARACTERISTICS

($0°C < T_A < 50°C$; $V_{SS} = 0V$; $V_{DD} = -13.5V$ to $-18.0V$ unless otherwise specified.)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IL}	Input logic 0 level – all except "I" inputs.	+ 0.3	0	- 1.5	Volts	Note: M/T input is internally pulled up to V_{SS}
V_{IH}	Input logic 1 level – all except "I" inputs	- 10.0	- 12.0	- 18.0	Volts	
f_{RC}	Internal oscillator frequency measured at RC input.	50		100	kHz	
T_S T_{RST}	Switch delay time Time to reset all latches using M/T input.	50	 100	200	msec msec	Frequency measured at RC Input = 50 kHz
V_{OL} V_{OH}	Output low voltage Output high voltage	V_{SS}		- 1.0 V_{DD}	Volts	$V_{BB} = V_{SS}$; 10K resistive load to V_{DD}
V_{OL} V_{OH}	Output low voltage Output high voltage	V_{SS} V_{BB} + 0.4		V_{SS} - 0.5 V_{BB}	Volts	V_{SS} = +5V; V_{BB} = 0V V_{DD} = 12V; 2800Ω resistive load to V_{SS}
SC1	Scan clock output: Output low voltage Output high voltage	 V_{SS}		 - 1.5 V_{DD}		Max. capacitive loading < 150 pF

OPERATION

Device operation can be understood by referring to Figure 1, depicting a typical application of the S9263. Each of the sixteen pairs of series capacitors labeled S1 – S16 is one touch switch located on a TouchControl panel. (For details on touch panel configuration and operation, see the TouchControl application note included in this APD.) In each capacitor pair, the two common plates represent the conductive area on the control panel surface that is to be touched. The other two plates are formed by two conductive surfaces parallel to the touched surface and located directly under it on the reverse side of the panel. Referring again to Figure 1, the S9263 generates a clock signal on output SC1 that is applied to one plate of each capacitor pair; this signal passes through the two series capacitors and is detected in the MOS circuit. When a panel switch surface is touched, the signal level into the chip dimishes, and the on-chip differential amplifier senses the change and performs the appropriate switching function. For example, if surface S1 is touched, the signal at input 13 decreases, and output 03, normally open, now becomes active and drives the S1 input to the TTL circuitry toward voltage level V_{BB}.

I INPUTS

Inputs from the touch switch pads to the TouchControl circuit are labeled I0 through I15 (S9263, S9264, and S9265) or I0 through I6 (S9260 and S9261). Each I input relates directly to an O output of identical numeral.

RC INPUT

A resistor connected to V_{DD} and a capacitor connected to V_{SS} are connected to the RC input pin to establish the on-chip clock frequency that controls the touch switch delay time. Nominal values for these components are suggested in Figure 1, but they may be varied to change clock frequency over a range of 50 kHz to 100 kHz.

REF INPUT

In order to allow flexibility in the choice of TouchControl panel materials, switch layout, and switch size, AMI Touch Control inputs have been designed to detect a differential change rather than an absolute change in level. To obtain a reference level, two resistors are connected to input REF, one to V_{SS} and the other to V_{DD}.

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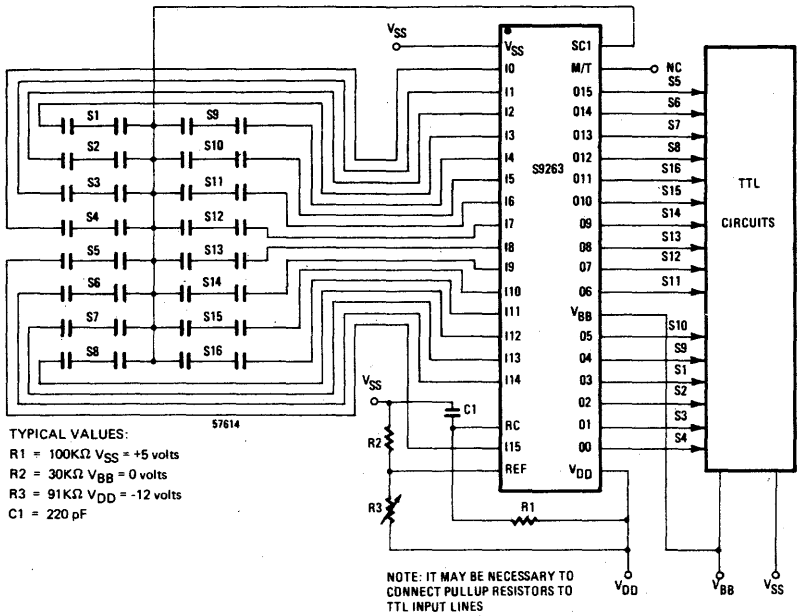


FIGURE 1. 16 SWITCH APPLICATION USING S9263

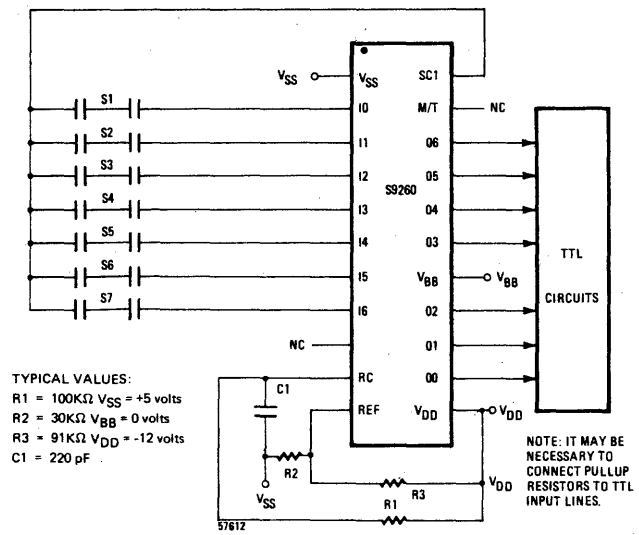
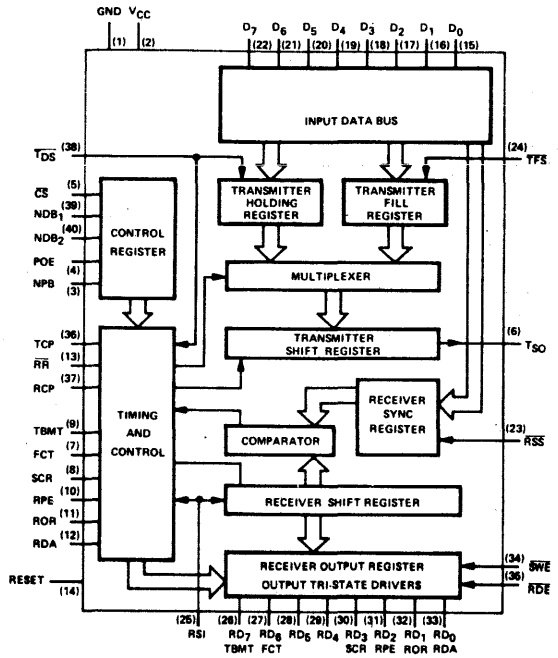


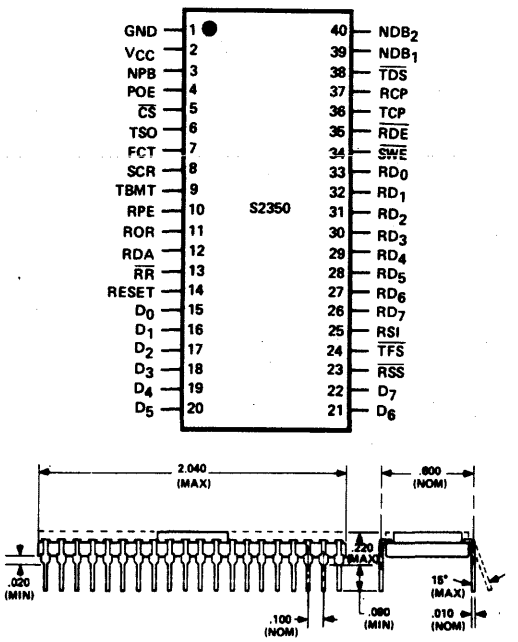
FIGURE 2. 7 SWITCH APPLICATION USING S9260

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Universal Synchronous Receiver/Transmitter (USRT)



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- 500 KHz Data Rates
- Internal Sync Detection
- Fill Character Register
- Double Buffered Input/Output
- Bus Oriented Outputs
- 5–8 Bit Characters
- Odd/Even or No Parity
- Error Status Flags
- Single Power Supply (+5v)
- Input/Output TTL Compatible

FUNCTIONAL DESCRIPTION

The S2350 Universal Synchronous Receiver Transmitter (USRT) is a single chip MOS/LSI device that totally replaces the serial to parallel and parallel to serial conversion logic required to interface a word parallel controller or data terminal to a bit-serial, synchronous communication network.

The USRT consists of separate receiver and transmitter sections with independent clocks, data lines and status. Common with the transmitter and receiver are word length and parity mode. Data is transmitted and received in a NRZ format at a rate equal to the respective input clock frequency.

Data messages are transmitted as a contiguous character stream, bit synchronous with respect to a clock and character synchronous with respect to framing or "sync" characters initializing each message. The USRT receiver compares the contents of the internal Receiver Sync Register with the incoming data stream in a bit transparent mode. When a compare is made, the receiver becomes character synchronous formatting a 5, 6, 7, or 8 bit character for output each character time. The receiver has an output buffer register allowing a full character time to transfer the data out. The receiver status outputs indicate received data available (RDA), receiver overrun (ROR), receive parity error (RPE) and sync character received (SCR). Status bits are available on individual output lines and can also be multiplexed onto the output data lines for bus organized systems. The data lines have tri-state outputs.

The USRT transmitter outputs 5, 6, 7, or 8 bit characters with correct parity at the transmitter serial output (TSO). The transmitter is buffered to allow a full character time to respond to a transmitter buffer empty (TBMT) request for data. Data is transmitted in a NRZ format changing on the positive transition of the transmitter clock (TCP). The character in the transmitter fill register is inserted into the data message if a data character is not loaded into the transmitter after a TBMT request.

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TYPICAL APPLICATIONS

- Computer Peripherals
- Communication Concentrators
- Integrated Modems
- High Speed Terminals
- Time Division Multiplexing
- Industrial Data Transmission

ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0°C to + 70°C
Storage temperature	–65°C to +150°C
Positive voltage on any pin with respect to GROUND	+7 volt
Negative voltage on any pin with respect to GROUND	–0.5 volt
Power dissipation	0.75 watt

DC (STATIC) CHARACTERISTICS*

V_{CC} = +5V ±5V ±5%, T_A = 25°C unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{IH}	Input High Voltage	2.0	V_{CC}	Volt	
V_{IL}	Input Low Voltage	- 0.5	+0.8	Volt	
I_{IL}	Input Leakage Current		10	μa	V_{IN} = OTO V_{CC} Volts
V_{OH}	Output High Voltage	2.4		Volts	I_{OH} = –100μa
V_{OL}	Output Low Voltage		+0.4	Volts	I_{OL} = 1.6ma
C_{IN}	Input Capacitance		10	pf	V_{IN} = 0 Volt, f = 1.0 MHZ
C_{OUT}	Output Capacitance		12	pf	
I_{CC}	V_{CC} Supply Current		100	ma	No Load

*Electrical characteristics included in this advanced product description are objective specifications and may be subject to change.

AC (DYNAMIC) CHARACTERISTICS

V_{CC} = +5V ±5%, T_A = 25°C unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Condition
TCP, RCP	Clock Frequency	DC	500	KHz	

Input Pulse Widths

P_{TCP}	Transmit Clock	900		nsec	C_L = 20pf
P_{RCP}	Receive Clock	900		nsec	1TTL Load
P_{RST}	Reset	500		nsec	
$P_{\overline{TDS}}$	Transmit Data Strobe	200		nsec	
$P_{\overline{TFS}}$	Transmit Fill Strobe	200		nsec	
$P_{\overline{RSS}}$	Receive Sync Strobe	200		nsec	
$P_{\overline{CS}}$	Control Strobe	200		nsec	
$P_{\overline{RDE}}$	Receive Data Enable	400		nsec	Note 1
$P_{\overline{SWE}}$	Status Word Enable	400		nsec	Note 1
$P_{\overline{RR}}$	Receiver Restart	500		nsec	

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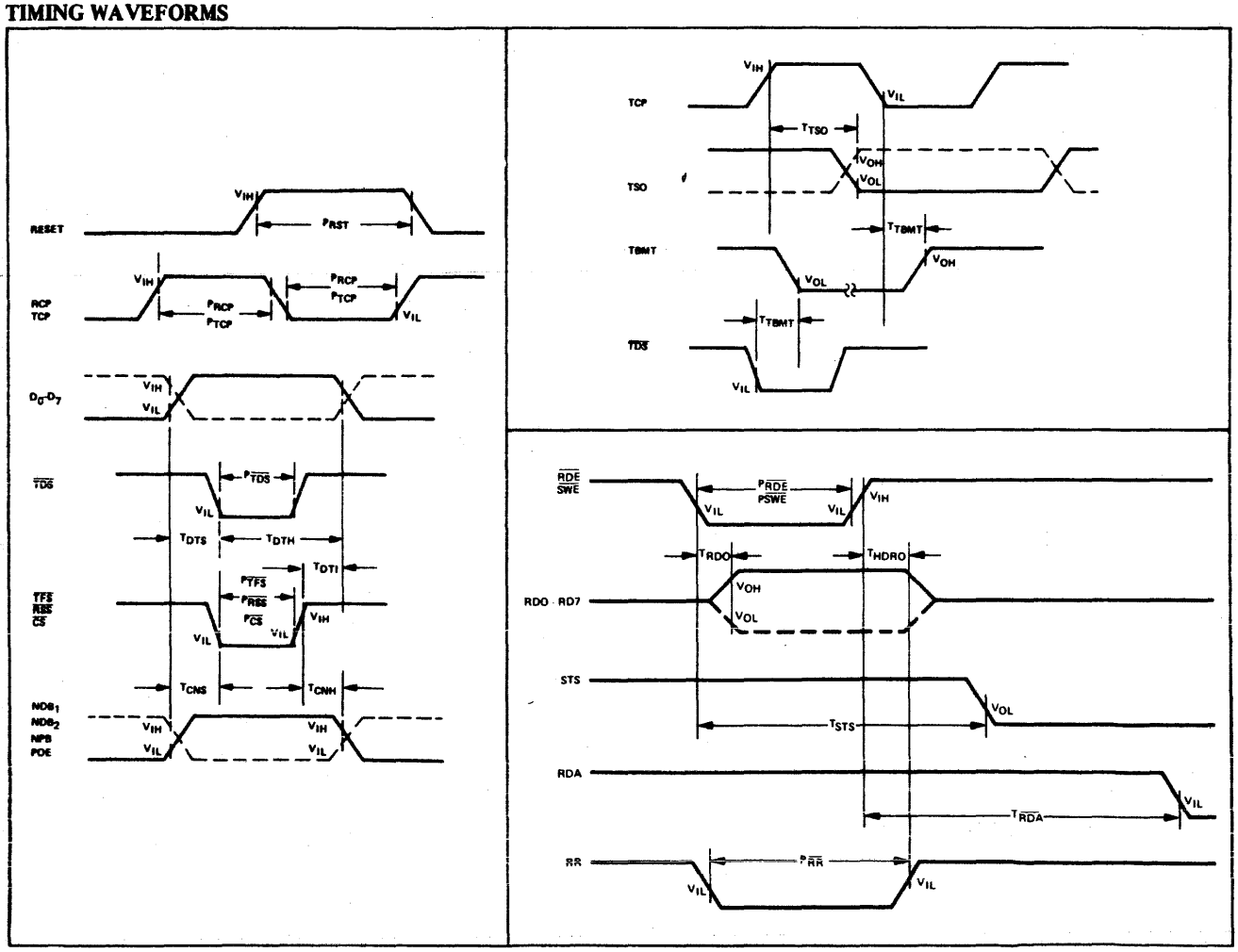
AC (DYNAMIC) CHARACTERISTICS (CONT'D)

SWITCHING CHARACTERISTICS

T_{TSO}	Delay, TCP Clock to Serial Data Out		700	nsec	
T_{TBMT}	Delay, TCP Clock to TBMT Output		1.4	μsec	
T_{TBMT}	Delay, $\overline{TDS}$ to TBMT		700	nsec	
T_{STS}	Delay, $\overline{SWE}$ to Status Reset		700	nsec	
T_{RDO}	Delay, $\overline{SWE}$, $\overline{RDE}$ to Data Outputs		400	nsec	1TTL Load
T_{HRDO}	Hold Time $\overline{SWE}$, $\overline{RDE}$ to Off State		400	nsec	C_L = 130 pf
T_{DTS}	Data Set Up Time $\overline{TDS}$, $\overline{TFS}$, $\overline{RSS}$, $\overline{CS}$	0		nsec	
T_{DTH}	Data Hold Time $\overline{TDS}$	700		nsec	
T_{DTI}	Data Hold Time $\overline{TFS}$, $\overline{RSS}$	200		nsec	
T_{CNS}	Control Set Up Time NDB1, NDB2, NPB, POE	0		nsec	
T_{CNH}	Control Hold Time NDB1, NDB2, NPB, POE	200		nsec	
T_{RDA}	Delay $\overline{RDE}$ to $\overline{RDA}$ Output	700		nsec	

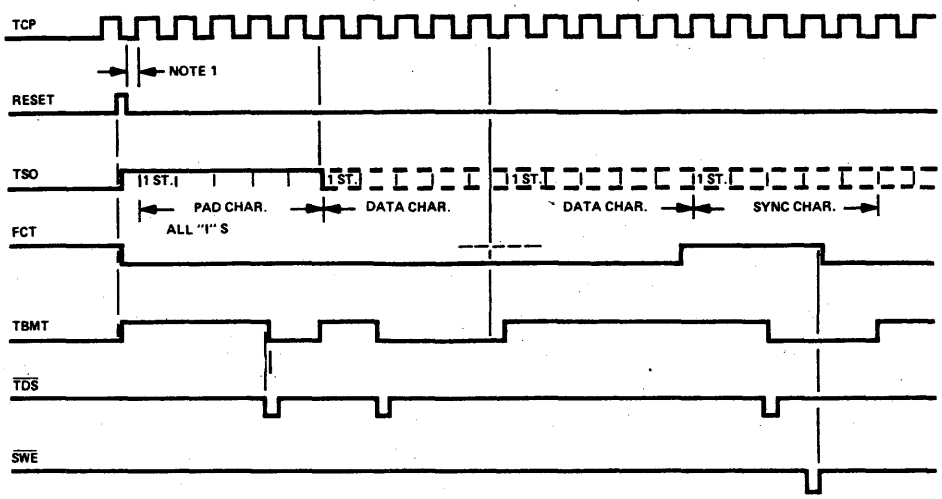
NOTE 1: Required to reset status and flags.

TIMING WAVEFORMS



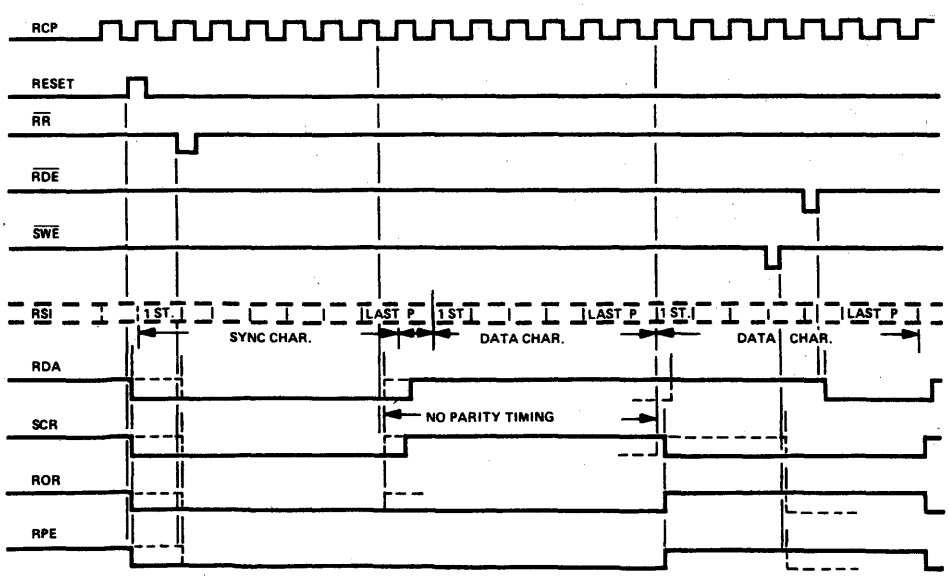
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TRANSMITTER TIMING DIAGRAM



NOTE 1 DATA TRANSMISSION WILL START ON THE FIRST LOW TO HIGH TRANSITION OF TCP AFTER RESET IS LOW. THE INITIAL RESET PULSE SHOULD NOT OCCUR UNTIL 100 MICROSECONDS AFTER POWER IS APPLIED.

RECEIVER TIMING DIAGRAM

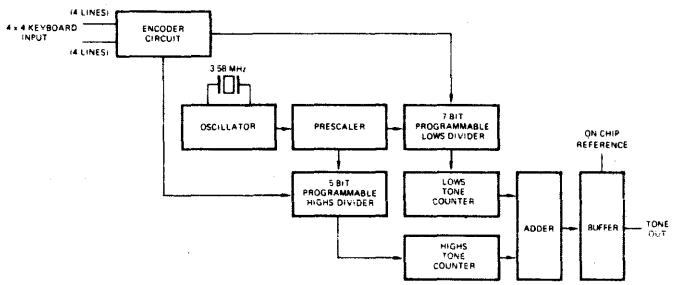


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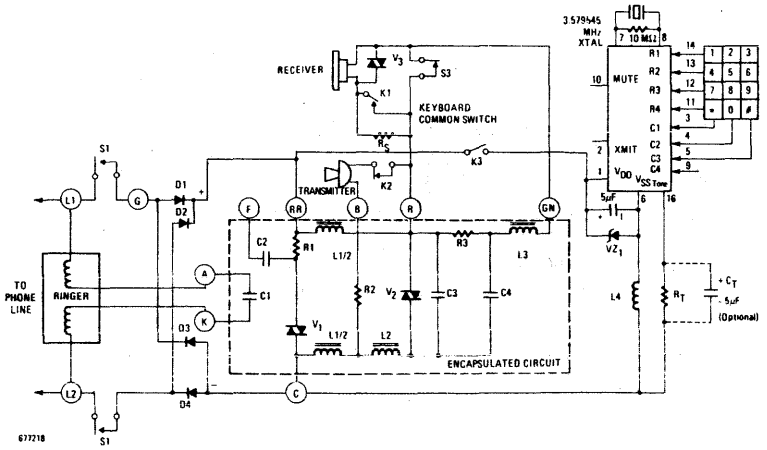
Two-of-Eight Digital Tone Generator

FEATURES

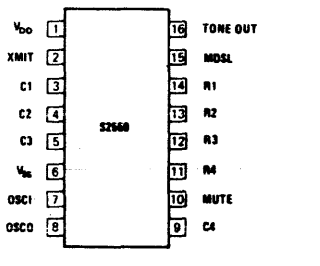
- Wide Operating Supply Voltage Range: 3.5 to 13 Volts.
- Low Power CMOS Circuitry Allows Device Power to be Derived Directly From the Telephone Lines or from Small Batteries, e.g., 9V.
- Uses TV Crystal Standard (3.58 MHz) to Derive All Frequencies Thus Providing Very High Accuracy and Stability.
- Mute and Transmitter Drivers On Chip.
- Interfaces Directly to a Standard Telephone Push-Button Keyboard.
- Digitally Synthesized Sine Wave for Individual Tones. The Harmonic Distortion is Well Below Industry Specification.
- On Chip Generation of a Reference Voltage to Assure Amplitude Stability of the Dual Tones Over the Operating Voltage and Temperature Range.
- Dual Tone as Well as Single Tone Capability.

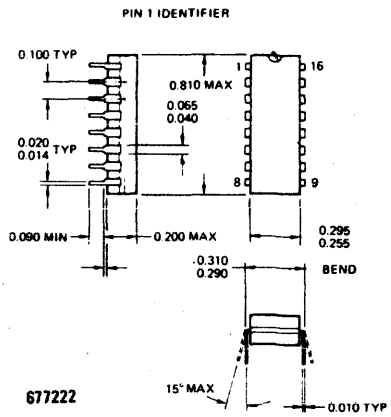


S2559 DIGITAL TONE GENERATOR BLOCK DIAGRAM



500 TYPE TELEPHONE SET MODIFIED FOR DUAL TONE SIGNALING



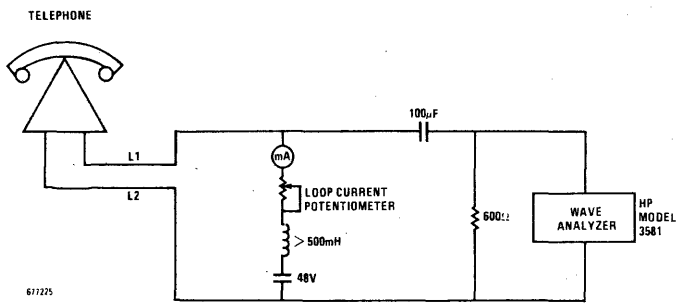


16 PIN PACKAGE CONFIGURATION (PLASTIC OR CERAMIC PACKAGE)

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ELECTRICAL SPECIFICATIONS All Parameters measured at 25°C in Circuit of Figure 1.

SYMBOL	PARAMETERS/CONDITIONS		V+ to V-	LIMITS MIN	LIMITS MAX	UNIT
	OUTPUT VOLTAGE					
VTL	Low Tone	RL = 600Ω	5.0	490	660	mVrms
VTH	High Tone	RL = 600Ω	5.0	650	880	mVrms
VTL	Low Tone	RL = 320Ω	12.0	440	600	mVrms
VTH	High Tone	RL = 320Ω	12.0	590	790	mVrms
dBhl	Ratio of High to Low Tone		–	1.75	3.75	dB
THD	Distortion (any dual frequency)				10.0	%
	OUTPUT CURRENT					
IOL	OSC	VIL = 0.5V	3.5	0.34		mA
IOH		VIH = 3.0V	3.5		- 0.23	mA
IOL	Mute	VOL = 0.5V	3.0	0.20		mA
IOL		VOL = 0.5V	10.0	0.50		mA
IOH		VOH = 2V	3.0		- 0.20	mA
IOH		VOH = 9V	10.0		- 0.50	mA
tsu	Oscillator Startup Time		3.5		6.0	ms
VDD	Operating Supply Voltage			3.5	13.5	V
	SUPPLY CURRENT					
IDD	Standby (No key selected XMIT disconnected)		13.0		130	μA
	Operating (One key selected XMIT disconnected)		5.0		18	mA
	INPUT VOLTAGE (Row and Column Inputs)					
VIL	"0" Level		3.5		0.5	V
			13.5		3.0	
VIH	"1" Level		3.5	3.2		
			13.5	10.0		
	INPUT CURRENT (Row and Column Inputs)					
IIH	Pullup	VIH = 3.0V	3.5	- .45		mA
		VIH = 13.0V	13.5	- 1.48		
IIL	Pulldown	VIL = 2.1V	3.5		.1	
		VIL = 9.1V	13.5		.6	
	OUTPUT VOLTAGE					
VOL	Mute, No Load		3.5		0.4	V
			13.5		1.0	
VOH			3.5	2.6		
			13.5	10.0		
VOH	XMIT	IOH = 0mA	3.5			
		IOH = 15mA	3.5	1.5		
		IOH = 0mA	13.5			
		IOH = 50mA	10.0	8.0		



TEST CIRCUIT FOR MEASUREMENTS OF AMPLITUDE/LOOP CURRENT AND DISTORTION

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Key Pulser

Features

- ☐ Low Voltage CMOS Process for Direct Operation From Telephone Lines
- ☐ Inexpensive R-C Oscillator Design Provides Better than ±3% Accuracy Over Supply Voltage, Temperature and Unit to Unit Variations
- ☐ Dialing Rate Can Be Varied By Changing the Dial Rate Oscillator Frequency
- ☐ Dial Rate Select Input Allows Changing of the Dialing Rate by a 2:1 Factor Without the Need of Changing Oscillator Components
- ☐ Two Selections of Mark/Space Ratios (33-1/3 /66-2/3 or 40/60)
- ☐ Twenty Digit Memory for Input Buffering and for Redial With Access Pause Capability
- ☐ Mute and Dial Pulse Drivers on Chip
- ☐ Accepts Standard Telephone DPCT Keypad or SPST Switch X-Y Matrix Keyboard Arranged in a 2 of 7 Format; Also Capable of Logic Interface
- ☐ Ignores Multi Key Entries

General Description

The S2560 Key Pulser is a CMOS integrated circuit that converts pushbutton inputs to a series of pulses suitable for telephone dialing. It is intended as a replacement for the mechanical telephone dial and can operate directly from the telephone lines with minimum interface. Storage is provided for 20 digits, therefore, the last dialed number is available for redial until a new number is entered.

Unique Features of S2560A (18 Pin Package)

IDP scaled to the dialing rate such as to produce smaller IDP at higher dialing rates. Additionally, the IDP can be changed by a 2:1 factor at a given dialing rate by means of the IDP select input.

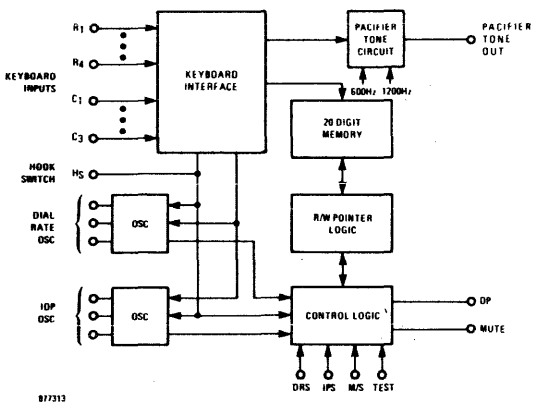
Unique Features of S2560B (24 Pin Package)

Separate IDP oscillator for selecting an IDP independent of the dialing rate. Provision for changing of the IDP by a 2:1 factor without the need of changing external components.

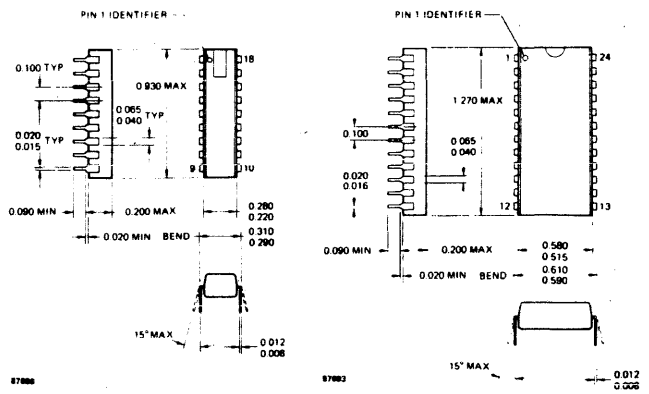
Alternating pacifier tone output simulates dual tone effects coincident with each keyboard number entry.

Data subject to change at any time without notice. These sheets transmitted for information only.

Block Diagram



Physical Dimensions



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Absolute Maximum Ratings

Supply Voltage	+5.5V
Operating Temperature Range	- 40°C to +85°C
Storage Temperature Range	- 40°C to +125°C
Voltage at Any Pin	V_{SS} - 0.3V to V_{DD} + 0.3V
Lead Temperature (Soldering, 10 Seconds)	300°C

Electrical Characteristics Specifications apply over the operating temperature range and $1.5V \leqslant V_{DD}$ to $V_{SS} \leqslant 3.5V$ unless otherwise specified.

Symbol	Parameter	V_{DD}-V_{SS} (Volts)	Min.	Max.	Units	Conditions
	Output Current Levels					
I_{OLDP}	$\overline{DP}$ Output Low Current	3.5	125		µA	V_{OUT} = 0.4V
I_{OHDP}	$\overline{DP}$ Output High Current	1.5 3.5	-20 -125		µA µA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLM}	$\overline{MUTE}$ Output Low Current	3.5	125		µA	V_{OUT} = 0.4V
I_{OHM}	$\overline{MUTE}$ Output High Current	1.5 3.5	-20 -125		µA µA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLT}	Tone Output Low Current	1.5	20		µA	V_{OUT} = 0.4V
I_{OHT}	Tone Output High Current	1.5	-20		µA	V_{OUT} = 1V
I_{DD}	Quiescent Current	3.5		1	µA	"On Hook" $\overline{HS}$ = V_{DD}
I_{IL}, I_{IH}	Input Current Any Pin (Keyboard Inputs)	3.5	1	10	µA	V_{IN} = V_{SS} or V_{DD}
I_{IL}, I_{IH}	Input Current Any Other Pin	3.5		100	nA	V_{IN} = V_{SS} or V_{DD}
I_{DD}	Operating Current	3.5 3.5		20 60	µA µA	$\overline{DP}$, $\overline{MUTE}$ open, $\overline{HS}$=V_{SS} ("Off Hook") Keyboard processing and dial pulsing space fo = 2400Hz $\overline{DP}$, $\overline{MUTE}$ sourcing 20µA, other conditions as above
fo	Oscillator Frequency	1.5		10	kHz	
Δfo/fo	Frequency Deviation	1.5 to 2.5 2.5 to 3.5	-3 -3	+3 +3	% %	Fixed R-C oscillator components $50k\Omega \leqslant R_D \leqslant 750k\Omega$; $100pF \leqslant C_D^* \leqslant 3000pF$; $1M\Omega \leqslant R_E \leqslant 5M\Omega$ *330pF most desirable value for C_D. Indicated and over the operating temperature range and unit to unit variations
	Input Voltage Levels					
V_{IH}	Logical "1"		V_{DD} - 0.25	V_{DD}	V	
V_{IL}	Logical "0"		V_{SS}	V_{SS} + 0.25	V	
C_{in}	Input Capacitance Any Pin			7.5	pF	

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leqslant V_I \leqslant V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded.

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Tone Ringer

Features

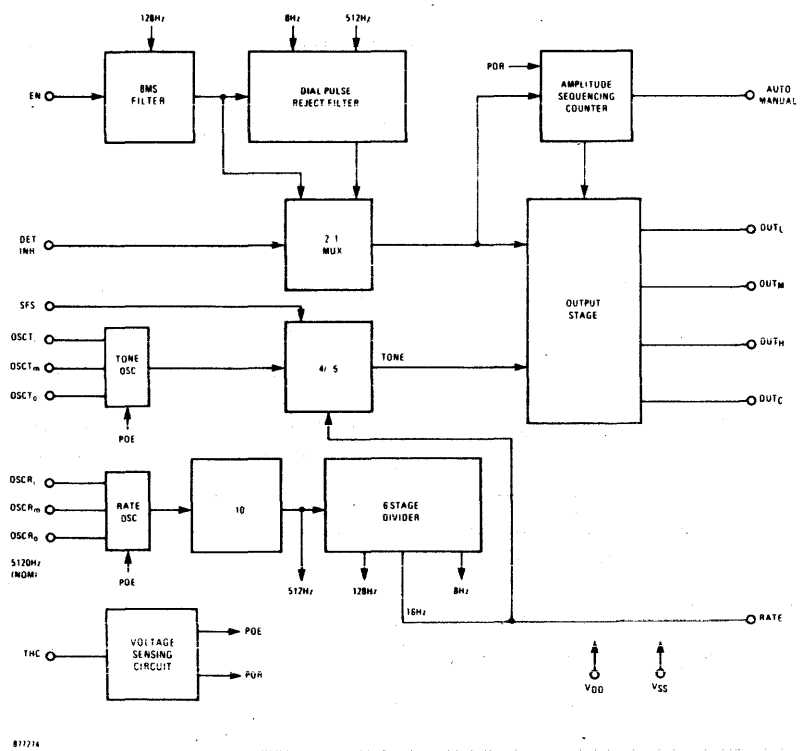
- ☐ CMOS Process for Low Power Operation
- ☐ Operates Directly from Telephone Lines with Simple Interface
- ☐ Also Capable of Logic Interface for Non-Telephone Applications
- ☐ Provides a Tone Signal that Shifts Between Two Predetermined Frequencies at Approximately 16Hz to Closely Simulate the Effects of the Telephone Bell
- ☐ Push-Pull Output Stage Allows Direct Drive, Eliminating Capacitive Coupling and Provides Increased Power Output
- ☐ 50mW Output Drive Capability at 10V Operating Voltage
- ☐ Auto Mode Allows Amplitude Sequencing such that the Tone Amplitude Increases in Each of the First Three Rings and Thereafter Continues at the Maximum Level
- ☐ Single Frequency Tone Capability

General Description

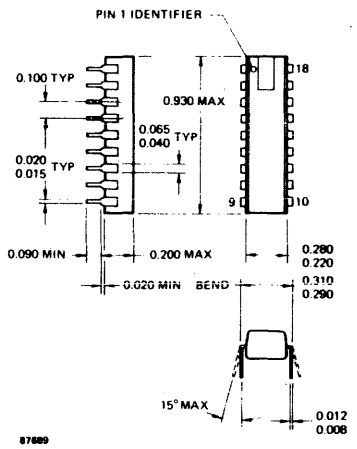
The S2561 Tone Ringer is a CMOS integrated circuit that is intended as a replacement for the mechanical telephone bell. It can be powered directly from the telephone lines with minimum interface and can drive a speaker to produce sound effects closely simulating the telephone bell.

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Block Diagram



Physical Dimensions



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Absolute Maximum Ratings

Supply Voltage	+13.5V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Voltage at Any Pin	V_{SS} - 0.3V to V_{DD} + 0.3V
Lead Temperature (Soldering, 10sec)	300°C

Electrical Characteristics Specifications apply over the operating temperature range and $3.5V \leq V_{DD}$ to $V_{SS} < 13.5V$ unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{DS}	Operating Voltage (V_{DD} to V_{SS})	7.5	13.5	V	Ringing, THC pin open
V_{DS}	Operating Voltage	3.5		V	"Auto" mode, non-ringing
I_{DS}	Operating Current		100	μA	Non-ringing, V_{DD} = 10V, THC pin open
I_{DS}	Operating Current		25	μA	Non-ringing, V_{DD} = 6V, THC pin open
	Output Drive				
I_{OHC}	Output Source Current (OUT_H, OUT_C outputs)	5		mA	V_{DD} = 10V, V_{OUT} = 9V
I_{OLC}	Output Sink Current (OUT_H, OUT_C outputs)	5		mA	V_{DD} = 10V, V_{OUT} = 0.5V
I_{OHM}	Output Source Current (OUT_M output)	2		mA	V_{DD} = 10V, V_{OUT} = 9V
I_{OLM}	Output Sink Current (OUT_M output)	2		mA	V_{DD} = 10V, V_{OUT} = 0.5V
I_{OHL}	Output Source Current (OUT_L output)	1		mA	V_{DD} = 10V, V_{OUT} = 9V
I_{OLL}	Output Sink Current (OUT_L output)	1		mA	V_{DD} = 10V, V_{OUT} = 0.5V
	CMOS to CMOS				
V_{IH}	Input Logic "1" Level	0.7 V_{DD}	V_{DD} + 0.3	V	All inputs
V_{IL}	Input Logic "0" Level	V_{SS} - 0.3	0.3 V_{DD}	V	All inputs
V_{OH}	Output Logic "1" Level	0.9V_{DD}		V	All outputs except OUT_C, OUT_H, OUT_M and OUT_L. I_O = -10μA
V_{OL}	Output Logic "0" Level		0.5	V	All outputs except OUT_C, OUT_H, OUT_M and OUT_L. I_O = 10μA
V_{OZ}	Output Leakage Current (OUT_H, OUT_M outputs in high impedance state)		1 -1	μA μA	V_{DD} = 10V, V_{OUT} = 0V V_{DD} = 10V, V_{OUT} = 10V
C_{in}	Input Capacitance		7.5	pF	Any pin
Δfo/fo	Oscillator Frequency Deviation	-3	+3	%	Fixed RC component values $1M\Omega \leq R_{si}, R_{ti} \leq 5M\Omega$; $100k\Omega \leq R_{sm}, R_{tm} \leq 750k\Omega$ $150pF \leq C_{so}, C_{to} \leq 3000pF$ 330pF recommended value of C_{so} and C_{to}, supply voltage varied from 9V ± 2V (over temperature and unit-unit variations)
R_{LOAD}	Output Load Impedance Connected Across OUT_H and OUT_C	600		Ω	Tone Frequency Range = 300Hz to 3400Hz
I_{IH}, I_L	Leakage Current, V_{in} = V_{DD} or V_{SS}		100	nA	Any input, V_{DD} = 10V
V_{TH}	Internal Threshold Voltage	6.5	8	V	Measured at THC pin; V_{DD} > 8V

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leq V_I \leq V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded.

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Repertory Dialer

Features

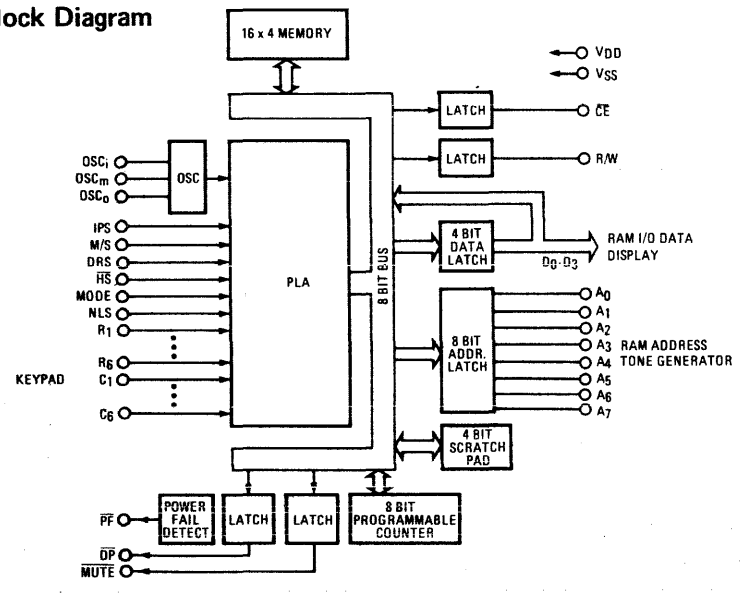
- ☐ CMOS Process Achieves Low Power Operation
- ☐ 8 or 16 Digit Number Capability (Pin Programmable)
- ☐ Dial Pulse and Mute Output
- ☐ Tone Outputs Obtained by Interfacing with Standard AMI S2559 Tone Generator
- ☐ Two Selections of Dial Pulse Rate
- ☐ Two Selections of Inter-Digit Pause
- ☐ Two Selections of Mark/Space Ratio (33-1/3 / 66-2/3 or 40/60)
- ☐ Memory Storage of 32 8-Digit Numbers or 16 16-Digit Numbers with Standard AMI S5101 RAM
- ☐ 16-Digit Memory for Input Buffering and for Redial with Access Pause Capability
- ☐ Accepts the Standard Telephone DPCT Keypad or SPST Switch X-Y Matrix Keyboards; Also Capable of Logic Interface
- ☐ Ignores Multi Key Entries
- ☐ Inexpensive, but Accurate R-C Oscillator Design Provides Better Than ±3% Accuracy Over Supply Voltage, Temperature and Unit-Unit Variations and Allows Different Dialing Rates, IDP and Tone Drive Timing by Changing the Time Base
- ☐ Power Fail Detection
- ☐ BCD Output with Update for Number Display Applications

General Description

The S2562 Repertory Dialer is a CMOS integrated circuit that can perform storing or retrieving, normal dialing, redialing or auto dialing and displaying of one of several telephone numbers. It is intended to be used with the AMI standard S5101—256x4 RAM that functions as telephone number storage. With one S5101 up to 32 8-digit or 16 16-digit numbers can be stored. It can provide either dial pulses or DTMF tones with the addition of the AMI S2559 tone generator for either the dial or tone line applications.

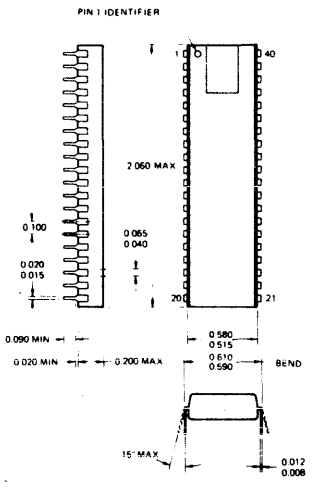
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Block Diagram



877283

Physical Dimensions



876100

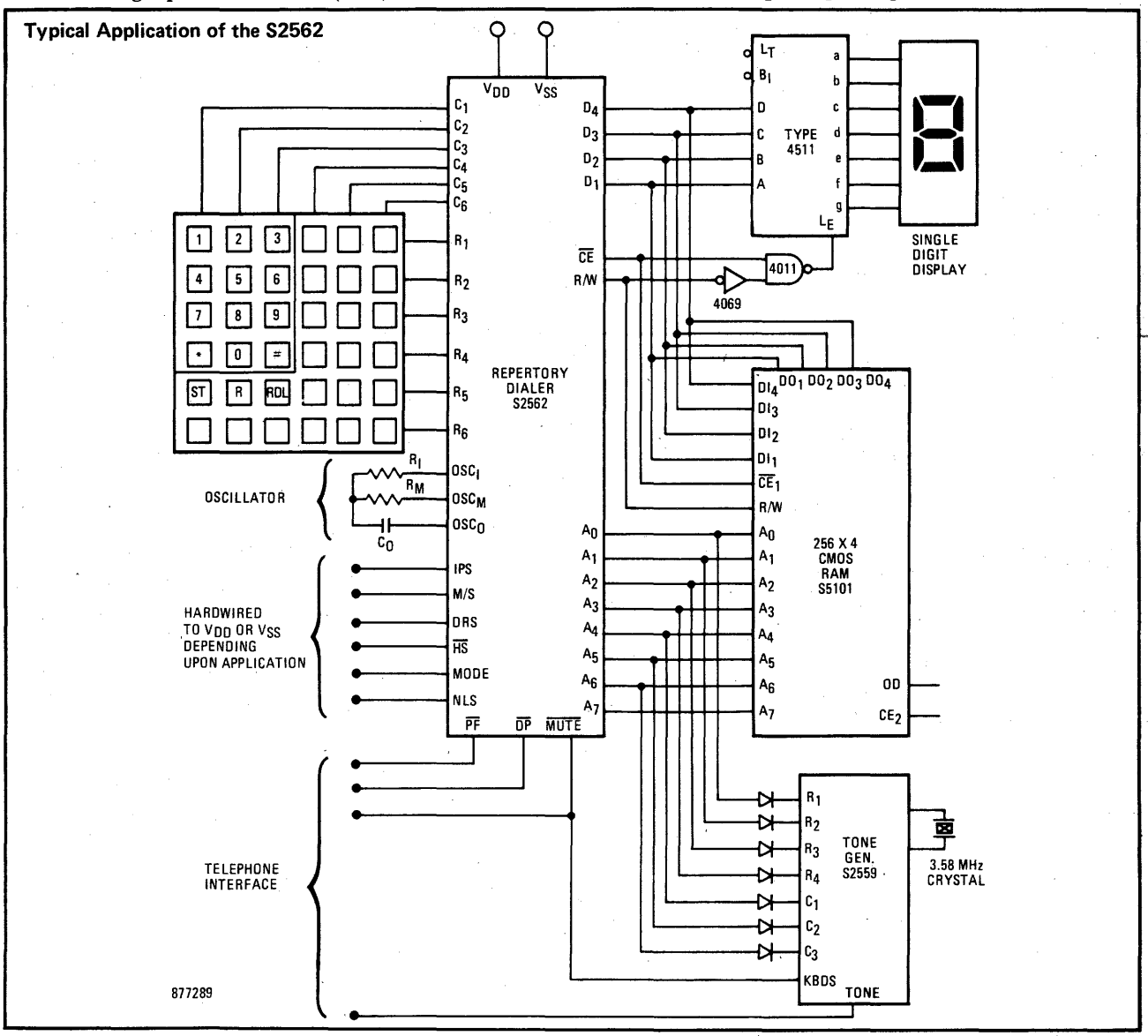
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Functional Description

The S2562 is a CMOS controller designed for storing or retrieving, normal dialing, redialing or auto dialing and displaying of one of several telephone numbers. It is intended to be used with the AMI standard S5101 256x4 RAM that functions as a telephone number storage. A single S5101 RAM will store up to 32 8-digit or 16 16-digit telephone numbers. The S2562 can be programmed to work with either 8-digit or 16-digit numbers by means of the Number Length Select (NLS) input.

The S2562 uses an inexpensive, but accurate R-C oscillator as a time base from which the dialing rate and inter-digit pause duration (IDP) are derived. Different dialing rates and IDP durations can be implemented by simply adjusting the oscillator frequency. The dialing rate and IDP can be further changed by a 2:1 factor by means of the dialing rate select (DRS) and inter-digit pause select (IPS) inputs. Thus, for the oscillator frequency of 8kHz, dialing rates of 10 and 20 pps and IDP's of 400 and 800ms can be achieved. The mark/space ratio is fixed independent of the time base and can be selected to be either 33-1/3 / 66-2/3 or 40/60 by means of M/S input. Over supply voltage (5V ±10%), operating temperature range and unit-unit variations, timing accuracy of ±3% can be achieved. A mute output is also available for muting of the receiver during dial pulsing.

Typical Application of the S2562



Single Channel PCM CODEC

Features

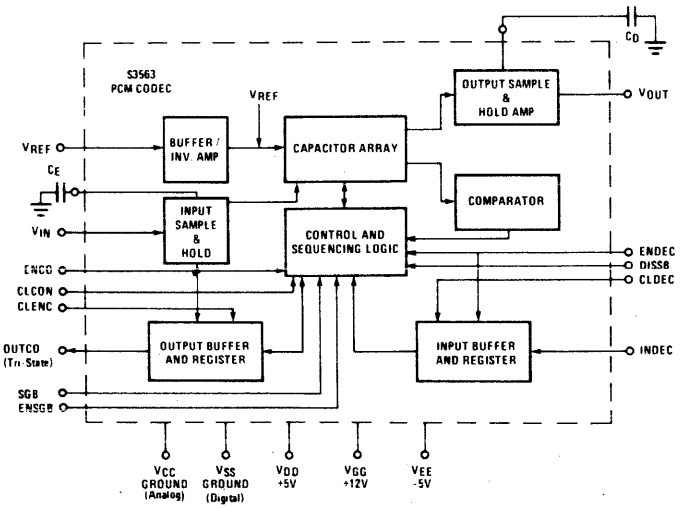
- ☐ Complete μ-Law (A-Law Option) PCM Encoder and Decoder on a Single Chip
- ☐ Time Shared Capacitor Array for Encode/Decode Functions
- ☐ Full Duplex Encode/Decode Operation Due to Input Sample and Hold Technique
- ☐ 8-Bit Companded Output for the Encoder and Full Duty Cycle PAM Sample Output for the Decoder
- ☐ Signal to Distortion Ratio Better than 22dB for Voice Signals at $-45dBV_r$
- ☐ Single Positive Polarity Reference Input
- ☐ Facility to Insert Signaling Bit in the Encoded Bit Stream
- ☐ Facility to Decode Signaling Bit Plus 7-Bit or 8-Bit PCM Word into a PAM Sample
- ☐ Reduced Power Dissipation in Non-Converting State
- ☐ Fast Conversion Time ($<30\mu s$ at 1MHz Rate)

General Description

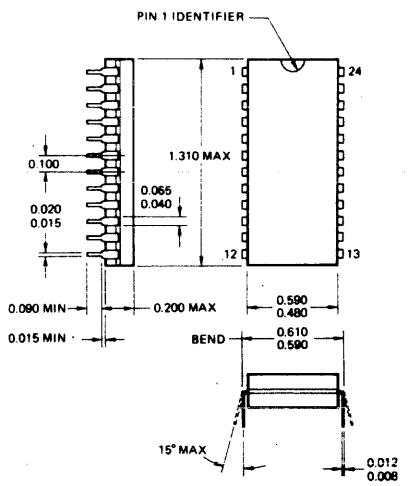
The S2563 PCM CODEC is an LSI circuit that encodes voice signals to a serial PCM data output and decodes PCM data input into analog samples representing the original voice signal. It is designed to meet the D3 channel bank specification for the implementation of a 24 channel μ-law system. A-law option is also available for the implementation of the 30/32 (CCITT) European system.

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Block Diagram



Physical Dimensions



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Absolute Maximum Ratings

DC Supply Voltages:

V_{GG} (with respect to V_{CC})	+16V
V_{EE} (with respect to V_{CC})	-8V
V_{DD} (with respect to V_{SS})	+8V

Input Voltages:

V_{IN} (analog input)	(V_{EE} - 0.5V) to (V_{GG} + 0.5V)
V_{REF}	(V_{EE} - 0.5V) to (V_{GG} + 0.5V)
$V_{DIGITAL}$	-0.5V to (V_{DD} + 0.5V)
Peak Current Drain Per Pin	10mA

Operating Temperature Range:

Plastic	0°C to +70°C
Ceramic	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C

Functional Description

The Single Channel PCM CODEC (S2563) is designed to meet the D3 channel bank specification for the implementation of a 24 channel μ-law system. A-law option is available for implementation of the 30/32 channel European system. The S2563 features time shared encode and decode circuitry. The encoding of the analog voltage sample into an 8-bit companded digital output and the decoding of an 8-bit companded digital input into an analog voltage sample is based on the charge-redistribution technique using a capacitor array. Even though the same capacitor array is employed for the encode and decode functions, full duplex performance can be achieved due to the use of a sample and hold circuit on the input analog voltage. The decode time is significantly shorter (less than 3μs) than the encode time (24μs); hence, if a decode request occurs on the ENDEC input while encoding operation is under way, it is interrupted and the decoding operation started. At the end of the decode operation, control is transferred back to the encode operation. There is no loss of information because the original analog sample is preserved by the hold circuit during the decode operation. Thus, a full duplex performance can be effectively achieved.

A single reference voltage of positive polarity (typically 2.5V) is required at the V_{REF} input. This input is internally buffered so that a single external reference circuit output may be bused to additional CODEC circuits. A negative voltage reference is derived internally from the positive reference by use of a unity gain inverting amplifier when it is determined that the polarity of the input voltage is negative. Otherwise this amplifier is used as a unity gain non-inverting buffer. The input analog voltage is applied at the V_{IN} terminal. Peak-to-peak amplitude of V_{IN} should be less than or equal to $2V_{REF}$. It is assumed that the input analog signal will be capacitively coupled into the V_{IN} terminal. The V_{IN} terminal will present a high input impedance. A continuous clock signal at nominal 1.544MHz frequency should be supplied at CLENC terminal. By making ENCO line "high," an 8-bit companded PCM word can be read out serially at the CLENC clock rate out of the encoder output buffer. The ENCO line must go "low" after 8 clock cycles of CLENC. The repetition rate of the ENCO determines the rate at which the analog input voltage will be sampled and encoded and therefore must be pulsed at the 8KHz rate.

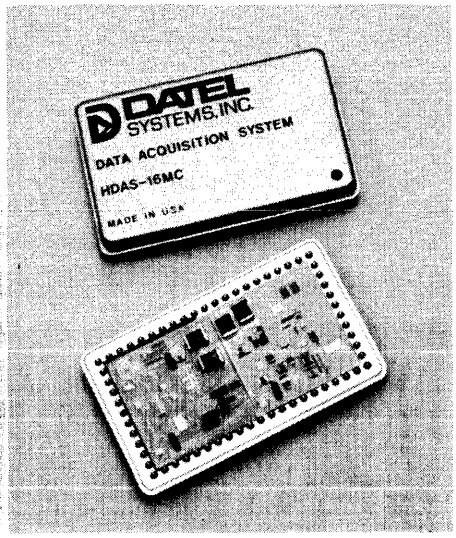
For every positive transition of the ENCO line, the old PCM data word is shifted out of the output buffer while a new analog sample is acquired simultaneously. Facility is provided for inserting the signaling bit in the encoded bit stream. When the ENSGB line is high, the data on the SGB line is substituted for the LSB of the PCM word. The decoder accepts a companded 8-bit PCM word serially at the INDEC terminal at the clock rate supplied at the CLDEC terminal when the ENDEC line is made "high." The ENDEC line must go "low" after 8 clock cycles of CLDEC. ENCO, CLENC, OUTCO, SGB, ENSGB, ENDEC, CLDEC, CLCON, and INDEC signals are TTL compatible. The OUTCO signal is a three-state output and is active when ENCO is "high." The received PCM word is decoded by the capacitor array and presented to the output sample and hold amplifier. The sample and hold amplifier holds the output voltage until a new PCM word is received. The output voltage will therefore be updated coincident with a positive transition on the ENDEC line, i.e., at the desired 8KHz rate. Facility is provided to discard the LSB of the received PCM word when DISSB line is "high" and only the most significant 7 bits are used to decode the PCM word with the LSB set to zero. When DISSB is "low" all 8 bits of the PCM word are used.

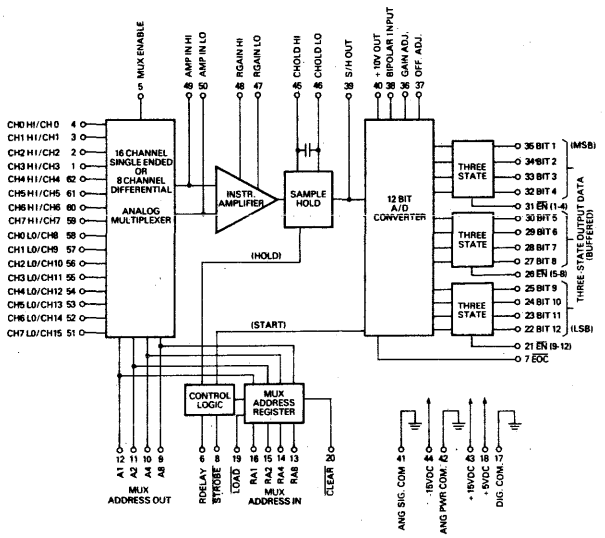
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DATEL SYSTEMS, INC.

HDAS-8, HDAS-16

12 BIT HYBRID DATA ACQUISITION SYSTEMS





FEATURES

- **12 Bit Resolution**
- **8 or 16 Channels**
- **Internal Instrumentation Amp**
- **50 kHz Throughput Rate**
- **Three State Outputs**

The HDAS-8, with 8 differential input channels, and the HDAS-16, with 16 single ended input channels, are industry's first complete 12 bit data acquisition systems in a single hybrid package. Acquisition and conversion times combined are 20μsec. maximum, giving a 50 kHz throughput rate. The 12 bit output data can be transferred out in three 4 bit bytes by means of three state data bus drivers. Output coding is straight binary for unipolar operation and offset binary for bipolar operation.

The HDAS circuitry includes an analog multiplexer, programmable gain instrumentation amplifier, sample-bold circuit with MOS hold capacitor, 10 volt buffered reference, 12 bit A/D converter, three state bus driver and digital control circuitry. The instrumentation amplifier can be programmed by a single external resistor for gains from 1 to 1000. This is an important feature for processing signals in the range of 10mV to 10 V full scale.

The internal sample-hold device has excellent characteristics and has its own self contained MOS hold capacitor. Aperture delay time is 50nsec. and hold mode droop is 1μV/μsec. Nonlinearity error is less than ½ LSB and total error is 1 LSB maximum at 50 kHz throughput rate.

The HDAS units are especially useful for microcomputer based measurement and control systems. The package is a miniature 2.3 × 1.4 × 0.24 inches

SPECIFICATIONS, Typical at 25°C

	HDAS-8	HDAS-16
No. Channels	8	16
Input Type	Single Ended	Differential
Input Range, unipolar FS	+10mV to +10 V	+10mV to +10 V
Input Range, bipolar FS	±10mV to ±10 V	±10mV to ±10 V
Common Mode Range	±11 V	—
Input Resistance	100 Meg.	100 Meg.
Input Bias Current, max.	200 pA	200 pA
Input Off. Voltage Drift	20μV/°C+(10μV/°C)G	
Input Gain Equation	G = 1+20K/RG	
Channel Addressing	3-Bit Code	4-Bit Code
Address Input Logic	DTL, TTL	DTL, TTL
Resolution	12 Bits	12 Bits
Nonlinearity Error, max.	½ LSB	½ LSB
Differential Nonlinearity, max.	½ LSB	½ LSB
Total Error, max.*	0.025%	0.025%
Gain Tempco, typ.	10 ppm/°C	10 ppm/°C
Gain Tempco, max.	30 ppm/°C	30 ppm/°C
No Missing Codes	Over Oper. Temp. Range	
Power Supply Sensitivity	0.01%/%	0.01%/%
Throughput Rate, max.	50 kHz	50 kHz
Acquisition Time	9 μsec.	9 μsec.
Conversion Time	9 μsec.	9 μsec.
Aperture Delay Time	50 nsec.	50 nsec.
Sample-Hold Droop	1 μV/μsec.	1 μV/μsec.
Feedthrough at 1 kHz, max.	0.01%	0.01%
Output Coding, unipolar	Straight Bin	Straight Bin
Output Coding, bipolar	Offset Bin.	Offset Bin.
Power Requirement	+15VDC at 67 mA max. −15 VDC at 71 mA max. +5VDC at 155 mA max.	
	Miniature 62 Pin	

*at maximim throughput rate

ORDERING INFORMATION

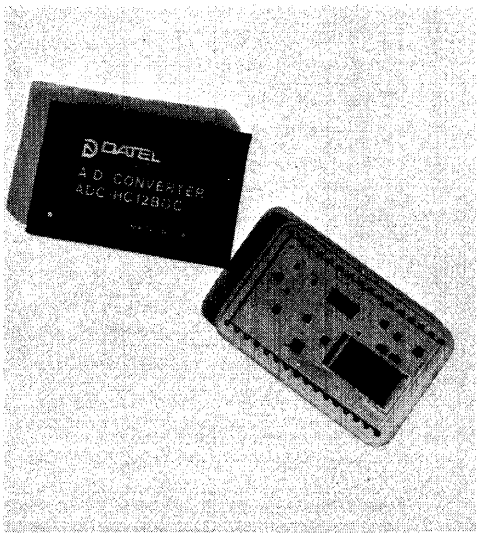
Model	Oper. Temp. Range	Seal	Price (1-9)
HDAS-8MC	0 to 70C	Hermetic	$295.00
HDAS-8MR	−25 to +85C	Hermetic	395.00
HDAS-8MM	−55 to +125C	Hermetic	695.00
HDAS-16MC	0 to 70C	Hermetic	295.00
HDAS-16MR	−25 to +85C	Hermetic	395.00
HDAS-16MM	−55 to +125C	Hermetic	695.00

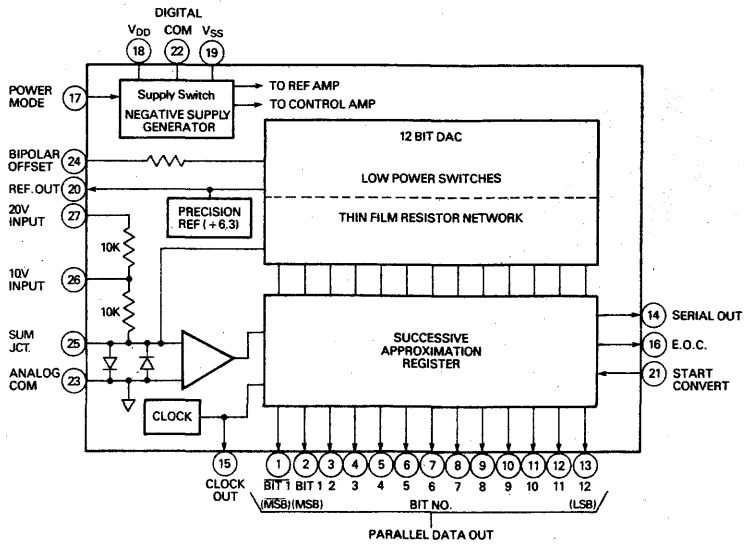
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DATEL SYSTEMS, INC.

ADC-HC12B

12 BIT, LOW POWER A/D CONVERTER





FEATURES

- **Single Supply Operation**
- **CMOS Circuitry**
- **12 Bit Resolution**
- **6 Input Voltage Ranges**
- **26 mW Consumption at 1000 Conversions/Sec.**

The ADC-HC12B is a complete, low power, 12 bit A/D converter utilizing CMOS circuitry. It is specifically designed for portable and remote instrumentation applications where low power consumption is essential; this unit operates from either a single +9 VDC to +15 VDC power source (interrupt mode) or from a dual ±9 VDC to ±15 VDC source (continuous mode). In the interrupt mode of operation the converter is initially in standby mode, drawing only 10 μA of current from the supply until a start convert pulse is applied to it. With the pulse applied the converter turns on, stabilizes, and then performs a 12 bit conversion and returns to the standby mode while the 12 bit data word is held at the output.

Power consumption is 112 milliwatts in the continuous mode and 26 milliwatts in the interrupt mode at 1,000 conversions per second. There are six different analog input voltage ranges.

SPECIFICATIONS, Typical at 25°C

	ADC-HC12B
Resolution	12 Bits
Conversion Time, continuous mode	305 μsec. max.
Conversion Time, interrupt mode	350 μsec. max.
Gain Tempco, max.	30 ppm/°C
Nonlinearity Error, max.	½ LSB
Differential Nonlinearity, max.	½ LSB
Differential Nonlinearity Tempco	2 ppm/°C of FSR
No Missing Codes	Over Op. Temp. Range
Power Supply Sensitivity	0.003%/%
Analog Input Ranges	0 to +5 V, +10 V, +20 V ±2.5 V, ±5 V, ±10 V
Input Impedance	5K, 10K, or 20K
Output Logic	CMOS
Unipolar Coding	Straight Binary
Bipolar Coding	Offset Binary Two's Complement
Power Requirement, continuous	±9 V to ±15 V
Power Requirement, interrupt	+9 V to +15 V
Package	32 Pin DIP

ORDERING INFORMATION

Model	Oper. Temp. Range	Seal	Price (1-24)
ADC-HC12BGC	0 to 70C	Epoxy	$129.00
ADC-HC12BMC	0 to 70C	Hermetic	139.00
ADC-HC12BMR	−25 to +85C	Hermetic	179.00
ADC-HC12BMM	−55 to +125C	Hermetic	219.00

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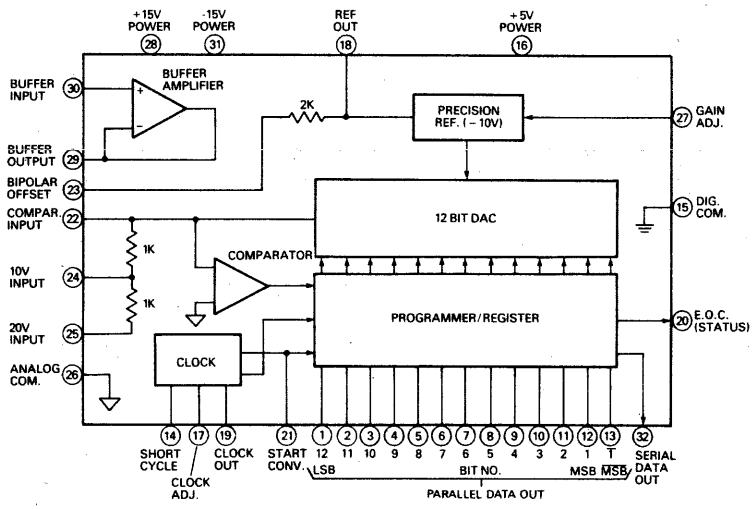
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DATEL SYSTEMS, INC.

ADC-HF12B

12 BIT, ULTRA-FAST A/D CONVERTER





FEATURES

- **12 Bit Resolution**
- **2.0 μsec. Conversion Time**
- **5 Programmable Input Ranges**
- **100 Megohm Buffer Amplifier**
- **Short Cycling Capability**

The ADC-HF12B is an ultra-fast, 12 bit A/D converter manufactured with thin film hybrid technology. Using the successive approximation technique this converter completes a 12 bit conversion in just 2 microseconds. Five different input voltage ranges are available by simple external pin connection. An input buffer amplifier is also provided for applications where 100 megohm input impedance is required.

The ADC-HF12B circuit design uses an ultra-fast DAC with 12 matched current sources; it also contains a fast comparator, precision reference, clock, successive approximation register, and buffer amplifier. A thin film R-2R resistor ladder network is actively laser trimmed for optimum linearity.

Excellent tracking of the DAC current sources results in no missing codes over the operating temperature range.

SPECIFICATIONS, Typical at 25°C

	ADC-HF12B
Resolution	12 Bits
Conversion Time, max.	2 μsec.
Gain Tempco, max.	20 ppm/°C
Nonlinearity Error, max.	½ LSB
Differential Nonlinearity, max.	½ LSB
Diff. Nonlinearity Tempco	3 ppm/°C of FSR
No Missing Codes	Over Op. Temp. Range
Power Supply Sensitivity, max.	0.01%/%
Analog Input Ranges	0 to −5 V, 0 to −10 V ±2.5 V, ±5 V, ±10 V
Input Impedance	500 Ω, 1K, 2K
Buffer Input Impedance	100 Megohms
Buffer Bias Current	125 nA
Buffer Settling Time	1 μsec.
Output Logic	TTL
Unipolar Coding	Straight Binary
Bipolar Coding	Offset Binary Two's Complement
Power Requirement	+15 VDC at 70 mA −15 VDC at 30 mA +5 VDC at 200 mA
Package	32 Pin DIP

ORDERING INFORMATION

Model	Oper. Temp. Range	Seal	Price (1-24)
ADC-HF12BGC	0 to 70C	Epoxy	$229.00
ADC-HF12BMC	0 to 70C	Hermetic	249.00
ADC-HF12BMR	−25 to +85C	Hermetic	299.00
ADC-HF12BMM	−55 to +100C	Hermetic	399.00

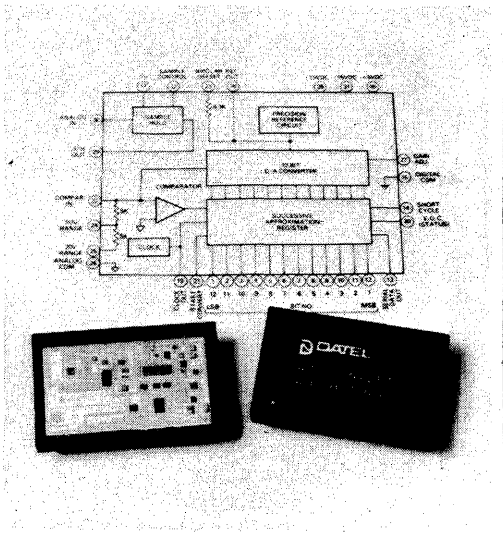
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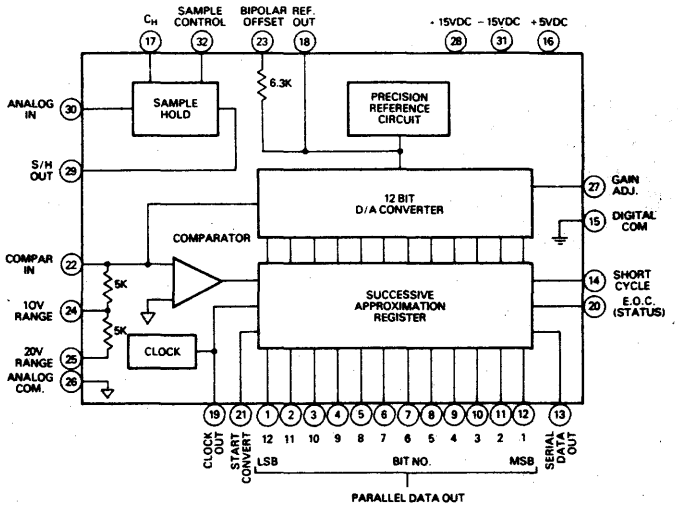
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DATEL SYSTEMS, INC.

ADC-HS12B

12 BIT A/D CONVERTER WITH SAMPLE HOLD





FEATURES

- **Internal Sample-Hold**
- **6 μsec. Acquisition Time**
- **8 μsec. Conversion Time**
- **12-Bit Resolution**
- **Programmable Input Ranges**

The ADC-HS12B is a high performance 12 bit A/D converter combined with a sample-hold in a miniature 32 pin package. It is specifically designed for systems applications where the sample-hold is an integral part of the conversion process. The sample hold has a 6 μsec. acquisition time and the A/D converter has an 8 μsec. conversion time. Five input voltage ranges are programmable by external pin connection. The input impedance to the sample-hold is 100 megohms, permitting direct connection to an analog multiplexer.

This converter incorporates proven thin film hybrid technology used in high volume production. The thin film resistor network is fabricated of nichrome on glass and then actively laser trimmed for best linearity. Other features include 20 ppm/°C gain tempco, 2 ppm/°C differential nonlinearity tempco and no missing codes over the operating temperature range.

SPECIFICATIONS, Typical at 25°C

	ADC-HS12B
Resolution	12 Bits
Acquisition Time	6 μsec.
Conversion Time, max.	8 μsec.
Gain Tempco, max.	20 ppm/°C
Nonlinearity Error, max.	½ LSB
Differential Nonlinearity, max.	½ LSB
No Missing Codes	Over Op. Temp. Range
Power Supply Sensitivity	0.002%/% max.
Analog Output Ranges	0 to +5 V, 0 to +10 V ±2.5 V, ±5 V, ±10 V
Input Impedance	100 Megohms
Input Bias Current	50 nA
Aperture Delay Time	50 nsec.
Aperture Uncertainty Time	5 nsec.
Hold Mode Droop	50 nV/μsec. max.
Hold Mode Feedthrough	0.01% max.
Output Logic	TTL
Unipolar Coding	Comp. Binary
Bipolar Coding	Comp. Offset Binary
Power Requirement	+15 VDC at 60 mA −15 VDC at 50 mA +5 VDC at 100 mA
Package	32 Pin DIP

ORDERING INFORMATION

Model	Oper. Temp. Range	Seal	Price (1-24)
ADC-HS12BGC	0 to 70C	Epoxy	$149.00
ADC-HS12BMC	0 to 70C	Hermetic	159.00
ADC-HS12BMR	−25 to +85C	Hermetic	199.00
ADC-HS12BMM	−55 to +100C	Hermetic	239.00

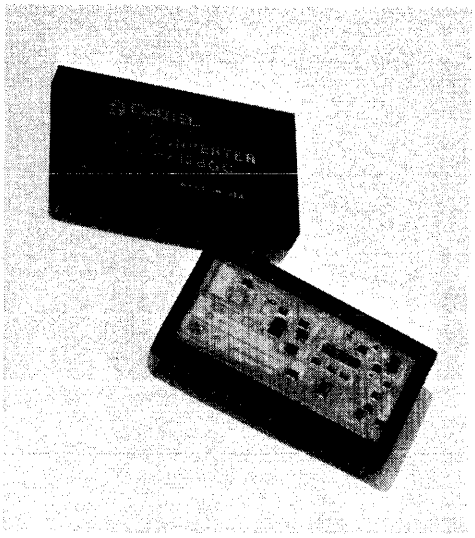
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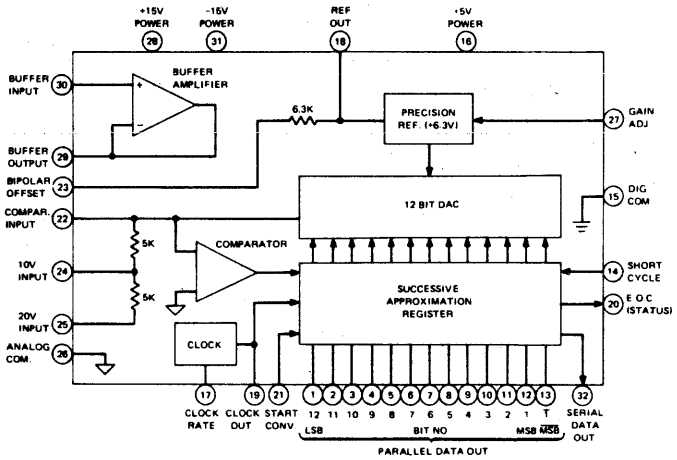
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DATEL SYSTEMS, INC.

ADC-HX12B

12 BIT, LOW COST A/D CONVERTER





FEATURES

- **12 Bit Resolution**
- **20 μsec. Conversion Time**
- **5 Programmable Ranges**
- **100 Megohm Buffer**
- **Lowest Cost**

The ADC-HX12B is a very low cost, 12 bit A/D converter which is functionally complete. It is fabricated with thin film hybrid technology to perform a conversion in 20 μsec. By means of external pin connections it can be programmed for 5 different input voltage ranges. An internal 100 megohm buffer is provided for high input impedance applications.

The circuit consists of a 12 bit DAC which employs quad current switches, a precision zener reference, a fast comparator, clock, successive approximation register, and buffer amplifier. A nichrome thin film resistor network is actively laser trimmed to achieve optimum linearity.

Output data is available in both parallel and serial forms. This converter can also be short cycled to achieve faster conversions at lower resolutions.

SPECIFICATIONS, Typical at 25°C

	ADC-HX12B
Resolution	12 Bits
Conversion Time, max.	20 μsec.
Gain Tempco, max.	20 ppm/°C
Nonlinearity Error, max.	½ LSB
Differential Nonlinearity, max.	½ LSB
Diff. Nonlinearity Tempco	2 ppm/°C of FSR
No Missing Codes	Over Op. Temp. Range
Power Supply Rejection, max.	0.002%/%
Analog Input Ranges	0 to +5 V, 0 to +10V ±2.5 V, ±5 V, ±10 V
Input Impedance	2.5 K, 5 K or 10 K
Buffer Input Impedance	100 Megohms
Buffer Bias Current	125 nA
Buffer Settling Time	3 μsec.
Unipolar Coding	Complementary Binary
Bipolar Coding	Comp. Offset Binary Comp. 2's Complement
Power Requirement	+15 VDC at 55 mA −15 VDC at 45 mA +5 VDC at 100 mA
Package	32 Pin DIP

ORDERING INFORMATION

Model	Oper. Temp. Range	Seal	Price (1-24)
ADC-HX12BGC	0 to 70C	Epoxy	$ 82.50
ADC-HX12BMC	0 to 70C	Hermetic	95.00
ADC-HX12BMR	−25 to +85C	Hermetic	125.00
ADC-HX12BMM	−55 to +100C	Hermetic	155.00

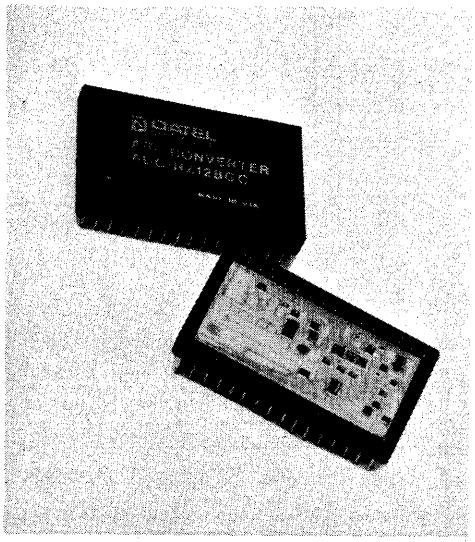
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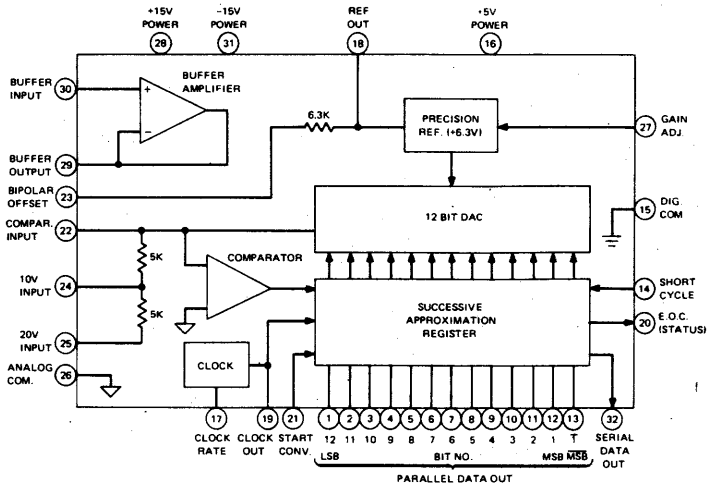
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DATEL SYSTEMS, INC.

ADC-HZ12B

12 BIT, HIGH PERFORMANCE A/D CONVERTER





FEATURES

- **8 μsec. Conversion Time**
- **20 ppm/°C Tempco**
- **5 Programmable Ranges**
- **Short Cycle Capability**
- **100 Megohm Buffer**

The ADC-HZ12B features high conversion speed in a hybrid 12 bit A/D converter. By employing a low capacitance nichrome-on-glass thin film resistor network, a conversion time of only 8 μsec. is achieved. This converter also has 5 different input voltage ranges determined by external pin connection and a 100 megohm buffer which may be connected if desired.

This ADC-HZ12B is functionally complete, incorporating a 12 bit DAC, precision reference, fast comparator, successive approximation register, a clock, and buffer amplifier. The thin film resistor network has excellent tracking characteristics resulting in no missing codes over the operating temperature range. The network is functionally laser trimmed.

Output coding is complementary binary, complementary offset binary, or complementary two's complement. Provision is made for precise, external adjustment of offset and gain.

SPECIFICATIONS, Typical at 25°C

	ADC-HZ12B
Resolution	12 Bits
Conversion Time, max.	8 μsec.
Gain Tempco, max.	20 ppm/°C
Nonlinearity Error, max.	½ LSB
Differential Nonlinearity, max.	½ LSB
Diff. Nonlinearity Tempco	2 ppm/°C of FSR
No Missing Codes	Over Op. Temp. Range
Power Supply Sensitivity, max.	0.002%/%
Analog Input Ranges	0 to +5 V, 0 to +10V ±2.5 V, ±5 V, ±10 V
Input Impedance	2.5K, 5K or 10K
Buffer Input Impedance	100 Megohms
Buffer Bias Current	125 nA
Buffer Settling Time	3 μsec.
Output Logic	TTL
Unipolar Coding	Complementary Binary
Bipolar Coding	Comp. Offset Binary Comp. 2's Complement
Power Requirement	+15 VDC at 55 mA −15 VDC at 45 mA +5 VDC at 100 mA
Package	32 Pin DIP

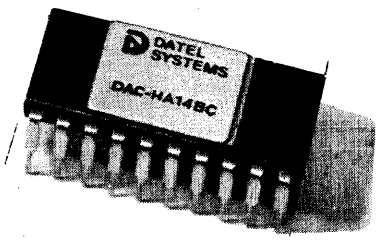
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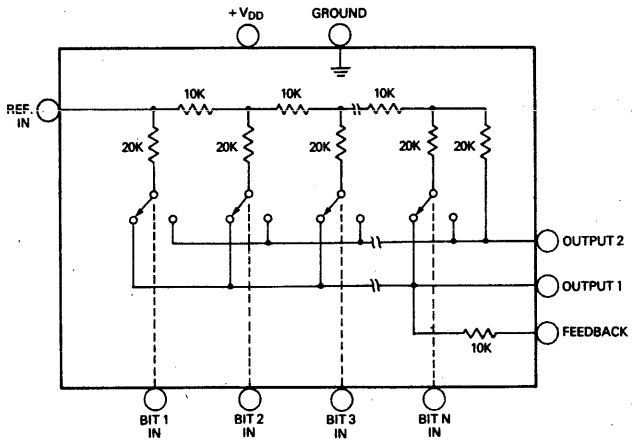
Model	Oper. Temp. Range	Seal	Price (1-24)
ADC-HZ12BGC	0 to 70C	Epoxy	$119.00
ADC-HZ12BMC	0 to 70C	Hermetic	129.00
ADC-HZ12BMR	−25 to +85C	Hermetic	169.00
ADC-HZ12BMM	−55 to +100C	Hermetic	195.00

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DATEL SYSTEMS, INC.
DAC-HA14B
HIGH RESOLUTION, MULTIPLYING CMOS D/A CONVERTER





FEATURES
- **14 Bit Resolution**
- **2 & 4 Quadrant Multiplying**
- **500 nsec. Settling Time**
- **10 ppm/°C Tempco**
- **+5 V or +15 V Power Supply**

The DAC-HA14B is a 14 bit, CMOS multiplying D/A converter. There are two versions, offering a choice of either +5 V or +15 V power supply operation. The +5 V model draws only 10 μA quiescent current while the +15 V model draws 2 mA. The device is packaged in a 20 pin ceramic DIP package.

The combination of low ON resistance CMOS switches and a laser-trimmed nichrome thin film resistor network result in a maximum nonlinearity of ±1 LSB with 14 bit monotonicity at 25°C. The gain temperature coefficient of the circuit is 10 ppm/°C maximum. The resistor network is an R-2R ladder with resistance values of 10K and 20K ohms.

The input resistance to the ladder is 10K ohms for the external reference source, which may be ±10 V. Bandwidth for the reference input is 200 kHz. The DAC-HA14B incorporates internal protection on the power supply and digital input terminals to prevent latch-up problems.

SPECIFICATIONS, Typical at 25°C

	DAC-HA14B
Resolution	14 Bits
Settling Time, to 1 LSB	500 nsec.
Gain Tempco, max.	10 ppm/°C
Nonlinearity, max.	1 LSB
Differential Nonlinearity, max.	1 LSB
Monotonicity	At 25°C
Power Supply Sensitivity	0.005%/%
Analog Output Current	±1 mA
Reference Input Range	±10 V
Reference Input Impedance	10K ±20%
Input Logic	TTL, CMOS
Coding, unipolar	Straight Binary
Coding, bipolar	Offset Binary
Power Requirement	+4 to +7 VDC at 10 μA +12 to +20 VDC at 2 mA*
Package	20 Pin DIP

*For models designated with −1 suffix

ORDERING INFORMATION

Model	Oper. Temp. Range	Supply Voltage	Price (1-24)
DAC-HA14BC	0 to 70C	+5 V	$ 69.00
DAC-HA14BR	−25 to +85C	+5 V	99.00
DAC-HA14BM	−55 to +125C	+5 V	139.00
DAC-HA14BC-1	0 to 70C	+15 V	69.00
DAC-HA14BR-1	−25 to +85C	+15 V	99.00
DAC-HA14BM-1	−55 to +125C	+15 V	139.00

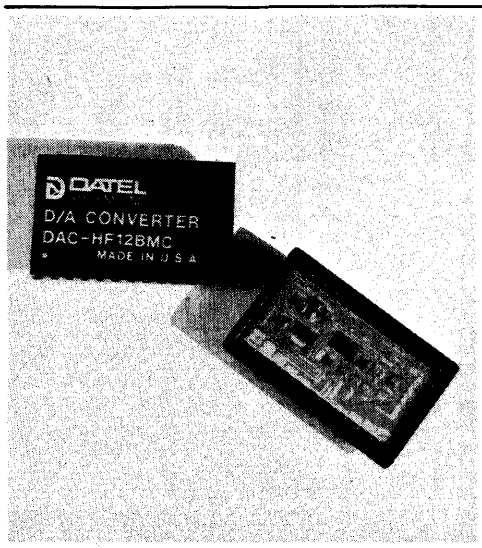
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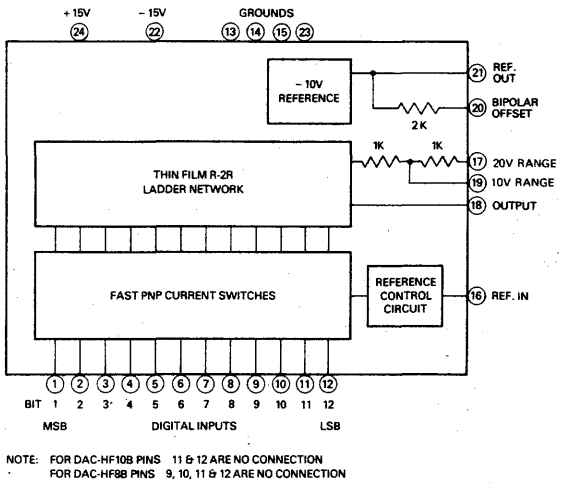
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DATEL SYSTEMS, INC.

DAC-HF SERIES

ULTRA-FAST, CURRENT OUTPUT D/A CONVERTERS





NOTE: FOR DAC-HF10B PINS 11 & 12 ARE NO CONNECTION
FOR DAC-HF8B PINS 9, 10, 11 & 12 ARE NO CONNECTION

FEATURES

- **8, 10, or 12 Bit Resolution**
- **25 nsec. Settling (8 or 10 Bits)**
- **50 nsec. Settling (12 Bits)**
- **Unipolar or Bipolar Operation**
- **10 mA Output Current**

The DAC-HF series features ultra-fast current outputs for 8, 10, and 12 bit resolutions. These state-of-the-art digital to analog converters give output settling times of 25 nanoseconds maximum for 8 and 10 bits and 50 nanoseconds maximum for 12 bits. They can be used to drive a load resistor directly for up to ±1.2 V outputs or with a fast inverting operational amplifier (Datel System's AM-500) for up to ±10 V outputs at sub-microsecond settling times. The required feedback resistors are incorporated inside the unit and give a selection of five different output ranges by external pin connection.

The circuit uses high speed PNP current switches combined with a low impedance R-2R ladder network. The network is fabricated with nichrome thin-film resistors which are then laser trimmed for optimum linearity. The output current is 0 to +10 mA or +5 mA with a 200 ohm output impedance.

SPECIFICATIONS, Typical at 25°C

	DAC-HF8B	DAC-HF10B	DAC-HF12B
Resolution	8 Bits	10 Bits	12 Bits
Settling time max.*	25 nsec.	25 nsec.	50 nsec.
Gain Tempco, max.	20 ppm/°C	20 ppm/°C	20 ppm/°C
Nonlinearity, max.	½ LSB	½ LSB	½ LSB
Diff. Nonlinearity, max.	½ LSB	½ LSB	½ LSB
Monotonicity	Over Operating Temp. Range		
Power Supply Sensitivity	0.01%/%	0.01%/%	0.01%/%
Analog Output Ranges	0 to +10 mA ±5 mA	0 to +10 mA ±5 mA	0 to +10 mA ±5 mA
Output Voltage Compliance	±1.2 V	±1.2 V	±1.2 V
Input Logic	DTL/TTL	DTL/TTL	DTL/TTL
Coding, unipolar	Straight Bin.	Straight Bin.	Straight Bin.
Coding, bipolar	Offset Bin.	Offset Bin.	Offset Bin.
Power Requirement	+15 VDC @ 50 mA −15 VDC @ 12 mA	+15 VDC @ 60 mA −15 VDC @ 12 mA	+15 VDC @ 70mA +15 VDC @ 12 mA
Package	24 Pin DIP	24 Pin DIP	24 Pin DIP

*To 1 LSB

ORDERING INFORMATION

Model	Oper. Temp. Range	Seal	Price (1-24)
DAC-HF8BGC	0 to 70C	Epoxy	$109.00
DAC-HF8BMC	0 to 70C	Hermetic	119.00
DAC-HF8BMR	−25 to +85C	Hermetic	159.00
DAC-HF8BMM	−55 to +125C	Hermetic	189.00
DAC-HF10BGC	0 to 70C	Epoxy	129.00
DAC-HF10BMC	0 to 70C	Hermetic	139.00
DAC-HF10BMR	−25 to +85C	Hermetic	179.00
DAC-HF10BMM	−55 to +125C	Hermetic	209.00
DAC-HF12BGC	0 to 70C	Epoxy	139.00
DAC-HF12BMC	0 to 70C	Hermetic	149.00
DAC-HF12BMR	−25 to +85C	Hermetic	189.00
DAC-HF12BMM	−55 to +125C	Hermetic	219.00

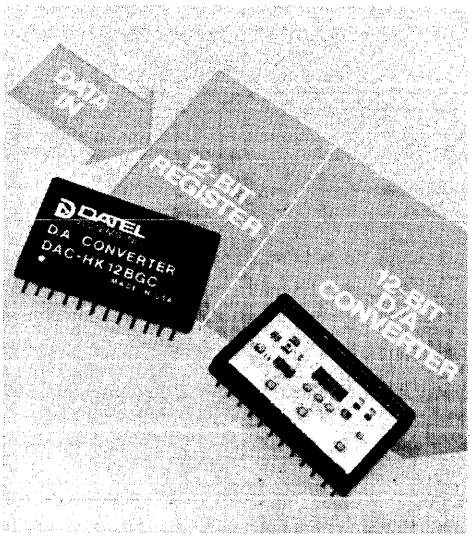
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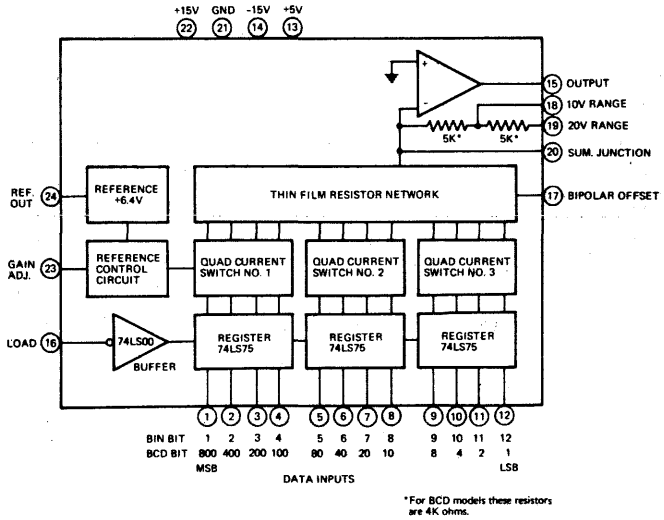
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DATEL SYSTEMS, INC.

DAC-HK SERIES

HIGH PERFORMANCE 12 BIT DAC'S WITH INPUT REGISTER





FEATURES

- **12 Bit Resolution**
- **Input Register**
- **20 ppm/°C Tempco**
- **Binary, BCD, or 2's Comp. Coding**
- **3 μsec. Settling Time**

The DAC-HK series D/A converters are high performance 12-bit devices with a fast settling voltage output. They incorporate a level controlled input storage register and are specifically designed for systems applications such as data-bus interfacing with computers. When the "load" input is high data in the storage register is held, and when the load input is low data is transferred through to the DAC. There are three basic models available by coding option: binary, BCD, and two's complement. The output voltage ranges are externally pin-programmable and include: 0 to +2.5 V, 0 to +5 V, 0 to +10 V, ±2.5 V, ±5 V, and ±10 V.

Quad current switches are combined with a low T.C. thin film resistor network and a low T.C. Zener reference to achieve better than 20 ppm/°C gain tempco. Optimum linearity is attained by functional laser trimming of the thin film nichrome resistors.

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SPECIFICATIONS, Typical at 25°C

	DAC-HK12B	DAC-HK12D
Resolution	12 Bits	3 Digits
Settling Time, to ½ LSB	3 μsec.	3 μsec.
Gain Tempco, max.	20 ppm/°C	20 ppm/°C
Nonlinearity, max.	½ LSB	¼ LSB
Differential Nonlinearity, max.	½ LSB	¼ LSB
Monotonicity	Over Oper. Temp. Range	
Power Supply Sensitivity	0.002%/%	0.002%/%
Analog Output Voltages	0 to +5 V 0 to +10 V ±2.5 V ±5 V ±10 V	0 to +2.5 V 0 to +5 V 0 to +10 V
Output Current	±5 mA	+5 mA
Input Logic	DTL/TTL	DTL/TTL
Coding, unipolar	Straight Bin.	BCD
Coding, bipolar	Offset Bin. Two's Comp.	
Power Requirement	+15 VDC at 15 mA −15 VDC at 30 mA +5 VDC at 45 mA	
Package	24 Pin DIP	

ORDERING INFORMATION

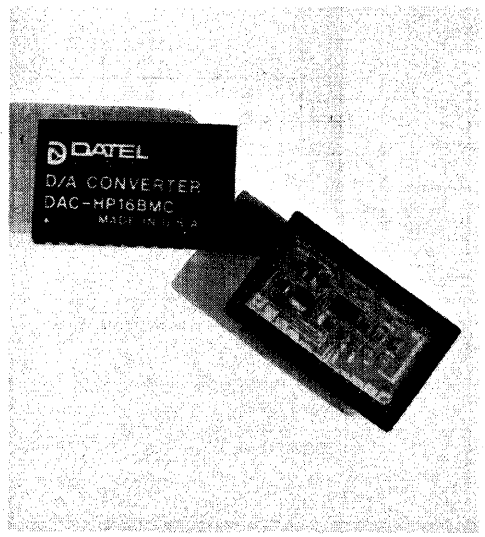
Model	Oper. Temp. Range	Coding	Seal	Price (1-24)
DAC-HK12BGC	0 to 70C	Binary	Epoxy	$ 59.00
DAC-HK12BMC	0 to 70C	Binary	Hermetic	69.00
DAC-HK12BMR	−25 to +85C	Binary	Hermetic	99.00
DAC-HK12BMM	−55 to +125C	Binary	Hermetic	139.00
DAC-HK12BGC-2	0 to 70C	2's Comp.	Epoxy	59.00
DAC-HK12BMC-2	0 to 70C	2's Comp.	Hermetic	69.00
DAC-HK12BMR-2	−25 to +85C	2's Comp.	Hermetic	99.00
DAC-HK12BMM-2	−55 to +125C	2's Comp.	Hermetic	139.00
DAC-HK12DGC	0 to 70C	BCD	Epoxy	59.00
DAC-HK12DMC	0 to 70C	BCD	Hermetic	69.00
DAC-HK12DMR	−25 to +85C	BCD	Hermetic	99.00
DAC-HK12DMM	−55 to +125C	BCD	Hermetic	139.00

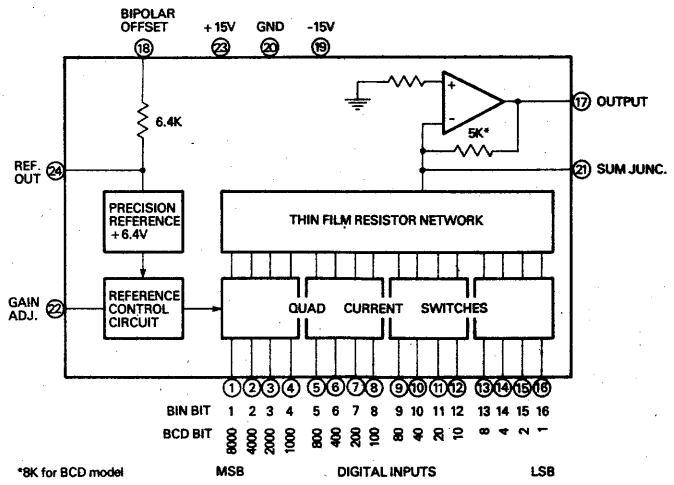
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DATEL SYSTEMS, INC.

DAC-HP16B, DAC-HP16D

HIGH RESOLUTION D/A CONVERTERS





FEATURES

- **16 Bit Binary Model**
- **4 Digit BCD Model**
- **Linearity to 0.003%**
- **15 ppm/°C Tempco, Max.**
- **Voltage Output**

The DAC-HP series are high resolution D/A converters with voltage output. They are self-contained, including a low tempco zener reference circuit and output operational amplifier, all in a miniature 24 pin double spaced ceramic DIP package. There are two basic models in the series. The DAC-HP16B has 16 bit binary resolution with ±0.003% linearity while the DAC-HP16D has 4 digit BCD resolution with ±0.005% linearity. Input coding is complementary binary and complementary offset binary for the DAC-HP16B and complementary BCD for the DAC-HP16D. The binary version operates in both unipolar and bipolar modes with output voltages of 0 to +10 V and ±5 V; the BCD version operates in unipolar mode only with 0 to +10 V output.

The DAC-HP design incorporates thin film hybrid technology which has been in volume production. Selected low tempco nichrome on silicon thin film resistor networks are combined with tightly matched quad current switches to achieve 16 bit resolution.

SPECIFICATIONS, Typical at 25°C

	DAC-HP16B	DAC-HP16D
Resolution	16 Bits	4 Digits
Settling Time	35 μsec.	15 μsec.
Gain Tempco, max.	15 ppm/°C	15 ppm/°C
Nonlinearity, max.	0.003%	0.005%
Monotonicity, 10°C to 40°C	14 Bits	16 Bits
Power Supply, Sensitivity	0.002%/%	0.002%/%
Analog Output Ranges	0 to +10 V ±5 V	0 to +10 V
Output Current	±5 mA	+5 mA
Input Logic	DTL/TTL	DTL/TTL
Coding, unipolar	Comp. Bin.	Comp. BCD
Coding, bipolar	Comp. Off. Bin.	
Power Requirement	+15 VDC at 42 mA −15 VDC at 36 mA	
Package	24 Pin DIP	

ORDERING INFORMATION

Model	Oper. Temp. Range	Seal	Price (1-24)
DAC-HP16BMC	0 to 70C	Hermetic	$119.00
DAC-HP16BMR	−25 to +85C	Hermetic	149.00
DAC-HP16BMM	−55 to +125C	Hermetic	199.00
DAC-HP16DMC	0 to 70C	Hermetic	119.00
DAC-HP16DMR	−25 to +85C	Hermetic	149.00
DAC-HP16DMM	−55 to +125C	Hermetic	199.00

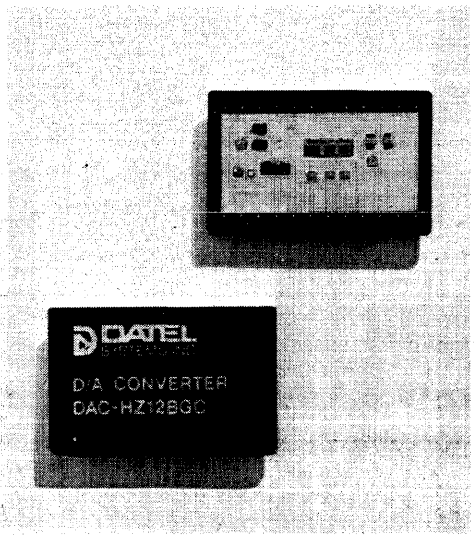
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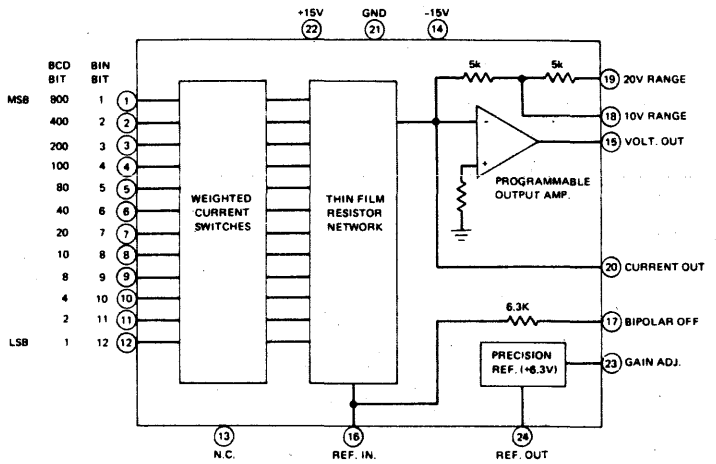
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DATEL SYSTEMS, INC.

DAC-HZ12B SERIES

LOW COST, HIGH PERFORMANCE 12 BIT D/A CONVERTERS





FEATURES

- **12 Bits Binary**
- **3 Digits BCD**
- **5 Output Ranges**
- **3 μsec. Settling time**
- **20 ppm/°C Tempco**

The DAC-HZ series are high performance, hybrid 12 bit binary and 3 digit BCD digital-to-analog converters. They are complete and self-contained with a precision internal reference and fast output operational amplifier. Pin programmable output voltage ranges are provided for a high degree of application flexibility; the output voltage ranges are 0 to +5 V, 0 to +10 V, ±2.5 V, ±5 V, and ±10 V with only unipolar ranges available on the BCD models.

The internal design utilizes three quad current switches, two thin film resistor networks, a precision zener reference circuit, reference control circuit and output amplifier. The thin film resistor networks are functionally trimmed with a laser to precisely set the binary weights of the current switches. The excellent tracking of the thin film resistors in conjunction with the tightly matched current switches results in a differential nonlinearity tempco of only 2 ppm/°C.

SPECIFICATIONS, Typical at 25°C

	DAC-HZ12B	DAC-HZ12D
Resolution	12 Bits	3 Digits
Settling Time, to ½ LSB	3 μsec.	3 μsec.
Gain Tempco, max.	20 ppm/°C	20 ppm/°C
Nonlinearity, max.	½ LSB	¼ LSB
Diff. Nonlinearity, max.	½ LSB	¼ LSB
Monotonicity	Over Op. Temp. Range	
Power Supply Sensitivity	0.002%/%	0.002%/%
Analog Output Ranges	0 to +5 V 0 to +10 V ±2.5 V ±5 V ±10 V	0 to +2.5 V 0 to +5 V 0 to +10 V
Output Current	±5 mA	+5 mA
Input Logic	DTL/TTL	DTL/TTL
Coding, unipolar	Comp. Bin.	Comp. BCD
Coding, bipolar	Comp. Off. Bin.	
Power Requirement	±15 VDC at 35 mA	
Package	24 Pin DIP	

ORDERING INFORMATION

Model	Oper. Temp. Range	Seal	Price (1-24)
DAC-HZ12BGC	0 to 70C	Epoxy	$ 39.00
DAC-HZ12BGR	−25 to +85C	Epoxy	55.00
DAC-HZ12BMC	0 to 70C	Hermetic	49.00
DAC-HZ12BMR	−25 to +85C	Hermetic	69.00
DAC-HZ12BMM	−55 to +125C	Hermetic	119.00
DAC-HZ12DGC	0 to 70C	Epoxy	39.00
DAC-HZ12DGR	−25 to +85C	Epoxy	55.00
DAC-HZ12DMC	0 to 70C	Hermetic	49.00
DAC-HZ12DMR	−25 to +85C	Hermetic	69.00
DAC-HZ12DMM	−55 to +125C	Hermetic	119.00

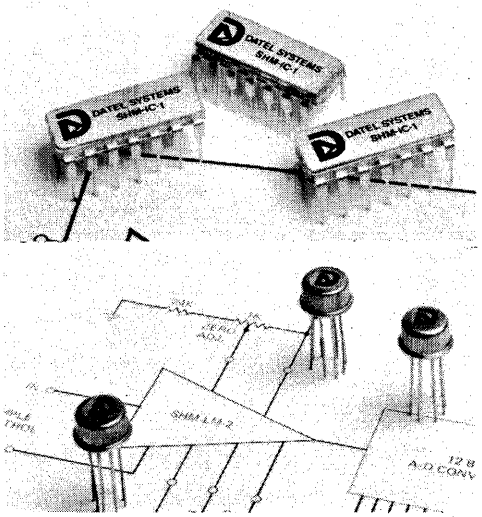
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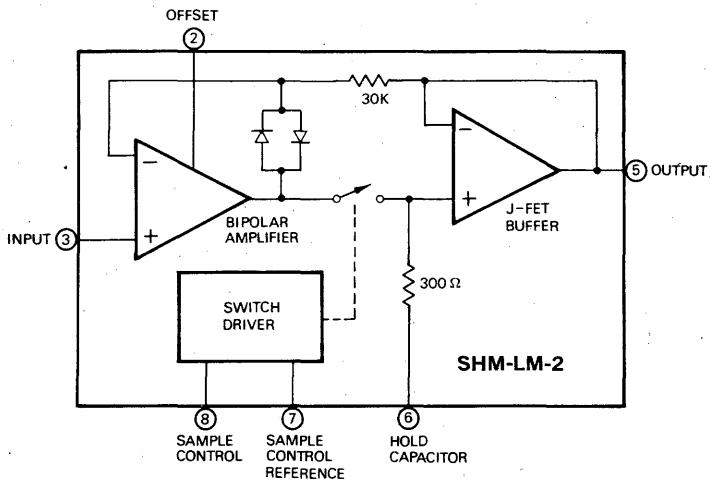
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DATEL SYSTEMS, INC.

SHM-IC-1, SHM-LM-2

MONOLITHIC SAMPLE-HOLDS





FEATURES

- **Acquisition Time to 5 μsec.**
- **0.01% Accuracy**
- **Bandwidth to 2 MHz**
- **0.01% Feedthrough**
- **Low Cost**

These monolithic sample-hold devices feature excellent performance specifications at a low price. They are self-contained units requiring only an external hold capacitor for operation. The SHM-LM-2 operates in a fixed gain configuration of +1 while the SHM-IC-1 can be externally connected for gains of ±1 or for higher gains by means of two external resistors. Both models consist of a high impedance input amplifier, a fast electronic switch, and a high impedance output buffer amplifier. The circuit operates in a closed loop configuration for maximum accuracy.

Accuracy is 0.01% for both models making them useful in 12 bit A/D converter applications. For a 1000pF hold capacitor the acquisition time is 5 μsec. for the SHM-IC-1 and 6 μsec. for the SHM-LM-2. Better accuracy with lower feedthrough and hold mode droop can be achieved by using higher value hold capacitance such as .01 μF.

SPECIFICATIONS, Typical at 25°C, C_H = 1000pF

	SHM-IC-1	SHM-LM-2
Accuracy	0.01%	0.01%
Acquisition Time to 0.01%	5 μsec.	6 μsec.
Acquisition Time to 0.1%	4 μsec.	5 μsec.
Aperture Delay Time	50 nsec.	100 nsec.
Hold Mode Droop	50 μV/nsec.	200 μV/nsec.
Hold Mode Feedthrough, max.	0.01%	0.01%
Bandwidth	2 MHz	1 MHz
Sample-to-Hold Error, max.	20 mV	25 mV
Gain	±1	+1
Input Voltage Range, min.	±10 V	±11.5 V
Input Impedance	10^8 ohms	10^{10} ohms
Input Bias Current, max.	200 nA	50 nA
Input Offset Voltage Drift	20 μV/°C	10 mV*
Digital Control	DTL, TTL	DTL, TTL, CMOS
Output Voltage, min.	±10 V	±11.5 V
Output Current	±5 mA	±5 mA
Power Requirement	±15 V at 5 mA	±15 V at 6 mA
Package	14 Pin DIP	TO-99

*Over Oper. Temp. Range

ORDERING INFORMATION

Model	Oper. Temp. Range	Package	Price (1-24)
SHM-IC-1	0 to 70C	Ceramic	$19.00
SHM-IC-1M	−55 to +125C	Ceramic	40.00
SHM-LM-2	0 to 70C	Metal	7.95
SHM-LM-2M	−55 to +125C	Metal	35.00

COVERED BY GSA CONTRACT

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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-200

Dual SPST CMOS Analog Switch

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 240ns
- LOW R_{ON} 55Ω
- LOW POWER DISSIPATION 15mW
- TTL/CMOS COMPATIBLE
- NO DIGITAL INPUT CURRENT SPIKE

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

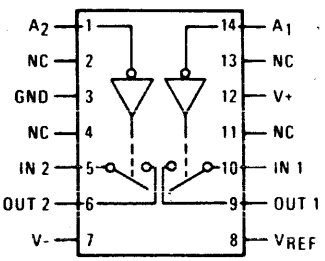
HI-200 is a monolithic device comprising two independently selectable SPST switches which feature fast switching speeds (290ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and Complementary CMOS processing, HI-200 operates without any applications problems induced by latch-up or SCR mode phenomena.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters and op amp gain switching networks.

HI-200 is available in D.I.P. (TO-116) and metal (TO-100) cans. HI-200-2 is specified from -55°C to +125°C while HI-200-5 operates from 0°C to +75°C. HI-200 is functionally and pin compatible with other available "200 series" switches.

PINOUT

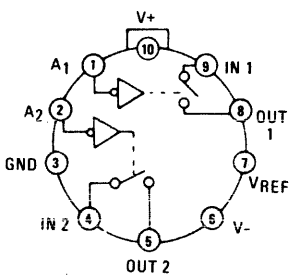
Package Code 4B



TO-116

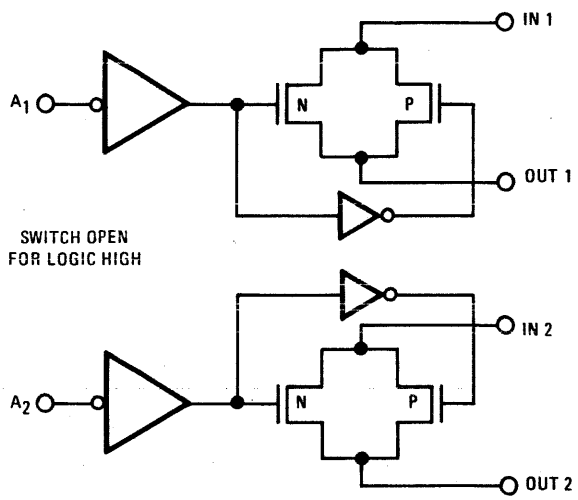
Package Code 2D

Top View



TO-100

FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 6 and 10	+40V	Total Power Dissipation*	450mW
V_{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	$+V_{Supply}$ +4V	HI-200-2	-55°C to +125°C
	$-V_{Supply}$ -4V	HI-200-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-200-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 6mW/°C Above T_A = 75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified
Supplies = +15V, -15V; V_{REF} = Open; V_{AH}(Logic Level High) = 3.0V V_{AL}(Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics

PARAMETER	TEMP.	HI-200-2** -55°C to +125°C MIN.	TYP.	MAX.	HI-200-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
* V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, On Resistance (Note 1)	+25°C		55	70		55	80	Ω
	Full		80	100		72	100	Ω
* $I_{S(OFF)}$, Off Input Leakage Current	+25°C		1			1		nA
	Full		100	500		10	500	nA
* $I_{D(OFF)}$, Off Output Leakage Current	+25°C		1			1		nA
	Full		100	500		10	500	nA
* $I_{D(ON)}$, On Leakage Current	+25°C		.02			.02		nA
	Full		6	500		6	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	3.0			3.0			V
* I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break - Before Make Delay (Note 3)	+25°C		60			60		ns
t_{on}, Switch on Time	+25°C		240	500		240		ns
t_{off}, Switch off Time	+25°C		330	500		500		ns
"Off Isolation" (Note 4)	+25°C		70			70		dB
$C_{S\,(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D\,(OFF)}$, Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS\,(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)	+25°C		15			15		mW
P_D, Power Dissipation	Full			60			60	mW
* I^+, Current (Pin 10)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
* I^-, Current (Pin 6)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

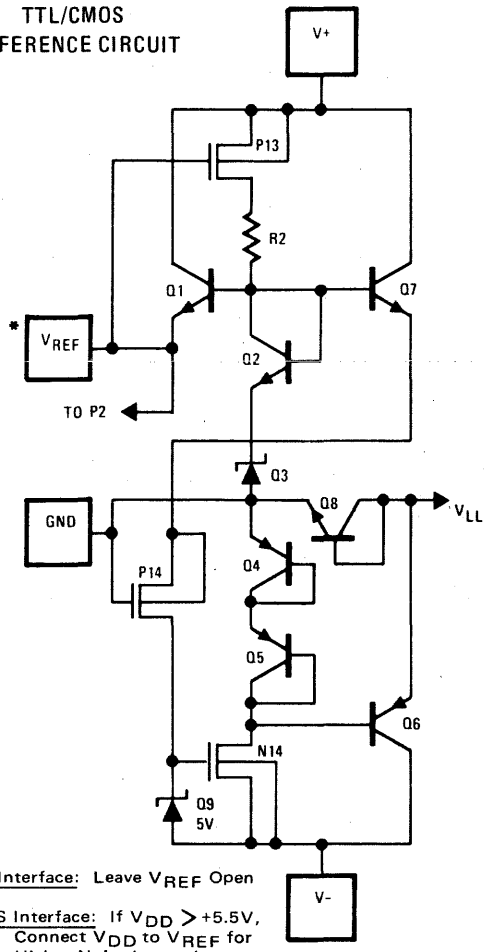
NOTES:
1. V_{OUT} = ±10V I_{OUT} = 1mA
2. Digital Inputs Are MOS Gates - Typical Leakage is Less Than 1nA
3. V_{AH} = 4.0V
4. V_A = +3V, R_L = 1KΩ, C_L = 10pF, V_S = 3VRMS, f, 100 kHz
5. V_A = +3V or V_A = OV For Both Switches

*100% Tested For Dash 8 At +25°C And +125°C Only

**Note: HI-200-4 has same specifications as HI-200-2 over the reduced temperature range -20°C to +85°C

SCHEMATIC DIAGRAMS

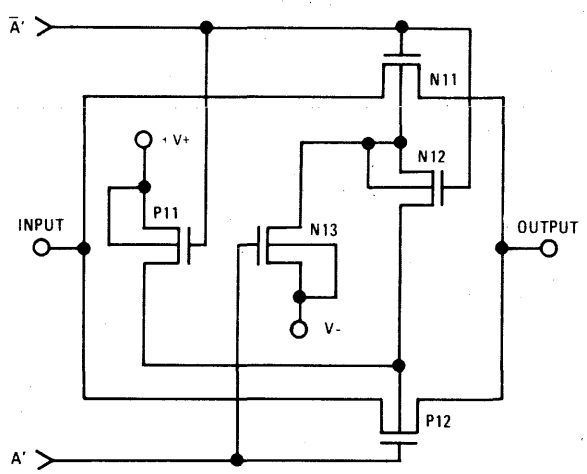
TTL/CMOS REFERENCE CIRCUIT



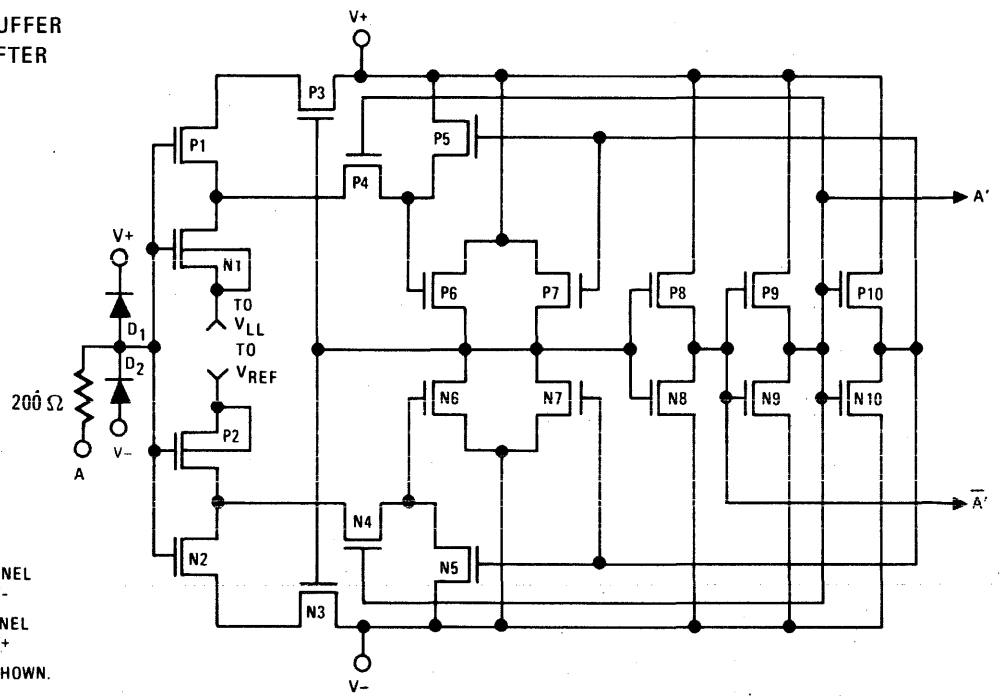
*TTL Interface: Leave V_{REF} Open

*CMOS Interface: If $V_{DD} > +5.5V$, Connect V_{DD} to V_{REF} for Higher Noise Immunity; Otherwise Leave Open.

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



ALL N-CHANNEL BODIES TO V-

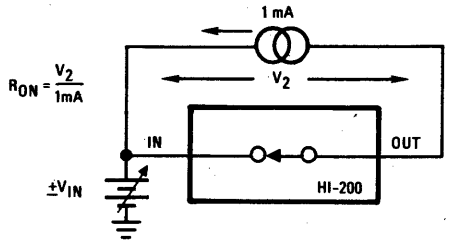
ALL P-CHANNEL BODIES TO V+

EXCEPT AS SHOWN.

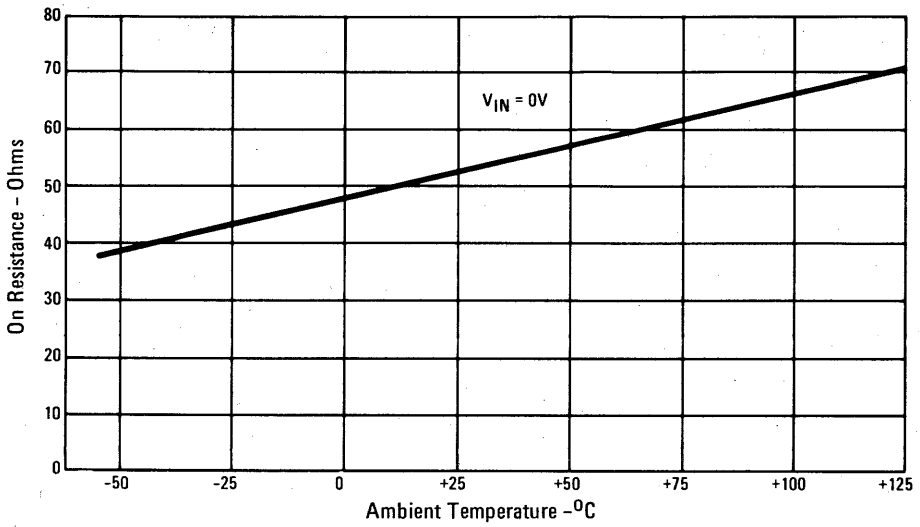
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(UNLESS OTHERWISE SPECIFIED $T_A = 25^0C$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = 3.0V$ $V_{AL} = 0.8V$ AND V_{REF} = OPEN).

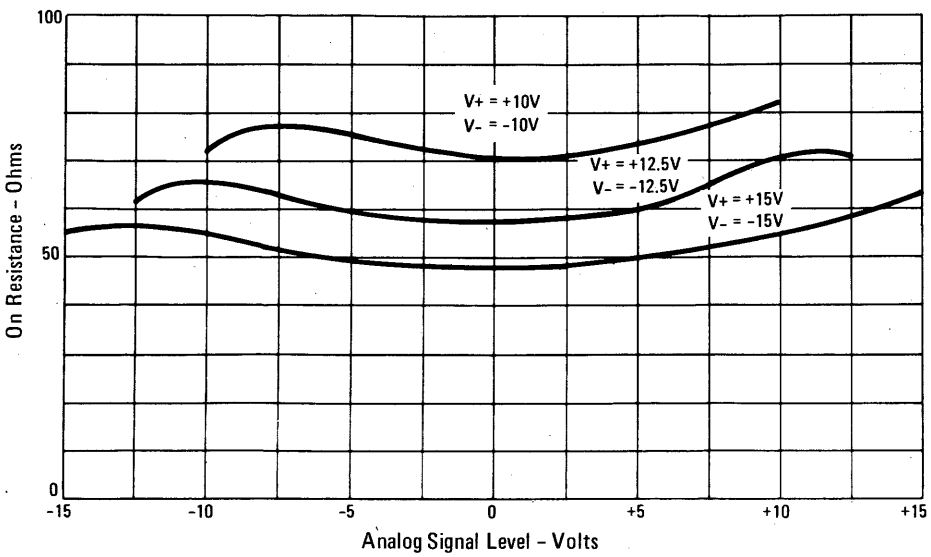
ON RESISTANCE vs. ANALOG SIGNAL LEVEL, SUPPLY VOLTAGE AND TEMPERATURE



ON RESISTANCE vs. TEMPERATURE

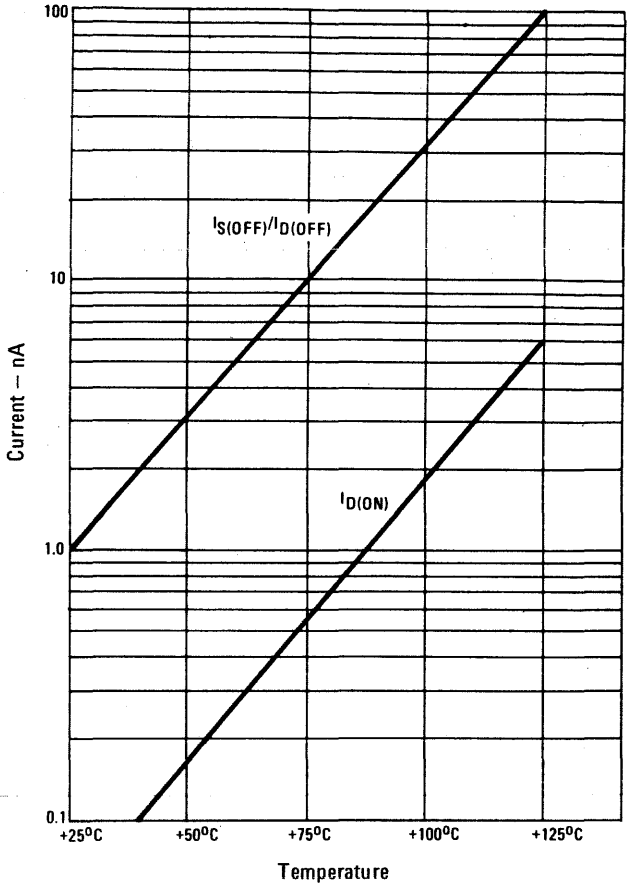


(HI-200)
ON RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

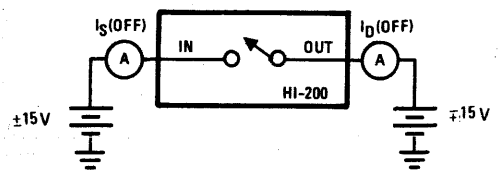


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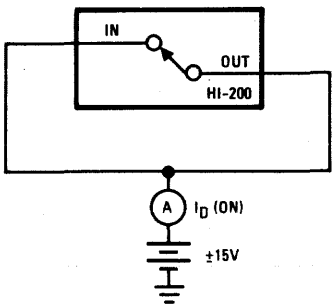
SWITCH LEAKAGE CURRENT vs. TEMPERATURE (HI-200)



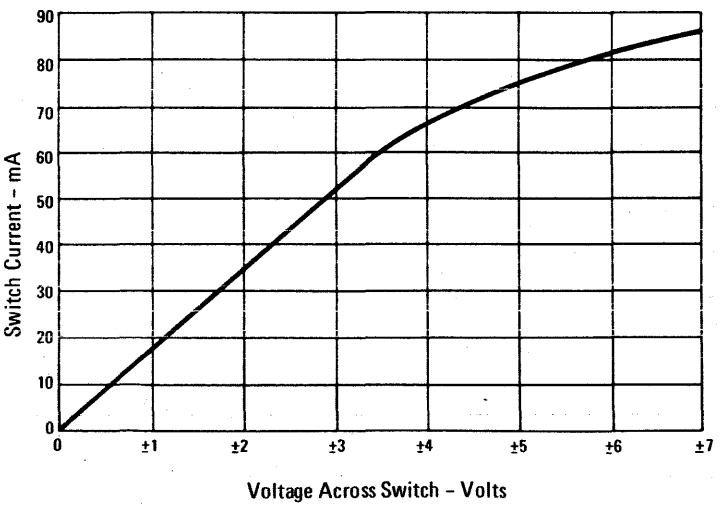
OFF LEAKAGE CURRENT vs. TEMPERATURE



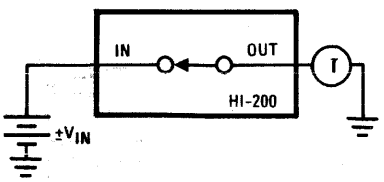
ON LEAKAGE CURRENT vs. TEMPERATURE



SWITCH CURRENT vs. VOLTAGE



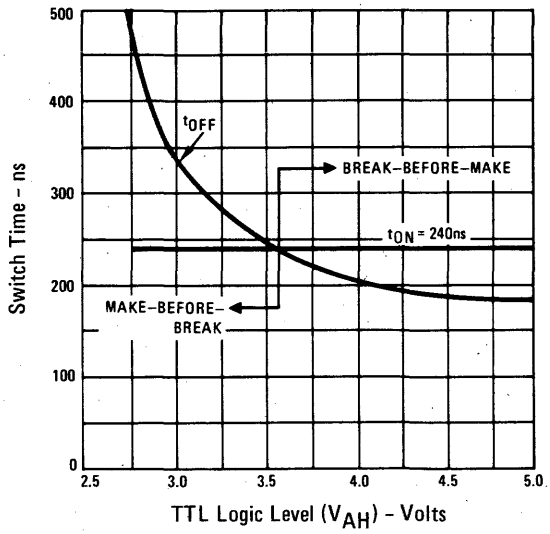
SWITCH CURRENT vs. VOLTAGE



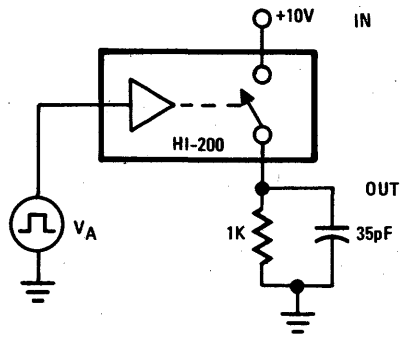
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PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

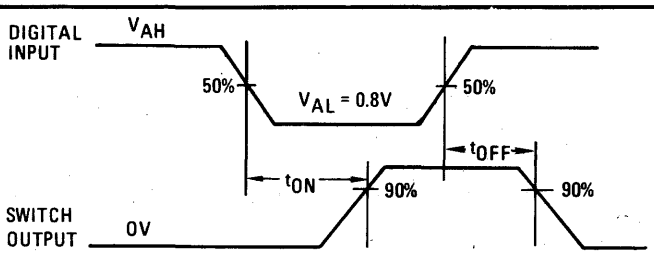
(HI-200)
SWITCH TIME vs. TTL LOGIC LEVEL



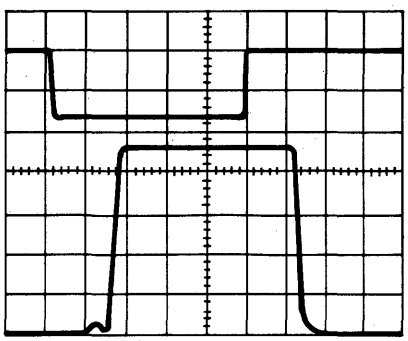
ON/OFF SWITCH TIME vs.
LOGIC LEVEL



SWITCHING WAVEFORMS

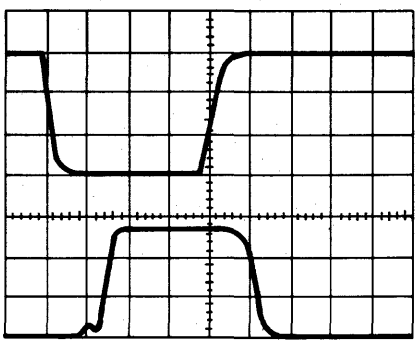


t_{ON}, t_{OFF} (TTL INPUT)
V_{AH} = +4.0V



Top: TTL Input
Bottom: Output
Vertical: 2V/Div.
Horizontal: 200ns/Div.

t_{ON}, t_{OFF} (CMOS INPUT)
V_{REF} = OPEN, V_{AH} = +15V



Top: CMOS Input
Bottom: Output
Vertical: 5V/Div.
Horizontal: 200ns/Div.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-201

Quad SPST CMOS Analog Switch

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 185ns
- LOW R_{ON} 65Ω
- LOW POWER DISSIPATION 15mW
- TTL/CMOS COMPATIBLE
- NO DIGITAL INPUT CURRENT SPIKE

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

HI-201 is a monolithic device comprising four independently selectable SPST switches which feature fast switching speeds (185ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and Complementary CMOS processing, HI-201 operates without any applications problems induced by latch-up or SCR-mode phenomena.

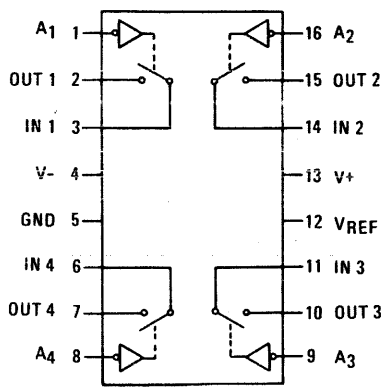
All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-201 is an ideal component for use in high frequency analog switching. Typical appliations include signal path switching, sample and hold circuit, digital filters and op amp gain switching networks.

HI-201 is available in a 16 lead dual-in-line package. HI-201-2 is specified from -55°C to +125°C while HI-201-5 operates from 0°C to +75°C. HI-201 is functionally and pin compatible with other available "200 series" switches.

PIN OUT

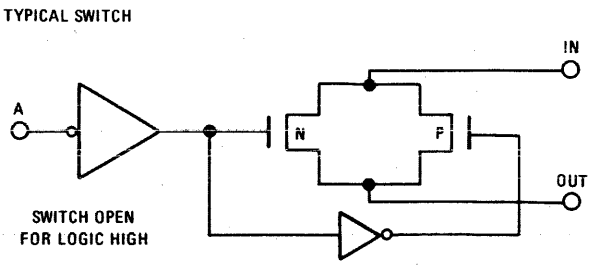
Package Code 4B

Top View



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

FUNCTIONAL DIAGRAM



SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 4 and 13	+40V	Total Power Dissipation*	750mW
V_{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	V_{Supply}(+) +4V	HI-201-2	-55°C to +125°C
	V_{Supply}(-) -4V	HI-201-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-201-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 8mW/°C Above T_A = +75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified
Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 3.0V V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics

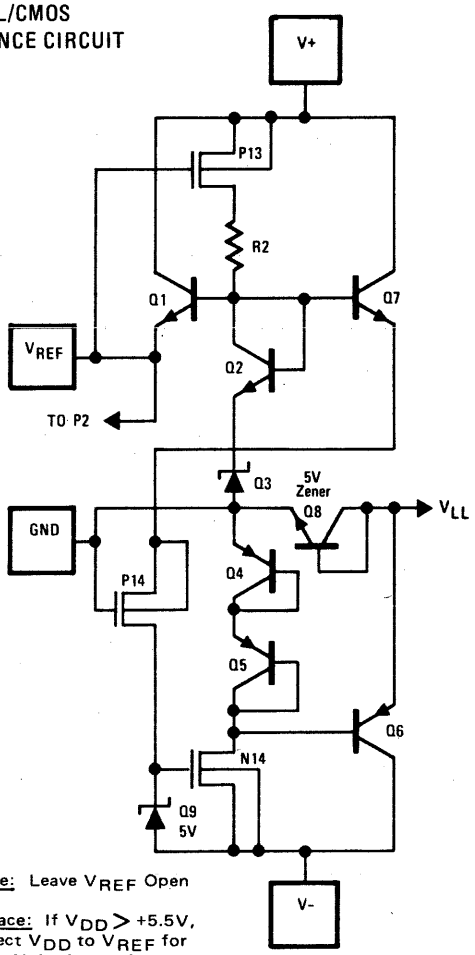
		HI-201-2** -55°C to +125°C			HI-201-5 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 1)	+25°C		65	80		65	100	Ω
	Full		85	125		75	125	Ω
*$I_{S(OFF)}$, Off Input Leakage Current	+25°C		2			2		nA
	Full			500			250	nA
*$I_{D(OFF)}$, Off Output Leakage Current	+25°C		2			2		nA
	Full			500			250	nA
*$I_{D(ON)}$, On Leakage Current	+25°C		2			2		nA
	Full			500			250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	3.0			3.0			V
*I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break - Before Make Delay (Note 3)	+25°C		30			30		ns
t_{on}, Switch ON Time	+25°C		185	500		185		ns
t_{off}, Switch OFF Time	+25°C		220	500		220		ns
"Off Isolation" (Note 4)	+25°C		80			80		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)	+25°C		15			15		mW
P_D, Power Dissipation	Full			60			60	mW
*I_+, Current (Pin 13)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
*I_- Current (Pin 4)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

NOTES:
1. V_{OUT} = ±10V I_{OUT} = 1mA
2. Digital Inputs Are MOS Gates - Typical Leakage is Less Than 1nA
3. V_{AH} = 4.0V
4. V_A = 5V, R_L = 1KΩ, C_L = 10pF, V_S = 3VRMS, f = 100KHz
5. V_A = +3V or V_A = 0V For all Switches

*100% Tested for Dash 8. ("Full" Tested at +25°C to +125°C)
**Note: HI-201-4 has same specifications as HI-201-2 over the reduced temperature range -20°C to +85°C

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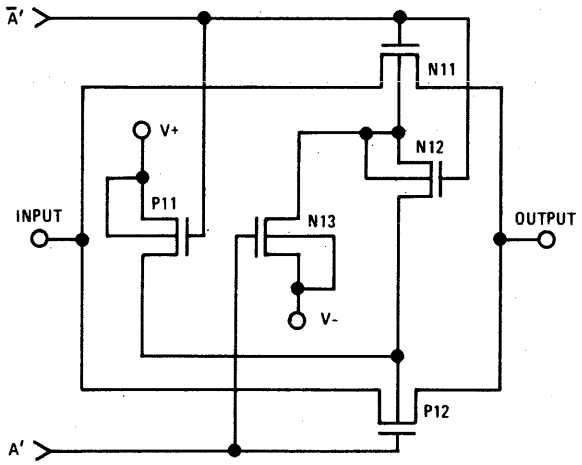
TTL/CMOS REFERENCE CIRCUIT



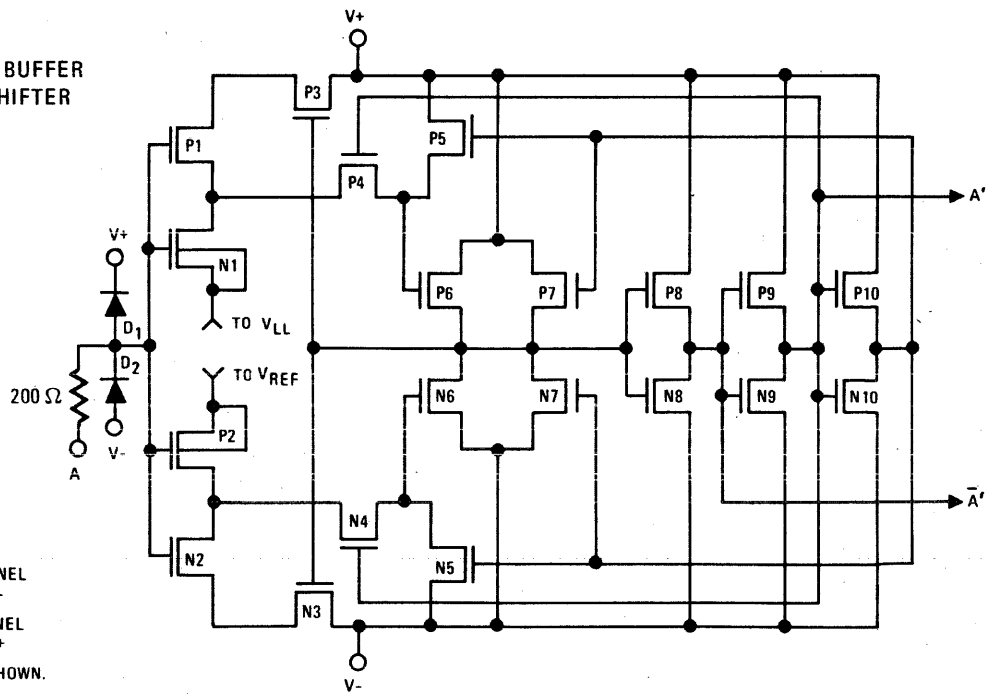
*TTL Interface: Leave V_{REF} Open

*CMOS Interface: If $V_{DD} > +5.5V$, Connect V_{DD} to V_{REF} for Higher Noise Immunity; Otherwise Leave Open.

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



ALL N-CHANNEL BODIES TO V-

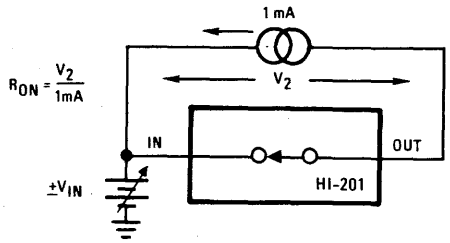
ALL P-CHANNEL BODIES TO V+

EXCEPT AS SHOWN.

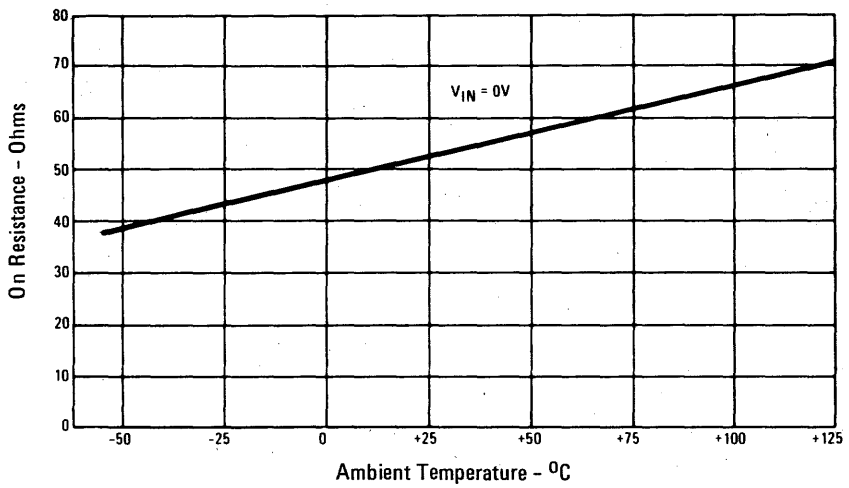
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(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = 3.0V$ $V_{AL} = 0.8V$ AND V_{REF} = OPEN).

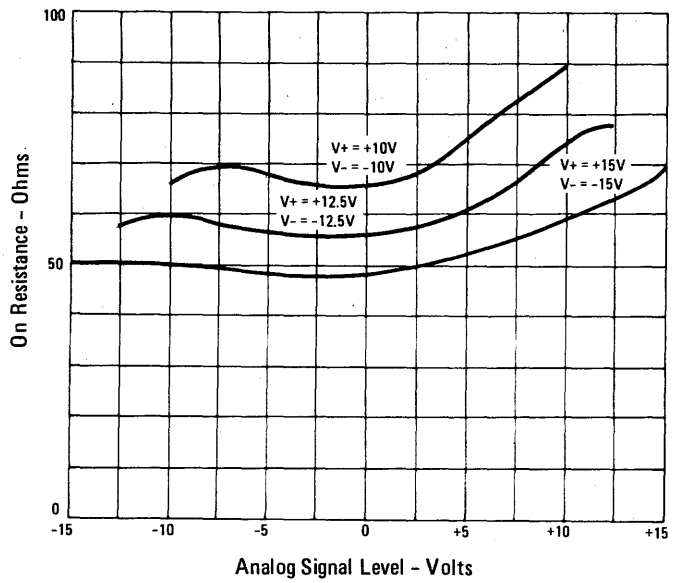
ON RESISTANCE vs. ANALOG SIGNAL LEVEL,
SUPPLY VOLTAGE AND TEMPERATURE



ON RESISTANCE vs. TEMPERATURE

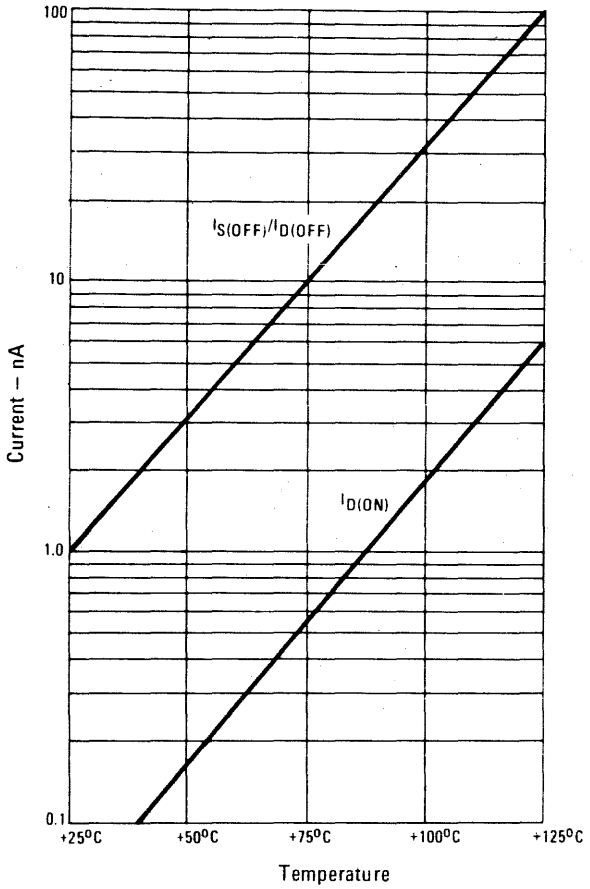


(HI-201)
ON RESISTANCE vs. ANALOG SIGNAL LEVEL
AND POWER SUPPLY VOLTAGE

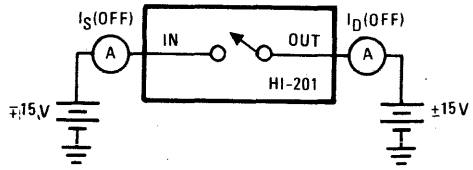


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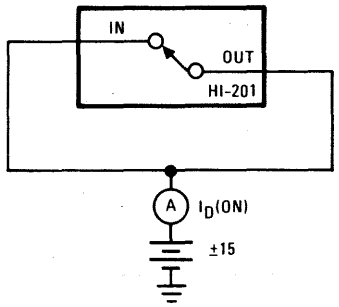
SWITCH LEAKAGE CURRENT vs. TEMPERATURE (HI-201)



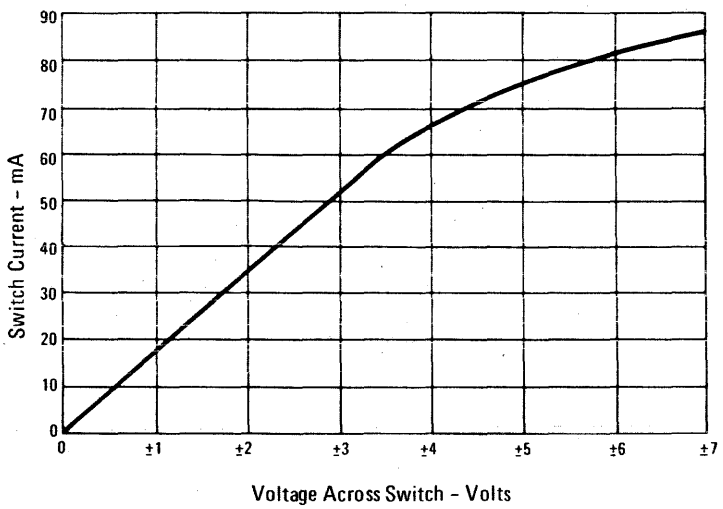
OFF LEAKAGE CURRENT vs. TEMPERATURE



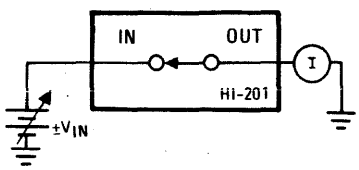
ON LEAKAGE CURRENT vs. TEMPERATURE



SWITCH CURRENT vs. VOLTAGE

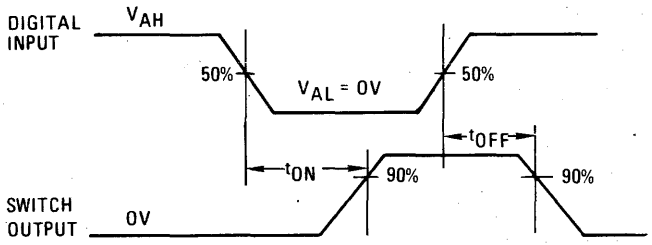


SWITCH CURRENT vs. VOLTAGE

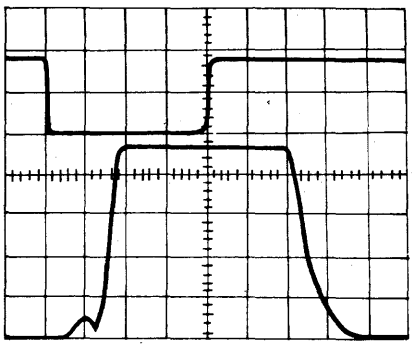


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SWITCHING WAVEFORMS



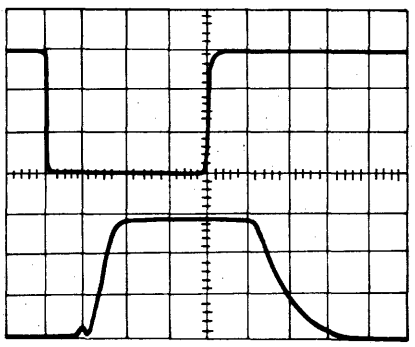
t_{ON}, t_{OFF}(TTL INPUT)
V_{IN} = 3.5V



Top: TTL Input
Bottom: Output

Horizontal: 100ns/Div.
Vertical: 2V/Div.

t_{ON}, t_{OFF}(CMOS INPUT)
V_{REF} = OPEN, V_{IN} = +15V



Top: CMOS Input
Bottom: Output

Vertical: 5V/Div.
Horizontal: 100ns/Div.

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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-1800A

Low Leakage Dual DPDT Analog Switch

FEATURES

- LEAKAGE AT +125°C (TYP.) 40nA
- SIGNAL RANGE ±15V
- "ON" RESISTANCE (TYP.) 125Ω
- ACCESS TIME (TYP.) 500ns
- DTL/TTL COMPATIBLE ADDRESS
- -55°C TO +125°C OPERATION

APPLICATIONS

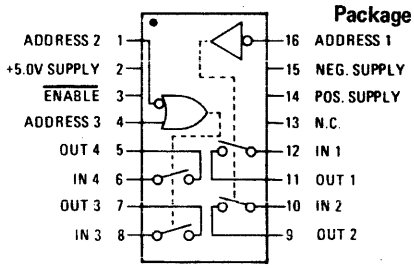
- SIGNAL SELECTOR
- CHOPPER
- SAMPLE AND HOLD
- GAIN SWITCHING

DESCRIPTION

The HI-1800A is a general purpose analog switch which may be used as a signal selector, multiplexer, chopper, or cross-point switch for signals from D.C. to R.F. The configuration is two independent DPST switches with versatile TTL compatibile addressing logic which allows connection as two SPDT, or as a single DPDT, SPDT, or SPST switch by connection of external jumpers. ON resistance decreases correspondingly when switching elements are connected in parallel. The HI-1800A is fabricated on a single dielectrically isolated chip using complementary N and P channel MOS devices. This unique process produces exceptionally low leakage currents (even at +125°C), constant ON resistance, low power dissipation, and fast switching. The HI-1800A is available in a hermetic 16 pin dual-in-line package.

PINOUT

Package Code 4B

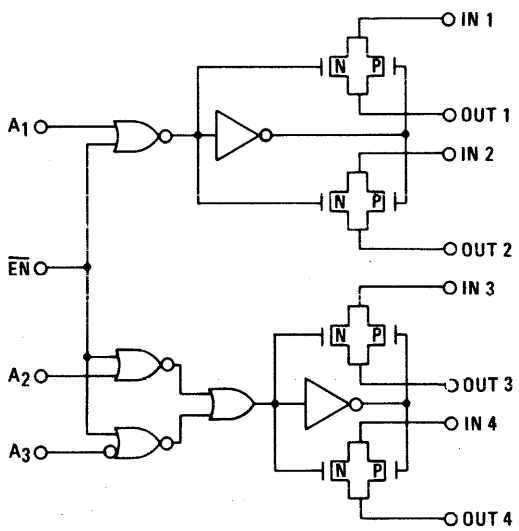


TRUTH TABLE

INPUT ADDRESS				SWITCH CHANNELS			
A1	A2	A3	$\overline{EN}$	1	2	3	4
L	X	X	L	ON	ON		
H	X	X	L	OFF	OFF		
X	L	X	L			ON	ON
X	X	H	L			ON	ON
X	H	L	L			OFF	OFF
X	X	X	H	OFF	OFF	OFF	OFF

H ≥ +4.0V L ≤ +0.4V

FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage Between Pins 14 and 15	40.0V	Digital Input Voltage	V^-_{Supply}, V^+_{Supply}
Logic Supply Voltage, Pin 2	30.0V	Total Power Dissipation	780 mW (Note 2)
Analog Input Voltage: V^+_{Supply} +2V	V^-_{Supply} -2V	Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

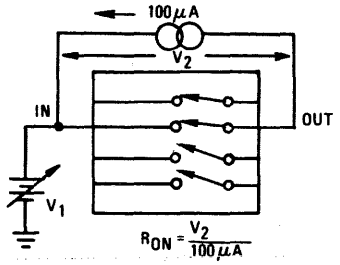
Supplies = +15V, −15V, +5.0V

PARAMETER	TEMP.	HI-1800A-2 −55°C to +125°C MIN.	TYP.	MAX.	HI-1800A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
* V_{IN}, Analog Signal Range	Full	-15		+15	−15		+15	V
* R_{ON}, ON Resistance (Note 3)	+25°C		125	200		125	200	Ω
	Full			250			250	Ω
* I_S (OFF), Input Leakage Current	Full		40	100		40	100	nA
* I_D (OFF), Output Leakage Current	Full		40	100		40	100	nA
* I_D (ON), On Channel Leakage Current	Full		40	100		40	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{IL}, Input Low Threshold	Full			0.4			0.4	V
V_{IH}, Input High Threshold (Note 4)	Full	4.0			4.0			V
* I_{IN}, Input Leakage Current	Full		.01	1		.01	1	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time (Note 5)	+25°C		500			500		ns
Break-Before-Make Delay	+25°C		200			200		ns
C_{IN}, Channel Input Capacitance	+25°C		8			8		pF
C_{OUT}, Channel Output Capacitance	+25°C		8			8		pF
C_D, Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		10			10		mW
P_{DS}, Standby Power (Note 6)	Full		10			10		mW
* I_+, Current Pin 14	Full		0.001	0.5		0.001	1	mA
* I_-, Current Pin 15	Full		0.5	1		0.5	2	mA
* I_L, Current Pin 2	Full		0.5	1		0.5	2	mA

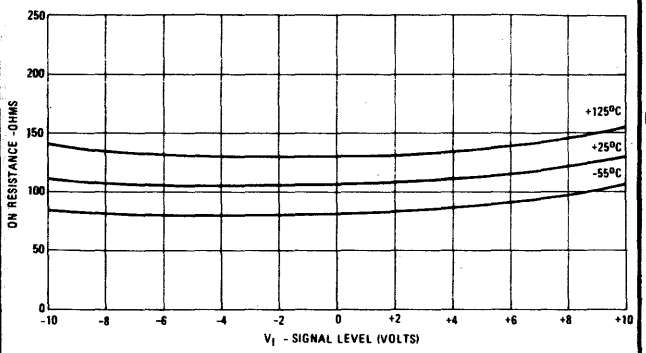
NOTES:
1. Voltage ratings apply when voltages at all other pins are within their nominal operating ranges.
2. Derate 9.25 mW/°C above t_A = +75°C
3. $V_{OUT} = \pm 10V$ $I_{OUT} = -100\mu A$.
4. To drive from DTL/TTL circuits, 1K pullup resistors to +5.0V supply are recommended.
5. Time measured to 90% of final output level; V_{OUT} = -5.0V to +5.0V, Digital Inputs = 0.4V to +4.0V.
6. Voltage at Pin 3, $\overline{ENABLE} \geq +4.0V$.

*100% Tested for Dash 8. ("Full" Tested at +25°C to +125°C)

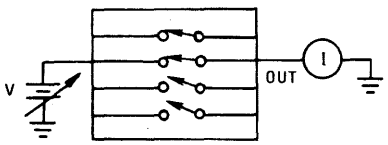
ON RESISTANCE vs ANALOG SIGNAL LEVEL



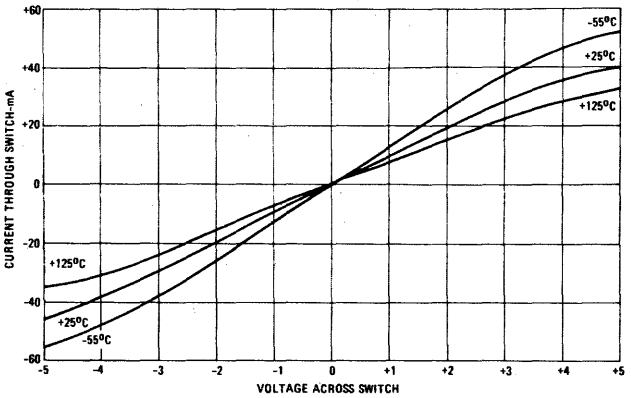
Test Circuit



ON CHANNEL CURRENT vs VOLTAGE

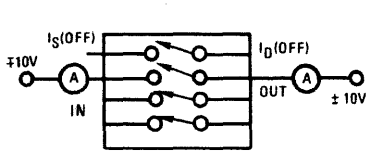


Test Circuit

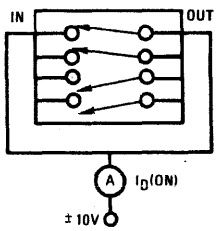


ON/OFF LEAKAGE CURRENTS vs TEMPERATURE

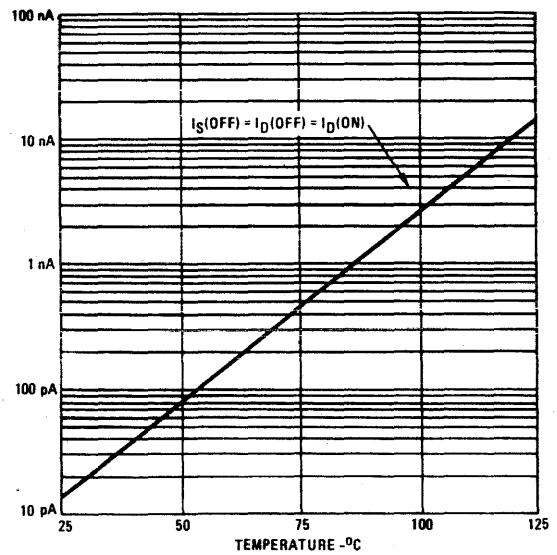
OFF LEAKAGE



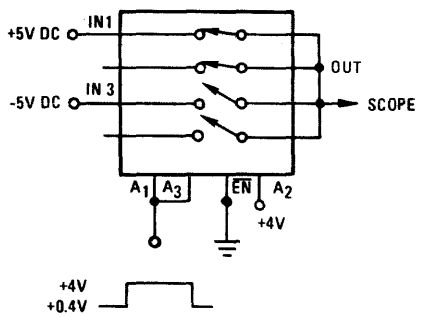
ON LEAKAGE

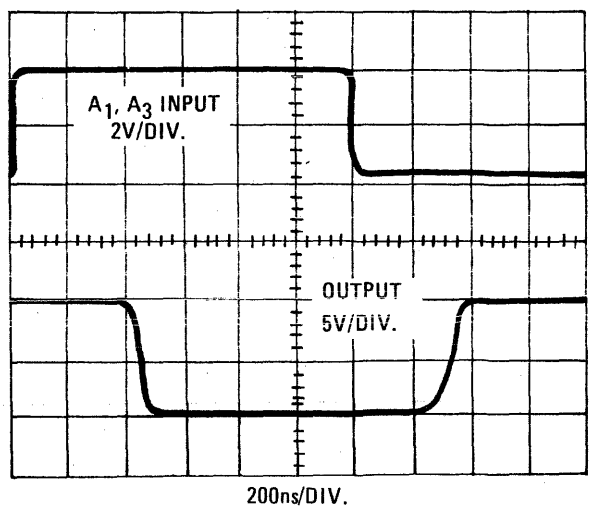


Test Circuit



ACCESS TIME



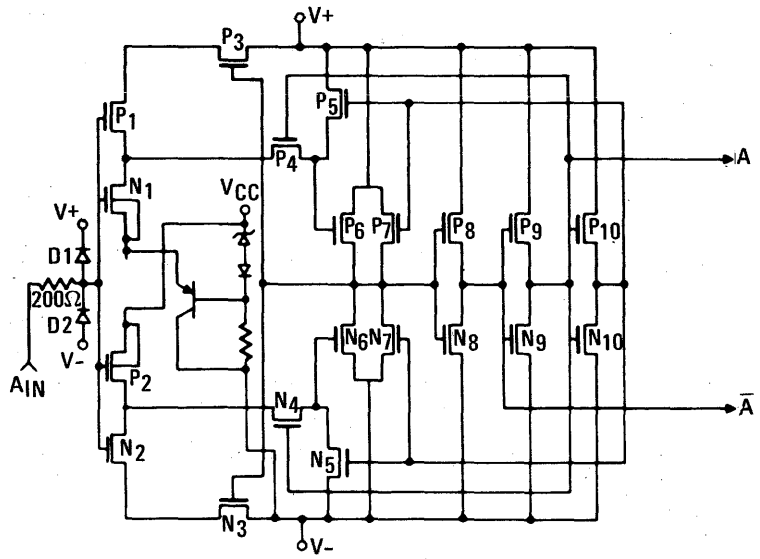


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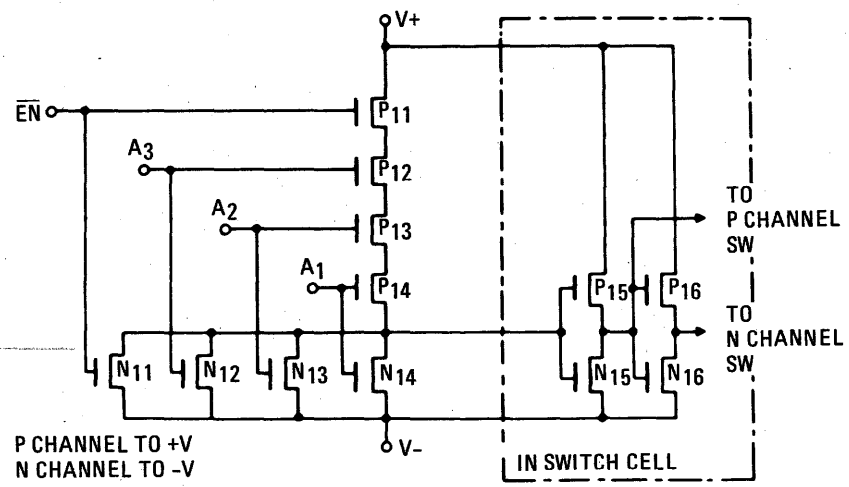
SCHEMATIC DIAGRAM

ADDRESS INPUT BUFFER

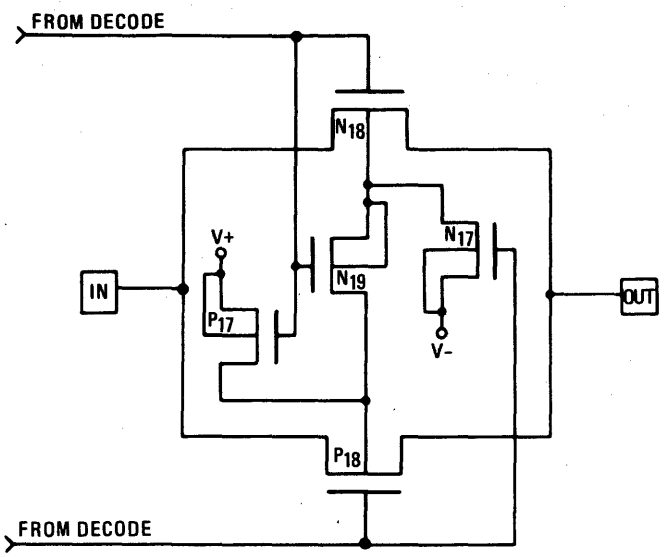
ALL N-CHANNEL BODIES TO V-
ALL P-CHANNEL BODIES TO V+
UNLESS OTHERWISE INDICATED



DECODER GATE



MULTIPLEX SWITCH



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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-5040 thru HI-5051
HI-5046A and HI-5047A

CMOS Analog Switches

FEATURES

- WIDE ANALOG SIGNAL RANGE ±15V
- LOW "ON" RESISTANCE (TYP) 25Ω
- HIGH CURRENT CAPABILITY (TYP) 80mA
- BREAK-BEFORE-MAKE SWITCHING
  - TURN-ON TIME (TYP) 370ns
  - TURN-OFF TIME (TYP) 280ns
- NO LATCH-UP
- INPUT MOS GATES ARE PROTECTED FROM ELECTROSTATIS DISCHARGE
- DTL, TTL, CMOS, PMOS COMPATIBLE

APPLICATIONS

- HIGH FREQUENCY SWITCHING
- SAMPLE AND HOLD
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING

DESCRIPTION

This family of CMOS analog switches offers low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 80mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 25 ohms for HI-5048 through HI-5051 and HI-5046A/5047A and 50Ω for HI-5040 through HI-5047.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at 25°C). This family of switches also features very low power operation (1.5mW at 25°C).

There are 14 devices in this switch series which are differentiated by type of switch action and value of R_{ON} (see Functional diagram). All devices are available in 16 pin D.I.P. packages. The HI-5040/5050 switches can directly replace IH-5040 series devices and are functionally compatible with the DG 180/190 family. Each switch type is available in the -55°C to +125°C and 0°C to +75°C performance grades.

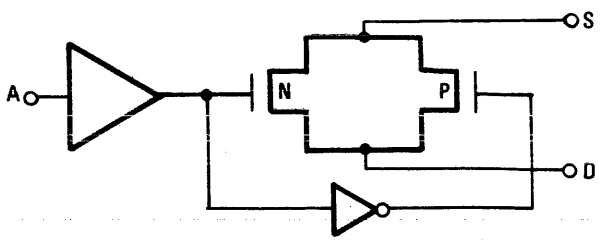
FUNCTIONAL DESCRIPTION

Package Code 4B

PART NUMBER	TYPE	RON
HI-5040	SPST	75Ω
HI-5041	DUAL SPST	75Ω
HI-5042	SPDT	75Ω
HI-5043	DUAL SPDT	75Ω
HI-5044	DPST	75Ω
HI-5045	DUAL DPST	75Ω
HI-5046	DPDT	75Ω
HI-5046A	DPDT	30Ω
HI-5047	4PST	75Ω
HI-5047A	4PST	30Ω
HI-5048	DUAL SPST	30Ω
HI-5049	DUAL DPST	30Ω
HI-5050	SPDT	30Ω
HI-5051	DUAL SPDT	30Ω

FUNCTIONAL DIAGRAM

TYPICAL SWITCH



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V^+ - V^-$)	36V	Analog Current (S to D)	80mA
V_R to Ground	V^+, V^-	Total Power Dissipation*	450mW
Digital and Analog	$V^+ + 4V$	Operating Temperature	
Input Voltage	$V^- - 4V$	HI-50XX-2	-55^oC to $+125^oC$
		HI-50XX-5	0^oC to $+75^oC$
		Storage Temperature	-65^oC to $+150^oC$

*Derate 6mW/^{o}C above $T_A = 75^oC$

ELECTRICAL CHARACTERISTICS

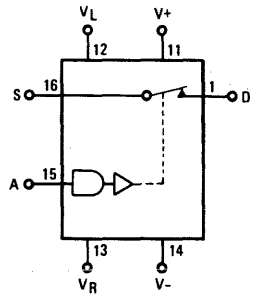
Unless Otherwise Specified
Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 3.0V; V_{AL} (Logic Level Low) = +0.8V, V_L = +5V
For Test Conditions, consult Performance Characteristics

PARAMETER	TEMP	-55°C to +125°C MIN	-55°C to +125°C TYP	-55°C to +125°C MAX	0°C to +75°C MIN	0°C to +75°C TYP	0°C to +75°C MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
* Analog Signal Range	Full	-15		+15	-15		+15	V
* Ron, "ON" Resistance (Note 1a)	+25°C		50			50		Ω
	Full			75			75	Ω
* Ron, "ON" Resistance (Note 1b)	+25°C		25			25		Ω
	Full			50			50	Ω
Ron, Channel-to-Channel Match (Note 1a)	+25°C		2	10		2	10	Ω
Ron, Channel-to-Channel Match (Note 1b)	+25°C		1	5		1	5	Ω
* $I_{S(OFF)} = I_{D(OFF)}$, Off Input or Output	+25°C		0.8			0.8		nA
Leakage Current	Full		100	500		100	500	nA
* $I_{D(ON)}$, On Leakage Current	+25°C		0.01			0.01		nA
	Full		2	500		2	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	3.0			3.0			V
* I_A, Input Leakage Current (High or Low)	Full		.01	1.0		.01	1.0	μA
SWITCHING CHARACTERISTICS								
t_{on}, Switch "ON" Time	+25°C		370	1000		370		ns
t_{off}, Switch "OFF" Time	+25°C		280	500		280		ns
Charge Injection (Note 2)	+25°C		5	20		5		mV
"OFF Isolation" (Note 3)	+25°C	75	80			80		dB
"Crosstalk" (Note 3)	+25°C	80	88			88		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		11			11		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		11			11		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		22			22		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS								
P_D, Quiescent Power Dissipation	+25°C		1.5			1.5		mW
* I^+, +15V Quiescent Current	Full			0.3			0.5	mA
* I^-, -15V Quiescent Current	Full			0.3			0.5	mA
* I_L, +5V Quiescent Current	Full			0.3			0.5	mA
* I_R, Gnd Quiescent Current	Full			0.3			0.5	mA

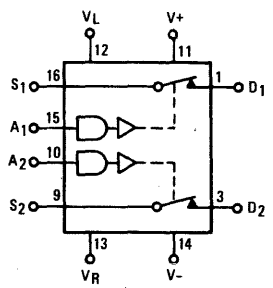
NOTES: 1. $V_{OUT} = \pm 10V$, $I_{OUT} = 1mA$
a) For HI-5040 thru HI-5047
b) For HI-5048 thru HI-5051, HI-5046A/5047A
2. $V_{IN} = 0V$, $C_L = 10{,}000pF$
3. $R_L = 100\Omega$, f= 100 KHz, $V_{IN} = 2\ V_{PP}$, $C_L = 5pF$

*100% Tested for Dash 8. ("Full" Tested at +25°C to +125°C)

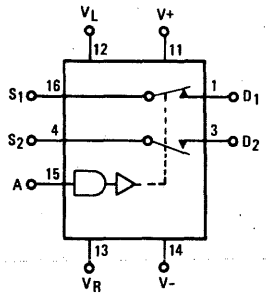
SPST
HI-5040 (75Ω)



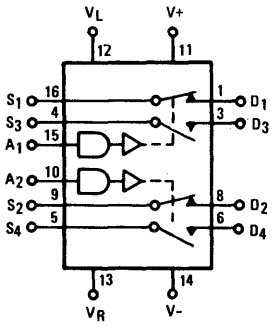
DUAL SPST
HI-5041 (75Ω)



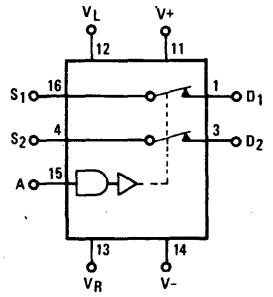
SPST
HI-5042 (75Ω)



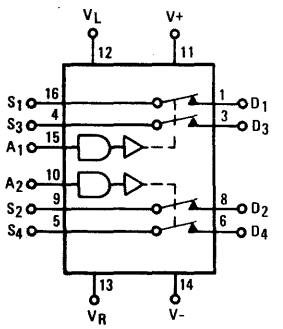
DUAL SPST
HI-5043 (75Ω)



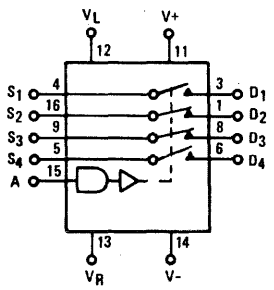
DPST
HI-5044 (75Ω)



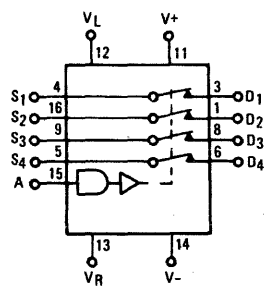
DUAL DPST
HI-5045 (75Ω)



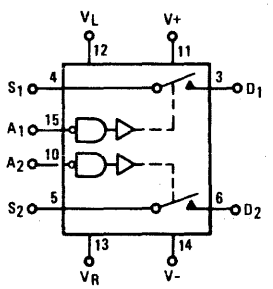
DPDT
HI-5046 (75Ω)
HI-5046A (30Ω)



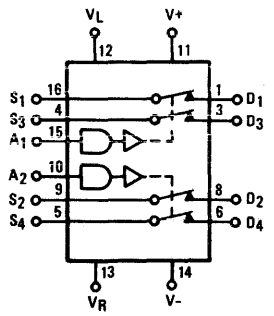
4PST
HI-5047 (75Ω)
HI-5047A (30Ω)



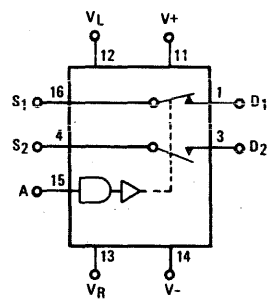
DUAL SPST
HI-5048 (30Ω)



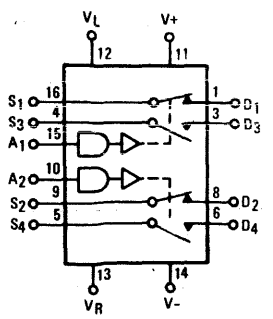
DUAL DPST
HI-5049 (30Ω)



SPST
HI-5050 (30Ω)



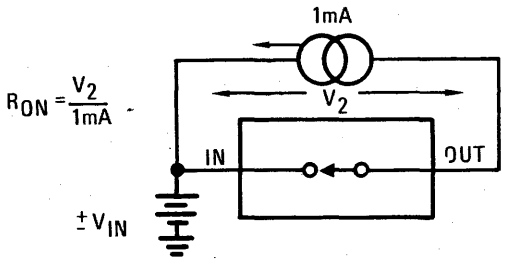
DUAL SPST
HI-5051 (30Ω)



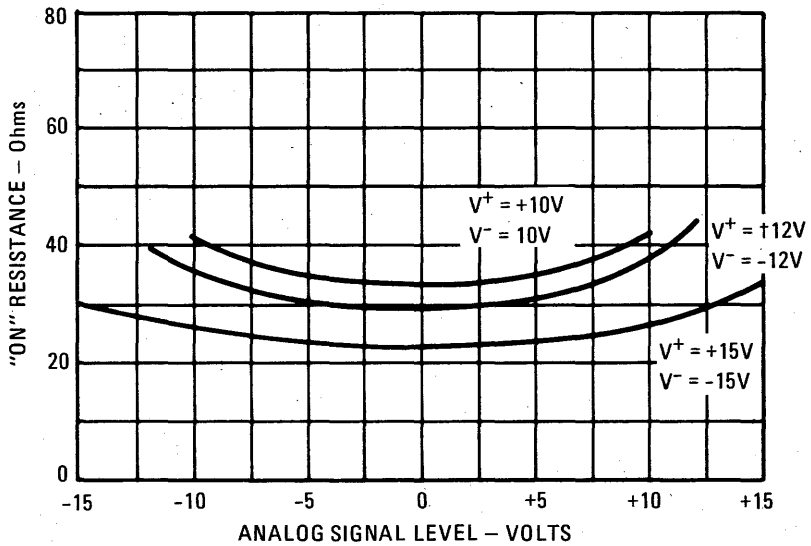
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(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$, $V_R = 0V$, $V_{AH} = 3.0V$ and $V_{AL} = 0.8V$

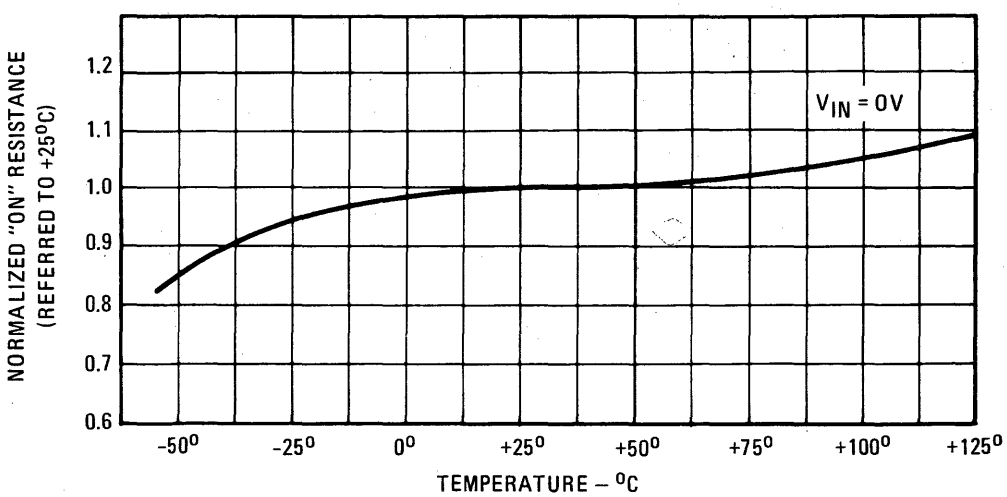
ON RESISTANCE vs. ANALOG SIGNAL LEVEL,
SUPPLY VOLTAGE AND TEMPERATURE



"ON"' RESISTANCE vs. ANALOG SIGNAL LEVEL
AND POWER SUPPLY VOLTAGE

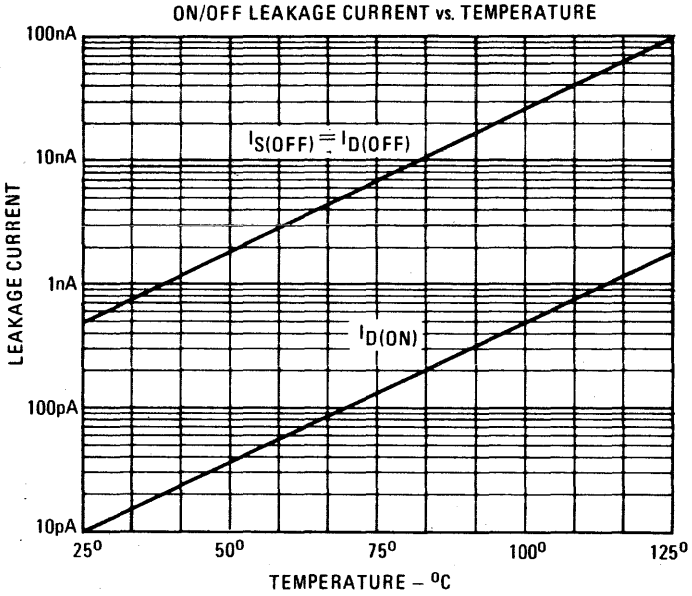


NORMALIZED "ON" RESISTANCE vs. TEMPERATURE

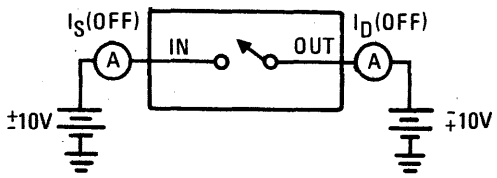


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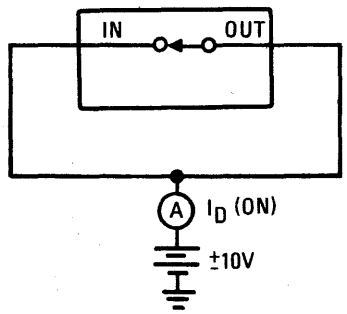
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



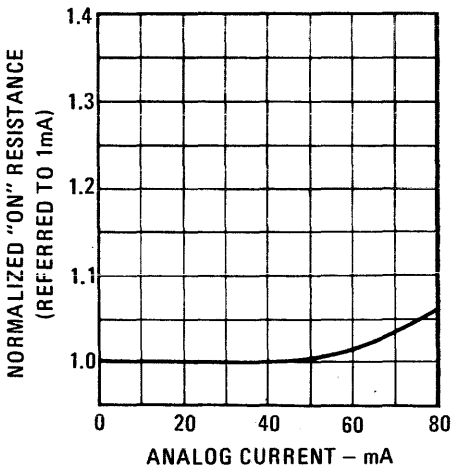
OFF LEAKAGE CURRENT vs. TEMPERATURE



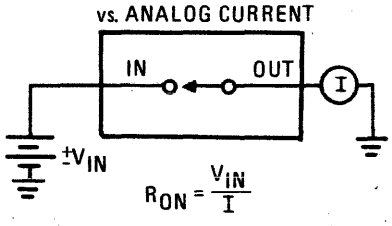
ON LEAKAGE CURRENT vs. TEMPERATURE



NORMALIZED "ON" RESISTANCE vs. ANALOG CURRENT

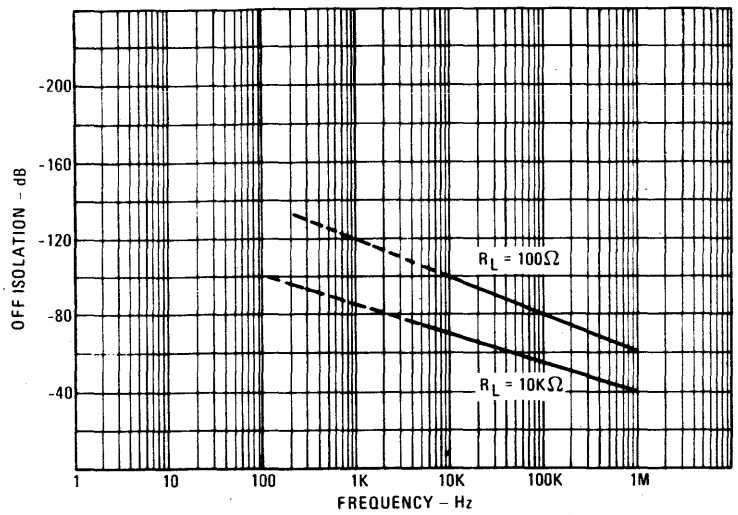


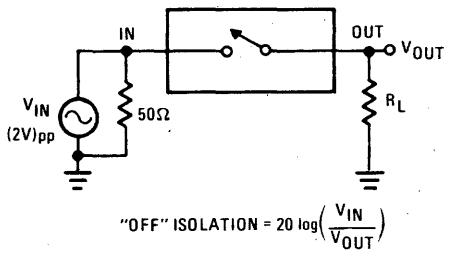
"ON" RESISTANCE vs. ANALOG CURRENT



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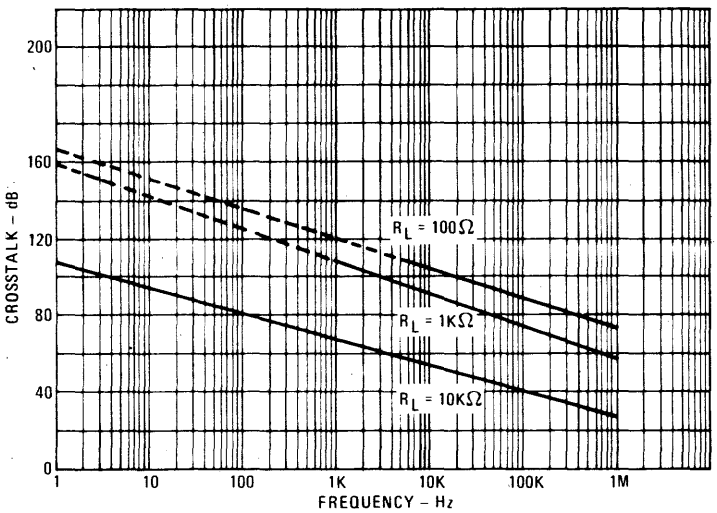
"OFF" ISOLATION vs. FREQUENCY

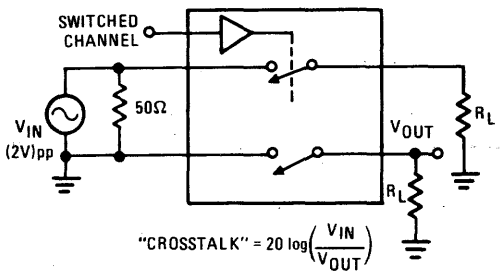




"OFF" ISOLATION = $20 \log\left(\frac{V_{IN}}{V_{OUT}}\right)$

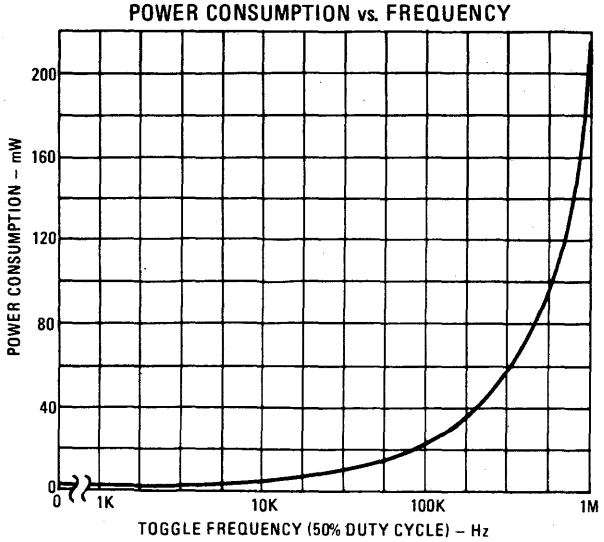
CROSSTALK vs. FREQUENCY

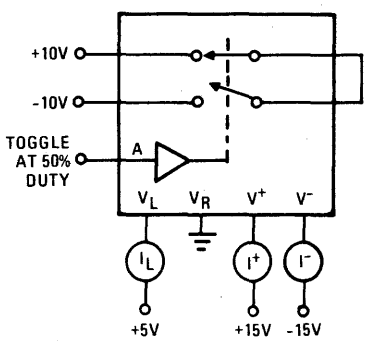




"CROSSTALK" = $20 \log\left(\frac{V_{IN}}{V_{OUT}}\right)$

POWER CONSUMPTION vs. FREQUENCY

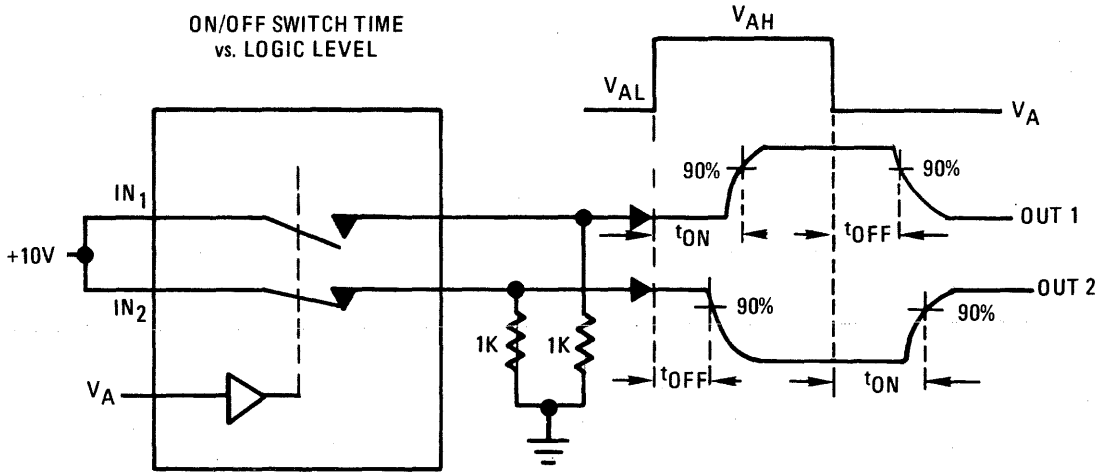


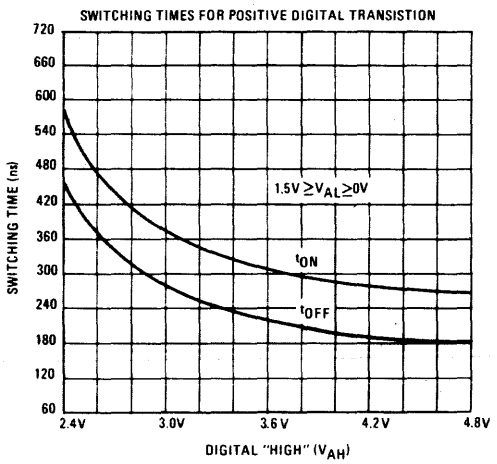


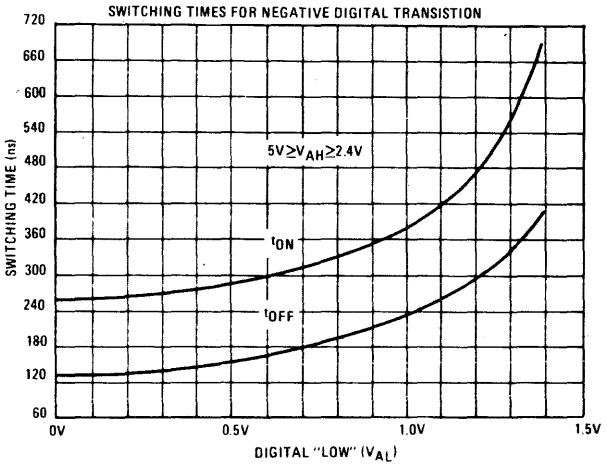
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SWITCHING CHARACTERISTICS

ON/OFF SWITCH TIME
vs. LOGIC LEVEL

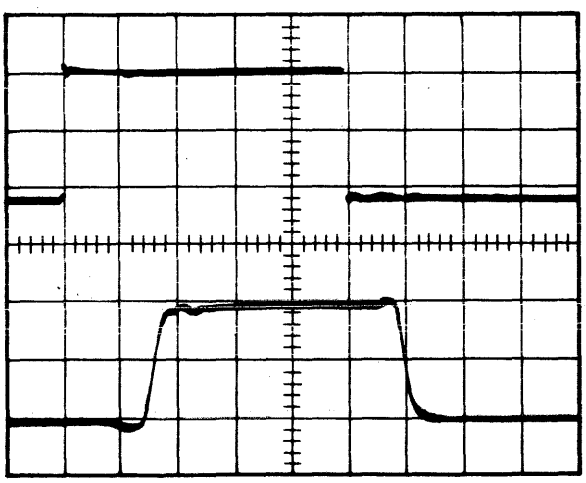






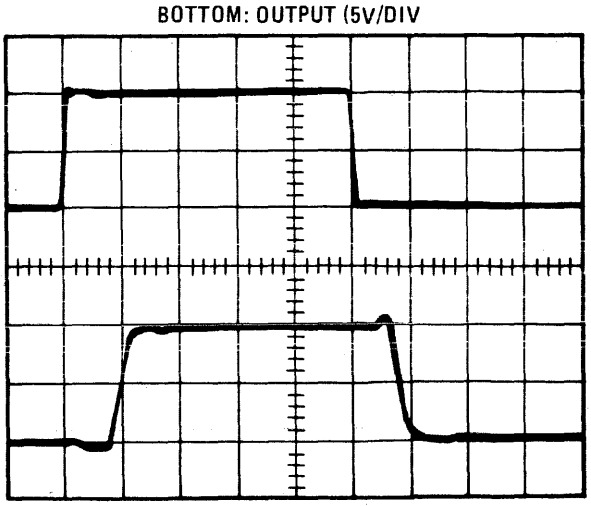
SWITCHING WAVEFORMS

TOP: TTL INPUT (1V/DIV)
V_{AH} = 3V, V_{AL} = 0.8V
BOTTOM: OUTPUT (5V/DIV)



200ns/DIV

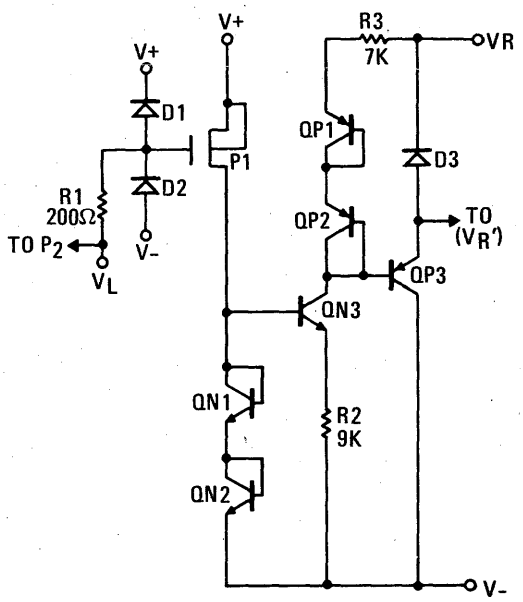
TOP: CMOS INPUT (5V/DIV)
V_{AH} = 10V, V_{AL} = 0V
BOTTOM: OUTPUT (5V/DIV



200ns/DIV

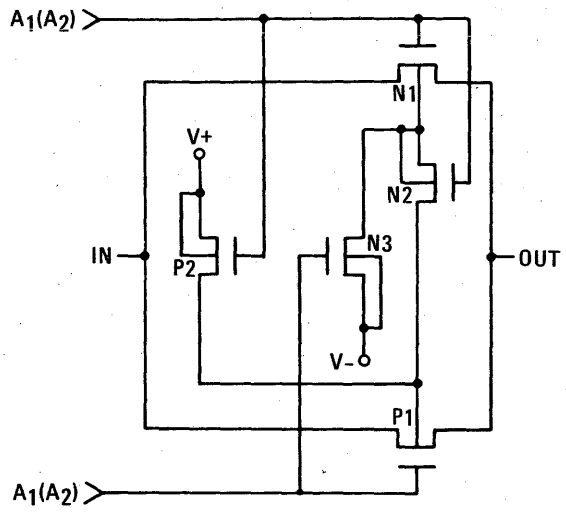
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TTL/CMOS
REFERENCE CIRCUIT*

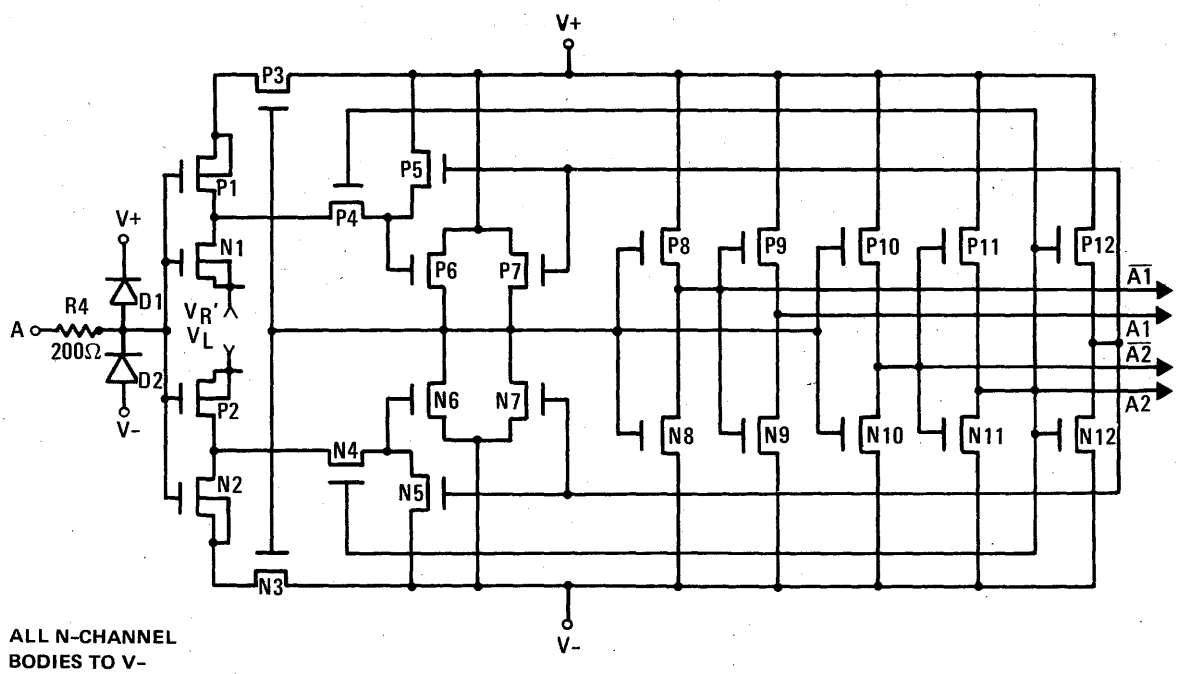


*Connect V^+ to V_L for minimizing power consumption when driving from CMOS circuits

SWITCH CELL



DIGITAL INPUT BUFFER
AND LEVEL SHIFTER



ALL N-CHANNEL
BODIES TO V-

ALL P-CHANNEL
BODIES TO V+

EXCEPT AS SHOWN

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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-506/HI-507

Single 16/Differential 8 Channel CMOS Analog Multiplexers

FEATURES

- LOW ON RESISTANCE (TYP.) 170Ω
- WIDE ANALOG SIGNAL RANGE ±15V
- DIRECTLY TTL/CMOS COMPATIBLE 2.4V (LOGIC "1")
- ACCESS TIME (TYP.) 300ns
- HIGH CURRENT CAPABILITY (TYP.) 50mA
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- DEMULTIPLEXING
- SELECTOR SWITCH

DESCRIPTION

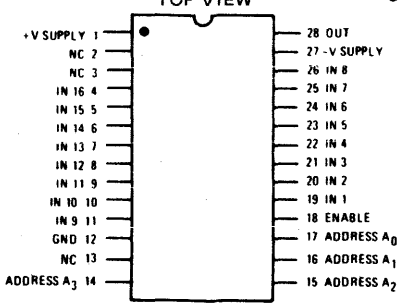
The HI-506/507 are monolithic high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit input for disabling all channels. Dielectric Isolation (DI) is used to fabricate these devices for enhanced reliability and performance over conventional Junction-Isolated (JI) devices. (See Application Note 521). Substrate leakages and parasitic capacitance are much lower in DI resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.3nA) and low channel ON resistance (170Ω) assure optimum performance in low level or current mode applications. Operation is specified with nominal ±15V supplies, however, supplies as low as ±7V can be used at somewhat lower performance. The HI-506/507 internally develops a +5V digital logic reference from the positive supply which eliminates an additional supply and provides direct TTL/CMOS compatibility without interface pull-up resistors.

The HI-506 is a single-ended 16 channel multiplexer while the HI-507 is a differential 8 channel version. Either device is ideally suited for medical instrumentation, telemetry systems and microprocessor based data acquisition systems.

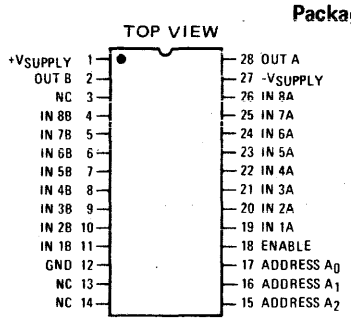
The HI-506-2 and HI-507-2 are specified over -55°C to +125°C, while the -5 versions are specified over 0°C to +75°C.

PINOUT

HI-506 TOP VIEW **Package Code 1M**



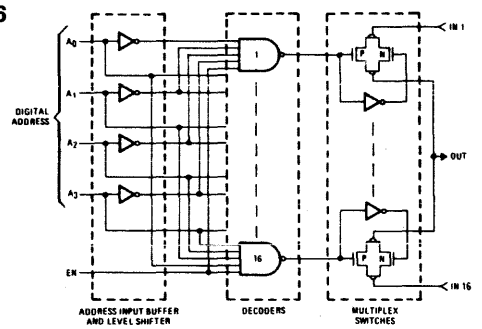
HI-507 TOP VIEW **Package Code 1M**



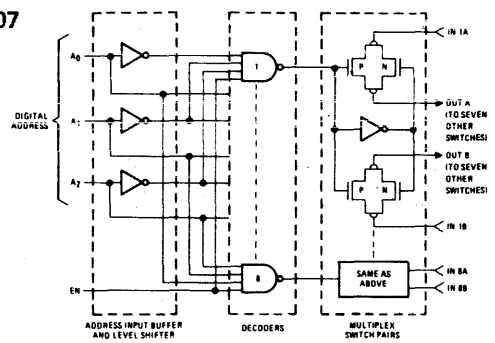
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

FUNCTIONAL DIAGRAM

HI-506



HI-507



SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27 — 40V

V_{EN}, V_A, Digital Input Overvoltage:

V_A { V_{Supply} (+) +4V; V_{Supply} (-) -4V

Analog Input Overvoltage: (Note 6)

V_D or V_S { V_{Supply} (+) +2V; V_{Supply} (-) -2V

Total Power Dissipation* — 1200 mW

Operating Temperature:

HI-506/HI-507-2 — -55°C to +125°C

HI-506/HI-507-5 — 0°C to +75°C

Storage Temperature — -65°C to +150°C

*Derate 8mW/°C above T_A = +25°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified: Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics section.

		HI-506/HI-507-2 -55°C to +125°C			HI-506/HI-507-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
* V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, On Resistance (Note 1)	+25°C		170	300		270	400	Ω
	Full			400			500	Ω
* ΔR_{ON}, (Between Channels)	+25°C		6			6		%
* $I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
* $I_{D(OFF)}$, Off Output Leakage Current	+25°C		0.3			1.0		nA
HI-506	Full			±500			±500	nA
HI-507	Full			±250			±250	nA
* $I_{D(ON)}$, On Channel Leakage Current	+25°C		0.3			1.0		nA
HI-506	Full			±500			±500	nA
HI-507	Full			±250			±250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			+0.8			+0.8	V
V_{AH}, Input High Threshold	Full	+2.4			+2.4			V
* I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			5.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		300	1000		300		ns
t_{OPEN}, Break-Before Make Delay	+25°C		80			80		ns
$t_{ON(EN)}$, Enable Delay (ON)	+25°C		300	1000		300		ns
$t_{OFF(EN)}$, Enable Delay (OFF)	+25°C		300	1000		300		ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.025%)	+25°C		2.4			2.4		μs
"Off Isolation" (Note 3)	+25°C		75			75		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		4			4		pF
$C_{D(OFF)}$, Channel Output Capacitance								
HI-506	+25°C		44			44		pF
HI-507	+25°C		22			22		pF
C_A, Digital Input Capacitance	+25°C		2.2			2.2		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.08			0.08		pF
POWER REQUIREMENTS								
* I+, Current Pin 1 (Note 4)	Full		1.7	3.0		3.4	5.0	mA
* I-, Current Pin 27 (Note 4)	Full		0.4	1.0		0.8	2.0	mA
* I+, Standby (Note 5)	Full		1.7	3.0		3.4	5.0	mA
* I-, Standby (Note 5)	Full		0.4	1.0		0.8	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -1mA
2. Digital Inputs are Mos Gates. Typical Leakage Less Than 1nA.
3. V_{EN} = 0.8V, R_L = 1K, C_L = 28pF, V_S = 7VRMS, f = 500kHz.
4. V_{EN} = 4.0V, All V_A = 4.0V
5. V_{EN} = 0V, All V_A = 0V
6. If Analog Input Overvoltage Conditions are Anticipated, Use of HI-506A/507A Protected Multiplexers is Recommended. See HI-506A/507A Data Sheet.

*100% Tested for Dash 8. ("Full" Tested at +25°C to +125°C)

TRUTH TABLES

HI-506

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507

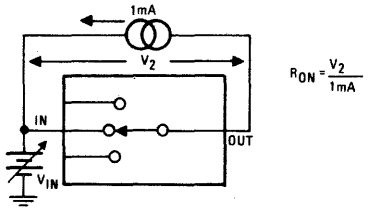
A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

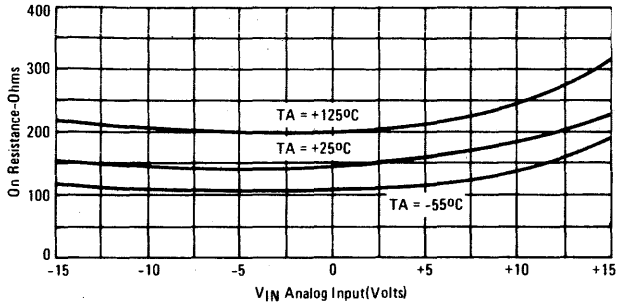
Unless Otherwise Specified; $T_A = 25^oC$, $V_{Supply} = \pm 15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$.

TEST CIRCUIT NO. 1

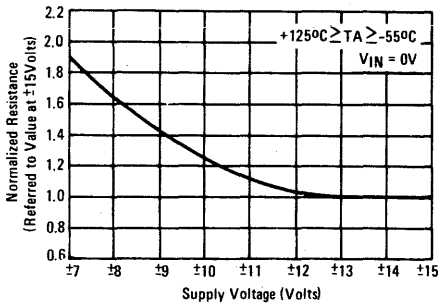
ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE



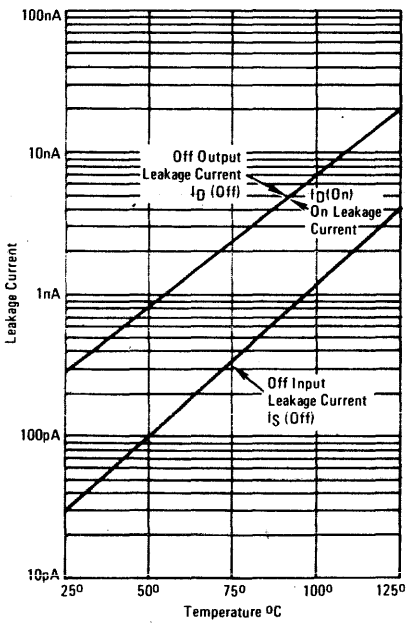
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE

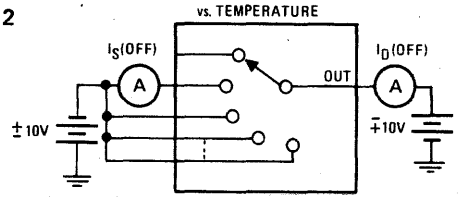


LEAKAGE CURRENT vs. TEMPERATURE



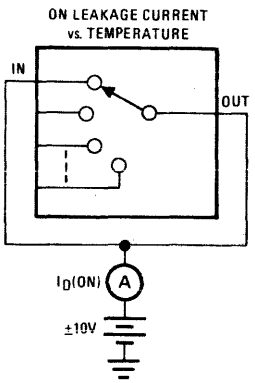
TEST CIRCUIT NO. 2

OFF LEAKAGE CURRENT vs. TEMPERATURE

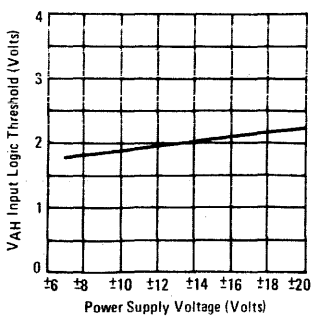


TEST CIRCUIT NO. 3

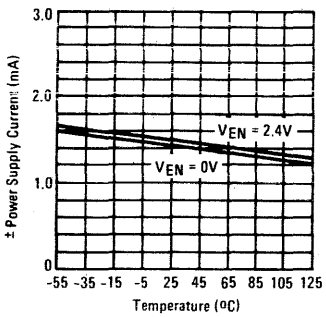
ON LEAKAGE CURRENT vs. TEMPERATURE



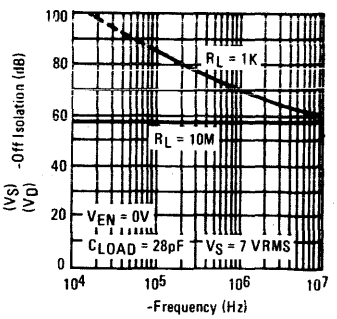
LOGIC THRESHOLD vs. POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT vs. TEMPERATURE



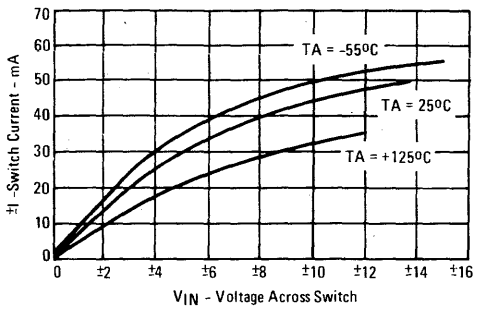
OFF ISOLATION vs. FREQUENCY



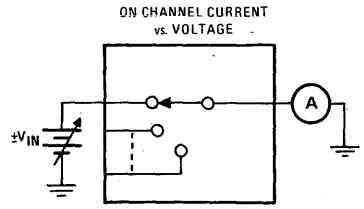
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PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

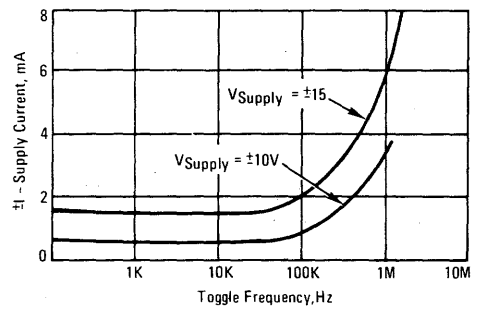
ON CHANNEL CURRENT vs. VOLTAGE



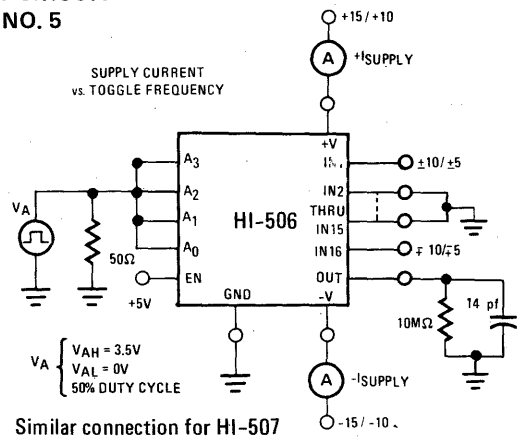
TEST CIRCUIT NO. 4



SUPPLY CURRENT vs. TOGGLE FREQUENCY

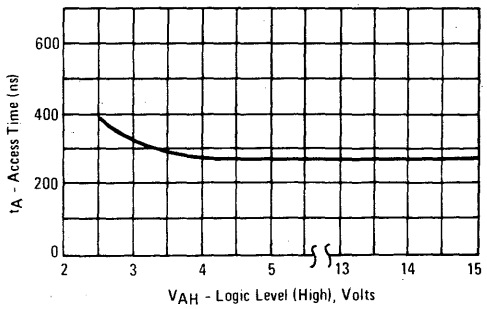


TEST CIRCUIT NO. 5

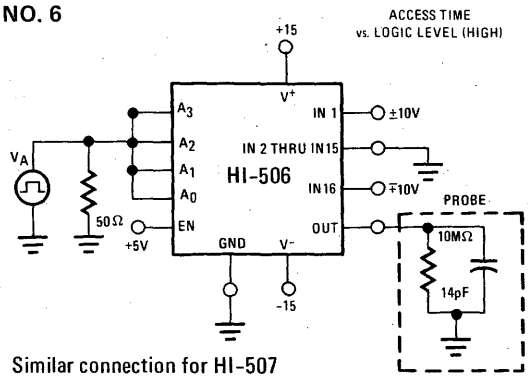


Similar connection for HI-507

ACCESS TIME vs. LOGIC LEVEL (HIGH)

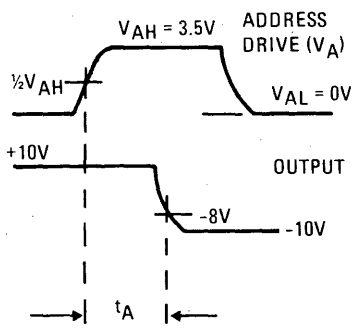


TEST CIRCUIT NO. 6

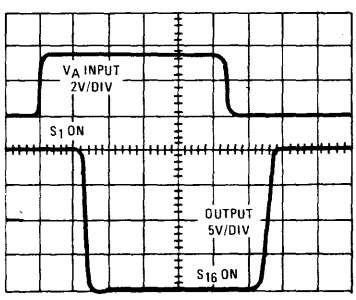


Similar connection for HI-507

SWITCHING WAVEFORMS

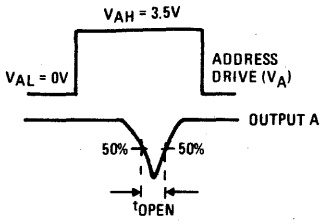


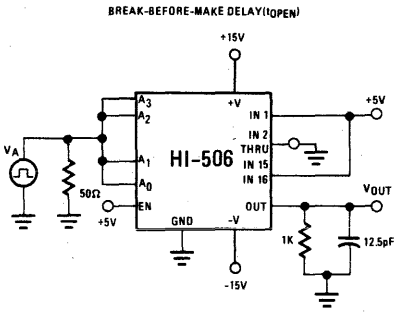
ACCESS TIME



SWITCHING WAVEFORMS (continued)

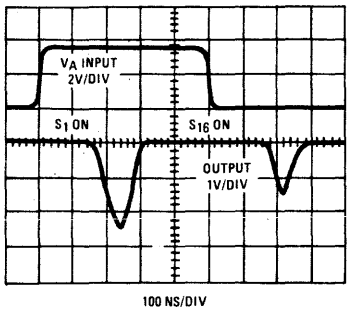
TEST CIRCUIT NO. 7



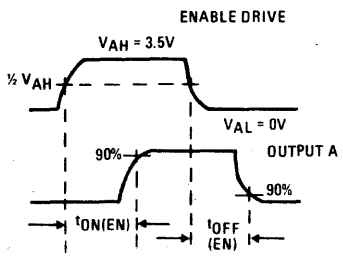


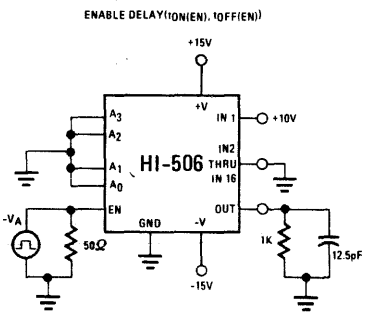
Similar connection for HI-507

BREAK-BEFORE-MAKE DELAY (t_{OPEN})



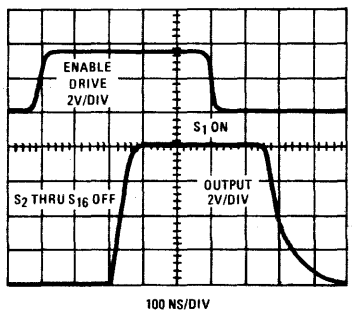
TEST CIRCUIT NO. 8





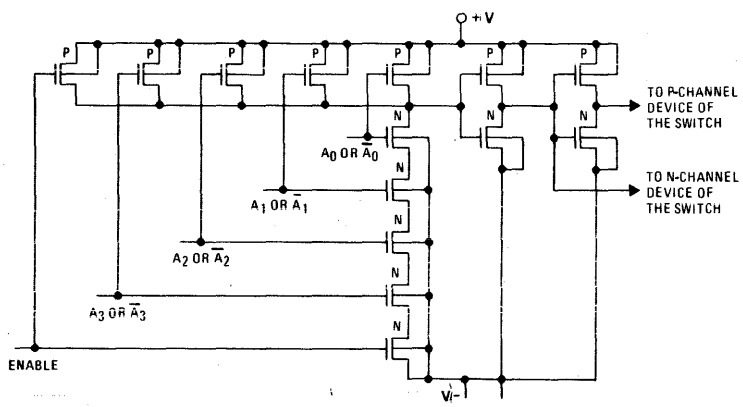
Similar connection for HI-507

ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



SCHEMATIC DIAGRAMS

ADDRESS DECODER

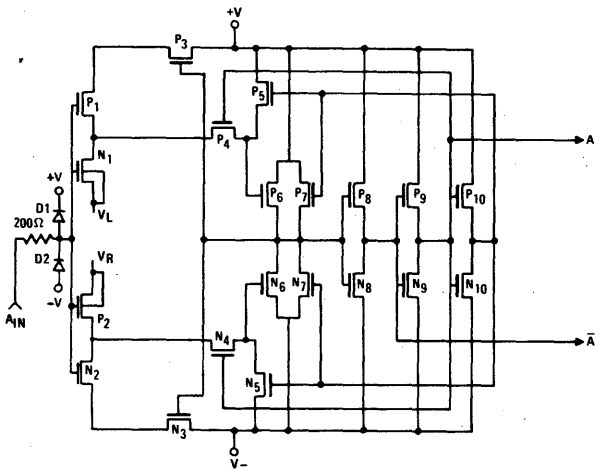


Delete A_3 or $\overline{A}_3$ Input for HI-507

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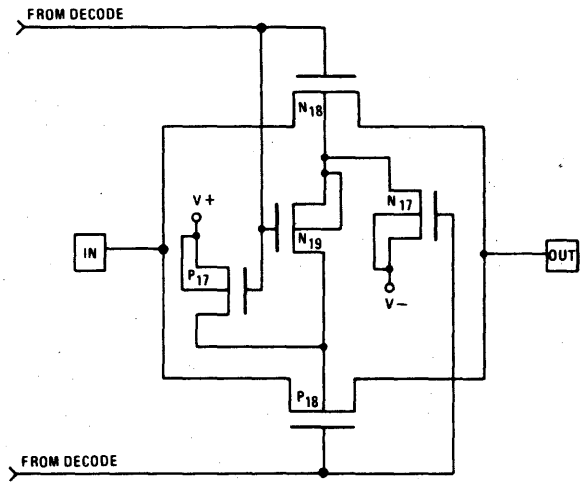
SCHEMATIC DIAGRAM (continued)

ADDRESS INPUT BUFFER LEVER SHIFTER

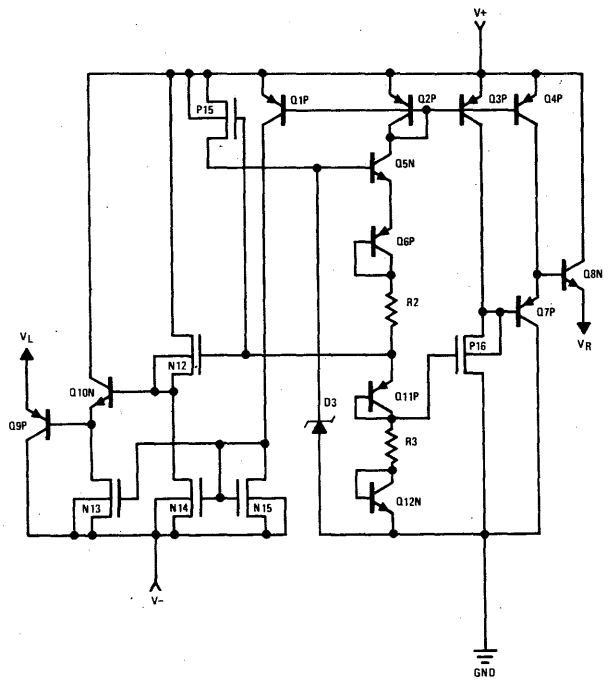


All N-Channel Bodies to V-
All P-Channel Bodies to V+ Unless Otherwise Indicated.

MULTIPLEX SWITCH



TTL REFERENCE CIRCUIT



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-506A/HI-507A

16 Channel CMOS Analog Multiplexer with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW

APPLICATIONS

- DATA ACQUISITION
- INDUSTRIAL CONTROLS
- TELEMETRY

DESCRIPTION

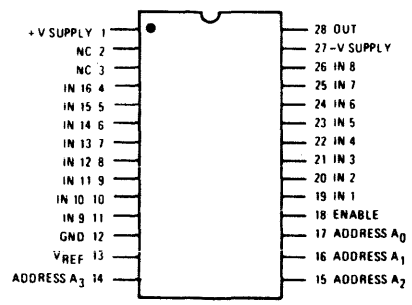
The HI-506A and HI-507A are dielectrically isolated CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage currents combine to produce low errors. Application Notes 520 and 521 further explain these features.

The HI-506A-2 and HI-507A-2 are specified over -55°C to +125°C while the -5 versions are specified over 0°C to +75°C.

PINOUT

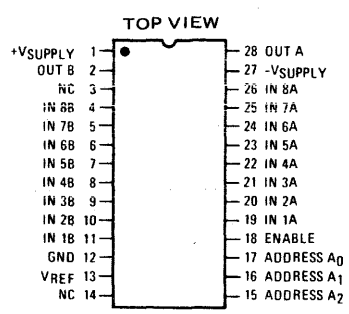
HI-506A **Package Code 1M**

TOP VIEW



HI-507A **Package Code 1M**

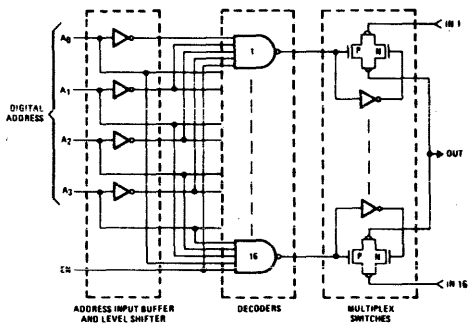
TOP VIEW



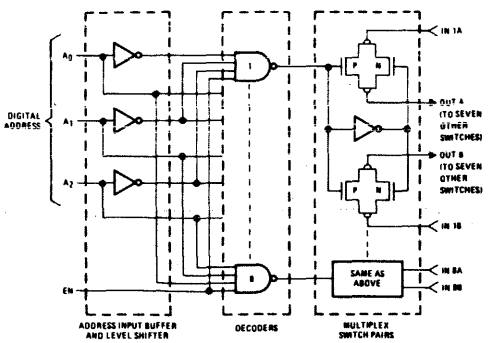
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

FUNCTIONAL DIAGRAM

HI-506A



HI-507A



SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27	40V
V_{REF} to Ground V+ to Ground	+20V
V_{EN}, V_A, Digital Input Overvoltage:	
V_A (V_{Supply} (+))	+4V
V_A (V_{Supply} (−))	-4V
Analog Overvoltage:	
V_S (V_{Supply} (+))	+20V
V_S (V_{Supply} (−))	-20V

Total Power Dissipation*	1200mW
Operating Temperature	
HI-506A/507A-2	-55°C to +125°C
HI-506A/507A-5	0°C to +75°C
Storage Temperature	-65°C to +150°C

*Derate 8mW/°C above T_A = +25°C

ELECTRICAL CHARACTERISTICS (Unless Otherwise Specified)

Supplies = +15V, -15V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characterisitcs section.

PARAMETER		TEMP.	HI-506A/507A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-506A/507A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS									
*V_S, Analog Signal Range		Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 1)		+25°C		1.2	1.5		1.5	1.8	KΩ
		Full		1.5	2.0		1.8	2.0	KΩ
*I_S (OFF), Off Input Leakage Current		+25°C		0.03			0.03		nA
		Full			±50			±50	nA
*I_D (OFF), Off Output Leakage Current		+25°C		1.0			1.0		nA
	HI-506A	Full			±500			±500	nA
	HI-507A	Full			±250			±250	nA
*I_D (OFF) with Input Overvoltage Applied (Note 2)		+25°C		4.0			4.0		nA
		Full			2.0				μA
*I_D (ON), On Channel Leakage Current		+25°C		0.1			0.1		nA
	HI-506A	Full			±500			±500	nA
	HI-507A	Full			±250			±250	nA
DIGITAL INPUT CHARACTERISTICS									
V_{AL}, Input Low Threshold | TTL Drive		Full			0.8			0.8	V
V_{AH}, Input High Threshold | (Note 7)		Full	4.0			4.0			V
V_{AL} | MOS Drive (Note 3)		+25°C			0.8			0.8	V
V_{AH} |		+25°C	6.0			6.0			V
*I_A, Input Leakage Current (High or Low)		Full			1.0			5.0	μA
SWITCHING CHARACTERISTICS									
t_A, Access Time		+25°C		0.5	1.0		0.5		μs
t_{OPEN}, Break-Before Make Delay		+25°C		80			80		ns
$t_{ON (EN)}$, Enable Delay (ON)		+25°C		300			300		ns
$t_{OFF (EN)}$, Enable Delay (OFF)		+25°C		300			300		ns
Settling Time (0.1%)		+25°C		1.3			1.3		μs
(0.025%)		+25°C		4.4			4.4		μs
"Off Isolation" (Note 4)		+25°C		65			65		dB
$C_{S (OFF)}$, Channel Input Capacitance		+25°C		5			5		pF
$C_{D (OFF)}$, Channel Output Capacitance	HI-506A	+25°C		50			50		pF
	HI-507A	+25°C		25			25		pF
C_A, Digital Input Capacitance		+25°C		5			5		pF
$C_{DS (OFF)}$, Input to Output Capacitance		+25°C		0.1			0.1		pF
POWER REQUIREMENTS									
P_D, Power Dissipation		Full		7.5			7.5		mW
*I+, Current Pin 1 (Note 5)		Full		0.5	2.0		0.5	5.0	mA
*I-, Current Pin 27 (Note 5)		Full		0.02	1.0		0.02	2.0	mA
*I+, Standby (Note 6)		Full		0.5	2.0		0.5	5.0	mA
*I-, Standby (Note 6)		Full		0.02	1.0		0.02	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = - 100 μA.
2. Analog Overvoltage = ±33V.
3. V_{REF} = +10V.
4. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3VRMS, f = 500KHz.
5. V_{EN} = +4.0V.
6. V_{EN} = 0.8V.
7. To drive from DTL/TTL circuits, 1KΩ pull-up resistors to +5.0V supply are recommended.

*100% Tested for Dash 8.
("Full" Tested at +25°C to +125°C)

TRUTH TABLES

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

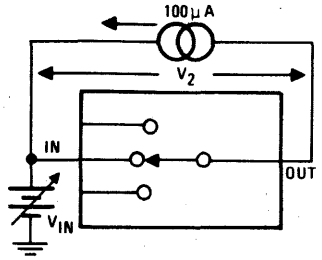
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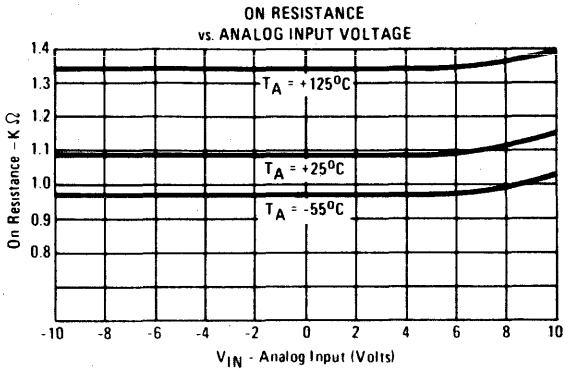
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

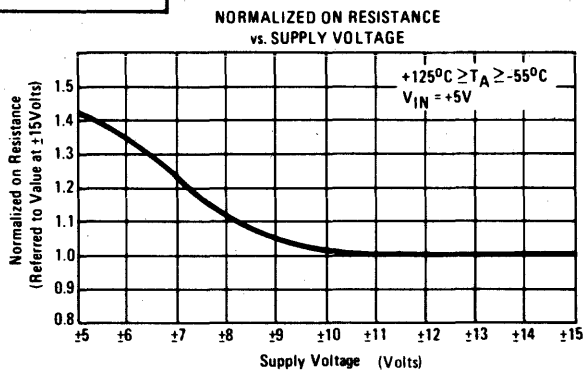
(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$ AND V_{REF} = OPEN.)

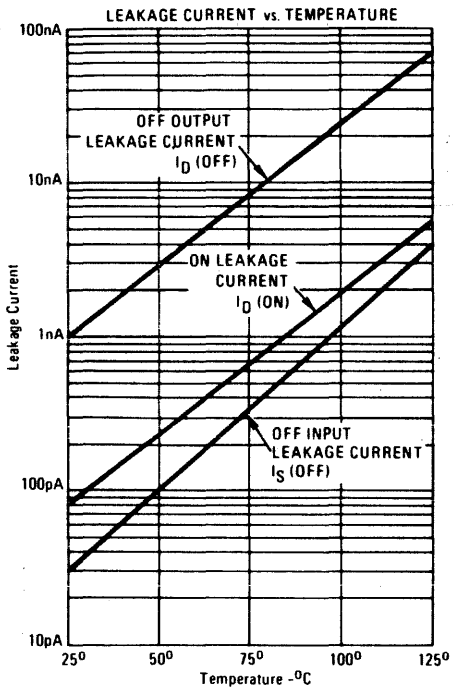
TEST CIRCUIT NO.1

$R_{ON} = \frac{V_2}{100\mu A}$

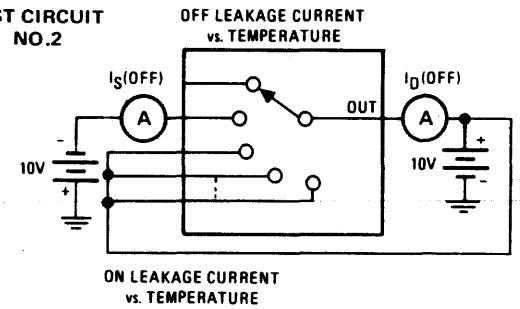


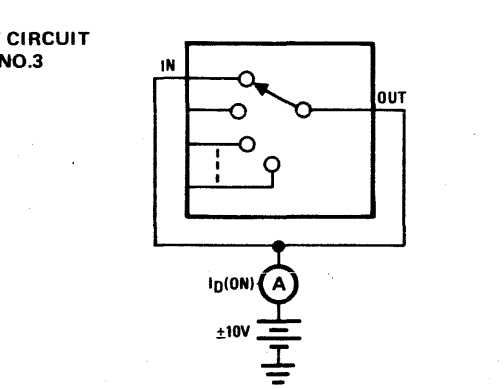




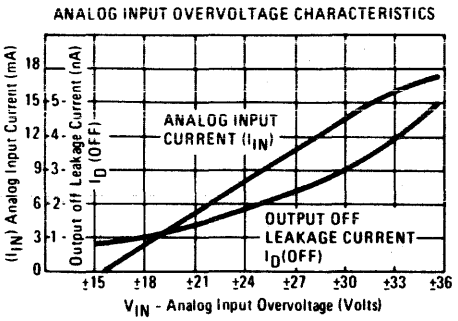


TEST CIRCUIT NO.2



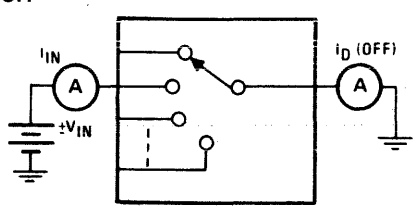


TEST CIRCUIT NO.3



ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

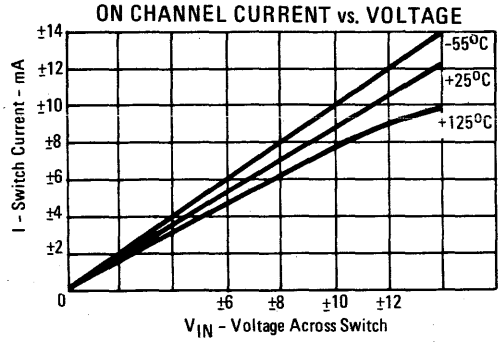
TEST CIRCUIT NO.4



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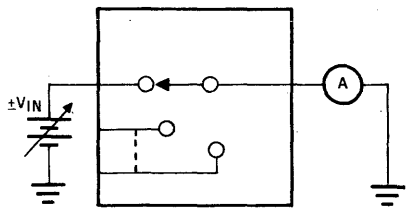
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

ON CHANNEL CURRENT vs. VOLTAGE

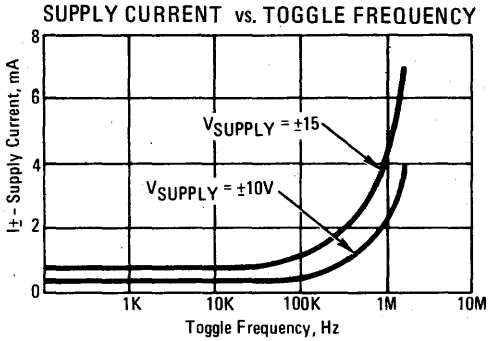


TEST CIRCUIT NO. 5

ON CHANNEL CURRENT vs. VOLTAGE

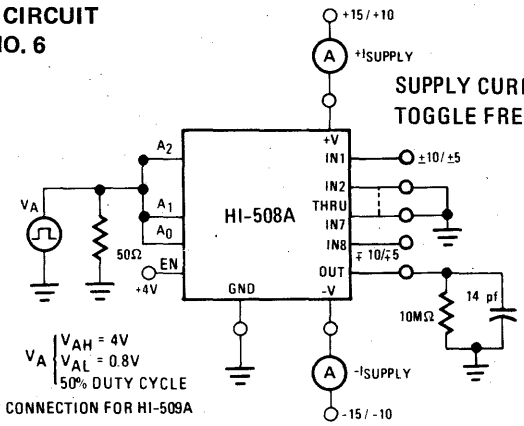


SUPPLY CURRENT vs. TOGGLE FREQUENCY



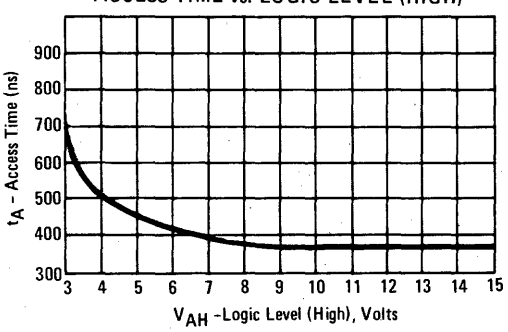
TEST CIRCUIT NO. 6

SUPPLY CURRENT vs.. TOGGLE FREQUENCY



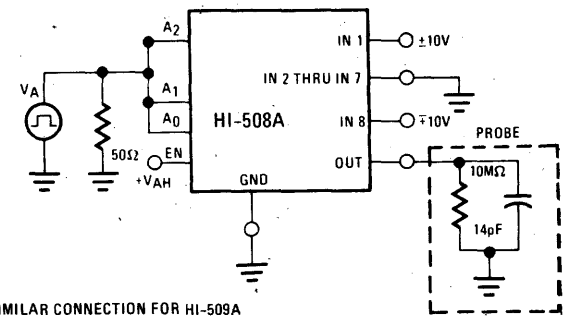
*SIMILAR CONNECTION FOR HI-509A

ACCESS TIME vs. LOGIC LEVEL (HIGH)



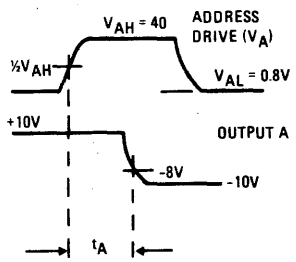
TEST CIRCUIT NO. 7

ACCESS TIME vs. LOGIC LEVEL(HIGH)

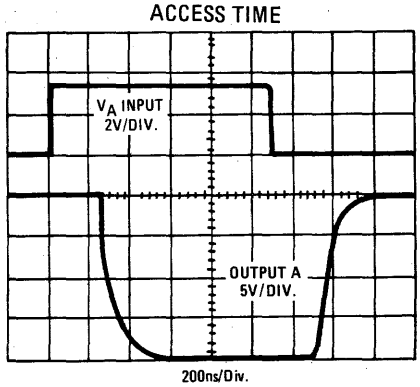


* SIMILAR CONNECTION FOR HI-509A

SWITCHING WAVEFORMS



ACCESS TIME



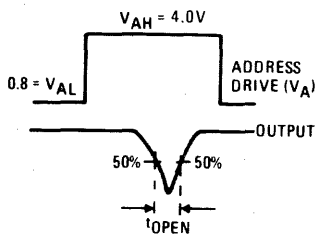
200ns/Div.

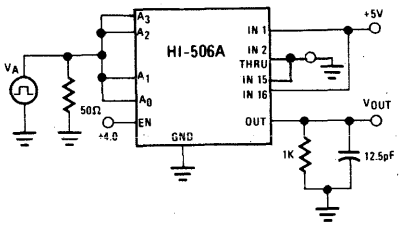
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SWITCHING WAVEFORMS (continued)

TEST CIRCUIT
NO.8

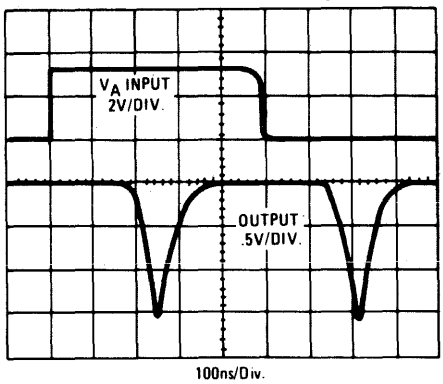
BREAK BEFORE MAKE DELAY (t_{OPEN})





SIMILAR CONNECTION FOR HI-507A

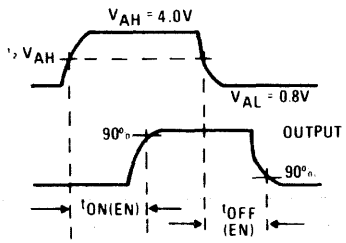
BREAK BEFORE MAKE DELAY (t_{OPEN})

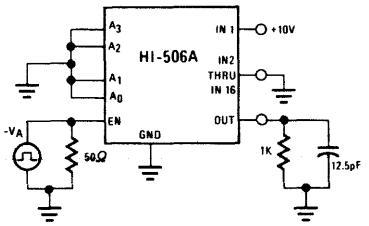


TEST CIRCUIT
NO.9

ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

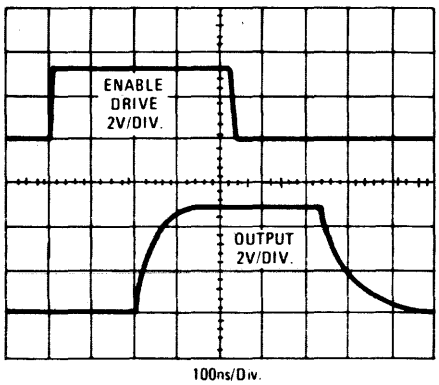
ENABLE DRIVE





SIMILAR CONNECTION FOR HI-507A

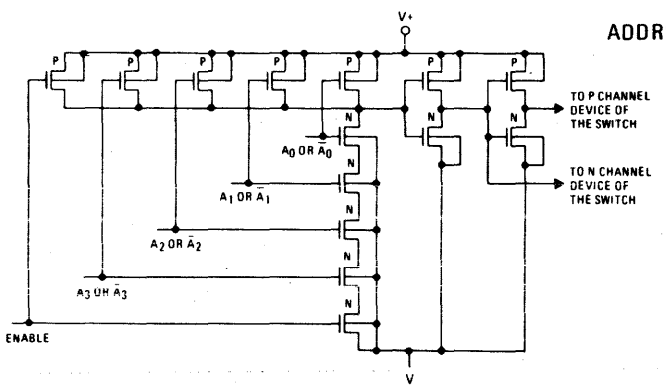
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



SCHEMATIC DIAGRAMS

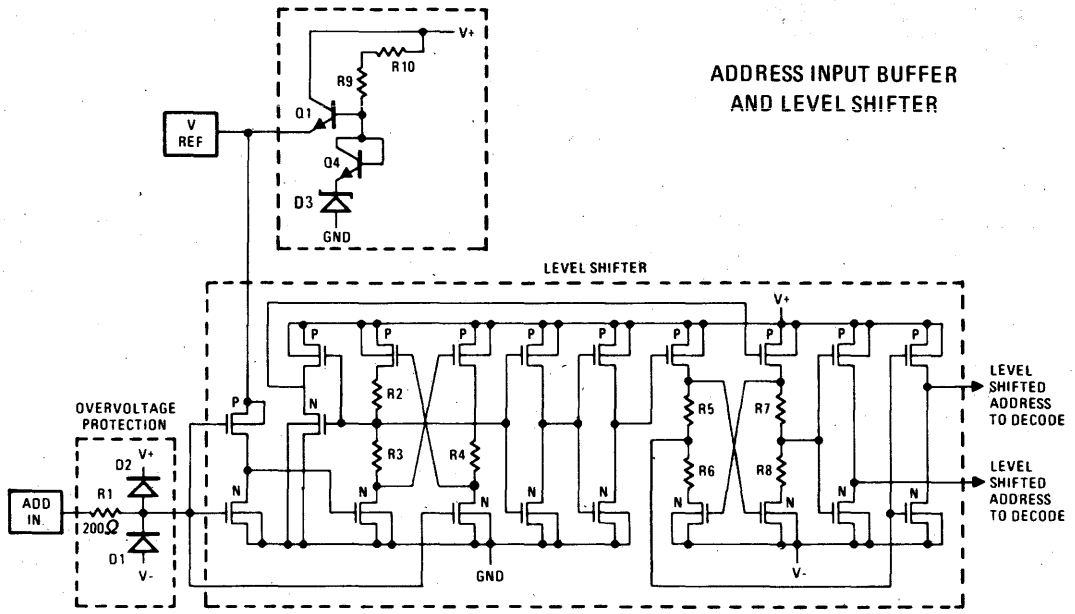
DELETE A_3 or $\overline{A}_3$
INPUT FOR HI-507A

ADDRESS DECODER

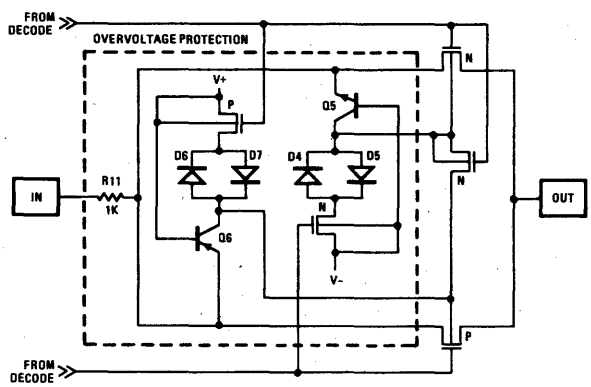


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ADDRESS INPUT BUFFER
AND LEVEL SHIFTER



MULTIPLEX SWITCH



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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-508A/509A

8 Channel CMOS Analog Multiplexers with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW

APPLICATIONS

- DATA ACQUISITION
- INDUSTRIAL CONTROLS
- TELEMETRY

DESCRIPTION

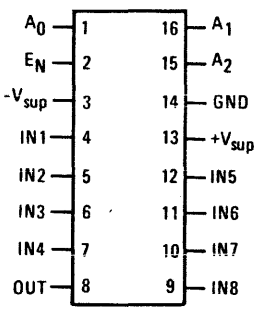
The HI-508A and HI-509A are dielectrically isolated CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage currents combine to produce low errors. Application Notes 520 and 521 further explain these features.

The HI-508A-2 and HI-509A-2 are specified over -55°C to +125°C while the -5 versions are specified over 0°C to +75°C.

PINOUT

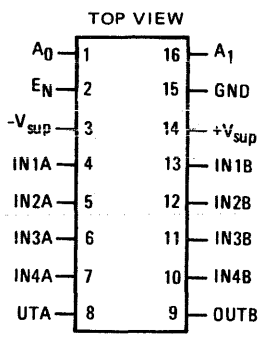
HI-508A — **Package Code 4B**

TOP VIEW



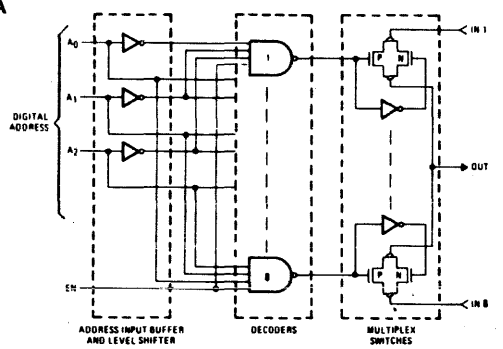
HI-509A — **Package Code 4B**

TOP VIEW

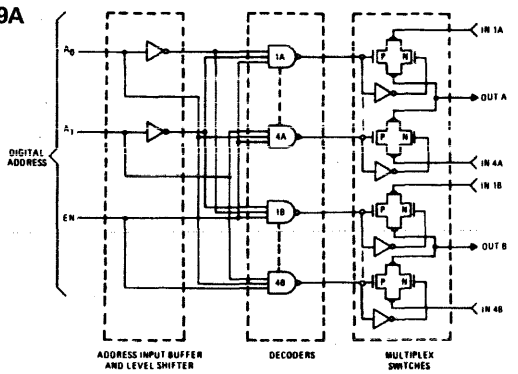


FUNCTIONAL DIAGRAM

HI-508A



HI-509A



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins 40V

V+ to Ground 20V

V_{EN}, V_A, Digital Input Overvoltage:

V_A { V_{Supply}(+) +4V; V_{Supply} (-) -4V

Analog Input Overvoltage:

V_S { V_{Supply} (+) +20V; V_{Supply} (-) -20V

Total Power Dissipation* 725 mW

Operating Temperature:

HI-508A/HI-509A-2 -55°C to +125°C

HI-508A/HI-509A-5 0°C to +75°C

Storage Temperature -65°C to +150°C

*Derate 8mW/°C above t_A = 75°C

ELECTRICAL CHARACTERISTICS (Unless Otherwise Specified)

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characterisitcs section.

PARAMETER	TEMP.	HI-508A/509A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-508A/509A-5 0°C to +75°C MIN.	TYP	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, On Resistance (Note 1)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	1.8		1.8	2.0	KΩ
*$I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
*$I_{D(OFF)}$, Off Output Leakage Current	+25°C		1.0			1.0		nA
HI-508A	Full			±250			±250	nA
*$I_{D(OFF)}$ with Input Overvoltage Applied (Note 2)	+25°C		4.0			4.0		nA
	Full			2.0				μA
*$I_{D(ON)}$, On Channel Leakage Current	+25°C		0.1			0.1		nA
HI-508A	Full			±250			±250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold (Note 6)	Full			0.8			0.8	V
V_{AH}, Input High Threshold (Note 6)	Full	4.0			4.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5	1.0		0.5		μs
t_{OPEN}, Break - Before Make Delay	+25°C		80			80		ns
$t_{ON(EN)}$, Enable Delay (ON)	+25°C		300			300		ns
$t_{OFF(EN)}$, Enable Delay (OFF)	+25°C		300			300		ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.0 25%)	+25°C		3.5			3.5		μs
"OFF Isolation" (Note 3)	+25°C		65			65		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		5			5		pF
$C_{D(OFF)}$, Channel Output Capacitance								
HI-508A	+25°C		25			25		pF
HI-509A	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current (Note 4)	Full		0.5	2.0		0.5	5.0	mA
*I-, Current (Note 4)	Full		0.02	1.0		0.02	2.0	mA
*I+, Standby (Note 5)	Full		0.5	2.0		0.5	5.0	mA
*I-, Standby (Note 5)	Full		0.02	1.0		0.02	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -100μA
2. Analog Overvoltage = ±33V
3. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3V RMS, f = 500KHz
4. V_{EN} = +4.0V
5. V_{EN} = 0.8V
6. To drive from DTL/TTL Circuits, 1KΩ pull-up resistors to +5.0V supply are recommended

*100% Tested for Dash 8. ("Full" Tested at +25°C to +125°C)

TRUTH TABLES

HI-508A

A_2	A_1	A_0	E_N	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

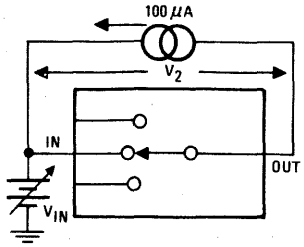
A_1	A_0	EN	ON SWITCH PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

UNLESS OTHERWISE SPECIFIED: $T_A = 25^oC$, $V_{SUPPLY} = +15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$

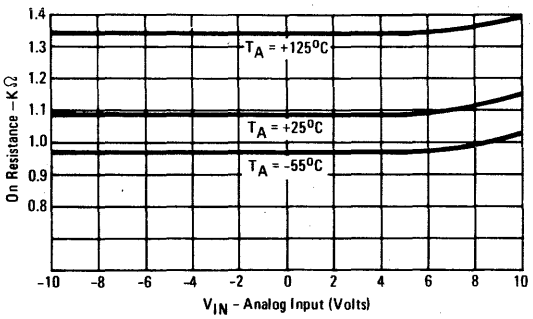
TEST CIRCUIT NO. 1

$R_{ON} = \frac{V_2}{100\mu A}$

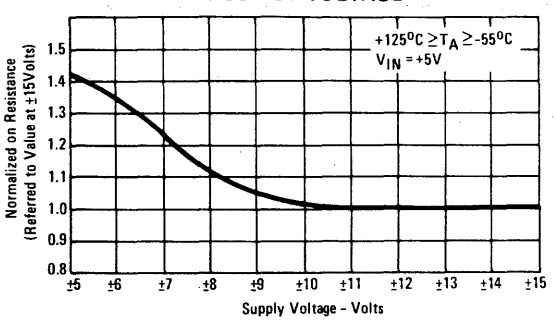


ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

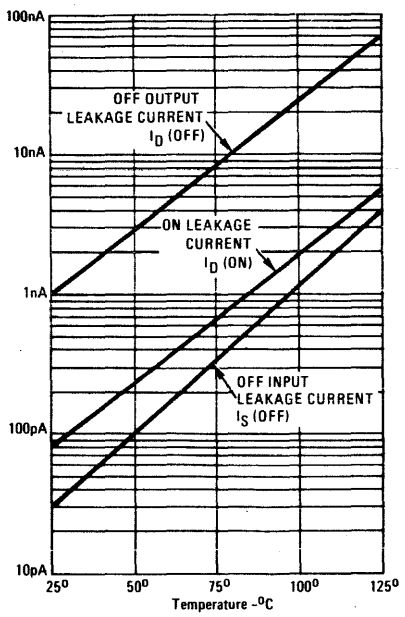
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE

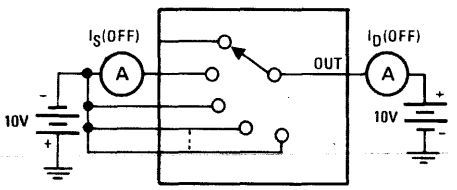


LEAKAGE CURRENT vs. TEMPERATURE



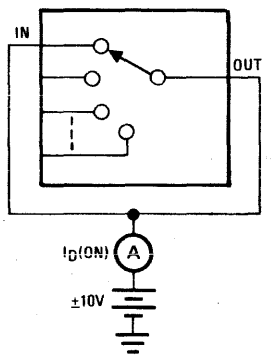
TEST CIRCUIT NO. 2

OFF LEAKAGE CURRENT vs. TEMPERATURE

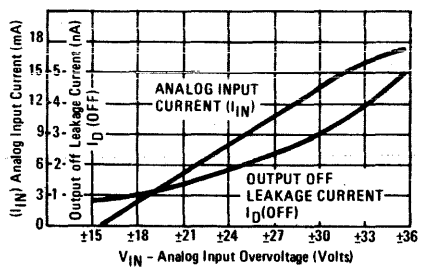


ON LEAKAGE CURRENT vs. TEMPERATURE

TEST CIRCUIT NO. 3

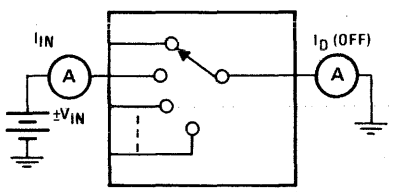


ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



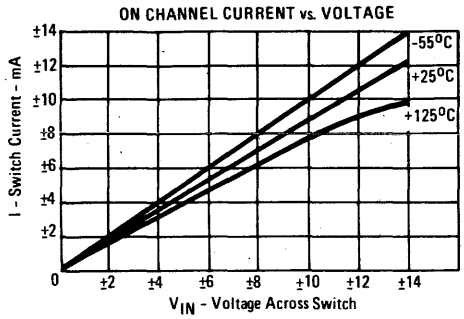
TEST CIRCUIT NO. 4

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

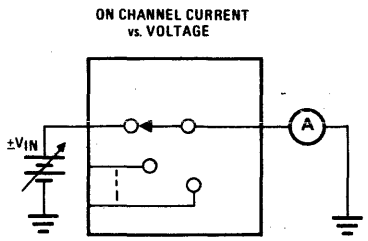


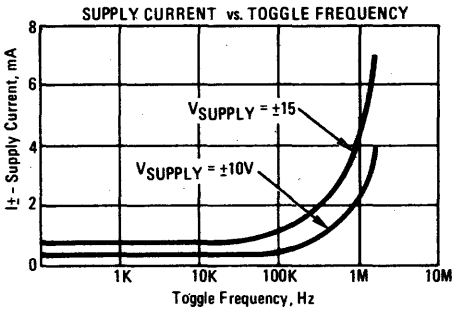
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PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

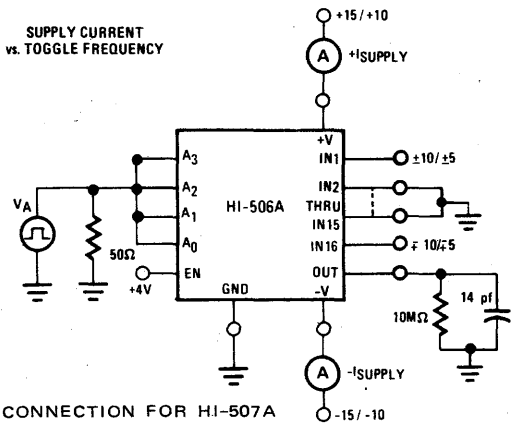


TEST CIRCUIT NO.5

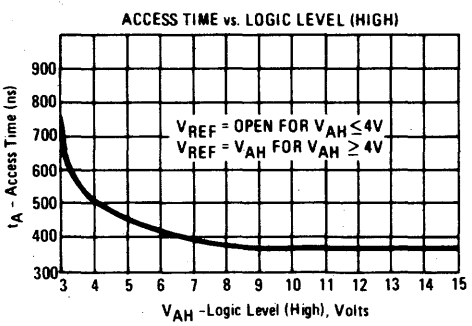




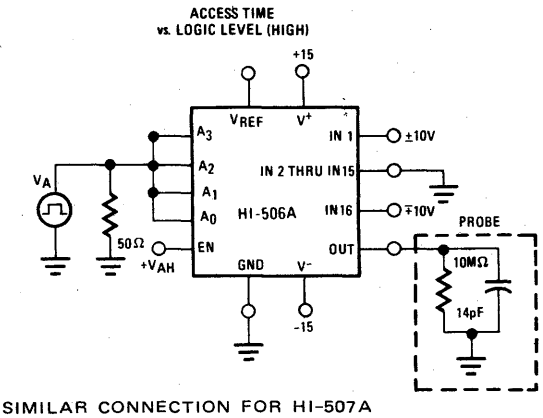
TEST CIRCUIT NO.6



SIMILAR CONNECTION FOR HI-507A

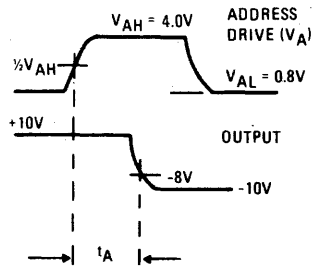


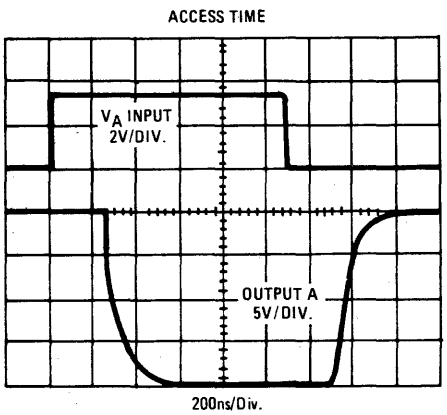
TEST CIRCUIT NO.7



SIMILAR CONNECTION FOR HI-507A

SWITCHING WAVEFORMS

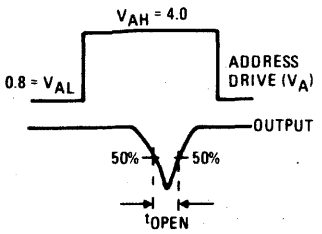


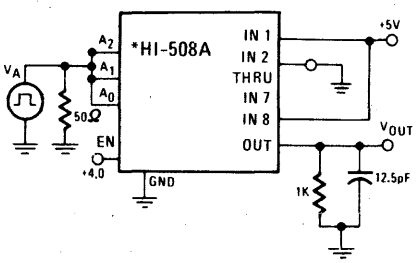


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SWITCHING WAVEFORMS (continued)

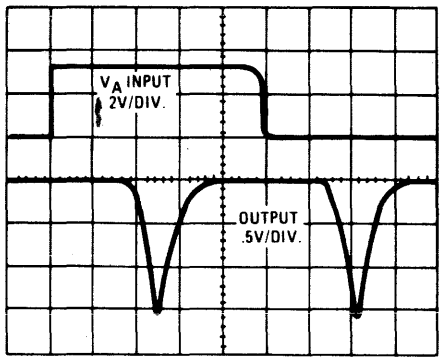
TEST CIRCUIT NO. 8 BREAK BEFORE MAKE DELAY (t_{OPEN})





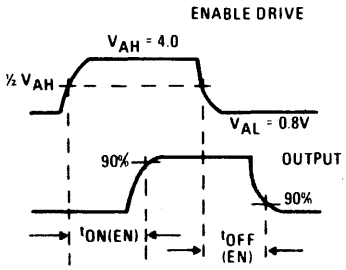
*SIMILAR CONNECTION FOR HI-509A

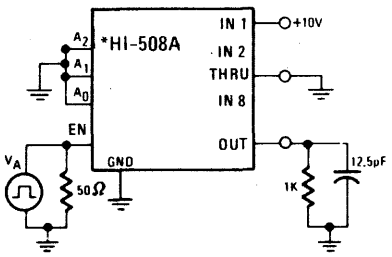
BREAK BEFORE MAKE DELAY (t_{OPEN})



100ns/Div.

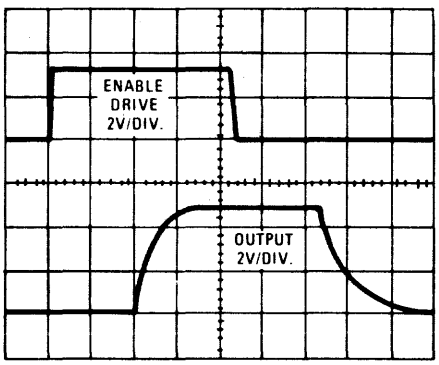
TEST CIRCUIT NO. 9 ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)





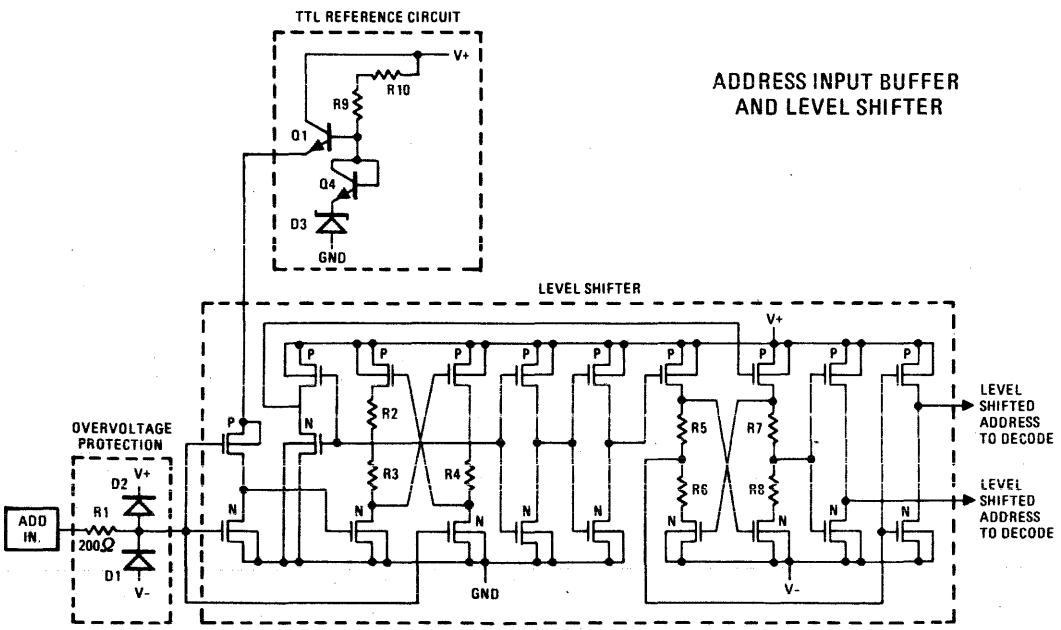
* SIMILAR CONNECTION FOR HI-509A

ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



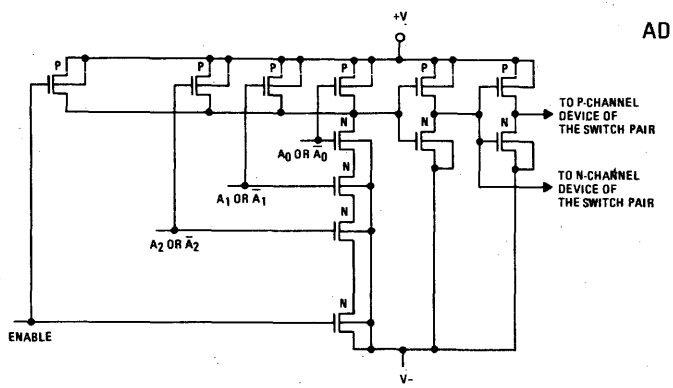
100ns/Div.

SCHEMATIC DIAGRAMS

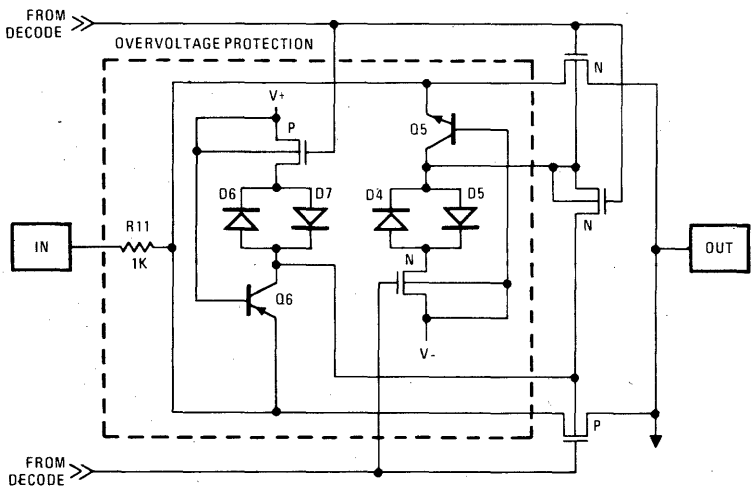


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ADDRESS DECODER



MULTIPLEX SWITCH



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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-1818A/1828A

Low Resistance 8 Channel CMOS Analog Multiplexers

FEATURES

- SIGNAL RANGE ±15V
- "ON" RESISTANCE (TYP.) 250Ω
- INPUT LEAKAGE AT +125°C (TYP.) 20nA
- ACCESS TIME (TYP.) 350ns
- POWER CONSUMPTION (TYP.) 5mW
- DTL/TTL COMPATIBLE ADDRESS
- -55°C to +125°C OPERATION

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- DEMULTIPLEXING
- SELECTOR SWITCH

DESCRIPTION

The HI-1818A/1828A are monolithic high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit (enable) input for disabling all channels. Dielectric Isolation (DI) processing is used for enhanced reliability and performance (see Application Note 521). Substrate leakage and parasitic capacitance are much lower, resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.1nA) and low channel ON resistance (250 Ω) assure optimum performance in low level or current mode applications.

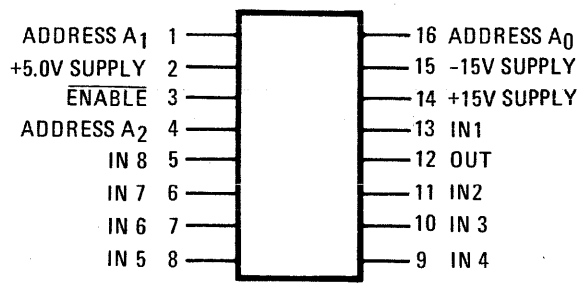
The 1818A is a single-ended 8 channel multiplexer, while the HI-1828A is a differential 8 channel version. Either device is ideally suited for medical instrumentation, telemetry systems, and microprocessor based data acquisition systems.

The HI-1818A-2 and HI-1828A are specified over -55°C to +125°C, while the -5 versions are specified over 0°C to +75°C.

PINOUT

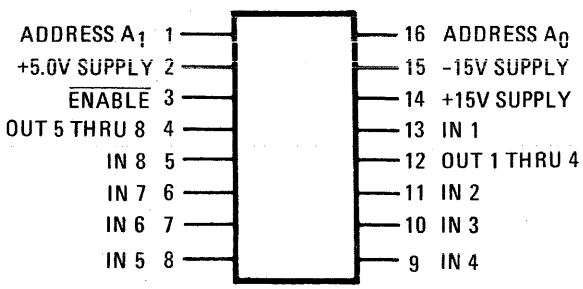
HI-1818A

Top View — Package Code 4B



HI-1828A

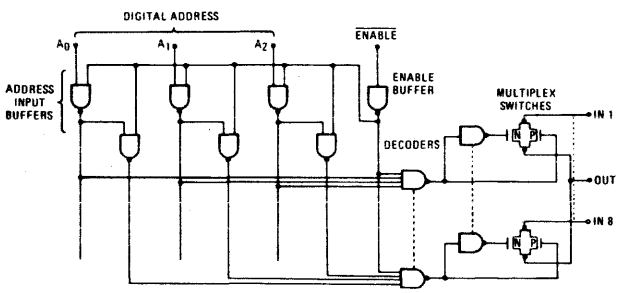
Top View — Package Code 4B



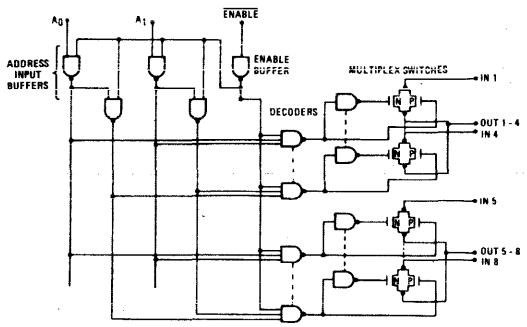
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

FUNCTIONAL DIAGRAM

HI-1818A



HI-1828A



SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage Between Pins 14 and 15	40.0V	Digital Input Voltage	V-Supply to V+ Supply
Logic Supply Voltage, Pin 2	30.0V	Total Power Dissipation (Note 2)	780mW
Analog Input Voltage: V^+_{Supply} +2V		Storage Temperature Range	-65°C to +150°C
V^-_{Supply} -2V			

ELECTRICAL CHARACTERISTICS

Supplies = +15V, -15V, +5V

PARAMETER	TEMP.	HI-1818A-2/1828A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-1818A-5/1828A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_{IN}, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, ON Resistance (Note 3)	+25°C		250	400		250	400	Ω
	Full		300	500		300	500	Ω
*I_S(OFF), Input Leakage Current	Full		20	50		20	50	nA
*I_D(ON), On Channel Leakage Current								
(HI-1818A)	Full		100	250		100	250	nA
(HI-1828A)	Full		50	125		50	125	nA
*I_D(OFF) Output Leakage Current								
(HI-1818A)	Full		100	250		100	250	nA
(HI-1828A)	Full		50	125		50	125	nA
DIGITAL INPUT CHARACTERISTICS								
V_{IL}, Input Low Threshold	Full			0.4			0.4	V
V_{IH}, Input High Threshold (Note 4)	Full	4.0			4.0			V
*I_{IN}, Input Leakage Current	Full		.01	1		.01	1	μA
SWITCHING CHARACTERISTICS								
T_S, Access Time (Note 5)	+25°C		350			350		ns
Break-Before-Make Delay	+25°C		100			100		ns
Settling Time (0.1%)	+25°C		1.08			1.08		μs
(0.025%)	+25°C		2.8			2.8		μs
C_{IN}, Channel Input Capacitance	+25°C		4			4		pF
C_{OUT}, Channel Output Capacitance								
(HI-1818A)	+25°C		20			20		pF
(HI-1828A)	+25°C		10			10		pF
C_{DS}(OFF), Drain-To-Source Capacitance	+25°C		0.6			0.6		pF
C_D, Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		5			5		mW
P_{DS}, Standby Power (Note 6)	Full		5			5		mW
*I_+, Current Pin 14	Full		0.1	0.5		0.1	1	mA
*I_-, Current Pin 15	Full		0.3	1		0.3	2	mA
*I_L, Current Pin 2	Full		0.3	1		0.3	2	mA

NOTES:
1. Voltage ratings apply when voltages at all other pins are within their normal operating ranges.
2. Derate 9.25 mW/°C above 75°C.
3. V_{OUT} = ±10V I_{OUT} = - 1mA.
4. To drive from DTL/TTL circuits, 1K pull-up resistors to + 5.0V supply are recommended.
5. Time measured to 90% of final output level; V_{OUT} = - 5.0V to +5.0V, Digital Inputs = 0V to + 4.0V.
6. Voltage at Pin 3, $\overline{ENABLE}$ = + 4.0V.

*100% Tested for Dash 8. ("Full" Tested at +25°C to +125°C)

TRUTH TABLES

HI-1818A

ADDRESS A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	H	NONE

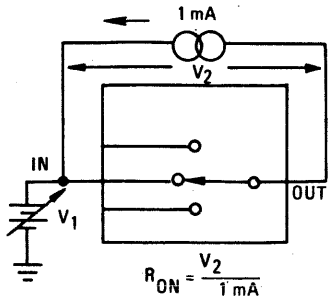
HI-1828A

ADDRESS A_1	A_0	$\overline{EN}$	"ON" CHANNELS
L	L	L	1 and 5
L	H	L	2 and 6
H	L	L	3 and 7
H	H	L	4 and 8
X	X	H	NONE

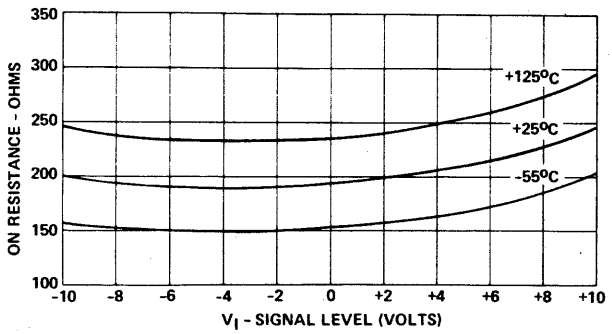
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PERFORMANCE CHARACTERISTICS

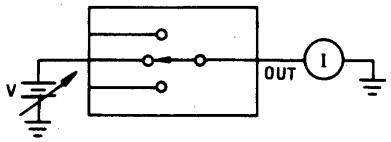
ON RESISTANCE vs ANALOG SIGNAL LEVEL



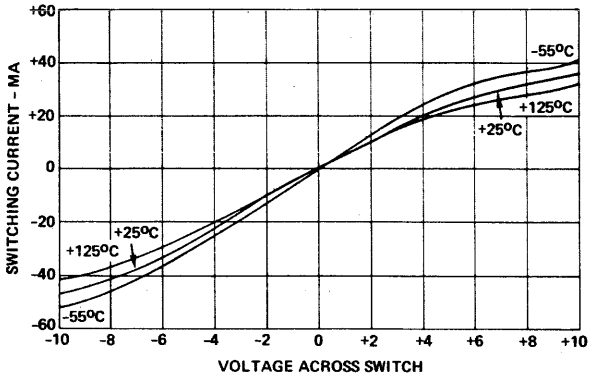
Test Circuit



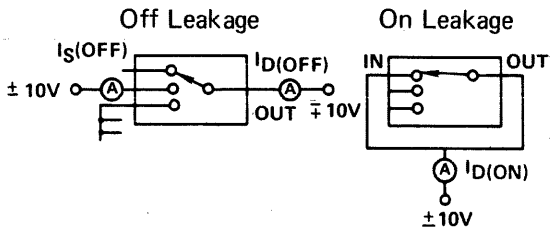
ON CHANNEL CURRENT vs VOLTAGE

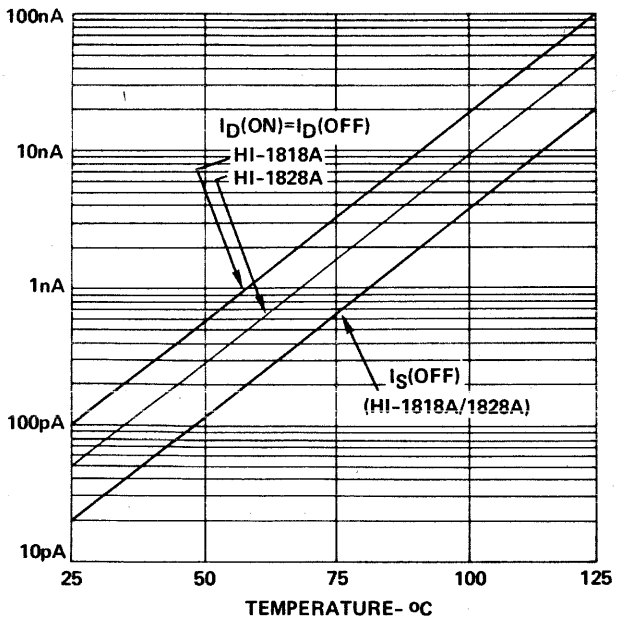


Test Circuit

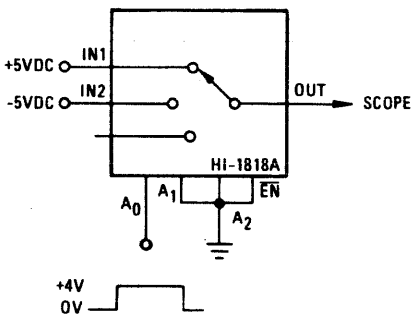


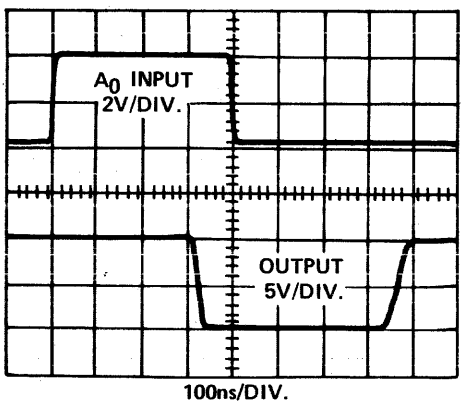
ON/OFF LEAKAGE CURRENTS vs TEMPERATURE





ACCESS TIME

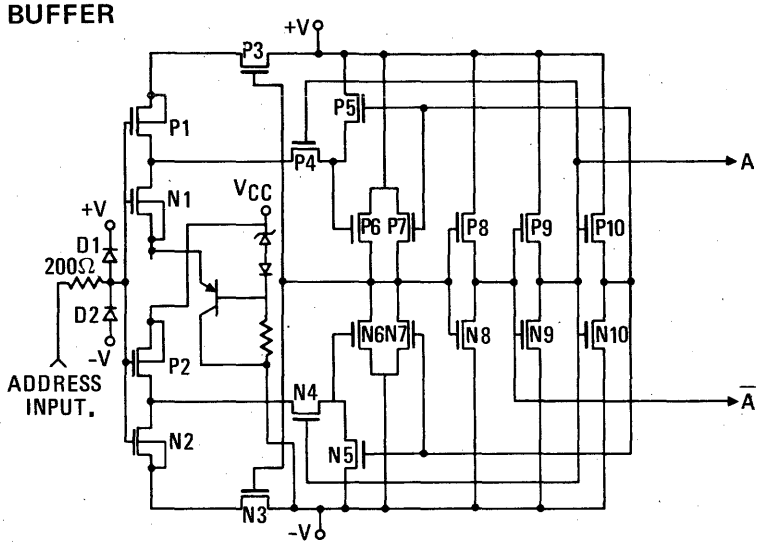




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SCHEMATIC DIAGRAM

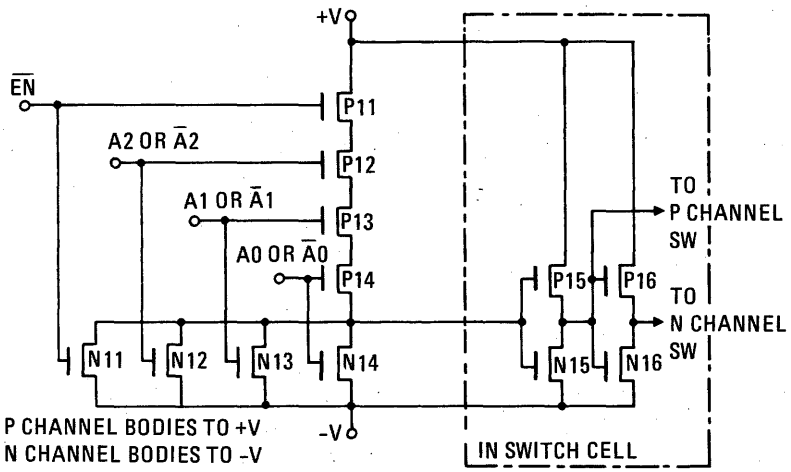
ADDRESS INPUT BUFFER



ALL N-CHANNEL BODIES TO V-

ALL P-CHANNEL BODIES TO V+ UNLESS OTHERWISE INDICATED.

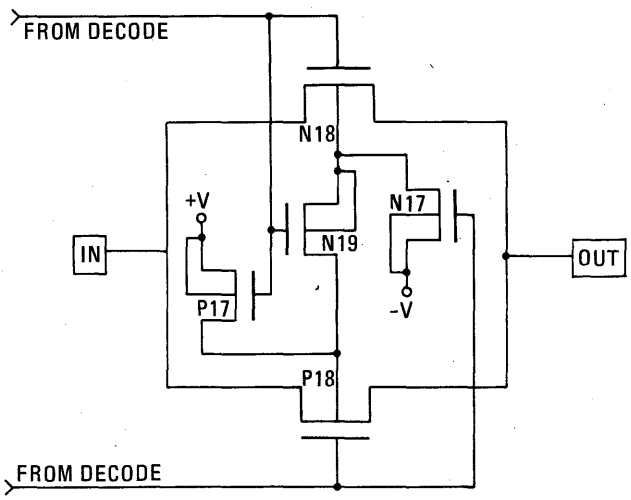
DECODER GATE



P CHANNEL BODIES TO +V
N CHANNEL BODIES TO -V

A2 OR Ā2 NOT USED FOR HI-1828A

MULTIPLEX SWITCH



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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-1840

16 Channel CMOS Analog Multiplexer with High-Z Analog Input Protection

FEATURES

- HIGH ANALOG INPUT IMPEDANCE DURING POWER LOSS (OPEN) 500MΩ
- LOW POWER CONSUMPTION (STANDBY) 600μW
- ACCESS TIME 500ns
- EXCELLENT IN HI-REL REDUNDANT SYSTEMS
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP

APPLICATIONS

- FAIL-SAFE DATA ACQUISITION SYSTEMS
- FAIL-SAFE TELEMETRY SYSTEMS
- AIRCRAFT INSTRUMENTATION AND CONTROL

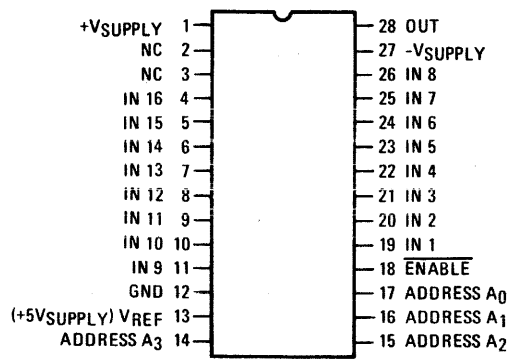
DESCRIPTION

The HI-1840 is a monolithic 16 channel multiplexer constructed with the Harris Linear Dielectric Isolation CMOS process. It is designed to provide a high input impedance to the analog source if device power fails (open) or the analog signal voltage inadvertently exceeds the supply rails during powered operation. Excellent for use in redundant applications, since the secondary device can be operated in a standby unpowered mode affording no additional power drain. But more significantly, a very high impedance exists between the active and inactive devices preventing any interaction. One of sixteen channel selection is controlled by a 4-bit binary address plus an Enable-Inhibit input which conveniently controls the ON/OFF operation of several multiplexers in a system. All digital inputs have electrostatic discharge protection. The HI-1840 is tested and guaranteed within the military temperature range and is available in a 28 pin dual-in-line package.

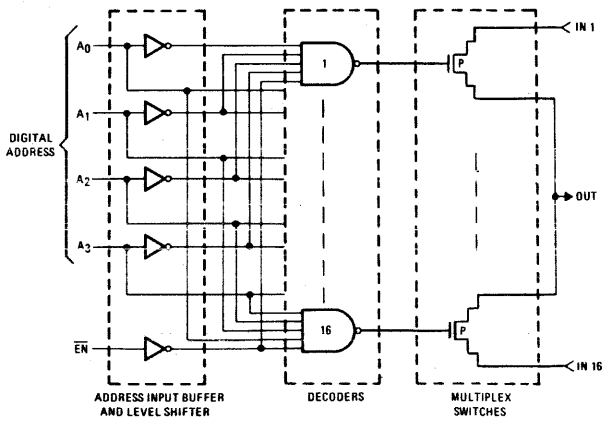
PINOUT

Package Code 1M

Top View



FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27 +40V
V_{REF} to Ground +20V
V_{EN}, V_A, Digital Input Overvoltage:
V_A V_{Supply} (+) +4V
V_{Supply} (-) -4V
Analog Input Overvoltage:
V_S V_{Supply} (+) +10V
V_{Supply} (-) -10V

Total Power Dissipation* 1200mW
Operating Temperature:
HI-1840-2 -55°C to +125°C
Storage Temperature -65°C to +150°C

*Derate 8mW/°C above T_A = +25°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified:
Supplies = +15V, -15V: V_{REF}(Pin 13) = +5V; V_{AH}(Logic Level High) = 4.0V; V_{AL}(Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics section.

PARAMETER	TEMP.	-55°C to +125°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS					
*V_S, Analog Signal Range	Full	-5		+15	V
*R_{ON}, On Resistance (Note 1) V_{IN} = +15V	Full		0.5	1.0	KΩ
V_{IN} = -5V	Full		2.5	5.0	KΩ
*I_S(OFF), Off Input Leakage Current	+25°C		0.03		nA
	Full			±100	nA
*I_S(OFF), with Power Off (Note 8)	Full			±100	nA
*I_D(OFF), Off Output Leakage Current	+25°C		1.0		nA
	Full			±1000	nA
* I_D(OFF), or I_S(OFF) with Input Overvoltage Applied (Note 2)	+25°C		50		nA
	Full			±1000	nA
*I_D(ON), On Channel Leakage Current	+25°C		1.0		nA
	Full			±1000	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold | TTL Drive	Full			0.8	V
V_{AH}, Input High Threshold | (Note 7)	Full	4.0			V
V_{AL} | MOS Drive (Note 3)	+25°C			0.8	V
V_{AH} |	+25°C	6.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0	μA
SWITCHING CHARACTERISTICS					
t_A, Access Time	+25°C		500	1000	ns
t_{OPEN}, Break-Before-Make Delay	+25°C	20	80		ns
t_{ON}(EN), Enable Delay (ON)	+25°C		300	1000	ns
t_{OFF}(EN), Enable Delay (OFF)	+25°C		300	1000	ns
Settling Time (0.1%)	+25°C		1.2		μs
(0.025%)	+25°C		4.1		μs
"Off Isolation" (Note 4)	+25°C		65		dB
C_S(OFF), Channel Input Capacitance	+25°C		5		pF
C_D(OFF), Channel Output Capacitance :	+25°C		50		pF
C_A, Digital Input Capacitance	+25°C		5		pF
C_{DS}(OFF), Input ot Output Capacitance	+25°C		0.15		pF
POWER REQUIREMENTS					
P_D, Power Dissipation (Note 5)	+25°C		0.6	15.0	mW
(Note 6)	+25°C		0.6	15.0	mW
*I+, Current Pin 1 (Note 5)	Full		0.02	0.5	mA
*I-, Current Pin 27 (Note 5)	Full		0.02	0.5	mA
*I+, Standby (Note 6)	Full		0.02	0.5	mA
*I-, Standby (Note 6)	Full		0.02	0.5	mA

TRUTH TABLE

A_3	A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
X	X	X	X	H	NONE
L	L	L	L	L	1
L	L	L	H	L	2
L	L	H	L	L	3
L	L	H	H	L	4
L	H	L	L	L	5
L	H	L	H	L	6
L	H	H	L	L	7
L	H	H	H	L	8
H	L	L	L	L	9
H	L	L	H	L	10
H	L	H	L	L	11
H	L	H	H	L	12
H	H	L	L	L	13
H	H	L	H	L	14
H	H	H	L	L	15
H	H	H	H	L	16

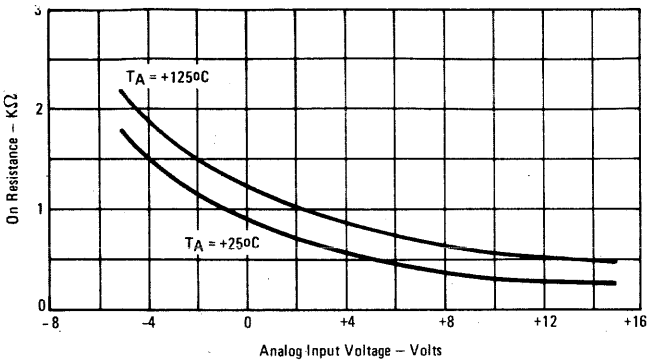
NOTES:
1. I_{OUT} = 1mA
2. Analog Overvoltage = ±20V
3. V_{REF} = +10V
4. V_{EN} = 4.0V, R_L = 1K, C_L = 7pF, V_S = 3VRMS, f = 500kHz
5. V_{EN} = 0.8V
6. V_{EN} = 4.0V
7. To drive from DTL/TTL circuits 1K pull-up resistors to +5.0V supply are recommended.
8. All supplies (V+, V-, +5V) and digital inputs (A_0, A_1, A_2, A_3, EN) opened. Analog input ±10V.

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PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

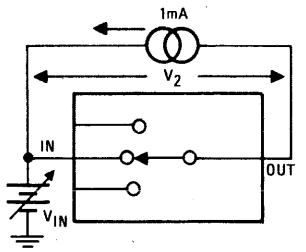
Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$ and $V_{REF} = 5V$.

ON RESISTANCE VS. ANALOG INPUT VOLTAGE

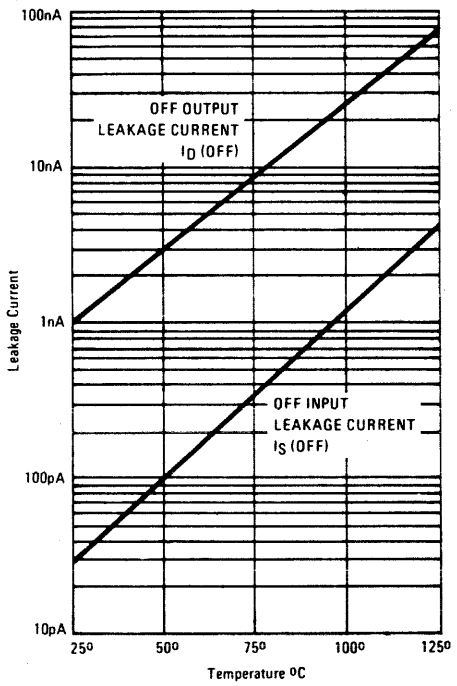


ON RESISTANCE vs. INPUT SIGNAL LEVEL

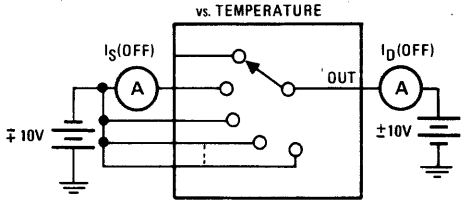
$R_{ON} = \frac{V_2}{1mA}$



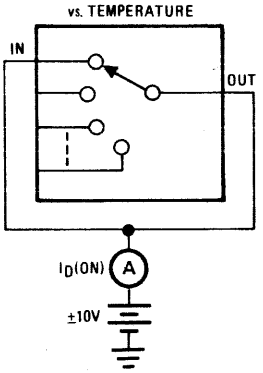
LEAKAGE CURRENT VS. TEMPERATURE



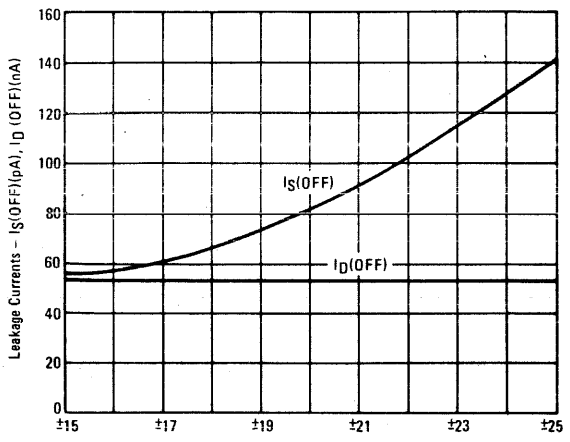
OFF LEAKAGE CURRENT vs. TEMPERATURE



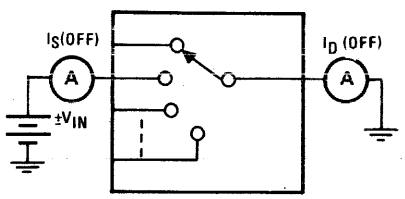
ON LEAKAGE CURRENT vs. TEMPERATURE



ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

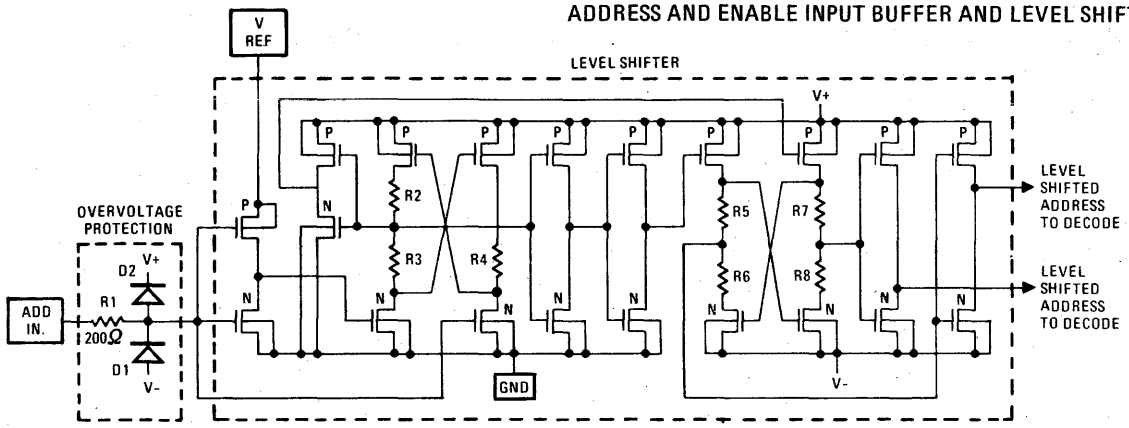


ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

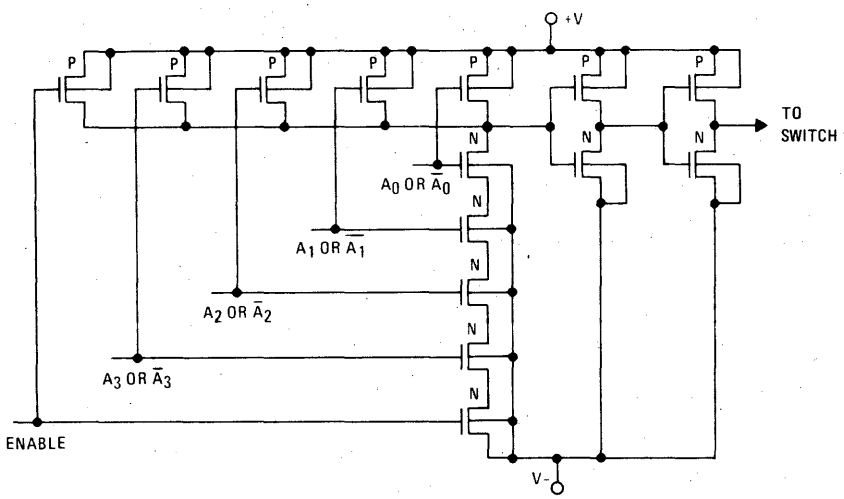


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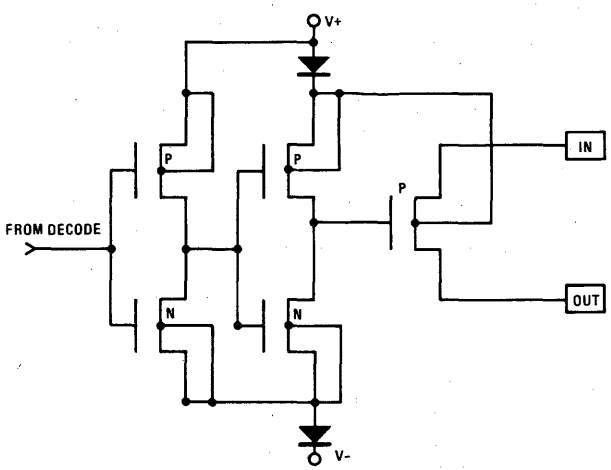
ADDRESS AND ENABLE INPUT BUFFER AND LEVEL SHIFTER



ADDRESS DECODER



MULTIPLEX SWITCH



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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

PRELIMINARY HI-562

12 Bit High Speed Monolithic Digital-to-Analog Converter

FEATURES

- MONOLITHIC CONSTRUCTION
- EXTREMELY FAST SETTLING — 200ns TO 0.01% (TYP.)
- LOW GAIN DRIFT — ±2ppm/°C (MAX.)
- EXCELLENT LINEARITY OVER TEMPERATURE — ±1/2 LSB (MAX.)
- DESIGNED FOR MINIMUM GLITCHES
- MONOTONIC OVER TEMPERATURE

APPLICATIONS

- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIZERS
- HIGH SPEED DATA ACQUISITION
- HIGH-REL APPLICATIONS
- PRECISION INSTRUMENTS

DESCRIPTION

The Harris HI-562 is the first monolithic digital-to-analog converter to combine both ultra-high speed performance and true 12-bit accuracy on the same chip. The HI-562's fast output current settling of 200ns to 0.01% is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-562 by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-ON and turn-OFF switching times. This creates within the chip a very uniform and constant thermal distribution for excellent linearity and also completely eliminates thermal transients during switching. High stability thin film resistor processing together with laser trimming provide the HI-562 with guaranteed true 12-bit linearity to within ±1/2 LSB maximum over the -55°C to +125°C temperature range. Beyond that, the HI-562's low offset and gain drift over this temperature range assure that its absolute accuracy when referred to a fixed 10V reference will not deviate more than ±3/2 LSB for unipolar mode operation (±2 LSB for bipolar operation). The input reference can be varied from +2V to +10V for two quadrant multiplying mode operation.

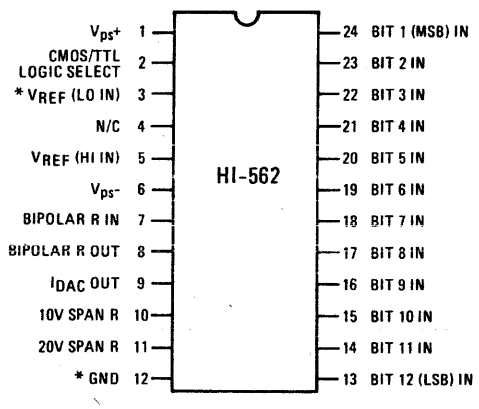
The HI-562 is recommended as a replacement for higher cost hybrid and modular units for increased reliability and accuracy in applications such as CRT displays, precision instruments and data acquisition systems requiring throughput rates as high as 5MHz for full range transitions. Its small size makes it an ideal choice as the heart of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-562 is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-562-5 is specified for operation over 0°C to +70°C, the HI-562-4 over -25°C to +85°C and the HI-562-2 and HI-562-8 over -55°C to +125°C. Processing to MIL-STD-883A Class B screening is available by selecting the HI-562-8. All are available in a hermetically sealed 24-lead dual-in-line package.

PINOUT

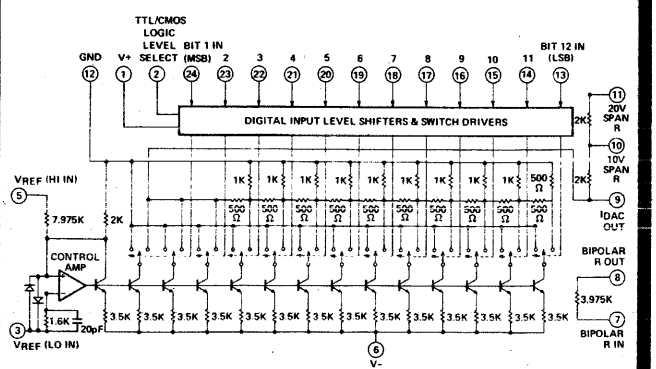
Package Code 1H

TOP VIEW



* Pins 3 and 12 connected to top and bottom case for high frequency shielding.

FUNCTIONAL DIAGRAM



SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground)[1]

Power Supply Inputs	$V_{PS}+$	+20V
	$V_{PS}-$	-20V
Reference Inputs	VREF (Hi)	$\pm V_{PS}$
	VREF (Lo)	0V
Digital Inputs	Bits 1-12	-1V, +12V
	CMOS/TTL Logic Select	-1V, +12V
Outputs	Pins 7, 8, 10, 11	$\pm V_{PS}$
	Pin 9	$+V_{PS}$, -5V

Power Dissipation P_d, Package	1000mW
Operating Temperature Range	
HI-562-2	-55°C to +125°C
HI-562-4	-25°C to +85°C
HI-562-5	0°C to +70°C
HI-562-8	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@ +25°C, $V_{PS}+$, = +5V, $V_{PS}-$ = -15V, V_{REF} = +10V, pin 2 open circuit unless otherwise noted)

PARAMETER	CONDITIONS	HI-562-2/HI-562-8 MIN	HI-562-2/HI-562-8 TYP	HI-562-2/HI-562-8 MAX	HI-562-4/HI-562-5 MIN	HI-562-4/HI-562-5 TYP	HI-562-4/HI-562-5 MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (3)	Bit ON "Logic 1" Bit OFF "Logic 0"							
TTL Input Voltage (2) Logic "1"	Over full temp. range	2.0			2.0			V
TTL Logic "0"				0.8			0.8	V
TTL Input Current (2) Logic "1"			20	100		20	100	nA
TTL Logic "0"			-50	-100		-50	-100	μA
CMOS Input Voltage Logic "1"	Pin 1 tied to pin 2, +4.75V ≤ $V_{PS}+$ ≤ +12V over full temp. range	$0.7V_{PS}+$			$0.7V_{PS}+$			V
CMOS Logic "0"				$0.3V_{PS}+$			$0.3V_{PS}+$	V
CMOS Input Current Logic "1"			20	100		20	100	nA
CMOS Logic "0"			-50	-100		-50	-100	μA
Reference Input								
Input Resistance	I_{OUT} = 5mA (±20%)		8K			8K		Ω
Input Voltage			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Over full temp. range			12			12	Bits
Nonlinearity (3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over full temp. range			±1/2			±1	
Differential Nonlinearity (3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over full temp. range			MONOTONICITY GUARANTEED				
Relative Accuracy (6)	With 24.9Ω(1%) Trim Resistors							
Gain Error	All Bits ON			±0.024			±0.024	% FSR (4)
Bipolar Offset Error	All Bits OFF			±0.024			±0.024	
Unipolar Offset Error				±0.012			±0.012	
Adjustment Range	See Operating Instructions							
Gain	With 50Ω Trim		±0.3			±0.3		% FSR
Bipolar Offset	Potentiometers		±0.6			±0.6		
Temperature Stability	Drift specified with internal span resistors for voltage output							
Gain Drift (3)	Over full			±2			±3	ppm of FSR/°C
Offset Drift (3)	temp. range							
Unipolar Offset	All Bits OFF			±0.4			±1	
Bipolar Offset				±1			±3	
Differential Nonlinearity	Over full temp. range		±1	±2		±2	±3	
Settling Time (3) to ±1/2 LSB	All Bits ON-to-OFF or OFF-to-ON		200	400		200	400	ns

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PARAMETER	CONDITIONS	HI-562-2/HI-562-8			HI-562-4/HI-562-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Major Carry Transient Peak Amplitude Settling Time to 90% Complete	From 011...1 to 100...0 or 100...0 to 011...1		0.7 35			0.7 35		mA ns
Power Supply Sensitivity (3) Unipolar Offset V_{ps}+ @ +5V or +15V V_{ps}- @ -15V Bipolar Offset V_{ps}+ @ 5V or +15V V_{ps}- @ -15V Gain V_{ps}+ @ +5V or +15V V_{ps}- @ -15V	All Bits OFF All Bits OFF, Bipolar mode All Bits ON		 ±0.5 ±0.5 ±1.5 ±1.5	 ±1 ±2		 ±0.5 ±0.5 ±1.5 ±1.5	 ±1 ±2	ppm of FSR/% V_{ps}

OUTPUT CHARACTERISTICS

Output Current Unipolar Bipolar			 -5.0 ±2.5			 -5.0 ±2.5		mA
Resistance			1000			1000		ohms
Capacitance			20			20		pF
Output Voltage Ranges Unipolar Bipolar	Using external op amp and internal scaling resistors. See Figure 1 and Table 1 for connections		0 to +5 0 to +10 ±2.5 ±5 ±10			0 to +5 0 to +10 ±2.5 ±5 ±10		V
Compliance Limit (3)		-3		+10	-3		+10	V
Compliance Voltage (3)	Over full temp. range		±1.0			±1.0		V
Output Noise	0.1 to 10Hz (All Bits ON) 0.1 to 5MHz (All Bits ON)		30 100			30 100		µV (p-p)

MULTIPLYING MODE PERFORMANCE

Quadrants	Bipolar Mode Reference Input; 2V to +10V		2			2		
Reference Voltage Feedthrough	Unipolar mode, all Bits OFF and +2V to +10V (p-p), 2kHz Sinewave		1			1		LSB (p-p)
Relative Accuracy	Reference Input @ $2V_{DC}$		±0.05			±0.05		% FSR
Output Slew Rate	All Bits ON and +2 to +10V Step change at reference input.		6			6		mA/µs
Settling Time to ±1/2 LSB			3			3		µs
Control Amplifier Bandwidth	Small signal		10			10		MHz

POWER REQUIREMENTS

V_{ps}+ (7) V_{ps}-	Over full temp. range	4.5 13.5	5 15	15 16.5	4.75 13.5	5 15	15 16.5	V
I_{ps}+ (5) I_{ps}- (5)	All Bits ON or OFF in either TTL or CMOS mode		9 28			9 28		mA
I_{ps}+ (5) I_{ps}- (5)	Same as above except over full temp. range		11 33			11 33		mA

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NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{ps}+ tolerance is ±10% for HI-562-2, -8. and ±5% for HI-562-4, -5.
3. See Definitions.
4. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc.; or 5mA(±20%) for current output.
5. After 30 seconds warm-up.
6. Using an external op amp with internal span resistors and specified external trim resistors in place of potentiometers R_1 and R_2. Errors are adjustable to zero using R_1 and R_2 potentiometers. (See Operating Instructions Figure 2.)
7. Maximum V_{ps}+ is +12V for high level logic only, i.e. when pin 1 is tied to pin 2.

DEFINITIONS OF SPECIFICATIONS

DIGITAL INPUTS

The HI-562 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement, or Offset Binary, (See Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement*
MSB LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	½FS	Zero	-FS
111...111	+FS – 1 LSB	+FS – 1 LSB	½FS – 1 LSB
011...111	½FS – 1 LSB	Zero – 1 LSB	+FS – 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

ACCURACY

NONLINEARITY – Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY – For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonictiy; i.e., the output always increases and never decreases for an increasing input.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, +5V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a large transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches to zero output. Matched switching times and fast switching will reduce glitches considerably.

DECOUPLING AND GROUNDING

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-562 (preferrably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

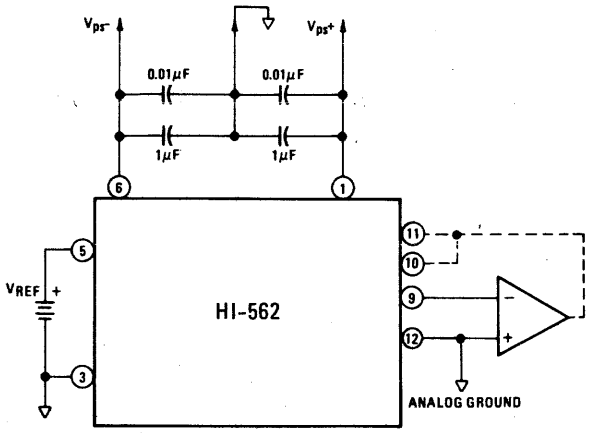
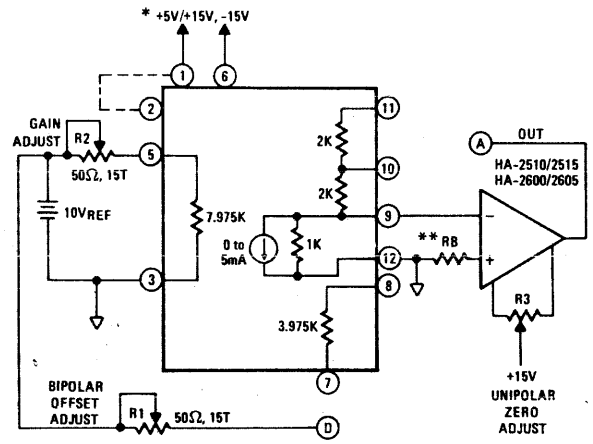


Figure 1

UNIPOLAR AND BIPOLAR VOLTAGE OUTPUT CONNECTIONS

CONNECTIONS – Using an external resistive load, the output compliance should not exceed ±1V to maintain specified accuracy. For higher output voltages, accuracy can be maintained by using an external op amp and the internal span resistors as shown in Figure 2 and defined in Table 1 for unipolar and bipolar modes.



* For TTL and DTL compatibility, connect +5V to pin 1 and leave pin 2 open. For CMOS compatibility, connect digital power supply (+4.85V ≤ VDD ≤ +12V) to pin 1 and short pin 2 to pin 1.

** Bias resistor, RB, should be chosen to equalize op amp offset voltage due to bias current. Its value is calculated from the parallel combination of the current source output resistance (1K) and the op amp feedback resistor. See Table 1 for values of RB.

Figure 2

Table 1

	OUTPUT RANGE	CONNECTIONS Pin 7 to	Pin 8 to	Pin 10 to	Pin 11 to	BIAS (R_B) RESISTOR
Unipolar Mode	0 to +10V	N.C.	N.C.	A	N.C.	667Ω
	0 to +5V	N.C.	N.C.	A	9	500Ω
Bipolar Mode	±10V	D	9	N.C.	A	667Ω
	±5V	D	9	A	N.C.	580Ω
	±2.5V	D	9	A	9	444Ω

EXTERNAL GAIN AND ZERO CALIBRATION (See Figure 2)

The input reference resistor (7.975K) and bipolar offset resistors shown in Figure 2 are both intentionally set low by 25Ω to allow the user to externally trim-out initial errors to a very high degree of precision. The adjustments are made in the voltage output mode using an external op amp as current-to-voltage converter and the HI-562 internal scaling resistors as feedback elements for optimum accuracy and temperature coefficient. For best accuracy over temperature, select an op amp that has good front-end temperature coefficients such as the HA-2600/2605 with offset voltage and offset current tempco's of 5μV/°C and 1nA/°C, respectively. For high speed voltage mode applications where fast settling is required, the HA-2510/2515 is recommended for better than 1.5μs settling to 0.01%. Using either one, potentiometer R_3 conveniently nulls unipolar offset plus op amp offset in one operation (for HA-2510/2515 and HA-2600/2605 use R_3 = 20K and 100K, respectively). For bipolar mode operation, R_3 should be used to null op amp offset to optimize its tempco (i.e., short 9 to A and adjust R_3 for zero before calibrating in bipolar mode). The gain and bipolar offset adjustment range using 50Ω potentiometers is ±12 LSB and ±25 LSB respectively. If desired, the potentiometers can be replaced with fixed 24.9Ω (1%) resistors resulting in an initial gain and bipolar offset accuracy of typically ±1/2 LSB.

UNIPOLAR CALIBRATION

Step 1: Unipolar Offset
- Turn all bits OFF
- Adjust R3 for zero volts output

Step 2: Gain
- Turn all bits ON
- Adjust R2 for an output of FS -1 LSB
  That is, adjust for:
  9.9976V for 0V to +10V range
  4.9988V for 0V to +5V range

BIPOLAR CALIBRATION

Step 1: Bipolar Offset
- Turn all bits OFF
- Adjust R1 for an output of:
  -10V for ±10V range
  -5V for ±5V range
  -2.5V for ±2.5V range

Step 2: Gain
- Turn bit 1 (MSB) ON; all other bits OFF
- Adjust R2 for zero volts output

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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-1080/1085

Precision Monolithic 8-Bit D to A Converter

FEATURES

- GUARANTEED ±1 L.S.B. ACCURACY OVER TEMPERATURE
  - HI-1080 -55°C to +125°C
  - HI-1085 0°C to +75°C
- FAST SETTLING 1.5 μs to ½ L.S.B.
- EXPANDABLE FOR HIGHER RESOLUTIONS
- MONOLITHIC CONSTRUCTION
- DTL/TTL COMPATIBLE INPUTS
- RELIABLE MONOLITHIC CONSTRUCTION MEETS REQUIREMENTS OF MIL-STD-883

APPLICATIONS

- WAVEFORM SYNTHESIZERS
- MICROPROCESSOR I/O INTERFACE
- HIGH REL APPLICATIONS
- A TO D CONVERTER (USING COMPARATOR AND DIGITAL LOGIC)
- DATA ACQUISITION SYSTEMS

DESCRIPTION

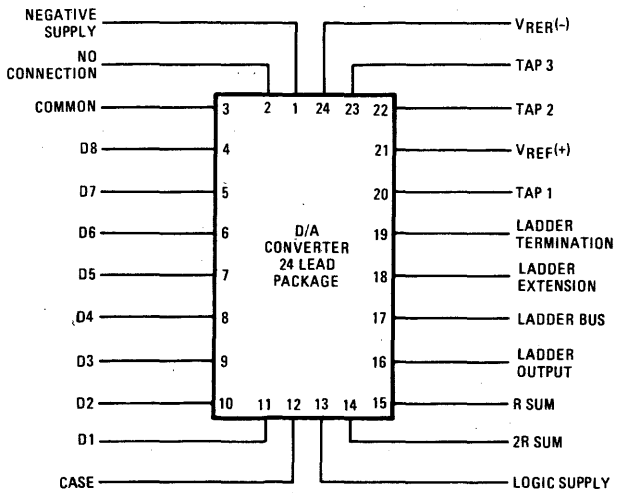
The HI-1080/1085 is a monolithic 8 bit digital-to-analog converter employing bipolar current switches feeding a thin film R-2R ladder network.

Because of the excellent stability of this device, it is practical to specify one all-inclusive accuracy parameter: ±1L.S.B. accuracy over the operating temperature range. This means that once the desired full scale output level is set at room temperature by adjustment of the input reference current, each of the 256 output levels will always measure within ±1 L.S.B. of the corresponding output of a "perfect" DAC. Thus the accuracy specification includes the worst case effects of all of the normally published errors such as non-linearity, zero drift, full scale drift, etc.

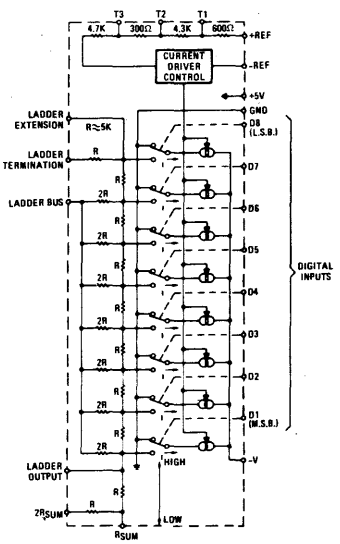
The device is exceptionally versatile, since it may be used in a voltage or current output mode, and may be offset to produce bipolar operation. Matched auxillary resistors are provided for amplifier feedback or current summing. Provisions are also made for scale factor adjustment and for cascading of additional D/A converters for extended resolution.

PINOUT

Top View — Package Code 4K



FUNCTIONAL DIAGRAM



SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Maximum Ratings are limiting values above which permanent circuit damage may occur.

Voltage
- V+ +8.0V
- V- -18.0V

Digital Inputs: +5.5V

Ladder Common: +8.0V

I_{REF}: 1.6mA

Storage Temperature: $-65^{o}C \leq TA \leq +150^{o}C$

Power Dissipation: 450mW *

*Derate at 4mW/°C above 85°C ambient.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated all measurements taken at V+ = +5V, V- = -15V
V_{REF} = +5V, V_{in}High = +2.4V, V_{in}Low = +0.4V
Unipolar, zero reference connection (Figure 3)

	TEMP	HI-1080 MIN	HI-1080 TYP	HI-1080 MAX	TEMP	HI-1085 MIN	HI-1085 TYP	HI-1085 MAX	UNITS
Resolution		8				8			Bits
Accuracy	+25°C		1/4	1/2					
(Calibrated at 25°C) (Note 1)	-55°C to +125°C		1/2	1	0°C to +75°C		1/2	1	L.S.B.
$V_{Full\ Scale}$ (Note 2) (Uncalibrated)	+25°C	-4.5	-4.98	-5.5	+25°C	-4.5	-4.98	-5.5	Volts
Power Supply Rejection (Note 3)	-55°C to +125°C	.05	.001		0°C to +75°C	.05	.001		L.S.B. per Volt
Settling Time (Note 4)	+25°C		1.5	3.0	+25°C		1.5		μs
Digital Inputs:									
High Threshold				2.0				2.0	Volts
Low Threshold (Note 5)		0.8				0.8			Volts
I_{in}High			.01	1	0°C		.01	1	mA
I_{in} Low (Note 6)	-55°C to +125°C		-0.7	-1.0	to +75°C		-0.7	-1.0	mA
Supply Current:									
I+	-55°C		8	10	0°C		8	10	mA
I-	to		8	10	to		8	10	mA
I_{REF} (Note 7)	+125°C		0.5	0.6	+75°C		0.5	0.6	mA

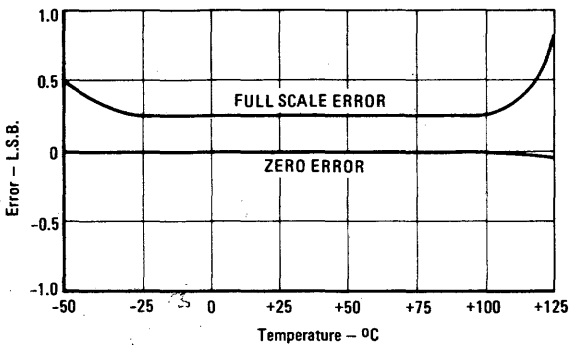
NOTES: Test Conditions -

1. Any Input Combination
2. Inputs all low
3. $\Delta V_{OUT}/\Delta V_{SUPPLY}$
   V+ = +5 ± 0.5V
   V- = -15 ± 3V
4. To ±0.2% of full scale after full scale input step
   $R_L > 10M$
   $C_L < 5pF$
5. V+ = 4.5V
6. V_{in} = 2.4 Volts
   V+ = 5.5V
   V_{in} = 0.4 Volts
   V+ = 5.5V
7. V+ = +5.0V
   V- = -15.0V
   V_{REF} = +5.0V
   Inputs all low

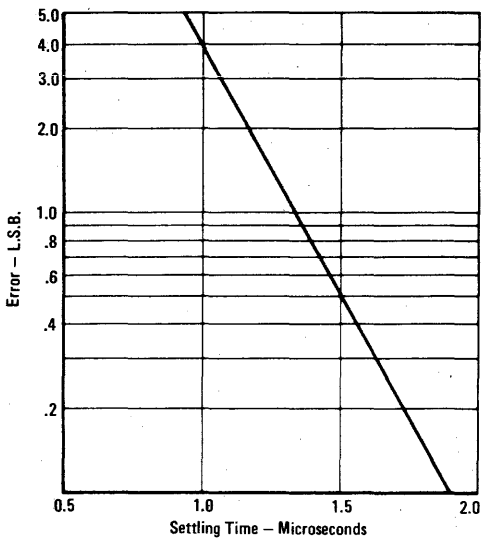
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PERFORMANCE CURVES

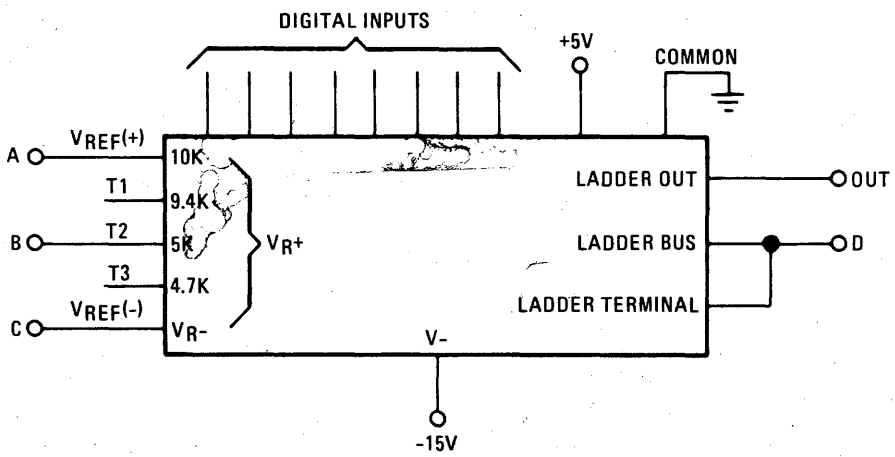
TYPICAL OUTPUT ACCURACY vs. TEMPERATURE



TYPICAL SETTLING TIME



D/A CONVERTER OPERATION MODES



MODE	OUTPUT RANGE INPUTS: ALL HIGH TO ALLLOW	CONNECTIONS			
		A*	B*	C	D
UNIPOLAR ZERO REFERENCE	0 TO -V_{R+} -1L.S.B.	V_{R+}	N.C.	GND	GND
UNIPOLAR ZERO F.S.	+/V_{R+}/TO 0 +1L.S.B.	V_{R+}	N.C.	GND	V_R
BIPOLAR	/V_{R+}/TO -V_R +1L.S.B.	N.C.	V_{R+}	GND	V_{R+}

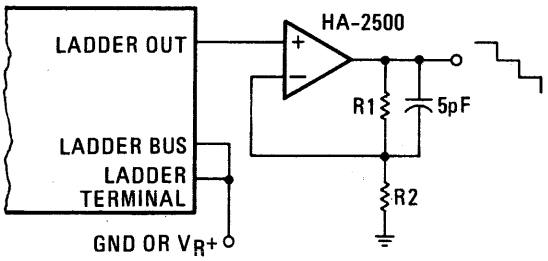
OPERATING MODES

*Tap 1 or Tap 3 with selected external series resistors may be substituted for points A or B, respectively, for fine adjustment of output range.

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TYPICAL APPLICATIONS

BUFFER AMPLIFIER CONNECTION

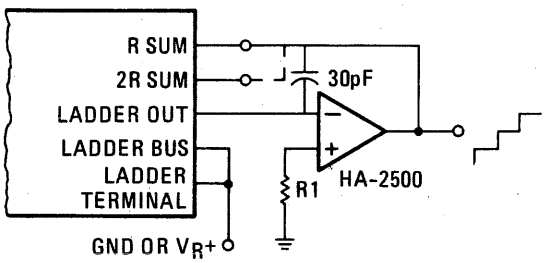


NON-INVERTING OUTPUT

(MORE NEGATIVE WITH INCREASING COMPLEMENT OF INPUT NUMBER)

OUTPUT RANGE: SAME AS SHOWN ON 'OPERATING MODE' CHART

MULTIPLIED BY $1+\frac{R1}{R2}$

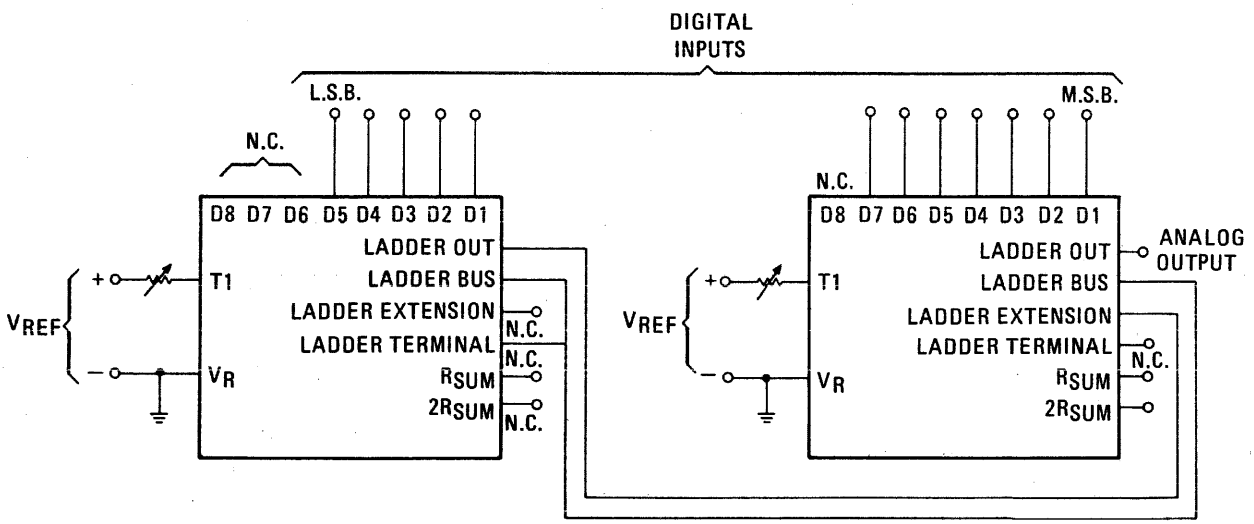


INVERTING OUTPUT

(MORE POSITIVE WITH INCREASING COMPLEMENT OF INPUT NUMBER)

FULL SCALE OUTPUT	OUTPUT FEEDBACK CONNECTED TO	R1
+4.98V	SUM	2.5K
+9.96V	$2R_{SUM}$	3.3K

CASCADED UNITS FOR 12 BIT RESOLUTION



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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-0165

Keyboard Encoder

FEATURES

- STROBE OUTPUT
- KEY ROLLOVER OUTPUT
- EXPANDABLE: 2 PACKAGES REQUIRED FOR FULL TELETYPEWRITER, EIGHT-BIT ENCODING
- SINGLE +5.0V SUPPLY REQUIRED
- DTL/TTL OUTPUTS
- MONOLITHIC RELIABILITY

APPLICATIONS

- MICROPROCESSOR DATA ENTRY (16 KEY TO HEX CODE)
- BCD DATA ENTRY
- TYPEWRITER TYPE KEYBOARDS
- CONTROL PANELS

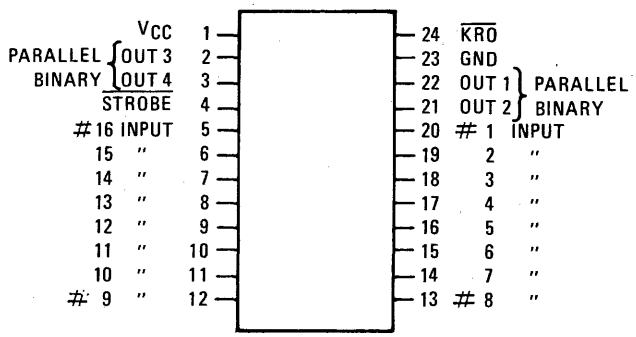
DESCRIPTION

The HD-0165 Keyboard Encoder is a 16 line to four-bit parallel encoder intended for use with manual data entry devices such as calculator or typewriter keyboards. In addition to the encoding function, there is a Strobe output and a Key Rollover output which energizes whenever two or more inputs are energized simultaneously. Any four-bit code can be implemented by proper wiring of the input lines. Inputs are normally wired through the key switches to the +5.0V power supply. Full typewriter keyboard encoding up to eight bits can be accomplished with two Encoder circuits by the use of double pole key switches or single pole switches with two isolation diodes per key. Outputs will interface with all popular DTL and TTL logic families. The circuit is packaged in a hermetic 24-pin dual-in-line package and operates over the temperature range of 0°C to +75°C.

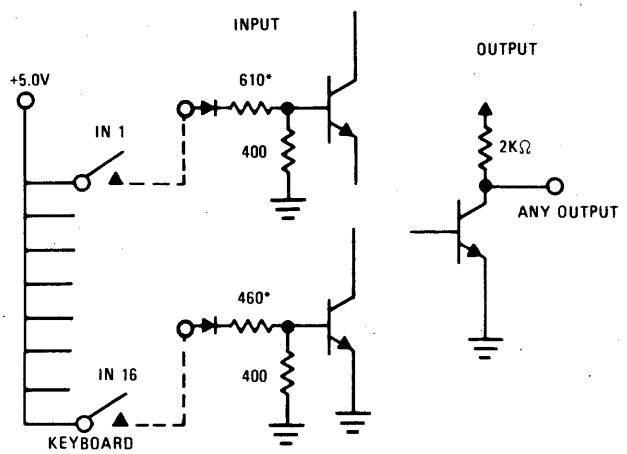
PINOUT

Package Code 4K

Top View



EQUIVALENT CIRCUITS



* EQUIVALENT RESISTORS FOR OTHER INPUTS ARE BETWEEN THESE TWO VALUES

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V	Output Current	30mA
Input Voltage	+5.5V	Storage Temperature	−65° to +150°C
Output Voltage	+5.5V	Operating Temperature (Case)	0°C to +75°C

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5.0V ± 5%
T_{Case} = 0°C to +75°C
Unless otherwise specified

	PARAMETER	SYM.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
	Input Current "1"	I_{IH}			17	mA	V_{IN} = +5.0V
D.C.	Output Voltage "0"	V_{OL}		+0.2	+0.4	V	V_{IH} = +4.5V I_{OL} = 10mA
D.C.	Output Voltage "0"	V_{OL}			+0.4	V	V_{IH} = +3.5V I_{OL} = 3.2mA
D.C.	Output Voltage "1"	V_{OH}	+2.4	+4.0		V	V_{IL} = Open Circuit, I_{OH} = −240µA
	Power Supply Current Operating	I_{CC}			52	mA	One Input at +5.25V
	Power Supply Current Maximum	I_{CCM}			88	mA	All Inputs at +5.25V
A.C.	Skew Time (Note 1)	T_{SK}		80	200	ns	T_{Case} = 25°C V_{CC} = V_{IN} = +5.0V C_L < 50pF

NOTE: (1) Skew time is the maximum time differential between propagation delay times of any outputs including $\overline{\text{strobe}}$ and $\overline{K_{RO}}$.

TRUTH TABLE

INPUTS 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	OUTPUTS 1	2	3	4	$\overline{St.}$	$\overline{K_{RO}}$
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H
H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L	H
L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	L	H
L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H
L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H	L	H
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H
L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	H	L	H
L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H
L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	H	L	L	H
L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	L	L	H
L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H	L	H	L	L	H
L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	H	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H
ANY TWO OR MORE HIGH																X	X	X	X	L	L

INPUTS: L = Open Circuit or < +1.0V H = > +4.5V Current Source
OUTPUTS: L = < +0.4V H = > +2.4V X = Erroneous Data

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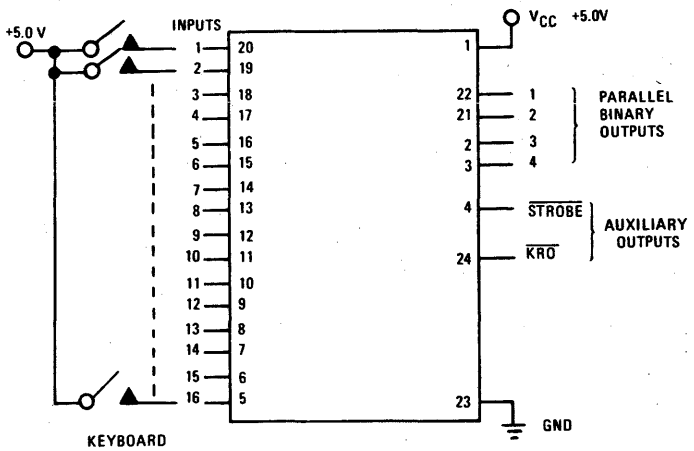


Figure 1. GENERAL CONFIGURATION FOR ENCODING TWO TO SIXTEEN KEYS

The Truth Table is used to determine wiring from the key switches to Encoder inputs to produce desired output codes.

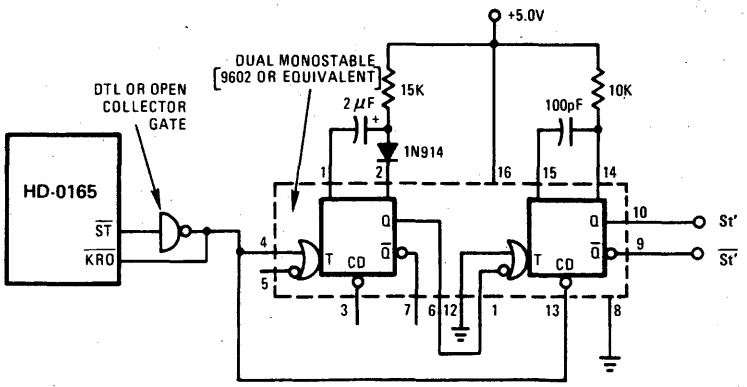
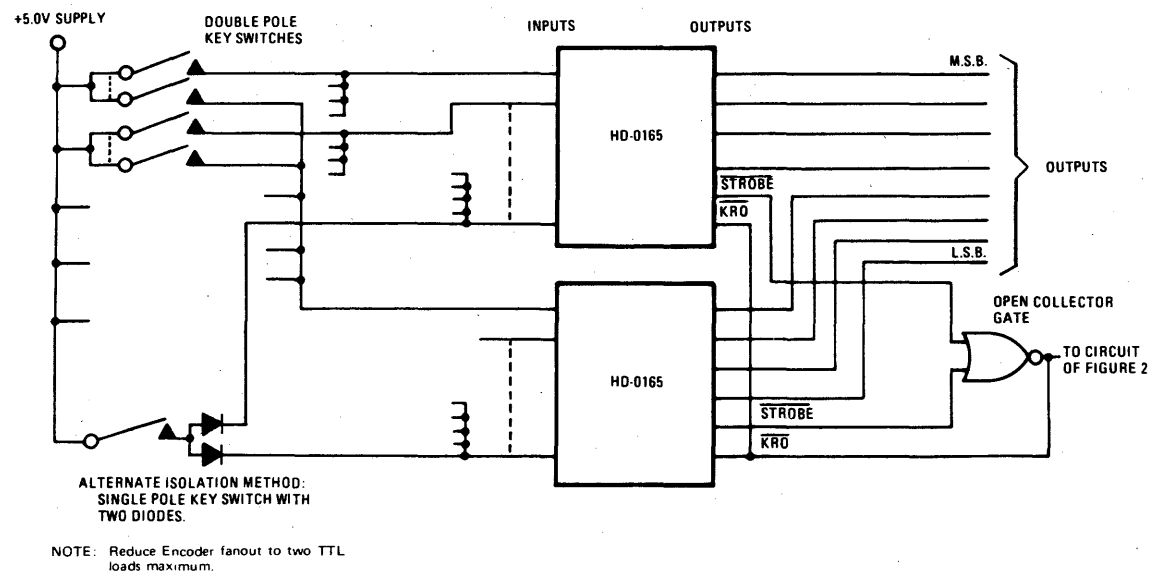


Figure 2. SWITCH BOUNCE ELIMINATION

This circuit generates a delayed Strobe pulse (St'). Delay time is determined by first monostable and should be about 10ms. Pulse width is determined by second monostable and should be set according to system requirements. Effect of switch bounce or arcing on make or break is positively eliminated and proper encoding will take place under two key rollover conditions.



NOTE: Reduce Encoder fanout to two TTL loads maximum.

Figure 3. ENCODING UP TO 256 KEYS

Use upper Encoder to produce the four most significant output bits; the lower to produce the least significant bits. Use Truth Table and required output codes to determine wiring from each key to the two Encoders.

SHIFT and CONTROL functions can be implemented by logic gates in series with the output lines.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-245/545 *Triple Line Transmitter*
HD-246/546/249/549 *Triple Line Receivers*
HD-248/548 *Triple Party Line Receiver*

FEATURES

- CURRENT MODE OPERATION
- HIGH SPEED: 15MHz WITH 50 FT. CABLE; 2MHz WITH 1,000 FT. CABLE
- HIGH NOISE IMMUNITY
- LOW EMI GENERATION
- LOW POWER DISSIPATION
- HIGH COMMON MODE REJECTION
- TRANSMITTER AND RECEIVER PARTY LINE CAPABILITY
- TOLERATES -2.0V GROUND DIFFERENTIAL (Transmitter with respect to receiver)
- TRANSMITTER INPUT/RECEIVER OUTPUT TTL/DTL COMPATIBLE

APPLICATIONS

- AIRCRAFT INSTRUMENTATION
- TELEMETRY
- INDUSTRIAL CONTROLS
- DATA EXCHANGE WITHIN AND BETWEEN BUILDINGS

DESCRIPTION

Each transmitter-receiver combination provides a digital interface between systems linked by 100Ω twisted pair, shielded cable. Each device contains three circuits fabricated within a single monliithic chip. Data rates greater than 15MHz are possible depending on transmission line loss characteristics and length.

The transmitter employs constant current switching which provides high noise immunity along with high speeds, low power dissipation, low EMI generation and the ability to drive high capacitance loads. In addition, the transmitters can be turned "off", allowing several transmitters to time-share a single line.

Receiver input/output differences are shown in the following table:

	INPUT	OUTPUT
HD-246 / 546	100 Ω	OPEN COLLECTOR
HD-248 / 548	HI-Z	6K PULL-UP RES.
HD-249 / 549	100Ω	6K PULL-UP RES.

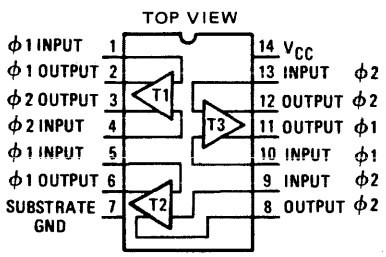
The internal 100Ω cable termination consists of 50Ω from each input to ground.

HD-248/548 "party line" receivers have a high-Z input such that as many as ten of these receivers can be used on a single transmission line.

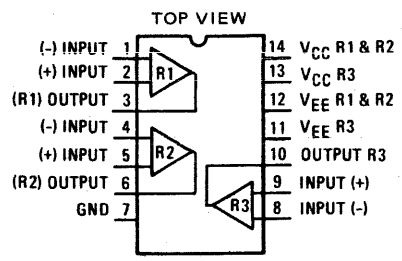
Each transmitter input and receiver output can be connected to TTL and DTL systems. When used with shielded transmission line, the transmitter-receiver system has very high immunity to capacitive and magnetic noise coupling from adjacent conductors. The system can tolerate ground differentials of -2.0V to +20.0V (transmitter with respect to receiver).

PINOUTS

TRANSMITTERS — **Package Codes 9V, 1S**

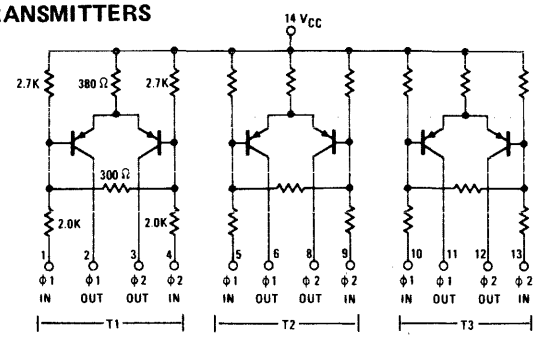


RECEIVERS — **Package Codes 9V, 1S**

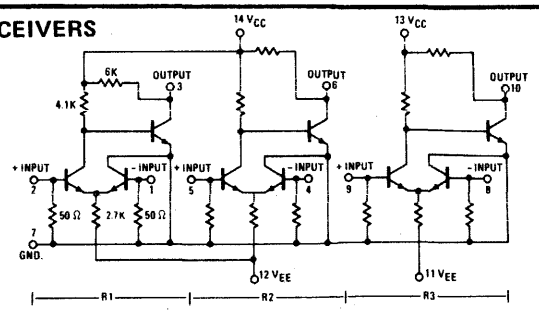


SCHEMATIC DIAGRAMS

TRANSMITTERS



RECEIVERS



NOTES:
1. HD- 249/549 is as shown
2. HD- 246/546 does not have 6K output pull- up resistors.
3. HD- 248/548 does not have 50 Ω input termination
4. Resistor values are nominal resistors.

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Input Voltage Range: -0.5V to +10V
Output Voltage Range: -30V to +0.5V with respect to V_{CC}
V_{CC} Range: -0.5V to +10V
Storage Temperature Range: -65°C to +150°C

ELECTRICAL CHARACTERISTICS

				HD-245 -55°C to +125°C			HD-545 0°C to +75°C				TEST CONDITION	
	PARAMETER	SYMBOL	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	V_{CC}	NOTES
DC	INPUT LOW CURRENT	I_{IL}	25°C Full		-1.5	-2.2 -2.5		-1.5	-2.3 -2.4	mA	5.5	1
DC	"ON" OUTPUT CURRENT	I_{OUT} "ON"	25°C Full Full	-2.3 -2.0 -1.6			-1.9 -1.8 -1.5			mA mA mA	4.5 4.5 4.5	1 1 2
DC			25°C Full		-4.1	-5.4 -5.6		-4.1	-6.3 -6.7	mA	5.5	1
DC	"ON" OUTPUT CURRENT UNBALANCE	ΔI_{OUT}	25°C Full		0.1	0.25 0.3		0.1	0.25 0.3	mA	5.5	3
DC	"OFF" OUTPUT CURRENT	I_{OUT} "OFF"	25°C Full		-30	-100 -100		-30	-100 -100	μA	4.5	1
DC	OUTPUT BREAKDOWN	BV_{CER}	25°C	-30	-50		-30	-50		V	GND	4
DC	POWER SUPPLY CURRENT-TOTAL		25°C 25°C		15	18.6 0.6		15	24 0.6	mA	5.0	5 6
AC	PROPAGATION DELAY	t_{PLH}	25°C Full		3	10 14		3	10 14	ns	5.0	
AC	TEST CIRCUIT 1, PAGE 4	t_{PHL}	25°C Full		3.2	10 14		3.2	10 14	ns	5.0	

NOTES:
1. One input at Gnd. one input open, each output at
2. One input at 0.45V, one input open, each output at Gnd.
3. Difference between $\phi 1$ and $\phi 2$ "ON" output data current.
4. Each input at Gnd., one output at Gnd., $I_{Limit} \geq 100\mu A$ on output tested with -30V applied.
5. One input of each transmitter at Gnd. and the other input open. All six output lines at Gnd.
6. All six input lines open, all six output lines at Gnd.

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ABSOLUTE MAXIMUM RATINGS

Input Voltage Range	-1.0V to +1.0V	Input Current	±25mA
Output Voltage Range	-0.5V to +6.0V	Output Current	+50mA
V_{CC} Range	-0.5V to +8.0V	Storage Temperature	-65°C to +150°C
V_{EE} Range	-8.0V to +0.5V		

ELECTRICAL CHARACTERISTICS

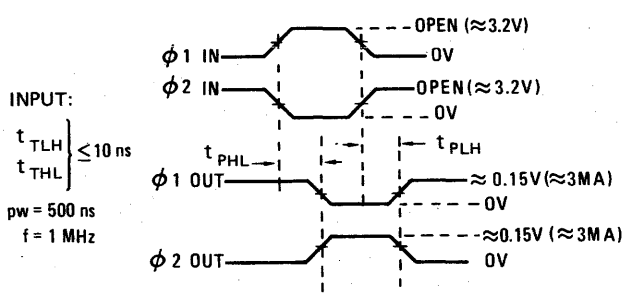
	PARAMETER	SYM.	TEMP.	HD-246 / 248 / 249 -55°C to +125°C MIN.	TYP.	MAX	HD-546 / 548 / 549 0°C to +75°C MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS V_{EE} = -5V V_{CC}	NOTES
	INPUT RESISTANCE (HD-246/546 & HD-249/549	R_{IN}	+25°C Full	40 39	47	61 68	35 33	47	65 70	Ohms		
	PULL-UP RESISTOR (HD-248/548 & HD-249/549)		+25°C Full	4.2 4.1	6	7.8 8.6	4.0 3.9	6	8.1 8.6	K Ohms		
	OUTPUT VOLTAGE (HIGH)	V_{OH}	+25°C Full	2.6 2.5			2.6 2.5			V	4.5	Note 1 I_{OH}=-120μA Ext. 6K Res. For HD-246/546
DC	OUTPUT VOLTAGE (LOW)	V_{OL}	+25°C Full			0.45 0.45			0.45 0.45	V	4.5	Note 2 I_{OL}=9.6mA 10mA For HD-246/546
	OUTPUT VOLTAGE (LOW) (INPUT SHORTCIRCUIT)	V_{OLSC}	+25°C		0.4			0.4		V	5.0	Note 3 I_{OL} = 3.2mA
	POWER SUPPLY CURRENT (TOTAL) HD-246 / 546	I_{CC} I_{EE}	+25°C		3.3 5.1	4.8 6.3		3.3 5.1	5.7 6.3	mA	5.0	Note 4
		I_{CC} I_{EE}	+25°C		3.9 5.1	6.6 6.3		3.9 5.1	7.5 6.3	mA	5.0	Note 5
	HD-248 / 548	I_{CC} I_{EE}	+25°C		6.3 5.1	7.8 6.3		6.3 5.1	8.7 6.3	mA	5.0	Note 4
		I_{CC} I_{EE}	+25°C		3.9 5.1	6.6 6.3		3.9 5.1	7.5 6.3	mA	5.0	Note 5
	HD-249 / 549	I_{CC} I_{EE}	+25°C		6.3 5.1	7.8 6.3		6.3 5.1	8.7 6.3	mA	5.0	Note 6
		I_{CC} I_{EE}	+25°C		3.9 5.1	6.6 6.3		3.9 5.1	7.5 6.3	mA	5.0	Note 7
	PROPAGATION DELAY	t_{PLH}	+25°C Full		18	30 30		18	30 30	ns	5.0	
AC	TEST CIRCUIT 2 PAGE 4	t_{PHL}	+25°C Full		25	30 30		25	30 30	ns	5.0	

NOTES:
1. (+) I_{IN} = 1.5mA; (-) Input = open (For HD-248/548; Ext. 50 Res. or 75mV).
2. (+) Input = open; (-) I_{IN} = 1.5mA. (For HD-248/548; Ext. 50 Res. or 75mA).
3. Both inputs shorted to Gnd; or both inputs open such that 50 termination resistors are in the circuit.
4. (+) Input = open; (-) I_{IN} = 3mA.
5. (+) I_{IN} = 3mA; (-) Input = open.
6. (+) Input = Gnd.; (-) Input = .15V.
7. (+) Input = .15V; (-) Input = Gnd.

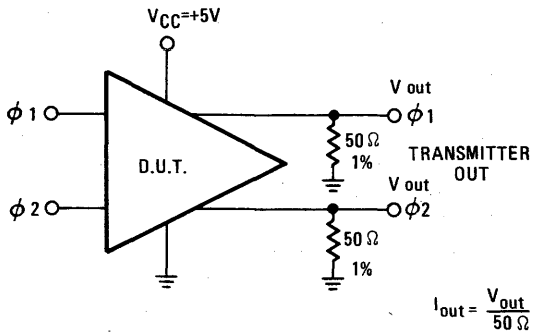
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TEST CIRCUITS

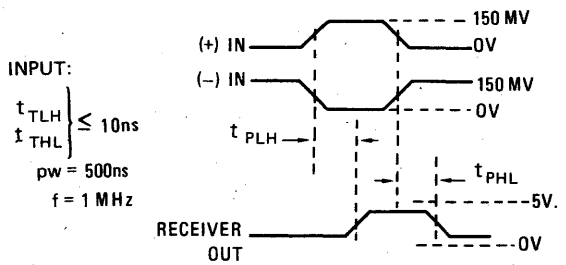
TEST CIRCUIT 1 - TRANSMITTER PROPAGATION DELAY



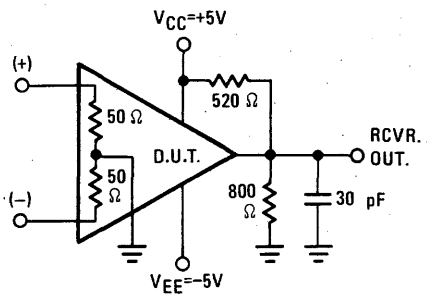
All measurements referenced to 50 % V points



TEST CIRCUIT 2 - RECEIVER PROPAGATION DELAY



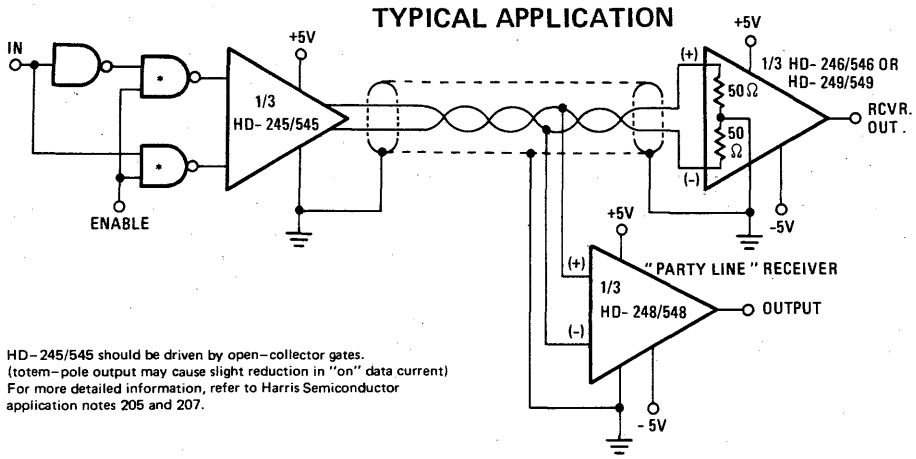
All measurements referenced to 50%V points.



NOTE: External 50Ω resistors needed for HD–248/548.

APPLICATIONS

TYPICAL APPLICATION



* HD–245/545 should be driven by open–collector gates. (totem–pole output may cause slight reduction in "on" data current) For more detailed information, refer to Harris Semiconductor application notes 205 and 207.

Octal Latch
Octal Register

SN54/74S373 and Options
SN54/74S374 and Options

FEATURES

- Inverting and Non-Inverting Outputs
- 20 mA and 32 mA I_{OL}
- 3-State Outputs Drive Bus Lines
- Slim 20 Pin Package Saves Space
- 8 Bits Matches Byte Boundaries
- Hystersis Improves Noise Margin
- Low Current PNP Inputs Reduce Loading
- Ideal for Microprocessor Interface

DESCRIPTION

The latch passes eight (octal) bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight (octal) bits of input data and passes it to the output on the "rising edge" of the clock.

The three state outputs are active when $\overline{OE}$ is low, and high impedance when $\overline{OE}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hystersis.

The SN54/74SXXX device types are industry standard parts. The 57/67SXXX device types are Monolithic Memories' "enhanced" versions. The enhancements include:

1) Increased output sink current (I_{OL}) from the standard Schottky I_{OL} of 20 mA to an improved 32 mA.

2) Inverting outputs instead of the standard non-inverting outputs.

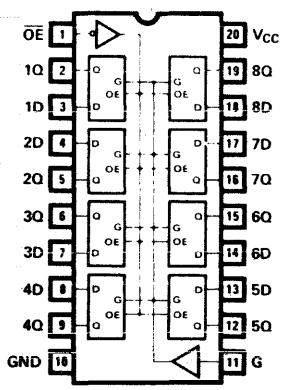
TYPE	OUTPUT	I_{OL}	TEMP	PART NUMBER	PACKAGE TYPE	PACKAGE PINS
Latch	non-invert	20 mA	com	SN74S373	J, N	20
			mil	SN54S373	J	20
		32 mA	com	67S373	J, N	20
			mil	57S373	J	20
	invert	20 mA	com	67S380	J, N	20
			mil	57S380	J	20
		32 mA	com	67S382	J, N	20
			mil	57S382	J	20
Reg-ister	non-invert	20 mA	com	SN74S374	J, N	20
			mil	SN54S374	J	20
		32 mA	com	67S374	J, N	20
			mil	57S374	J	20
	invert	20 mA	com	67S376	J, N	20
			mil	57S376	J	20
		32 mA	com	67S378	J, N	20
			mil	57S378	J	20

Package Types: J - Ceramic DIP, N - Plastic DIP

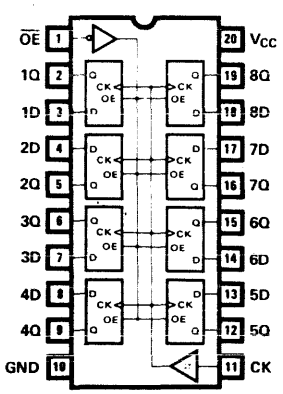
The higher I_{OL} is intended for upgrading systems which presently satisfy 32 mA requirements with SN54/74365, 366, 367, 368, Hex Buffers. The inverting outputs are intended for bus applications that require inversion as in interfacing the Am 2901A 4-Bit Slice to an active low bus.

All of the octal devices are packaged in the popular 20 pin skinny DIP.

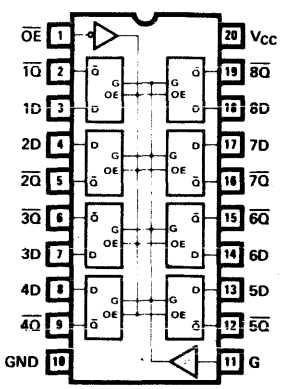
Octal Latch
SN54/74S373
57/67S373



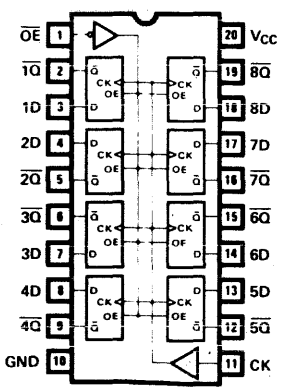
Octal Register
SN54/74374
57/67S374



Octal Latch (Inverting)
57/67S380
57/67S382



Octal Register (Inverting)
57/67S376
57/67S378



Monolithic Memories
1165 East Arques Ave., Sunnyvale CA 94086
Tel: (408) 739-3535/TWX: (910) 339-9229

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Off-State Output Voltage 5.5V
Storage Temperature Range . . . . . -65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		MILITARY			COMMERCIAL			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{OH}	High Level Output Voltage				5.5			5.5	V
I_{OH}	High Level Output Current				-2			-6.5	mA
t_W	Width of Clock/Gate	High	6			6			ns
		Low	7.3			7.3			ns
t_{SU}	Set Up Time	Latch	0↓			0↓			ns
		Register	5↑			5↑			ns
t_H	Hold Time	Latch	10↓			10↓			ns
		Register	2↑			2↑			ns
T_A	Operating Free Air Temperature		-55		125	0		70	°C

The arrow ↑ or ↓ indicates the transition of gate/clock input for reference: ↑ means the low to high transition

ELECTRICAL CHARACTERISTICS

Over recommended operating free air temperature range unless otherwise noted

SYMBOL	PARAMETER		CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High Level Input Voltage				2			V
V_{IL}	Low Level Input Voltage						0.8	V
V_{IC}	Input Clamp Voltage		V_{CC} = Min, I_I = -18 mA				-1.2	V
V_{OH}	High Level Output Voltage		V_{CC} = Min. V_{IH} = 2V, I_{OH} = Max V_{IL} = 0.8V		2.4	3.1		V
V_{OL}	Low Level Output Voltage	SN54/74S373 57/67S380 SN54/74S374 57/67S376	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 20 mA			0.5	V
		57/67S373 57/67S382 57/67S374 57/67S378		I_{OL} = 32 mA				
I_{HZ}	High Level Off-State Output Current		V_{CC} = Max, V_O = 2.4V, V_{IH} = 2V				50	μA
I_{LZ}	Low Level Off-State Output Current		V_{CC} = max, V_O = 0.5V, V_{IH} = 2V				-50	μA
I_I	Maximum Input Current		V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current		V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current		V_{CC} = Max, V_I = 0.5V				-250	μA
I_{OS}	Output Short Circuit Current		V_{CC} = Max		-40		-100	mA
I_{CC}	Supply Current	Latch	V_{CC} = Max			105	160	mA
		Register	V_{CC} = Max			90	140	mA

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	LATCH			REGISTER			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Maximum Clock Frequency					75	100		MHz
t_{PLH}	Data to Output Delay	C_L = 15 pF R_L = 280Ω		5	9				ns
t_{PHL}				9	13				ns
t_{PLH}	Clock/Gate to Output Delay			7	14		8	15	ns
t_{PHL}				12	18		11	17	ns
t_{PZH}	Output Enable Delay			8	15		8	15	ns
t_{PZL}				11	18		11	18	ns
t_{PHZ}	Output Disable Delay	C_L = 5pF R_L = 280Ω		6	9		5	9	ns
t_{PLZ}				8	12		7	12	ns

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Octal Buffers

SN74S240 SN74S241 SN74S244
SN54S240 SN54S241 SN54S244

FEATURES

- 3-State Outputs Drive Bus Lines
- Slim 20 Pin Package Saves Space
- 8 Bits Matches Byte Boundaries
- Hystersis Improves Noise Margin
- Low Current PNP Inputs Reduce Loading
- Ideal for Microprocessor Interface

DESCRIPTION

The Octal Buffers pack eight high current bus drivers into one 20 pin skinny DIP. Each output can deliver a source current of 15 mA and a sink current of 64 mA. The drive power is sufficient to drive two of the popular 330Ω/220Ω computer peripheral terminations. (Two are important as both ends of a transmission line need to be terminated). PNP inputs and hystersis provide improved fan-in and 400 mV noise margin.

The series includes three options which are distinguished as follows:

DEVICE	OUTPUT	ENABLE
S240	inverting	active low
S241	non-inverting	active low and active high
S244	non-inverting	active low

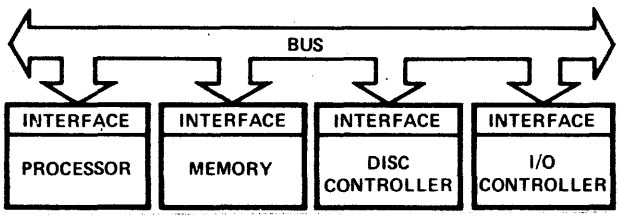
The S240 and S244 provide both output polarities with the standard active low enable ($\overline{E}$ low enables the output). The S241 allows transceiver operation when $\overline{E}$ and E are tied together.

TYPE	OUTPUT	I_{OL}	TEMP	PART NUMBER	PACKAGE TYPE	PACKAGE PINS
Buffer	invert	64 mA	com	SN74S240	J, N	20
	invert	48 mA	mil	SN54S240	J	20
	non-invert	64 mA	com	SN74S241	J, N	20
	non-invert	48 mA	mil	SN54S241	J	20
	non-invert	64 mA	com	SN74S244	J, N	20
	non-invert	48 mA	mil	SN54S244	J	20

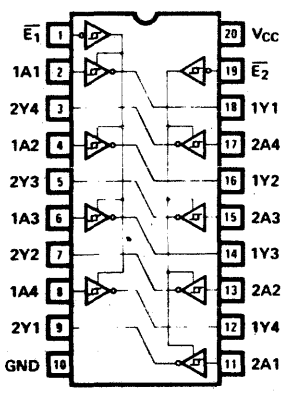
Package Types: J - Ceramic DIP, N - Plastic DIP

APPLICATIONS

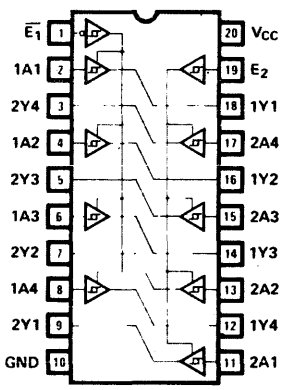
The Octal Buffers are used in both high performance microprogrammed digital processors and low performance MOS microcomputer systems. As buffers are used to interface computer components together over a common bus, their usage spans the entire digital system as shown below.



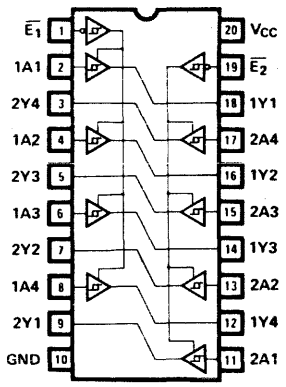
SN54/74S240



SN54/74S241



SN54/74S244



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Off-State Output Voltage 5.5V
Storage Temperature Range . . . . . -65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High Level Output Current			-12			-15	mA
I_{OL}	Low Level Output Current			48			64	mA
T_A	Operating Free Air Temperature	-55		125	0		70	°C

The SN54S241J or SN54S244J operating at free air temperature above 116°C requires a heat sink such that $R_{\theta CA}$ is not more than 40°C/W.

ELECTRICAL CHARACTERISTICS

Over recommended operating free air temperature range

SYMBOL	PARAMETER		CONDITIONS		S240			S241, S244			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High Level Input Voltage				2			2			V
V_{IL}	Low Level Input Voltage						0.8			0.8	V
V_{IC}	Input Clamp Voltage		V_{CC} = Min, I_I = -18mA				-1.2			-1.2	V
	Hystersis ($V_{T+} - V_{T-}$)		V_{CC} = Min		0.2	0.4		0.2	0.4		V
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = -3mA		2.4	3.4		2.4	3.4		V
			V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.5V, I_{OH} = Max		2			2			
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = Max				0.55			0.55	V
I_{OZH}	Off State Output Current		V_{CC} = Max V_{IH} = 2V V_{IL} = 0.8V	V_O = 2.4V			50			50	μA
I_{OZL}				V_O = 0.5V			-50			-50	
I_I	Maximum Input Current		V_{CC} = Max, V_I = 5.5V				1			1	mA
I_{IH}	High Level Input Current		V_{CC} = Max, V_I = 2.7V				50			50	μA
I_{IL}	Low Level Input Current	Any A	V_{CC} = Max, V_I = 0.5V				-400			-400	μA
		Any E					-2			-2	mA
I_{OS}	Short Circuit Output Current*		V_{CC} = Max		-50		-225	-50		-225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = Max Outputs Open	SN54S'		80	123		95	147	mA
				SN74S'		80	135		95	160	
		Outputs Low		SN54S'		100	145		120	170	
				SN74S'		100	150		120	180	
		Outputs Disabled		SN54S'		100	145		120	170	
				SN74S'		100	150		120	180	

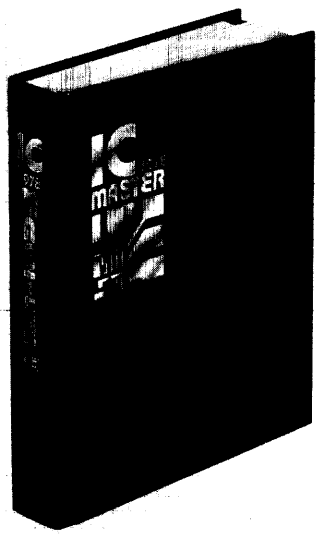
*Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	S240			S241, S244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data to Output Delay	C_L = 50 pF R_L = 90Ω		4.5	7		6	9	ns
t_{PHL}				4.5	7		6	9	ns
t_{PZL}	Output Enable Delay			10	15		10	15	ns
t_{PZH}				6.5	10		8	12	ns
t_{PLZ}	Output Disable Delay	C_L = 5 pF R_L = 90Ω		10	15		10	15	ns
t_{PHZ}				6	9		6	9	ns

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DP/INS4201 clock generator

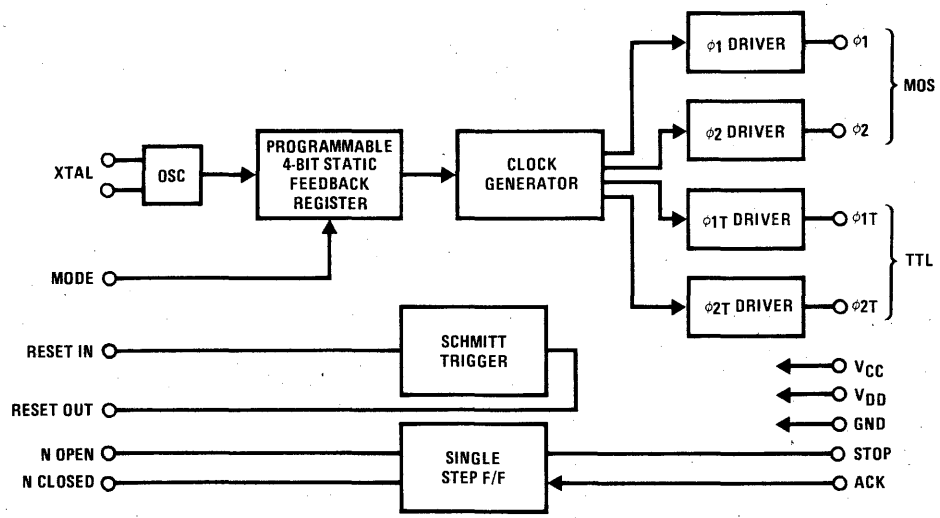
general description

The DP4201 Clock Generator is designed for 4004 micro-computer series family applications, and satisfies clock signal requirements MCS-40™ and FIPS (4-Bit Integrated Processing System) micro-computer devices. An externally crystal controlled oscillator is required for generation of TTL and MOS level clock signals. Power "ON" or external reset may be accomplished with the DP4201. A single step feature also exists.

features

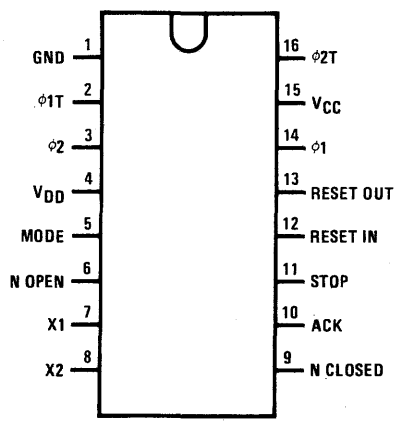
- Satisfies clock requirements for FIPS and MCS-40
- Crystal controlled oscillator
- MOS and TTL level clock outputs
- Power "ON" and external reset control
- Operative frequency from dc to 6 MHz

block diagram



connection diagram

Dual-In-Line Package



TOP VIEW

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ac electrical characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} - V_{DD} = 15V \pm 5\%$, Gnd = $V_{CC} - 5V \pm 5\%$, $1.35\ ns \leq t_{cy} \leq 2\mu s$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{cy}	Clock Period	Mode = V_{CC}		$t_{XTAL}x7$		ns
$t_{\phi PW}$	Clock Pulse Width	Mode = V_{CC}	$(2/7)t_{cy}-10$	$(2/7)t_c$	$(2/7)t_{cy}+10$	ns
$t_{\phi D1}$	Clock Delay From ϕ_1 to ϕ_2	Mode = V_{CC}	$(2/7)t_{cy}-10$	$(2/7)t_{cy}$	$(2/7)t_{cy}+10$	ns
$t_{\phi D2}$	Clock Delay From ϕ_2 to ϕ_1	Mode = V_{CC}	$(1/7)t_{cy}-10$	$(1/7)t_{cy}$	$(1/7)t_{cy}+10$	ns
t_{cy}	Clock Period	Mode = V_{DD}		$t_{XTAL}x8$		ns
$t_{\phi PW}$	Clock Pulse Width	Mode = V_{DD}	$(1/4)t_{cy}-10$	$(1/4)t_{cy}$	$(1/4)t_{cy}+10$	ns
$t_{\phi D1}$	Clock Delay From ϕ_1 to ϕ_2	Mode = V_{DD}	$(1/4)t_{cy}-10$	$(1/4)t_{cy}$	$(1/4)t_{cy}+10$	ns
$t_{\phi D2}$	Clock Delay From ϕ_2 to ϕ_1	Mode = V_{DD}	$(1/4)t_{cy}-10$	$(1/4)t_{cy}$	$(1/4)t_{cy}+10$	ns
$t_{\phi D3}$	TTL Clock to MOS Clock Skew		0	20	40	ns
$t_{\phi r}, t_{\phi f}$	Clock Rise and Fall Time	C_L = 300 pF = ϕ_1, ϕ_2 C_L = 50 pF = ϕ_{1T}, ϕ_{2T}		25	50	ns
t_D	Delay From ACK to Stop	C_L = 20 pF		60	500	ns

pin description

Pin No.	Designation	Description of Function
1	GND	Circuit ground potential. This pin can be left floating for low power application. MOS clock output will be operative. TTL clock outputs will not.
2	ϕ_{1T}	Phase 1. TTL level clock output. Positive true.
3	ϕ_2	Phase 2. MOS level clock output.
4	V_{DD}	Main power supply pin. $V_{DD} = V_{CC} - 15V \pm 5\%$.
5	MODE	Counter mode control pin. Determines whether counter divides basic frequency by 8 or 7. Mode = V_{CC}; ÷7 Mode = V_{DD}; ÷8
6	N. OPEN	Input of single step circuitry to which normally open contact of SPDT switch is connected.
7	X1	External crystal connection. This pin may be driven by an external frequency source. X2 should be left unconnected.
8	X2	External crystal connection.
9	N. CLOSED	Input of single step circuitry to which normally closed contact of SPDT switch is connected.
10	ACK	Acknowledge input to single step circuitry normally connected to stop acknowledge output of 4004.
11	STOP	Stop output of single step circuitry normally connected to stop input of 4004. A SPDT toggle switch may be inserted in this line for RUN/HALT control.
12	RESET IN	Input to which RC network is connected to provide power on reset timing.
13	RESET OUT	This signal is active low.
14	ϕ_1	Phase 1 MOS level clock output.
15	V_{CC}	Circuit reference potential—most positive supply voltage.
16	ϕ_{2T}	Phase 2. TTL level clock output. Positive true.

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absolute maximum ratings (Note 1)

$V_{CC} - V_{DD}$ dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	V_{DD} − 0.3 to V_{CC} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

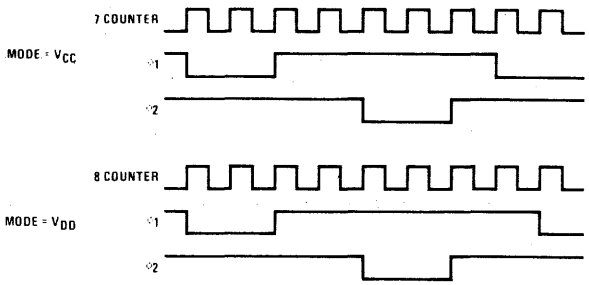
$V_{CC} - V_{DD}$ dc Supply Voltage	15 V_{DC}
V_{CC} − Gnd dc Supply Voltage	5 V_{DC}
V_{IN} Input Voltage	V_{DD} to V_{CC}
T_A Operating Temperature Range	0°C to +70°C

dc electrical characteristics $T_A = 0°C$ to +70°C, $V_{CC} - V_{DD} = 15V \pm 5\%$, Gnd = $V_{CC} - 5V \pm 5\%$

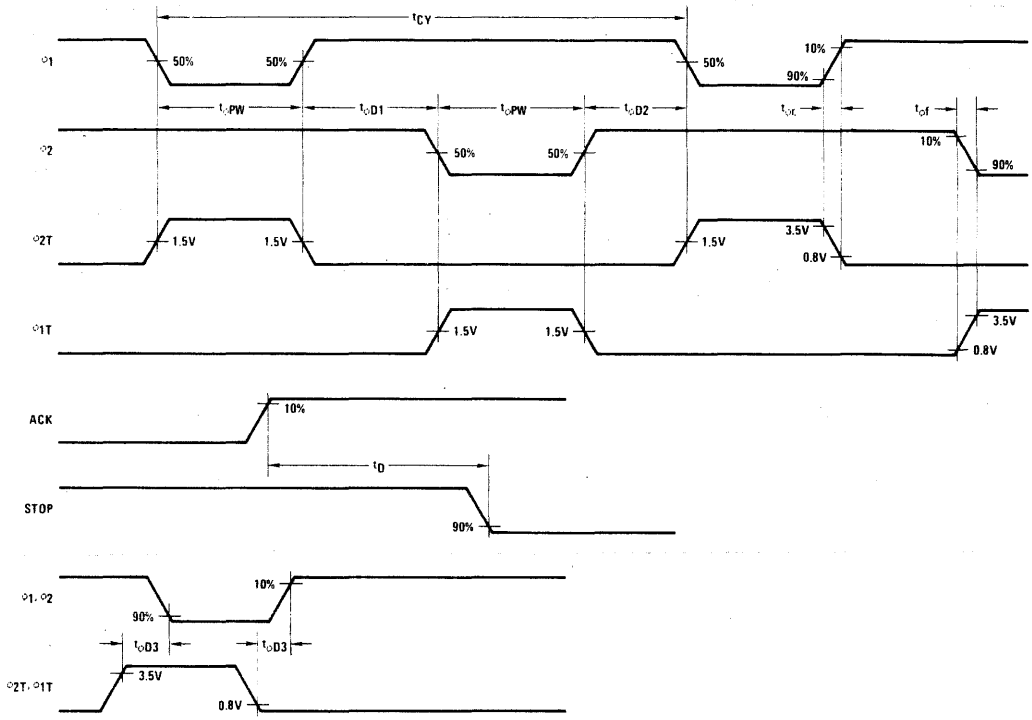
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Supply Current (Measurement in V_{CC} Pin)	Static Operation, Pin 6, Pin 9 = V_{CC}, Pin 12, Pin 10 = V_{DD}, Pin 7 = V_{CC}			300	μA
		Dynamic Operation, 5.185 MHz Crystal, C_L = 20 pF, ϕ_1 and ϕ_2			25	mA
I_{L1}	Input Leakage Current	$V_{IL} = V_{DD}$, All Inputs Except X1, X2, N. Open, N. Closed			1	μA
V_{IH}	Input High Voltage	All Inputs Except X1, X2, Reset	V_{CC}−1.5		V_{CC}+0.5	V
V_{IL}	Input Low Voltage	All Inputs Except X1, X2, Reset	V_{DD}		V_{CC}−13	V
V_{OH}	Output High Voltage	Capacitive Load Only	V_{CC}−1.5		V_{CC}	V
V_{OL}	Output Low Voltage	Capacitive Load Only	V_{DD}		V_{CC}−13.4	V
V_{OH}	ϕ1T, ϕ2T, Output High Voltage	I_{OH} = −400μA	V_{CC}−0.75			V
V_{OL}	ϕ1T, ϕ2T Output Low Voltage	I_{OL} = 1.6 mA			Gnd+0.5	V
I_{OL}	ϕ_1, ϕ_2 Sink Current	$V_{OUT} = V_{CC}$, Pulse Width ≤ 1μs	400			mA
I_{OH}	ϕ_1, ϕ_2 Source Current	$V_{OUT} = V_{DD}$	180			mA
I_{OL}	ϕ1T, ϕ2T Sink Current	$V_{OUT} = V_{CC}$	15			mA
I_{OH}	ϕ1T, ϕ2T Source Current	$V_{OUT} = V_{DD}$	8			mA
I_{OL}	Reset Sink Current	$V_{OUT} = V_{CC}$	6			mA
I_{OH}	Reset Source Current	$V_{OUT} = V_{DD}$	6			mA
I_{OL}	Stop Sink Current	$V_{OUT} = V_{CC}$	1			mA
I_{OH}	Stop Source Current	$V_{OUT} = V_{DD}$	1			mA
V_{IL}	Reset Input Low Voltage		V_{DD}		V_{CC}−11	V
V_{IH}	Reset Input High Voltage		V_{CC}−6.5		V_{CC}+0.5	V
R_I	Pull-Up Resistance on N. Open, N. Closed	$V_{IN} = V_{DD}$	20		120	kΩ
C_{IN}	Input Capacitance	All Inputs Except X1, X2		5		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

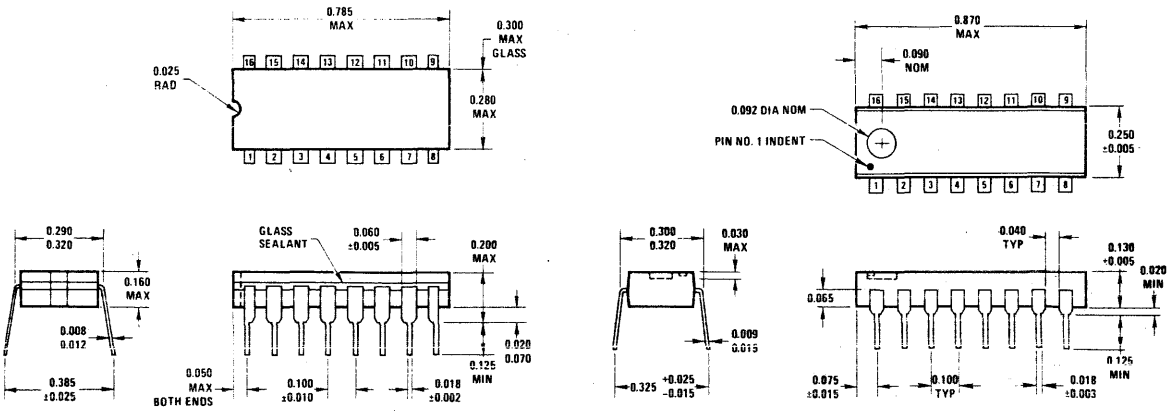
timing diagrams



switching time waveforms



physical dimensions



Cavity Dual-In-Line Package (J)
Order Number DP4201J

Molded Dual-In-Line Package (N)
Order Number DP4201N

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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National Semiconductor

DP8212 8-Bit Input/Output Port

general description

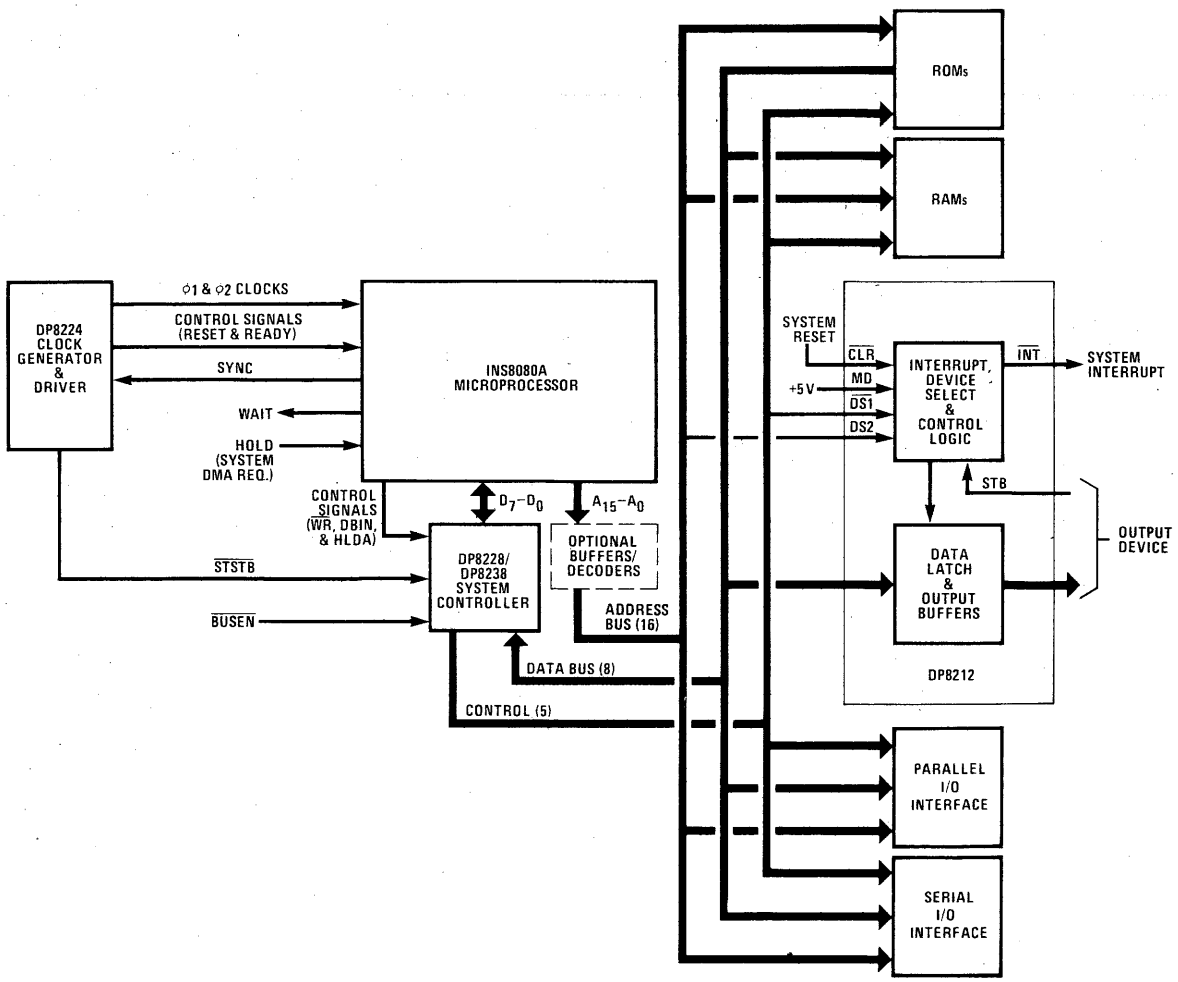
The DP8212 is an 8-bit input/output port contained in a standard 24-pin dual-in-line package. The device, which is fabricated using Schottky Bipolar technology, is part of National Semiconductor's N8080 microcomputer family. The DP8212 can be used to implement latches, gated buffers, or multiplexers. Thus, all of the major peripheral and input/output functions of a microcomputer system can be implemented with this device.

The DP8212 includes an 8-bit latch with TRI-STATE® output buffers, and device selection and control logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

features

- 8-Bit Data Latch and Buffer
- Service Request Flip-flop for Generation and Control of Interrupts
- 0.25mA Input Load Current
- TRI-STATE TTL Output Drive Capability
- Outputs Sink 15mA
- Asynchronous Latch Clear
- 3.65V Output for Direct Interface to INS8080A
- Reduces System Package Count by Replacing Buffers, Latches, and Multiplexers in Microcomputer Systems

N8080A microcomputer family block diagram



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absolute maximum ratings

Temperature Under Bias Plastic . . . . . −65°C to +75°C
Storage Temperature . . . . . −65°C to +160°C
All Output or Supply Voltages. . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to 5.5V
Output Currents 125mA

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

dc electrical characteristics

$T_A = 0°C$ to $+75°C$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Load Current STB, DS_2, $\overline{CLR}$, DI_1-DI_8 Inputs			−0.25	mA	$V_F = 0.45V$
I_F	Input Load Current MD Input			−0.75	mA	$V_F = 0.45V$
I_F	Input Load Current $\overline{DS_1}$ Input			−1.0	mA	$V_F = 0.45V$
I_R	Input Leakage Current STB, DS_2, $\overline{CLR}$, DI_1-DI_8 Inputs			10	μA	$V_R = 5.25V$
I_R	Input Leakage Current MD Input			30	μA	$V_R = 5.25V$
I_R	Input Leakage Current $\overline{DS_1}$ Input			40	μA	$V_R = 5.25V$
V_C	Input Forward Voltage Clamp			−1	V	$I_C = -5mA$
V_{IL}	Input "Low" Voltage			0.85	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			0.45	V	$I_{OL} = 15mA$
V_{OH}	Output "High" Voltage	3.65	4.0		V	$I_{OH} = -1mA$
I_{SC}	Short Circuit Output Current	−15		−75	mA	$V_O = 0V$
$\|I_O\|$	Output Leakage Current High Impedance State			20	μA	$V_O = 0.45V/5.25V$
I_{CC}	Power Supply Current		90	130	mA	

capacitance*

$F = 1MHz$, $V_{BIAS} = 2.5V$, $V_{CC} = +5V$, $T_A = 25°C$

Symbol	Test	Limits	
		Typ.	Max.
C_{IN}	DS_1, MD Input Capacitance	9pF	12pF
C_{IN}	DS_2, $\overline{CLR}$, STB, DI_1-DI_8 Input Capacitance	5pF	9pF
C_{OUT}	DO_1-DO_8 Output Capacitance	8pF	12pF

*This parameter is sampled and not 100% tested.

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ac electrical characteristics

$T_A = 0°C$ to $+75°C$, $V_{CC} = +5V \pm 5\%$

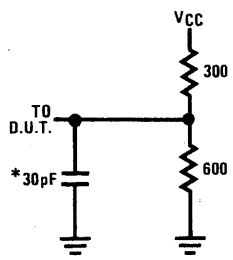
Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{PW}	Pulse Width	30			ns	
t_{PD}	Data to Output Delay			30	ns	
t_{WE}	Write Enable to Output Delay			40	ns	
t_{SET}	Data Setup Time	15			ns	
t_H	Data Hold Time	20			ns	
t_R	Reset to Output Delay			40	ns	
t_S	Set to Output Delay			30	ns	
t_E	Output Enable/Disable Time			45	ns	
t_C	Clear to Output Delay			55	ns	

switching characteristics

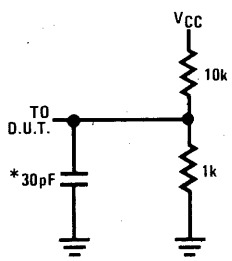
Conditions of Test:

1. Input Pulse Amplitude = 2.5V.
2. Input Rise and Fall Times = 5ns.
3. Between 1V and 2V Measurements made at 1.5V with 15mA & 30pF Test Load.

Test Load
15mA & 30pF

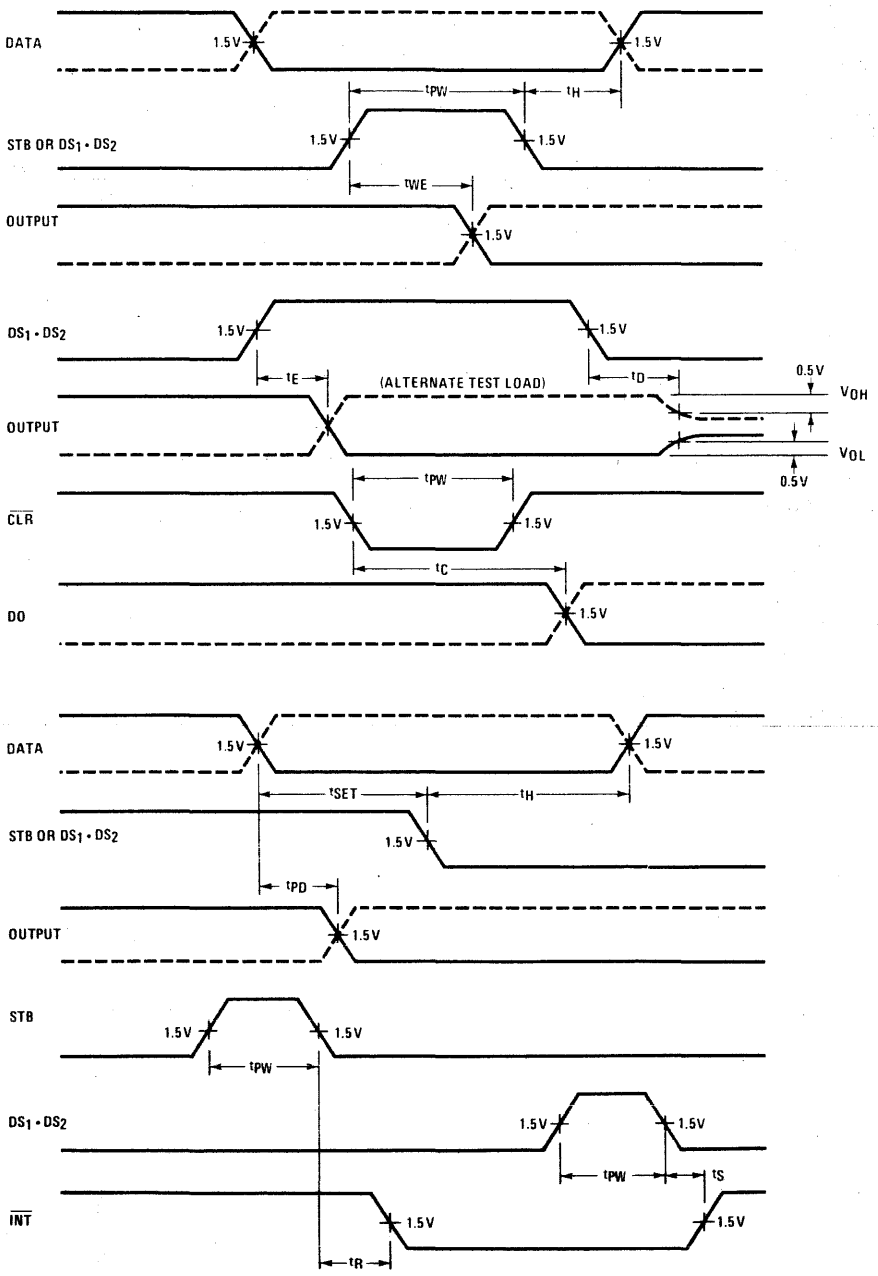


Alternate Test Load



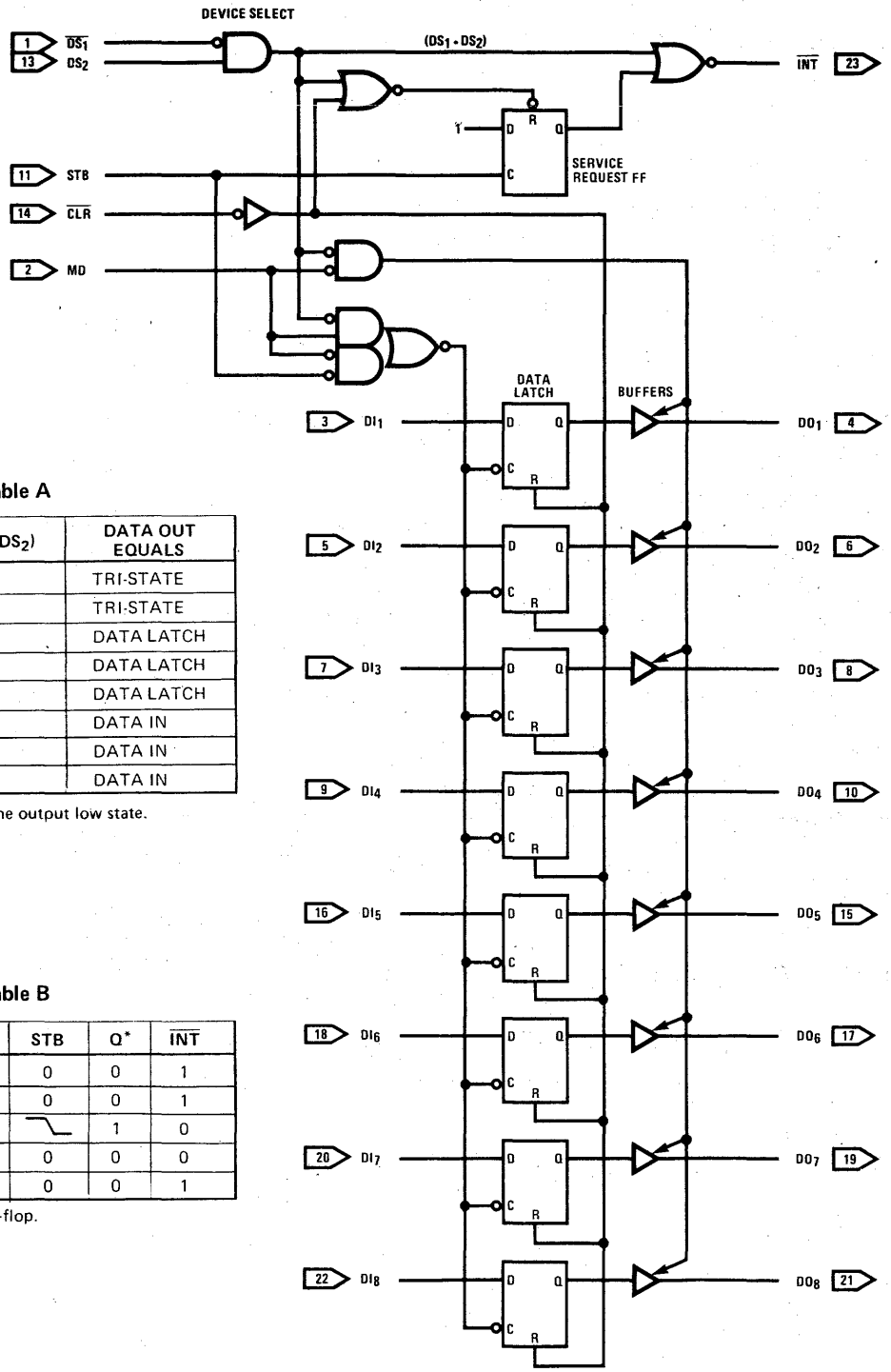
*including jig & probe capacitance

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DP8212 logic diagram



Logic Table A

STB	MD	$(DS_1 \cdot DS_2)$	DATA OUT EQUALS
0	0	0	TRI-STATE
1	0	0	TRI-STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

$\overline{CLR}$ ⌝ resets data latch to the output low state.

Logic Table B

$\overline{CLR}$	$(DS_1 \cdot DS_2)$	STB	Q*	$\overline{INT}$
0 RESET	0	0	0	1
1	0	0	0	1
1	0	⌝	1	0
1	1 RESET	0	0	0
1	0	0	0	1

*Internal Service Request flip-flop.

DP8212 functional pin definitions

The following describes the function of all the DP8212 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Device Select ($\overline{DS_1}$, DS_2): When $\overline{DS_1}$ is low and DS_2 is high, the device is selected. The output buffers are enabled and the service request flip-flop is asynchronously reset (cleared) when the device is selected.

Mode (MD): When high (output mode), the output buffers are enabled and the source of the data latch clock input is the device selection logic ($DS_1 \cdot DS_2$). When low (input mode), the state of the output buffers is determined by the device selection logic ($DS_1 \cdot DS_2$) and the source of the data latch clock input is the strobe (STB) input.

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DP8212 functional pin definitions (cont'd.)

Strobe (STB): Used as data latch clock input when the mode (MD) input is low (input mode). Also used to synchronously set the service request flip-flop, which is negative edge triggered.

Data In ($DI_1 - DI_8$): Eight-bit data input to the data latch, which consists of eight D-type flip-flops. While the data latch clock input is high, the Q output of each flip-flop follows the data input. When the clock input returns low, the data latch stores the data input. The clock input high overrides the clear ($\overline{CLR}$) input data latch reset.

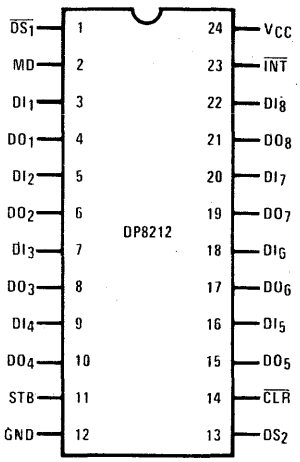
Clear ($\overline{CLR}$): When low, asynchronously resets (clears) the data latch and the service request flip-flop. The service request flip-flop is in the non-interrupting state when reset.

OUTPUT SIGNALS

Interrupt ($\overline{INT}$): Goes low (interrupting state) when either the service request flip-flop is synchronously set by the strobe (STB) input or the device is selected.

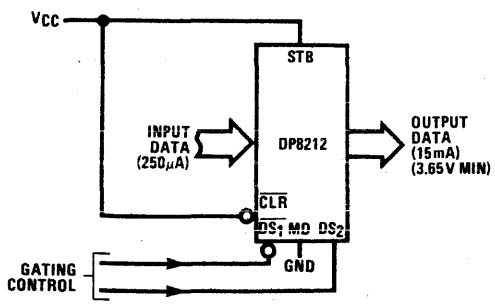
Data Out ($DO_1 - DO_8$): Eight-bit data output of data buffers, which are TRI-STATE, non-inverting stages. These buffers have a common control line that either enables the buffers to transmit the data from the data latch outputs or disables the buffers by placing them in the high-impedance state.

pin configuration

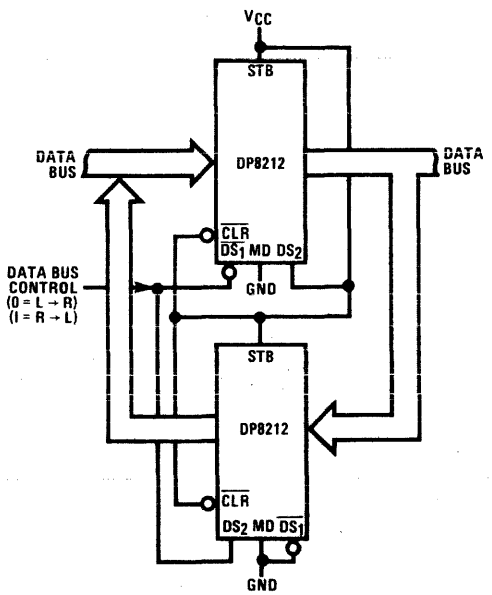


applications in microcomputer systems

Gated Buffer
(TRI-STATE)



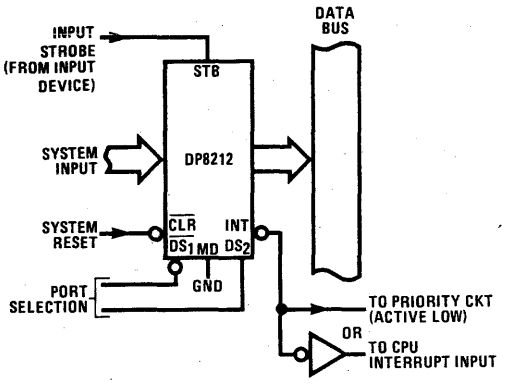
Bi-Directional Bus Driver



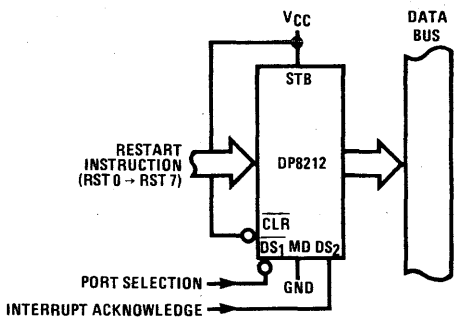
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applications in microcomputer systems (cont')

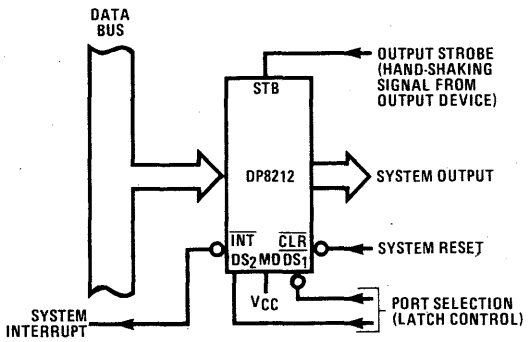
Interrupting Input Port



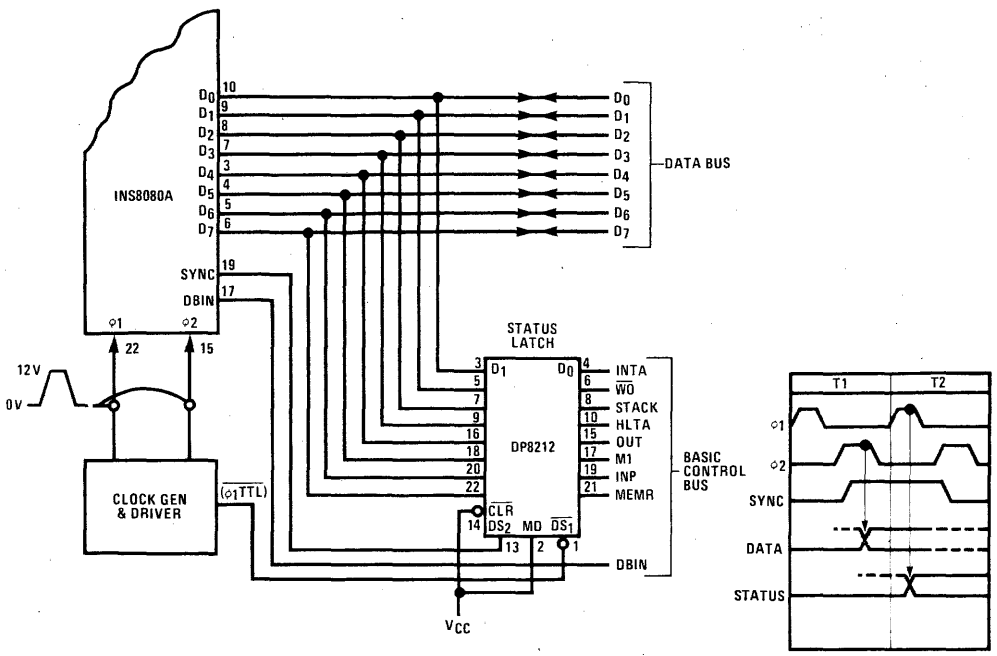
Interrupt Instruction Port



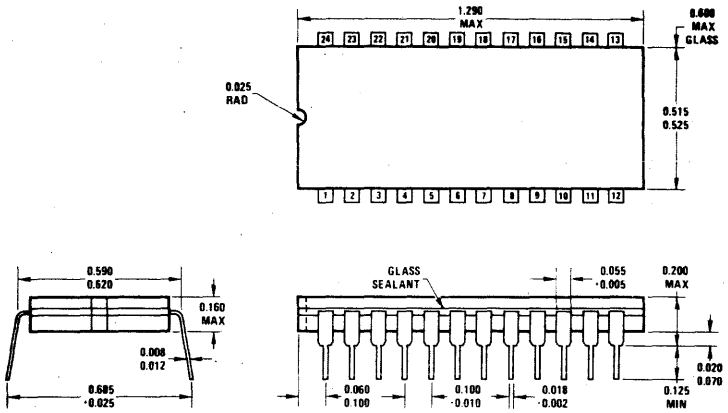
Output Port (with Hand-Shaking)



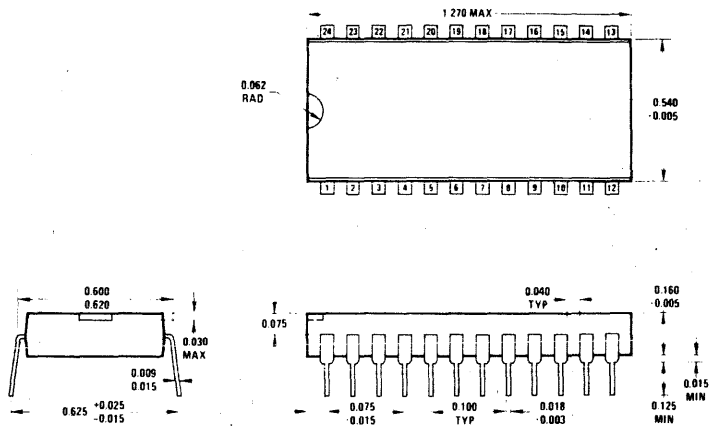
INS8080A Status Latch



physical dimensions



Ceramic Dual-in-Line Package (J)
Order Number DP8212J



Epoxy Dual-in-Line Package (N)
Order Number DP8212N

Manufactured under one or more of the following U.S. patents: 3383363, 3389758, 3231797, 3303356, 3317671, 3303071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571670, 3575609, 3579059, 3593094, 3597744, 3617469, 3617859, 3633211, 3633052, 3638131, 3648071, 3651565, 3693248.

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National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied, and National reserves the right, at any time without notice, to change said circuitry.

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National Semiconductor

DP8224 Clock Generator and Driver

general description

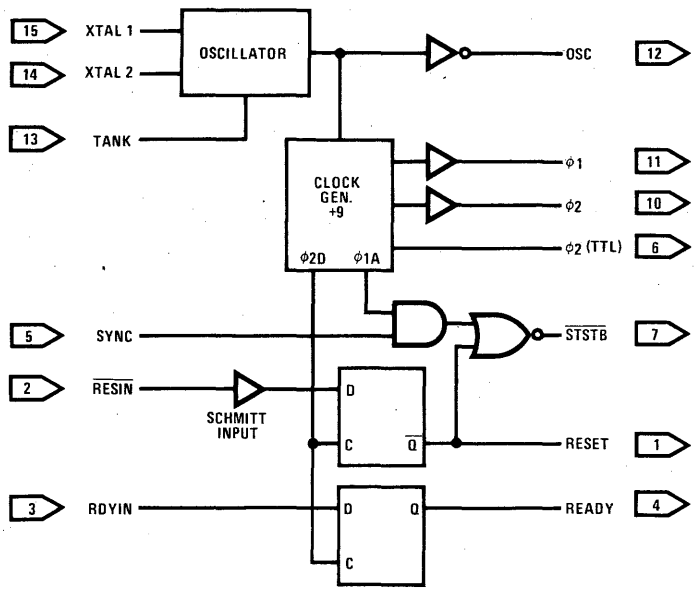
The DP8224 is a clock generator/driver contained in a standard, 16-pin dual-in-line package. The chip, which is fabricated using Schottky Bipolar technology, generates clocks and timing for National Semiconductor's N8080 microcomputer family.

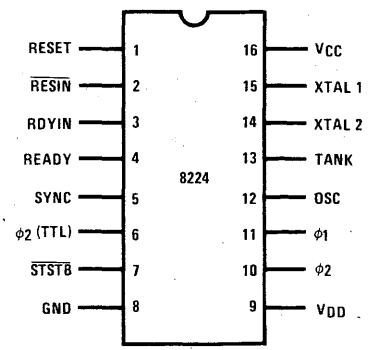
Included in the DP8224 is an oscillator circuit that is controlled by an external crystal, which is selected by the designer to meet a variety of system speed requirements. Also included in the chip are circuits that provide: a status strobe for the DP8228 or DP8238 system controllers, power-on reset for the INS8080A microprocessor, and synchronization of the READY input to the INS8080A.

features

- Crystal-Controlled Oscillator for Stable System Operation
- Single Chip Clock Generator and Driver for INS8080A Microprocessor
- Provides Status Strobe for DP8228 or DP8238 System Controllers
- Provides Power-On Reset for INS8080A Microprocessor
- Synchronizes READY Input to INS8080A Microprocessor
- Provides Oscillator Output for Synchronization of External Circuits
- Reduces System Component Count

logic diagram and pin configuration





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absolute maximum ratings (NOTE 2)

Supply Voltage, V_{CC} . . . . . 7 V
V_{DD} . . . . . 15 V
Input Voltage . . . . . −1.0 V to +5.5 V
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

operating conditions

	Min.	Max.	Units
Supply Voltage			
V_{CC}	4.75	5.25	V
V_{DD}	11.4	12.6	V
Temperature	0	70	°C

dc electrical characteristics

T_A = 0°C to +70°C; V_{CC} = +5.0 V ± 5%; V_{DD} = +12 V ± 5%.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Current Loading			−0.25	mA	V_F = 0.45 V
I_R	Input Leakage Current			10	μA	V_R = 5.25 V
V_C	Input Forward Clamp Voltage			1.0	V	I_C = −5 mA
V_{IL}	Input "Low" Voltage			0.8	V	V_{CC} = 5.0 V
V_{IH}	Input "High" Voltage	2.6 2.0			V V	$\overline{RESIN}$ Input All Other Inputs
V_{IH} - V_{IL}	$\overline{RESIN}$ Input Hysteresis	0.25			V	V_{CC} = 5.0 V
V_{OL}	Output "Low" Voltage			0.45 0.45	V V	(ϕ_1, ϕ_2), Ready, Reset, $\overline{STSTB}$ I_{OL} = 2.5 mA All Other Outputs I_{OL} = 15 mA
V_{OH}	Output "High" Voltage ϕ_1, ϕ_2 READY, RESET All Other Outputs	 9.4 3.6 2.4			 V V V	 I_{OH} = −100 μA I_{OH} = −100 μA I_{OH} = −1 mA
I_{SC}[1]	Output Short Circuit Current (All Low Voltage Outputs Only)	−10		−60	mA	V_O = 0 V V_{CC} = 5.0 V
I_{CC}	Power Supply Current			115	mA	
I_{DD}	Power Supply Current			12	mA	

Notes:
1. Caution — ϕ_1 and ϕ_2 output drivers do not have short circuit protection.
2. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

crystal requirements

Tolerance . . . . . 0.005% at 0°C to +70°C
Resonance . . . . . Series (Fundamental)*
Load Capacitance . . . . . 20 pF to 30 pF
Equivalent Resistance . . . . . 75 Ω to 20 Ω
Power Dissipation (min) . . . . . 4 mW

*With tank circuit use 3rd overtone mode.

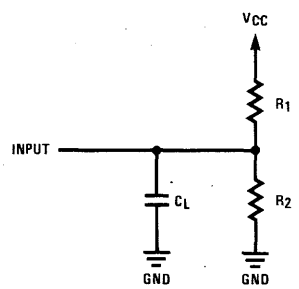
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ac electrical charicteristics

$T_A = 0°C$ to $+70°C$; $V_{CC} = +5.0\ V \pm 5\%$; $V_{DD} = +12\ V \pm 5\%$.

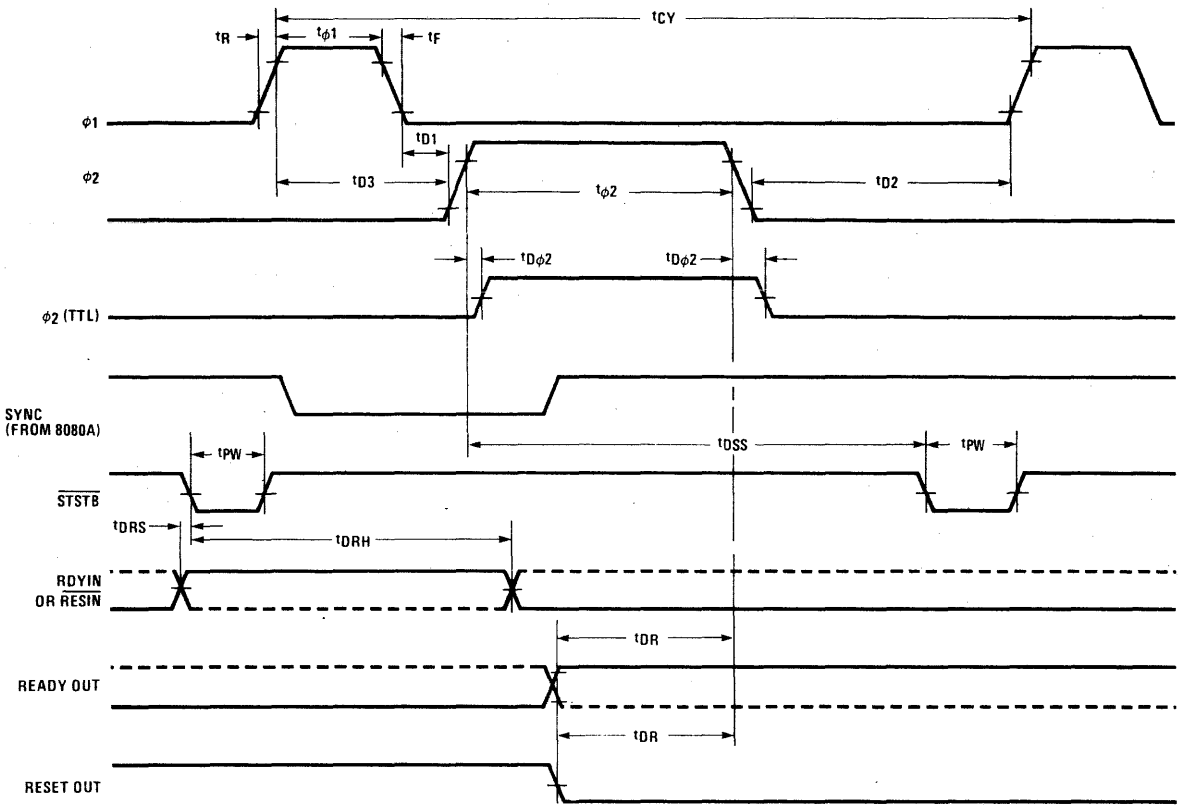
Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{\phi 1}$	ϕ_1 Pulse Width	$\frac{2t_{CY}}{9} - 20$ ns			ns	$C_L = 20$ pF to 50 pF
$t_{\phi 2}$	ϕ_2 Pulse Width	$\frac{5t_{CY}}{9} - 35$ ns				
t_{D1}	ϕ_1 to ϕ_2 Delay	0				
t_{D2}	ϕ_2 to ϕ_1 Delay	$\frac{2t_{CY}}{9} - 14$ ns				
t_{D3}	ϕ_1 to ϕ_2 Delay	$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9} + 20$ ns		
t_R	ϕ_1 and ϕ_2 Rise Time			20		
t_F	ϕ_1 and ϕ_2 Fall Time			20		
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	−5		+15	ns	ϕ_2 TTL, $C_L = 30$ pF $R_1 = 300\ \Omega$ $R_2 = 600\ \Omega$
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\frac{6t_{CY}}{9} - 30$ ns		$\frac{6t_{CY}}{9}$		$\overline{STSTB}$, $C_L = 15$ pF $R_1 = 2\ k\Omega$ $R_2 = 4\ k\Omega$
t_{PW}	$\overline{STSTB}$ Pulse Width	$\frac{t_{CY}}{9} - 15$ ns				
t_{DRS}	RDYIN Setup Time to Status Strobe	$50\ ns - \frac{4t_{CY}}{9}$				
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$	$\frac{4t_{CY}}{9}$				
t_{DR}	READY or RESET to ϕ_2 Delay	$\frac{4t_{CY}}{9} - 25$ ns				Ready & Reset $C_L = 10$ pF $R_1 = 2\ k\Omega$ $R_2 = 4\ k\Omega$
t_{CLK}	CLK Period		$\frac{t_{CY}}{9}$			
f_{MAX}	Maximum Oscillating Frequency	27			MHz	
C_{IN}	Input Capacitance			8	pF	$V_{CC} = +5.0$ V $V_{DD} = +12$ V $V_{BIAS} = 2.5$ V f = 1 MHz

test circuit



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waveforms



VOLTAGE MEASUREMENT POINTS: ϕ_1, ϕ_2 Logic "0" = 1.0 V, Logic "1" = 8.0 V. All other signals measured at 1.5 V.

ac electrical charicteristics (For t_{CY} = 488.28 ns)

$T_A = 0°C$ to $+70°C$; $V_{CC} = +5.0\ V \pm 5\%$; $V_{DD} = +12\ V \pm 5\%$.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{\phi1}$	ϕ_1 Pulse Width	89			ns	t_{CY} = 488.28 ns
$t_{\phi2}$	ϕ_2 Pulse Width	236			ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0			ns	
t_{D2}	Delay ϕ_2 to ϕ_1	95			ns	ϕ_1 & ϕ_2 Loaded to C_L = 20 to 50 pF
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	109		129	ns	
t_r	Output Rise Time			20	ns	
t_f	Output Fall Time			20	ns	
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	296		326	ns	
$t_{D\phi2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	
t_{PW}	Status Strobe Pulse Width	40			ns	
t_{DRS}	RDYIN Setup Time to $\overline{STSTB}$	-167			ns	Ready & Reset Loaded to 2 mA/10 pF
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$	217			ns	All measurements referenced to 1.5 V unless specified otherwise.
t_{DR}	READY or RESET to ϕ_2 Delay	192			ns	
f_{MAX}	Oscillator Frequency			18.432	MHz	

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DP8224 functional pin definitions

The following describes the function of all of the DP8224 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Crystal Connections (XTAL 1 and XTAL 2): Two inputs that connect an external, series resonant, crystal to the oscillator circuit of the DP8224. Normally, a fundamental mode crystal is used to determine the basic operating frequency of the oscillator. However, overtone mode crystals may also be used. The crystal frequency is nine times the desired microprocessor speed (that is, crystal frequency = $1/t_{CY} \times 9$). When the crystal frequency is above 10 MHz, a selected capacitor (3 to 10 picofarads) may have to be connected in series with the crystal to produce the exact desired frequency.

Tank: Allows the use of overtone mode crystals with the oscillator circuit. When an overtone mode crystal is used, the tank input connects to a parallel LC network that is ac coupled to ground. The formula for determining the resonant frequency of this LC network is as follows:

$$F = \frac{1}{2\pi\sqrt{LC}}$$

Synchronizing (SYNC) Signal: When high, indicates the beginning of a new machine cycle. The INS8080A microprocessor outputs a status word (which describes the current machine cycle) onto its data bus during the first state (SYNC interval) of each machine cycle.

Reset In ($\overline{\text{RESIN}}$): Provides an automatic system reset and start-up upon application of power as follows. The $\overline{\text{RESIN}}$ input, which is obtained from the junction of an external RC network that is connected between V_{CC} and ground, is routed to an internal Schmitt Trigger circuit. This circuit converts the slow transition of the power supply rise into a sharp, clean edge when its input reaches a predetermined value. When this occurs, an internal D-type flip-flop is synchronously reset, thereby providing the RESET output signal discussed below.

For manual system reset, a momentary contact switch that provides a low (ground) when closed is also connected to the $\overline{\text{RESIN}}$ input.

Ready In (RDYIN): An asynchronous READY signal that is re-clocked by a D-type flip-flop of the DP8224 to provide the synchronous READY output discussed below.

+5 Volts: V_{CC} supply.

+12 Volts: V_{DD} supply.

Ground: 0 volt reference.

OUTPUT SIGNALS

Oscillator (OSC): A buffered oscillator signal that can be used for external timing purposes.

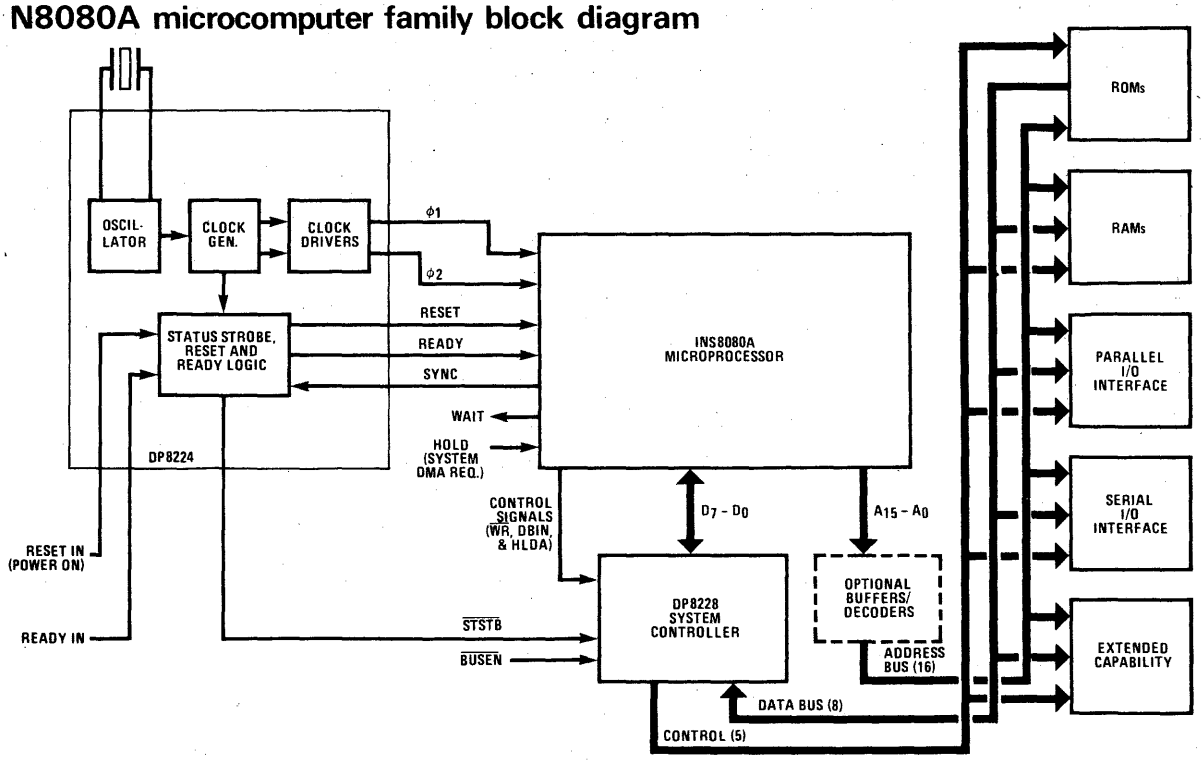
ϕ_1 and ϕ_2 Clocks: Two non-TTL compatible clock phases that provide nonoverlapping timing references for internal storage elements and logic circuits of the INS8080A microprocessor. The two clock phases are produced by an internal clock generator that consists of a divide-by-nine counter and the associated decode gating logic.

ϕ_2 (TTL) Clock: A TTL ϕ_2 clock phase that can be used for external timing purposes.

Status Strobe ($\overline{\text{STSTB}}$): Activated (low) at the start of each new machine cycle. The $\overline{\text{STSTB}}$ signal is generated by gating a high-level SYNC input with the ϕ_{1A} timing signal from the internal clock generator of the DP8224. The $\overline{\text{STSTB}}$ signal is used to clock status information into the status latch of the DP8228 system controller and bus driver.

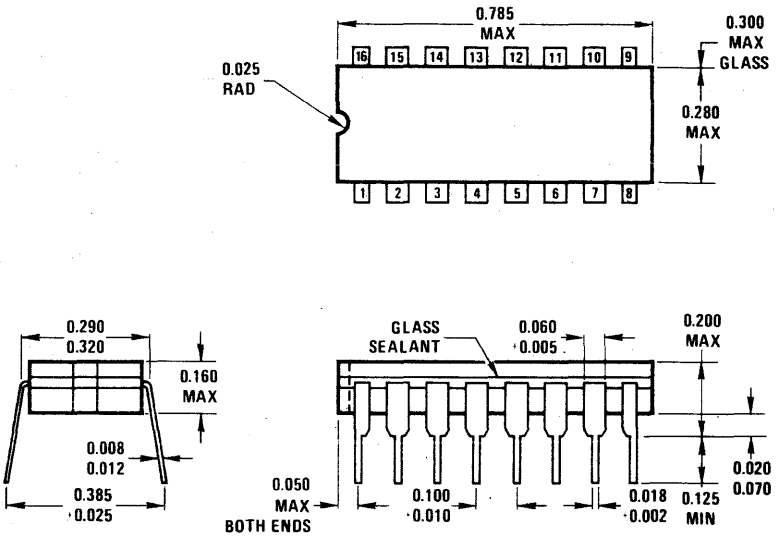
The power-on reset $\overline{\text{RESIN}}$ input also generates a $\overline{\text{STSTB}}$ signal. However, since this signal lasts for a longer duration, it is used to reset the status latch of the DP8228.

N8080A microcomputer family block diagram

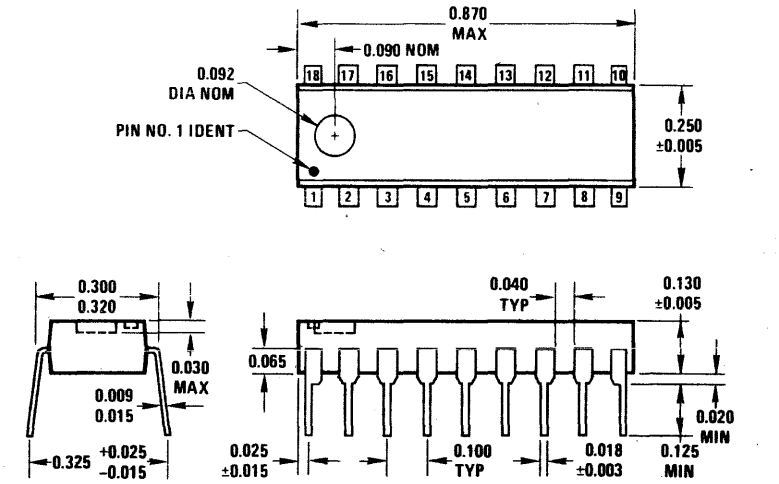


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physical dimensions



Order Number 8224(J)



Order Number 8224(N)

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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National Semiconductor

DP8228/DP8238 system controller and bus driver

general description

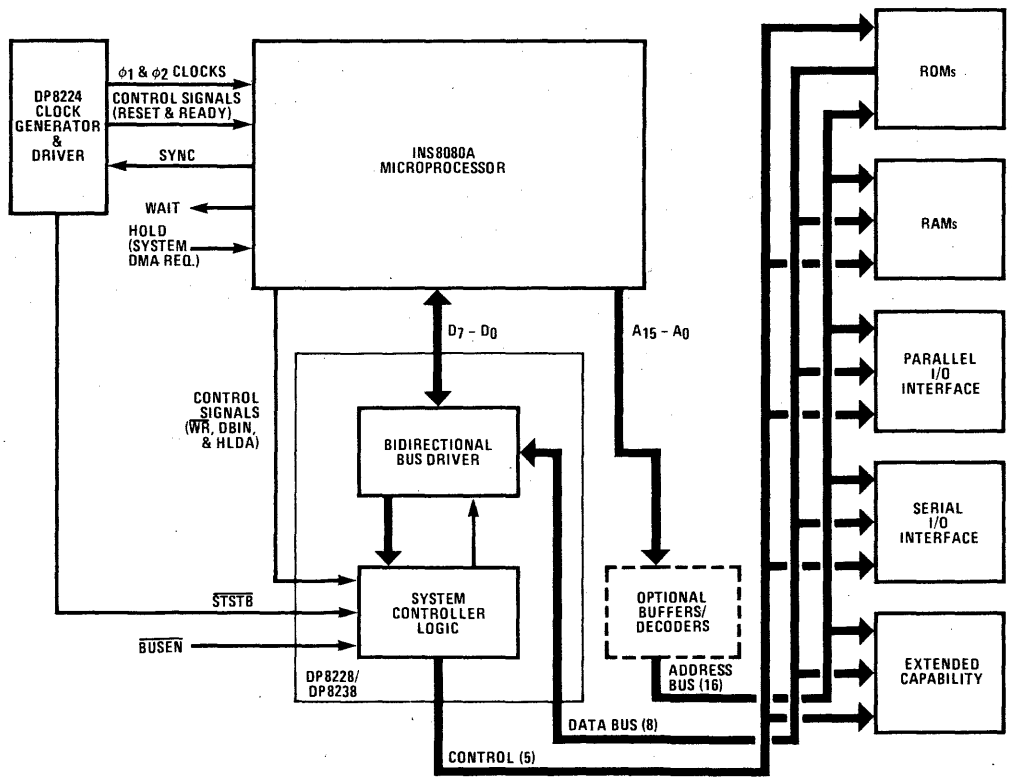
The DP8228/DP8238 is a system controller/bus driver contained in a standard, 28-pin dual-in-line package. The chip, which is fabricated using Schottky Bipolar technology, generates all the read and write control signals required to directly interface the memory and input/output components of National Semiconductor's INS8080A microcomputer family. The chip also provides drive and isolation for the bidirectional data bus of the INS8080A microprocessor. Data bus isolation enables the use of slower memory and input/output components in a system, and provides for enhanced system noise immunity.

A user-selected single-level interrupt vector (RST 7) is provided by the chip for use in the interrupt structure of small systems that need only one basic vector. No additional components (such as an interrupt instruction port) are required to use the single interrupt vector in these systems. The DP8228/DP8238 also generates an Interrupt Acknowledge ($\overline{INTA}$) control signal for each byte of a multibyte CALL instruction when an interrupt is acknowledged by the INS8080A. This feature permits the use of a multilevel priority interrupt structure in large, interrupt-driven systems.

features

- Single Chip System Controller and Bus Driver for INS8080A Microcomputer Systems
- Allows Use of Multibyte CALL Instructions for Interrupt Acknowledge
- Provides User-Selected Single-Level Interrupt Vector (RST 7)
- Provides Isolation for Data Bus
- Supports A Wide Variety of System Bus Structures
- Reduces System Component Count
- DP8238 Provides Advanced Input/Output Write and Memory Write Control Signals for Large System Timing Control

N8080A microcomputer family block diagram



absolute maximum ratings

Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . -65°C to +150°C
Supply Voltage, V_{CC} . . . . . -0.5 V to +7 V
Input Voltage . . . . . -1.5 V to +7 V
Output Current . . . . . 100 mA

dc electrical characteristics

T_A = 0°C to +70°C; V_{CC} = 5 V ± 5%.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.[1]	Max.		
V_C	Input Clamp Voltage, All Inputs		0.75	-1.0	V	V_{CC} = 4.75 V; I_C = -5 mA
I_F	Input Load Current					
	$\overline{STSTB}$			500	μA	V_{CC} = 5.25 V
	D_2 & D_6			750	μA	V_F = 0.45 V
	D_0, D_1, D_4, D_5, & D_7			250	μA	
	All Other Inputs			250	μA	
I_R	Input Leakage Current					
	$\overline{STSTB}$			100	μA	V_{CC} = 5.25 V
	DB_0 - DB_7			20	μA	V_R = 5.25 V
	All Other Inputs			100	μA	
V_{TH}	Input Threshold Voltage, All Inputs	0.8		2.0	V	V_{CC} = 5 V
I_{CC}	Power Supply Current		140	190	mA	V_{CC} = 5.25 V
V_{OL}	Output Low Voltage					
	D_0 - D_7			0.45	V	V_{CC} = 4.75 V; I_{OL} = 2 mA
	All Other Outputs			0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage					
	D_0 - D_7	3.6	3.8		V	V_{CC} = 4.75 V; I_{OH} = -10 μA
	All Other Outputs	2.4			V	I_{OH} = -1 mA
I_{OS}	Short Circuit Current, All Outputs	15		90	mA	V_{CC} = 5 V
$I_{O\,(off)}$	Off State Output Current			100	μA	V_{CC} = 5.25 V; V_O = 5.25 V
	All Control Outputs			-100	μA	V_O = 0.45 V
I_{INT}	INTA Current			5	mA	(See Test Conditions—Pg. 3)

Notes:
1. Typical values are for T_A = 25°C and nominal supply voltages.

capacitance

This parameter is periodically sampled and not 100% tested.

Symbol	Parameter	Limits			Units
		Min.	Typ.[1]	Max.	
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

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ac electrical characteristics

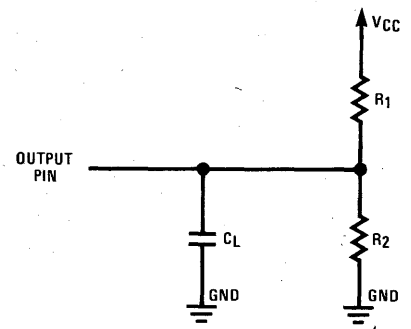
$T_A = 0°C$ to $+70°C$; $V_{CC} = 5\ V \pm 5\%$.

Symbol	Parameter	Limits		Units	Condition
		Min.	Max.		
t_{PW}	Width of Status Strobe	22		ns	
t_{SS}	Setup Time, Status Inputs D_0 - D_7	8		ns	
t_{SH}	Hold Time, Status Inputs D_0 - D_7	5		ns	
t_{DC}	Delay from $\overline{STSTB}$ to any Control Signal	20	60	ns	$C_L = 100$ pF
t_{RR}	Delay from DBIN to Control Outputs		30	ns	$C_L = 100$ pF
t_{RE}	Delay from DBIN to Enable/Disable 8080 Bus		45	ns	$C_L = 25$ pF
t_{RD}	Delay from System Bus to 8080 Bus during Read		30	ns	$C_L = 25$ pF
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	5	45	ns	$C_L = 100$ pF
t_{WE}	Delay to Enable System Bus DB_0 - DB_7 after $\overline{STSTB}$		30	ns	$C_L = 100$ pF
t_{WD}	Delay from 8080 Bus D_0 - D_7 to System Bus DB_0 - DB_7 during Write	5	40	ns	$C_L = 100$ pF
t_E	Delay from System Bus Enable to System Bus DB_0 - DB_7		30	ns	$C_L = 100$ pF
t_{HD}	HLDA to Read Status Outputs		25	ns	$C_L = 100$ pF
t_{DS}	Setup Time, System Bus Inputs to HLDA	10		ns	
t_{DH}	Hold Time, System Bus Inputs to HLDA	20		ns	

test conditions

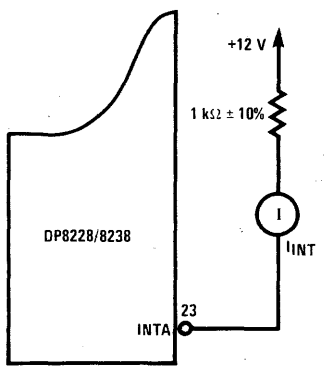
$V_{BIAS} = 2.5\ V$, $V_{CC} = 5.0\ V$, $T_A = 25°C$, f = 1 MHz.

Test Load[2]



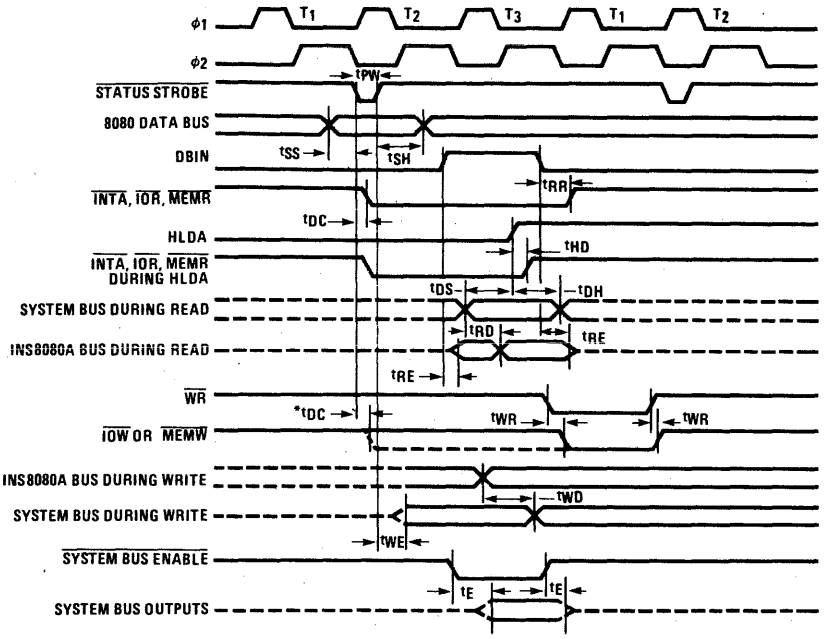
2. For D_0 - D_7: $R_1 = 4\ k\Omega$, $R_2 = \infty$, $C_L = 25$ pF. For all other outputs: $R_1 = 500\ \Omega$, $R_2 = 1\ k\Omega$, $C_L = 100$ pF.

INTA Test Circuit (for RST 7)



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waveforms



VOLTAGE MEASUREMENT POINTS: D_0 - D_7 (when outputs) Logic "0" = 0.8 V, Logic "1" = 3.0 V. All other signals measured at 1.5 V.

*Advanced $\overline{I/OW}$ $\overline{MEMW}$ for 8238 only.

DP8228/DP8238 functional pin definitions

The following describes the function of all of the DP8228/DP8238 pinouts. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Status Strobe ($\overline{STSTB}$): Activated (low) at the start of each new machine cycle. The $\overline{STSTB}$ input is used to store a status word (refer to chart) from the INS8080A microprocessor into the internal status latch of the DP8228/DP8238. The INS8080A outputs this status word onto its data bus during the first state (SYNC interval) of each machine cycle.

Data Bus In (DBIN): When high, indicates that the INS8080A data bus is in the input mode. The DBIN signal is used to gate data from memory or an input/output device onto the data bus.

Write ($\overline{WR}$): When low, indicates that the data on the INS8080A data bus are stable for WRITE memory or output operation.

Hold Acknowledge (HLDA): When high, indicates that the INS8080A data and address buses will go to their high impedance state. When in the data bus read mode, DBIN input in the high state, a high HLDA input will latch the data bus information into the driver circuits and gate off the applicable control signal $\overline{I/OR}$, $\overline{MEMR}$, or $\overline{INTA}$ (return to the output high state).

Bus Enable ($\overline{BUSEN}$): Asynchronous DMA input to the internal gating array of the DP8228/DP8238. When low, normal operation of the internal bidirectional bus driver and gating array occurs. When high, the bus driver and gating array are driven to their high impedance state.

V_{CC} Supply: +5 volts.

Ground: 0 volt reference.

OUTPUT SIGNALS

Memory Read ($\overline{MEMR}$): When low, signals data to be loaded in from memory. The $\overline{MEMR}$ signal is generated by strobing in status word 1, 2, or 4. (Refer to status word chart.)

Memory Write ($\overline{MEMW}$): When low, signals data to be stored in memory. The $\overline{MEMW}$ signal is generated for the DP8238 by strobing in status word 3 or 5. (Refer to status word chart.) For the DP8228, the $\overline{MEMW}$ signal is generated by gating a low-level $\overline{WR}$ input with the strobed in status word 3 or 5.

Input/Output Read ($\overline{I/OR}$): When low, signals data to be loaded in from an addressed input/output device. The $\overline{I/OR}$ signal is generated by strobing in status word 6.

Input/Output Write ($\overline{I/OW}$): When low, signals data to be transferred to an addressed input/output device. The I/OW signal for the DP8238 is generated by strobing in status word 7. For the DP8228 the $\overline{I/OW}$ signal is generated by gating in a low-level WR input with the strobed in status word 7.

Interrupt Acknowledge ($\overline{INTA}$): When low, indicates that an interrupt has been acknowledged by the INS8080A microprocessor. The $\overline{INTA}$ signal is generated by strobing in status word 8 or 10.

Single Level Interrupt (RST 7): When the $\overline{INTA}$ output is tied to 12 V through a 1 kΩ resistor, strobing in status work 8 or 10 will cause the CPU data bus outputs, when active, to go to the high state.

INPUT/OUTPUT SIGNALS

CPU Data (D_7 - D_0) Bus: This bus comprises eight TRI-STATE input/output lines that connect to the INS8080A microprocessor. The bus provides bidirec-

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DP8228/DP8238 functional pin definitions (con'd.)

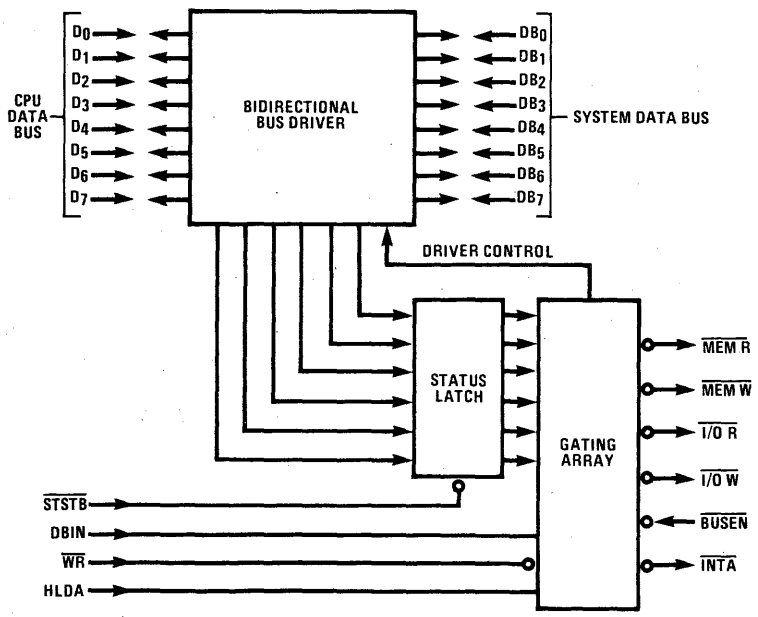
tional communication between the CPU, memory, and input/output devices for instructions and data transfers. A status word (which describes the current machine cycle) is also outputted on this data bus during the first microcycle of each machine cycle (SYNC = logic 1).

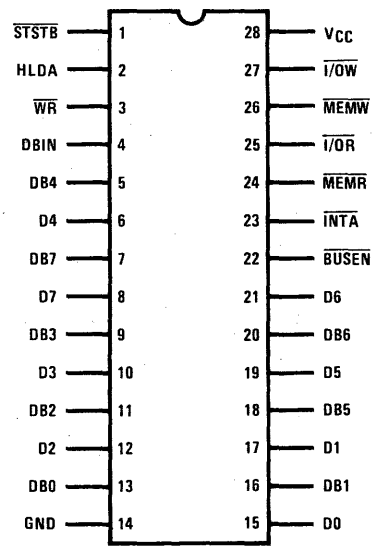
System Data (DB_7 - DB_0) Bus: This bus comprises eight TRI-STATE input/output lines that connect to the memory and input/output components of the system. The internal bidirectional bus driver isolates the DB_7 - DB_0 Data Bus from the D_7 - D_0 Data Bus.

Status Word Chart

Machine Cycle	Status Word	Data Bus Bit								Control Signal
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Instruction Fetch	1	1	0	1	0	0	0	1	0	$\overline{MEMR}$
Memory Read	2	1	0	0	0	0	0	1	0	$\overline{MEMR}$
Memory Write	3	0	0	0	0	0	0	0	0	$\overline{MEMW}$
Stack Read	4	1	0	0	0	0	1	1	0	$\overline{MEMR}$
Stack Write	5	0	0	0	0	0	1	0	0	$\overline{MEMW}$
Input Read	6	0	1	0	0	0	0	1	0	$\overline{I/OR}$
Output Write	7	0	0	0	1	0	0	0	0	$\overline{I/OW}$
Interrupt Acknowledge	8	0	0	1	0	0	0	1	1	$\overline{INTA}$
Halt Acknowledge	9	1	0	0	0	1	0	1	0	(none)
Interrupt Acknowledge While Halt	10	0	0	1	0	1	0	1	1	$\overline{INTA}$

DP8228/DP8238 block diagram and pin configuration





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DP8300 PACE bidirectional transceiver element (PACE BTE/8)

general description

The DP8300 is an 8-bit TRI-STATE® MOS/TTL bus transceiver element specifically intended for application in PACE microprocessor-based systems. Its electrical characteristics and control flexibility make the BTE/8 attractive in other applications requiring the translation of MOS current outputs to high fan-out TTL levels.

Two BTE/8 devices provide complete system buffering for all 16-bit address and data input/output between the PACE CPU and all system memory and peripheral interfaces.

In the driving mode, the MOS sense amplifiers convert the MOS current outputs of the PACE CPU to a fan-out 30 (50 mA) TTL system bus. [This characteristic makes the BTE/8 an ideal buffer (driving mode only) for the PACE system timing and control bus consisting of the address data strobe (NADS), input data strobe (IDS), output data strobe (ODS) and the four output control flags (F11, F12, F13, F14).]

In the receiving mode the BTE accepts bus data through high impedance input buffers and applies the TTL signals to the PACE I/O pins.

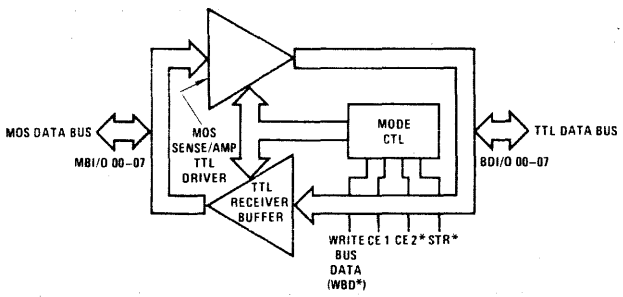
A third mode allows both the MOS and TTL bus to be placed in the TRI-STATE (high impedance) mode. This function facilitates direct memory access (DMA) over the TTL system bus.

A latched chip enable allows the use of multiplexed address/data lines to drive CE 1 and CE 2*, selecting the BTE/8 for an input cycle. The latching function may be eliminated by connecting the strobe to ground.

features

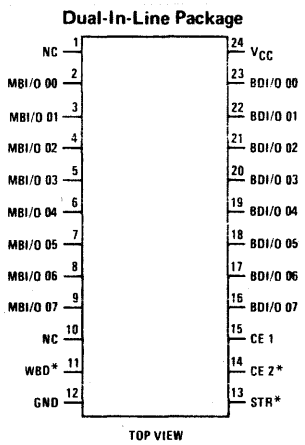
- High TTL fan-out eliminates additional buffering requirements
- Low system data bus loading for minimum input drive
- TRI-STATE data ports and chip enables maximize application flexibility
- 8-bit parallel data flow reduces system package count
- Pin-outs are compatible with hybrid version and simplify system interconnections and layout
- Latched chip enable simplifies transmit/receive control
- High voltage output high level (V_{CC} − 1.1V) on TTL bus

block diagram

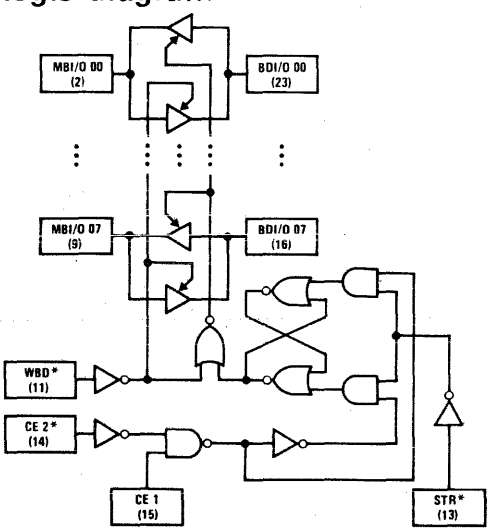


Signal* = N Signal = $\overline{\text{Signal}}$ = Low Active Signal

connection diagram



logic diagram



truth table

t_n			$t_n + 1$	
CE 1	CE 2*	STR*	WBD*	TRANSCEIVER MODE
X	X	X	0	Receiving MOS Bus and Driving TTL Bus
X	X	1	1	Mode t_n: See Note 1
0	0	0	1	TRI-STATE Mode
0	1	0	1	TRI-STATE Mode
1	0	0	1	Receiving TTL Bus and Driving MOS Bus
1	1	0	1	TRI-STATE Mode

Note 1. On the positive-edge transition of STR* logic conditions present on CE 1 and CE 2* at the time of transition will be latched internally. The transceiver will either be in the TRI-STATE or receiving mode.

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absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage (All Inputs Except MBI/O Input Active)	5.5V
Output Voltage	5.5V
MOS Bus Input Current	±10 mA
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	+70	°C

dc electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
TTL BUS PORT (BDI/O 00–07)							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
V_{OH}	Logical "1" Output Voltage	WBD* = 0.8V, MBI/O = 0.5 mA	I_{OH} = −1 mA	V_{CC}−1.1	V_{CC}−0.8		V
			I_{OH} = −5.2 mA	2.4	3.7		V
V_{OL}	Logical "0" Output Voltage	WBD* = 0.8V, MBI/O = 100μA	I_{OL} = 20 mA		0.25	0.4	V
			I_{OL} = 50 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	WBD* = 0.8V, MBI/O = 0.5 mA, V_{OUT} = 0V, V_{CC} = 5.25V, (Note 4)		−10	−35	−75	mA
I_{IH}	Logical "1" Input Current	WBD* = 2V, V_{IH} = 2.4V				80	μA
I_I	Input Current at Maximum Input Voltage	WBD* = 2V, V_{IH} = 5.5V, V_{CC} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	WBD* = 2V, V_{IL} = 0.4V			−10	−250	μA
V_{CLAMP}	Input Clamp Voltage	WBD* = 2V, I_{IN} = −12 mA			−0.2	−1.5	V
I_{OD}	Output/Input Bus Disable Current	WBD* = STR* = 2V, BDI/O = 0.4V to 4V, V_{CC} = 5.25V		−80		80	μA
MOS BUS PORT (MBI/O 00–07)							
I_0	Logical "0" Input Current	WBD* = 0.8V, $I_{OL(TTL)}$ = 50 mA, $V_{OL} \leq$ 0.5V, (Note 5)		−5.0		0.10	mA
I_1	Logical "1" Input Current	WBD* = 0.8V, $I_{OH(TTL)}$ = −1 mA, $V_{OH} \geq V_{CC}$ − 1.1V, (Notes 5 and 6)		0.50		5.0	mA
V_0	Logical "0" Input Voltage	WBD* = 0.8V, $I_{OL(TTL)}$ = 50 mA, $V_{OL} \leq$ 0.5V				0.8	V
V_1	Logical "1" Input Voltage	WBD* = 0.8V, $I_{OH(TTL)}$ = −1 mA, $V_{OH} \geq V_{CC}$ − 1.1V		2.0	1.5		V
V_{OH}	Logical "1" Output Voltage	WBD* = CE1 = BDI/O = 2V, $I_{OH(MOS)}$ = −1 mA, CE2* = STR* = 0.8V		2.4	3.3		V
V_{OL}	Logical "0" Output Voltage	WBD* = CE1 = 2V, $I_{OL(MOS)}$ = 5 mA, CE2* = STR* = BDI/O = 0.8V			0.28	0.5	V
I_{OS}	Output Short Circuit Current	WBD* = CE1 = BDI/O = 2V, V_{CC} = 5.25V, V_{OUT} = 0V, STR* = CE2* = 0.8V, (Note 4)		−7	−15	−45	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA				−1.5	V
I_{OD}	Output/Input Bus Disable Current	MBI/O = 0.4V to 4V, V_{CC} = 5.25V		−80		80	μA
CONTROL INPUTS (WBD*, CE1, CE2*, STR*)							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V				20	μA
I_1	Input Current at Maximum Input Voltage	V_{IN} = 5.5V				1.0	mA

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dc electrical characteristics (Continued) (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL INPUTS (WBD*, CE1, CE2*, STR*) (continued)						
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V		−250	−400	μA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA		−0.85	−1.5	V
POWER SUPPLY CURRENT						
I_{CC}	Power Supply Current	V_{CC} = 5.25V		70	110	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are shown as positive, out of device pins are negative. All voltages are referenced to ground unless otherwise noted.

Note 4: Only one output at a time should be shorted.

Note 5: The MBI/O Input Characteristic Graph illustrates this parameter and defines the regions of guaranteed logical "0" and logical "1" outputs. See equivalent input structure for clarification. When the MBI/O input is loaded with a high impedance source (open), the TTL output will be in the logic "0" state.

Note 6: The maximum MOS bus positive input current specification is intended to define the upper limit on guaranteed input clamp operation. At higher input currents (up to the absolute maximum rating) clamp operation is not guaranteed but TTL bus logic state is valid and no device damage will occur.

Note 7: In most applications the MOS bus data lines are higher impedance and more sensitive to noise coupling than TTL bus lines. Conservative design practice would dictate routing MOS bus lines away from high speed, low impedance TTL lines and MOS clock lines or providing a ground shield when they are adjacent.

ac electrical characteristics V_{CC} = 5V ±5%, T_A = 0°C to +70°C

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
DATA TRANSFER SPECIFICATIONS							
Receiving Mode (BDI/O Bus to MBI/O Bus)		WBD* = 3V, C_L = 15 pF,	t_{pd0}		17	40	ns
		R_L = 1 kΩ, *(Figures 4 and 6)*	t_{pd1}		20	40	ns
	Driving Mode (MBI/O Bus to BDI/O Bus)	WBD* = CE1 = 0V,	t_{pd0}		40	60	ns
		STR* = CE2* = 3V,	t_{pd1}		40	60	ns
		C_L = 50 pF, R_L = 100 Ω, *(Figures 3 and 5)*					
TRANSCEIVER MODE SPECIFICATIONS							
Select Bus							
t_{DS}	Chip Enable Data Set-Up	*(Figure 1)*		45	23		ns
t_{DH}	Chip Enable Data Hold	*(Figure 1)*		0			ns
t_{ES}	Set-Up	*(Figure 1)*		0			ns
TTL Data Bus (BDI/O 00–07)							
$t_{BD\ OD}$	Bus Data Output Disable	C_L = 5 pF, R_L = 100 Ω, *(Figure 1)*		5	20	50	ns
$t_{BD\ OE}$	Bus Data Output Enable	C_L = 50 pF, R_L = 100 Ω, *(Figure 1)*			25	80	ns
$t_{BD\ IE}$	Bus Data Input Enable	*(Figure 1)*			30		ns
$t_{BD\ ID}$	Bus Data Input Disable	*(Figure 1)*			30		ns
MOS Data Bus (MBI/O 00–07)							
$t_{MB\ OD}$	MOS Bus Output Disable	C_L = 15 pF, R_L = 1 kΩ, *(Figure 1)*		15	50	100	ns
$t_{MB\ OE}$	MOS Bus Output Enable	C_L = 15 pF, R_L = 1 kΩ, *(Figure 1)*			50	100	ns
$t_{MB\ ID}$	MOS Bus Input Disable	*(Figure 1)*			55		ns
$t_{MB\ IE}$	MOS Bus Input Enable	*(Figure 1)*			20		ns
Select Bus							
t_{CLR}	Clear Previous Chip Enable	*(Figure 2)*			25	50	ns

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switching time waveforms and ac test circuits

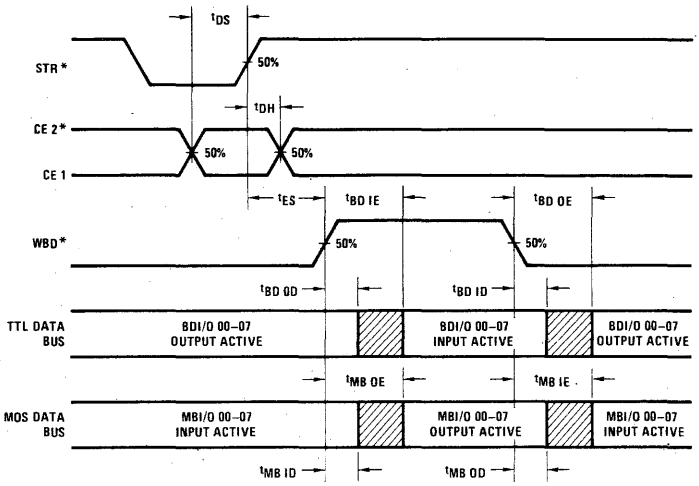


FIGURE 1

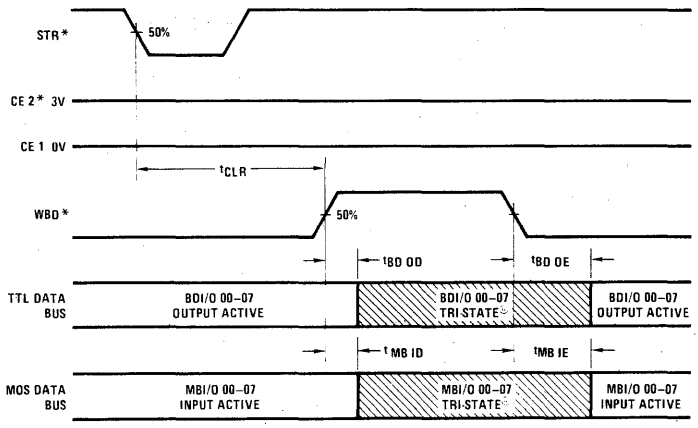


FIGURE 2

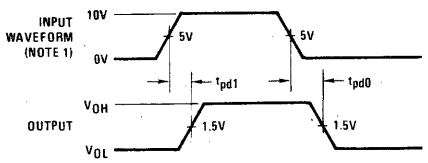
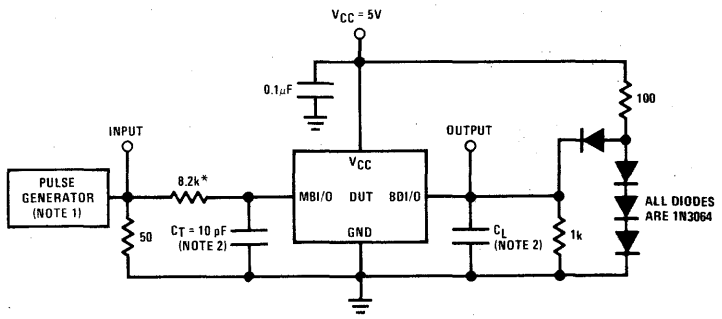


FIGURE 3. BDI/O Bus



*This input network simulates the actual drive characteristic of the PACE outputs

FIGURE 5. MBI/O to BDI/O ac Loads

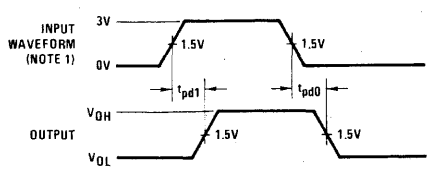


FIGURE 4. MBI/O Bus

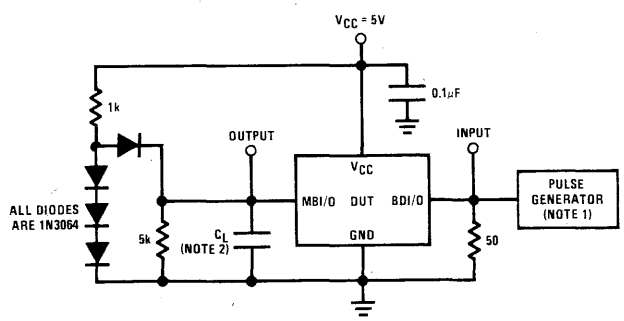


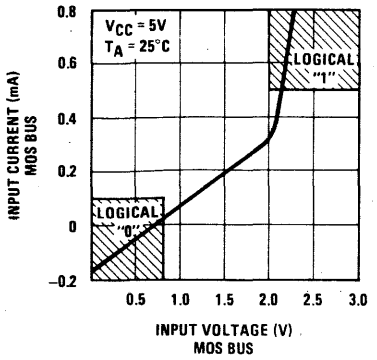
FIGURE 6. BDI/O to MBI/O ac Loads

Note 1: Freq = 1 MHz, duty cycle = 50%, $t_R = t_F \leq 10$ ns (refer to *Figures 5 and 6)*.

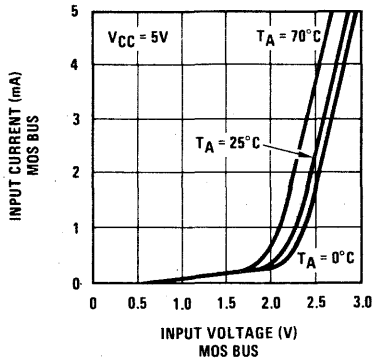
Note 2: All capacitance values include probe and jig capacitance (refer to *Figures 5 and 6)*.

typical performance characteristics

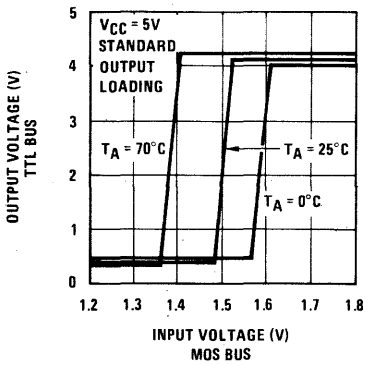
MOS Bus Input Characteristic



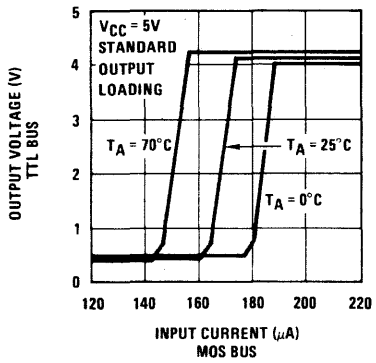
MOS Bus Input Characteristic



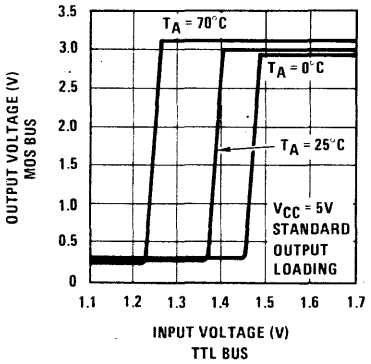
MOS Bus Voltage Threshold



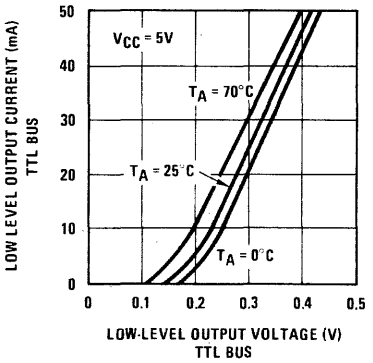
MOS Bus Current Threshold



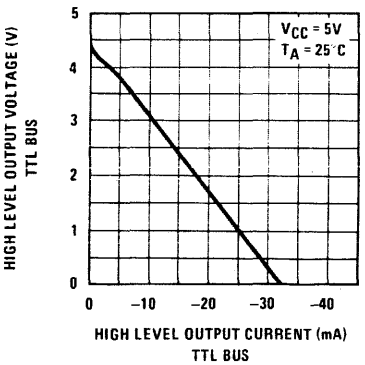
TTL Bus Threshold Characteristic



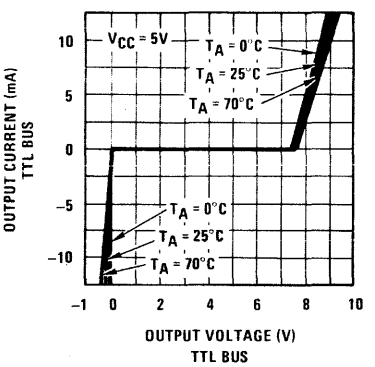
Low-Level Output Voltage vs Output Current TTL Bus



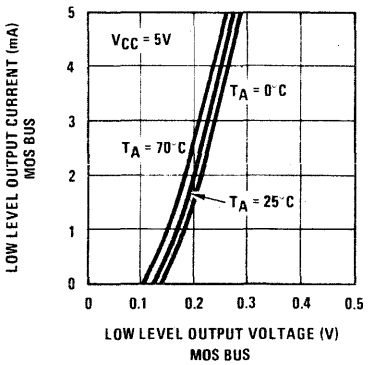
High-Level Output Voltage vs Output Current TTL Bus



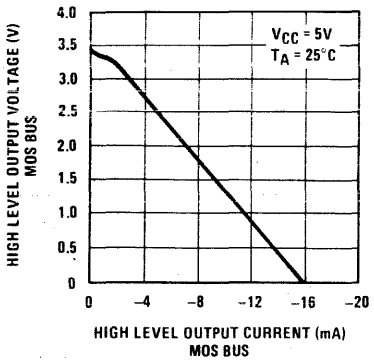
Output Current vs Output Voltage High Impedance State TTL Bus



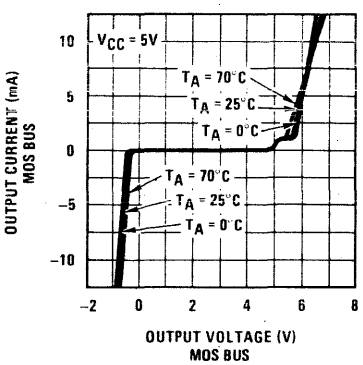
Low-Level Output Voltage vs Output Current MOS Bus



High-Level Output Voltage vs Output Current MOS Bus



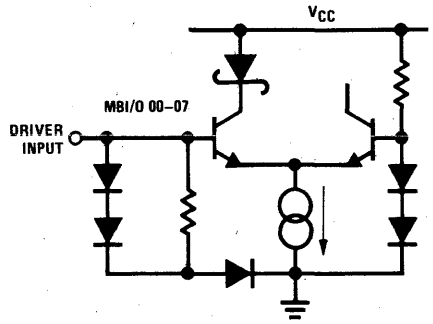
Output Current vs Output Voltage High Impedance State MOS Bus



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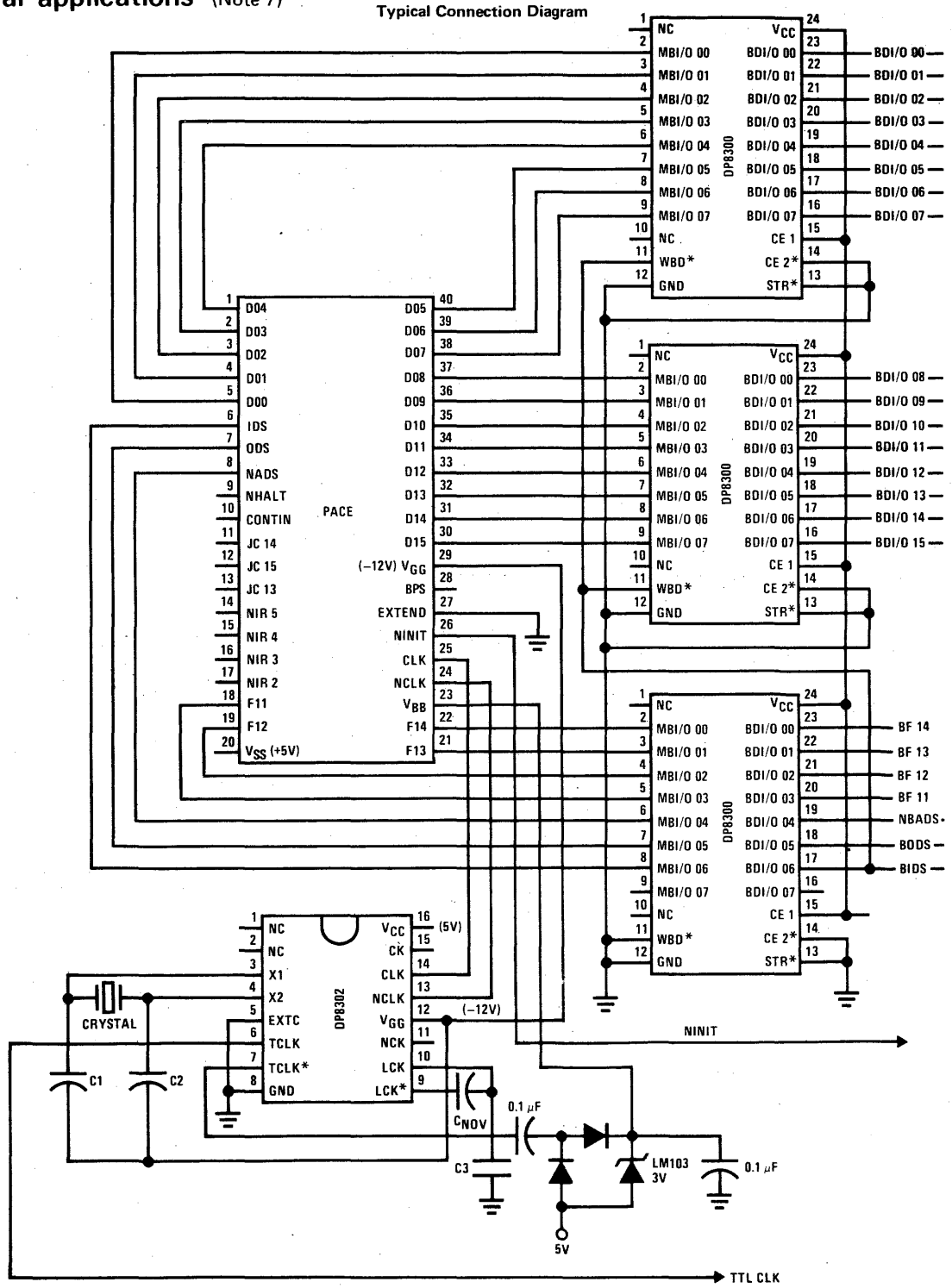
equivalent circuit

MOS Bus Driver Input



typical applications (Note 7)

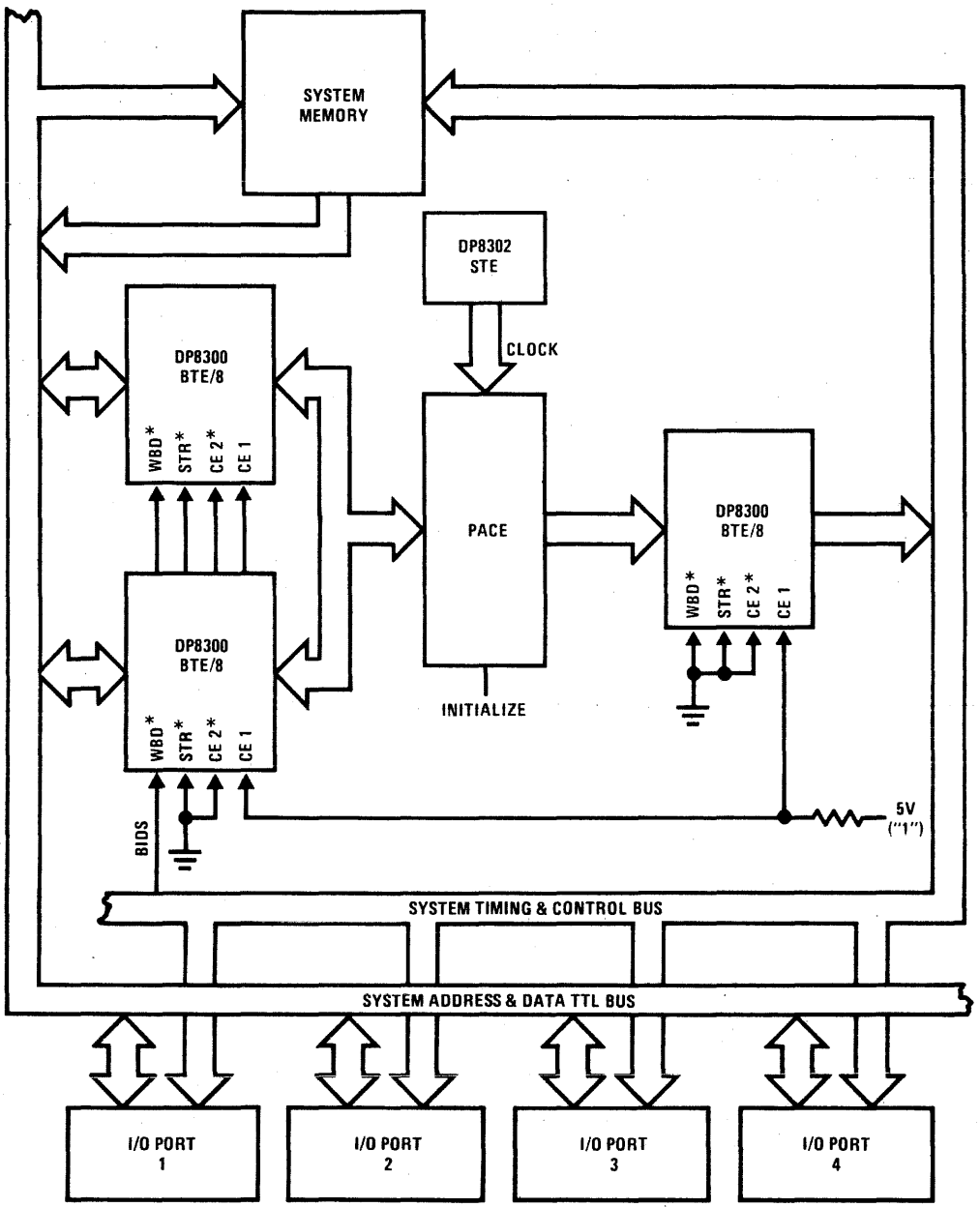
Typical Connection Diagram



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typical applications (Continued)

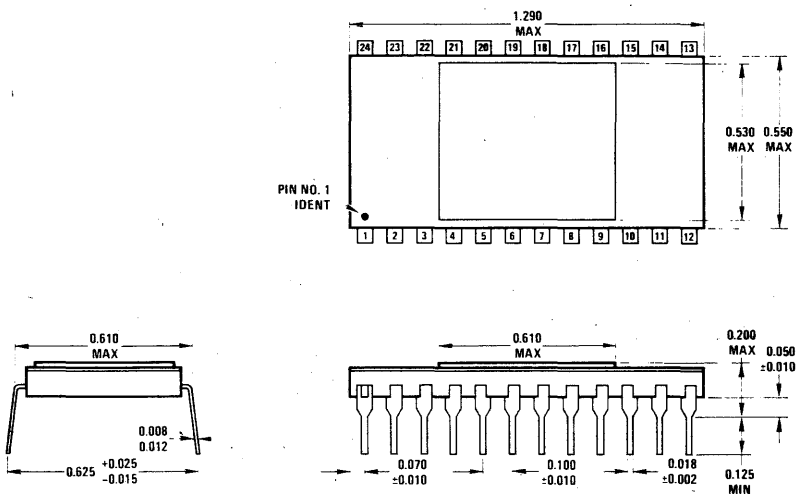
Multiplexed TTL System Bus*



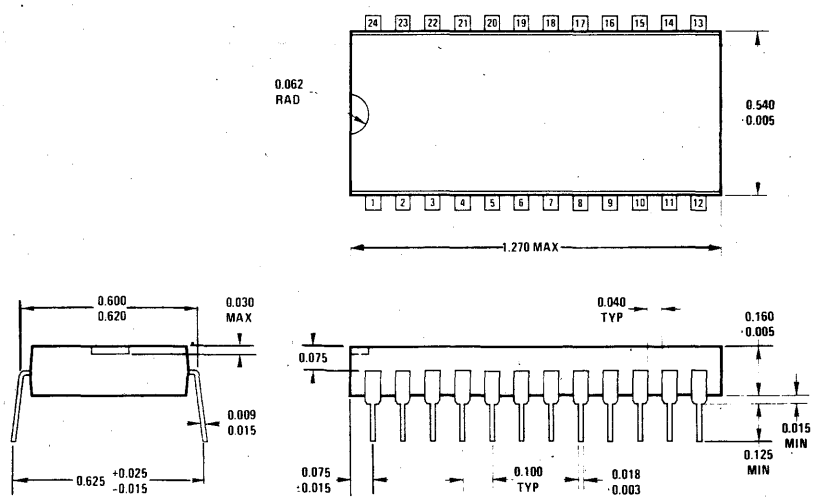
*See Note 7

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physical dimensions



Cavity Dual-In-Line Package (D)
Order Number DP8300D



Molded Dual-In-Line Package (N)
Order Number DP8300N

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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National Semiconductor

DP8302 PACE system timing element (PACE STE)

general description

The PACE STE provides an oscillator, CPU clock driver, and TTL system clocks in a single 16-pin DIP. The STE is intended specifically for application in PACE microprocessor-based systems.

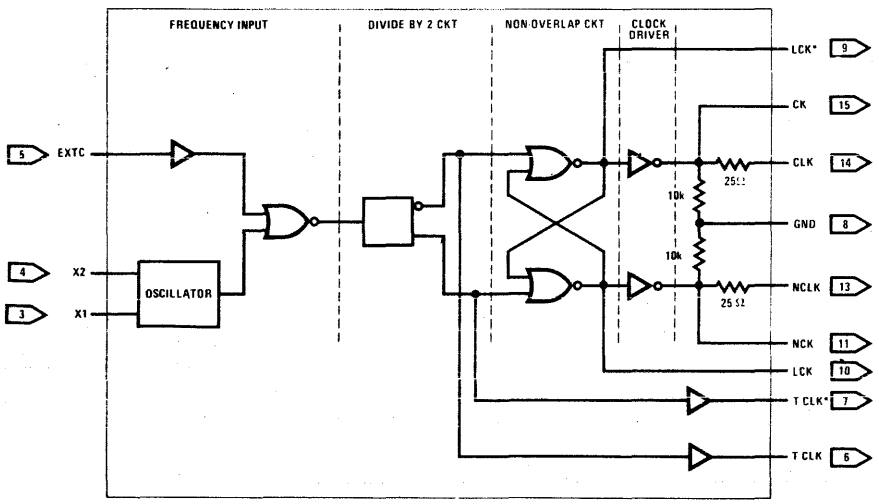
An external crystal provides frequency control. True and complemented non-overlapping clock outputs are generated at one-half the oscillator frequency. Non-overlap intervals may be controlled with a single external capacitor. Series damping resistors are provided on the MOS (CPU) clock outputs (CLK, NCLK).

TTL level system clock outputs are also provided to facilitate the synchronizing of system operations.

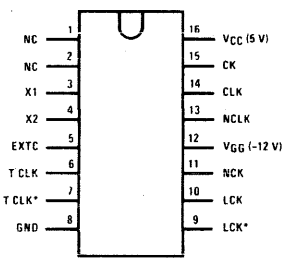
features

- Internal Oscillator Driven Directly from External Crystal, Minimizing Package Count
- External Oscillator Input Maximizes Application Flexibility
- TTL System Clocks Simplify Interfaces and Facilitate Synchronization of System Operations
- MOS Clock Outputs, No External MOS Clock Drivers Required
- High Voltage Output High Level (V_{CC} − 1.1 V) on TTL System Clocks

block and connection diagrams



Dual-In-Line Package



Signal* ≡ N Signal ≡
$\overline{\text{Signal}}$ ≡ Low Active Signal

NC = No Connection

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recommended crystal specifications

- At-cut crystal
- 4.0 MHz ± 0.1%, or 2.6667 MHz ± 0.1%, fundamental mode
- 5 mW maximum
- 150 Ω maximum series resistance

functional description

OSCILLATOR

The oscillator incorporates a low-power inverter biased in the linear region utilizing an internal feedback network. An external crystal is connected between pins X1 and X2 to provide frequency control. EXTC must be grounded for this operating mode. The circuit board traces connecting the crystal to pins X1 and X2 should be as short as possible and should be physically isolated from all high energy level switching signal traces, particularly the CPU MOS clock lines.

When an external oscillator is to be used in place of the internal crystal oscillator, pin X1 must be tied to V_{GG} and pin X2 must be left open. Then, EXTC may be used as a TTL input for the external oscillator.

DIVIDE AND SQUARING CIRCUIT

A flip-flop is used to provide a square wave clock signal by dividing the buffered oscillator output by two. The outputs of this circuit are buffered to provide TTL system clock signals which lead the MOS level clock outputs.

NON-OVERLAP CIRCUIT

The Divider output drives a cross-coupled latch containing a delay in the feedback path which insures non-overlapping MOS clock signals. The delay in the feedback path can be increased by connecting a capacitor between pins LCK and LCK*. The effect of the capacitor on increasing the non-overlap interval is shown in the Typical Characteristics section.

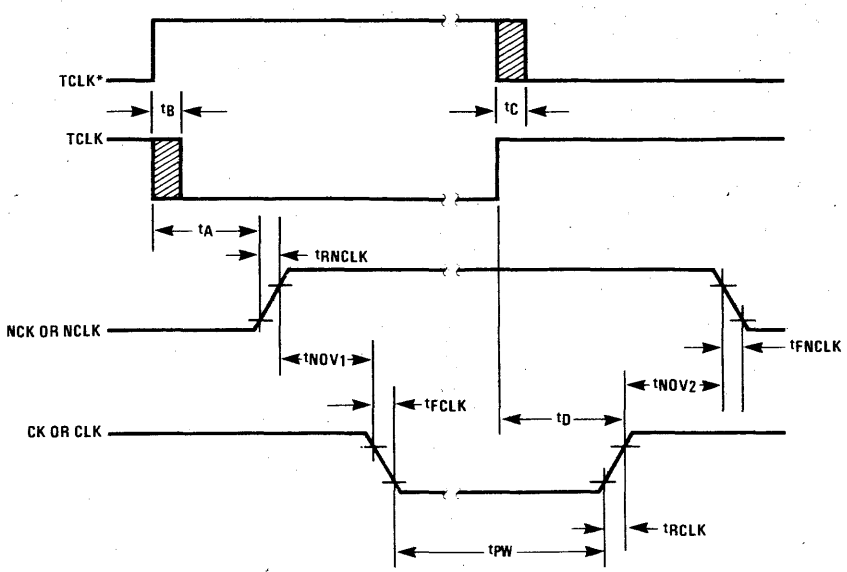
MOS CLOCK DRIVER

The MOS Clock Driver produces output voltage swings from the +5 V supply to the −12 V supply. CLK and NCLK outputs contain a 25 Ω series damping resistor, a typically optimum value for circuit board layouts with clock interconnect lines of less than two inches.

Undamped MOS clock outputs, CK and NCK, are also available in the event other values of series damping resistors are desired.

It is recommended that 0.1 μF high frequency capacitors be provided from V_{CC} to ground and from V_{GG} to ground immediately adjacent to the STE.

timing diagram



Times measured at 10% and 90%

$C_1 = C_2 = 60_{pf}$, $C_3 = 90_{pf}$, $C_{nov} = 40_{pf}$

Figure 1.

absolute maximum ratings [1]

Supply Voltage (V_{CC}) . . . . . 7.0 V
(V_{GG}) . . . . . −15.0 V
Input Voltage . . . . . 5.5 V
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . 300°C

operating conditions

	Min.	Max.	Units
Supply Voltage (V_{CC})	4.75	5.25	V
(V_{GG})	−11.40	−12.6	V
Temperature	0	+70	°C

dc electrical characteristics (Notes 2 and 3)

Parameter	Conditions		Min.	Typ.	Max.	Units
OUTPUT SPECIFICATIONS:						
TCLK, TCLK*						
V_{OH} Logic "1" Output Voltage	V_{CC} = 4.75 V	I_{OH} = −1 mA		4.25		V
V_{OL} Logic "0" Output Voltage	V_{CC} = 4.75 V	I_{OL} = 32 mA				V
		I_{OL} = 50 mA				V
I_{OS} Output Short Circuit Current	(Note 4), V_{CC} = 5.25 V, V_O = 0			−33		mA
CK, NCK, CLK, NCLK						
V_{OH} Logic "1" Output Voltage	I_{OH} = −50 μA			4.0		V
V_{OL} Logic "0" Output Voltage	V_{CC} = 4.75 V, V_{GG} = −11.4 V	I_{OL} = 100 μA		V_{GG} + 0.1		V
		I_{OL} = 10 mA		V_{GG} + 0.2		V
INPUT SPECIFICATIONS						
EXTC						
V_{IH} Logic "1" Input Voltage						V
I_{IH} Logic "1" Input Current	V_{CC} = 5.25 V	V_{IN} = 2.4 V				μA
		V_{IN} = 5.5 V				mA
V_{IL} Logic "0" Input Voltage						V
I_{IL} Logic "0" Input Current	V_{CC} = 5.25 V	V_{IL} = 0.4 V				mA
V_{CLAMP} Input Clamp Diode	V_{CC} = 4.75 V	I_{IL} = −12 mA				V
POWER SUPPLY CURRENT						
I_{CC} Supply Current from V_{CC}	V_{CC} = 5.25 V					mA
I_{GG} Supply Current from V_{GG}	V_{GG} = −12.6 V					mA

ac electrical characteristics

T_A = 0°C to +70°C, V_{CC} − V_{GG} = +17 V ± 5%

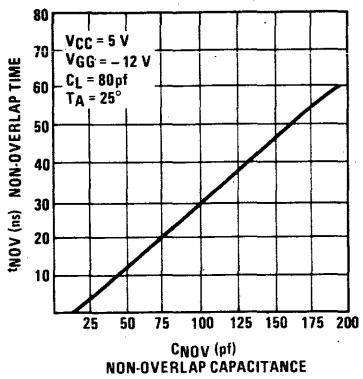
Parameter	Conditions	Min.	Typ.	Max.	Units
t_{RCK}, t_{RNCK}	C_L = 80 pF Figure 1		20		ns
t_{FNCK}, t_{FCK}	C_L = 80 pF Figure 1		20		ns
t_{NOV1}, t_{NOV2}	C_L = 80 pF Figure 1		12		ns
t_A, t_D	C_L = 80 pF Figure 1		10		ns
t_B, t_C	C_L = 80 pF Figure 1		8		ns
t_{PW}	C_L = 80 pF Figure 1 Crystal Frequency = 4 MHz				ns
t_{PW}	C_L = 80 pF Figure 1 Crystal Frequency = 2.6667 MHz				ns
f_{MAX} Maximum Input Frequency					MHz

Notes:

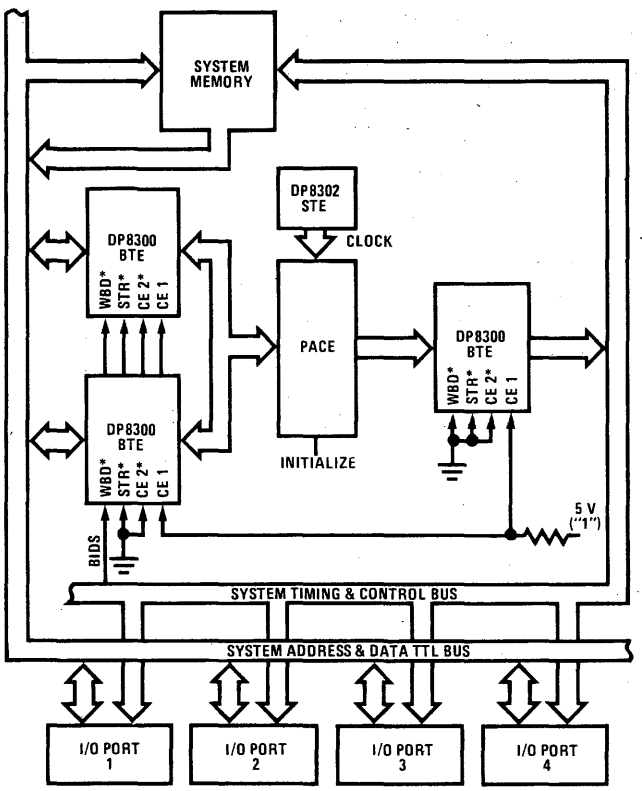
1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
2. Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and V_{CC} = 4.75 V to 5.25 V, V_{GG} = −11.4 V to −12.6 V power supply range. All typicals are given for V_{CC} = 5.0 V, V_{GG} = −12 V, and T_A = +25°C.
3. All currents into device pins are shown as positive; currents out of device pins are shown as negative. All voltages are references to ground unless otherwise noted.
4. Only one output at a time should be shorted.

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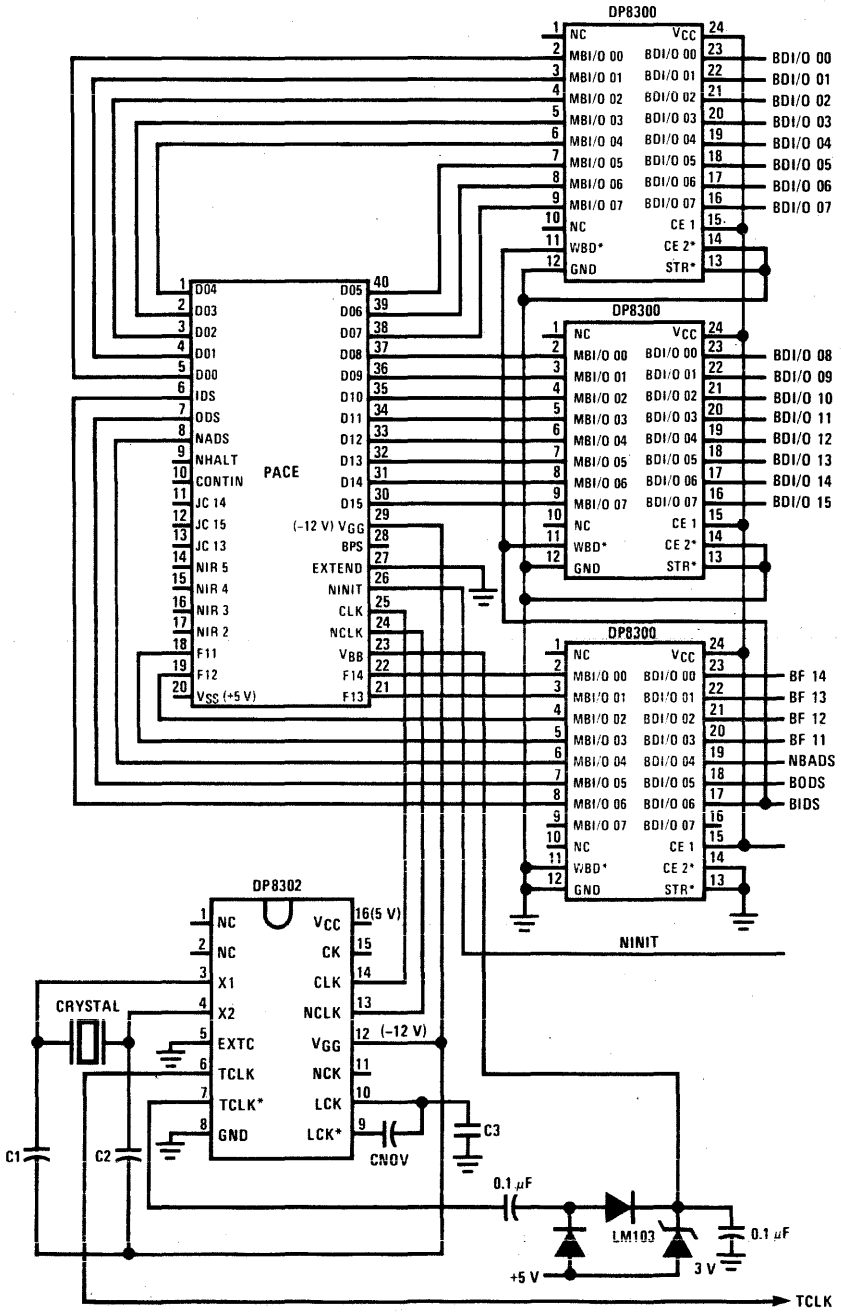
TYPICAL NON-OVERLAP TIME VS. NON-OVERLAP CAPICITOR



typical applications



typical connection diagram



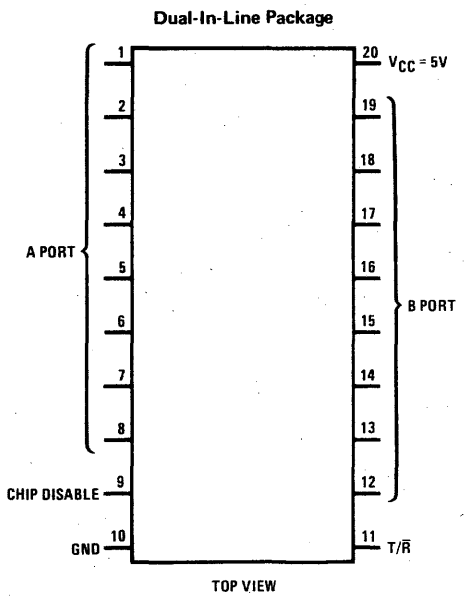
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DP8304 8-bit bidirectional bus transceiver

general description

The DP8304 is an 8-bit bidirectional Bus transceiver able to drive a common Bus (B port) or 10 LS input loads (A port). Inputs to both ports are LSTTL. A chip disable provides TRI-STATE® to both ports when high, and data flow is controlled by the transmit/$\overline{\text{receive}}$ enable. Both outputs provide 3.6V V_{OH} when active. Signals are non-inverting for both ports. With T/$\overline{R}$ low data flows from B port to A port.

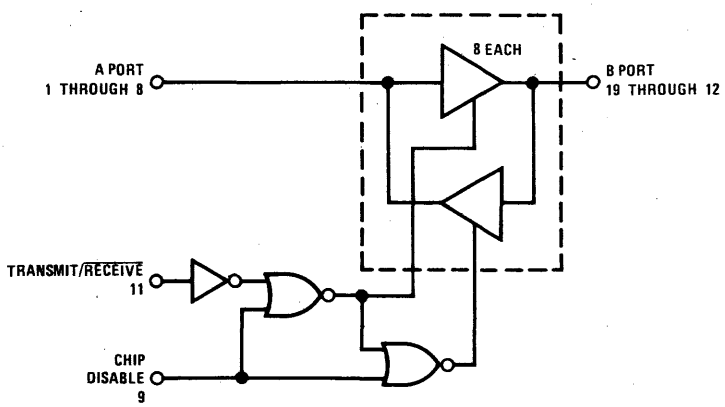
connection diagram



truth table

PIN DESCRIPTION	RECEIVE	TRANSMIT	DISABLE
Chip Disable	0	0	1
Transmit/$\overline{\text{Receive}}$	0	1	X
A Port	Out	In	TRI-STATE
B Port	In	Out	TRI-STATE

logic diagram



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DS0025/DS0025C two phase MOS clock driver

general description

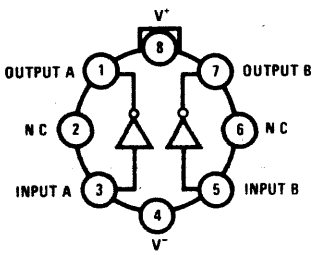
The DS0025/DS0025C is monolithic, low cost, two phase MOS clock driver that is designed to be driven by TTL/DTL line drivers or buffers such as the DM932, DS8830 or DM7440. Two input coupling capacitors are used to perform the level shift from TTL/DTL to MOS logic levels. Optimum performance in turn-off delay and fall time are obtained when the output pulse is logically controlled by the input. However, output pulse widths may be set by selection of the input capacitors eliminating the need for tight input pulse control.

features

- 8-lead TO-5 or 8-lead dual-in-line package
- High Output Voltage Swings—up to 30V
- High Output Current Drive Capability—up to 1.5A
- Rep. Rate: 1.0 MHz into > 1000 pF
- Driven by DM932, DS8830, DM7440 (SN7440)
- "Zero" Quiescent Power

connection diagrams

Metal Can Package

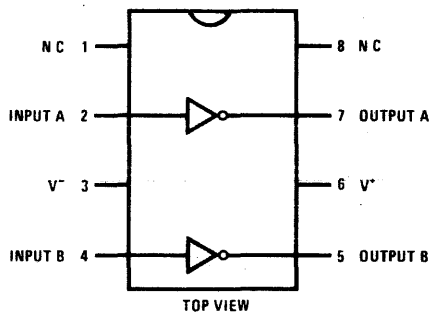


Note: Pin 4 connected to case.

TOP VIEW

Order Number DS0025H or DS0025CH
See Package 23

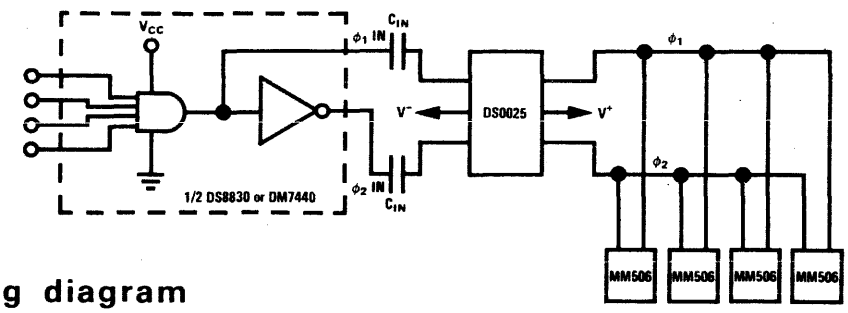
Dual-In-Line Package



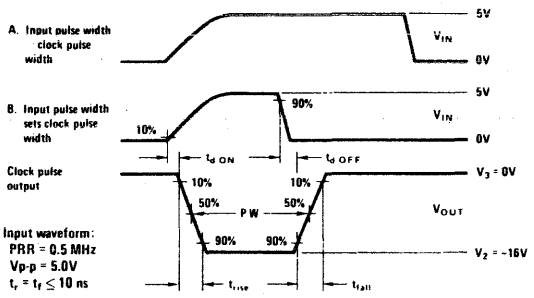
TOP VIEW

Order Number DS0025CN
See Package 12

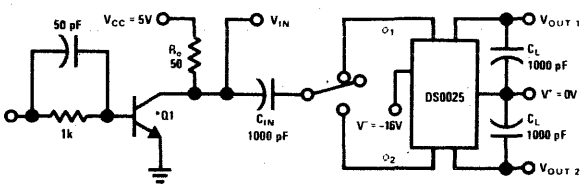
typical application



timing diagram



ac test circuit



*Q1 is selected high speed NPN switching transistor.

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DS0026, DS0056 5 MHz two phase MOS clock drivers

general description

DS0026/DS0056 are low cost monolithic high speed two phase MOS clock drivers and interface circuits. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. They may be driven from standard 54/74 series and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The DS0026 and DS0056 are intended for applications in which the output pulse width is logically controlled; i.e., the output pulse width is equal to the input pulse width.

The DS0026/DS0056 are designed to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon-gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16-bit 1103 RAM memory system. Information on the correct usage of the DS0026 in these as well as other systems is included in the application note AN-76A.

The DS0026 and DS0056 are identical except each driver in the DS0056 is provided with a V_{BB} connection to supply a higher voltage to the output stage. This aids in pulling up the output when it is in the high state. An external resistor tied between these extra pins and a supply higher than V^+ will cause the output to pull up to $(V^+ - 0.1V)$ in the off state.

For DS0056 applications, it is required that an external resistor be used to prevent damage to the device when the driver switches low. A typical V_{BB} connection is shown on the next page.

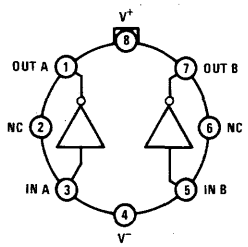
These devices are available in 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, and one and a half watt ceramic DIP, and TO-8 packages.

features

- Fast rise and fall times—20 ns with 1000 pF load
- High output swing—20V
- High output current drive—±1.5 amps
- TTL/DTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Drives to 0.4V of GND for RAM address drive

connection diagrams (Top Views)

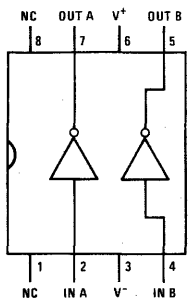
TO-5 Package



Note: Pin 4 connected to case.

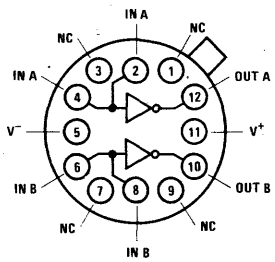
Order Number DS0026H or DS0026CH
See Package 23

Dual-In-Line Package



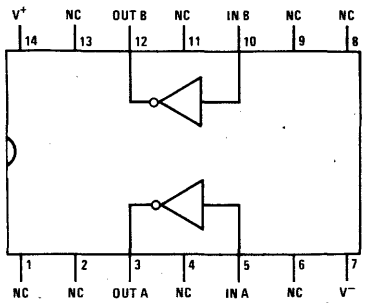
Order Number DS0026CN
See Package 12

TO-8 Package



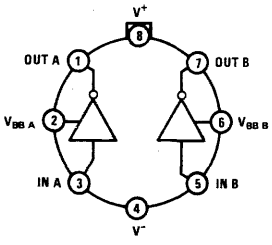
Order Number DS0026G or DS0026CG
See Package 25

Dual-In-Line Package



Order Number DS0026J, DS0026CJ or DS0026W
See Package 9 or 27

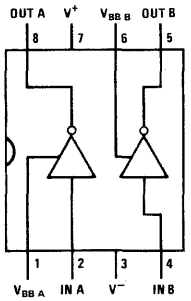
TO-5 Package



Note: Pin 4 connected to case.

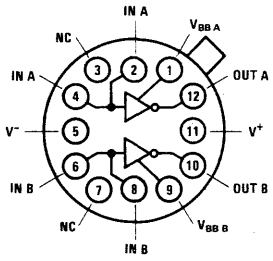
Order Number DS0056H or DS0056CH
See Package 23

Dual-In-Line Package



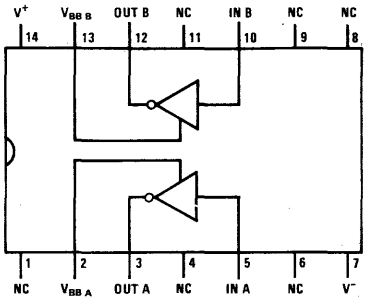
Order Number DS0056CN
See Package 12

TO-8 Package



Order Number DS0056G or DS0056CG
See Package 25

Dual-In-Line Package



Order Number DS0056J or DS0056CJ
See Package 9

DS1603/DS3603, DS3604, DS55107/DS75107, DS55108/DS75108, DS75207, DS75208 dual line receivers

general description

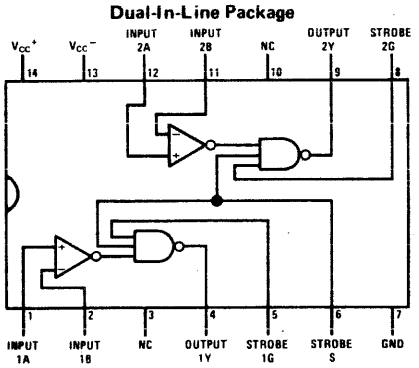
The nine products described herein are TTL compatible dual high speed circuits intended for sensing in a broad range of system applications. While the primary usage will be for line receivers or MOS sensing, any of the products may effectively be used as voltage comparators, level translators, window detectors, transducer preamplifiers, and in other sensing applications. As digital line receivers the products are applicable with the DS55109/DS75109 and DS55110/DS75110 companion drivers, or may be used in other balanced or unbalanced party-line data transmission systems. The improved input sensitivity and delay specifications of the DS75207, DS75208 and DS3604 make them ideal for sensing high performance MOS memories as well as high sensitivity line receivers and voltage comparators. TRI-STATE® products enhance bused organizations.

features

- Diode protected input stage for power "OFF" condition
- 17 ns typ high speed
- TTL compatible
- ±10 mV or ±25 mV input sensitivity
- ±3V input common-mode range
- High input impedance with normal V_{CC}, or $V_{CC} = 0V$
- Strobes for channel selection
- TRI-STATE outputs for high speed buses
- Dual circuits
- Sensitivity gntd. over full common-mode range
- Logic input clamp diodes—meets both "A" and "B" version specifications
- ±5V standard supply voltages

connection diagrams

Dual-In-Line Package



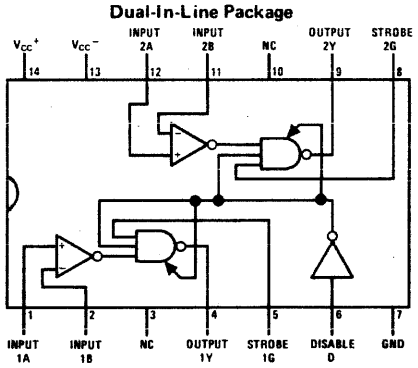
TOP VIEW

Order Number DS55107J, DS75107J, DS55108J, DS75108J, DS75207J or DS75208J
See Package 9

Order Number DS75107N, DS75108N, DS75207N or DS75208N
See Package 14

Order Number DS55107W or DS55108W
See Package 27

Dual-In-Line Package



TOP VIEW

Order Number DS1603J, DS3603J DS3604J or DS1603W
See Package 9 or 27

Order Number DS3603N or DS3604N
See Package 14

product selection guide

TEMPERATURE→ / PACKAGE→	$-55°C \leq T_A \leq +125°C$ CAVITY DIP	$0°C \leq T_A \leq +70°C$ CAVITY OR MOLDED DIP	
INPUT SENSITIVITY→ / OUTPUT LOGIC↓	±25 mV	±25 mV	±10 mV
TTL Active Pull-up	DS55107	DS75107	DS75207
TTL Open Collector	DS55108	DS75108	DS75208
TTL TRI-STATE	DS1603	DS3603	DS3604

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DS1605/DS3605, DS1606/DS3606, DS1607/DS3607, DS1608/DS3608 hex MOS sense amplifiers (MOS to TTL converters)

general description

The DS3605 series is a new series of programmable hex MOS sense amplifiers featuring high speed direct MOS sense capability with high impedance states to allow use of a common bus line. The DS1605/DS3605 and the DS1606/DS3606 have TRI-STATE® outputs. The DS1607/DS3607 and DS1608/DS3608 have both TRI-STATE inputs and outputs. High impedance states are controlled by an enable input.

Input current threshold (the level at which the output changes state) is determined by the current at the programming pin. The current threshold is 100μA with the programming pin grounded and 250μA with the pin unconnected. The threshold can be set from 100μA to 300μA by connecting a resistor from the pin to ground, and set above 300μA by connecting a resistor from the pin to the positive supply.

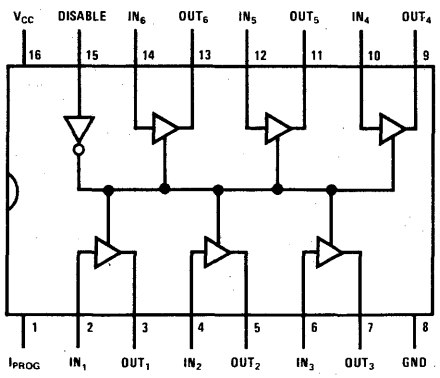
Outputs are high current drivers capable of sinking 50 mA in the low state and sourcing 5 mA in the high state.

features

- Non-inverting inputs (DS1605/DS3605, DS1607/DS3607)
- Inverting inputs (DS1606/DS3606, DS1608/DS3608)
- No external components required (direct MOS sensing)
- Programmable input thresholds
- Current sensing—100μA minimum
- 50 mA drive capability
- TRI-STATE control
- Single 5V supply
- 15 ns typical propagation delay (DS3605)

connection diagram

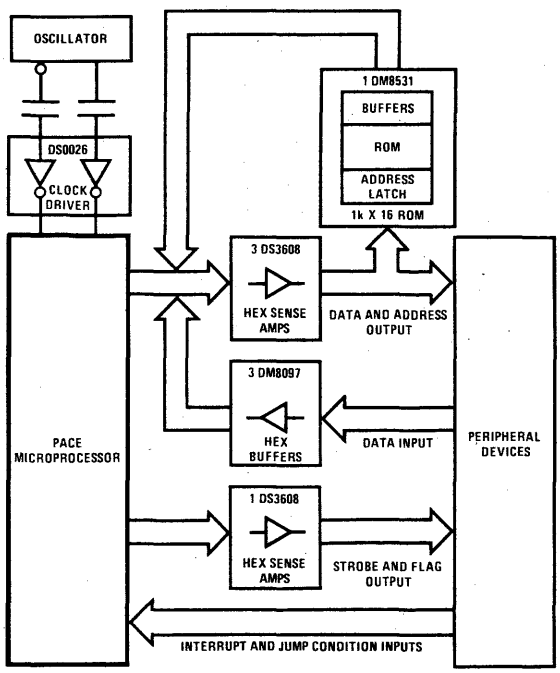
Dual-In-Line Package



TOP VIEW

typical application

PACE Interface



DS3608 shown as an interface between the PACE microprocessor and TTL data bus and I/O bus.

ordering information

ORDER NUMBERS	PACKAGE
DS1605J, DS1606J, DS1607J, DS1608J	Cavity DIP (J)
DS3605J, DS3606J, DS3607J, DS3608J	Cavity DIP (J)
DS3605N, DS3606N, DS3607N, DS3608N	Molded DIP (N)

See Package 10 or 15

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DS1640/DS3640, DS1670/DS3670 quad MOS TRI-SHARE™ port drivers general description

The DS1640/DS3640 and DS1670/DS3670 are quad MOS TRI-SHARE port drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input current, allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay.

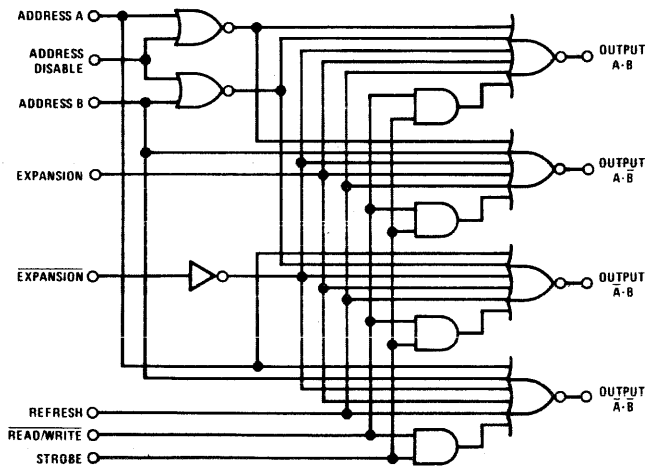
The DS1640/DS3640 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1670/DS3670 has a direct, low impedance output source for use with or without an external resistor.

The DS1640/DS1670 has two address inputs which decode to one-of-four-high outputs. Provisions are made for address expansion. For example, two packages may be used to implement a three-input, eight-output decoder. Also included is a refresh control, read/write, and strobe input. These functions are required by the MM5270 4k TRI-SHARE MOS RAM.

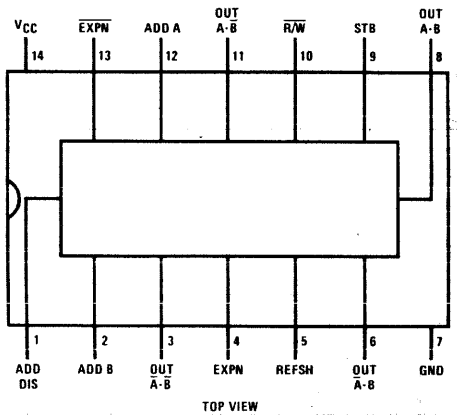
features

- TRI-SHARE port driver for MM5270 RAM
- TTL/DTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driving outputs
- Built-in damping resistor (DS1640/DS3640)

logic and connection diagrams

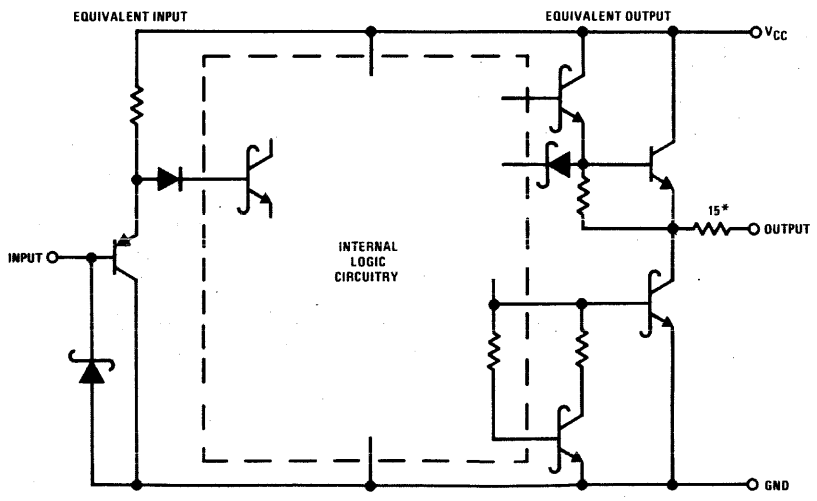


Dual-In-Line Package



TOP VIEW

schematic diagram



*DS1640/DS3640 only

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DS1642/DS3642, DS1672/DS3672
dual bootstrapped TTL to MOS clock drivers

general description

The DS1672 is a dual bipolar-to-MOS clock driver designed to provide high output current and voltage capabilities necessary for driving high capacitance (up to 500 pF) MOS memory systems. The circuit needs only one power supply, (12V typical). This feature greatly reduces high stand-by power levels and at the same time simplifies system deisgn.

The circuit also features output bootstrapping, eliminating the need for an additional supply to provide a higher voltage to the output stage. The function is accomplished by connecting a small value capacitor (typically 200 pF) from the output to the bootstrap pin on each driver.

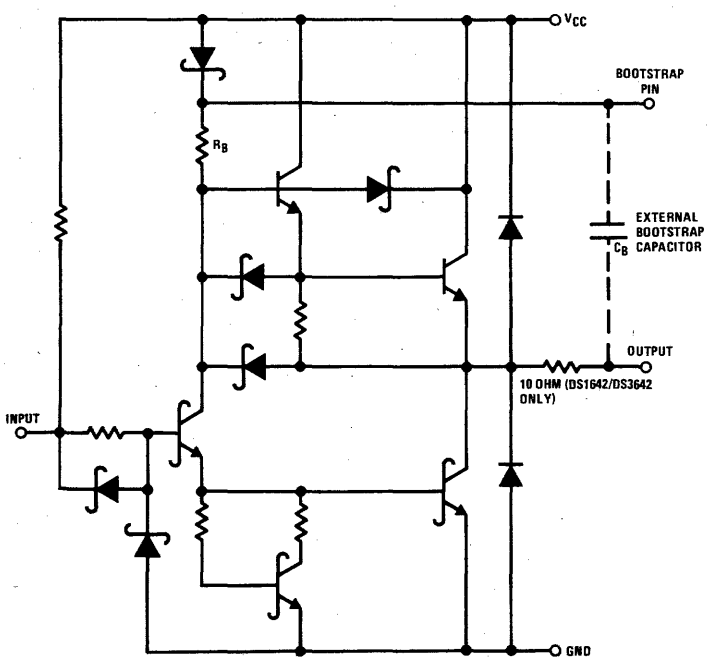
The circuit has Schottky-clamped transistor logic for minimum propagation delay. Typical stand-by power (output low) is 48 mW per driver. A fail-safe condition is provided in the circuit, so if the input is opened the output assumes the logic "0" state.

The DS1642/DS3642 has a 10 Ω resistor in series with each output to dampen transients caused by the fast-switching output. The DS1672/DS3672 has a direct low impedance output for use with or without an external resistor.

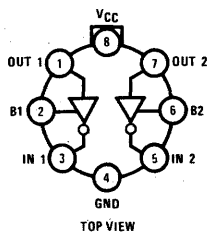
features

- High output voltage capability 13.2V
- TTL/DTL compatible inputs
- High speed operation
- Bootstrapping eliminates extra supplies—reduces power
- Low stand-by power 48 mW/driver
- Built-in 10 Ω damping resistor (DS1642/DS3642)

schematic and connection diagrams

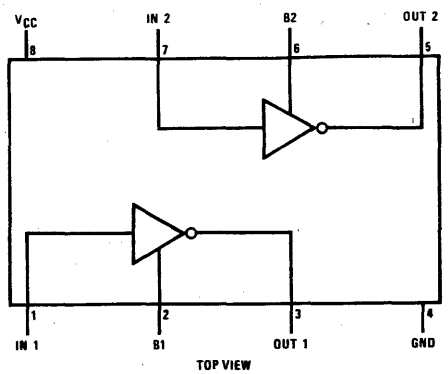


Metal Can Package



TOP VIEW

Dual-In-Line Package



TOP VIEW

©IC MASTER 1978

DS1645/DS3645, DS1675/DS3675 hex TRI-STATE® TTL to MOS latch/drivers

general description

The DS1645/DS3645 and DS1675/DS3675 are hex MOS latch/drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are used to reduce input currents, allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE® outputs which allow bus operation.

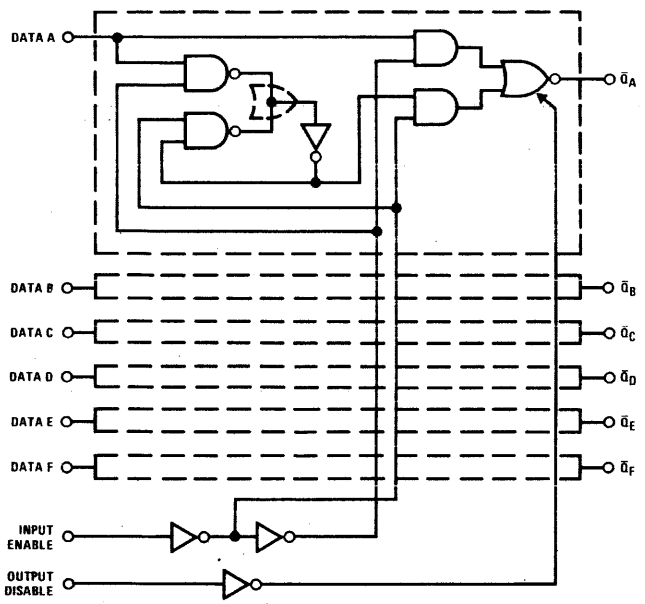
The DS1645/DS3645 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1675/DS3675 has a direct, low impedance output for use with or without an external resistor.

The circuit employs a fall-through-latch which captures the data in parallel with the output, thereby eliminating the delay normally encountered in other latch circuits. The DS1645/DS3645 and DS1675/DS3675 may be used for input address lines or input/output data lines of a MOS memory system.

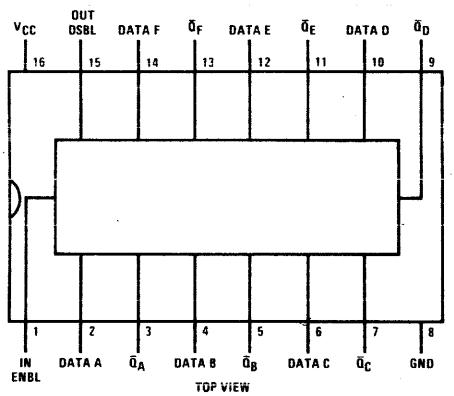
features

- TTL/DTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driving outputs
- TRI-STATE outputs
- Built-in damping resistor (DS1645/DS3645)

logic and connection diagrams



Dual-In-Line Package



truth table

INPUT ENABLE	OUTPUT DISABLE	DATA	OUTPUT	OPERATION
1	0	1	0	Data Feed-Through
1	0	0	1	Data Feed-Through
0	0	X	Q	Latched to Data Present when Enable Went Low
X	1	X	Hi-Z	High Impedance Output

X = Don't care
Hi-Z = TRI-STATE mode

DS1645/DS3645, DS1675/DS3675 hex TRI-STATE® TTL to MOS latch/drivers

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Memory/Clock Drivers

Advance Information*

DS1646/DS3646, DS1676/DS3676 6-bit TRI-STATE® MOS refresh counter/driver

general description

The DS1646/DS3646 and DS1676/DS3676 are 6-bit refresh counters with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE outputs allow it to be used on common data buses.

The DS1646/DS3646 has a 15Ω resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1676/DS3676 has a direct, low impedance output, for use with or without an external resistor.

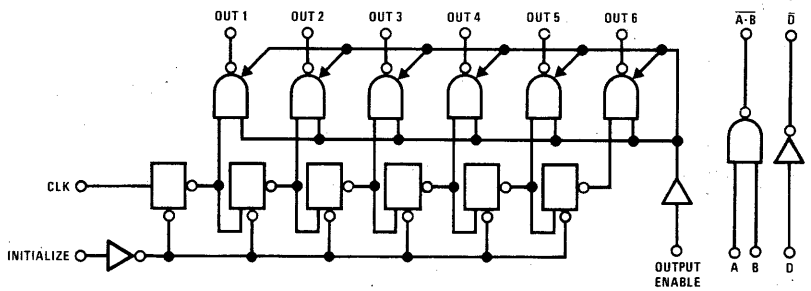
The counter uses as its input the RAM clock signal, and with each clock input, it advances the count by one, thus generating a new refresh address.

Extra pins in the package are used for a 2-input NAND gate and a 2-input NOR gate, both of which have capacitive drive outputs.

features

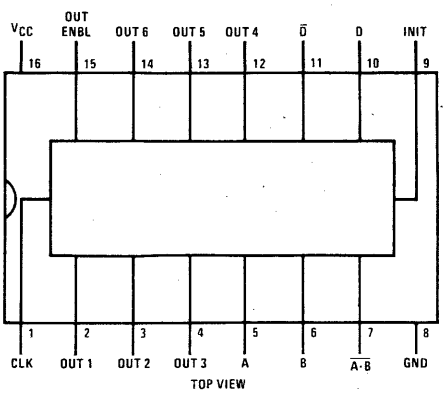
- Circuit counts when clock goes high
- TTL/DTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driver outputs
- TRI-STATE outputs
- Extra gates on unused pins
- Built-in damping resistor (DS1646/DS3646)
- Initialize input

logic diagram



connection diagram

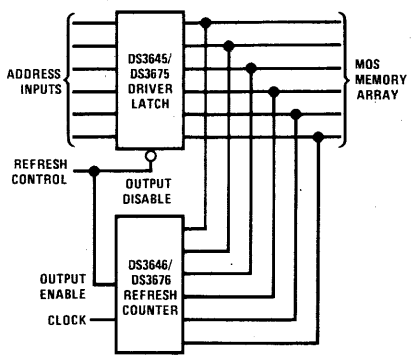
Dual-In-Line Package



Order Number DS1646J, DS1676J, DS3646J, DS3676J, DS3646N, or DS3676N
See Package 10 or 15

typical application

The DS1646/DS3646 and DS1676/DS3676 have TRI-STATE outputs which can be tied to the outputs of another TRI-STATE driver. The refresh counter can control the address lines into a memory array during a short refresh cycle, and then return to the high-impedance state to allow the primary driver to control the address lines.



*Specifications may change.

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DS1647/DS3647, DS1677/DS3677, DS16147/DS36147, DS16177/DS36177 quad TRI-STATE® MOS memory I/O registers

general description

The DS1647/DS3647 series are 4-bit I/O buffer registers intended for use in MOS memory systems. The circuits employ a fall-through latch for data storage. This method of latching captures the data in parallel with the output, thus eliminating the delays encountered in other designs. The circuits use Schottky-clamped transistor logic for minimum propagation delay and employ PNP input transistors so that input currents are low, allowing large fan-out to these circuits needed in a memory system.

Two pins per bit are provided, and data transfer is bi-directional so that the register can handle both input and output data. The direction of data flow is controlled through the input enables. The latch control, when taken low, will cause the register to hold the data present at that time and display it at the outputs. Data can be latched into the register independent of the output disables or EXPANSION input. Either or both of the outputs may be taken to the high-impedance state with the output disables. The EXPANSION pin disables both outputs to facilitate multiplexing with other I/O registers on the same data lines.

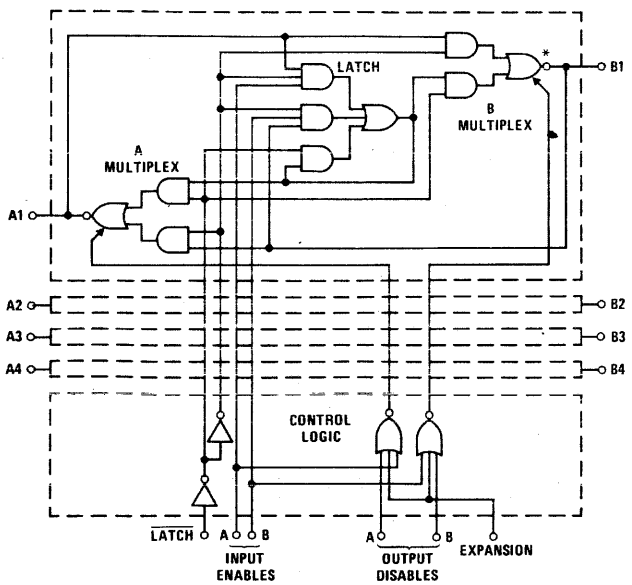
The "B" port outputs in the DS16147/DS36147 and DS16177/DS36177 are open collectors, and in the DS1647/DS3647 and DS1677/DS3677 they are TRI-STATE. The "B" port outputs are also designed for use in bus organized data transmission systems and can sink 50 mA and source −5.2 mA. The "A" port outputs in all four types are TRI-STATE.

Data going from port "A" to port "B" is inverted in the DS1647/DS3647 and DS16147/DS36147 and is not inverted in the DS1677/DS3677 and DS16177/DS36177. Data going from port "B" to port "A" is inverted in all four types.

features

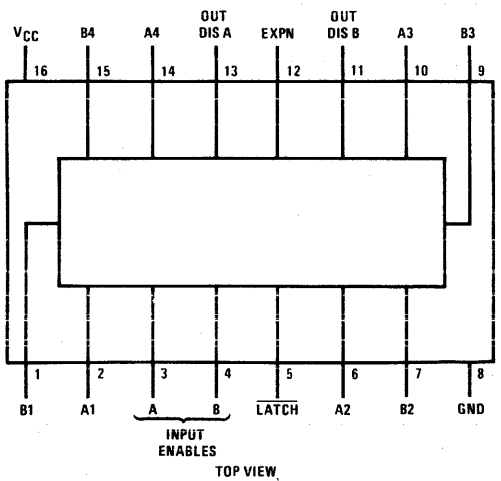
- PNP inputs minimize loading
- Fall-through latch design
- High speed circuitry
- TRI-STATE outputs
- EXPANSION control
- Bi-directional data flow
- TTL/DTL compatible
- Transmission line driver output

logic and connection diagrams



*Inverting DS1647/DS3647 and DS16147/DS36147 only

Dual-In-Line Package



TOP VIEW

Order Number DS1647D, DS3647D, DS1677D, DS3677D, DS16147D, DS36147D, DS16177D, DS36177D, DS3647N, DS3677N, DS36147N or DS36177N

*Specifications may change.

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DS1648/DS3648, DS1678/DS3678
TRI-STATE® TTL to MOS multiplexer/drivers

general description

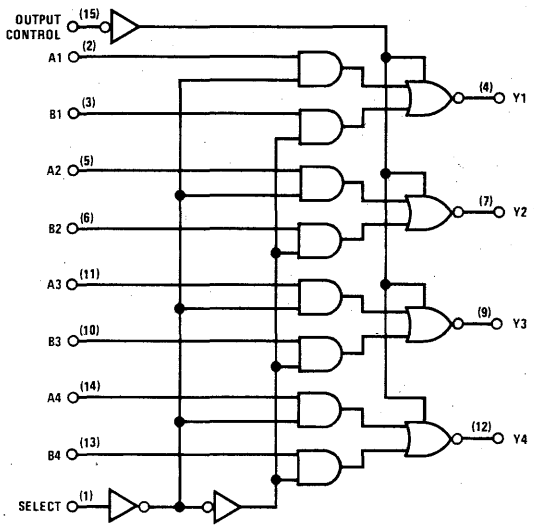
The DS1648/DS3648 and DS1678/DS3678 are quad 2-input multiplexers with TRI-STATE outputs designed to drive the large capacitive loads (up to 500 pF) associated with MOS memory systems. A PNP input structure is employed to minimize input currents so that driver loading in large memory systems is reduced. The circuit employs Schottky-clamped transistors for high speed and TRI-STATE outputs for bus operation.

The DS1648/DS3648 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1678/DS3678 has a direct, low impedance output for use with or without an external resistor.

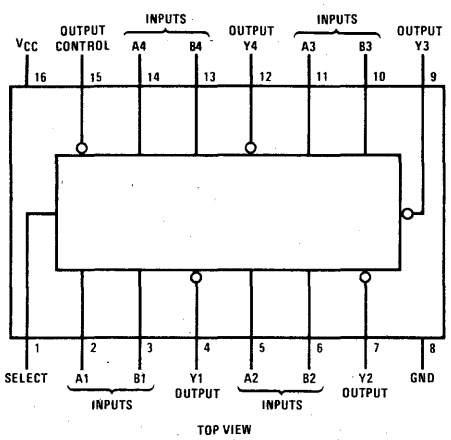
features

- TRI-STATE outputs interface directly with system bus
- Schottky-clamped for better ac performance
- PNP inputs to minimize input loading
- DTL and TTL compatible
- High-speed capacitive load drivers
- Built-in damping resistor (DS1648/DS3648 only)

logic and connection diagrams

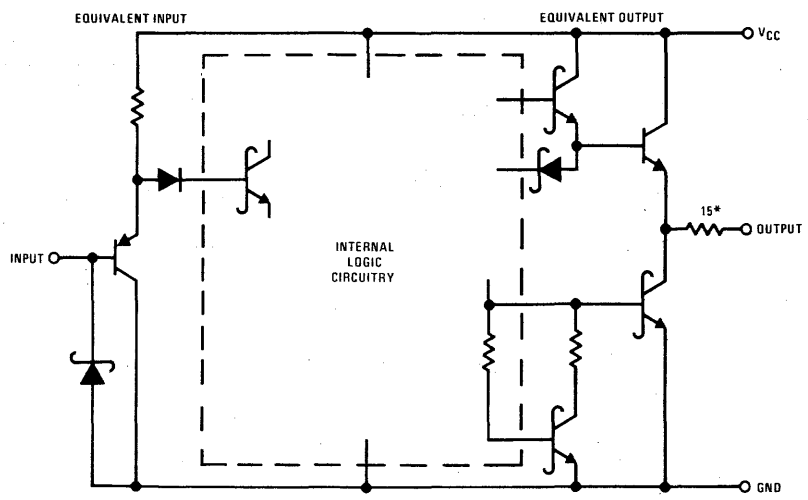


Dual-In-Line Package



TOP VIEW

schematic diagram



*DS1648/DS3648 only

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DS1649/DS3649, DS1679/DS3679 hex TRI-STATE® TTL to MOS drivers

general description

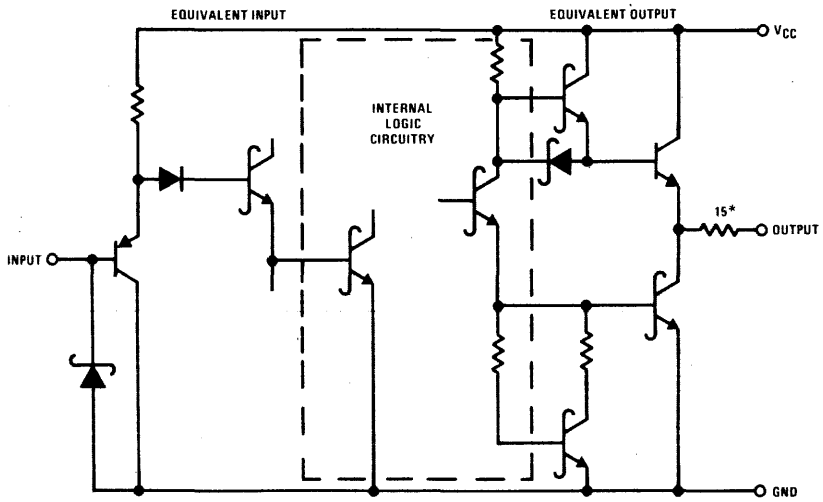
The DS1649/DS3649 and DS1679/DS3679 are Hex TRI-STATE MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE outputs for bus operation.

The DS1649/DS3649 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1679/DS3679 has a direct low impedance output for use with or without an external resistor.

features

- High speed capabilities
  - Typ 9 ns driving 50 pF
  - Typ 30 ns driving 500 pF
- TRI-STATE outputs for data bussing
- Built-in 15 Ω damping resistor (DS1649/DS3649)
- Same pin-out as DM8096 and DM74366

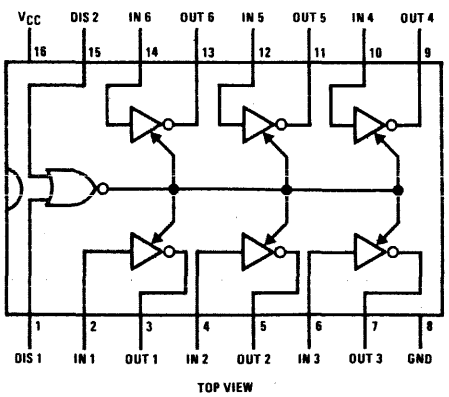
schematic diagram



*DS1649/DS3649 only

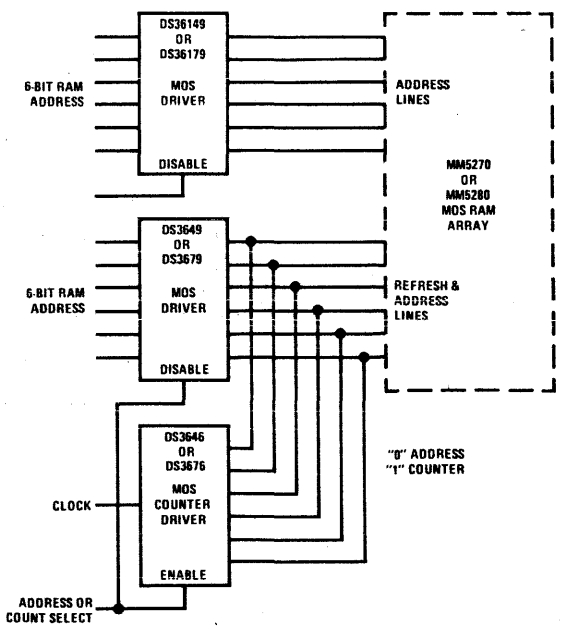
connection diagram

Dual-In-Line Package



TOP VIEW

typical application



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DS1671/DS3671 bootstrapped two phase MOS clock driver

general description

The DS1671/DS3671 is a high speed dual MOS clock driver and interface circuit. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. It may be driven from standard 54/74 and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The circuit can be used in both P-channel and N-channel MOS memory system drive applications.

The DS1671/DS3671 is intended to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for an 8k by 16-bit 1103 RAM memory system.

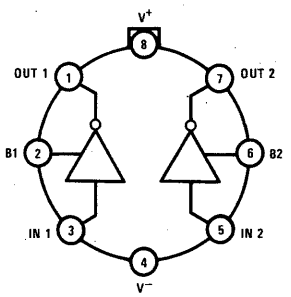
Each driver uses output bootstrapping to provide a higher voltage to the output stage, thus eliminating the need for an additional V_{DD} supply. The bootstrapping function is accomplished by connecting a small value capacitor (typically 200 pF) from each output to each drivers bootstrap node.

features

- Fast rise and fall times—20 ns with 1000 pF load
- High output swing—20V
- High output current drive—±1.5A
- TTL/DTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Swings to 0.4V of GND for RAM address drive

connection diagrams

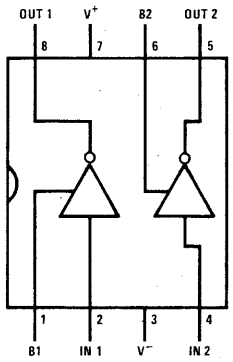
Metal Can Package



TOP VIEW

Order Number DS1671H
or DS3671H
See Package 23

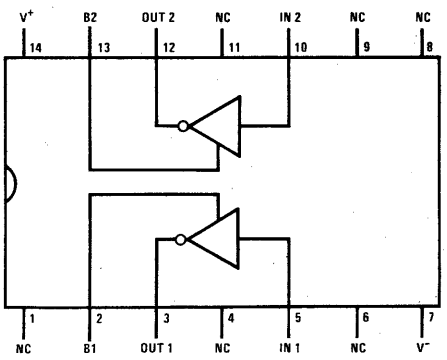
Dual-In-Line Package



TOP VIEW

Order Number DS3671N
See Package 12

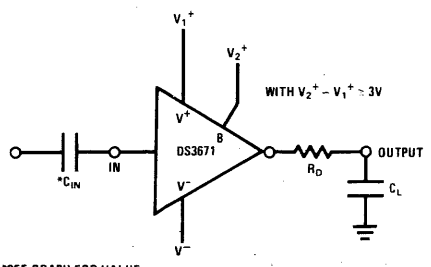
Dual-In-Line Package



TOP VIEW

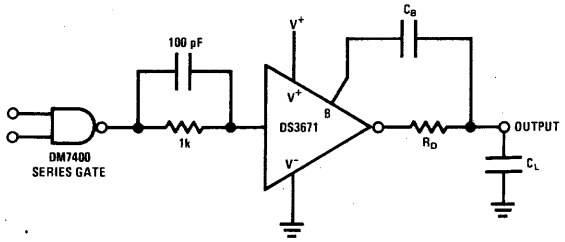
Order Number DS1671J or DS3671J
See Package 9

typical applications



*SEE GRAPH FOR VALUE

DS3671 Operating with Extra Supply
to Inhance Output Voltage Level



Bootstrap Clock Driver Driven from a TTL Gate

*Specifications may change.

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DS3625 dual high speed MOS sense amp

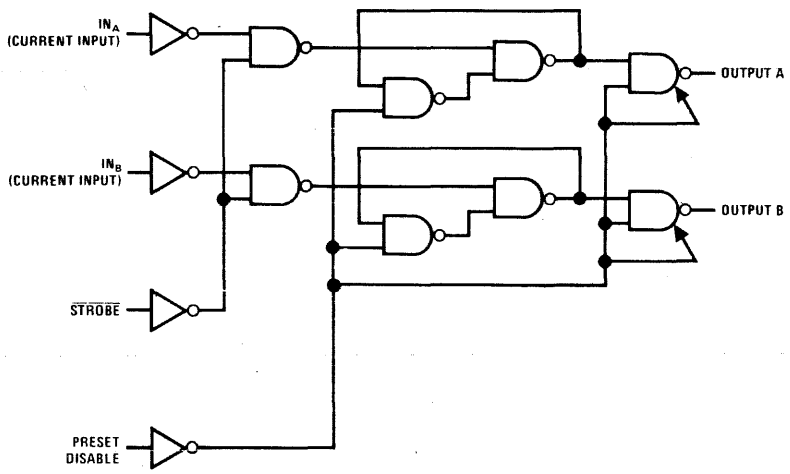
general description

The DS3625 is a dual high speed MOS to TTL level converter. It acts as an interface level converter between MOS and TTL logic devices. It consists of two 1-input converters with common strobe input to inhibit "0" entry when strobe is high. It allows parallel entry when strobe is low and the internal latch is preset by the common preset input. TRI-STATE® output logic is implemented in this circuit to facilitate high speed time sharing of decoder-drivers, fast random-access (or sequential) memory arrays, etc.

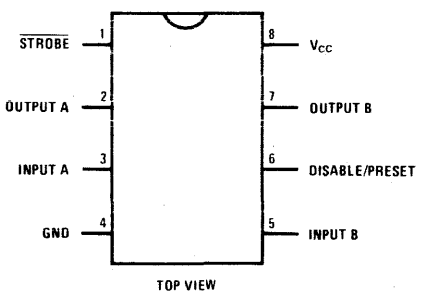
features

- Easily interfaces with most popular 1k and 2k dynamic MOS RAMs
- Pin-for-pin replacement for the 8T25
- Very low output impedance — high drive ability
- High impedance output state which allows many outputs to be connected to a common bus line
- Average power dissipation 110 mW per converter

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS3625N
See Package 12

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Interface
Advance Information*

DS3643, DS3673 decoded quad MOS clock drivers

general description

The DS3643 and DS3673 are quad bipolar-to-MOS decoder/clock drivers with TTL/DTL compatible inputs. They are designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

The device features full decoding of input address lines from two inputs to one of four outputs. Also featured is the capability of expanding to three inputs to one of eight outputs with the use of the Expansion and $\overline{\text{Expansion}}$ inputs. Also included are clock and refresh inputs.

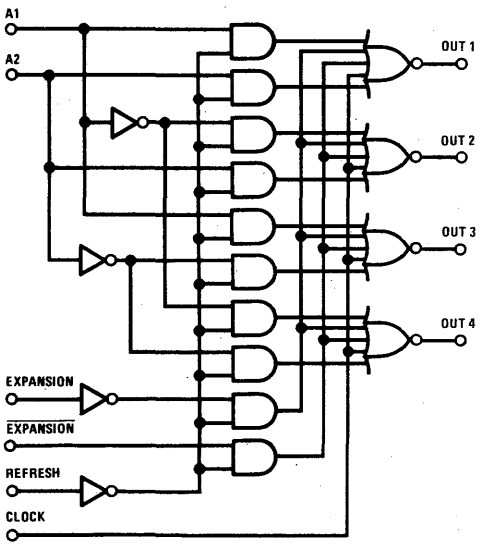
The circuit was designed for driving large capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs, thereby minimizing input loading.

The DS3643 has a 10 Ω damping resistor in series with each output to dampen transients caused by the fast switching output, while the DS3673 has a direct, low impedance output, for use with or without an external resistor.

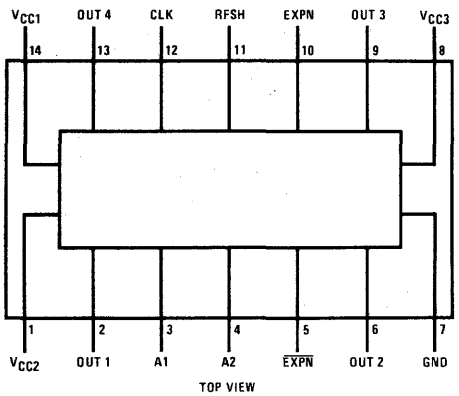
features

- TTL/DTL compatible inputs
- Operates from standard bipolar and MOS supplies
- PNP inputs minimize input loading
- Full logic decoding for either two inputs to one of four outputs or three inputs to one of eight outputs
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Built-in damping resistors (DS3643)

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS3643J or DS3643N

Order Number DS3673J or DS3673N

See Package 9 or 14

truth table

INPUTS						OUTPUTS			
CLOCK	REFRESH	EXPANSION	$\overline{\text{EXPANSION}}$	A_2	A_1	OUT 1	OUT 2	OUT 3	OUT 4
1	X	X	X	X	X	0	0	0	0
0	1	X	X	X	X	1	1	1	1
0	0	1	0	0	0	1	0	0	0
0	0	1	0	0	1	0	1	0	0
0	0	1	0	1	0	0	0	1	0
0	0	1	0	1	1	0	0	0	1
0	0	1	1	X	X	0	0	0	0
0	0	0	1	X	X	0	0	0	0
0	0	0	0	X	X	0	0	0	0

X = Don't Care State.

*Specifications may change.

DS3644, DS3674 quad TTL to MOS clock drivers general description

The DS3644 and DS3674 are quad bipolar-to-MOS clock drivers with TTL/DTL compatible inputs. They are designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

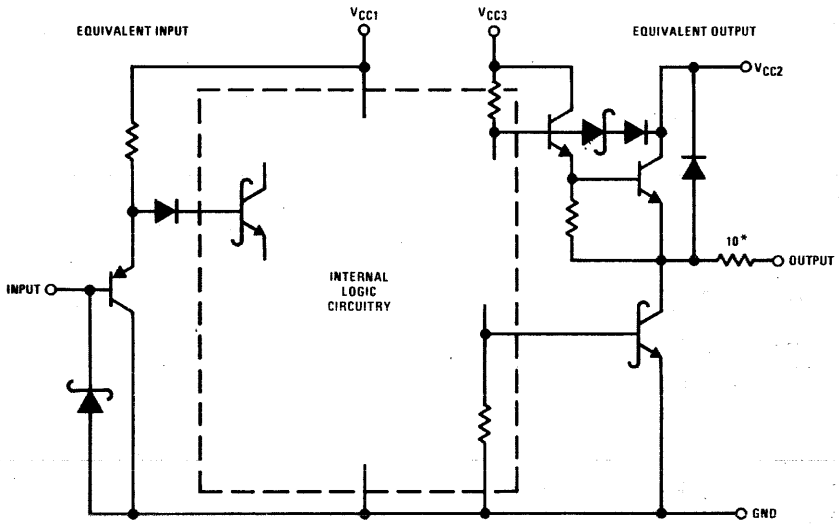
The device features two common enable inputs, a refresh input, and a clock control input for simplified system designs. The circuit was designed for driving highly capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs thereby minimizing input loading.

The DS3644 contains a 10 Ω resistor in series with each output to dampen the transients caused by the fast-switching output, while the DS3674 has a direct, low impedance output for use with or without an external damping resistor.

features

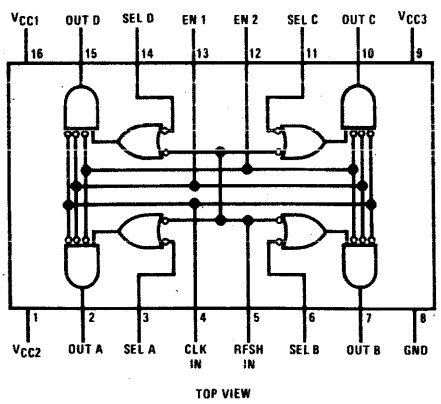
- TTL/DTL compatible inputs
- Operates from standard bipolar and MOS supplies
- PNP inputs minimize loading
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Pin and function compatible with MC3460 and 3235
- Built-in damping resistors (DS3644)

schematic and connection diagrams



*DS3643 only

Dual-In-Line Package



TOP VIEW

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Interface
Advance Information*

DS3651, DS3653 quad high speed MOS sense amplifiers

general description

The DS3651 and DS3653 are TTL compatible high speed circuits intended for sensing in a broad range of MOS memory system applications. Switching speeds have been enhanced over conventional sense amplifiers by application of Schottky technology, and TRI-STATE® strobing is incorporated offering a high impedance output state for bused organization.

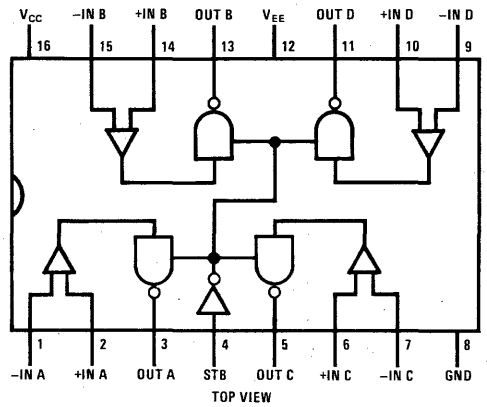
The DS3651 has active pull-up outputs, and the DS3653 offers open collector outputs providing implied "AND" operations.

features

- High speed — 15 ns (typ)
- TTL compatible
- Input sensitivity — ±7 mV
- TRI-STATE outputs for high speed buses
- Standard supply voltages — ±5V
- Pin and function compatible with MC3430 and MC3432

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DS3651J, DS3653J, DS3651N or DS3653N
See Package 10 or 15

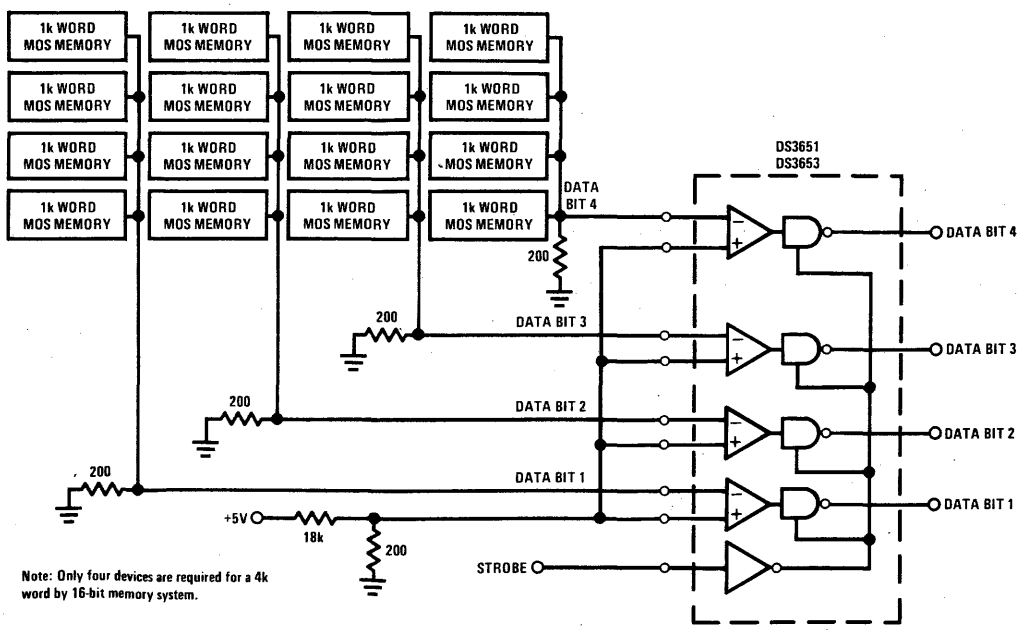
truth table

INPUT	STROBE	OUTPUT	
		DS3651	DS3653
$V_{ID} \geq +7.0$ mV, $T_A = 0°C$ to $+70°C$	L	H	Open
	H	Open	Open
-7.0 mV $\leq V_{ID} \leq +7.0$ mV, $T_A = 0°C$ to $+70°C$	L	X	X
	H	Open	Open
$V_{ID} \leq -7.0$ mV, $T_A = 0°C$ to $+70°C$	L	L	L
	H	Open	Open

L = Low logic state
H = High logic state
Open = TRI-STATE
X = Indeterminate State

typical applications

A Typical MOS Memory Sensing Application for a 4k word by 4-bit memory arrangement employing 1103 type memory devices



Note: Only four devices are required for a 4k word by 16-bit memory system.

*Specifications may change

Interface

DS7803/DS8803, DS8813 two phase oscillator/clock driver

general description

The DS7803 is a self contained two phase oscillator/clock driver. It requires no external components to generate one of three primary oscillator frequencies and pulse widths. Other frequencies can easily be obtained by programming input voltages. Three sets of outputs are provided: damped and undamped MOS outputs and TTL monitor outputs. The MOS outputs easily drive 500 pF loads with less than 150 ns rise and fall times. In addition the outputs have current limiting to protect against momentary shorts to the supplies.

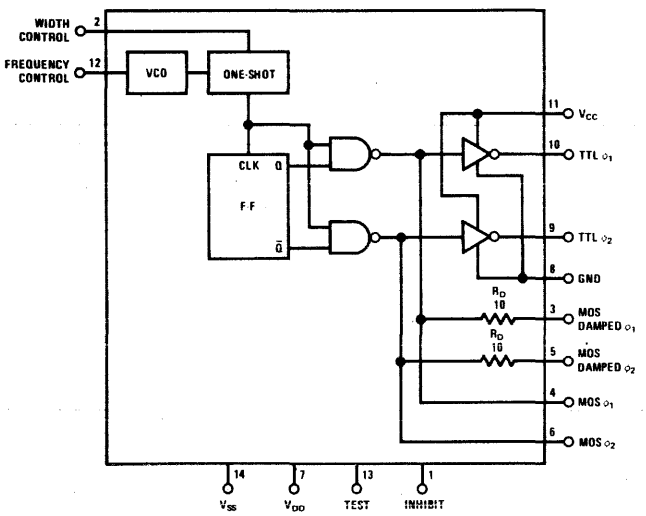
The DS7803 and DS8803 are available in a 14-lead cavity DIP. The DS8803 is also available in a 14-pin molded DIP. The DS8813 comes in an 8-pin molded DIP, providing damped MOS outputs only.

features

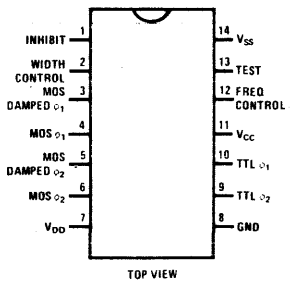
- Two phase non-overlapping outputs
- No external timing components required
- Frequency adjustable from 100 kHz to 500 kHz
- Pulse width adjustable from 260 ns to 1.4μs
- Damped and undamped MOS outputs
- TTL monitor outputs

block and connection diagrams

DS7803/DS8803

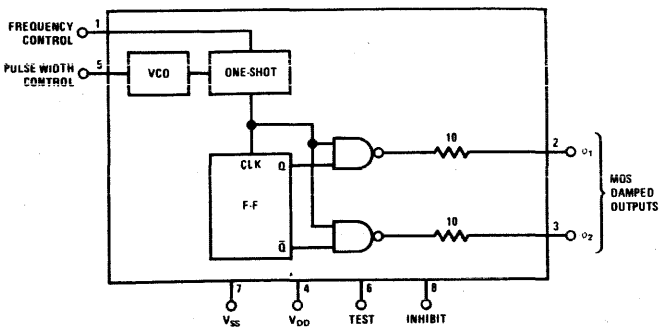


Dual-In-Line Package

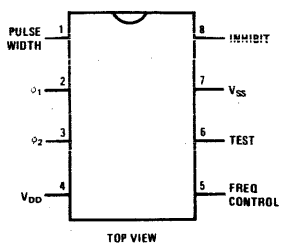


Order Number DS7803J, DS8803J or DS8803N
See Package 9 or 14

DS8813



Dual-In-Line Package



Order Number DS8813N
See Package 12

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DS16149/DS36149, DS16179/DS36179 hex MOS drivers

general description

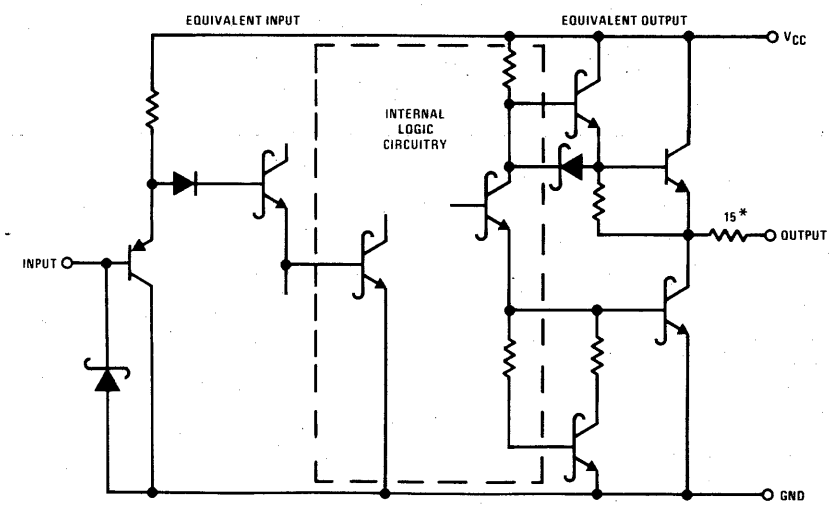
The DS16149/DS36149 and DS16179/DS36179 are Hex MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and a disable control that places the outputs in the logic "1" state (see truth table). This is especially useful in MOS RAM applications where a set of address lines has to be in the logic "1" state during refresh.

The DS1649/DS3649 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1679/DS3679 has a direct low impedance output for use with or without an external resistor.

features

- High speed capabilities
  - Typ 9 ns driving 50 pF
  - Typ 29 ns driving 500 pF
- TRI-STATE outputs for data bussing
- Built-in 15 Ω damping resistor (DS16149/DS36149)
- Same pin-out as DM8096 and DM74366

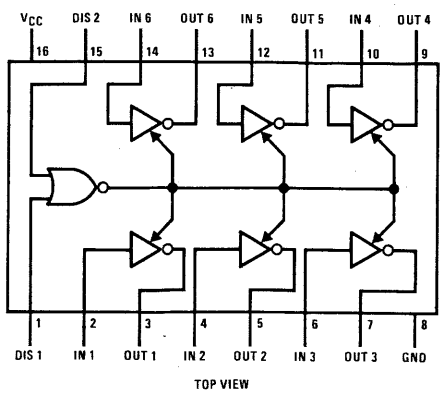
schematic diagram



*DS16149/DS36149 only.

connection diagram

Dual-In-Line Package



TOP VIEW

truth table

DISABLE INPUT		INPUT	OUTPUT
DIS 1	DIS 2		
0	0	0	1
0	0	1	0
0	1	X	1
1	0	X	1
1	1	X	1

X = Don't care

DS55325/DS75325 memory drivers general description

The DS55325 and DS75325 are monolithic memory drivers which feature high current outputs as well as internal decoding of logic inputs. These circuits are designed for use with magnetic memories.

The circuit contains two 600 mA sink-switch pairs and two 600 mA source-switch pairs. Inputs A and B determine source selection while the source strobe (S_1) allows the selected source turn on. In the same manner, inputs C and D determine sink selection while the sink strobe (S_2) allows the selected sink turn on.

Sink-output collectors feature an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2}. This protects the outputs from voltage surges associated with switching inductive loads.

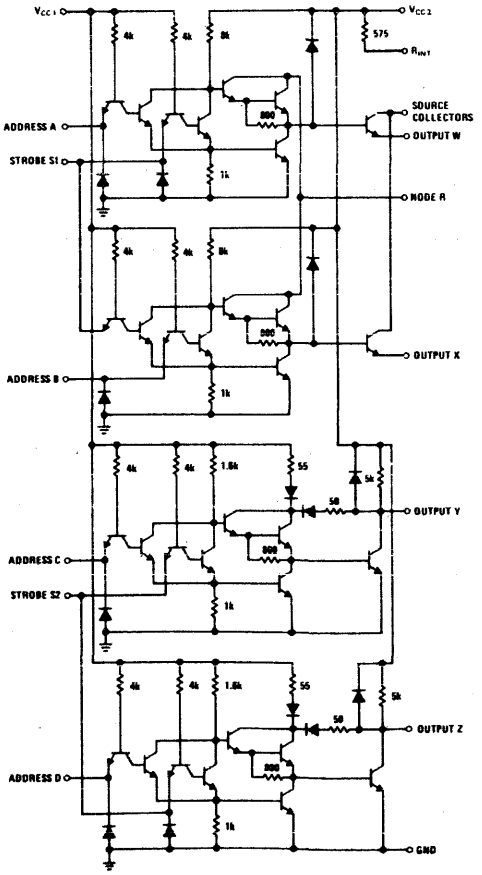
The source stage features Node R which allows extreme flexibility in source current selection by controlling the amount of base drive to each source transistor. This method of setting the base drive brings the power associated with the resistor outside the package thereby allowing the circuit to operate at higher source currents for a given junction temperature. If this method of source current setting is not desired, then Nodes R and R_{INT} can be shorted externally activating an internal resistor connected from V_{CC2} to Node R. This provides adequate base drive for source currents up to 375 mA with V_{CC2} = 15V or 600 mA with V_{CC2} = 24V.

The DS55325 operates over the fully military temperature range of −55°C to +125°C, while the DS5325 operates from 0°C to +70°C.

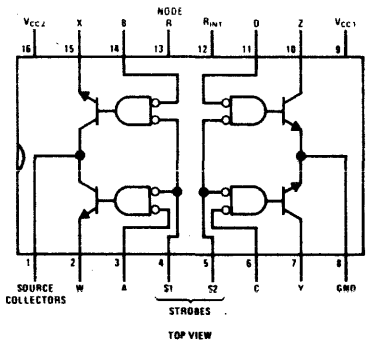
features

- 600 mA output capability
- 24V output capability
- Dual sink and dual source outputs
- Fast switching times
- Source base drive externally adjustable
- Input clamping diodes
- DTL/TTL compatible

schematic and connection diagrams



Dual-In-Line Package



Order Number DS55325J, DS75325J, DS75325N or DS55325W
See Package 10, 15 or 28

truth table

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant

NOTE: Not more than one output is to be on at any one time.

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DS75322 dual TTL-to-MOS driver

general description

The DS75322 is a monolithic integrated dual TTL-to-MOS driver and interface circuit. The device has separate driver address inputs with common strobe. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. The DS75322 is designed for driving N-channel RAMs where low power dissipation is desirable when the driver output is in the low state. It may be used to drive the chip-enable clock of 4096-bit dynamic MOS RAM components.

The DS75322 requires two external PNP transistors per package.

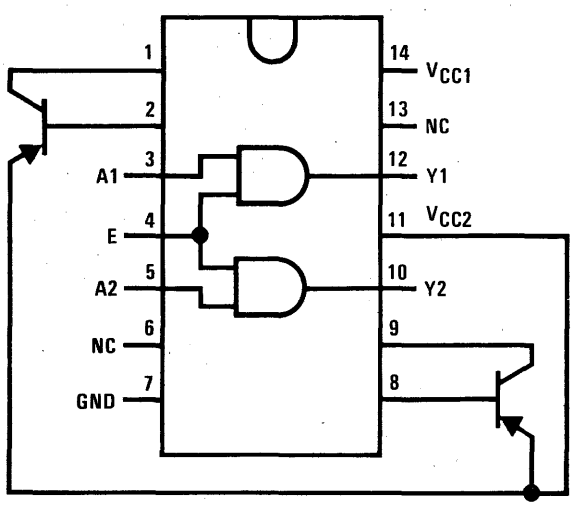
The DS75322 operates from the TTL 5V supply and the MOS V_{DD} supply. With the use of an external pull-down resistor, the driver output of the DS75322 will be forced to the low state upon loss of the 5V supply.

features

- Operates from standard bipolar and MOS supply voltages
- High speed switching
- TTL and DTL compatible inputs
- Separate driver address inputs with common strobe
- V_{OH} and V_{OL} compatible with 4k RAMs
- No 12V supply current (except leakage) when output in low state
- Low 5V supply supply current when output in low state
- Output in high impedance state upon loss of 5V supply
- Requires 2 external PNPs per package for operation

connection diagram

Dual-In-Line Package



TOP VIEW

Positive logic: Y = AE

DS75324 memory driver with decode inputs

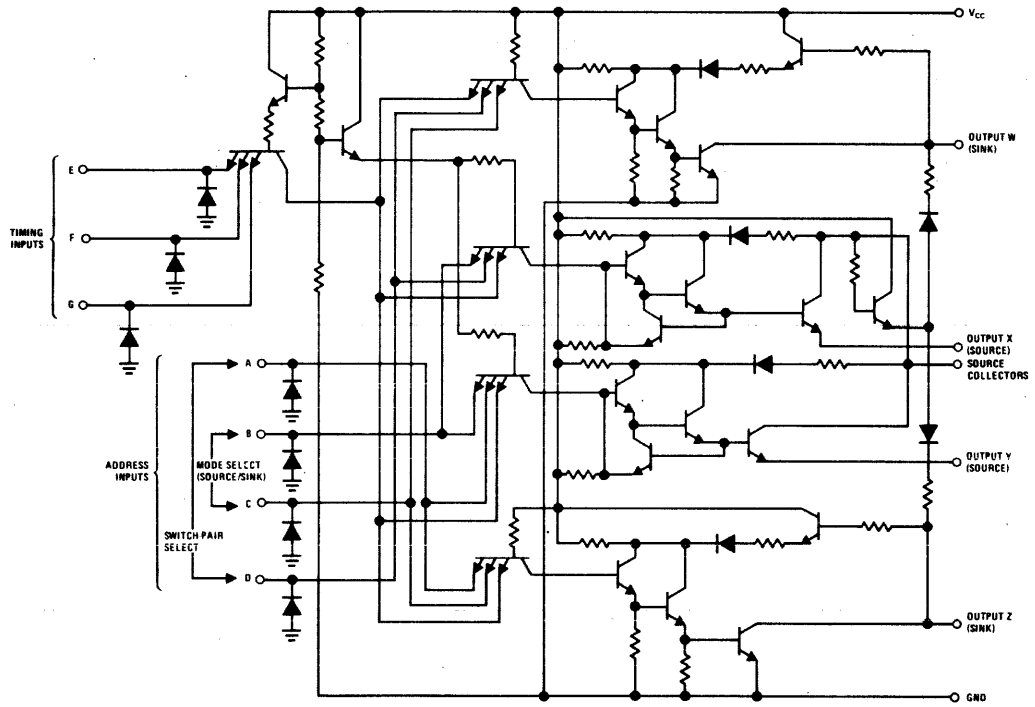
general description

The DS75324 is a monolithic memory driver which features two 400 mA (source/sink) switch pairs along with decoding capability from four address lines. Inputs B and C function as mode selection lines (source or sink) while lines A and D are used for switch-pair selection (output pair Y/Z or W/X).

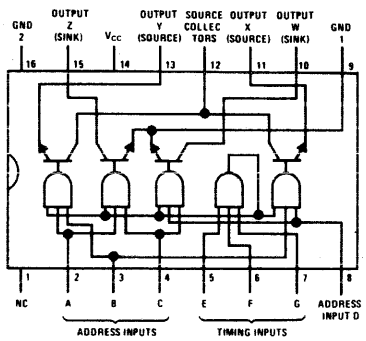
features

- High voltage outputs
- Dual sink/source outputs
- Internal decoding and timing circuitry
- 400 mA output capability
- DTL/TTL compatible
- Input clamping diodes

schematic and connection diagrams



Dual-In-Line Package

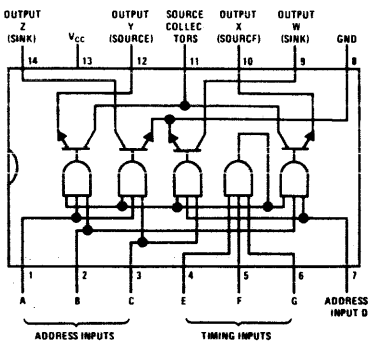


GND 1 and GND 2 are to be used in parallel.

TOP VIEW

Order Number DS75324J
See Package 10

Dual-In-Line Package



TOP VIEW

Order Number DS75324N
See Package 14

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DS75361 dual TTL-to-MOS driver

general description

The DS75361 is a monolithic integrated dual TTL-to-MOS driver interface circuit. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103 and MM5270 and MM5280

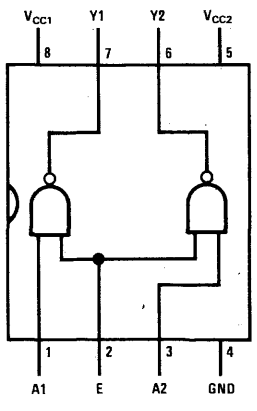
The DS75361 operates from standard TTL 5V supplies and the MOS V_{SS} supply in many applications. The device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V; however, it is designed for use over a much wider range of V_{CC2}.

features

- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- V_{CC2} supply voltage variable over wide range to 24V
- Diode-clamped inputs
- TTL and DTL compatible
- Operates from standard bipolar and MOS supplies
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

connection diagrams

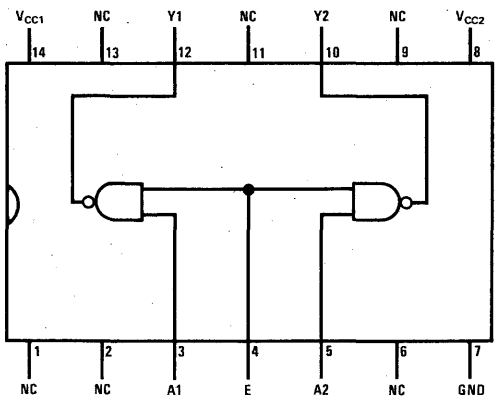
Dual-In-Line Package



TOP VIEW

Order Number DS75361N
See Package 12

Dual-In-Line Package



TOP VIEW

Order Number DS75361J
See Package 9

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DS75362 dual TTL-to-MOS driver

general description

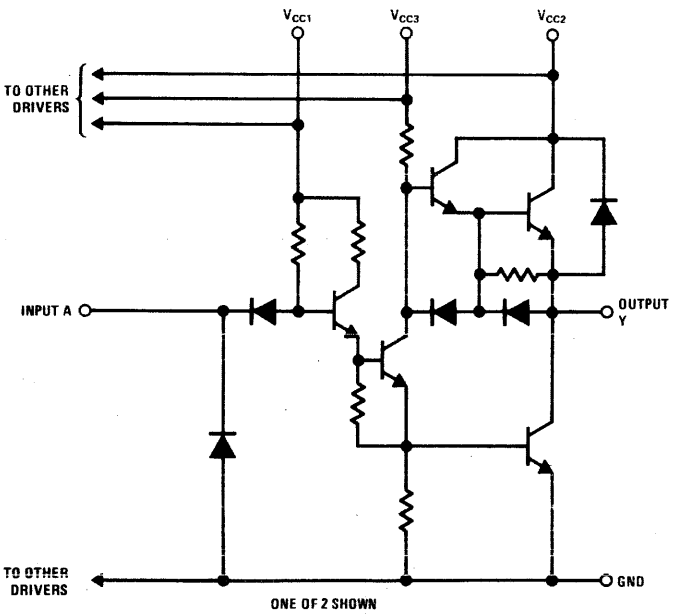
The DS75362 is a dual monolithic integrated TTL-to-MOS driver and interface circuit that accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103.

The DS75362 operates from the TTL 5V supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V, and with nominal V_{CC3} supply voltage from 3V to 4V higher than V_{CC2}. However, it is designed so as to be usable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

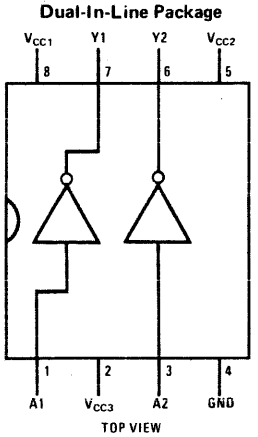
features

- Dual positive-logic NAND TTL-to-MOS driver
- Versatile interface circuit for use between TTL and high-current, high-voltage systems
- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- V_{CC2} supply voltage variable over wide range to 24V maximum
- V_{CC3} supply voltage pin available
- V_{CC3} pin can be connected to V_{CC2} pin in some applications
- TTL and DTL compatible diode-clamped inputs
- Operates from standard bipolar and MOS supply voltages
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

schematic and connection diagrams

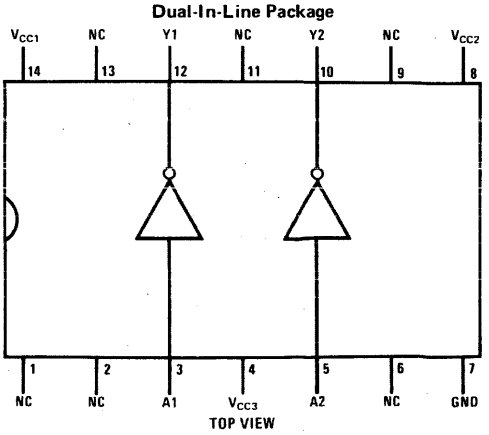


Dual-In-Line Package



Order Number DS75362N
See Package 12

Dual-In-Line Package



Order Number DS75362J
See Package 9

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DS75364 dual MOS clock driver

general description

The DS75364 is a dual MOS driver and interface circuit that operates with either current source or voltage source input signals. The device accepts signals from TTL levels or other logic systems and provides high current and high voltage output levels suitable for driving MOS circuits. It may be used to drive address, control and/or timing inputs for several types of MOS RAMs and MOS shift registers.

The DS75364 operates from standard MOS and bipolar supplies, and has been optimized for operation with V_{CC1} supply voltage from 12–20V positive with respect to V_{EE}, and with nominal V_{CC2} supply voltage from 3–4V more positive than V_{CC1}. However, it is designed so as to be useable over a much wider range of V_{CC1} and V_{CC2}. In some applications the V_{CC2} power supply can be eliminated by connecting the V_{CC2} pin to the V_{CC1} pin.

Inputs of the DS75364 are referenced to the V_{EE} terminal and contain a series current limiting resistor. The device will operate with either positive input current signals or input voltage signals which are positive with respect to V_{EE}. In many applications the V_{EE} terminal is connected to the MOS V_{DD} supply of −12V to −15V with the inputs to be driven from TTL levels or other positive voltage levels. The required negative level shifting may be done with an external PNP transistor current source or by use of capacitive coupling and appropriate input voltage pulse characteristics.

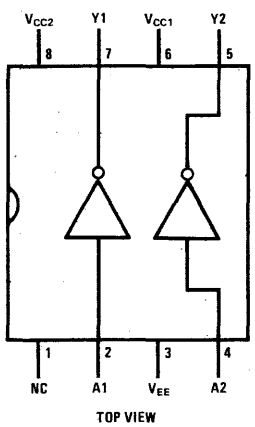
The DS75364 is characterized for operation over the 0°C to +70°C temperature range.

features

- Versatile interface circuit for use between TTL levels and level shifted high current, high voltage systems
- Inputs may be level shifted by use of a current source or capacitive coupling or driven directly by a voltage source
- Capable of driving high capacitance loads
- Compatible with many popular MOS RAMs and MOS shift registers
- V_{CC1} supply voltage variable over wide range to 22V maximum with respect to V_{EE}
- V_{CC2} pull-up supply voltage pin available
- Operates from standard bipolar and/or MOS supply voltages
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

connection diagrams

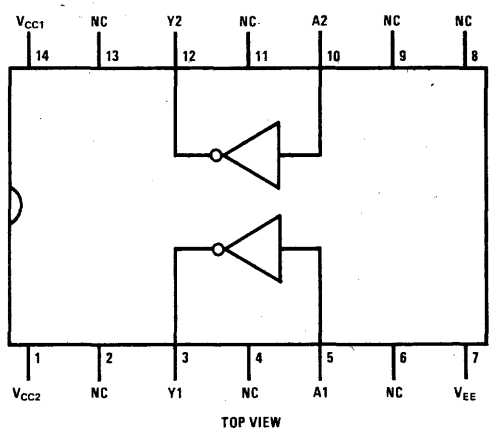
Dual-In-Line Package



TOP VIEW

Order Number DS75364N
See Package 12

Dual-In-Line Package



TOP VIEW

Order Number DS75364J
See Package 9

DS75365 quad TTL-to-MOS driver

general description

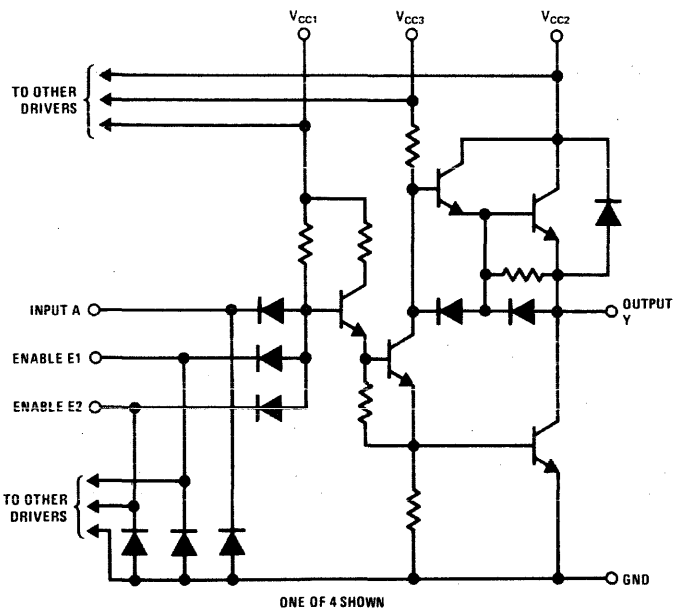
The DS75365 is a quad monolithic integrated TTL-to-MOS driver and interface circuit that accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103.

The DS75365 operates from the TTL 5V supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V, and with nominal V_{CC3} supply voltage from 3V to 4V higher than V_{CC2}. However, it is designed so as to be usable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

features

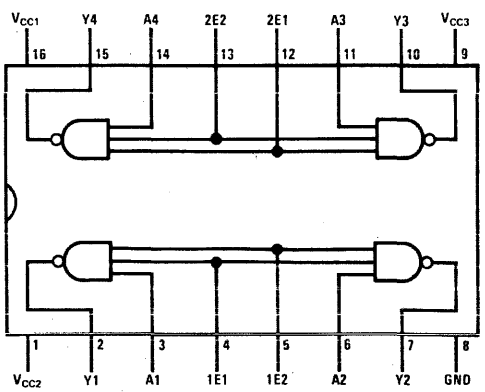
- Quad positive-logic NAND TTL-to-MOS driver
- Versatile interface circuit for use between TTL and high-current, high-voltage systems
- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- Interchangeable with Intel 3207
- V_{CC2} supply voltage variable over wide range to 24V maximum
- V_{CC3} supply voltage pin available
- V_{CC3} pin can be connected to V_{CC2} pin in some applications
- TTL and DTL compatible diode-clamped inputs
- Operates from standard bipolar and MOS supply voltages
- Two common enable inputs per gate-pair
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

schematic and connection diagrams



ONE OF 4 SHOWN

Dual-In-Line Package

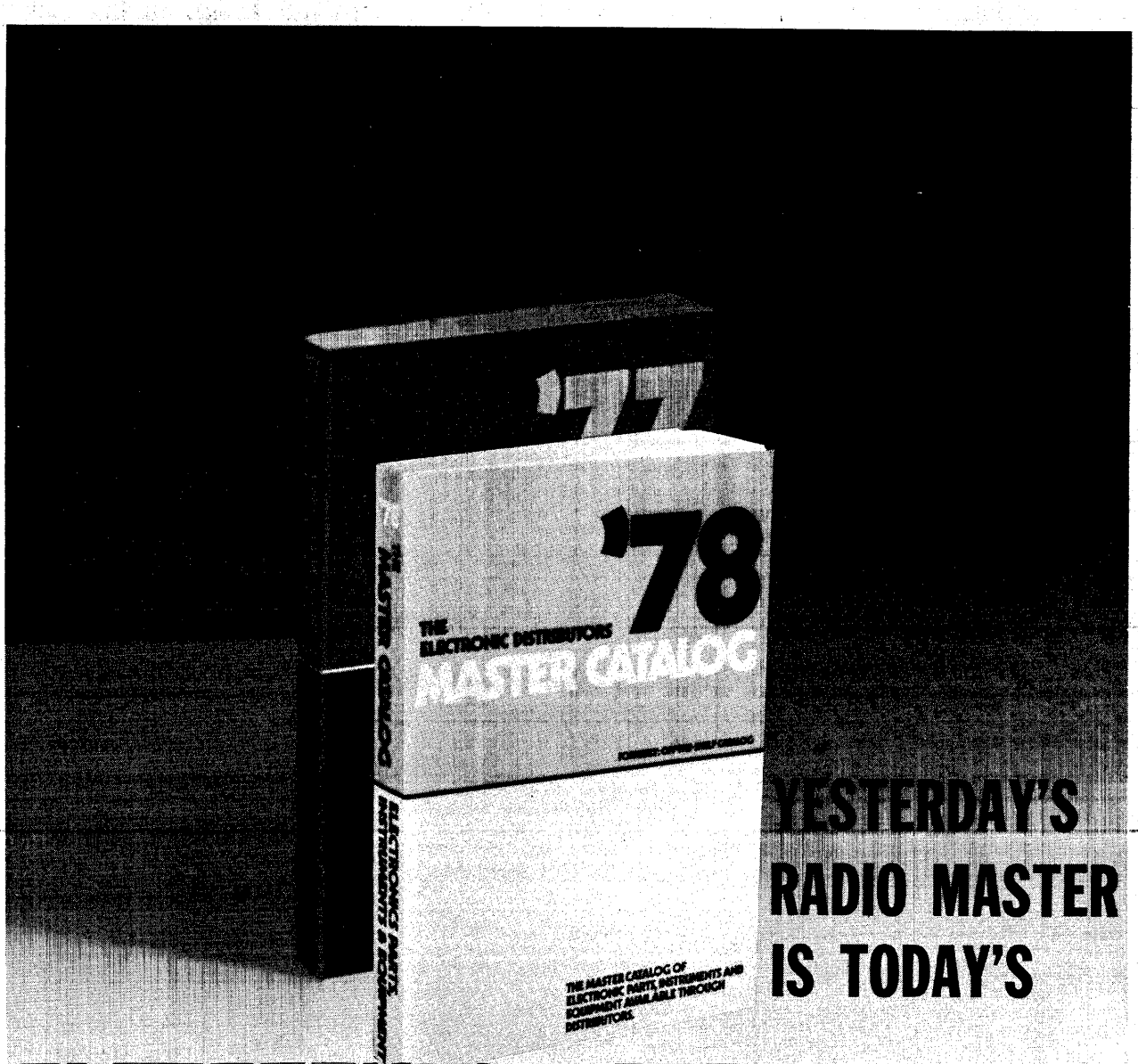


TOP VIEW

Positive Logic: $Y = \overline{A \cdot E1 \cdot E2}$

Order Number DS75365J
or DS75365N
See Package 10 or 15

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ELECTRONIC DISTRIBUTORS MASTER CATALOG

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It encompasses the following product areas: electronic and electromechanical components, audio and communications equipment, subassembly and panel components, hardware, production equipment and tools, test instrumentation, power sources, wire and cable, and chemicals.

The MASTER CATALOG is divided into four basic sections:

The **GENERAL INDEX** lists manufacturers and products alphabetically, including product cross references. Page numbers are displayed for both manufacturers and products. Manufacturers names are **bold-faced.**

The **MANUFACTURERS' CATALOG SECTION** is a collection of their respective product pages, alphabetically by manufacturer, again including addresses and phone numbers.

The **MANUFACTURERS DIRECTORY** is an alphabetical listing of all manufacturers whose products information is shown. Page numbers are referenced. Sales offices, representatives and distributors are included for many manufacturers.

The **DEALER/DISTRIBUTOR DIRECTORY** geographically lists distribution outlets by state and city. The listings were supplied by manufacturers cataloging in this edition.

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Siliconix incorporated

DG300 DG301 DG302 DG303 DG304 DG305 DG306 DG307

OPERATING TEMPERATURE RANGE:
A SUFFIX –55 to +125°C
B SUFFIX –20 to +85°C
C SUFFIX 0 to +70°C

SERIES CMOS ANALOG SWITCHES

LATCHPROOF MONOLITHIC CMOS SWITCH WITH DRIVER

Description

The DG300 through DG307 switch family features four switching functions using CMOS technology for low and nearly constant ON resistance (less than 50 Ω) over the full analog signal range. In the ON condition the switches will conduct current in either direction with no offset voltage. With low power dissipation, (a few milliwatts for the DG300-303, a few hundred microwatts for the DG304-307), this series of switches becomes an ideal candidate for battery-powered or remote switching applications. The switching speed is among the fastest available with the low quiescent power dissipation. In the OFF condition, the switches will block voltages up to 30 V peak-to-peak. A logic input driver controls the ON/OFF state of the switches. (See the "Pin Configuration" for switch status with a logic "1" input.) The DG300-303 switches are TTL and CMOS input compatible and have a logic "0" state with an input less than 0.8 V and a logic "1" state with an input greater than 4.0 V. The DG304-307 switches are CMOS input compatible and have a logic "0" state with an input less than 3.5 V and a logic "1" state with an input greater than 11 V (for 15 V positive supply). The logic inputs are protected against overvoltage up to 18 V above and 36 V below the positive supply. The combination of low cost, low power, low resistance and fast speed optimizes system design.

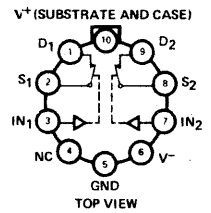
Features

- **Analog Switching With Low Quiescent Power Consumption**
- **Impossible to Latch Up Under Any Circumstances**
- **±15 V Analog Signal Range With ±15 V Supplies**
- **$r_{DS} < 50\ \Omega$ Over Full Signal Range**
- **Fast Switching Speed – t_{on} = 150 ns Typ (DG300-303)**
  t_{on} = 110 ns Typ (DG304-307)
- **DG300-303 TTL, DTL, CMOS Input Compatible**
- **DG304-307 CMOS Input Compatible**
- **All Terminals Protected Against Static Electricity**
- **Logic Inputs Overvoltage Protected to 18 V Above or 36 V Below the Positive Supply**
- **Four Different Switch Functions to Give Optimum Flexibility**

PIN CONFIGURATIONS

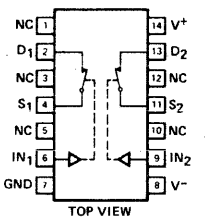
DUAL SPST DG300 or DG304

Metal Can Package



ORDER NUMBERS:
DG300AA OR DG300BA
DG304AA OR DG304BA

Dual-In-Line and Flat Package



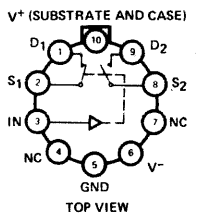
ORDER NUMBERS:
DG300AP OR DG300BP
DG304AP OR DG304BP

DG300CJ
DG304CJ

DG300AL OR DG300BL
DG304AL OR DG304BL

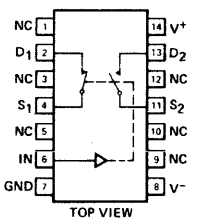
SPDT DG301 or DG305

Metal Can Package



ORDER NUMBERS:
DG301AA OR DG301BA
DG305AA OR DG305BA

Dual-In-Line and Flat Package



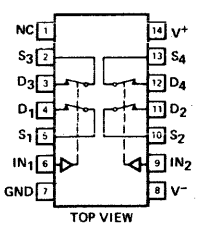
ORDER NUMBERS:
DG301AP OR DG301BP
DG305AP OR DG305BP

DG301CJ
DG305CJ

DG301AL OR DG301BL
DG305AL OR DG305BL

DUAL DPST DG302 or DG306

Dual-In-Line and Flat Package



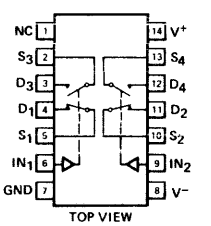
ORDER NUMBERS:
DG302AP OR DG302BP
DG306AP OR DG306BP

DG302CJ
DG306CJ

DG302AL OR DG302BL
DG306AL OR DG306BL

DUAL SPDT DG303 or DG307

Dual-In-Line and Flat Package



ORDER NUMBERS:
DG303AP OR DG303BP
DG307AP OR DG307BP

DG303CJ
DG307CJ

DG303AL OR DG303BL
DG307AL OR DG307BL

SWITCH STATES ARE FOR LOGIC "1" INPUTS (POSITIVE LOGIC)

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ABSOLUTE MAXIMUM RATINGS

V_{IN} to Ground	V^+ +18 V, V^+ −36 V
V_S or V_D	V^+ to V^-
V^+ to Ground	+36 V
V^+ to V^-	+36 V
Current, Any Terminal (Except S or D)	30 mA
Current, S or D, Continuous	30 mA
Pulsed 1 ms 10% Duty Cycle	100 mA
Operating Temperature (A Suffix)	−55 to +125°C
(B Suffix)	−20 to +85°C
(C Suffix)	0 to +70°C
Storage Temperature (A & B Suffix)	−65 to +150°C
(C Suffix)	−65 to +125°C

Power Dissipation*	
14 Pin Sidebraze DIP (P)**	825 mW
14 Pin Plastic DIP (J)***	470 mW
Metal Can (A)****	450 mW
Flat Package (L)*****	750 mW

*Device mounted with all leads welded or soldered to PC board.
**Derate 11 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C
****Derate 6 mW/°C above 75°C
*****Derate 10 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		Characteristics			Typ[1] 25°C	Max Limits A/B Suffix −55°C/−20°C	A/B Suffix 25°C	A/B Suffix 125°C/85°C	C Suffix 0°C	C Suffix 25°C	C Suffix 70°C	Unit	Test Conditions V^+ = +15 V, V^- = −15 V, Gnd = 0 V	
1	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance		30	50	50	75	50	50	75	Ω	V_D = +10 V, I_S = −10 mA	Note 2
2					30	50	50	75	50	50	75		V_D = −10 V, I_S = +10 mA	
3		$I_{S(off)}$	Source OFF Leakage Current		0.1		1	100		5	100	nA	V_S = +15 V, V_D = −15 V	Note 2
4					−0.1		−1	−100		−5	−100		V_S = −15 V, V_D = +15 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		0.1		1	100		5	100		V_D = +15 V, V_S = −15 V	
6					−0.1		−1	−100		−5	−100		V_D = −15 V, V_S = +15 V	
7		$I_{D(on)}$	Channel ON Leakage Current		0.1		1	100		5	100		V_D = V_S = +15 V	Note 2
8					−0.1		−2	−200		−5	−200		V_D = V_S = −15 V	
9	INPUTS	I_{INH}	Input Current Input Voltage High	DG300-303 Only	−0.001	−1	−1	−1		−1		μA	V_{IN} = +5 V	
10				DG300-307	0.001	1	1	1		1			V_{IN} = +15 V	
11		I_{INL}	Input Current Input Voltage Low		−0.001	−1	−1	−1		−1			V_{IN} = 0	
12	DYNAMIC	t_{on}	Turn ON Time	DG300-303 Only	150		300					nS	See Switching Time Test Circuit	
13		t_{off}	Turn OFF Time		130		250							
14		t_{on}	Turn ON Time	DG304-307 Only	110		250							
15		t_{off}	Turn OFF Time		70		150							
16		$t_{on} - t_{off}$	Break-Before-Make Interval	DG301/303 DG305/307 Only	50								See Break-Before-Make Time Test Circuit	
17		$C_{S(off)}$	Source OFF Capacitance		14							pF	V_S = 0, Note 2	f = 1 MHz
18		$C_{D(off)}$	Drain OFF Capacitance		14								V_D = 0, Note 2	
19		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		40								V_D = V_S = 0, Note 2	
20		C_{IN}	Input Capacitance		6								V_{IN} = 0	
21					3.5								V_{IN} = +15 V	
22			OFF Isolation[3]		62							dB	V_{IN} = 0, R_L = 1K Ω, C_L = +15 pF V_S = 1 V_{RMS}, f = 500 kHz	
23	SUPPLY	I_1	Positive Supply Current	DG300-303 Only	0.23	1	0.5	0.5		1		mA	V_{IN} = 4 V (One Input) (All Other Inputs = 0)	
24		I_2	Negative Supply Current		−0.001	−10	−10	−100		−100		μA		
25		I_1	Positive Supply Current		0.001	10	10	100		100			V_{IN} = 0.8 V (All Inputs)	
26		I_2	Negative Supply Current		−0.001	−10	−10	−100		−100				
27		I_1	Positive Supply Current	DG304-307 Only	0.001	10	10	100		100			V_{IN} = +15 V (All Inputs)	
28		I_2	Negative Supply Current		−0.001	−10	−10	−100		−100				
29		I_1	Positive Supply Current		0.001	10	10	100		100			V_{IN} = 0 (All Inputs)	
30		I_2	Negative Supply Current		−0.001	−10	−10	−100		−100				

NOTES:

1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. V_{IN} = Input voltage to perform proper function, DG300-303: V_{IN} – For logic "1" = 4 V, for logic "0" = 0.8 V
   DG304-307: V_{IN} – For logic "1" = 11 V, for logic "0" = 3.5 V
3. "OFF" Isolation $\triangleq$ 20 log V_S/V_D. V_S = Input to OFF switch, V_D = Output

DG300 ICMA-A DG302 ICMB-A
DG301 ICMA-B DG303 ICMB-B
DG304 ICMA-C DG306 ICMB-C
DG305 ICMA-D DG307 ICMB-D

Siliconix incorporated

DG381 DG384 DG387 DG390

OPERATING TEMPERATURE RANGE:
A SUFFIX –55 to +125°C
B SUFFIX –20 to +85°C
C SUFFIX 0 to +70°C

SERIES CMOS ANALOG SWITCHES

LATCHPROOF MONOLITHIC CMOS SWITCH WITH DRIVER

Description

The DG381 through DG390 switch family features four switching functions using CMOS technology for low and nearly constant ON resistance (less than 50 Ω) over the full analog signal range. In the ON condition the switches will conduct current in either direction with no offset voltage. With low power dissipation, a few milliwatts, this series of switches becomes an ideal candidate for battery-powered or remote switching applications. The switching speed is among the fastest available with the low quiescent power dissipation. In the OFF condition, the switches will block voltages up to 30 V peak-to-peak. A logic input driver controls the ON/OFF state of the switches. (See the "Pin Configuration" for switch status with a logic "1" input.) The switches are TTL and CMOS input compatible and have a logic "0" state with an input less than 0.8 V and a logic "1" state with an input greater than 4.0 V. The logic inputs are protected against overvoltage up to 18 V above and 36 V below the positive supply. The combination of low cost, low power, low resistance and fast speed optimizes system design.

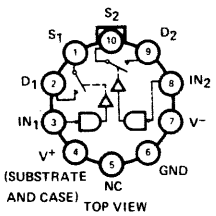
Features

- **Pin for Pin Compatible with DG181-190 Series**
- **Analog Switching with Low Quiescent Power Consumption**
- **Impossible to Latch Up Under Any Circumstances**
- **±15 V Analog Signal Range with ±15 V Supplies**
- **$r_{DS} < 50\ \Omega$ Over Full Signal Range**
- **Fast Switching Speed – t_{on} = 150 ns Typ**
- **TTL, DTL, CMOS Input Compatible**
- **All Terminals Protected Against Static Electricity**
- **Logic Inputs Overvoltage Protected to 18 V Above or 36 V Below the Positive Supply**
- **Four Different Switch Functions to Give Optimum Flexibility**

PIN CONFIGURATIONS

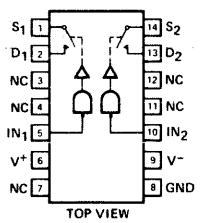
DUAL SPST DG381

Metal Can Package



ORDER NUMBERS:
DG381AA OR DG381BA

Dual-In-Line Package

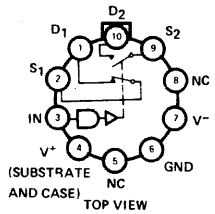


ORDER NUMBERS:
DG381AP OR DG381BP

DG381CJ

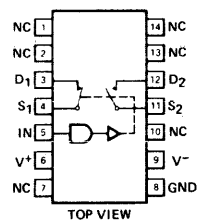
SPDT DG387

Metal Can Package



ORDER NUMBERS:
DG387AA OR DG387BA

Dual-In-Line Package

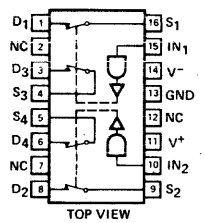


ORDER NUMBERS:
DG387AP OR DG387BP

DG387CJ

DUAL DPST DG384

Dual-In-Line Package

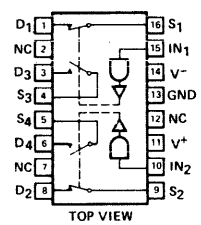


ORDER NUMBERS:
DG384AP OR DG384BP

DG384CJ

DUAL SPDT DG390

Dual-In-Line-Package



ORDER NUMBERS:
DG390AP OR DG390BP

DG390CJ

SWITCH STATES ARE FOR LOGIC "1" INPUTS (POSITIVE LOGIC)

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ABSOLUTE MAXIMUM RATINGS

V_{IN} to Ground . . . . . V^+ +18 V, V^+ −36 V
V_S or V_D . . . . . V^+, V^-
V^+ to Ground . . . . . +36 V
V^+ to V^- . . . . . +36 V
Current, Any Terminal (Except S or D) . . . . 30 mA
Current, S or D, Continuous . . . . . 30 mA
Pulsed 1 ms 10% Duty Cycle . . . . . 100 mA
Operating Temperature (A Suffix) . . −55 to +125°C
(B Suffix) . . −20 to +85°C
(C Suffix) . . . 0 to +70°C
Storage Temperature (A & B Suffix) . . −65 to +150°C
(C Suffix) . . . . −65 to +125°C

Power Dissipation*
14 Pin Sidebraze DIP (P)** . . . . . 825 mW
14 Pin Plastic DIP (J)*** . . . . . 470 mW
Metal Can (A)**** . . . . . 450 mW

*Device mounted with all leads welded or soldered to PC board.
**Derate 11 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C
****Derate 6 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

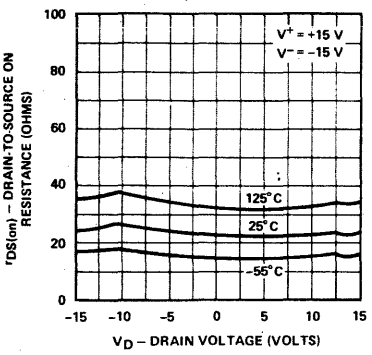
		Characteristics		Typ[1] 25°C	Max Limits A/B Suffix −55°C/−20°C	A/B Suffix 25°C	A/B Suffix 125°C/85°C	C Suffix 0°C	C Suffix 25°C	C Suffix 70°C	Unit	Test Conditions V^+ = +15 V, V^- = −15 V, Gnd = 0 V	
1	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	30	50	50	75	50	50	75	Ω	V_D = +10 V, I_S = −10 mA	Note 2
2				30	50	50	75	50	50	75		V_D = −10 V, I_S = +10 mA	
3		$I_{S(off)}$	Source OFF Leakage Current	0.1		1	100		5	100	nA	V_S = +15 V, V_D = −15 V	Note 2
4				−0.1		−1	−100		−5	−100		V_S = −15 V, V_D = +15 V	
5		$I_{D(off)}$	Drain OFF Leakage Current	0.1		1	100		5	100		V_D = +15 V, V_S = −15 V	
6				−0.1		−1	−100		−5	−100		V_D = −15 V, V_S = +15 V	
7		$I_{D(on)}$	Channel ON Leakage Current	0.1		1	100		5	100		V_D = V_S = +15 V	Note 2
8				−0.1		−2	−200		−5	−200		V_D = V_S = −15 V	
9	IN	I_{INH}	Input Current Input Voltage High	−0.001	−1	−1	−1		−1		μA	V_{IN} = +5 V	
10				0.001	1	1	1		1			V_{IN} = +15 V	
11		I_{INL}	Input Current Input Voltage Low	−0.001	−1	−1	−1		−1			V_{IN} = 0	
12	DYNAMIC	t_{on}	Turn ON Time	150		300					nS	See Switching Time Test Circuit	
13		t_{off}	Turn OFF Time	130		250							
14		$t_{on} - t_{off}$	Break-Before-Make Interval DG387/390 only	50								See Break-Before-Make Time Test Circuit	
15		$C_{S(off)}$	Source OFF Capacitance	14							pF	V_S = 0, Note 2	f = 1 MHz
16		$C_{D(off)}$	Drain OFF Capacitance	14								V_D = 0, Note 2	
17		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	40								V_D = V_S = 0, Note 2	
18		C_{IN}	Input Capacitance	6								V_{IN} = 0	
19				3.5								V_{IN} = +15 V	
20			OFF Isolation[3]	62							dB	V_{IN} = 0, R_L = 1K Ω, C_L = +15 pF V_S = 1 V_{RMS}, f = 500 kHz	
21	SUPPLY	I_1	Positive Supply Current	0.23	1	0.5	0.5		1		mA	V_{IN} = 4 V (One Input) (All Other Inputs = 0)	
22		I_2	Negative Supply Current	−0.001	−10	−10	−100		−100		μA		
23		I_1	Positive Supply Current	0.001	10	10	100		100			V_{IN} = 0.8 V (All Inputs)	
24		I_2	Negative Supply Current	−0.001	−10	−10	−100		−100				

NOTES:
1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing
2. V_{IN} = Input voltage to perform proper function, V_{IN} for logic "1" = 4 V, for logic "0" = 0.8 V
3. "OFF" Isolation $\triangleq$ 20 log V_S/V_D = Input to OFF switch, V_D = Output

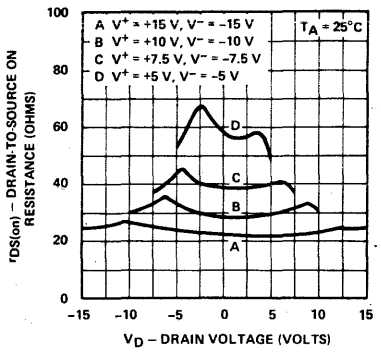
DG381 ICMA-E **DG384 ICMB A**
DG387 ICMA B **DG390 ICMB B**

TYPICAL CHARACTERISTICS

$r_{DS(on)}$ vs V_D and Temperature

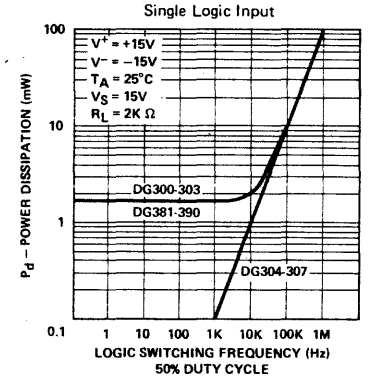


$r_{DS(on)}$ vs V_D and Power Supply Voltage

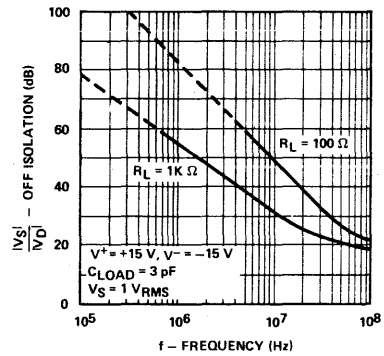


Device Power Dissipation vs Switching Frequency

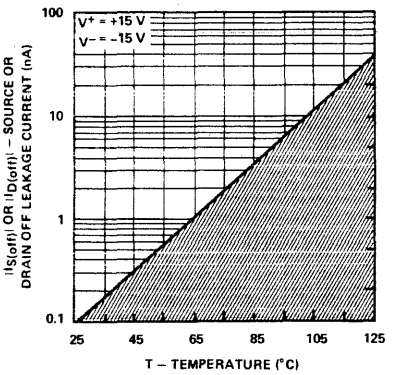
Single Logic Input



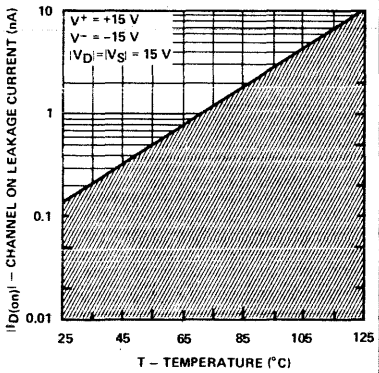
OFF Isolation vs Frequency



$I_{S(off)}$ or $I_{D(off)}$ vs Temperature*

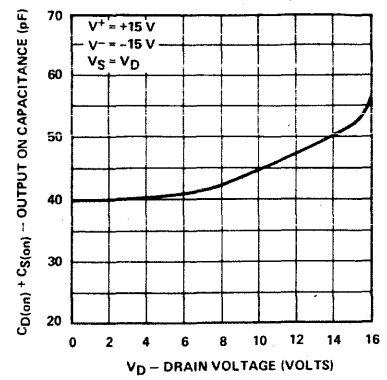


$I_{D(on)}$ vs Temperature*

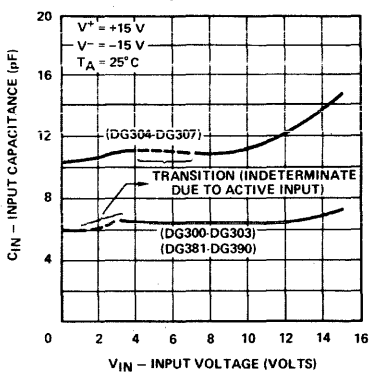


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

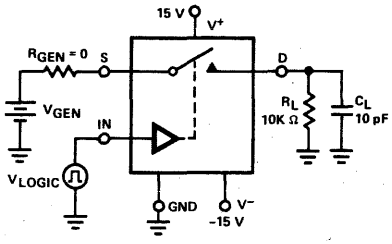
Output ON Capacitance vs Drain Voltage



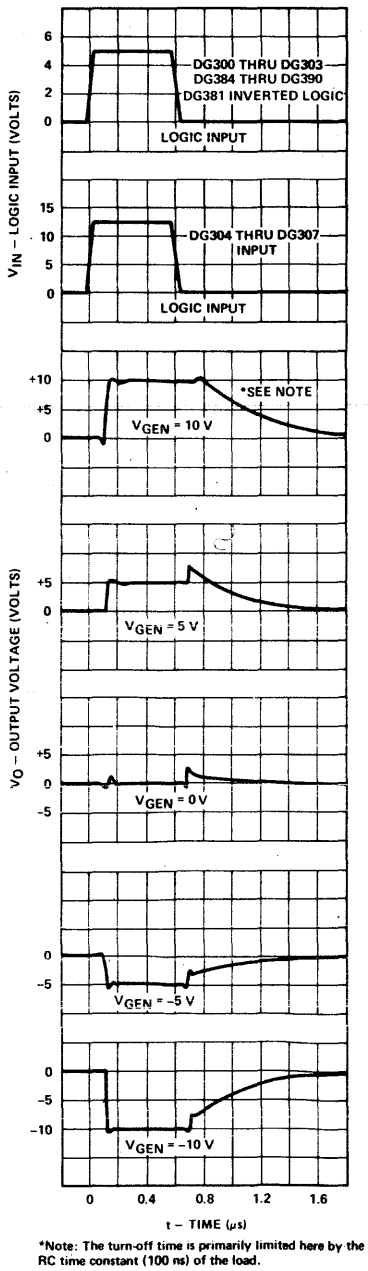
Input Capacitance vs Input Voltage



Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times. Applying V_{GEN} to D rather than S results in much greater spikes.

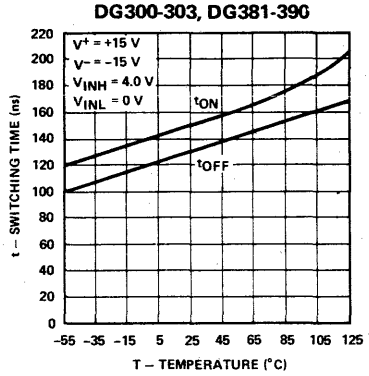


*Note: The turn-off time is primarily limited here by the RC time constant (100 ns) of the load.

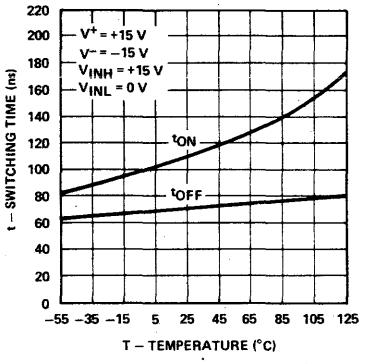
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TYPICAL CHARACTERISTICS (Cont'd)

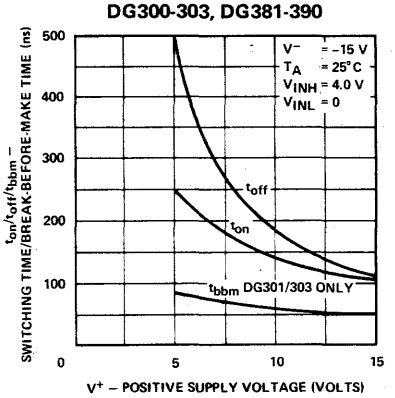
Switching Time vs Temperature
DG300-303, DG381-390



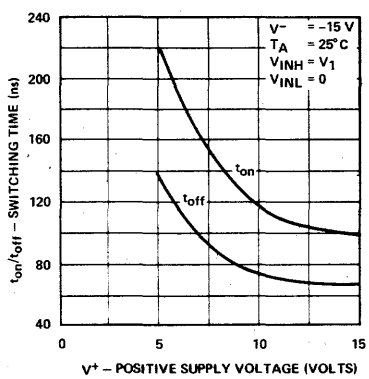
Switching Time vs Temperature
DG304-307



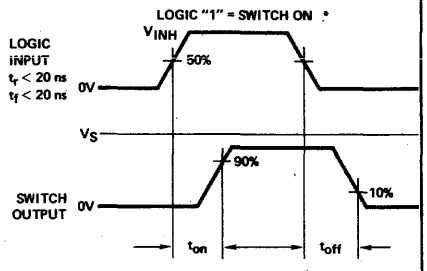
Switching Time and Break-Before-Make Time vs Positive Supply Voltage
DG300-303, DG381-390



Switching Time vs Positive Supply Voltage
DG304-307

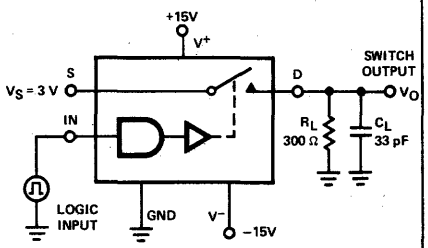


SWITCHING TIME TEST CIRCUIT (DG300-307 DG381-390)

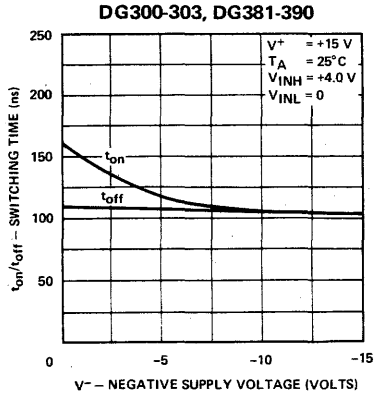


		VINH
DG300-303	DG381-DG390	4 V
DG304-307		15 V

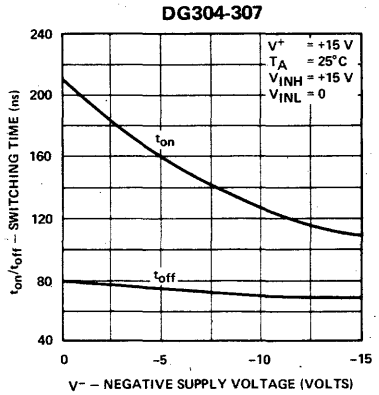
*INVERTED LOGIC FOR DG381



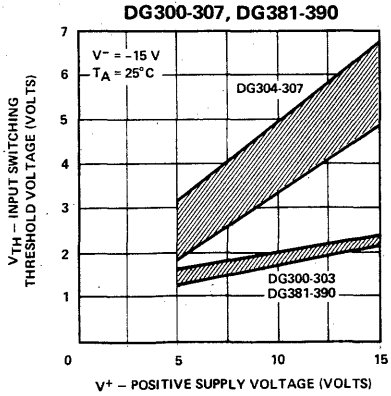
Switching Time vs Negative Supply Voltage
DG300-303, DG381-390



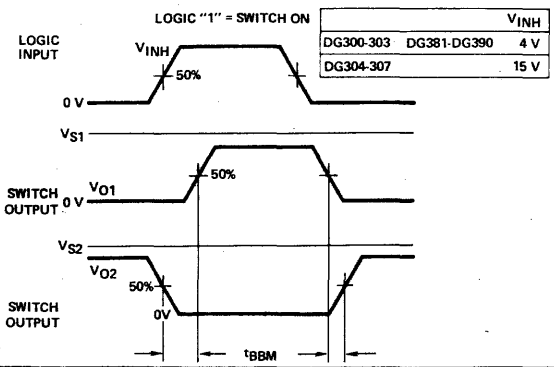
Switching Time vs Negative Supply Voltage
DG304-307



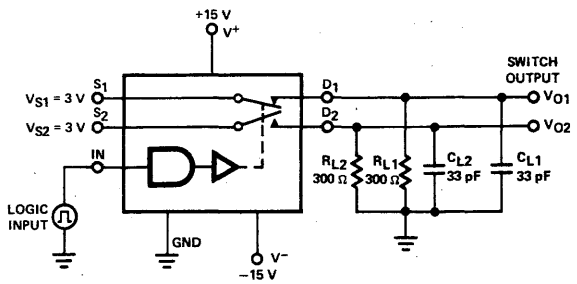
Input Switching Threshold vs Positive Supply Voltage
DG300-307, DG381-390



BREAK-BEFORE-MAKE TIME TEST CIRCUIT SPDT (DG301, DG303, DG305, DG307, DG384, DG390)

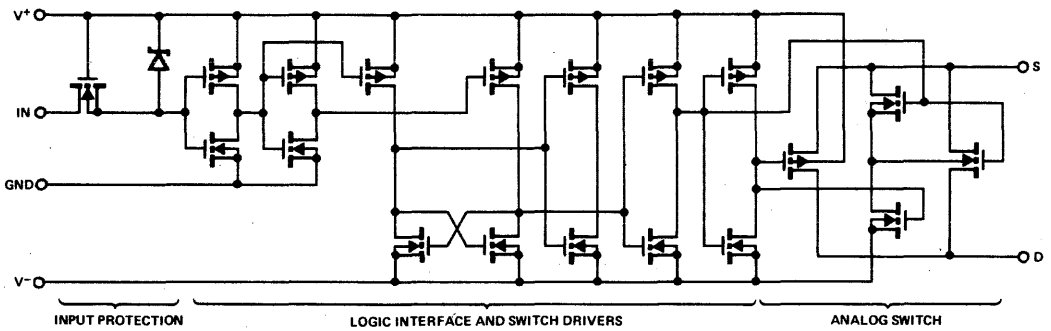


		VINH
DG300-303	DG381-DG390	4 V
DG304-307		15 V



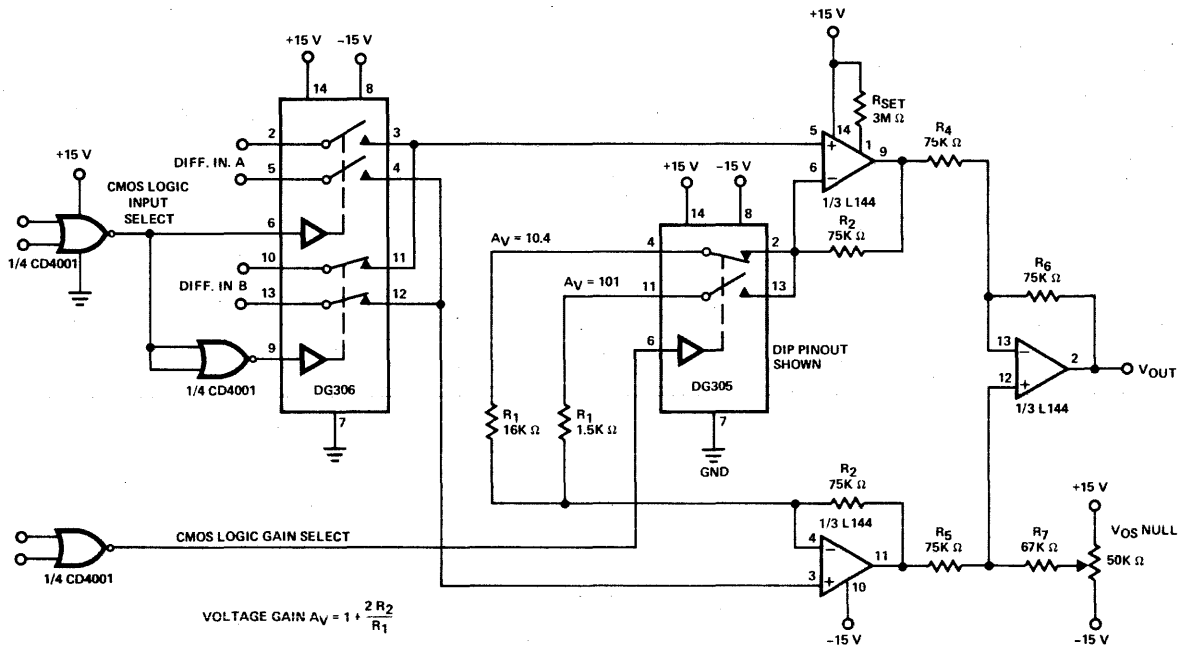
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PARTIAL SCHEMATIC OF TYPICAL SWITCH (DG300-307, DG381-390)

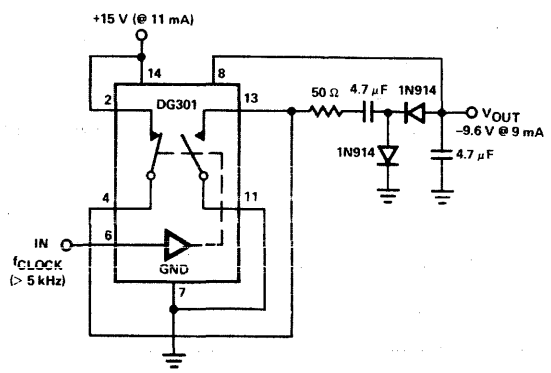


APPLICATIONS

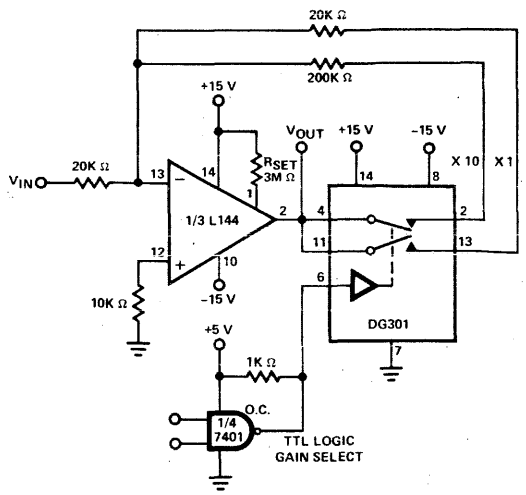
Low Power Instrumentation Amplifier With Digitally Selectable Inputs and Gain



Negative Voltage Converter For Use In Single Supply Systems



Low Power Inverting Amplifier With Digitally Selectable Gain



©IC MASTER 1978

Siliconix incorporated

LD110 LD111 LD111A LD114

OPERATING TEMPERATURE RANGE:
C SUFFIX 0 to +70°C

3 1/2 DIGIT A/D CONVERTER SETS

LD110/LD114 DIGITAL A/D PROCESSOR
LD111/LD111A ANALOG A/D PROCESSOR

Description

The PMOS LD110 synchronous digital processor combines the counting, storage and data multiplexing functions with the random logic necessary to control the quantized charge-balancing function of the analog processor. Seventeen static latches store the 3½ digits of BCD data as well as overrange, underrange and polarity information. Nine push-pull output buffers (capable of driving one standard TTL load each) provide the sign, digit strobe and multiplexed BCD data outputs, all of which are active high. The digit scan is an interlaced format of digits 1, 3, 2 and 4.

The monolithic LD111 analog processor contains a bipolar comparator, a bipolar integrating amplifier, two MOSFET input unity gain amplifiers, several P-Channel enhancement mode analog switches and the necessary level shifting drivers to allow the analog and digital processors to be directly interfaced. A wide range of conversion rates (1/3 to 12 samples per second) as well as two voltage ranges can be accommodated using externally determined RC time constants. All amplifiers are internally compensated.

The monolithic LD111A high performance analog processor contains a bipolar comparator, a bipolar integrating amplifier, a bipolar reference amplifier, two MOSFET input unity gain amplifiers, several P-channel enhnacement mode analog switches and the necessary level shifting drivers to allow the analog and digital processors to be directly interfaced. The high impedance input and reference buffer amplifiers eliminate source loading errors and provide the outstanding temperature coefficient inherent in this system. Break-before-make switch action insures that neither the analog input nor the reference voltage will be shorted to ground at any time.

The PMOS LD114 digital processor combines the counting storage and data multiplexing functions with the random logic necessary to control the quantized charge-balancing function of the analog processor. Seventeen static latches, in response to external control, store the 3 1/2 Digits of BCD data as well as underrange and polarity information. Ten push-pull output buffers (capable of driving one standard TTL load) provide the clock frequency ÷ 512, sign, digit strobe and multiplexed BCD data. Four data output format options allow the user to tailor the BCD output to his circuit requirements.

Features

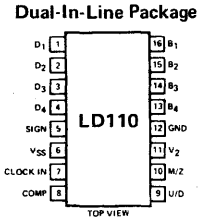
- 0.05% Accuracy (of reading) ±1 Count (LD110/LD111)
- 0.02% Accuracy (of reading) ±1 Count (LD110/LD111A)
- Two Voltage Ranges — 1.999 V and 199.9 mV
- Sampling Rates up to 12 Samples/Sec.
- FET Input for $Z_{in} > 1000M\ \Omega$
- Auto-Zero Minimizes Effects of Offset, Drift and Temperature
- 10 μV Resolution (A Usable 20 mV Scale) (LD110/LD111A)
- Auto-Polarity
- Differential Input Capability
- External Latch Inhibit Control (LD114)
- Multiplexed Parallel BCD or Serial BCD Output (LD114)
- Active High or Active Low Logic Outputs (LD114)
- Overrange and Underrange Signals Available for Auto-Ranging Capability
- ÷512 Output Available for Phase Locked Loop Clock (LD114)
- TTL Compatible Outputs
- LD111A Directly Replaces LD111
- Typical T.C. of 5 ppm/°C (LD111A)

Applications

- DVM/DPM
- Micro Processor Interface
- Controllers
- Digital Weighing Systems
- Digital Thermometers
- Instrumentation
- Sampling A/D Converter

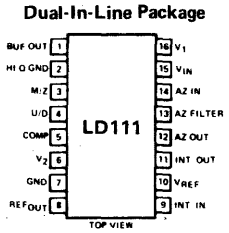
PIN CONFIGURATIONS

Dual-In-Line Package



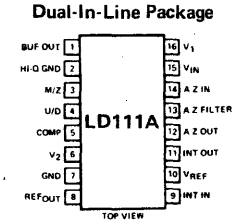
ORDER NUMBER: LD110CJ

Dual-In-Line Package



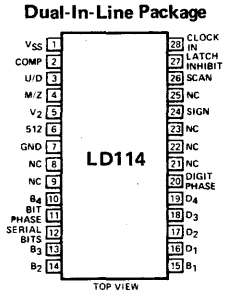
ORDER NUMBER: LD111CJ

Dual-In-Line Package



ORDER NUMBER: LD111ACJ

Dual-In-Line Package



ORDER NUMBER: LD114CR

Siliconix incorporated

DF411

OPERATING TEMPERATURE RANGE:
C SUFFIX 0 to 70°C

4 DIGIT LCD DECODER DRIVER

MONOLITHIC CMOS FOUR DIGIT DECODER DRIVER

Description

The DF411 Four Digit LCD Decoder Driver is a CMOS Monolithic multiplexed BCD to LCD Decoder Driver. One DF411 contains all of the circuitry needed to decode up to 4 digits of multiplexed BCD information and derive the AC signals needed to drive a 4 digit LCD display.

An on board oscillator, its frequency being controlled by an external capacitor, develops a backplane (BP) signal which is a square wave swinging between ground (V_{SS}) and the positive supply (V_{DD}). Segment drivers supply square waves of the same frequency as the backplane but either in phase for an OFF segment or out of phase for an ON segment. In this manner of LCD digit driving the net DC voltage applied between segment and backplane is zero, a necessary requirement for long display life. Digital input levels are defined as input voltages > 5V being a logic "1" and input voltages < 0.8V being a logic "0" with V_{DD} = 6V.

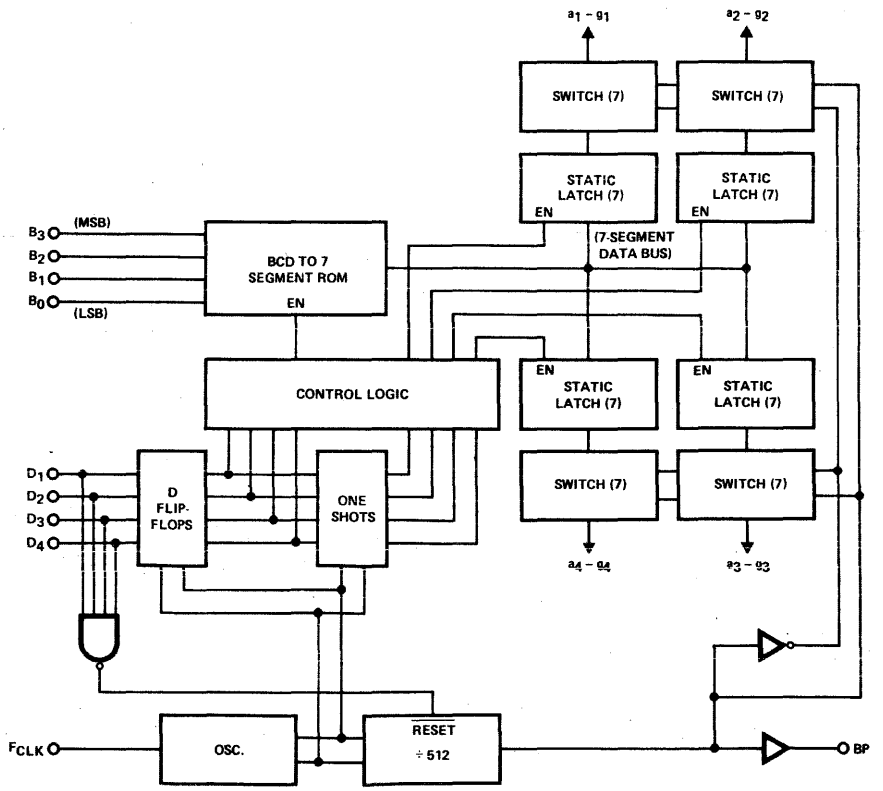
BCD input data is decoded into 7 segment form using an on board ROM. The 7 segment data is then latched into the appropriate static latches via the digit strobe inputs and control logic.

The pinout of the DF411 allows easy PC board interfaces to Dual In-Line LCDs as well as edge connecting types of displays.

Features

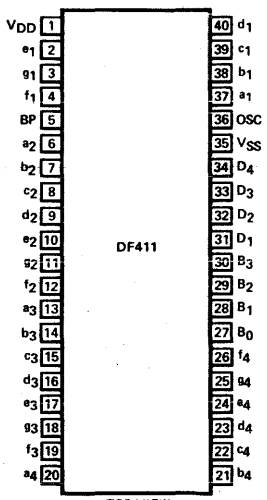
- **Decodes MUX BCD to LCD 7 Segments**
- **4 Digit Drive Capability**
- **Low Power Consumption**
- **TTL (Open Collector), DTL, CMOS Input Compatible**
- **Easy LCD/Driver Interfacing**
- **Internal Oscillator**
- **AC LCD Drive Signals**
- **Drives Large LCD Displays Easily**
- **Can be Clocked Using an External Oscillator**
- **Reset Capability Allows Easy Ganging of Devices to Drive More than 4 Digits**

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

Dual-In-Line Package



TOP VIEW
V_{DD} COMMON TO SUBSTRATE

ORDER NUMBER: DF411CJ

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Siliconix incorporated

LD130 LD131

OPERATING TEMPERATURE RANGE:
B SUFFIX −20 to +85°C
C SUFFIX 0 to +70°C

LD130 ±3 DIGIT A/D CONVERTER
LD131 ±3 1/3 DIGIT A/D CONVERTER

MONOLITHIC CMOS CONVERTERS

Description

The LD130 combines both the analog and digital subsystems of a 3 digit A/D system in a single monolithic CMOS I.C. The "Quantized Feedback" conversion scheme, introduced by Siliconix, provides the LD130 with an Auto-zero, Auto-polarity A/D system requiring only a single reference voltage. External parts are minimized by the on-chip resistors and buffer amplifiers. These high impedance input and reference buffer amplifiers eliminate source loading errors providing the outstanding temperature coefficient and ratio operation inherent in this system. Break-before-make switch action insures that neither the analog input nor the reference voltage will be shorted to ground at any time.

The LD130 3 digit A/D is made functionally complete by the following additions:

1. C_{AZ} (0.10 μF) between AZ and Σ pins
2. C_{INT} (0.033 μF) between INT and Σ pins
3. C_{OSC} (0.001 μF) between OSC and Digital Ground
4. $V_{REF} \cong 2.000$ V
5. ±5 V supplies (@ 3 mA)

The LD131 is functionally equivalent to the 3 digit LD130 A/D converter with the exception of not having overrange blinking when the count exceeds 999.

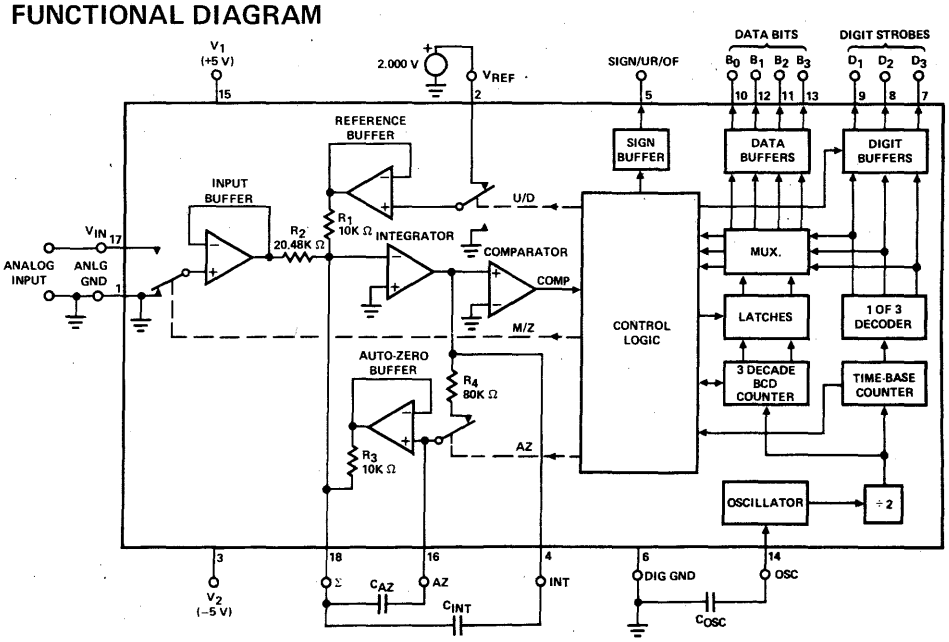
Features

- Low Cost
- Accuracy of 0.1% (of reading) ±1 Count
- Auto-Zero
- Auto-Polarity
- Low Power Consumption (25 mW Typical)
- 1 mV Resolution (1.000 V Full Scale LD130)
- 1 mV Resolution (1.500 V Full Scale LD131)
- Minimum of External Components (3 Capacitors, 1 Reference)
- Buffered Analog Input ($Z_{IN} > 1000M\,\Omega$)
- Buffered Reference Input ($Z_{IN} > 1000M\,\Omega$)
- Internal Clock Oscillator
- Overrange and Underrange Signals Provided for Auto-ranging
- Multiplexed BCD with Inter-Digit Blanking
- TTL Compatible Outputs (1 Load)
- Sampling Rates from 1 to 60 samples/second

Applications

- DVM/DPM
- Digital Thermometers
- Digital Environment Meters (Noise, Light, pH)
- Digital Scales
- Instrumentation
- Controllers
- μP Interface to Analog World

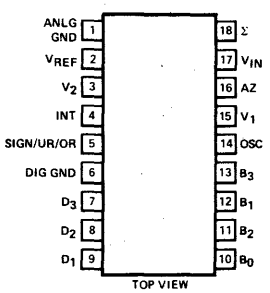
FUNCTIONAL DIAGRAM



Connection Diagram

PIN CONFIGURATION

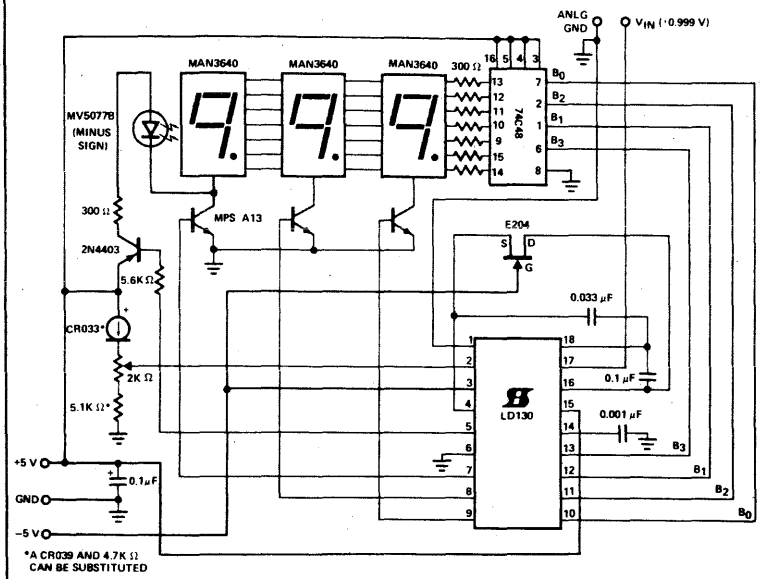
Dual-In-Line Package



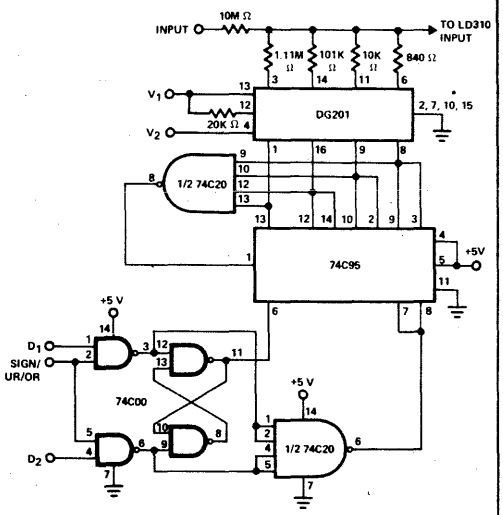
ORDER NUMBERS:
LD130DP, LD130CJ
OR
LD131CJ

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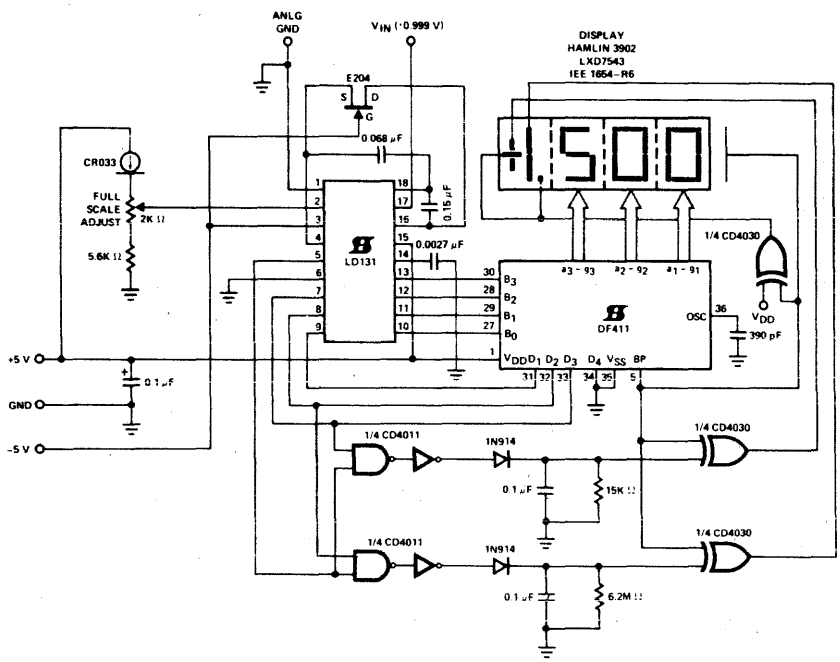
APPLICATIONS



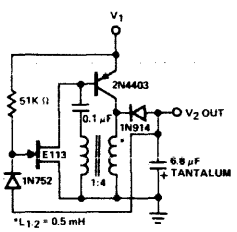
3 Digit DVM (±999 mV, 5 samples/sec)



Autoranging System For LD130



±3 1/3 Digit DVM-LCD Display



DC to DC Converter

©IC MASTER 1978

Siliconix incorporated

LD120 LD121

OPERATING TEMPERATURE RANGE:
C SUFFIX 0 to +70°C

4½ DIGIT A/D CONVERTER

LD120 ANALOG A/D PROCESSOR/LD121 DIGITAL A/D PROCESSOR

Description

The LD120/LD121 4½ digit A/D system uses Siliconix's proprietary "Quantized Feedback" (patent pending) conversion technique. Intrinsic features of this sytem are Auto-Polarity, Auto-Zero and ratiometric operation. No critical components are required except for a stable voltage reference. The technique offers superior linearity, normal mode rejection, and stability due to the simultaneous integration of the unknown input and the reference voltages. Unlike other conversion techniques, the integrator output voltage never represents more than 30 counts, thus critical, high resolution performance is not required of either the integrator or comparator.

The LD120 analog processor is fabricated with a unique combined PMOS, bipolar process. It contains all the necessary amplifiers, MOSFET switches, and switch driver circuits for the system. The reference voltage input is fully buffered on the LD120 to eliminate the reference switch resistance as a source of error. All the amplifiers are internally compensated. The LD120 directly interfaces the LD121 digital processor with no additional active components required. (Continued on page 3)

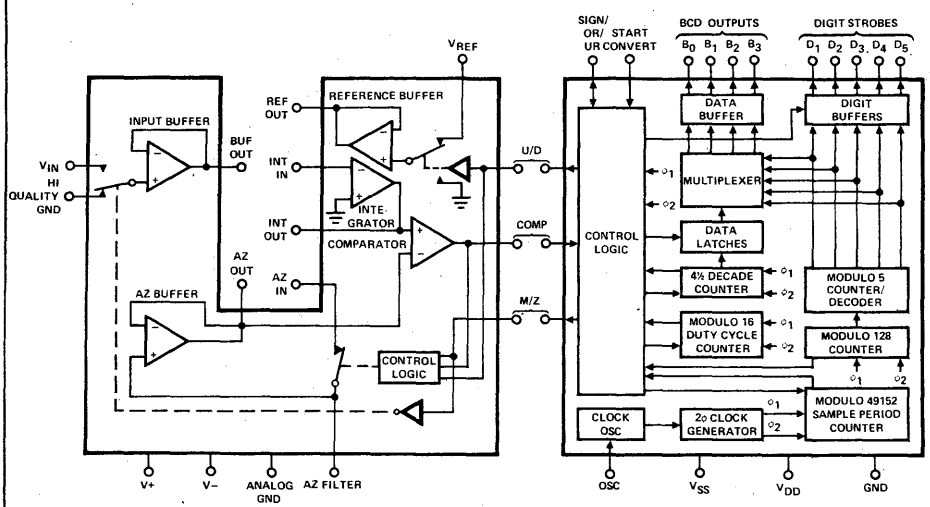
Applications

- DVM/DPM's up to 4½ Digits
- A/D Converters
- Controllers
- Digital Weighing Systems
- Digital Process Control
- Digital Thermometers
- Scientific Instrumentation

Features

- Proven Siliconix "Quantized Feedback" A/D Technique
- 0.005% Accuracy ±1 Count, 2 Volt Range
- 0.01% Accuracy ±1 Count, 200.00 mV Range
- 0.5 Count Stability on 2.0000 V Range, 1.0 Count Stability 200.00 mV Range
- Linear to 28,500 Counts
- 1 to 5 Samples/Second
- MOSFET Input for $Z_{IN} > 1000M\ \Omega$
- Auto-Zero Cycle
- Intrinsic Auto-Polarity Operation
- Monolithic Design
  - LD120 Bipolar/PMOS Linear Process
  - LD121 Depletion Load PMOS/LSI Process
- Multiplexed TTL Compatible BCD Outputs
- Space Saving 300 Mil DIP Packages
- 25% Interdigit Blanking for Ghost-Free LED or Gas Discharge Display Interface
- Autoranging Control Outputs
- Convert-on-Command Input Permits Processor Controlled Operation
- Blinking Display Overrange Indication at 20,000 Counts (Electrically Selectable)
- Underrange Output Indicates Underrange at 1800 Counts

FUNCTIONAL BLOCK DIAGRAM

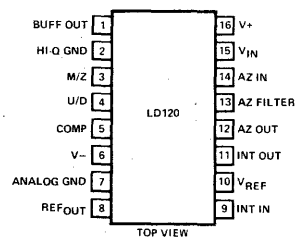


LD120 LD121

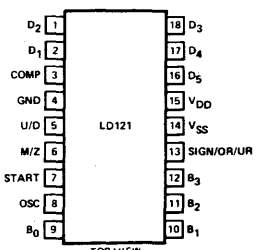
SWITCH STATES ARE FOR A LOGIC "0" AT U/D AND M/Z INPUTS.

PIN CONFIGURATIONS

Dual-In-Line Packages



ORDER NUMBER LD120CJ



ORDER NUMBER LD121CJ

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APPLICATIONS

1. The recommended supply voltages are:

   $V+ = 12\ V \pm 10\%$
   $V_{DD}, V- = -12\ V \pm 10\%$
   $V_{SS} = 5\ V \pm 10\%$
   $V_{REF} = 2\ V$ to $10\ V$

2. The reading is essentially the proportionality of V_{IN} compared to V_{REF} as shown in the gain equation:

$$V_{READOUT} = (V_{IN} - V_{HI\text{-}Q\ GND}) \bullet \frac{R_1}{R_2} \bullet \frac{65{,}536}{V_{REF}}$$

   R_1 is independent of the U/D switch resistance due to the incorporation of the U/D buffer amplifier in the LD120. Gain can be calibrated either by varying V_{REF} or trimming the resistance of R_1 to obtain the correct full scale reading.

3. The output of the integrator should always be more positive than $-9\ V$ (for $V_{DD} = -12\ V$) to obtain specified accuracy:

$$V_O\ (min) > -9\ V$$

$$V_{O\ (min)} = -\frac{V_{REF}\ R_3}{2R_1} - \frac{15}{f_{OSC}\ C_{INT}}\left[\frac{V_{REF}}{2R_1} + \frac{V_{IN\ (max)}}{R_2}\right]$$

   Large integrator swing provides the best performance. V_{INT} (P-P) = 6 to 8 volts is recommended.

$$V_{INT\ (P\text{-}P)} = \frac{30}{f_{OSC}\ C_{INT}}\left[\frac{V_{REF}}{2R_1} + \frac{V_{IN\ (max)}}{R_2}\right]$$

4. Although any oscillator frequency from 50 kHz to 250 kHz can be used, frequencies that provide integer number of line frequency cycles per measure period provide maximum line noise rejection. These frequencies are:

$$f_{OSC} = \frac{32{,}768\ F_{LINE}}{n},\ n = 8, 9, 10, \ldots 40$$

5. The sampling rate = $f_{OSC}/49{,}152$ cycles/sample.

6. After a start conversion pulse, data is valid 32,850 clock pulses later and remains valid until at least 32,768 clock pulses after the next start pulse. During continuous cycle operation, data is assured valid when M/Z is high or 100 clock cycles after the one/zero transition of M/Z.

7. Any capacitive coupling between U/D and Comp. is detrimental to proper algorithm operation. PC board layouts should not allow these traces to be adjacent.

8. All power supplies should be capacitively bypassed to ground for maximum count stability.

9. C_{INT} and C_{STRG} should be selected for low leakage. Silvered mica is recommended for C_{INT} and mylar for C_{STRG}. Polypropylene capacitors also work well for both C_{STRG} and C_{INT}.

10. For a given leakage into C_{STRG} of I_{STRG}:

$$\Delta V_{STRG} = \frac{\Delta t\ I_{AZ}}{C_{STRG}}$$

where Δt = a measure interval $= \frac{2}{3}\ \frac{1}{F_{SAMPLE}}$

ΔV_{STRG} will inject a ΔI integrator of $\Delta V_{STRG}/R_3$

Now a ΔI integrator would have been equivalent to a $\Delta V_{IN}/R_2$

So the equivalent input drift is $\Delta V_{IN} = \frac{1}{2}\ \frac{R_2}{R_3}\ \frac{2}{3}$

$$\frac{I_{STRG}}{F_{SAMPLE}\ C_{STRG}}$$

the ½ factor is provided by integrator action.

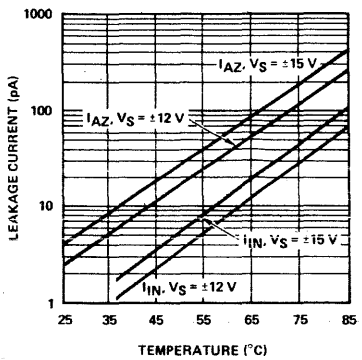
Example: We wish to see 1 count (0.1 mV of ΔV_{IN} on the 2 V range) of drift for the circuit of Figure 6 with $I_{STRG} = 100\ pA$ @ 70°C. What C_{STRG} is needed?

Answer:

$$C_{STRG} = \frac{R_2}{R_3}\ \frac{1}{3}\ \frac{I_{STRG}}{F_{SAMPLE} \cdot \Delta V_{IN}} =$$

$$\frac{100K\ \Omega}{62K\ \Omega} \times \frac{1}{3} \times \frac{10^{-10}\ F}{3\ Hz \times 10^{-4}\ V}$$

$= 0.18\ \mu F$ Minimum



Typical Leakage Over Temperature

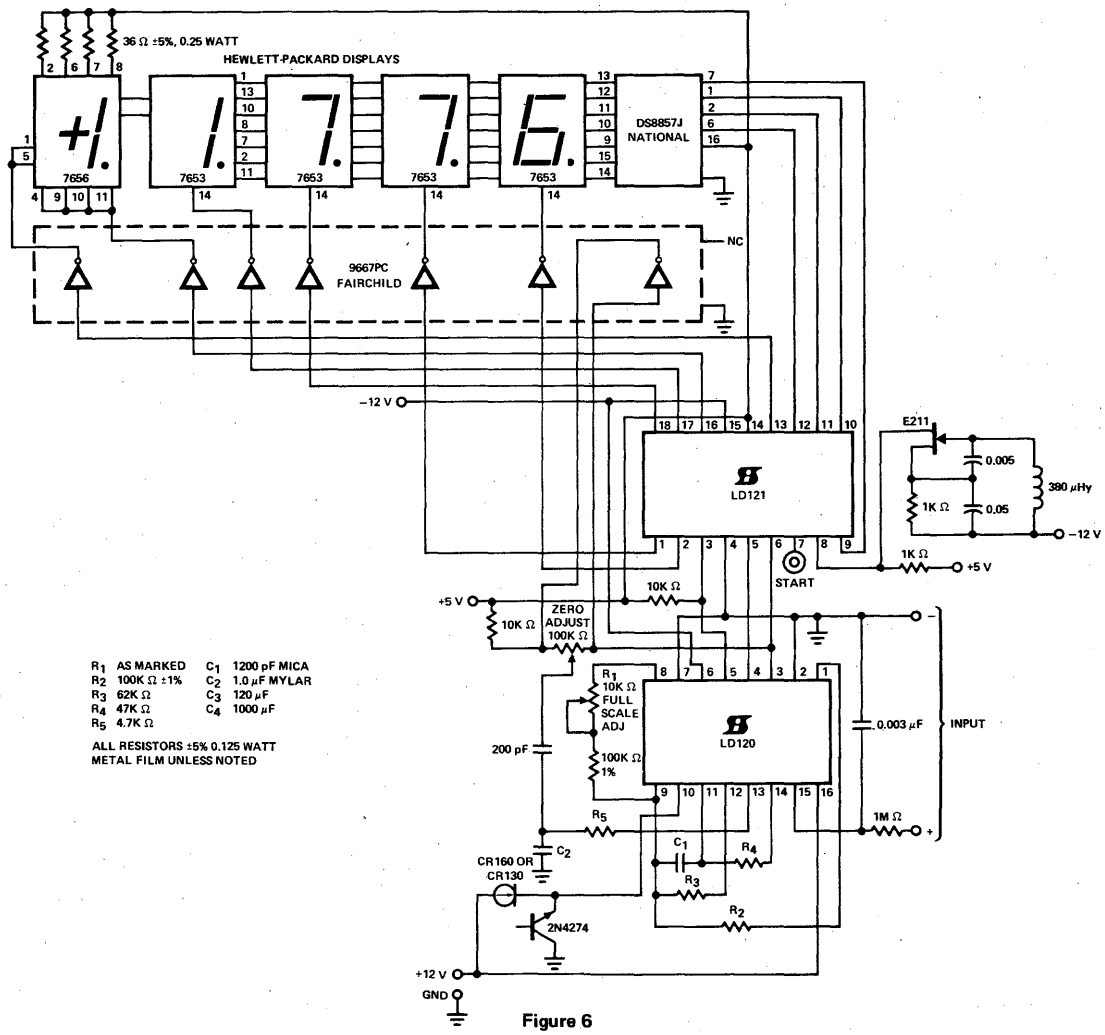


Figure 6

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Siliconix incorporated

S75V03

high speed, power peripheral drivers (2.0 A, 60 V) *designed for . . .*

- **Laser Diode Pulsing**
- **High Speed Line Drivers**
- **CMOS to High Current Interfacing**
- **TTL to High Current Interfacing**
- **Switching Reactive Loads**

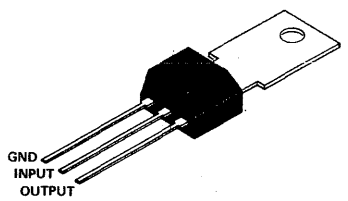
BENEFITS

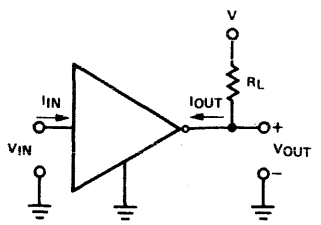
- Directly Interfaces to CMOS, TTL, DTL, and MOS Logic Families Low Input Current, Typically <1 nA
- Fan Out from CMOS Greater than 100
- Output will Sink 2 Amps
- Open Drain Output
- Output will Withstand 90 V
- No Power Supply Required
- Easily Paralleled for Greater than 2 Amp Currents
- Very Short Propagation Delay t_{on} Typically less than 4 ns

ABSOLUTE MAXIMUM RATINGS

Output Voltage	60V
Continuous Output Current	2.0 A
Peak Output Current	3.0 A
Voltage at Input	35 V
Power Dissipation at 25°C Case Temperature	12.5 W
Linear Derating Factor	100 mW/°C
Storage Temperature	−55°C to 150°C
Operating Temperature	−55°C to 150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-202





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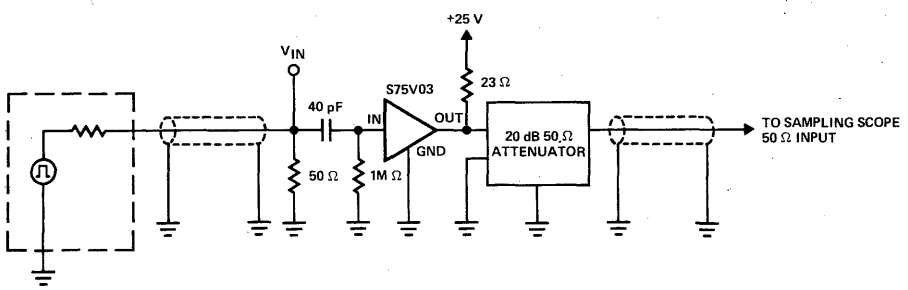
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Characteristic	Min	Typ	Max	Unit	Test Conditions
1	V_{IN} Logical "1" Input Voltage (Note 2)	4.0	2.0		V	I_O = 100 mA, V_{OUT} = 25 V
2		5.0	3.5			I_O = 300 mA, V_{OUT} = 25 V
3		10.0	6.5			I_O = 1 Amp, V_{OUT} = 25 V
4	V_{IN} Logical "0" Input Voltage (Note 2)		1.2	0.8		I_O = 1.0 mA, V_{OUT} = 25 V
5		0.8	0.8			I_O = 0.1 mA, V_{OUT} = 25 V
6				0		I_O = 10 μA, V_{OUT} = 25 V
7	I_{IH} Logical "1" Input Current		0.01	0.5	μA	V_{IN} = 10 V, V_{OUT} = 0
8	I_{IL} Logical "0" Input Current (Note 2)		−0.01			V_{IN} = 0V, V_{OUT} = 25 V
9	V_{ON} Output Breakdown Voltage	60			V	I_O = 10 μA, V_{IN} = 0
	Specifications For Use With CMOS					
10	V_{OL} Output ON Voltage (Note 1)		0.3		V	I_O = 100 mA, V_{IN} = 5 V
11			1.0	1.5		I_O = 300 mA, V_{IN} = 5 V
12			2.0	3.5		I_O = 1.0 Amp, V_{IN} = 10 V
13	Propagation Delay to tpd0 Logical "0" Output (Notes 2, 3)		5		ns	I_O = 0.3 Amp, V_{IN} = 0–15 V
14			4	10		I_O = 1.0 Amp, V_{IN} = 0–10 V
15	Propagation Delay to tpd1 Logical "1" Output (Notes 2, 3)		5			I_O = 0.3 Amp, V_{IN} = 5–0 V
16			4	10		I_O = 1.0 Amp, V_{IN} = 10–0 V
	Specifications For Use With TTL					
17	V_{OL} Output ON Voltage (Note 1)		0.3		V	I_O = 100 mA, V_{IN} = 5 V
18			1.0	1.5		I_O = 300 mA, V_{IN} = 5 V
19	tpd0 Propagation Delay to Logical "0" Output (Notes 2, 3)		8		ns	V+ = 10 V, R_L = 30 Ω, I_O = 0.3 Amp
20	tpd1 Propagation Delay to Logical "1" Output (Notes 2, 3)		5			V+ = 10 V, R_L = 30 Ω, I_O = 0.3 Amp

NOTES:
1. Pulse Test – 80 μs pulse, 1% duty cycle.
2. Sample Test 3. See switching time test circuit.

VNAR

Switching Time Test Circuit



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INTRODUCTION TO LINEAR

The Master Selection Guide provides sufficient information to make initial product selections, to lead you to a group of device numbers and manufacturers' names. It enables you to find the products which are most appropriate to fulfill your major requirements and then provides data for many of the more important products.

All devices that appear in this section, both in the initial selection guide and in the data pages, are included in the Part Number and Product Indexes. These index listings lead to the page and the line on that page where each device appears.

In the Linear section over 1000 operational amplifiers are covered. Since there are so many devices, the operational amplifier entries have been given special consideration. Separate lists are provided for those which have High Speed, High Voltage capability, Wide Bandwidth, etc. Under General Purpose, four amplifier types are listed; these are the ones that the high volume manufacturers indicate are the most widely used; however, quad amplifiers should also be considered when appropriate. If you have located an op amp in a specialized category, you can review its characteristics by finding it in the Part Number or Product Indexes and looking it up in the Operational Amplifier Characteristics and in the Data Sections.

Following the special lists, the "Operational Amplifier-Characteristics" listings, categorize amplifiers by input parameters. They are arranged in order of increasing offset voltage, bias current, offset current and then voltage drift. The other parameters listed do not affect the sequence in which the devices are presented. The column labeled "Comp" indicates the number of external components normally used for compensation; for example, "0" means no compensation is required.

Consumer circuits such as audio amplifiers, AM, FM, and TV circuits as well as some digital devices (watches, calculators, etc.) are covered by model number in the Consumer Circuit Section. Linear devices and unusual circuits which do not fit elsewhere are listed under the heading "Other Linear Devices."

Category	Page
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The manufacturers listed above are providing detailed information on their latest and most significant products. They have made this investment to help you.

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LINEAR–Amplifiers, Special Purpose

Function	Device	Source	Line
Special Purpose			
AC Amplifier, Dual with automatic gain control, for tape recorders	M5130	Mitsubishi	
AC Amplifier, Quad, Single Supply	CA3048	†RCA	
	CA3052	RCA	
AGC/Squelch Amplifier (Gain Controlled Amplifier)	LM170	†National	
	LM270	National	
	LM370	National	10
AGC Generator, for SSB receivers	SL621C	Plessey	
	SL1621C	Plessey	
AGC Generator (voice operated gain adjusting device)	SL620C	Plessey	
	SL622C	Plessey	
	SL1620C	Plessey	
	SL1622C	Plessey	
Amplifier, CATV. See Linear Consumer Circuits, TV			
Amplifier, Audio with three NPN transistors	LM389	National	20
Amplifier, triple for active filters (See also Linear Other Devices, Active Filters)	TAA960	Signetics	
Current Amplifier (unity gain, 100 ma output)	SH0002C	Fairchild	
	LH0002	†National	
	LH0002C	National	
	9910	†OEI	
Current Amplifier (unity gain, 200 ma output)	3553	† Burr-Brown	30
	9963	†OEI	
Current Amplifier (unity gain, 300 ma output)	MC1438	Motorola	
	MC1538	†Motorola	
Current Amplifier (unity gain, 500 ma output)	823	Beckman	
	9911	†OEI	
Current Amplifier (unity gain, 600 ma output)	**HA-2630**	**†Harris** (696)	40
	HA-2635	**Harris** (696)	
Current Amplifiers, See also Linear Followers			
Differential Input/Differential Output Amplifier (bandwidth less than 2 MHz)	μA730C	Fairchild	
	μA730M	†Fairchild	
	MC1590	†Motorola	
	CA3000	†RCA	
	CA3007	†RCA	
	NE515	Signetics	50
	SE515	†Signetics	
Differential Input/Single Output DC Amplifier with switched inputs for a gain of ±1	MN2120	Micro Net	
	MN2120H	Micro Net	
Differential/Cascode Amplifier (dc to r.f.)	MC3330	Motorola	
	LM3028	†National	
	LM3053	†National	
	CA3028	†RCA	
	CA3028A	†RCA	60
	CA3028B	†RCA	
	TA7045	Toshiba	

Function	Device	Source	Line
Special Purpose (Cont'd)			
Followers. See Linear Followers			
Front End Amplifier, for ultrasonic or infrared remote control systems	TDA4180	Telefunken	
Gated Linear Amplifier (operational amplifier)	ZN424	Ferranti	
Hearing Aid Amplifiers. See Linear Consumer Circuits			
Instrumentation, (Differential Input, Independent Gain Adjustment)	AD520J	AD	70
	AD520K	AD	
	AD520S	†AD	
	AD521J	AD	
	AD521K	AD	
	AD521S	†AD	
	AD522A	AD	
	AD522B	AD	
	AD522C	AD	80
	AD522S	†AD	
	3660J	Burr-Brown	
	3660K	Burr-Brown	
	3660S	† Burr-Brown	
	3626A	Burr-Brown	
	3626B	Burr-Brown	
	3626C	Burr-Brown	
	3662	Burr-Brown	
	HC3020	HyComp	
	MN2000	Micro Net	90
	MN2200	Micro Net	
	LH0036	†National	
	LH0036C	National	
	LH0037	†National	
	LH0037C	National	
Instrumentation, (Differential FET Input, Independent Gain Adjustment)	3670J	Burr-Brown	
	3670K	Burr-Brown	
	3670S	† Burr-Brown	100
	AM-435-1C	Datel	
	AM-435-1M	†Datel	
	LF152	†National	
	LF252	National	
	LF352	National	
Instrumentation, (unity gain)	3627	Burr-Brown	
Instrumentation, with low pass filter	MN2200	Micro Net	
Isolation Amplifier, Optically Coupled	3650	Burr-Brown	110
	3652	Burr-Brown	
Linear Antilog Amplifier, Dual (Differential input, separate control input)	SSM2000	SSM	
	SSM2020	SSM	
Log/Antilog Amplifier, (Antilog)	8049C	Intersil	
	2910	†OEI	
Log/Antilog Amplifier, (Log)	4127	Burr-Brown	120
	8048C	Intersil	
	2910	†OEI	
	TL441C	TI	
	TL441M	†TI	
Microphone/Headphone Amplifier	SL630C	Plessey	
(Continued)			

Function	Device	Source	Line
Special Purpose (Cont'd)			
Microphone/Headphone Amplifier (Cont'd.)	SL1630	Plessey	
	TA1066	Toshiba	130
Microphone Amplifier (for microphones in telephones)	TBA830	Siemens	
	TAA970	Signetics	
	TCA980	Signetics	
Mixer (to 200 MHz)	S042	Siemens	
MOS Amplifier, MOS and NPN transistors, 3 terminal	TAA320	Signetics	
	TAA320A	Signetics	
Operational Amplifier, Dual with Dual Voltage Comparator	MC3405	Motorola	140
	MC3505	†Motorola	
Operational Transconductance Amplifier	CA3060	RCA	
	CA3060	†RCA	
	CA3060A	†RCA	
	CA3060B	†RCA	
	CA3080	RCA	
	CA3080A	†RCA	150
Power Amplifier, Motor and Actuator Driver, to 24V, 3a	IH8510C	Intersil	
	IH8510M	†Intersil	
	IH8520C	Intersil	
	IH8520M	†Intersil	
	IH8553C	Intersil	
	IH8553M	†Intersil	
Power Amplifier/Switch (equivalent to an operational amplifier with uncommitted Darlington power output transistor), Programmable Gain	CA3094	†RCA	160
	CA3094A	†RCA	
	CA3094B	†RCA	
Preamplifier, JFET (Impedance Converter)	T100	Siliconix	
	T300	Siliconix	
Preamplifier JFET (to precede operational amplifiers and comparators)	HA-2000	†Harris	
	HA-2005	Harris	170
Preamplifier, Low Noise. (60db gain, 15MHz bandwidth)	ZN459C	Ferranti	
	ZN459T	Ferranti	
Preamplifier, Precision (to precede operational amplifiers)	LM121	†National	
	LM221	National	
	LM321	National	
	LM121A	†National	180
	LM221A	National	
	LM321A	National	
Preamplifier, Temperature Controlled	μA727C	Fairchild	
	μA727M	†Fairchild	
Preamplifier, with ALC transistor, for tape recorders	LA3201	Sanyo	
Preamplifier with automatic level control, for tape recorders	TDA1054	SGS	
	TDA1002	Signetics	190
(Continued)			

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Amplifiers, Special Purpose (Cont'd)

Function	Device	Source	Line
Special Purpose (Cont'd)			
Preamplifier with automatic level control, for tape recorders (Cont'd.)	TA7055	Toshiba	
Programmable Channel Op Amp (one of 4 input stages can be connected to single output)	**HA-2400**	**† Harris**	**(668)**
	HA-2404	**Harris**	**(668)**
	HA-2405	**Harris**	**(668)**
Read Amplifier/Preamplifier (for magnetic tape memory systems)	MC3467	Motorola	10
	MC3468	Motorola	
R.F. Amplifier, Gated	MC1445	Motorola	
	MC1545	† Motorola	
Signal Sources Switch, (Buffer Amplifiers with input switches)	TDA1028	Signetics	
	TDA1029	Signetics	
Single ended Input/Output Amplifier, Triple	CA3035	RCA	20
Two Wire Transmitter (Sends current signal over same two lines from which it is powered)	LH0045	† National	
	LH0045C	National	
Video, IF and RF Amplifiers	592C	AMD	
	592M	† AMD	
	733	† AMD	
	733C	AMD	30
	HFS-23	DDC	
	HVA-23	DDC	
	μA703C	Fairchild	
	μA703M	† Fairchild	
	μA733C	Fairchild	
	μA733M	† Fairchild	
	μA753	Fairchild	
	TBA970	Fairchild	
	733C	Intersil	
	733M	† Intersil	40
	753	Intersil	
	MC1350	Motorola	
	MC1410	Motorola	
	MC1510	† Motorola	
	MC1550	† Motorola	
	MC1552	† Motorola	
	MC1553	† Motorola	
	MC1590	† Motorola	
	MC1733	† Motorola	
	MC1733C	Motorola	50
	NE592	Motorola	
	SE592	† Motorola	
	LM171	† National	
	LM271	National	
	LM371	National	
	LM703	† National	
	LM703C	National	
	LM733	† National	
	LM733L	National	
	LM3011	National	60
	AN606	Panasonic	
	AN607	Panasonic	
	AN608	Panasonic	
	SL541	Plessey	
	SL550	Plessey	
	SL560	Plessey	
	SL610C	Plessey	

(Continued)

Function	Device	Source	Line
Special Purpose (Cont'd)			
Video, IF and RF Amplifiers (Cont'd.)	SL611C	Plessey	
	SL612C	Plessey	70
	SL1205	Plessey	
	SL1550	Plessey	
	SL1610C	Plessey	
	SL1611C	Plessey	
	SL1612C	Plessey	
	SL1030	† Plessey	
	RC733	Raytheon	
	RM733	† Raytheon	
	CA3001	† RCA	
	CA3002	† RCA	80
	CA3004	† RCA	
	CA3005	† RCA	
	CA3006	† RCA	
	CA3011	† RCA	
	CA3012	† RCA	
	CA3020	† RCA	
	CA3020A	RCA	
	CA3021	† RCA	
	CA3022	† RCA	
	CA3023	† RCA	90
	TAA721	Siemens	
	TAA722	Siemens	
	TBA400	Siemens	
	NE592	Signetics	
	SE592	† Signetics	
	TAA263	Signetics	
	TBA1440	Signetics	
	TDA2541	Signetics	
	μA733	† Signetics	
	μA733C	Signetics	100
	SG1401	† Silicon G	
	SG2401	Silicon G	
	SG3001	† Silicon G	
	SG3401	Silicon G	
	TDA440	Telefunken	
	μA733C	TI	
	μA733M	† TI	
	TA7027	Toshiba	
	TA7060	Toshiba	
	TA7061	Toshiba	110
	TA7081	Toshiba	
	TA7084	Toshiba	
	CA2800	TRW	
	CA2810	TRW	
	CA2820	TRW	
	CA2830	TRW	
	CA2840	TRW	
	CA2870	TRW	
	CA2875	TRW	
Gain Controlled IF Amplifier	μA757	Fairchild	120
	SL550	Plessey	
Limiting Amplifier/Detector (IF or RF)	SL613C	Plessey	
	SL1613C	Plessey	
Voltage Controlled Amplifier	SSM2000	SSM	
	SSM2020	SSM	
Wideband Amplifier with low level video detection (7 to 200 MHz for log IF amplifiers)	SL521	Plessey	130
	SL571	Plessey	
	SL525	† Plessey	
	SL613C	Plessey	
	SL1521	† Plessey	

(Continued)

Function	Device	Source	Line
Special Purpose (Cont'd)			
Wideband Amplifier with low level video detection (7 to 200 MHz for log IF amplifiers) (Cont'd.)	SL1522	Plessey	
	SL1523	Plessey	
Wideband Amplifier, Logarithmic limiting (4 to 85 MHz)	SL530C	Plessey	140
Wideband Amplifier, Triple	CA3035	† RCA	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Arrays

Function	Device	Source	Line
Transistor Arrays			
Dual Transistors, Monolithic NPN Tightly Matched			
	AD810	†AD	
	AD811	†AD	
	AD812	†AD	
	AD813	†AD	
	AD814	†AD	
	AD815	†AD	
	AD816	†AD	
	MPS301	Micro Power	
	MPS302	Micro Power	10
	MPS303	Micro Power	
	MPS310	Micro Power	
	MPS311	Micro Power	
	MPS312	Micro Power	
	LM114	†National	
	LM114A	†National	
	LM115	†National	
	LM115A	†National	
	LM3018	†National	
	LM194	†National	20
	LM394	National	
	LM3018A	†National	
	SL301	Plessey	
	SL360	Plessey	
	SL362	Plessey	
	MAT-01	**†PMI** (887)	
	MAT-01A	**†PMI** (887)	
	MAT-01F	**†PMI** (887)	
	MAT-01G	**†PMI** (887)	
Dual Transistors, Monolithic PNP, Tightly Matched			30
	AD820	†AD	
	AD821	†AD	
	AD822	†AD	
	MPS350	Micro Power	
	MPS351	Micro Power	
	MPS352	Micro Power	
Dual Transistors, Monolithic NPN, Logarithmic Conformance			
	AD818	†AD	
	MPS318	Micro Power	40
	MAT-01	**†PMI** (887)	
	MAT-01A	**†PMI** (887)	
	MAT-01F	**†PMI** (887)	
	MAT-01G	**†PMI** (887)	
Dual Transistors, Monolithic PNP, Logarithmic Conformance			
	MPS358	Micro Power	
Dual Transistors, NPN, Matched plus a third transistor			
	SL303	Plessey	
Dual Matched Transistor Pairs, NPN			50
	SL354	Plessey	
Darlington Pair and two Matched NPN Transistors			
	μA3018M	†Fairchild	
	μA3018AM	†Fairchild	
	LM3018	†National	
	LM3018A	†National	
	LM3118	†National	
	LM3118A	†National	
	SFC2018	†NPC	
	SL3018	†Plessey	60
	SL3018A	†Plessey	
	SL3118	†Plessey	
	SL3118A	†Plessey	
	CA3018	†RCA	
	CA3018A	†RCA	
	CA3118	†RCA	
	CA3118A	†RCA	
	SG3818	Silicon G	
	(Continued)		

Function	Device	Source	Line
Transistor Arrays (Cont'd)			
Darlington Pair and two Matched NPN Transistors (Cont'd.)			
	SG3818A	Silicon G	70
	TA7047	Toshiba	
Dual Darlington (NPN)			
	μA3036M	†Fairchild	
	SFC2036	†NPC	
	SL305	Plessey	
	CA3036	†RCA	
Dual Darlington (NPN PNP Quasi Complementary)			
	TDA1410	SGS	
	TDA1420	SGS	
Dual Darlington Switch			80
	ULN-2061M	Sprague	
Quad Darlington Switch			
	ULN-2064B	Sprague	
	ULN-2074B	Sprague	
	ULN-2841	Sprague	
	ULN-2842	Sprague	
	ULN-2843	Sprague	
	ULN-2844	Sprague	
	ULN-2845	Sprague	
	ULN-2846	Sprague	90
Four High Current NPN Transistors (Core Driver)			
	FQ3724	Fairchild	
	FQ3725	Fairchild	
	MHQ4001A	Motorola	
	MHQ4002A	Motorola	
	MHQ4013	Motorola	
	MHQ4014	Motorola	
	MPQ3303	Motorola	
	MPQ3725	Motorola	
	MPQ3725A	Motorola	100
	MPQ4003	Motorola	
	MPQ4004	Motorola	
	DH3725C	National	
	DH6376C	National	
	AN807	Panasonic	
	CA3138	†RCA	
	CA3138A	†RCA	
	CA3724	†RCA	
	CA3725	†RCA	
	TPQ3724	Sprague	110
	TPQ3725	Sprague	
	TPQ3725A	Sprague	
Four High Current PNP Transistors (Core Driver)			
	FQ3467	Fairchild	
	FQ3468	Fairchild	
	MHQ3467	Motorola	
	DH3467C	National	
Differential Pair and Three NPN Transistors			
	μA3045M	†Fairchild	
	μA3046C	Fairchild	120
	μA3086C	Fairchild	
	MC3346	†Motorola	
	MC3386	†Motorola	
	LM3045	†National	
	LM3046	National	
	LM3086	National	
	LM3145	†National	
	LM3145A	†National	
	LM3146	National	
	LM3146A	National	130
	SFC2046	†NPC	
	AN903	Panasonic	
	AN905	Panasonic	
	SL3045	†Plessey	
	(Continued)		

Function	Device	Source	Line
Transistor Arrays (Cont'd)			
Differential Pair and Three NPN Transistors (Cont'd.)			
	SL3046	Plessey	
	SL3086	Plessey	
	SL3145	†Plessey	
	SL3146	Plessey	
	CA3045	†RCA	140
	CA3046	†RCA	
	CA3086	†RCA	
	CA3146	RCA	
	CA3146A	RCA	
	L159	SGS	
	TBA331	SGS	
	TCA671	Siemens	
	TCA871	Siemens	
	SG3045	Silicon G	
	SG3046	Silicon G	150
	SG3146	Silicon G	
	SG3821	Silicon G	
	SG3886	Silicon G	
	ULS-2045A	†Sprague	
	ULN-2046A	Sprague	
	ULN-2086A	Sprague	
Three NPN and two PNP Transistors			
	CA3096	†RCA	
	CA3096A	†RCA	
Five High Current NPN Transistors			160
	SL3083	†Plessey	
	SL3183	†Plessey	
	CA3083	†RCA	
	CA3183	†RCA	
	CA3183A	†RCA	
	CA3083	†Signetics	
	CA3183	†Signetics	
	CA3183A	†Signetics	
	TDA3083	Signetics	
	SG3083	†Silicon G	170
	SG3183	†Silicon G	
	SG3183A	†Silicon G	
	ULN-2083	Sprague	
	ULS-2083	†Sprague	
Five High Frequency NPN Transistors, (f>GHz)			
	SL3127	Plessey	
	CA3127	RCA	
Dual Darlington (NPN) and two NPN Transistors			
	SG3823	Silicon G	
Dual Differential Amplifiers (NPN) with diode			180
	M5109	Mitsubishi	
Dual Differential Amplifiers (NPN), to 120 MHz			
	μA3026	†Fairchild	
	μA3054	Fairchild	
	LM3026	†National	
	LM3054	National	
	AN904	Panasonic	
	CA3026	†RCA	
	CA3054	RCA	
	SG3822	Silicon G	190
	ULN-2054A	Sprague	
Dual Differential Amplifiers (NPN), biasing, to above 100 MHz			
	NE510	Signetics	
	NE511	Signetics	
	SE510	†Signetics	
	SE511	†Signetics	
Dual Differential Amplifiers (NPN), to 500 MHz			
	CA3049	†RCA	
	CA3102	†RCA	200

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Arrays (Cont'd)

Transistor Arrays (Cont'd)

Function	Device	Source	Line
Dual Differential Darlington Amplifiers (NPN) with Diode Bias String			
	CA3050	†RCA	
	CA3051	RCA	
Three Differential Amplifiers (NPN)			
	ULN-2047A	Sprague	
One Darlington PNP Pair, and one Current Mirror Pair with shared Diode, and two PNP Transistors			
	MC1416	Motorola	
	CA3084	RCA	
Five High Voltage, High Current NPN Darlington Amplifiers			10
	LB1287	Sanyo	
	LB1288	Sanyo	
Five High Voltage, High Current NPN Darlington Amplifiers, Source, for load connected to negative supply			
	UDN-2956A	Sprague	
	UDN-2957A	Sprague	
Seven NPN Transistors, Common Emitter			
	SL3081	Plessey	
	CA3081	†RCA	20
	CA3081	Signetics	
	TDA3081	Signetics	
	SG3081	Silicon G	
	ULN-2081A	Sprague	
Seven High Current NPN Transistors, Common Collector			
	SL3082	Plessey	
	CA3082	†RCA	
	CA3082	Signetics	
	TDA3082	Signetics	30
	SG3082	Silicon G	
	ULN-2082A	Sprague	
Seven NPN Darlingtons			
	LB1270	Sanyo	
Seven High Current Darlingtons			
	ULN-2031A	Sprague	
	ULN-2032A	Sprague	
	ULN-2033A	Sprague	
Seven High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 50v, 500ma			40
	XR2201	Exar	
	XR2201M	†Exar	
	XR2202	Exar	
	XR2202M	†Exar	
	XR2203	Exar	
	XR2203M	†Exar	
	XR2204	Exar	
	XR2204M	†Exar	
	9665	Fairchild	
	9666	Fairchild	50
	9667	Fairchild	
	9668	Fairchild	
	MC1411	Motorola	
	MC1412	Motorola	
	MC1413	Motorola	
	MC1416	Motorola	
	ULN2001	Signetics	
	ULN2002	Signetics	
	ULN2003	Signetics	
	ULN2004	Signetics	60
	PBD352301	RIFA	
	PBD352302	RIFA	
	PBD352303	RIFA	
	L201	SGS	
	L202	SGS	

(Continued)

Transistor Arrays (Cont'd)

Function	Device	Source	Line
Seven High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 50v, 500ma (Cont'd.)			
	L203	SGS	
	SG2001	Silicon G	
	SG2002	Silicon G	70
	SG2003	Silicon G	
	SG3851	Silicon G	
	SG3852	Silicon G	
	SG3853	Silicon G	
	ULN-2001A	Sprague	
	ULN-2002A	Sprague	
	ULN-2003A	Sprague	
	ULN-2004A	Sprague	
	ULN-2005A	Sprague	
	ULS-2001H	†Sprague	80
	ULS-2002H	†Sprague	
	ULS-2003H	†Sprague	
	ULS-2004H	†Sprague	
	SN75466	TI	
	SN75467	TI	
	SN75468	TI	
	SN75469	TI	
	ULN2001A	TI	
	ULN2002A	TI	
	ULN2003A	TI	90
	ULN2004A	TI	
Seven High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 50v, 600ma			
	ULN-2011A	Sprague	
	ULN-2012A	Sprague	
	ULN-2013A	Sprague	
	ULN-2014A	Sprague	
	ULN-2015A	Sprague	
Seven High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 95v, 500ma			100
	NE5501	Signetics	
	NE5502	Signetics	
	NE5503	Signetics	
	NE5504	Signetics	
	ULN-2021A	Sprague	
	ULN-2022A	Sprague	
	ULN-2023A	Sprague	
	ULN-2024A	Sprague	
	ULN-2025A	Sprague	
Eight High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 50v, 500ma			110
	ULN-2801A	Sprague	
	ULN-2802A	Sprague	
	ULN-2803A	Sprague	
	ULN-2804A	Sprague	
	ULN-2805A	Sprague	
Eight High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 50v, 600ma			
	ULN-2811A	Sprague	
	ULN-2812A	Sprague	120
	ULN-2813A	Sprague	
	ULN-2814A	Sprague	
	ULN-2815A	Sprague	
Eight High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 95v, 500ma			
	ULN-2821A	Sprague	
	ULN-2822A	Sprague	
	ULN-2823A	Sprague	
	ULN-2824A	Sprague	
	ULN-2825A	Sprague	130
Eight High Current, High Voltage NPN Darlington Amplifiers, Current Source			
	UDN-2981A	Sprague	

(Continued)

Transistor Arrays (Cont'd)

Function	Device	Source	Line
Eight High Current, High Voltage NPN Darlington Amplifiers, Current Source (Cont'd.)			
	UDN-2982A	Sprague	
	UDN-2983A	Sprague	
	UDN-2984A	Sprague	
Super Beta Differential Cascode Amplifier and three NPN Transistors			140
	CA3095	†RCA	

Special Arrays

Function	Device	Source	Line
Audio Amplifier and three NPN transistors			
	LM389	National	
CMOS (Three p channel and three n channel enhancement MOS Transistors tested for linear operation)			
	CA3600	†RCA	
Thyristor/Transistor Array (SCR, Programmable Unijunction Transistor, PNP/NPN Transistor Pair, NPN Transistor and Zener Diode)			150
	CA3097	†RCA	
Transistor/Diode Array (Three NPN Transistors two Zener Diodes and one Diode)			
	CA3093	RCA	
Eight SCRs			
	TCP2410	TI	
	TCP2411	TI	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Comparators

Offset Voltage mv (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage	Device	Source
Comparators-Single									
0.8	50nA	3nA	270	11	200K		5 to ±18	**CMP-02**	**†PMI (906)**
								CMP-02E	**PMI (906)**
	600nA	25nA	180	11	200K		5 to ±18	**CMP-01**	**†PMI (902)**
								CMP-01E	**PMI (902)**
1.0	15µA	1µA	60	5	1400		-6,12	RM710A	Raytheon
2.0	10µA	1µA	6.5	6			-5.2,6	685L	AMD
								685M	†AMD
			12	6		5	-6,5	686M	†AMD
	15µA	3µA	80	5	12.5K		-6,12	TL810M	†TI
	20µA	3µA	40	5	40K*	10	-3 to -12,12	LM106	†AMD
								LM206	AMD
								LM106	†National
								LM206	National
								LM106	†Raytheon
								LM206	Raytheon
								LM106	†TI
								LM206	TI
			40*	5	1250	1	-6,12	µA710M	†Fairchild
								MC1710	†Motorola
								LM710	†National
								µA710	†Signetics
								SG710	†Silicon G
								SFC2710	†NPC
								µA710M	†TI
			60	5	1250	1	-6,12	RM710	†Raytheon
2.8	100nA	15nA	270	11	100K		5 to ±18	**CMP-02C**	**PMI (906)**
	900nA	80nA	180	11	200K		5 to ±18	**CMP-01C**	**PMI (902)**
3.0	50nA	10nA	200	10	35K		±5 to ±18	µA734M	†Fairchild
	100nA	10nA	165*	30	200K*	5	5, 0 to ±15	LM111	†TI
			200*	30	200K*	5	5, 0 to ±15	AD111	†AD
								AD211	AD
								µA111M	†Fairchild
								111	†Intersil
								211	Intersil
								LM111	†Motorola
								LM211	Motorola
								LM111	†National
								LM211	National
								SFC2111	†NPC
								SFC2211	NPC
								CA111	†RCA
								CA211	RCA
								LM111	†Raytheon
								LM211	Raytheon
								LM111	†Signetics
								LM211	Signetics
								SG111	†Silicon G
								SG211	Silicon G
			250	30	200K*	5	5, 0 to ±15	LM111	†AMD
								LM211	AMD
		20nA	250*	15	15K		5-15, ±5-±15	8001M	†Intersil
	5µA	2µA*	20	5	3K*	2	5,(-6, 5-±15)	LM161	†National
								LM261	National
	10µA	1µA	12	6			-6, 5	686C	AMD
3.5	20µA	5µA	80	5	10K		-6,12	TL510C	TI
								TL810C	TI
4.0	50pA	25pA	200*	30	200K*	5	5, 0 to ±15	LF111	†AMD
								LF211	AMD
								µAF111	†Fairchild
								LF111	†National
								LF211	National

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Comparators (Cont'd)

Offset Voltage mv (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage	Device	Source
Comparators-Single (Cont'd)									
4.0	(Cont'd.)								
	2μA	0.5μA	26	5	5K*		5,(-6, 5-±10)	SE527	† Signetics
	12μA	3μA	22	5	5K*		5,(-6, 5-±10)	SE529	† Signetics
5.0	10μA	2μA	20	5	3K*	2	(-6, 5 to ±15)	LM361	National
	20μA	3μA	14*	5	3K*	4	±5	LM160	† National
								LM260	National
								LM360	National
	25μA	5μA	40	5	40K*	10	-3 to -12,12	LM306	National
								LM306	Raytheon
								LM306	TI
			40*	5	40K*	10	-3 to -12,12	LM306	AMD
					1000	1	-6,12	MC1710C	Motorola
								LM710C	National
								μPC71	NEC America
								RC710	Raytheon
								SG710C	Silicon G
								μA710C	Signetics
	35μA	5μA	48	5		10	±5	NE526	Signetics
								SE526	† Signetics
	75μA	10μA	40*	5	750		-6,12	TL710M	† TI
	100nA	25nA	200*	10	35K		±5 to ±10	μA734C	Fairchild
			1300*	36	200K*		2 to 36	TL331M	† TI
	150nA	50nA	1300*	36	200K*		2 to 36	TL331C	TI
	250nA	50nA	250*	15	15K		5-15, ±5-±15	8001C	Intersil
6.0	2μA	0.75μA	26	5	5K*		5,(-6, 5-±10)	NE527	Signetics
	20μA	5μA	22	5	5K*		5,(-6, 5-±10)	NE529	Signetics
	60μA	7.5μA	16*	5	5K*	2	±4.5 to ±6.5	μA760M	† Fairchild
								μA760C	Fairchild
	250nA	100nA	250	10	15K		±6 to ±18	AD351J	AD
								AD351K	AD
								AD351S	† AD
7.5	250nA	50nA	165*	30	200K*	5	5, 0 to ±15	LM311	TI
			200*	30	200K*	5	5, 0 to ±15	AD311	AD
								μA311C	Fairchild
								311	Intersil
								LM311	Motorola
								LM311	National
								μPC271	NEC America
								μPC311	NEC America
								SFC2311	NPC
								CA311	RCA
								LM311	Raytheon
								LM311	Signetics
								SG311	Silicon G
								μAF311	Fairchild
			250	30	200K*	5	5, 0 to ±15	LM311	AMD
	100μA	15μA	40*	5	700		-6,12	TL710C	TI
10.0	150pA	75pA	200*	30	200K*	5	5, 0 to ±15	LF311	AMD
								μAF311	Fairchild
								LF311	National
—	100nA	—	50*	Vcc	—	—	1.7 to 6	M51201	Mitsubishi
Comparators-Dual									
1.5	15μA	1μA	40	5	1400	1	-6,12	RM711A	† Raytheon
2.0	100nA	25nA	1300*	36	50K		2 to 36	LM193A	† National
								LM193A	† Signetics
	250nA	50nA	1300*	36	50K		2 to 36	LM293A	National

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Comparators (Cont'd)

Offset Voltage mv (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage	Device	Source
Comparators-Dual (Cont'd)									
2.0	250nA	50nA	1300*	36	50K		2 to 36	(Cont'd.)	
								LM393A	National
								LM293A	Signetics
								LM393A	Signetics
	10μA	1μA	8	6			-5.2, 5	687AM	†AMD
			10	6			-5.2, 5	687M	†AMD
	15μA	3μA	80	5	12.5K		-6,12	TL514M	†TI
								TL820M	†TI
	20μA	3μA	30*	5	1250	1	-6,12	LM1514	†National
			40	5	40K*	10	-3 to -12,12	SN52506	†TI
			40*	5	1250		-6,12	MC1514	†Motorola
								RM1514	†Raytheon
3.0	100nA	10nA	200*	30	200K*	5	5, 0 to ±15	LH2111	†AMD
								LH2211	AMD
								LH2111	†Intersil
								LH2111	†National
								LH2211	National
								LH2111	†Signetics
								LH2211	Signetics
			250	30	200K*		5, 0 to ±15	1500M	†AMD
								1500L	AMD
	10μA	1μA	8	6			-5.2, 5	687AL	AMD
			10	6			-5.2, 5	687L	AMD
3.5	20μA	3μA	80	5	12.5K		-6,12	TL811M	†TI
		5μA	80	5	10K		-6,12	TL514C	TI
								TL820C	TI
	75μA	10μA	40*	5	700	1	-6,12	MC1711	†Motorola
					750	1	-6,12	μA711M	†Fairchild
								LM711	†National
								RM711	†Raytheon
								μA711	†Signetics
			60	5	750	1	-6,12	SG711	Silicon G
			80	5	750	1	-6,12	μA711M	†TI
4.0	500nA	75nA	80*	5	10K	2	5, 0 to ±15	LM119	†AMD
								LM219	AMD
								LM119	†National
								LM219	National
								LM119	†Signetics
								LM219	Signetics
5.0	100nA	25nA	1300*	36	50K		2 to 36	LM193	†National
								LM193	†Signetics
								LM193	†TI
	250nA	50nA	1300*	36	50K		2 to 36	LM293	National
								LM393	National
								LM293	Signetics
								LM393	Signetics
								LM293	TI
								LM393	TI
	600nA	150nA	5000	30			4.5 to 20	μPC379	NEC America
	25μA	5μA	28*	5	40K*	10	-3 to -12,12	TL506C	TI
			30*	5	1000	1	-6,12	LM1414	National
			40*	5	1000		-6,12	MC1414	Motorola
								RC1414	Raytheon
	30μA	5μA	33*	5	10K		-6,12	TL811C	TI
	100μA	15μA	40*	5	700	1	-6,12	μA711C	Fairchild
								MC1711C	Motorola
								SFC2711	NPC

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Comparators (Cont'd)

Offset Voltage mv (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage	Device	Source
Comparators-Dual (Cont'd)									
5.0	100μA	15μA	40*	5	700	1	-6,12	(Cont'd.)	
								LM711C	National
								RC711	Raytheon
								μA711C	Signetics
								SG711C	Silicon G
								μA711C	TI
			65*	5	700	1	-6,12	HA17711	Hitachi
7.0	250nA	50nA	1500*	36	25K		2 to 36	LM2903	National
								LM2903	Signetics
								LM2903	TI
7.5	250nA	50nA	200*	30	200K*	5	5, 0 to ±15	LH2311	AMD
								LH2311	Intersil
								MC3411	Motorola
								LH2311	National
								LH2311	Signetics
			250	30	200K		5, 0 to ±15	1500C	AMD
	20μA	5μA	18	6	5K*	10	±5	NE521	Signetics
			25	6	5K*	10	±5	NE522	Signetics
	100μA	15μA	40*	5	700		-6,12	TL720C	TI
8.0	1μA	0.2μA	80*	5	8K	2	5, 0 to ±15	LM319	AMD
								μPC319	NEC America
								LM319	National
								LM319	Signetics
								TDA0319	Signetics
Comparators-Quad									
2.0*	20μA	1μA*	55	5	1.2K*	10	±5	MC3430	Motorola
								MC3431	Motorola
			65	5	1.2K*	10	±5	MC3432	Motorola
								MC3433	Motorola
2.0	100nA	25nA	1300*	36	50K	2	2-36/±1-±18	LM139A	† AMD
								LM139A	† Intersil
								LM139A	† Motorola
								LM139A	† National
								CA139A	† RCA
								SG139A	† Silicon G
					200K*	2	2-36/±1-±18	LM139A	Signetics
	250nA	50nA	1300*	36	50K	2	2-36/±1-±18	LM239A	AMD
								LM339A	AMD
								LM239A	Intersil
								LM339A	Intersil
								LM239A	Motorola
								LM339A	Motorola
								CA239A	RCA
								CA339A	RCA
								LM239A	National
								LM339A	National
								SG239A	Silicon G
								SG339A	Silicon G
					200K*	2	2-36/±1-±18	LM239A	Signetics
								LM339A	Signetics
2.5	5nA	0.5nA	10ms	36	25K		2 to 36	**L161**	**Siliconix (984)**
3.0	75nA	25nA	130*	15	400K*		5 to ±15	**HA-4900**	**Harris (739)**
5.0	100nA	25nA	1300*	36	200K*	2	2-36/±1-±18	LM139	† AMD
								μA139M	† Fairchild
								LM139	† Intersil
								LM139	† Motorola
								LM139	† Raytheon
								LM139	† National
								CA139	† RCA

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Comparators (Cont'd)

Offset Voltage mv (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage	Device	Source
Comparators-Quad (Cont'd)									
5.0	100nA	25nA	1300*	36	200K*	2	2-36/±1-±18	(Cont'd.)	
								LM139	† Signetics
								SG139	† Silicon G
								LM139	† TI
								LM239	AMD
								LM339	AMD
								μA339C	Fairchild
								LM239	Intersil
								LM339	Intersil
								LM239	Motorola
								LM339	Motorola
								LM239	National
								LM339	National
								μPC177	NEC America
								μPC339	NEC America
								LM239	Raytheon
								LM339	Raytheon
								CA239	RCA
								CA339	RCA
								LM239	Signetics
								LM339	Signetics
								SG239	Silicon G
								SG339	Silicon G
								LM239	TI
								LM339	TI
	250nA	50nA	1300*	15	200K*	1	3-15	HD54C909	† Harris
								HD74C909	Harris
								MM54C909	† National
								MM74C909	National
	500nA	75nA	1300*	36	200K*		3-36	MC3505	† Motorola
	2 Operational Amplifiers, 2 Comparators								
7.0	250nA	50nA	1300*	36	50K	2	2-36/±1-±18	LM2901	Motorola
								LM2901	National
								LM2901	Raytheon
								LM2901	Signetics
								LM2901	TI
7.5	150nA	50nA	130*	15	400K*		5 to ±15	**HA-4905**	**† Harris (739)**
9.0	300nA	70nA	1300*	36			2-36/±1-±18	μA775C	Fairchild
	2 Operational Amplifiers, 2 Comparators								
	10	500nA	1300*	36			3-36	MC3405	Motorola
20	500nA	3nA*	2000*	Vcc	2K	1	2 to 28	MC3302	Motorola
								μA3302C	Fairchild
								RV3302	Raytheon
								MC3302	Signetics
								SG3302	Silicon G
		100nA	1300*	Vcc	2K	2	5 to ±15	LM3302	National
Special purpose comparators (Alarm Circuits; Analog Digital Control Circuits; Comparators, Programmable; Level Detectors; Voltage Sensors, etc.) are listed under Linear Other Devices.									

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Consumer Circuits

Consumer Circuits

Function	Device	Source	Line
Alarm Circuits: See Linear Other Devices, Alarms			
Amplifier, AGC/Squelch			
	LM170	†National	
	LM270	National	
	LM370	National	
Amplifier, with AGC, for recorders			
	TDA1054	SGS	
	TDA1002	Signetics	
	TA7055	Toshiba	
Amplifier, Dual with AGC, for stereo recorders			10
	M5130	Mitsubishi	
Amplifier, Dual, Tone, for stereo recorders			
	M5138	Mitsubishi	
Amplifier, Hearing Aid			
	MCC263	Micro Comp	
	MPS5003	Micro Power	
	MPS5014	Micro Power	
	μPC12	NEC America	
	OM200	Panasonic	
	CA3078	†RCA	20
	OM200	Signetics	
	TAA370	Signetics	
AM IF Amplifier			
	LM172	†National	
	LM272	National	
	LM372	National	
AM Receiver System			
	μA720	Fairchild	
	μA7330	Fairchild	
	ZN414	Ferranti	30
	HA1138	Hitachi	
	HA1151	Hitachi	
	LM1820	National	
	LM1860	National	
	AN259	Panasonic	
	CA3088	†RCA	
	CA3123	†RCA	
	TDA1046	Siemens	
	NE546	Signetics	
	TCA440	Signetics	40
	TBA651	SGS	
	ULN-2137	Sprague	
	SN76635	TI	
AM RF, Mixer, IF			
	μPC30	NEC America	
	μPC1013	NEC America	
	μPC1021	NEC America	
AM/FM IF Amplifier			
	μA757	†Fairchild	
	μPC27	NEC America	50
	μPC577	NEC America	
	AN203	Panasonic	
	AN210	Panasonic	
	AN353	Panasonic	
	LA1201	Sanyo	
	TAA991	Siemens	
	TA7142	Toshiba	
AM/FM IF and AF Amplifier			
	TBA460	Siemens	
AM/FM Receiver System			60
	μA721	Fairchild	
	LM273	National	
	LM274	National	
	LM373	National	
	LM374	National	
	AN217	Panasonic	

(Continued)

Consumer Circuits (Cont'd)

Function	Device	Source	Line
AM/FM Receiver System (Cont'd.)			
	AN253	Panasonic	
	AN260	Panasonic	
	AN277	Panasonic	70
	SL437	Plessey	
	SL624C	Plessey	
	MCC401	Micro Comp	
	MCC402	Micro Comp	
	AN366	Panasonic	
	TDA1220	SGS	
	TDA1230	SGS	
	TBA570	Signetics	
	TBA700	Signetics	
	ULN-2204A	Sprague	80
	TBA570	Telefunken	
	TDA1083	Telefunken	
AM/FM/SSB Detector			
	SL624C	Plessey	
AM/SSB Detector			
	SL623C	Plessey	
AM/FM Tuner Control and Clock			
	AY3-8110	GI	
	AY3-8112	GI	
	Stereomega	GI	90
Appliance Timer			
	FCM7040	Fairchild	
	AY5-1230	GI	
	AY5-1231	GI	
	AY5-1232	GI	
	AY5-1233	GI	
	AY5-1250	GI	
	AY5-1251	GI	
	CD22017	RCA	
	UCN-4105	Sprague	100
Audio Amplifier and Preamplifier, low power			
	TCA210	Signetics	
Audio Amplifier, low power			
	TBA915	Signetics	
Audio Controls, Stereo, dc operated			
	TCA730	Signetics	
	TCA740	Signetics	
Audio Driver			
	MC1385	Motorola	
	MC3320	Motorola	110
	MC3321	Motorola	
	LM391	National	
	NE540	Signetics	
	NE541	Signetics	
Audio Noise Reduction, Compander. See Linear Telecommunications Circuits			
Audio, Noise Reduction, Dolby			
	μA7300	Fairchild	
	LM1101	National	
	LM1101A	National	120
	NE545B	Signetics	
	NE645B	Signetics	
Audio, Power Amplifier, <5 Watts			
	TBA641	Fairchild	
	TBA820	Fairchild	
	HA1306	Hitachi	
	HA1310	Hitachi	
	HA1311	Hitachi	
	HA1312	Hitachi	
	HA1313	Hitachi	130

(Continued)

Consumer Circuits (Cont'd)

Function	Device	Source	Line
Audio, Power Amplifier, <5 Watts (Cont'd.)			
	HA1314	Hitachi	
	HA1316	Hitachi	
	HA1325	Hitachi	
	HA1329	Hitachi	
	M5106	Mitsubishi	
	M5115	Mitsubishi	
	M5115R	Mitsubishi	
	M5118	Mitsubishi	
	M5155	Mitsubishi	140
	M5156	Mitsubishi	
	M51182	Mitsubishi	
	M51512	Mitsubishi	
	M51513	Mitsubishi	
	MC1306	Motorola	
	MC1384	Motorola	
	MC1454	Motorola	
	MC1554	†Motorola	
	MC3360	Motorola	
	LM380	National	150
	LM386	National	
	LM388	National	
	LM389	National	
	LM390	National	
	μPC41	NEC America	
	μPC1025	NEC America	
	AN214	Panasonic	
	AN215	Panasonic	
	AN252	Panasonic	
	AN374	Panasonic	160
	SL414	Plessey	
	SL424	Plessey	
	CA3020	†RCA	
	CA3094	†RCA	
	LA4030	Sanyo	
	LA4031	Sanyo	
	LA4032	Sanyo	
	LA4050	Sanyo	
	LA4051	Sanyo	
	LA4100	Sanyo	170
	LA4101	Sanyo	
	LA4102	Sanyo	
	LA4200	Sanyo	
	LA4201	Sanyo	
	LA4220	Sanyo	
	LA4430	Sanyo	
	TAA611	SGS	
	TBA641	SGS	
	TBA820	SGS	
	TCA830	SGS	180
	NE540	Signetics	
	SE540	Signetics	
	TCA160	Signetics	
	TCA760	Signetics	
	ULN-2280	Sprague	
	ULN-2281	Sprague	
	TBA0800	Telefunken	
	TCA830	Telefunken	
	SN76000	TI	
	SN76011	TI	190
	SN76021	TI	
	SN76024	TI	
	TA7083	Toshiba	
	TA7200	Toshiba	
	TA7204	Toshiba	
Audio, Power Amplifier, 5 10 Watts			
	μA706	Fairchild	
	TBA800	Fairchild	
	TBA810	Fairchild	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Function	Device	Source	Line
Consumer Circuits (Cont'd)			
Audio, Power Amplifier, 5 10 Watts (Cont'd.)			
	TDA2002	**Fairchild (643)**	
	TDA2002A	**Fairchild (643)**	
	HA1308	Hitachi	
	HA1317	Hitachi	
	HA1322	Hitachi	
	HA1338	Hitachi	
	HA1339	Hitachi	
	TBA810	Hitachi	
	TBA800	ITT	10
	M5112	Mitsubishi	
	LM383	National	
	LM383A	National	
	LM384	National	
	TDA2002	National	
	TDA2002A	National	
	µPC571	NEC America	
	µPC578	NEC America	
	µPC1020	NEC America	
	µPC1155	NEC America	20
	µPC1156	NEC America	
	AN272	Panasonic	
	AN315	Panasonic	
	AN7150	Panasonic	
	AN7151	Panasonic	
	SL415	Plessey	
	SL425	Plessey	
	TBA800	Plessey	
	CA810	RCA	
	CA2002	RCA	30
	CA3131	RCA	
	CA3132	RCA	
	SI1010	Sanken	
	LA4420	Sanyo	
	STK011	Sanyo	
	TDA1037	Siemens	
	L165	SGS	
	TBA800	SGS	
	TBA810	SGS	
	TCA940E	SGS	40
	TDA2002	SGS	
	TDA2002A	SGS	
	TDA1037	Siemens	
	TDA1004A	Signetics	
	TDA1010	Signetics	
	TDA2611	Signetics	
	TBA810	Telefunken	
	TCA940	Telefunken	
	SN76005	TI	
	TA7201	Toshiba	50
	TA7202	Toshiba	
	TA7205	Toshiba	
Audio Power Amplifier, >10 Watts			
	LM391	National	
	ESM532	NPC	
	TCA940	SGS	
	TDA2010	SGS	
	TDA2020	SGS	
	SI1020	Sanken	
	SI1030	Sanken	60
	SI1050	Sanken	
	STK015	Sanyo	
	STK016	Sanyo	
	STK020	Sanyo	
	STK022	Sanyo	
	STK024	Sanyo	
	STK025G	Sanyo	
	STK031	Sanyo	
	STK032	Sanyo	
(Continued)			

Function	Device	Source	Line
Consumer Circuits (Cont'd)			
Audio Power Amplifier, >10 Watts (Cont'd.)			70
	STK035	Sanyo	
	STK036	Sanyo	
	STK050	Sanyo	
	STK055	Sanyo	
	STK057	Sanyo	
	STK058	Sanyo	
	STK060	Sanyo	
	STK062	Sanyo	
	STK070	Sanyo	
	STK075	Sanyo	80
	STK077	Sanyo	
	STK078	Sanyo	
	STK080	Sanyo	
	STK082	Sanyo	
	STK084	Sanyo	
	STK086	Sanyo	
	STK0030	Sanyo	
	STK0035	Sanyo	
	STK0040	Sanyo	
	STK0045	Sanyo	90
	STK0065	Sanyo	
Audio Power Amplifier, Dual, <5 Watts			
	LM377	National	
	LM378	National	
	LM1877	National	
	AN274	Panasonic	
	AN313	Panasonic	
	ULN-2274	Sprague	
	ULN-2275	Sprague	
	ULN-2277	Sprague	100
	ULN-2278	Sprague	
	TA7203	Toshiba	
Audio Power Amplifier, Dual, 5 10 Watts			
	DA-101	Delco	
	LM379	National	
	STK433	Sanyo	
	STK435	Sanyo	
	TDA1009	Signetics	
Audio Power Amplifier, Dual, >10 Watts			
	STK040A	Sanyo	110
	STK041	Sanyo	
	STK043	Sanyo	
	STK437	Sanyo	
	STK439	Sanyo	
	STK441	Sanyo	
Audio Preamplifier			
	ZN459C	Ferranti	
	ZN459T	Ferranti	
	HA1406	Hitachi	
	LM3080	National	120
	LM3080A	National	
	ML120	Mitsubishi	
	µPC566	NEC America	
	µPC573	NEC America	
	µPC592	NEC America	
	µPC1016	NEC America	
	µPC1023	NEC America	
	µPC1024	NEC America	
	µPC1027	NEC America	
	µPC1032	NEC America	130
	AN127	Panasonic	
	AN136	Panasonic	
	AN262	Panasonic	
	AN270	Panasonic	
	CA3080	RCA	
	CA3080A	†RCA	
	LA3120	Sanyo	
(Continued)			

Function	Device	Source	Line
Consumer Circuits (Cont'd)			
Audio Preamplifier (Cont'd.)			
	LA3134	Sanyo	
	LA3150	Sanyo	140
	TAA263	Signetics	
	TAA310A	Signetics	
	TAA1002	Signetics	
	TA7063	Toshiba	
	TA7120	Toshiba	
	TA7122	Toshiba	
	TA7129	Toshiba	
	TA7136	Toshiba	
Audio, Preamplifier with ALC			
	LA3201	Sanyo	150
	LA3210	Sanyo	
	TDA1054	SGS	
	TA7055	Toshiba	
Audio, Preamplifier, Dual			
	XR4739	Exar	
	XR4739M	†Exar	
	µA739	Fairchild	
	µA381	Fairchild	
	µA7305	Fairchild	
	µA749	†Fairchild	160
	HA1451	Hitachi	
	HA1452	Hitachi	
	M5111	Mitsubishi	
	M5152	Mitsubishi	
	M51521	Mitsubishi	
	MC1303	Motorola	
	LM1303	National	
	LM381	National	
	LM382	National	
	LM387	National	170
	AN215	Panasonic	
	AN264	Panasonic	
	AN360	Panasonic	
	AN370	Panasonic	
	CA3048	RCA	
	CA3052	RCA	
	LA3115	Sanyo	
	LA3122	Sanyo	
	LA3133	Sanyo	
	LA3155	Sanyo	180
	NE542	Signetics	
	LM381	Signetics	
	LM382	Signetics	
	LM387	Signetics	
	PA239	Signetics	
	TCA490	Signetics	
	ULN-2231	Sprague	
	SN76130	TI	
	SN76131	TI	
	SN76149	TI	190
	TA7108	Toshiba	
Audio Preamplifier, Quad			
	XR4212	Exar	
	XR4212M	†Exar	
Automotive Adaptive Sense Amplifier (one shot with peak detector adjusted shut off threshold)			
	LM1815	National	
Automotive, Ignition Circuit			
	MC3333	Motorola	
Automotive, Speed Control Processor			200
	MC14460	Motorola	
Automotive, Speedometer Circuit			
	SAY115	ITT	

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Consumer Circuits (Cont'd)

Consumer Circuits (Cont'd)

Function	Device	Source	Line
Automotive, Tachometer Circuit. See Tachometer Circuit below.			
Automotive, Voltage Regulator			
	FA8008	Hitachi	
	FA8025	Hitachi	
	TCA700	ITT	
	MC3325	Motorola	
	MC3326	Motorola	
Calculator			
	C/CF583	GI	
	C/CF585	GI	
	C/CF589	GI	10
	C/CF593	GI	
	C/CF594	GI	
	C/CF595	GI	
	C/CF596	GI	
	C/CF598	GI	
	C/CF599	GI	
	C683D	GI	
	C/CF683	GI	
	C685D	GI	
	C/CF685	GI	20
	C/CF687	GI	
	C687D	GI	
	CF689	GI	
	C689D/HV	GI	
	HD3633	Hitachi	
	MPS2529	MOS	
	MM5725	National	
	MM5734	National	
	MM5736	National	
	MM5737	National	30
	MM5738	National	
	MM5739	National	
	MM5758	National	
	MM5760	National	
	MM5762	National	
	MM5763	National	
	MM5764	National	
	MM5765	National	
	MM57123	National	
	MM5766	National	40
	MM5767	National	
	MM5777	National	
	MM5780	National	
	MM5791	National	
	MM5794	National	
	MM5795	National	
	MM57103	National	
	MM57104	National	
	MM57109	National	
	μPD276	NEC America	50
	μPD277	NEC America	
	μPD278	NEC America	
	μPD284	NEC America	
	μPD286	NEC America	
	μPD299	NEC America	
	μPD940	NEC America	
	μPD941	NEC America	
	μPD943	NEC America	
	μPD946	NEC America	
	μPD947	NEC America	60
	μPD950	NEC America	
	μPD951	NEC America	
	μPD952	NEC America	
	μPD1201	NEC America	
	μPD1801	NEC America	
	MN5530	Panasonic	
	MN5540	Panasonic	

(Continued)

Consumer Circuits (Cont'd)

Function	Device	Source	Line
Calculator (Cont'd.)			
	MN5550	Panasonic	
	MN5556	Panasonic	70
	MN5701	Panasonic	
	MN5710	Panasonic	
	MN5750	Panasonic	
	MN5752	Panasonic	
	A4521	Rockwell	
	A550	Rockwell	
Calculator, Display Interface, (use with printer)			
	C719	GI	
	C720	GI	
Calculator, Printing			80
	EA7251	EA	
	EA7261	EA	
	C716	GI	
	C717	GI	
	C717X	GI	
	C718	GI	
	μPD299	NEC America	
	1022	SMC	
Camera, Exposure Control			
	MCC100	Micro Comp	90
	MCC102	Micro Comp	
	MCC122	Micro Comp	
	MCC127	Micro Comp	
	MCC129	Micro Comp	
	MCC130	Micro Comp	
	MCC131	Micro Comp	
	MCC132	Micro Comp	
	MCC137	Micro Comp	
	MCC580	Micro Comp	
	μPC551	NEC America	100
	μPC558	NEC Amenca	
	μPC589	NEC America	
Camera, Strobe Lights			
	MCC139	Micro Comp	
Citizens Band Programmer, for PLL			
	DS8900	National	
	MM57190	National	
	LC7120	Sanyo	
	LC7123	Sanyo	
Citizens Band Remote Controller and Display Driver			110
	FCB0801	Fairchild	
	MC3391	Motorola	
	MN6080	Panasonic	
	LC7181	Sanyo	
	LC7190	Sanyo	
	LC7191	Sanyo	
Citizens Band Controller			
	TMS1022	TI	
Citizen Band, See Linear Phase Locked Loops/Synthesizers			120
Clock (See also Digital CMOS Oscillators/Dividers)			
	S1427A	AMI	
	S1998A	AMI	
	S1998B	AMI	
	S1998C	AMI	
	S1998E	AMI	
	S1998F	AMI	
	S2622	AMI	
	S2709	AMI	
	S1856	AMI	130
	AY5-1200A	GI	
	AY5-1202A	GI	

(Continued)

Consumer Circuits (Cont'd)

Function	Device	Source	Line
Clock (See also Digital CMOS Oscillators/Dividers) (Cont'd.)			
	AY5-1203A	GI	
	AY5-1204A	GI	
	AY5-1224A	GI	
	CK3500	GI	
	ICM7028	Intersil	
	ICM7051	Intersil	
	SAJ300	ITT	140
	TAA780	ITT	
	TCA860	ITT	
	C1200	LSI Comp	
	MC14440	Motorola	
	MM5218	National	
	MM5309	National	
	MM5311	National	
	MM5312	National	
	MM5313	National	
	MM5314	National	150
	MM5315	National	
	MM5375	National	
	MM5376	National	
	MM5377	National	
	MM5378	National	
	MM5379	National	
	MM5382	National	
	MM5383	National	
	μPD811	NEC America	
	μPD815	NEC America	160
	μPD816	NEC America	
	CD22010	RCA	
	CD22011	RCA	
	CD22012	RCA	
	CD22013	RCA	
	CD22014	RCA	
	CD22015	RCA	
	MN6070	Panasonic	
	SAA1028	Signetics	
	SAJ250	Signetics	170
	UCN-4103	Sprague	
	UCN-4104	Sprague	
	UCN-4112	Sprague	
Clock, Alarm Clock			
	S1998A	AMI	
	S1998B	AMI	
	S1998C	AMI	
	S1998E	AMI	
	S1998F	AMI	
	S2622	AMI	180
	EA5316	EA	
	EA7316	EA	
	EA7317	EA	
	3817	Fairchild	
	CK3000	GI	
	CK3100	GI	
	CK3200	GI	
	CK3400	GI	
	ICM1115	Intersil	
	ICM7038	Intersil	190
	ICM7049	Intersil	
	ICM7050	Intersil	
	MPS7111	Micro Power	
	MK50250	Mostek	
	MK50253	Mostek	
	MK50254	Mostek	
	MM5316	National	
	MM5370	National	
	MM5371	National	
	MM5375	National	200
	MM5376	National	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Function	Device	Source	Line
Consumer Circuits (Cont'd)			
Clock, Alarm Clock (Cont'd.)			
	MM5385	National	
	MM5386	National	
	MM5387	National	
	MM5396	National	
	MM5397	National	
	MM53108	National	
	MM5402	National	
	MM5405	National	
	μPD832	NEC America	10
	μPD833	NEC America	
	μPD5388	NEC America	
	MN6052	Panasonic	
	MN6053	Panasonic	
	MN6091	Panasonic	
	MN6092	Panasonic	
	CD22016	RCA	
	SAA114	Signetics	
	UCN-4111	Sprague	
	UCN-4113	Sprague	20
	UCN-4114	Sprague	
Clock, Clock Radio			
	S1998A	AMI	
	S1998B	AMI	
	S1998C	AMI	
	S1988E	AMI	
	S1988F	AMI	
	3817	Fairchild	
	CK3300	GI	
	MM5282	National	30
	MM5283	National	
	MM5284	National	
Coinbox Circuit			
	AY1-8622	GI	
	LM8091	Sanyo	
	LM8092	Sanyo	
FM Detector. See Linear Phase Locked Loop Circuits and IF Amplifier/Detector below.			
FM IF Amplifier			
	μA753	Fairchild	40
	μA3076	Fairchild	
	HA1150	Hitachi	
	HA1211	Hitachi	
	MC1350	Motorola	
	MC1355	Motorola	
	MC3310	Motorola	
	AN278	Panasonic	
	AN377	Panasonic	
	CA3002	†RCA	
	CA3005	†RCA	50
	CA3006	†RCA	
	CA3012	†RCA	
	CA3028	†RCA	
	CA3076	†RCA	
	LA1111	Sanyo	
	LA1222	Sanyo	
	ULN2208	Signetics	
	ULN2209	Signetics	
	ULN-2208	Sprague	
	ULN-2209	Sprague	60
	SN76676	TI	
	SN76678	TI	
FM IF Amplifier/Detector			
	μA2136	Fairchild	
	μA3065	Fairchild	
	μA3075	Fairchild	
	μA3089	Fairchild	
(Continued)			

Function	Device	Source	Line
Consumer Circuits (Cont'd)			
FM IF Amplifier/Detector (Cont'd.)			
	μA3089M	†Fairchild	
	HA1137	Hitachi	70
	M5143	Mitsubishi	
	M5144	Mitsubishi	
	M51172	Mitsubishi	
	MC1351	Motorola	
	MC1356	Motorola	
	MC1375	Motorola	
	LM1351	National	
	LM1841	National	
	LM2111	National	
	LM2113	National	80
	LM273	National	
	LM274	National	
	LM373	National	
	LM374	National	
	LM3065	National	
	LM3075	National	
	LM3089	National	
	TBA120	National	
	μPC1004	NEC America	
	μPC1028	NEC America	90
	TAA661	Plessey	
	TBA120	Plessey	
	TBA750	Plessey	
	CA2111A	†RCA	
	CA3014	†RCA	
	CA3041	RCA	
	CA3042	RCA	
	CA3043	†RCA	
	CA3065	RCA	
	CA3075	†RCA	100
	CA3089	†RCA	
	LA1230	Sanyo	
	TDA1200	SGS	
	TDA1230	SGS	
	S041	Siemens	
	TBA120	Siemens	
	TDA1047	Siemens	
	CA3089	Signetics	
	TBA120	Signetics	
	TBA750	Signetics	110
	TCA420	Signetics	
	TCA770	Signetics	
	ULN2111	Signetics	
	ULN2211	Signetics	
	ULN-2111	Sprague	
	ULN-2113	Sprague	
	ULN-2136	Sprague	
	ULN-2289	Sprague	
	TBA120	Telefunken	
	SN76642	TI	120
	SN76643	TI	
	SN76669	TI	
	SN76675	TI	
	SN76689	TI	
	TA7028	Toshiba	
FM, IF Amplifier, PLL, Squelch, narrow band			
	SL660	Plessey	
	SL662	Plessey	
	SL664	Plessey	
	SL665	Plessey	130
FM Muting/Tuning Point System			
	HA1149	Hitachi	
FM Noise Canceller			
	M51011	Mitsubishi	
	AN101	Panasonic	
(Continued)			

Function	Device	Source	Line
Consumer Circuits (Cont'd)			
FM Noise Canceller (Cont'd.)			
	LA2100	Sanyo	
FM Receiver System with squelch and scan control			
	MC3357	Motorola	
FM, RF/IF Amplifier			140
	AN219	Panasonic	
	CA3127	†RCA	
	TCA770	Signetics	
FM Stereo Decoder			
	XR1310	Exar	
	μA732	Fairchild	
	μA758	Fairchild	
	μA767	Fairchild	
	μA1310	Fairchild	
	HA1115	Hitachi	150
	HA1120	Hitachi	
	HA1142	Hitachi	
	HA1156	Hitachi	
	HA1173	Hitachi	
	M5132	Mitsubishi	
	M5133	Mitsubishi	
	MC1310	Motorola	
	LM1304	National	
	LM1305	National	
	LM1307	National	160
	LM1310	National	
	LM1800	National	
	LM1810	National	
	μPC554	NEC America	
	μPC585	NEC America	
	μPC587	NEC America	
	μPC1026	NEC America	
	AN211	Panasonic	
	AN271	Panasonic	
	AN362	Panasonic	170
	AN363	Panasonic	
	SL758	Plessey	
	SL1310	Plessey	
	CA758	RCA	
	CA1310	RCA	
	CA3090A	†RCA	
	LA3300	Sanyo	
	LA3301	Sanyo	
	LA3350	Sanyo	
	TBA450	Siemens	180
	μA758	Signetics	
	TCA290	Signetics	
	TDA1005	Signetics	
	ULN-2120	Sprague	
	ULN-2121	Sprague	
	SN76104	TI	
	SN76105	TI	
	SN76110	TI	
	SN76111	TI	
	SN76113	TI	190
	SN76115	TI	
	SN76116	TI	
	TA7154	Toshiba	
	TA7156	Toshiba	
	TA7159	Toshiba	
FM Tuner			
	TDA1062	Telefunken	
Four Channel Sound			
	μA1312	Fairchild	
	HA1327	Hitachi	200
	HA1328	Hitachi	
	HA1333	Hitachi	
(Continued)			

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Consumer Circuits (Cont'd)

Function	Device	Source	Line
Consumer Circuits (Cont'd)			
Four Channel Sound (Cont'd.)			
	HA1334	Hitachi	
	MC1312	Motorola	
	MC1314	Motorola	
	MC1315	Motorola	
	LM1852	National	
	LM1853	National	
	QSI5022	Panasonic	
	CG392	Signetics	
	CG477	Signetics	10
	TA7117	Toshiba	
Games, T.V.			
	AY3-8500	GI	
	AY3-8500-1	GI	
	AY3-8550	GI	
	AY3-8550-1	GI	
	AY3-8600	GI	
	AY3-8600-1	GI	
	AY3-8601	GI	
	AY3-8602	GI	20
	AY3-8603	GI	
	AY3-8604	GI	
	AY3-8605	GI	
	AY3-8700	GI	
	AY3-8700-1	GI	
	AY3-8900	GI	
	AY3-8900-1	GI	
	MPS7100	MOS	
	LM1889	National	
	MM4789	National	30
	MM5789	National	
	MM53104	National	
	MM57100	National	
	MM57105	National	
	MM57106	National	
	VES	Nortec	
	C10091	Synertek	
	SN76400	TI	
	SN76401	TI	
	SN76402	TI	
	SN76423	TI	40
	SN76424	TI	
	SN76425	TI	
	SN76426	TI	
	SN76427	TI	
	SN76428	TI	
	SN76429	TI	
	SN76430	TI	
	SN76431	TI	
	SN76442	TI	50
	SN76443	TI	
	SN76445	TI	
	SN76450	TI	
	SN76460	TI	
	SN76462	TI	
Games, T.V. Color Converter (converts game chip B/W outputs to Color)			
	AY3-8515-1	GI	
	AY3-8615-1	GI	
Ground Fault Interrupter			60
	μA7390	Fairchild	
	MC3426	Motorola	
	LM1850	National	
Microwave Oven Controller			
	TMS1117	TI	
Motor Speed Regulator			
	μA7391	Fairchild	
	MCC140	Micro Comp	
(Continued)	LM1815	National	

Function	Device	Source	Line
Consumer Circuits (Cont'd)			
Motor,Speed Regulator			70
	SL440	Plessey	
	TCA900	SGS	
	TCA910	SGS	
	TDA1151	SGS	
Motor Speed Regulator, with erase oscillator, for tape recorders			
	TDA1003A	Signetics	
Motor Speed Regulator, with tape end indicator, for tape recorders			
	TDA1006	Signetics	80
Motor, Stepping Motor Drive			
	SAA1027	Signetics	
Music, Electronic Piano Keyboard Interface			
	AY1-1320	GI	
Music, Voltage Controlled Oscillator			
	SSM2030	SSM	
Music, Voltage Controlled Transient Generator			
	SSM2050	SSM	
Music, See Organ Circuits			
Organ, Arpeggio, Chord and Bass Accompaniment Generator			90
	M251	SGS	
Organ, Chord Generator			
	AY5-1317A	GI	
	S163	Siemens	
Organ, Delay Circuit, See also Analog Shift Registers under Linear Other Devices.			
	S10110	AMI	
	S10111	AMI	
	TCA350	ITT	100
	SAD512	Reticon	
	SAD1024	Reticon	
Organ, Electronic Attenuator			
	MC3340	Motorola	
	CA3080	RCA	
	CA3080A	†RCA	
Organ, Frequency Divider, 4 Stage			
	AY1-5051	GI	
Organ, Frequency Divider, 5 Stage			
	AY1-6721/5	GI	110
Organ, Frequency Divider, 6 Stage			
	S10129	AMI	
	S10130	AMI	
	S10131	AMI	
	AY1-1006	GI	
	AY1-2006	GI	
	AY1-6721/6	GI	
	HD3111	Hitachi	
	MM5554	National	
	MM5823	National	120
	MM5824	National	
	LM3216	Sanyo	
Organ, Frequency Divider, 7 Stage			
	S2193	AMI	
	F4727	Fairchild	
	AY1-1007B	GI	
	AY1-5050	GI	
	ITT3715	ITT	
	SAA1024	ITT	
	MC1302	Motorola	130
	HBF4727	SGS	
	HBF4737	SGS	
(Continued)			

Function	Device	Source	Line
Consumer Circuits (Cont'd)			
Organ, Frequency Divider, 7 Stage (Cont'd.)			
	SAJ210	SGS	
	SAJ410	Siemens	
	SAJ110	Signetics	
Organ, Counter/Divider, ÷ 2^7, 2^{10}, 2^{11}, 2^{12}, 2^{15}, 2^{16}			
	AY9-1000	GI	
Organ, Frequency Generator. See also Organ, Top Octave Generator			140
	M081	SGS	
	M082	SGS	
	M087	SGS	
	SAJ205	Siemens	
Organ, Gate for Key Contact			
	TDA0470	ITT	
	H629	SGS	
	H632	SGS	
Organ, Latch Pedal Sustain			
	M147	SGS	150
Organ, Noise Generator			
	S2688	AMI	
	MM5837	National	
Organ, Priority Latching Network			
	AY1-1313	GI	
Organ, Rhythm Circuit			
	S2566	AMI	
	S2567	AMI	
	S8890	AMI	
	S9660	AMI	160
	AY5-1315	GI	
	MCM6550	Motorola	
	MM5871	National	
	LM8271	Sanyo	
	LM8272	Sanyo	
	LM8371	Sanyo	
	LM8372	Sanyo	
	LM8471	Sanyo	
	LM8972	Sanyo	
	M252	SGS	170
	M253	SGS	
	M254	SGS	
	M255	SGS	
Organ, Serial to Parallel Converter, 33 Bits			
	MM5559	National	
Organ, Top Octave Generator			
	S50240	AMI	
	S50241	AMI	
	S50242	AMI	
	S50243	AMI	180
	S50244	AMI	
	S50245	AMI	
	AY1-0212	GI	
	AY1-0212A	GI	
	AY3-0214	GI	
	AY3-0215	GI	
	AY3-0216	GI	
	MK50240	Mostek	
	MK50241	Mostek	
	MK50242	Mostek	190
	MM5555	National	
	MM5556	National	
	MM5832	National	
	MM5833	National	
	MM5891	National	
	NC1183	Nitron	
	NC1184	Nitron	
	LM8071	Sanyo	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Function	Device	Source	Line
Consumer Circuits (Cont'd)			
Organ, Voltage Controlled Filter, Four Stage	SSM2040	SSM	
Radio Receiver, Noise Inverter for car radios	TDA1068	Telefunken	
Radio, Receiver, Counter/Display and Clock	AY5-8100	GI	
	AY5-8102	GI	
Remote Control Transmitters, Receivers. See Citizen Band and T.V. Remote Control above			
RF Amplifier/Mixer	CA3005	†RCA	10
	CA3006	†RCA	
	CA3049	†RCA	
	CA3127	†RCA	
	SD6000	Signetics	
RF Detector/Video Amplifier	SL510	Plessey	
	SL511	Plessey	
	CA3068	RCA	
Servo Driver	NE543	Signetics	20
	NE544	Signetics	
	NE644	Signetics	
Security Systems Detector	**L911**	**Siliconix**	**(983)**
Smoke Detector	MEM4962	GI	
	MEM4963	GI	
	MCC158	Micro Comp	
	MCC258	Micro Comp	
	MD4301	Mitel	30
	MC14461	Motorola	
	MC14462	Motorola	
	LM1801	National	
	NF5301	National	
	ESM427	NPC	
	SM110	Siliconix	
	SM120	Siliconix	
Sonar Transceiver	LM1812	National	
SSB Detector	SL623C	Plessey	40
	SL624C	Plessey	
Synthesizers. See Linear Phase Locked Loop/Synthesizer Circuits			
Switches, Capacitance or Touch Sensing	**S9260**	**AMI**	**(364)**
	S9261	**AMI**	**(364)**
	S9262	**AMI**	**(359)**
	S9263	**AMI**	**(364)**
	S9264	**AMI**	**(364)**
	S9265	**AMI**	**(364)**
	S9266	**AMI**	**(359)**
	SAS560	Siemens	
	SAS570	Siemens	
	SAS580	Siemens	
	SAS590	Siemens	
	TCA205	Siemens	
	SAS660	Telefunken	
	SAS670	Telefunken	
	SAS6600	Telefunken	60
	SAS6610	Telefunken	
	SAS6700	Telefunken	
	SAS6710	Telefunken	
	U112	Telefunken	
(Continued)			

Function	Device	Source	Line
Consumer Circuits (Cont'd)			
Switches, Capacitance or Touch Sensing (Cont'd.)	U113	Telefunken	
	U221	Telefunken	
Tachometer Circuit	SAK215	ITT	
	LM2907	National	70
	LM2917	National	
	AN603	Panasonic	
	SN76810	TI	
Telephone. See Linear Telecommunication Circuits			
Timers. See Appliance Timers, Clock, Watch circuits in this section and Linear Timers			
Tuning Voltage Stabilizer, for use with variable capacitance diodes	ZTK6.3	ITT	
	ZTK9	ITT	80
	ZTK11	ITT	
	ZTK18	ITT	
	ZTK22	ITT	
	ZTK23	ITT	
	ZTK33	ITT	
	TAA550	Signetics	
	TCA530	Signetics	
	TCA750	Signetics	
	TAA550	SGS	
T.V. AFT System	μA3064	†Fairchild	90
	HA1108	Hitachi	
	HA1126	Hitachi	
	M5134	Mitsubishi	
	M5135	Mitsubishi	
	MC1364	Motorola	
	LM3064	National	
	μPC423	NEC America	
	AN220	Panasonic	
	AN221	Panasonic	100
	AN222	Panasonic	
	AN320	Panasonic	
	AN321	Panasonic	
	AN325	Panasonic	
	AN326	Panasonic	
	CA3044	†RCA	
	CA3064	†RCA	
	CA3139	RCA	
	LA1364	Sanyo	
	ULN-2264	Sprague	110
	SN76565	TI	
	TA7050	Toshiba	
	TA7070	Toshiba	
T.V. Camera Sync. Generator	3262A	Fairchild	
	3262B	Fairchild	
	ZNA134	Ferranti	
	MM5320	National	
	MM5321	National	
	MN6060	Panasonic	120
TV, CATV Amplifiers	CA2100	TRW	
	CA2300	TRW	
	CA2301	TRW	
	CA2418	TRW	
	CA2600	TRW	
	CA2601	TRW	
T.V. Channel Display	AY5-8300	GI	
(Continued)			

Function	Device	Source	Line
Consumer Circuits (Cont'd)			
T.V. Channel Display (Cont'd.)	AY5-8301	GI	130
T.V. Channel Display with Time	AY5-8310	GI	
	AY5-8311	GI	
	AY5-8321	GI	
	AY5-8322	GI	
	AY5-8324	GI	
	AY5-8320	GI	
	MM5318	National	
	MM5810	National	140
	MM5841	National	
	MM58106*	National	
T.V. Channel Selection	M51230	Mitsubishi	
	M51231	Mitsubishi	
	μPC1009	NEC America	
	LB1500	Sanyo	
	LB1501	Sanyo	
	LB1515	Sanyo	
	SAS560	Siemens	150
	SAS570	Siemens	
	SAS580	Siemens	
	SAS590	Siemens	
	TDA2620	Signetics	
	TDA2630	Signetics	
	TDA2631	Signetics	
	ML231	TI	
	ML232	TI	
	SN76701	TI	
	SN76702	TI	160
	SN76710	TI	
	SN76721	TI	
	SN76727	TI	
	TM4357	Toshiba	
T.V. Chroma Circuits	μA746	Fairchild	
	μA780	Fairchild	
	μA781	Fairchild	
	μA787	Fairchild	
	μA788	Fairchild	170
	μA3067	Fairchild	
	TAA630	Fairchild	
	TBA510	Fairchild	
	TBA520	Fairchild	
	TBA540	Fairchild	
	TBA560	Fairchild	
	TBA990	Fairchild	
	TDA2510	Fairchild	
	TDA2521	Fairchild	
	HA1153	Hitachi	180
	HA1157	Hitachi	
	HA1158	Hitachi	
	HA1177	Hitachi	
	M5108	Mitsubishi	
	M5192	Mitsubishi	
	M5190	Mitsubishi	
	MC1323	Motorola	
	MC1324	Motorola	
	MC1327	Motorola	
	MC1398	Motorola	190
	MC1399	Motorola	
	LM746	National	
	LM1828	National	
	LM1848	National	
	LM3067	National	
	LM3070	National	
	LM3071	National	
(Continued)			

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Consumer Circuits (Cont'd)

Function	Device	Source	Line
Consumer Circuits (Cont'd)			
T.V. Chroma Circuits (Cont'd.)			
	LM3126	National	
	TBA510	National	
	TBA530	National	
	TBA540	National	
	TBA560	National	
	TBA990	National	
	μPC29	NEC America	
	μPC31	NEC America	
	μPC32	NEC America	10
	μPC562	NEC America	
	μPC580	NEC America	
	μPC1380	NEC America	
	μPC1381	NEC America	
	AN225	Panasonic	
	AN227	Panasonic	
	AN234	Panasonic	
	AN235	Panasonic	
	AN236	Panasonic	
	AN237	Panasonic	20
	AN242	Panasonic	
	AN281	Panasonic	
	AN282	Panasonic	
	AN288	Panasonic	
	AN289	Panasonic	
	AN342	Panasonic	
	AN343	Panasonic	
	AN380	Panasonic	
	SL901	Plessey	
	SL917	Plessey	30
	SL918	Plessey	
	SL1327	Plessey	
	TBA520	Plessey	
	TBA530	Plessey	
	TBA540	Plessey	
	TBA560	Plessey	
	TBA990	Plessey	
	TCA800	Plessey	
	CA1398	RCA	
	CA3066	RCA	40
	CA3067	RCA	
	CA3070	RCA	
	CA3071	RCA	
	CA3072	RCA	
	CA3121	RCA	
	CA3125	RCA	
	CA3126	RCA	
	CA3128	RCA	
	CA3135	RCA	
	CA3137	RCA	50
	CA3143	RCA	
	CA3144	RCA	
	CA3170	RCA	
	CA3172	RCA	
	LA1366N	Sanyo	
	LA1367	Sanyo	
	LA1368	Sanyo	
	LA1369	Sanyo	
	LA1373	Sanyo	
	LA1374	Sanyo	60
	LA1375	Sanyo	
	LA1376	Sanyo	
	LA1397	Sanyo	
	MC1327	Signetics	
	MC1399	Signetics	
	TAA630	Signetics	
	TAA6301	Siemens	
	TBA327	Signetics	
	TBA395	Signetics	
(Continued)			

Function	Device	Source	Line
Consumer Circuits (Cont'd)			
T.V. Chroma Circuits (Cont'd.)			70
	TBA396	Signetics	
	TBA500	Signetics	
	TBA510	Signetics	
	TBA520	Signetics	
	TBA530	Signetics	
	TBA540	Signetics	
	TBA550	Signetics	
	TBA560	Signetics	
	TBA990	Signetics	
	TCA640	Signetics	80
	TCA650	Signetics	
	TCA660	Signetics	
	TCA800	Signetics	
	TDA2500	Signetics	
	TDA2510	Signetics	
	TDA2520	Signetics	
	TDA2522	Signetics	
	TDA2523	Signetics	
	TDA2530	Signetics	
	TDA2560	Signetics	90
	TDA2670	Signetics	
	ULN-2114	Sprague	
	ULN-2124	Sprague	
	ULN-2127	Sprague	
	ULN-2216	Sprague	
	ULN-2224	Sprague	
	ULN-2228	Sprague	
	ULN-2229	Sprague	
	ULN-2269	Sprague	
	ULN-2298	Sprague	100
	TBA520	Telefunken	
	TBA530	Telefunken	
	TBA540	Telefunken	
	TBA560	Telefunken	
	TBA990	Telefunken	
	TDA2140	Telefunken	
	TDA2150	Telefunken	
	TDA2151	Telefunken	
	TDA2160	Telefunken	
	TDA2161	Telefunken	110
	SN76242	TI	
	SN76243	TI	
	SN76246	TI	
	SN76267	TI	
	SN76298	TI	
	TA7053	Toshiba	
	TA7102	Toshiba	
	TA7103	Toshiba	
	TA7141	Toshiba	
	TA7150	Toshiba	120
	TA7161	Toshiba	
	TA7168	Toshiba	
	TA7169	Toshiba	
T.V. Color Bar Generator			
	MM5332	National	
T.V. Convergence Circuit			
	HA1146	Hitachi	
	HA1147	Hitachi	
	HA1148	Hitachi	
T.V. Games, see Games, T.V.			130
T.V. Horizontal Processor			
	μA1391	Fairchild	
	μA1394	Fairchild	
	TBA920	Fairchild	
	HA1160	Hitachi	
	TDA9400	ITT	
(Continued)			

Function	Device	Source	Line
Consumer Circuits (Cont'd)			
T.V. Horizontal Processor (Cont'd.)			
	TDA9500	ITT	
	MC1391	Motorola	
	MC1394	Motorola	140
	LM1391	National	
	LM1394	National	
	TBA920	National	
	μPC570	NEC America	
	SL451	Plessey	
	TBA920	Plessey	
	TBA940	Plessey	
	TBA950	Plessey	
	CA1391	RCA	
	CA1394	RCA	150
	CA3147	RCA	
	CA920	RCA	
	LA1384	Sanyo	
	TBA720A	Signetics	
	TBA920	Signetics	
	TDA2571	Signetics	
	TDA2573	Signetics	
	TDA2581	Signetics	
	TDA2590	Signetics	
	ULN-2291	Sprague	160
	ULN-2294	Sprague	
	SN76525	TI	
	TA7151	Toshiba	
T.V. Horizontal & Vertical Processor			
	M5188	Mitsubishi	
	LM1880	National	
	AN202	Panasonic	
	AN232	Panasonic	
	AN332	Panasonic	
	AN334	Panasonic	170
	LA1381	Sanyo	
	LA1382	Sanyo	
	TCA511	SGS	
T.V. Picture Sharpness			
	TA7126	Toshiba	
T.V. Remote Control (also for other remote control applications)			
	S2600	AMI	
	S2601	AMI	
	S2742	AMI	180
	S2743	AMI	
	S2744	AMI	
	AY5-8410	GI	
	AY5-8411	GI	
	AY5-8420	GI	
	AY5-8450	GI	
	AY5-8460	GI	
	AY5-8461	GI	
	SAA1024	GI	
	SAA1025-01	GI	190
	SAA1025-02	GI	
	SAA1024	ITT	
	SAA1025	ITT	
	SAA1130	ITT	
	MC14422	Motorola	
	MC6525	Motorola	
	MC6526	Motorola	
	MC6527	Motorola	
	LM1812	National	
	CA3035	†RCA	200
	SAF1031	Signetics	
	SAF1032	Signetics	
	M054	SGS	
	M055	SGS	
(Continued)			

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Consumer Circuits (Cont'd)

Function	Device	Source	Line
T.V. Remote Control (also for other remote control applications) (Cont'd.)			
	M1024	SGS	
	M1025	SGS	
	SAB2000	Telefunken	
	SAB2010	Telefunken	
	SAB2020	Telefunken	
	U318M	Telefunken	
	U321M	Telefunken	
	SN76730	TI	10
	TM4500	Toshiba	
T.V. Signal Processor (Jungle Circuit)			
	HA1155	Hitachi	
	HA1159	Hitachi	
	HA1180	Hitachi	
	MC1344	Motorola	
	LM1845	National	
	AN228	Panasonic	
	AN229	Panasonic	
	AN230	Panasonic	20
	AN231	Panasonic	
	AN249	Panasonic	
	AN328	Panasonic	
	AN331	Panasonic	
	AN349	Panasonic	
	AN350	Panasonic	
	SN76544	Plessey	
	TBA550	Plessey	
	CA3120	RCA	
	CA3142	RCA	30
	LA1388	Sanyo	
	LA3181	Sanyo	
	LA3182	Sanyo	
	LA3187	Sanyo	
	TBA311	SGS	
	TBA550	Signetics	
	TBA890	Signetics	
	TBA900	Signetics	
	TDA2680	Signetics	
	TDA2690	Signetics	40
	ULN-2125	Sprague	
	SN76524	TI	
	SN76544	TI	
	SN76545	TI	
T.V. Sound Circuit			
	μA3065	Fairchild	
	HA1124	Hitachi	
	HA1125	Hitachi	
	HA1154	Hitachi	
	TDA1035	ITT	50
	M5143	Mitsubishi	
	M5144	Mitsubishi	
	MC1331	Motorola	
	MC1351	Motorola	
	MC1357	Motorola	
	MC1358	Motorola	
	TDA1190	Motorola	
	LM1351	National	
	LM1808	National	
	LM2111	National	60
	LM2113	National	
	LM3065	National	
	TBA120	National	
	μPC16	NEC America	
	μPC558	NEC America	
	μPC575	NEC America	
	μPC576	NEC America	
	μPC1022	NEC America	
	AN239	Panasonic	
	AN206	Panasonic	70

(Continued)

Consumer Circuits (Cont'd)

Function	Device	Source	Line
T.V. Sound Circuit (Cont'd.)			
	AN240	Panasonic	
	AN241	Panasonic	
	AN255	Panasonic	
	AN341	Panasonic	
	AN340	Panasonic	
	SL432	Plessey	
	SL437	Plessey	
	TAA570	Plessey	
	TAA661	Plessey	80
	TBA120	Plessey	
	TBA750	Plessey	
	CA2111	†RCA	
	CA3041	RCA	
	CA3042	RCA	
	CA3043	†RCA	
	CA3065	RCA	
	CA3075	†RCA	
	CA3134	RCA	
	LA1363	Sanyo	90
	LA1365	Sanyo	
	TDA1190	SGS	
	TDA1290	SGS	
	TBA120	Siemens	
	TBA120	Signetics	
	TBA750	Signetics	
	TDA2610	Signetics	
	ULN2111	Signetics	
	ULN2211	Signetics	
	ULN-2111	Sprague	100
	ULN-2165	Sprague	
	ULN-2211	Sprague	
	ULN-2212	Sprague	
	TBA120	Telefunken	
	SN76643	TI	
	SN76651	TI	
	SN76660	TI	
	SN76665	TI	
	SN76666	TI	
	SN76688	TI	110
	TA7051	Toshiba	
	TA7071	Toshiba	
	TA7072	Toshiba	
	TA7073	Toshiba	
	TA7130	Toshiba	
	TA7146	Toshiba	
T.V. Timer, Programmable			
	MM53100	National	
	MM53105	National	
T.V. Tone Control			120
	TA7125	Toshiba	
T.V. Touch Tuner. See also Switches, Capacitance above.			
	TDA2620	Signetics	
	TDA2630	Signetics	
	TDA2631	Signetics	
	SAS660	Telefunken	
	SAS670	Telefunken	
T.V. Tuner Controller			
	AY3-8203	GI	130
	AY5-8290	GI	
	MEM4956	GI	
	T1001	GI	
	T1101	GI	
	T1201	GI	
	μPC1010	NEC America	
	μPC1011	NEC America	

Consumer Circuits (Cont'd)

Function	Device	Source	Line
T.V. Tuning Indicator			
	AY3-8330	GI	
T.V. Tuning System			140
	Economega	GI	
	Omega	GI	
T.V. Vertical Deflection			
	TDA1170	Fairchild	
	M5188	Mitsubishi	
	MC1393	Motorola	
	μPC572	NEC America	
	μPC1031	NEC America	
	AN232	Panasonic	
	AN332	Panasonic	150
	AN334	Panasonic	
	LA1383	Sanyo	
	TDA1170	SGS	
	TDA1270	SGS	
	TDA2600	Signetics	
	TA7152	Toshiba	
	TA7166	Toshiba	
T.V. Video Circuits			
	TBA970	Fairchild	
	AY3-8900	GI	160
	AY3-8900-1	GI	
	HA1144	Hitachi	
	HA1152	Hitachi	
	M5167	Mitsubishi	
	M5168	Mitsubishi	
	M5169	Mitsubishi	
	M5181	Mitsubishi	
	M5184	Mitsubishi	
	MC1330	Motorola	
	MC1331	Motorola	170
	MC1349	Motorola	
	MC1350	Motorola	
	MC1352	Motorola	
	LM1807	National	
	LM1889	National	
	TBA440	National	
	μPC50	NEC America	
	μPC595	NEC America	
	μPC596	NEC America	
	AN239	Panasonic	180
	AN245	Panasonic	
	AN246	Panasonic	
	AN247	Panasonic	
	AN248	Panasonic	
	AN279	Panasonic	
	AN349	Panasonic	
	AN350	Panasonic	
	SL437	Plessey	
	SL456	Plessey	
	SL457	Plessey	190
	TBA440	Plessey	
	TCA270	Plessey	
	TDA440	Plessey	
	CA270	RCA	
	CA1352	RCA	
	CA3068	RCA	
	CA3136	RCA	
	LA1352	Sanyo	
	LA1353	Sanyo	
	TBA1440	Siemens	200
	TBA1441	Siemens	
	TBA440	Signetics	
	TBA1440	Signetics	
	TBA1441	Signetics	
	TBA14406	Signetics	
	TCA270	Signetics	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Consumer Circuits (Cont'd)

Consumer Circuits (Cont'd)

Function	Device	Source	Line
T.V. Video Circuits (Cont'd.)			
	TCA540	Signetics	
	TDA2540	Signetics	
	TDA2541	Signetics	
	TDA440	SGS	
	TDA440	Telefunken	
	TDA4400	Telefunken	
	TDA4410	Telefunken	
	TDA4420	Telefunken	
	TDA4421	Telefunken	10
	SN76600	TI	
	SN76644	TI	
	SN76650	TI	
	TA7069	Toshiba	
	TA7074	Toshiba	
	TA7076	Toshiba	
	TA7124	Toshiba	
	TA7145	Toshiba	
	TA7147	Toshiba	
	TA7162	Toshiba	20
	TA7175	Toshiba	
Video Tape Recorder			
	AN301	Panasonic	
	AN302	Panasonic	
	AN303	Panasonic	
	AN304	Panasonic	
	AN305	Panasonic	
	AN306	Panasonic	
	AN307	Panasonic	
	AN316	Panasonic	30
	AN318	Panasonic	
	AN605	Panasonic	
	TDA2700	Signetics	
	TDA2710	Signetics	
	TDA2720	Signetics	
	TDA2730	Signetics	
Watch, Analog (See also Digital CMOS Oscillators/Dividers)			
	ICM7047	Intersil	
	MC14450	Motorola	40
	MC14451	Motorola	
	μPD809	NEC America	
	CD22004	RCA	
	SY5008	Synertek	
Watch, Digital (See also Digital CMOS Oscillators/Dividers)			
	S1424A	AMI	
	S1424C	AMI	
	S1427A	AMI	
	S2732	AMI	50
	S2733	AMI	
	S10305	AMI	
	HDO4821	Harris	
	HDO4822	Harris	
	HDO4823	Harris	
	HDO4830	Harris	
	HDO4831	Harris	
	MD4111	Hitachi	
	HD4205	Hitachi	
	300	Hughes	60
	313	Hughes	
	352	Hughes	
	359	Hughes	
	367	Hughes	
	371	Hughes	
	398	Hughes	
	405	Hughes	
	5810	Intel	

(Continued)

Consumer Circuits (Cont'd)

Function	Device	Source	Line
Watch, Digital (See also Digital CMOS Oscillators/Dividers) (Cont'd.)			70
	ICM1424	Intersil	
	ICM7200	Intersil	
	ICM7202	Intersil	
	ICM7203	Intersil	
	ICM7204	Intersil	
	ICM7210	Intersil	
	ICM7214	Intersil	
	ICM7220	Intersil	
	ICM7221	Intersil	
	ICM7222	Intersil	80
	MPS7145	Micro Power	
	MPS7155	Micro Power	
	MPS7175	Micro Power	
	MC14440	Motorola	
	MC14470	Motorola	
	MC14479	Motorola	
	MC14480	Motorola	
	MC14481	Motorola	
	MCC14482	Motorola	
	MC14483	Motorola	90
	MM58104	National	
	MM58115	National	
	MM58117	National	
	MM58118	National	
	MM58119	National	
	MM58120	National	
	MM5829	National	
	MM5860	National	
	MM58601	National	
	MM5880	National	100
	MM58801	National	
	MM5882	National	
	MM5885	National	
	MM5886	National	
	MM5890	National	
	MM58127	National	
	MM58128	National	
	MM58129	National	
	MM58130	National	
	μPD810	NEC America	110
	μPD819	NEC America	
	μPD824	NEC America	
	μPD826	NEC America	
	μPD828	NEC America	
	μPD829	NEC America	
	μPD844	NEC America	
	5024	Nortec	
	5055	Nortec	
	MN6050	Panasonic	
	MN6051	Panasonic	120
	MN6052	Panasonic	
	MN6053	Panasonic	
	MN6070	Panasonic	
	MM6090	Panasonic	
	MN6091	Panasonic	
	MN6092	Panasonic	
	MS680	RTC	
	MS681	RTC	
	MS682	RTC	
	MS683	RTC	130
	CD22001	RCA	
	CD22002	RCA	
	CD22003	RCA	
	CD22005	RCA	
	CD22006	RCA	
	CD22007	RCA	
	CD22008	RCA	
	CD22009	RCA	

(Continued)

Consumer Circuits (Cont'd)

Function	Device	Source	Line
Watch, Digital (See also Digital CMOS Oscillators/Dividers) (Cont'd.)			140
	TA6656	RCA	
	TA10176	RCA	
	TA10177	RCA	
	TA10294	RCA	
	SCL5430	SSS	
	SY5001	Synertek	
	SY5002	Synertek	
	SY5007	Synertek	
Watch, Digital Calculator			
	MM58101	National	150
	MM58102	National	
Watch Message			
	325	Hughes	
	328	Hughes	
Watch, Stopwatch			
	400	Hughes	
	ICM7045	Intersil	
	ICM7205	Intersil	
	ICM7215	Intersil	
	C1200	LSI Comp	160
	MM5865	National	
	CD22007-1	RCA	
	CD22008-1	RCA	
	DF213	**Siliconix** (981)	
	DF214	**Siliconix** (981)	
	SY5009	Synertek	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Followers

Bias Current na 25°C	Offset Voltage mv 25°C	Voltage Drift µV/°C	Unity Gain Bandwidth MHz min	Slew Rate v/µs	Output v @ ma	Supply Range	Comments	Device	Source
Followers									
0.1	10	25*	100*	1000	9 @ 90	±5 to ±20	Fast Follower	LH0033	† National
	50	400	200	3000	10 @ 200	±11 to ±18	Very Fast, FET	9963	† OEI
0.15	20	25*	100*	1000	9 @ 90	±5 to ±20	Fast Follower	LH0033C	National
0.2	25	300*	200*	2000	10 @ 200	±5 to ±20	Very Fast Follower	LH0063	† National
	50	300*	200*	2000	10 @ 200	±5 to ±20	Very Fast Follower	LH0063C	National
0.2*	50	300*	300*	2000	10 @ 200	±5 to ±20	Gain 0.094 (50 ohm)	3553	† Burr-Brown
1.0	10.0	—	—	4*	12 @ 2	±5 to ±18	Follower	TCA410A	Signetics
3	4.0	6*	12*	30*	10 @ 1	±5 to ±18	Follower, replaces 102	SG210	Silicon G
			20*	30*	10 @ 1	±5 to ±18	Follower, replaces 102	LM210	AMD
								LM210	Motorola
								LM210	National
							Dual 210 Follower	LH2210	National
		10*	20*	30*	10 @ 1	±5 to ±18	Follower, replaces 102	110	† Intersil
								210	Intersil
		12*	12*	30*	10 @ 1	±5 to ±18	Follower, replaces 102	SG110	† Silicon G
			20*	30*	10 @ 1	±5 to ±18	Follower, replaces 102	LM110	† AMD
								µA110M	† Fairchild
								LM110	† Motorola
								LM110	† National
							Dual 110 Follower	LH2110	Intersil
								LH2110	† National
	10.0	—	—	4*	12 @ 2	±5 to ±18	Follower	TCA410B	Signetics
								TCA410D	Signetics
5	20.0	100	200	1000	10 @ 500	±11 to ±18	Fast, High Current	9911	† OEI
7	7.5	10*	12*	30*	10 @ 1	±5 to ±18	Follower, replaces 102	SG310	Silicon G
			20*	30*	10 @ 1	±5 to ±18	Follower, replaces 102	LM310	AMD
								µA310C	Fairchild
								310	Intersil
								LM310	Motorola
								LM310	National
							Dual 310 Follower	LH2310	Intersil
								LH2310	† National
10	5.0	6*	8*	10*	10 @ 1	±15	Follower	SG102	† Silicon G
			10*	10*	10 @ 1.25	±12 to ±18	Follower	LM102	† National
			20*	20*	10 @ 1.25	±5 to ±18	Follower	LM202	AMD
			—	—	10 @ 1.25	±15	Follower	µA102M	† Fairchild
								102	† Intersil
		12*	20*	20*	10 @ 1.25	±5 to ±18	Follower	LM102	† AMD
15	10.0	15*	8*	10*	10 @ 1	±15	Follower	SG202	Silicon G
			10*	10*	10 @ 1.25	±12 to ±18	Follower	LM202	National
			—	—	10 @ 1.25	±15	Follower	202	Intersil
20	20.0	100	60	2000	10 @ 100	±6 to ±18	Very Fast Follower	9910	† OEI
30	15.0	20*	8*	10*	10 @ 1	±15	Follower	SG302	Silicon G
			10*	10*	10 @ 1.25	±12 to ±18	Follower	LM302	National
			20*	20*	10 @ 1.25	±5 to ±18	Follower	LM302	AMD
			—	—	10 @ 1.25	±15	Follower	µA302C	Fairchild
								302	Intersil
See also Linear Amplifiers, Special Purpose Current Amplifiers									

† Military Temperature Range (−55° to 125°C) * Typical Values

LINEAR–Operational Amplifiers

General Purpose

The 101A series consists of the 101A (55°C to 125°C), the 201A (25°C to 85°C) and the 301 (0°C to 70°C). These units require an external compensation capacitor which permits the bandwidth to be optimized for particular applications.

Device	Source	
LM101A	AMD	
AD101A	AD	
µA101A	Fairchild	
101A	Intersil	
LM101A	Motorola	
LM101A	National	
CA101A	RCA	
LM101A	Raytheon	
LM101A	Signetics	
SG101A	Silicon G	
LM101A	TI	
TA7506	Toshiba	

The performance of the 741 series is similar to the 101. These units include internal compensation to make the device stable and to eliminate the need for an external capacitor.

Device	Source	
741	AMD	
AD741	AD	
µA741	Fairchild	
HA17741	Hitachi	
741	Intersil	
MC1741	Motorola	
LM741	National	
µPC741	NEC America	
SFC2741	NPC	
OP-02	**PMI**	**(839)**
PM741	**PMI**	**(839)**
SSS741	**PMI**	**(839)**
CA741	RCA	
RC741	Raytheon	
TBA221	Siemens	
SG741	Silicon G	
µA741	Signetics	
TDA0741	Signetics	
TL1741	Telefunken	
µA741	TI	
TA7504	Toshiba	

Dual Amplifiers. The 1458 (0°C to 70°C) and the 1558 (55°C to 125°C) offer approximately the same performance as the 741. Compensation is built in.

Device	Source	
1458	AMD	
XR1458	Exar	
µA1458	Fairchild	
MC1458	Motorola	
LM1458	National	
µPC1458	NEC America	
OP-14	**PMI**	**(844)**
PM1458	**PMI**	**(844)**
SSS1458	**PMI**	**(844)**
CA1458	RCA	
RC1458	Raytheon	
MC1458	Signetics	
SG1458	Silicon G	
MC1458	TI	

FET Input. Bipolar/JFET available in standard (155), wideband (156) and uncompensated (157) versions, premium performance (A and B suffixes), and various temperature ranges (155, 255, 355, etc are available.) Some versions approach the low cost of the units below.

Device	Source	
LF155	AMD	
µAF155	Fairchild	
LF155	Intersil	
LF155	Motorola	

(Continued)

General Purpose (Cont'd)

FET Input. Bipolar/JFET available in standard (155), wideband (156) and uncompensated (157) versions, premium performance (A and B suffixes), and various temperature ranges (155, 255, 355, etc are available.) Some versions approach the low cost of the units below. (Cont'd.)

Device	Source	
LF155	**National**	**(786)**
OP-15	**PMI**	**(871)**
PM155	**PMI**	**(871)**
LF155	Raytheon	
LF155	Signetics	
LF155	TI	

FET Input. The "741" of the FET input devices has yet to be established. Such a device requires very low cost, several sources, and many users. Commercial devices in the 155 series above meet some of these criteria, however, devices from the series below are generally lower in cost.

Device	Source	
µAF771	Fairchild	
LF351	**National**	**(776)**
LF13741	National	
CA3140	RCA	
CA3160	RCA	
TL081	**TI**	**(991)**

High Output Current

ma @ v	Device	Source
3000 @ 24	IH8530C	Intersil
	IH8530M	† Intersil
2000 @ 30	3572A	Burr-Brown
2000 @ 24	IH8520C	Intersil
	IH8520M	† Intersil
1100 @ 11	833-21	Beckman
	LH0021	† National
1000 @ 30	3571A	Burr-Brown
1000 @ 24	IH8510C	Intersil
	IH8510M	† Intersil
1000 @ 10	833-21C	Beckman
	LH0021C	National
500 @ 10	LH0061	† National
	LH0061C	National
200 @ 10	µA759	† Fairchild
	µA759C	Fairchild
130 @ 13	LH0041	† National
	LH0041C	National
100 @ 10	3554A	Burr-Brown
	3554B	Burr-Brown
	3554S	Burr-Brown
	LH0003	National
100 @	CA3094	RCA
75 @ 145	3583	Burr-Brown
60 @ 30	3580J	Burr-Brown
50 @ 10	1430	Teledyne P
50 @ 5	LH0005	National
	LH0005A	† National
47 @ 14	LH0020	† National
	LH0020C	National
40 @ 4	LH0005C	National
38 @ 11	CA3033A	† RCA
	CA3047A	RCA
32 @ 8	TAA851	Telefunken
	TAA865	Telefunken
30 @ 70	3581J	Burr-Brown
30 @ 10	HVA23	DDC
	HFS23	DDC

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers (Cont'd)

High Output Current (Cont'd)

ma @ v	Device	Source	Line
20 @ 12	TAA761	Siemens	
	TAA762	†Siemens	
	TAA765	Siemens	
	TCA315	Siemens	
	TCA325	Siemens	
20 @ 10	9912	†OEI	
20 @ 8	TAA861	Siemens	
	TAA862	†Siemens	10
18 @ 9	CA3033	†RCA	
15 @ 145	3582J	Burr-Brown	
	3584	Burr-Brown	
15 @ 30	LH0004C	National	
15 @ 10	**HA-2620**	**†Harris** **(692)**	
	HA2620	Intersil	20

High Speed

Unity Gain Slew Rate (v/μsec min)	Device	Source	Line
1000	AM-500	Datel	
800(g=2)	NE539	Signetics	
600	9912	†OEI	
500	1430	Teledyne P	
400	LH0024	†National	30
350	LH0032	†National	
	LH0032C	National	
300	9916	†OEI	
280	**HA-2530**	**†Harris** **(684)**	
250	**HA-2535**	**Harris** **(684)**	
	LH0024C	National	40
	1435	†Teledyne P	
250(g=5)	9906	†OEI	
200	9908	†OEI	
120	AD505J	AD	
	AD505K	AD	
	AD505S	†AD	
100(g=3)	**HA-2520**	**Harris** **(680)**	50
100	AD509K	AD	
	AD509S	†AD	
	3550K	Burr-Brown	
80	AD509J	AD	
	3507J	Burr-Brown	
	1322	†Teledyne P	
	1322-01	Teledyne P	60
65	3550J	Burr-Brown	
	3550S	†Burr-Brown	
50	LM118	†AMD	
	LM318	AMD	
	AD518	AD	
	AD518S	†AD	
	AD528	AD	
	AD528S	†AD	70
	μA118	†Fairchild	
	μA318	Fairchild	
	HA-2510	**†Harris** **(676)**	
	LH0062	†National	
	LH0062C	National	
	LM118	†National	
	LM318	National	
	SFC2118	†NPC	
	SFC2318	NPC	
	LM118	†Raytheon	80
	LM318	Raytheon	
	LM118	†TI	
	LM318	TI	

High Voltage

Maximum Supply Voltage	Device	Source	Line
450 (5v Internal Regulator)	ZN417	Ferranti	
±225 (5v Internal Regulator)	ZN417-	Ferranti	
±150	3582J	†Burr-Brown	
	3583	Burr-Brown	90
	3584	Burr-Brown	
±75	3581J	†Burr-Brown	
±40	3571A	†Burr-Brown	
	3572A	†Burr-Brown	
	AM-464-2	Datel	
	AM-464-2M	†Datel	
	HA-2640	**†Harris** **(700)**	
	HA-2645	**Harris** **(700)**	100
	MC1536	†Motorola	
	LH0004	†National	
	LH0004C	National	
	LM143	†National	
	LM243	National	
	LM144	†National	
	SG1536	Silicon G	
	1332	Teledyne P	
±35	3580J	Burr-Brown	110
±34	MC1436	Motorola	
	LM344	National	
	SG1436	Silicon G	
±30	IH8510C	Intersil	
	IH8510M	†Intersil	
	IH8520C	Intersil	
	IH8520M	†Intersil	
	IH8530C	Intersil	120
	IH8530M	†Intersil	
	MC1436C	Motorola	
	LM343	National	
	SG1436C	Silicon G	

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers (Cont'd)

Low Bias Current

Rated values do not usually include thermal rise due to circuit operation.

Current pa 25°C	Device	Source	Line
0.01	ICH8500A	Intersil	
0.075	AD515L	AD	
0.1	3523L	Burr-Brown	
	ICH8500	Intersil	
0.15	AD515K	AD	10
0.25	3523K	Burr-Brown	
0.3	AD515J	AD	
0.5	3523J	Burr-Brown	
1.0	AD523J	AD	
	3522L	Burr-Brown	20
	8007AC	Intersil	
	8007AM	† Intersil	
	LH0052	† National	
	1439	Teledyne P	
2.0	3527B	Burr-Brown	
5.0	ADM501C	AD	
	AD506L	AD	
	AD523K	AD	30
	3522K	Burr-Brown	
	3522S	Burr-Brown	
	3527A	Burr-Brown	
	3527C	Burr-Brown	
	LH0052C	National	
	CA3080	RCA	
	CA3080A	† RCA	
	1425-01	Teledyne P	
	1425-02	Teledyne P	

Low Drift

Voltage Drift (μv/°C Max)	Device	Source		Line
0.1	AM-490-2C	Datel		40
0.3	AM-490-2B	Datel		
	HA-2904	**Harris**	(724)	
0.5	AD504M	AD		
	3570C	Burr-Brown		
	LH0044A	† National		
	LH0044AC	National		
	LH0044B	National		50
	OP-05A	**PMI**	(849)	
0.6	SSS725A	† AMD		
	μA714A	† Fairchild		
	HA-2900	**† Harris**	(724)	
	OP-05E	PMI		
	OP-07A	**† PMI**	(853)	
	SSS725A	† PMI		
	SSS725E	PMI		
1.0	AD504S	† AD		60
	3500E	Burr-Brown		
	3510B	Burr-Brown		
	3510S	† Burr-Brown		
	3521L	Burr-Brown		
	AM-490-2A	Datel		
	μA714	**† Fairchild**	(627)	
	μA714E	Fairchild		
	μA725A	† Fairchild		
	μA725E	Fairchild		70
	LH0044	† National		
	LH0044C	National		
	LM725A	National		
	SSS725	**† PMI**	(849)	
	SSS725B	PMI		
	OP-05	**† PMI**	(849)	
1.0 (Dual Unit)	**OP-10**	**† PMI**	(857)	
	OP-10A	† PMI		
	OP-10E	PMI		80
1.3	**OP-07**	**† PMI**	(853)	
	OP-07E	**PMI**	(853)	
1.5	3510A	Burr-Brown		
	μA714C	Fairchild		
	OP-05C	PMI		
	SSS725C	PMI		
1.5 (Dual Unit)	OP-10C	PMI		90
1.6	**OP-07C**	**PMI**	(853)	
2.0	3527C	Burr-Brown		

Low Power

Supply Current μa @ ±15v	Device	Source		Line
Programmable				
The current drain limits of these units are approximately 10 300 μa.				
	μA776	† Fairchild		
	μA776C	Fairchild		
	HA-2720	**Harris**	(712)	100
	HA-2725	**Harris**	(712)	
	4250	† Intersil		
	4250C	Intersil		
	8021C	Intersil		
	8021M	† Intersil		
	MC1776	† Motorola		
	MC1776C	Motorola		
	MC3476	Motorola		
	LM4250	† National		
	LM4250C	National		110
	CA3078	† RCA		
	CA3078A	† RCA		
	CA3094	† RCA		
	CA3094A	† RCA		
	CA3094B	† RCA		
	CA6078AT	† RCA		
	SG1250	† Silicon G		
	SG2250	Silicon G		
	SG3250	Silicon G		
	SG4250	† Silicon G		120
	SG4250C	Silicon G		
	UC4250	† Solitron		
	UC4250C	Solitron		
Non Adjustable				
125	LH0001	National		
150	**HA-2700**	**Harris**	(708)	
	HA-2704	**Harris**	(708)	
	HA-2705	**Harris**	(708)	130
200	**TL061**	**TI**	(985)	
See TL061 series				
600	AD108	† AD		
	LM108	† AMD		
	LM112	† AMD		
	LM212	AMD		
	μA108	† Fairchild		
	108	† Intersil		140
	LM108	† Motorola		
	LM108	† National		
	LM112	† National		
	LM212	National		
	LM216A	National		
	LM316A	National		
	SFC2108	NPC		
	OP-08	**† PMI**	(858)	
	OP-12	**† PMI**	(858)	
	PM108	**† PMI**	(858)	150
	LM108	Raytheon		
	CA108	† RCA		
	LM108	† Signetics		
	SG108	Silicon G		

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers (Cont'd)

Programmable

Function	Device	Source		Line
Adjustable Current/Performance				
Single (1 unit per package)				
	μA776C	Fairchild		
	μA776M	† Fairchild		
	HA-2720	**† Harris**	**(712)**	
	HA-2725	**Harris**	**(712)**	
	4250	Intersil		
	4250C	Intersil		
	8021C	Intersil		
	8021M	† Intersil		10
	MC1776	† Motorola		
	MC1776C	Motorola		
	MC3476	Motorola		
	LM4250	† National		
	LM4250C	National		
	CA3078	RCA		
	CA3078A	† RCA		
	CA3080	RCA		
	CA3080A	† RCA		
	CA3094	† RCA		20
	CA3094A	† RCA		
	CA3094B	† RCA		
	SG1250	† Silicon G		
	SG2250	Silicon G		
	SG3250	Silicon G		
	SG4250	† Silicon G		
	SG4250C	Silicon G		
	TL066	**TI**	**(985)**	
Dual (2 units per package)				
	HA-2730	**† Harris**	**(718)**	30
	HA-2735	**Harris**	**(718)**	
	8022C	Intersil		
	8022M	† Intersil		
	LH24250	† National		
	LH24250C	National		
Triple (3 units per package)				
	8023C	Intersil		
	8023M	† Intersil		
	CA3060	RCA		
	CA3060	† RCA		40
	CA3060A	RCA		
	CA3060B	RCA		
	L144A	**† Siliconix**	**(982)**	
	L144B	**Siliconix**	**(982)**	
	L144C	**Siliconix**	**(982)**	
	SL144	Siltronics		
Quad (4 units per package)				
	XR146	† Exar		
	XR246	Exar		
	XR346	Exar		50
	XR4202	Exar		
	XR4202M	† Exar		
	LM146	**† National**	**(766)**	
	LM246	**National**	**(766)**	
	LM346	**National**	**(766)**	

Single Supply

Supply Voltage	Device	Source	Line
Single (1 unit per package)			
5 to 16			
	CA3130	† RCA	
	CA3130A	† RCA	
	CA3130B	† RCA	60
to 24			
	CA3094	† RCA	
to 36			
	μA759	† Fairchild	
	μA759C	Fairchild	
	CA3140	Intersil	
	CA3140	RCA	
	CA3094A	† RCA	
to 44			
	CA3140B	† Intersil	70
	CA3140B	† RCA	
	CA3094B	† RCA	
Dual (2 units per package)			
10 to 16			
	DA-101	Delco	
3 to 26			
	LM2904	National	
	LM2904	TI	
3 to 30			
	LM158	† Motorola	80
	LM258	Motorola	
	LM358	Motorola	
	LM158	† National	
	LM258	National	
	LM358	National	
	LM158A	† National	
	LM258A	National	
	LM358A	National	
	LM158	† Signetics	
	LM258	Signetics	90
	LM358	Signetics	
	NE532	† Signetics	
	SA532	Signetics	
	SE532	Signetics	
	LM158	† TI	
	LM258	TI	
	LM358	TI	
3 to 36			
	μA798	Fairchild	
	MC3458	Motorola	100
8 to 36			
	TBA231	SGS	
Quad (4 units per package)			
4 to 18			
	μA3401C	Fairchild	
	LM3401	National	
	MC3401	Motorola	
	CA3401	† RCA	
	RC3401	Raytheon	
3 to 26			110
	LM2902	Motorola	
	LM2902	National	
4 to 28			
	μA3301C	Fairchild	
	MC3301	Motorola	
	LM3301	National	
	RC3301	Raytheon	
3 to 30			
	LM124	† AMD	

(Continued)

Single Supply (Cont'd)

Supply Voltage	Device	Source	Line
3 to 30 (Cont'd.)			
	LM224	AMD	120
	LM324	AMD	
	μA124	† Fairchild	
	μA224	Fairchild	
	μA324	Fairchild	
	LM124	† Intersil	
	LM224	Intersil	
	LM324	Intersil	
	LM324	Motorola	
	LM124	† National	130
	LM224	National	
	LM324	National	
	μPC224	NEC America	
	μPC324	NEC America	
	CA124	† RCA	
	CA224	RCA	
	CA324	RCA	
	LM124	† Raytheon	
	LM224	Raytheon	
	LM324	Raytheon	140
	LM124	† Signetics	
	LM224	Signetics	
	LM324	Signetics	
	SA534	Signetics	
	SG124	† Silicon G	
	SG224	Silicon G	
	SG324	Silicon G	
	LM124	† TI	
	LM224	TI	
	LM324	TI	150
	TL321C	TI	
	TL321M	† TI	
3 to 32			
	LM2902	Motorola	
	LM2902	Raytheon	
	RC4137	Raytheon	
	RM4137	† Raytheon	
	RV4137	Raytheon	
4 to 32			
	LM2900	National	160
	LM3900	National	
3 to 36			
	XR3303	Exar	
	XR3403	Exar	
	XR3503M	† Exar	
	μA3303C	Fairchild	
	μA3403C	Fairchild	
	μA3503M	† Fairchild	
	MC3303	Motorola	
	MC3403	Motorola	170
	MC3503	† Motorola	
	RC3403	Raytheon	
	RM3503	† Raytheon	
	RV3403	Raytheon	
4 to 36			
	LM1900	National	
	LM2900	Raytheon	
	LM3900	Raytheon	

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers (Cont'd)

Wide Band

Unity Gain Bandwidth MHz	Device	Source	Line
500*			
	1435	† Teledyne P	
200			
	9916	† OEI	
100			
	AM-500	Datel	
	HVA23	DDC	
	9908	† OEI	
80			
	HFS23	DDC	10
70*			
	3554A	Burr-Brown	
	3554B	Burr-Brown	
	3554S	† Burr-Brown	
	LH0024	† National	
	LH0024C	National	
	LH0032	† National	
	LH0032C	National	
65*			
	μA715C	Fairchild	20
	μA715M	† Fairchild	
60*			
	9912	† OEI	
	1430	Teledyne P	
50*			
	3551J	Burr-Brown	
	3551S	† Burr-Brown	
	CA3015	† RCA	
	CA3015A	† RCA	
	CA3016	† RCA	30
	CA3016A	† RCA	
	CA3030	RCA	
	CA3030A	RCA	
	CA3038	† RCA	
	CA3038A	† RCA	
38*			
	CA3100	† RCA	
35*			
	AD507J	AD	
	AD507K	AD	40
	AD507S	† AD	
30*			
	μA702C	Fairchild	
	μA702M	† Fairchild	
	MC1712	Motorola	
	LH0003	† National	
	LH0003C	National	
	LH0005	† National	
	LH0005A	National	
	LH0005C	† National	50
	μPC51A	NEC America	
	μPC702	NEC America	
	SL702C	Plessey	
	RC702	Raytheon	
	RM702	† Raytheon	
	TL702M	† TI	
	TL702C	TI	
	μA702M	† TI	

Unity Gain Bandwidth MHz	Device	Source	Line

Unity Gain Bandwidth MHz	Device	Source	Line

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics

Single Units

In this list the "Comp." column indicates the number of compensation components required at unity gain. Thus 0 indicates a fully compensated amplifier. The bandwidth and slew rate are listed with the amplifier compensated for unity gain.

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
0.020*	0.15*	0.05*	0.1	3*	2.5*	1M	120	3	Chopper Stabilized	AM-490-2C	Datel
			0.3	3*	2.5*	1M	120	3	Chopper Stabilized	AM-490-2B	Datel
			0.6	3*	2.5*	1M	120	3	Chopper Stabilized	AM-490-2M	†Datel
			1.0	3*	2.5*	1M	120	3	Chopper Stabilized	AM-490-2A	Datel
0.025	2	2	0.6	1.2*	0.25*	300K	110	0	Ultra Low Offset Voltage. Low Drift	µA714A **OP-07A**	†Fairchild **†PMI (853)**
	10	2.5	2	0.3*	0.1*	1M	110	0	Trimmed Offset	AD510L AD510S	AD †AD
	15	2.5	0.5	0.4*	0.06*	1M	120	1	Precision, Low Noise	LH0044A LH0044AC	†National National
0.05	0.050	0.0005*	75*	1*	6*	20K	70	0	FET	3540J	†Burr-Brown
	0.5	0.3	0.2*	3*	10*	100K	80	3	Chopper Stabilized	TL089I	TI
	1	0.5	0.4	3*	2.5*	10M	130	3	Chopper Stabilized	**HA-2904**	**Harris (724)**
	13	4.0	1	0.3	0.1*	1M	110	0	Trimmed Offset	AD510K	AD
	30	5	0.5	0.4*	0.06*	500K	114	1	Precision, Low Noise	LH0044B	National
			1	0.4*	0.06*	500K	114	1	Precision, Low Noise	LH0044	†National
0.06	1	0.5	0.6	3*	2.5*	1M	120	3	Chopper Stabilized	**HA-2900**	**†Harris (724)**
	15	10	0.5	0.4*	0.5	1M	110	1	Low Drift	3510C	Burr-Brown
0.075	3	2.8	1.3	1.2*	0.25*	200K	110	0	Ultra Low Offset Voltage, Low Drift	**µA714** **OP-07**	**†Fairchild (627)** **†PMI (853)**
	4	3.8	1.3	1.2*	0.25*	200K	106	0	Ultra Low Offset Voltage, Low Drift	µA714E	Fairchild
0.12	25	15	1	0.4*	0.5	1M	110	1	Low Drift	3510B 3510S **OP-07E**	Burr-Brown †Burr-Brown **PMI (853)**
0.08	1	0.5	0.2*	3*	2.5*	1M	120	3	Chopper Stablilized	AM-490 **HA-2905** 1340	Datel **Harris (724)** Teledyne P
0.10	10	5	0.5	0.3*	0.1*	1-1000	80	0	Instrumentation	AD522C	AD
	25	5	3	3*	0.1*	250K	94	0	Trimmed Offset	AD510J	AD
	35	5	1	0.4*	0.06*	500K	114	1	Precision, Low Noise	LH0044C	National
	70	1	0.6	—	—	1M	120	4	Instrumentation	SSS725A	†PMI
			0.8	—	—	1M	120	4	High Performance 725	SSS725A	†AMD
0.15	1	0.6	0.2*	3*	10*	100K	100	3	Chopper Stabilized	TL089C	TI
	2	0.2	2.5	0.8*	0.12*	80K	104	0	Improved 108A, low bias, compensated	 **OP-12A** **OP-12E**	 **†PMI (858)** **PMI (858)**
								1	Improved 108A, low bias	**OP-08A** **OP-08E**	**†PMI (858)** **PMI (858)**
		2	0.9	1.2*	0.25*	300K	114	0	Instrumentation	OP-05A	†PMI
	7	6	1.8	1.2*	0.25*	120K	100	0	Ultra Low Offset Voltage, Low Drift	µA714C **OP-07C**	Fairchild **PMI (853)**
	12	6	2.5	1.2*	0.25*	120K	94	0	Ultra Low Offset, Low Drift	**OP-07D**	**PMI (853)**
	35	20	2	0.4*	0.5	1M	110	1	Low Drift	3510A	Burr-Brown
0.20	15	10	2	0.3*	0.1*	1-1000	80	0	Instrumentation	AD522B	AD
	25	20	6	0.3*	0.1*	1-1000	75	0	Instrumentation	AD522S	†AD
0.25	0.002	0.0003*	5	1*	0.6	100K	76*	0	Low Drift FET	3527B	Burr-Brown
	0.005	0.0003*	2	1*	0.6	100K	76*	0	Ultra Low Drift FET	3527C	Burr-Brown
	0.010	0.002*	1	1.5*	0.6	100K	90*	0	Ultra Low Drift FET	3521L	Burr-Brown
	0.015	0.002*	2	1.5*	0.6	100K	90*	0	Ultra Low Drift FET	3521K	Burr-Brown
	0.020	0.020*	5	1.5*	0.6	50K	90*	0	Ultra Low Drift FET	3521J	Burr-Brown

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
0.25	0.020	0.020*	5	1.5*	0.6	50K	90*	0	Ultra Low Drift FET	(Cont'd.) 3521R	† Burr-Brown
0.30	2	0.2	3.5	0.8*	0.12*	80K	104	0	Improved 108A, low power, compensated	**OP-12B**	**† PMI (858)**
										OP-12F	**PMI (858)**
								1	Improved 108A, low power	**OP-08B**	**† PMI (858)**
										OP-08F	**PMI (858)**
0.40	25	20	6	0.3*	0.1*	1-1000	75	0	Instrumentation	AD522A	AD
0.5	0.0001	0.00005	25	1*	0.6	100K	80*	0	Ultra Low Bias FET	3523L	Burr-Brown
	0.00025	0.0001	25	1*	0.6	100K	80*	0	Ultra Low Bias FET	3523K	Burr-Brown
	0.001	0.0001	5	1*	1.5	100K	80	0	Precision FET	LH0052	† National
	0.005	0.001*	25	1*	0.6	50K	90*	0	Low Offset FET	3522K	Burr-Brown
										3522S	Burr-Brown
		0.0003*	10	1*	0.6	100K	76*	0	Low Drift FET	3527A	Burr-Brown
	0.020	0.002*	10	1.5*	0.6	50K	90*	0	Ultra Low Drift FET	3521H	Burr-Brown
	0.050	0.01	5	2.5*	3	50K	95	0	Precision Bipolar JFET	**LFT155**	**† National (800)**
										LFT355	**National (800)**
				4	10	50K	95	0	Precision Wideband JFET	**LFT156**	**† National (800)**
										LFT356	**National (800)**
				14*	10	100K	86	0	Bipolar-JFET, bias comp.	**OP-15A**	**† PMI (871)**
										OP-15E	**PMI (871)**
				19*	18	100K	86	0	Wideband-JFET, bias comp.	**OP-16A**	**† PMI (877)**
										OP-16E	**PMI (877)**
				—	—	100K	86	—	Wideband, Decompensated, Settles to 0.01% in 1.5 µs	**OP-17A**	**† PMI (882)**
										OP-17E	**PMI (882)**
	2	0.2	5	1*	0.3*	80K	96	1	Precision Bipolar, Low Bias	LM108A	† AMD
										LM208A	AMD
										AD108A	† AD
										AD208A	AD
										µA108AM	† Fairchild
										µA208AM	Fairchild
										108A	† Intersil
										208A	Intersil
										LM108A	† Motorola
										LM208A	Motorola
										LM108A	† National
										LM208A	National
										SFC2108A	† NPC
										SFC2208A	NPC
										PM108A	**† PMI (858)**
										PM208A	PMI
										LM108A	† Raytheon
										LM208A	† Raytheon
										CA108A	† RCA
										CA208A	RCA
										LM108A	† Signetics
										LM208A	Signetics
										SG108A	† Silicon G
										SG208A	Silicon G
				0.3*	0.1	80K	96	0	Compensated 108A	SG1118A	† Silicon G
										SG2118A	Silicon G
	3	2.8	2	1.2*	0.25*	200K	114	0	Instrumentation	**OP-05**	**† PMI (849)**
	4	3.8	2	1.2*	0.25*	200K	110	0	Instrumentation	OP-05E	PMI
	7	1	5	1*	0.3*	80K	96	1	Precision Bipolar	LM308A	AMD
										AD308A	AD
										µA308AC	Fairchild
										308A	Intersil

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
0.5	7	1	5	1*	0.3*	80K	96	1	Precision Bipolar	(Cont'd.)	
										LM308A	Motorola
										LM308A	National
										PM308A	PMI
										CA308A	RCA
										LM308A	Raytheon
										LM308A	Signetics
										SG308A	Silicon G
				0.3*	0.1	80K	96	0	Compensated 308A	SG3118A	Silicon G
	30	5	5	1*	0.25*	80K	90	1	General Purpose	AD301AL	AD
	35	2	8	0.8	0.25	100K	90	0	General Purpose	**OP-02A**	**†PMI (839)**
										OP-02E	**PMI (839)**
	50	5	5	1*	0.5*	50K	90	0	Higher Accuracy 741	AD741L	AD
		30	1	1.5*	0.8	100K*	100*	0	Low Drift	3500E	Burr-Brown
	75	5	2	1	0.005*	1000K	110	4	High Accuracy Instrumentation	µA725AM	† Fairchild
	80	5	0.6	—	—	1000K	120	4	Instrumentation	SSS725E	PMI
			1	—	—	1000K	120	4	Instrumentation	**SSS725**	**PMI (849)**
	500	200	15	0.3	—	—	72	0	Instrumentation	HC3020	HyComp
0.7	30	2	5	2.5*	18*	50K	90	0	High Speed	**OP-01**	**†PMI (837)**
										OP-01H	**PMI (837)**
0.75	80	5	1	—	—	1000K	110	4	Instrumentation	SSS725B	PMI
			2.8*	—	—	1000K	110	4	High Performance 725	SSS725B	AMD
			—	1*	0.3*	50K	80	0	High Performance	µA741AM	† Fairchild
				0.44	0.3	50K	80	0	High Performance	µA741EC	Fairchild
1.0	0.000075	—	25	0.35	0.3	50K	70	0	FET Electrometer	AD515L	AD
	0.00015	—	15	0.35	0.3	100K	80	0	FET Electrometer	AD515K	AD
	0.0005	0.0002	50	1*	0.6	100K	80*	0	Ultra Low Bias FET	3523J	Burr-Brown
	0.005	0.0002	10	1*	1	75K	76	0	Precision FET	LH0052C	National
		0.002	25	4*	3	25K	80*	0	General Purpose FET	ADM501C	AD
				1	3	50K	70		Low Bias Current, FET	1425-01	Teledyne P
		0.002*	10	1	3	50K	70	0	Low Bias Current, FET	1425-02	Teledyne P
		—	10	1*	3	75K	80	0	High Accuracy, FET	AD506L	AD
	0.010	0.002*	50	1*	0.6	50K	90*	0	Low Offset FET	3522J	Burr-Brown
		0.005*	25	1	3	50K	70		Low Drift, FET	1426-01	Teledyne P
				10*	65	25K	70*	0	Fast Settling, 1 µs to 0.01%	3550J	Burr-Brown
										3550S	† Burr-Brown
				20*	100	25K	70*	0	Fast Settling, 0.6 µs to 0.01%	3550K	Burr-Brown
		—	25	4*	3	25K	80*	0	General Purpose FET	ADM501B	AD
	0.015	—	25	10*	50	50K	80	0	Fast Wideband, High Accuracy	AD528K	AD
										AD528S	† AD
	0.025	0.01*	5	1	3	50K	70	0	Low Drift, FET	1426-03	Teledyne P
			10	1	3	50K	70	0	Low Drift, FET	1426-02	Teledyne P
	0.050	0.01	15	70	1000	100K	44	1	150ns Settling to 0.05%	3554B	Burr-Brown
			25	70	1000	100K	44	1	150ns settling to 0.05%	3554S	† Burr-Brown
	0.10	0.01	50	50*	250*	100K	70*	1	Wideband, Fast Settling	3551J	Burr-Brown
										3551S	† Burr-Brown
		0.02	10	13*	7.5	75K	86	0	Bipolar-JFET, bias comp.	**OP-15B**	**†PMI (871)**
										OP-15F	**PMI (871)**
				18*	12	75K	86	0	Wideband-JFET, bias comp.	**OP-16B**	**†PMI (877)**
										OP-16F	**PMI (877)**
				—	35	75K	86	—	Wideband, Decompensated, Settles to 0.01% in 1.5 µs	**OP-17B**	**†PMI (882)**

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
1.0	0.10	0.02	10	—	35	75K	86	—	Wideband, Decompensated, Settles to 0.01% in 1.5 µs	(Cont'd.) **OP-17F**	**PMI (882)**
	5	0.5	10	0.8*	0.12*	40K	84	0	Precision, low input current	**OP-12C**	**† PMI (858)**
										OP-12G	**PMI (858)**
								1	Precision, low input current	**OP-08C**	**† PMI (858)**
										OP-08G	**PMI (858)**
		7*	3	1.5*	1	45K	100*	0	Low Bias, Low Noise	3500C	Burr-Brown
			5	1.5*	1	45K	100*	0	Low Bias, Low Noise	3500T	† Burr-Brown
		7	—	—	1.5*	50K	—	0	Low Input Bias, High Slew Rate	ULS-2171	† Sprague
	100	20	4*	1*	0.25*	25K	70	2	General Purpose, Low Quiescent Power		
										LH0001	† National
						30K	70	2	High Voltage	LH0004	† National
			5	1*	0.005*	1000K	110	4	High Accuracy Instrumentation	µA725M	† Fairchild
										LM725	† National
				0.5*	0.01*	1000K	110	4	Instrumentation	RM725	† Raytheon
				—	—	1000K	110	4	Instrumentation	725	† AMD
										µPC154	NEC America
										PM725	**† PMI (849)**
	200	50	6	1*	0.4*	25K	80	3	General Purpose	RM709A	† Raytheon
1.3	7	6	4.5	1.2*	0.25*	120K	100	0	Instrumentation	OP-05C	PMI
	110	13	4.5	—	—	500K	100	4	Instrumentation	SSS725C	PMI
1.5	0.010	—	25	1*	3	50K	80	0	High Accuracy, FET	AD506K	AD
			50	1*	3	50K	80	0	High Accuracy, FET	AD506S	† AD
	0.020	—	25	1*	50*	50K	80	1-3	High Speed, Laser Trim	AD516K	AD
			50	1*	50*	50K	80	1-3	High Speed, Laser Trim	AD516S	† AD
	80	5	2	—	—	1000K	120	4	High Performance 725	SSS725	† AMD
				0.5*	0.005*	1000K	120	4	Instrumentation	LM725A	† National
			2*	—	—	1000K	120	4	High Performance 725	SSS725E	AMD
		10	0.5	0.3*	0.12*	1000K	110	1	Low Drift, Low Noise	AD504M	AD
			1	0.3*	0.12*	1000K	110	1	Low Drift, Low Noise	AD504L	AD
										AD504S	† AD
	100	15	3	0.3*	0.12*	500K	100	1	Low Drift, Low Noise	AD504K	AD
	120	45	4*	1*	0.25*	30K	70	2	High Voltage	LH0004C	National
2.0	0.010	0.0005*	5	1*	3	50K	70	0	Low Offset Voltage, FET	8007C-1	Intersil
			15	1*	3	50K	70	0	Low Offset Voltage, FET	8007C-2	Intersil
										8007M-2	† Intersil
		0.005*	50	1	3	50K	70	—	Low Bias Current, FET	1425	Teledyne P
		—	75	4*	3	25K	80*	0	General Purpose FET	ADM501A	AD
	0.020	0.010	15	4*	10*	50K	86	1	MOS FET, Single Supply, Strobe	CA3130B	† RCA
						100K	86	0	MOS FET Single Supply, Strobe	CA3160B	† RCA
	0.025	0.01*	50	1	3	100K	72		Low Drift, FET	1426	Teledyne P
	0.030	0.01	5*	4.5*	9*	50K	86	0	MOS FET, Single Supply	CA3140B	† Intersil
										CA3140B	† RCA
	0.050	0.01	5	2.5*	3	50K	85	0	Bipolar - JFET	LF155A	† AMD
										LF355A	AMD
										µAF155A	† Fairchild
										µAF355A	Fairchild
										LF155A	† Intersil
										LF355A	Intersil

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
2.0	0.050	0.01	5	2.5*	3	50K	85	0	Bipolar - JFET	(Cont'd.)	
										LF155A	† Motorola
										LF355A	Motorola
										PM155A	**† PMI (871)**
										PM355A	**PMI (871)**
										LF155A	**† National (786)**
										LF355A	**National (786)**
										LF155A	† Raytheon
										LF355A	Raytheon
										LF155A	† Signetics
										LF355A	Signetics
										LF155A	† TI
										LF355A	TI
				4	10	50K	85	0	Wideband - JFET	LF156A	† AMD
										LF356A	AMD
										µAF156A	† Fairchild
										µAF356A	Fairchild
										LF156A	Intersil
										LF356A	Intersil
										LF156A	† Motorola
										LF356A	Motorola
										LF156A	**† National (786)**
										LF356A	**National (786)**
										PM156A	**† PMI (877)**
										PM356A	**PMI (877)**
										LF156A	† Raytheon
										LF356A	Raytheon
										LF156A	† Signetics
										LF356A	Signetics
										LF156A	† TI
										LF356A	TI
				—	40	50K	85	—	Wideband Decompensated	LF157A	† AMD
										LF357A	AMD
										µAF157A	† Fairchild
										µAF357A	Fairchild
										LF157A	† Intersil
										LF357A	Intersil
										LF157A	† Motorola
										LF357A	Motorola
										LF157A	**† National (786)**
										LF357A	**National (786)**
										PM157A	**† PMI (882)**
										PM357A	**PMI (882)**
										LF157A	† Raytheon
										LF357A	Raytheon
										LF157A	† Signetics
										LF357A	Signetics
										LF157A	† TI
										LF357A	TI
			50	70	1000	100K	44	1	150ns Settling to 0.05%	3554A	Burr-Brown
	0.10	0.05	10*	4*	13*	50K	80	0	Wideband Bipolar JFET	**LF351A**	**National (776)**
		0.05*	40	0.5*	3	50K	80	1	High Current, High Power	3571A	Burr-Brown
										3572A	Burr-Brown
	0.50	—	75	60*	500	200K	—	0	Inverting, Settles to 0.01% in 200 ns	1430	Teledyne P
	2	0.2	15	1*	0.2*	50K	85	0	Micropower, Supply Current 600 µa	LM112	† AMD
										LM212	AMD
										LM112	† National
										LM212	National
					0.1*	50K	85	0	Compensated 108/208	SG1118	† Silicon G
										SG2118	Silicon G
					0.3*	50K	85	1	Precision Bipolar	LM108	† AMD
										LM208	AMD
										AD108	† AD
										AD208	AD

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
2.0	2	0.2	15	1*	0.3*	50K	85	1	Precision Bipolar	(Cont'd.)	
										µA108M	† Fairchild
										µA208M	Fairchild
										108	† Intersil
										208	Intersil
										LM108	† Motorola
										LM208	Motorola
										LM108	† National
										LM208	National
										SFC2108	† NPC
										SFC2208	NPC
										PM108	**† PMI (858)**
										PM208	PMI
										LM108	† Raytheon
										LM208	Raytheon
										CA108	† RCA
										CA208	RCA
										LM108	† Signetics
										LM208	Signetics
										SG108	† Silicon G
										SG208	Silicon G
				0.3*	0.3*	50K	85	1	Low Noise 108	108LN	† Intersil
	3	2	10	0.5*	0.1	45K	100*	0	Low Bias Current	3501C	Burr-Brown
	5	0.5	10	—	1.7*	2.5K	80	3	Wideband	µA702M	† TI
	7	3	10	0.5*	0.1	45K	100*	0	Low Bias Current	3501B	Burr-Brown
										3501S	† Burr-Brown
	15	5	3	3	1.5	40K	80	0	High Performance, High Gain	MC1556	† Motorola
										RM1556A	† Raytheon
	20	10*	5	1.5*	1	45K	100*	0	Low Bias, Low Noise	3500B	Burr-Brown
			10	1.5*	1	45K	100*	0	Low Bias, Low Noise	3500S	† Burr-Brown
	25	3	15	0.5	0.5*	50K	80	1	Low Offset Current	µA777M	† Fairchild
										SG777	† Silicon G
										µA777M	† TI
	50	5	8	2.5*	18*	50K	80	0	High Speed	**OP-01E**	**PMI (837)**
										OP-01F	**† PMI (837)**
			10	0.8	0.25	50K	90	0	General Purpose	**OP-02**	**† PMI (839)**
										OP-02C	**PMI (839)**
			15	1*	0.4	50K	80	0	High Performance, Low Drift	1319-01	† Teledyne P
			—	—	—	100K	80	0	High Performance 741	SSS741	† AMD
										SSS741	**† PMI (839)**
					0.6*	50K	—	0	General Purpose	ULS-2151	† Sprague
		10	15	4*	1.5	25K	80	0	High Performance, High Gain	RM4131	† Raytheon
		50	25	1*	0.4	50K	80	0	High Performance, Low Drift	1319	Teledyne P
	60	10	15	—	10	50K	70	0	High Slew Rate	SE535	† Signetics
					40	50K	70	1	60V/µs Comp. for g=5	SE538	† Signetics
	75	10	15	1*	0.5*	50K	80	0	General Purpose, Compensated	LM107	† AMD
										LM207	AMD
										µA107M	† Fairchild
										µA207M	Fairchild
										107	† Intersil
										207	Intersil
										LM107	† Motorola
										LM207	Motorola
										LM107	† National
										LM207	National
										SFC2107	† NPC
										SFC2207	NPC
										LM107	† Raytheon
										LM207	Raytheon
										CA107	† RCA

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
2.0	75	10	15	1*	0.5*	50K	80	0	General Purpose, Compensated	(Cont'd.)	
										CA207	RCA
										LM107	† Signetics
										LM207	Signetics
										SG107	† Silicon G
										SG207	Silicon G
										LM107	† TI
										LM207	TI
									Higher Accuracy 741	AD741S	† AD
							90	0	Higher Accuracy 741C	AD741K	AD
							80	1	General Purpose, Improved 101, Uncompensated		
										AD101A	† AD
										AD201A	AD
										LM101A	† AMD
										LM201A	AMD
										µA101AM	† Fairchild
										µA201AM	Fairchild
										101A	† Intersil
										201A	Intersil
										LM101A	† Motorola
										LM201A	Motorola
										LM101A	† National
										LM201A	National
										LM101A	† Raytheon
										LM201A	Raytheon
										CA101A	† RCA
										CA201A	RCA
										LM101A	† Signetics
										LM201A	Signetics
										SG101A	† Silicon G
										SG201A	Silicon G
										LM101A	† TI
										LM201A	TI
				0.8*	0.5*	50K	80	1	Low Noise 101A	101ALN	† Intersil
		30	—	—	1	50K	70	0	Improved 307	844C	Teledyne S
								1	Improved 301A	846C	Teledyne S
		—	15*	4*	120	100K	—	0	High Speed Inverting	AD505J	AD
	200	50	10	5*	0.3*	25K	80	3	General Purpose	µA709AM	† Fairchild
										MC1709A	† Motorola
										LM709A	† National
										SFC2709A	† NPC
										µA709A	† Signetics
										µA709AM	† TI
	800	200	—	10*	6*	50K	80	1	Wideband, low noise	SE5534	† Signetics
										SE5334A	† Signetics
	4000	1500	1.2*	15*	3*	0.7K	70	1	6 Volt, Wideband	CA3008A	RCA
										CA3010A	† RCA
										CA3029A	RCA
										CA3037A	† RCA
	5000	500	2.5*	7*	1.5*	2.5K	80	2	Wideband	MC1712	† Motorola
			10	30*	3.5*	2.5K	80	3	Wideband	µA702M	† Fairchild
										RM702	† Raytheon
										µA702M	† TI
	6000	1600	1.2*	50*	7*	2K	80	1	12 Volt, Wideband	CA3015A	† RCA
										CA3016A	† RCA
										CA3030A	RCA
										CA3038A	† RCA
2.5	25	5	3	0.3*	0.12*	250K	94	1	Chopperless, Low Drift	AD508J	AD
		—	15*	4*	120	200K	—	0	High Speed Inverting	AD505K	AD
										AD505S	† AD

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
2.5	(Cont'd.)										
	100	20	3*	1*	0.25*	25K	70	2	Micropower, High Performance	LH0001A	† National
	125	35	2*	1*	0.005*	250K	94	4	High Accuracy Instrumentation	725C	AMD
										µA725C	Fairchild
										LM725C	National
										µPC725	NEC America
										PM725C	PMI
										RC725	Raytheon
			3	—	—	250K	96	4	725 type	µPC154A	NEC America
	200	40	5	0.3*	0.12*	250K	94	1	Low Drift, Low Noise	AD504J	AD
	250	50	10*	1*	0.25*	100K	90	2	High Gain Instrumentation, 50 ma	LH0020	† National
3.0	0.0003	—	50	0.35	0.3	40K	66	0	FET Electrometer	AD515J	AD
	0.020	0.020*	25	5	20*	50K	110*	0	High Voltage FET	3581J	Burr-Brown
				3*	20*	100K	110*	0	High Voltage FET	3582J	Burr-Brown
				5*	20*	400K	110*	0	High Voltage FET	3583	Burr-Brown
				7*	—	1000K	110*	2	High Voltage FET	3584	Burr-Brown
	0.030	—	50	10*	50	25K	70	0	Fast Wideband, High Accuracy	AD528J	AD
	0.050	0.01	8*	4*	13*	50K	80	0	Wideband FET	µAF771A	† Fairchild
		0.015	—	1*	0.3*	40K	80	0	High Performance, Low Input Current	LM216A	AMD
										LM316A	AMD
										LM216A	National
										LM316A	National
										LM216A	Raytheon
										LM316A	Raytheon
	20.0	0.05	10*	3*	13*	50K	80	0	Low noise, Bipolar-FET	**TL071AM**	**† TI (988)**
										TL071BC	**TI (988)**
			15	12*	5	50K	82	0	Bipolar-JFET, bias comp.	**OP-15C**	**† PMI (871)**
										OP-15G	**PMI (871)**
				17*	9	50K	82	0	Wideband-JFET, bias comp.	**OP-16C**	**† PMI (877)**
										OP-16G	**PMI (877)**
				—	25	50K	82	—	Wideband, Decompensated, Settles to 0.01% in 1.6 µs		
										OP-17C	**† PMI (882)**
										OP-17G	**PMI (882)**
		0.1	10*	1*	3.5*	4K	80	0	Low power, Bipolar-JFET	**TL061AM**	**† TI (985)**
										TL061BC	**TI (985)**
									Programmable Bipolar FET	**TL066AM**	**† TI (985)**
										TL066BC	**TI (985)**
				3*	13*	50K	80	0	Bipolar-JFET	**TL081AM**	**† TI (991)**
										TL081BC	**TI (991)**
								1	Bipolar-JFET	**TL080BC**	**TI (991)**
	4	0.5	5	100	1000	1000K	0		Settles to 0.01% in 200ns	AM-500GC	Datel
										AM-500MC	Datel
			7	100	1000	1000K	0	—	Fast Settling	AM-500MR	Datel
			10	100	1000	1000K	0	—	Fast Settling	AM-500MM	† Datel
	5	3	10*	—	0.1*	40K	80	0	Programmable Amplifier	**HA-2720**	**† Harris (712)**
	7.5	3	—	0.25*	0.16*	100K	70	0	Programmable	4250	† Intersil
										LM4250	† National
										SG4250	† Silicon G
										UC4250	† Solitron
	10	2	15	0.3*	0.13*	50K	80	0	Micropower	RM4132	† Raytheon
				12*	4	100K	80	0	High Impedance	**HA-2600**	**† Harris (588)**
										HA2600	† Intersil
	12	5	4*	—	0.2*	100K	70	0	Programmable	SG1250	† Silicon G
										SG2250	Silicon G
	15	15	15	35*	25	100K	80	1	Wideband, General Purpose	AD507K	AD

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
3.0	(Cont'd.)										
	20	7.5	5*	0.27*	0.16*	50K	70	0	Low Power Adjustable Current	8021M	† Intersil
		10	5*	1*	10	400K	86	0	Wide Response, Low Power	**HA-2700** **HA-2704**	**† Harris (708)** **Harris (708)**
	25	5	10*	—	—	4K	60	3	Matched Transistors	LH0005A	† National
	50	5	—	—	—	50K	80	0	Higher Performance	**SSS741B**	**PMI (839)**
	80	30	15	0.4	0.3	50K	80	0	Higher Performance	LM741A LM741E	† National National
								1	High Slew Rate Inverting	**HA-2530**	**† Harris (684)**
			—	1*	0.6	50K	80	0	to 500 ma, single supply	µA759	† Fairchild
	100	25	—	—	—	25K	70	0	High Performance 741	**SSS741** **SSS741G**	**† PMI (839)** **† PMI (839)**
	110	30	15	0.43	0.3	50K	80	0	JAN 741	38510/10101	† Intersil
	200	50	20	1*	0.5*	50K	80	0	Higher Accuracy 741C	AD741J	AD
									High Current	AD512K	AD
			25	1*	0.5*	50K	80	0	High Current	AD512S	† AD
	300	100	—	2*	1	25K	70	1	±1 amp	833-21	† Beckman
			3*	1*	1.5*	100K	70	1	0.2 amp Power	LH0041	† National
			10	1*	0.4*	25K	70	3	High Gain	RM709	† Raytheon
			25	1*	1.5	100K	70	1	1.0 amp Power	LH0021	† National
	500	60	5*	1*	34*	50K	80	3	Fast General Purpose	1339-02	† Teledyne P
			—	—	4.2*	15K		2	High Slew Rate	ULS-2139	† Sprague
		75	3*	2*	4.2*	50K	80	2	General Purpose	MC1539	† Motorola
	2000	200	4*	10*	—	20K	70	0	General Purpose Wide Bandwidth	LH0003 LH0003C	† National National
3.5	0.015	—	75	1*	3	20K	70	0	High Accuracy, FET	AD506J	AD
	0.030	—	75	1*	50*	20K	70	1-3	High Speed, Laser Trim	AD516J	AD
	12	2.5	6*	—	0.04*	40K	80	1	Micropower	CA3078A	† RCA
									Low Noise, Micropower	CA6078A	† RCA
4.0	0.010	0.002	10	1*	1.5	100K	80	0	High Performance FET	LH0022	† National
	0.020	0.0005*	30	1*	3	50K	70	0	FET Input	8007C-3	Intersil
	15	2	15	4*	2*	40K	80	0	High Performance, High Gain	RM1556	† Raytheon
			—	1*	2.5*	100K	80	0	High Performance	MC1556 MC1556 SG1556	† Motorola Signetics † Silicon G
		15	10*	35*	25	100K	80	1	Wide Band, High Impedance	**HA-2620** HA2620	**† Harris (692)** † Intersil
			20	35*	20	100K	80	1	Wideband, General Purpose	AD507S	† AD
	25	12	15*	4*	5*	100K	80	0	High Voltage	**HA-2640**	**† Harris (700)**
	200	50	15	12*	10	50K	80	0	High Speed, Fast Settling	AD518K	AD
			20	12*	10	50K	80	0	High Speed, Fast Settling	AD518S	† AD
	250	50	—	15*	50	50K	80	0	Precision High Speed	LM118 LM218 µA118 µA218 LM118 LM218 SFC2118 SFC2218 LM118 LM218 LM118 LM218	† AMD AMD † Fairchild Fairchild † National National † NPC NPC † Raytheon Raytheon † TI TI
	300	100	5*	1*	25	50K	70	1	0.5a, Wideband	LH0061	† National

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
4.0	(Cont'd.)										
	350	100	3*	1*	0.5	50K	80	0	741 type	TBA222	† Siemens
	1500	300	—	10*	6*	25K	70	1	Low noise, Comp. for G=3	NE5534	Signetics
										NE5534A	Signetics
	30000	5000	20*	70*	400	4K	60*	3	High Slew Rate	LH0024	† National
4.5	170	32	6*	—	0.04*	25K	80	1	Micropower	CA3078	RCA
5.0	0.001	0.0005*	25	1*	0.6	50K	90*	0	Low Offset FET	3522L	Burr-Brown
	0.005	0.0006		2*	50*	—	80	0	Micropower, Transconductance Amplifier		
										CA3080	RCA
										CA3080A	† RCA
	0.025	0.002	25	15*	50	50K	80	0	Precision, High Speed, FET	LH0062	† National
	0.030	0.02	6*	4*	10*	50K	80	0	MOS-Bipolar	CA3160A	† RCA
			10*	4*	10*	50K	80	1	MOS, Single Supply, Strobe	CA3130A	† RCA
	0.040	0.02	6*	4.5*	9*	20K	70	0	MOS FET, Single Supply	CA3140A	Intersil
										CA3140A	RCA
	0.10	0.02	5*	2.5*	5*	50K	85	0	Bipolar - JFET	LF155	† AMD
										LF255	AMD
										µAF155	† Fairchild
										µAF255	Fairchild
										LF155	† Intersil
										LF255	Intersil
										LF155	† Motorola
										LF255	Motorola
										LF355B	Motorola
										LF155	**† National (786)**
										LF255	**National (786)**
										LF355B	**National (786)**
										PM155	**† PMI (871)**
										PM255	**PMI (871)**
										LF155	† Raytheon
										LF255	Raytheon
										LF155	† Signetics
										LF255	Signetics
										LF355B	Signetics
										LF155	† TI
										LF255	TI
				5*	7.5*	50K	85	0	Wideband - JFET	LF156	† AMD
										LF256	AMD
										µAF156	† Fairchild
										µAF256	Fairchild
										LF156	† Intersil
										LF256	Intersil
										LF156	† Motorola
										LF256	Motorola
										LF356B	Motorola
										LF156	**† National (786)**
										LF256	**National (786)**
										LF356B	**National (786)**
										PM156	**† PMI (877)**
										PM256	**PMI (877)**
										LF156	† Raytheon
										LF256	Raytheon
										LF156	† Signetics
										LF256	Signetics
										LF356B	Signetics
										LF156	† TI
										LF256	TI
				—	—	50K	85	—	Wideband Decompensated	LF157	† AMD
										LF257	AMD
										µAF157	† Fairchild
										µAF257	Fairchild
										LF157	† Intersil

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
5.0	0.10	0.02	5*	—	—	50K	85	—	Wideband Decompensated	(Cont'd.)	
										LF257	Intersil
										LF157	† Motorola
										LF257	Motorola
										LF357B	Motorola
										LF157	**† National (786)**
										LF257	**National (786)**
										LF357B	National
										PM157	**† PMI (882)**
										PM257	**PMI (882)**
										LF157	† Raytheon
										LF257	Raytheon
										LF157	† Signetics
										LF257	Signetics
										LF357B	Signetics
										LF157	† TI
										LF257	TI
			8*	4*	13*	50K	80	0	Wideband-JFET	µAF771	† Fairchild
										µAF771E	Fairchild
		0.025	25*	70*	350	1K	50	2	Ultra Fast FET	LH0032	† National
	0.20	0.1	10*	4*	13*	50K	80	0	Wideband Bipolar-JFET	**LF351B**	**National (776)**
	4	1	10	1*	0.5*	20K	80	0	Low Input Current	AD502L	AD
				0.5*	—	15K	65	1	Low Input Current 709	AD801B	AD
		2	20	0.5*	—	15K	65	1	Low Input Current 709	AD801A	AD
			40	0.5*	—	15K	65	1	Low Input Current 709	AD801S	† AD
	7	4	20	1*	0.5*	20K	80	0	Low Input Current	AD502K	AD
	10	5	7*	1*	0.5*	20K	70	0	Low Input Current	8008M	† Intersil
			10*	—	0.1*	25K	74	0	Programmable Amplifier	**HA-2725**	**Harris (712)**
			20*	1*	0.5*	20K	80	0	Darlington 741	AD502S	† AD
		6	—	0.25*	0.16*	50K	70	0	Programmable	4250C	Intersil
										LM4250C	National
										SG4250C	Silicon G
										UC4250C	Solitron
	15	5	20	0.5*	0.1	45K	100*	0	Low Bias Current	3501A	Burr-Brown
										3501R	† Burr-Brown
	20	3	—	1*	2*	100K	80	0	High Voltage	MC1536	† Motorola
										SG1536	† Silicon G
				—	2.5*	100K	80	1	High Voltage	LM144	† National
	25	5	20	0.3*	0.13*	50K	70	0	Micropower	RC4132	Raytheon
		25	10*	12*	4	80K	74	0	High Impedance	AM-460-2	Datel
										AM-460-2M	† Datel
										HA-2602	**† Harris (688)**
										HA-2605	**Harris (688)**
										HA2602	† Intersil
										HA2605	Intersil
			15*	35*	20	80K	74	1	Wide Band, High Impedance	AM-462-1	Datel
										AM-462-2	Datel
										AM-462-2M	† Datel
										HA-2622	**† Harris (692)**
										HA-2625	**Harris (692)**
										HA2622	† Intersil
										HA2625	Intersil
			20*	12*	—	80K	74	0	Wideband	3506J	Burr-Brown
			30*	1	—	80K	74	1	Wideband	3508J	Burr-Brown
			—	10*	20	80K	100*	1	Wideband, High Gain	1321	Teledyne P
										1321-01	† Teledyne P
	30	15*	20	1.5*	0.6	45K	100*	0	Low Bias, Low Noise	3500A	Burr-Brown
										3500R	† Burr-Brown

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
5.0	(Cont'd.)										
	35	10	20	1.5	3	40K	70	0	High Performance, High Gain	RC1556A	Raytheon
	40	2.5	30*	1*	10	200K	80	0	Micropower FET High Current Out	1323	Teledyne P
		15	10	1*	10	200K	80	0	Wide Response, Low Power	**HA-2705**	**Harris (708)**
		20	0.5	0.2	2.5	1-1000	70	1	Full Instrumentation	AD520K	AD
										AD520S	† AD
	50	15	—	0.2	0.8*	100K	70	0	Programmable Low Power	MC1776	† Motorola
		20	20*	—	0.8	25K	80	0	General Purpose	1320	Teledyne P
			—	—	1.5*	25K	—	0	Low Input Bias, High Slew Rate	ULN-2171	Sprague
	100	20	10	2.5*	18*	25K	80	0	High Speed	**OP-01C**	**PMI (837)**
										OP-01G	**† PMI (837)**
			30	0.5	0.5*	25K	70	1	Precision	SG777C	Silicon G
										µA777C	TI
				1*	0.5*	25K	70	1	Precision	µA777C	Fairchild
			—	—	—	50K	70	0	High Performance 741C	SSS741C	AMD
		25	—	—	—	50K	70	0	High Performance 741	**SSS741G**	**† PMI (839)**
		50	3*	—	—	20-40K	80	1	Micropower	µPC153A	NEC America
										µPC253A	NEC America
		100	—	1*	0.4*	50K	70	0	Programmable	XR146	Exar
	150	20	20	4*	2*	25K	70	0	High Performance, High Gain	RC4131	Raytheon
		30	—	—	—	50K	70	0	Single Supply	TL321I	TI
										TL321M	† TI
		40	6*	—	10	50K	70	0	High Slew Rate	NE535	Signetics
					60*	50K	70	1	60V/µs, Comp. for G=5	NE538	Signetics
	180	25	6.6*	—	3*	22K	93	2	High Output Current	CA3033A	† RCA
			—	—	3*	22K	93	2	High Output Current	CA3047A	RCA
	200	20	5*		250	100K	80	1	High Slew Rate, Inverting	**HA-2535**	**Harris (684)**
		25	20*	12*	25	20K	80	0	High Slew Rate	**HA-2500**	**† Harris (672)**
										HA2500	† Intersil
		50	20*	8*	15*	50K	80	1	Four Addressable Inputs, Single Amplifier		
										HA-2400	**† Harris (668)**
										HA-2404	**Harris (668)**
		60	3*	1*	0.25*	25K	70	2	Micropower, High Performance	LH0001AC	National
		—	10*	10*	130	25K	—	2	High Speed Inverting	8017M	† Intersil
	250	20	20	1*	0.5*	25K	96	1	General Purpose	LM301A	Raytheon
								0	General Purpose	LM307	Raytheon
			25	1*	0.4	50K	80	0	High Performance, Low Drift	1319	Teledyne P
		50	—	—	0.6*	25K	—	0	General Purpose	ULN-2151	Sprague
	300	150	10*	7*	3.5	25K	80	0	Low Noise	**HA-909**	**† Harris (656)**
	350	35	6.6*	—	2.7*	16K	84	2	High Output Current	CA3033	† RCA
			—	—	2.7*	16K	84	2	High Output Current	CA3047	RCA
	500	200	3*	0.5*	0.3*	25K	70	3	General Purpose	µA709M	† Fairchild
										MC1709	† Motorola
										LM709	† National
										TAA522	† Siemens
										µA709	† Signetics
										TL1709	Telefunken
										µA709M	† TI
				0.8*	5*	50K	70	0	Wideband 741	SG1217	† Silicon G
				1*	0.5*	50K	70	0	General Purpose Compensated	AD741	† AD
										741M	† AMD
										µA741M	† Fairchild
										741	† Intersil

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
5.0	500	200	3*	1*	0.5*	50K	70	0	General Purpose Compensated	(Cont'd.)	
										M5141	Mitsubishi
										MC1741	Motorola
										MC1741	†Motorola
										LM741	†National
										PM741	**PMI** (839)
										RM741	†Raytheon
										CA741	†RCA
										µA741	†Signetics
										SG741	†Silicon G
										TL1741	Telefunken
										µA741M	†TI
									Low Noise 741	741LN	†Intersil
										CA6741	†RCA
									Compensated 101	LH101	†National
										LH101	†Raytheon
								1	General Purpose, Uncompensated	LM101	†AMD
										LM201	AMD
										µA101	†Fairchild
										LM101	†National
										LM101	†Raytheon
										CA101	†RCA
										LM101	†Signetics
										SG101	†Silicon G
									Uncompensated 741	748M	†AMD
										µA748M	†Fairchild
										MC1748	†Motorola
										LM748	†National
										LM748C	National
										RM748	†Raytheon
										CA748	†RCA
										µA748	†Signetics
										SG748	†Silicon G
										µA748M	†TI
					10	50K	70	0	High Slew Rate 741	MC1741S	†Motorola
										SG741S	†Silicon G
			4*	30*	0.7*	20K	70	2	Programmable	CA3094	†RCA
										CA3094A	†RCA
										CA3094B	†RCA
			—	0.5*	35	50K	70	1	High Slew Rate	RM4531	†Raytheon
				1*	0.7	50K	70	0	High Speed 741	741MHS	†Intersil
					30*	50K	70	1	High Slew Rate	SE531	†Signetics
				—	—	100K*	70	0	General Purpose	M51802	Mitsubishi
	750	250	6*	65*	15	15K	74	3	High Speed High Gain	µA715M	†Fairchild
										715	†AMD
	800	200	20	—		2K	70	3	709 Type	µPC55A	NEC America
	1000	150	8*	—	2*	40K	90	3	General Purpose	MC1533	Motorola
	2000	400	—	38*	25*	0.6K	76	1	Large Signal Wideband	CA3100	†RCA
	7000	2000	5*	—	—	2K	70	1	702 Type	µPC51A	NEC America
	7500	2000	5*	7*	1.5*	2K	70	2	Wideband	MC1712C	Motorola
			20	30*	3.5*	2K	70	3	Wideband	µA702C	Fairchild
										µPC702	NEC America
										SL702C	Plessey
										RC702	Raytheon
	10000	2000	10*		1.7*	1.4K	70	3	General Purpose	TL702M	†TI
						4.5K	70	3	General Purpose	MC1530	†Motorola
	12000	5000	1.2*	15*	3*	0.7K	70	1	6 Volt, Wideband	CA3008	†RCA
										CA3010	†RCA
										CA3029	RCA

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† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
5.0	12000	5000	1.2*	15*	3*	0.7K	70	1	6 Volt, Wideband	(Cont'd.) CA3037	†RCA
	20000	—	10	—	800	250	70	1	Fast, slews 800 V/µs	NE5539	Signetics
										SE5539	†Signetics
			25	500*	250	10K	80	1	Settles to 0.01% in 70 ns	1435	†Teledyne P
	24000	5000	3.5*	50*	7*	2K	80	1	12 Volt, Wideband	CA3015	†RCA
										CA3016	†RCA
										CA3030	RCA
										CA3038	†RCA
6.0	0.025	0.002	15	1*	1	75K	70	0	High Performance FET	LH0022C	National
	0.2	0.05	10*	3*	13*	50K	80	0	Low Noise Bipolar-JFET	**TL071AC**	**TI (988)**
										TL071M	**†TI (988)**
			0.1	10*	1*	3.5*	40K	0	Low Power Bipolar JFET	**TL061AC**	**TI (985)**
										TL061M	**†TI (985)**
									Programmable Bipolar JFET	**TL066AC**	**TI (985)**
										TL066M	**†TI (985)**
				3*	13*	50K	80	0	Bipolar-JFET	µPCF081	NEC America
										TL081AC	**TI (991)**
										TL081M	**†TI (991)**
								1	Bipolar-JFET	**TL080AC**	**TI (991)**
										TL080M	**†TI (991)**
	25	10	6*	—	0.2*	75K	70	0	Programmable	SG3250	Silicon G
		12	40	1*	0.5*	20K	80	0	Low Input Current	AD502J	AD
		20	15*	—	0.5*	20K	70	0	Low Input Current	8008C	Intersil
		25	15*	35*	20	80K	74	1	Wideband, General Purpose	AD507J	AD
	30	30	15*	4*	5*	100K	74	0	High Voltage	AM-464-2	Datel
										AM-464-2M	†Datel
										HA-2645	**Harris (700)**
										1332	Teledyne P
	35	10	5*	0.27*	0.16*	50K	70	0	Low Power Adjustable Current	8021C	Intersil
	50	25	—	0.2	0.8*	50K	70	0	Programmable Low Power	MC1776C	Motorola
										MC3476	Motorola
	100	25	—	—	—	25K	70	0	High Performance 741C	**SSS741C**	**PMI (839)**
		30	5*	—	0.3*	25K	70	1	Supply to ±10v	TCA520	Signetics
	250	50	—	1*	0.5	25K	80	0	to 500 ma, single supply	µA759C	Fairchild
	500	200	3*	1*	10	20K	70	0	High Slew Rate 741	MC1741SC	Motorola
										SG741SC	Silicon G
			5*	0.8*	5*	20K	70	0	Wideband 741C	SG3217	Silicon G
				1*	1	100K	70	1	0.2 amp Power	LH0041C	National
			10*	1*	0.25	100K	90	2	High Gain, Instrumentation, 50 ma Output	LH0020C	National
					0.5*	25K	70	0	Low Noise 741	741CLN	Intersil
			15*	0.2*	0.2*	20K	70	0	High Power	µA791C	Fairchild
			30	1*	1*	100K	70	0	1.0 amp Power	LH0021C	National
			—	1*	0.5*	20-50K	70	1	General Purpose	748C	AMD
										µA748C	Fairchild
										MC1748C	Motorola
										SFC748C	NPC
										SL748	Plessey
										RC748	Raytheon
										CA748C	RCA
										µA748C	Signetics
										TDA0748	Signetics
										SG748C	Silicon G
										µA748C	TI

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† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
6.0	500	200	—	1*	0.5*	20-50K	70	1	(Cont'd.) High Reliability	L148	SGS
					0.5	20-50K	70	0	General Purpose Compensated	AD741C	AD
										µA741C	Fairchild
										HA17741	Hitachi
										741C	Intersil
										MC1741C	Motorola
										LM741C	National
										µPC151	NEC America
										µPC741	NEC America
										SFC741C	NPC
										PM741C	**PMI** (839)
										RC741	Raytheon
										CA741CC	RCA
										µA741C	Signetics
										SA741C	Signetics
										TDA0741	Signetics
										SG741C	Silicon G
										TL1741C	Telefunken
										TL3741C	Telefunken
										TL4741C	Telefunken
										µA741C	TI
					0.7	25K	70	0	High Speed 741	741CHS	Intersil
				—	1	20K	70	1	1 amp	833-21C	Beckman
		300	10*	7*	5*	20K	74	0	Low Noise	**HA-911**	**Harris** (656)
				12*	50	25K	70	0	High Speed, Fast Settling	AD518J	AD
	1000	300	6*	—	18*	5K	60	0	20ma Output	TCA325	Siemens
						12K	65	1	20ma Output	TAA761	Siemens
										TAA765	Siemens
						18K	70	1	20ma Output	TAA762	† Siemens
										TAA862	† Siemens
	1200	500	5*	4*	4*	10K	70	2	Gated	ZN424	Ferranti
	1500	200	—	0.5*	35*	20K	70	1	High Slew Rate	RC4531	Raytheon
				1*	20	20K	70	1	High Slew Rate, High Performance	NE531	Signetics
7.0	200	10*	10*	10*	130*	25K	—	2	High Speed Inverting	8017C	Intersil
		50	—	—	—	25K	65	0	Single Supply	TL321C	TI
7.5	7	1	6*	—	—	25K	80	1	308 Type	µPC156A	NEC America
			30	1*	0.3*	25K	80	0	Micropower, Supply Current 800µa	LM312	AMD
										LM312	National
				0.3*	0.1	25K	80	0	Compensated 308	SG3118	Silicon G
				1*	0.3*	25K	80	1	Precision Bipolar	AD308	AD
										LM308	AMD
										µA308C	Fairchild
										308	Intersil
										LM308	Motorola
										LM308	National
										SFC2308	NPC
										PM308	PMI
										LM308	Raytheon
										CA308	RCA
										LM308	Signetics
										SG308	Silicon G
			—	0.3*	0.3*	25K	80	1	Low Noise 308	308LN	Intersil
	15	2	30		0.1	25K	80	1	Precision	1660	AMD
				0.3*	0.1	25K	80	1	Improved 201, 301A	SG1660	Silicon G
								0	Improved 307, 741	SG1760	Silicon G
	250	50	30	1*	0.5*	25K	70	0	General Purpose, Uncompensated	LM307	AMD
										µA307C	Fairchild
										307	Intersil

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
7.5	250	50	30	1*	0.5*	25K	70	0	General Purpose, Uncompensated	(Cont'd.)	
										LM307	Motorola
										LM307	National
										SFC2307	NPC
										CA307	RCA
										LM307	Signetics
										SG307	Silicon G
										LM307	TI
								1	General Purpose, Compensated	AD301A	AD
										LM301A	AMD
										µA301A	Fairchild
										301A	Intersil
										LM301A	Motorola
										LM301A	National
										µPC157	NEC America
										µPC301	NEC America
										SFC2301A	NPC
										CA301A	RCA
										LM301A	Signetics
										TDA0301	Signetics
										SG301A	Silicon G
										LM301A	TI
			—	0.8*	0.5*	25K	70	1	Low Noise 301A	301ALN	Intersil
	350	35	—	—	—	16K	84	2	General Purpose	M5133	Mitsubishi
	600	60	5*	1*	34*	40K	80	3	Fast General Purpose	1339-01	Teledyne P
	1000	100	12*	1*	34*	15K	80	3	Fast General Purpose	1339	Teledyne P
		150	3*	2*	4.2*	15K	80	2	General Purpose	MC1439	Motorola
	1500	250	6	65*	10	10K	74	3	High Speed	715C	AMD
										µA715C	Fairchild
		500	6*	1*	0.5*	20K	65	0	Compensated 201	LH201	National
										LH201	Raytheon
								1	General Purpose	LM301	AMD
										µA201M	Fairchild
										LM201	National
										LM201	Raytheon
										CA201	RCA
										LM201	Signetics
										SG201	Silicon G
			6-10*	1*	0.3*	15K	65	3	General Purpose	µA709C	Fairchild
										M51709	Mitsubishi
										LM709C	National
										RC709	Raytheon
										TAA521	Siemens
										µA709C	Signetics
										SA709C	Signetics
										TL1709C	Telefunken
										TL3709C	Telefunken
										µA709C	TI
	2000	100	—	—	4.2*	50K	—	2	High Slew Rate	ULN-2139	Sprague
		500	10*	—	2*	30K	80	3	General Purpose	MC1433	Motorola
8.0	40	10	—	1*	2.5*	70K	70	1	High Voltage	LM344	National
	200	25	20*	10*	50	10K	80	0	High Slew Rate	**HA-2510**	**† Harris** (676)
				20*	100	10K	80	1	100v/µs, Gain=3	**HA-2520**	**† Harris** (680)
										HA2520	† Intersil
			30	20*	100	10K	80	1	High Speed, Fast Settling	AD509K	AD
										AD509S	† AD
	250	50	20*	12*	20	15K	74	0	High Slew Rate	AM-450-2	Datel
										AM-450-2M	† Datel
										HA-2502	**† Harris** (672)
										HA-2505	**Harris** (672)
										HA2502	† Intersil

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† Military Temperature Range (−55° to 125°C) * Typical Values

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
8.0	250	50	20*	12*	20	15K	74	0	High Slew Rate	(Cont'd.) HA2505	Intersil
				6*	20	16K	74	0	Fast Slewing	3505J	Burr-Brown
	40000	15000	25*	70*	250	3K	60*	3	High Slew Rate	LH0024C	National
9.0	250	50	30*	8*	15*	50K	74	1	Four Addressable Inputs Single Amplifier	**HA-2405**	**Harris** (668)
10.0	0.010	0.0005*	10	1*	3	50K	70	0	FET Input	8007C-4	Intersil
			15	1*	3	50K	70	0	FET Input	8007C-5	Intersil
										8007M-5	† Intersil
	0.050	0.020*	30	3*	15*	20K	86*	0	High Voltage FET	3580J	† Burr-Brown
	0.15	0.05	—	1*	0.3*	20K	80	0	High Performance, Low Input Current	LM216	AMD
										LM316	AMD
										LM216	National
										LM316	National
										LM216	Raytheon
										LM316	Raytheon
	0.20	0.05	5*	2.5	5*	25K	80	0	Bipolar - JFET	LF355	AMD
										µAF355	Fairchild
										LF355	Intersil
										LF355	Motorola
										LF355	**National** (786)
										PM355	**PMI** (871)
										LF355	Raytheon
										LF355	Signetics
										LF355	TI
				5	12*	25K	80	0	Wideband - JFET	LF356	AMD
										µAF356	Fairchild
										LF356	Intersil
										LF356	Motorola
										LF356	**National** (786)
										PM356	**PMI** (877)
										LF356	Raytheon
										LF356	Signetics
										LF356	TI
				—	—	25K	80	—	Wideband Decompensated	LF357	AMD
										µAF357	Fairchild
										LF357	Intersil
										LF357	Motorola
										LF357	**National** (786)
										PM357	**PMI** (882)
										LF357	Raytheon
										LF357	Signetics
										LF357	TI
			8*	4*	13*	25K	70	0	Wideband JFET	µAF771C	Fairchild
			10*	3*	13*	25K	70	0	Low Noise Bipolar-JFET	**TL071C**	**TI** (988)
				5*	15*	25K	70	0	Bipolar-JFET	**LF351**	**National** (776)
	10	3	150	—	250	0.7K	50	1	100MHZ Unity Gain Frequency	9906	OEI
	30	10	20	4*	2*	40K	70	0	High Performance, High Gain	RC1556	Raytheon
			—	1*	2.5*	70K	70	0	High Performance	MC1456	Motorola
										SG1456	Silicon G
	40	10	—	1*	2*	70K	70	0	High Voltage	MC1436	Motorola
										MC1456	Signetics
										SG1436	Silicon G
	50	20	20*	—	—	2K	55	3	Matched Input Transistors	LH0005	† National
	80	40	1000	0.2	2.5	1-1000	65	1	Full Instrumentation	AD520J	AD
	100	25	25*	—	—	2K	50	3	Matched Input Transistors	LH0005C	† National
	150	25	—	—	0.4*	2.5K	65	3	Darlington Input	MC1531	† Motorola
	250	50	20*	20*	80	7.5K	74	1	High Speed, Fast Settling	AD509J	AD

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† Military Temperature Range (−55° to 125°C) * Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
10.0	250	50	(Cont'd.)								
			25*	12*	40	7.5K	74	0	High Slew Rate	**HA-2512**	**†Harris (676)**
				20*	80	7.5K	74	1	80V/µs Gain = 3	**HA-2522**	**†Harris (680)**
										HA2522	†Intersil
			30*	12*	40	7.5K	74	0	High Slew Rate	**HA-2515**	**Harris (676)**
					80	7.5K	74	1	80V/µs Gain = 3	AM-452-2	Datel
										AM-452-2M	†Datel
										HA-2525	**Harris (680)**
										HA2525	Intersil
				20*	80	7.5K	89*	1	High Slew Rate	1322	Teledyne P
										1322-01	†Teledyne P
				—	80	7K	74	1	Fast Slewing	3507J	Burr-Brown
	500	200	5*	1*	25	25K	60	1	0.5A, wideband	LH0061C	National
			—	15*	50	25K	70	0	Precision, high speed	LM318	AMD
										µA318	Fairchild
										LM318	National
										µPC159A	NEC America
										SFC2318	NPC
										LM318	TI
	600	200	—	15*	50	25K	70	2	Precision, High Speed	LM318	Raytheon
	750	—	—	—	—	14K	—	1	Telephone Channel Amplifier	L045	SGS
	1000	300	6*	—	18*	0.56K	60	1	to 90 ma Output	TAA861	Siemens
										TAA865	Siemens
										TAA861	Telefunken
										TAA865	Telefunken
	15000	4000	—	—	1.7	3K	65	3	General Purpose	MC1430	Motorola
		5000	5*	—	1.7*	1K	65	3	General Purpose	TL702C	TI
	2000	100	2*	10*	5*	1K	75	2	Differential Output	MC1520	†Motorola
12.0	0.020	0.02	20*	5*	10*	80K	74	1	Wideband, FET Input	**HA-2060A**	**†Harris (664)**
			40*	5*	10*	80K	70	1	Wideband, FET Input	**HA-2065A**	**Harris (664)**
	90	25	—	1*	2*	50K	50	0	High Voltage	MC1436C	Motorola
										SG1436C	Silicon G
		30	—	1*	2.5	25K	110*	0	High Performance	MC1456C	Motorola
										SG1456C	Silicon G
14.0	0.020	0.02	20*	8*	40*	7.5K	74	1	120V/µs Gain = 3	**HA-2050A**	**†Harris (660)**
			40*	8*	40*	7.5K	70	1	120V/µs Gain = 3	**HA-2055A**	**Harris (660)**
	20	—	75*	20*	60	40K*	90	0	High Slew Rate	1434	Teledyne P
15.0	0.010	0.005	25	1	3	100K	80	0	General Purpose, Low Drift	1421-02	Teledyne P
	0.015	0.01	25	1	3	100K	72	0	Low Noise	1421-25	Teledyne P
			50	1	3	100K	72	0	General Purpose, Low Drift	1421-01	Teledyne P
		0.01*	50	5	8	100K	72	—	Wideband, FET	1422-01	Teledyne P
	0.020	0.01	10*	0.14*	1*	1-1000	75	2	Full Instrumentation FET	AM-435-1M	†Datel
										LF152	†National
	0.050	0.025	50	1	3	50K	72	0	General Purpose	1421	Teledyne P
				—	—	50K	72	0	Low Noise	1421-24	Teledyne P
		0.030	10*	4*	10*	50K	70	1	MOS FET Single Supply, Strobe	CA3130	†RCA
			8*	4*	10*	50K	70	0	MOS FET, Single Supply	CA3160	†RCA
				4.5*	9*	20K	70	0	MOS FET, Single Supply	CA3140	Intersil
										CA3140	†RCA
	0.065	0.005	35	15*	50	25K	70	0	Precision, High Speed, FET	LH0062C	National
	0.20	0.05	10*	1*	0.5*	25K	70	0	JFET-741	LF13741	National
			25*	50*	350	1K	50	2	Ultra Fast FET	LH0032C	National
		0.10	5*	1*	6*	50K	80	0	FET Input	LH740A	†National

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
15.0	(Cont'd.)										
	0.4	0.2	10*	1*	3.5*	3K	70	0	Low Power Bipolar-JFET	**TL061C**	**TI (985)**
									Programmable Bipolar-JFET	**TL066C**	**TI (985)**
				3*	13*	25K	70	0	Bipolar-JFET	µPCF081	NEC America
										TL081C	**TI (991)**
								1	Bipolar-JFET	**TL080C**	**TI (991)**
	300	100	—	—	1.4*	1.5K	60	3	Darlington Input	MC1431	Motorola
	4000	200	2*	10*	5*	0.75K	60	2	Differential Output	MC1420	Motorola
20.0	0.005	—	30	0.5*	3	40K	80	0	Electrometer, FET	AD523K	AD
	0.010	0.002*	25	1*	2.5	31K	86*	0	High Performance, Low Bias FET	3503B	Burr-Brown
										3503S	† Burr-Brown
		—	25	0.75*	0.5*	50K	70	0	Low Noise FET	AD514L	AD
	0.020	0.0005*	75	1*	6*	50K	70	0	High Performance FET	8007M	† Intersil
		—	25	1*	3	50K	80	1-3	50V/µs Feed Forward	AD513K	AD
				0.75*	0.5	50K*	70	0	Low Noise FET	AD514K	AD
			50	0.75*	0.5*	50K*	70	0	Low Noise FET	AD514S	† AD
				1*	3	50K	80	1-3	50V/µs Feed Forward	AD513S	† AD
	0.025	0.002*	50	1*	0.5*	25K	80*	0	Low Noise	3542J	Burr-Brown
										3542S	† Burr-Brown
		0.010	20	1*	1.5	50K	70	0	Low Cost FET Input	LH0042	† National
		—	25	1*	6*	50K	70	0	Low Cost FET Input	AD540K	AD
			50	1*	6*	50K	70	0	Low Cost FET Input	AD540S	† AD
					0.5*	25K	80	0	FET	AD3542J	AD
			60	0.5*	3	40K	80	0	Electrometer, FET	AD523L	AD
	0.030	0.005*	20*	1*	6*	50K	70	0	FET	SU536	Signetics
	0.050	0.005	25	1*	1	25K	70	0	Low Cost FET	LH0042C	National
		—	25	1*	6*	25K	70	0	Low Cost FET	AD0042C	AD
	0.10	—	25	1*	3	50K	80	0	Low Cost FET Input	AD503K	AD
										AD503S	† AD
	0.20	0.15	20*	3*	6*	50K	64	0	High Slew Rate FET	µA740M	† Fairchild
										740	† Intersil
	0.50	0.15	5*	1*	6*	50K	80	0	FET Input	LH740AC	National
	50	25	200	—	—	3K	60	0	Darlington Input	TCA315	Siemens
								1	Darlington Input	TCA335	Siemens
25.0	0.020	0.02	50*	5*	10*	80K	74	1	120V/µs Gain=3	**HA-2060**	**† Harris (664)**
				8*	40*	7.5K	74	1	High Slew Rate, FET	**HA-2050**	**† Harris (660)**
	40000	10000	1000	60	600	1K	50	2	Wide Gain-Bandwidth	9912	† OEI
30.0	0.001	0.0002*	50	1*	2.5	20K	86	0	Low Bias FET	8007AM	† Intersil
										8007AC	Intersil
		—	50*	1*	6*	20K	86	0	FET	1439	Teledyne P
	0.040	0.020	10*	0.14*	1*	1-1000	65	2	Full Instrumentation, FET	AM435-1C	Datel
										LF252	National
										LF352	National
	30*	2	0.06*	1*	6*	1000K	80*	0	High Slew Rate FET	µA740C	Signetics
	30000	10000	150	200	300	1K	50	0	Wide band	9916	† OEI
50.0	0.00001	—	—	—	0.5*	20K	60	0	Ultra Low Bias FET	ICH8500A	Intersil
	0.0001	—	—	—	0.5*	20K	60	0	Ultra Low Bias FET	ICH8500	Intersil
	0.001	0.0005*	90	0.5*	3	20K	70	0	Electrometer, FET	AD523J	AD
		—	50	0.3*	—	10K	70		MOS FET	µPC250A	NEC America
	0.015	—	75	1*	3	20K	70	0	Low Cost FET Input	AD503J	AD
	0.025	0.005*	75	1*	2.5	20K	86*	0	High Performance, Low Bias FET	3503A	Burr-Brown

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† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units (Cont'd)											
50.0	0.025	0.005*	75	1*	2.5	20K	86*	0	High Performance, Low Bias FET	(Cont'd.) 3503R	† Burr-Brown
	0.030	—	75	1*	3	20K	70	1-3	50V/µs Feed Forward	AD513J	AD
	0.050	0.0005*	75	1*	6*	20K	70	0	High Performance, FET	3540J 8007C	Burr-Brown Intersil
									Low Cost FET	1424	Teledyne P
		—	75	0.75*	0.5*	20K	70	0	Low Noise FET	AD514J	AD
				1*	6*	20K	70	0	Low Cost FET	AD540J	AD
50.0*	150	—	25	100	600	63K	—	0	Wideband Inverting	HVA23	DDC
60.0	0.020	0.02	60*	5*	10*	80K	70	1	Wideband, FET Input	AM-406-2 AM-406-2M **HA-2065** 1433	Datel † Datel **Harris (664)** Teledyne P
				8*	40*	7.5K	70	1	120V/µs Gain = 3	AM-405-2 AM-405-2M **HA-2055**	Datel † Datel **Harris (660)**
90.0	0.10	0.005*	30*	1*	6*	50K	64	0	FET, High Input Impedance	NE536	Signetics
110.0	2	0.3	20*	1*	6*	20K	55	0	High Slew Rate FET	µA740C	Fairchild
			—	1*	6*	20K	55	0	High Slew Rate FET	740C	Intersil
200.0	0.01	—	50*	1*	0.4*	10K	70*		MOS FET	µPC152A	NEC America
—	0.3	0.1	3000	100	200	0.3K	50	0	Wideband, Fast Slewing	9908	OEI
	150	—	25	80	400	63K	—	0	Fast Settling, Inverting	HFS23	DDC
Dual Units											
0.5	2	0.2	15	1*	0.3*	80K	96	1	Dual 108A	LH2108 LH2108A LH2208A LH2108A LH2208A	† Intersil † National National † Signetics Signetics
	3	2.8	2	1.2*	0.25*	200K	114	0	Dual Matched Instrumentation	**OP-10** OP-10A	**† PMI (857)** † PMI
	4	3.8	2	1.2*	0.25*	200K	110	0	Dual Matched Instrumentation	OP-10E	PMI
	7	1	30	1*	0.3*	80K	96	1	Dual 308A	LH2308 LH2308A LH2308A	Intersil National Signetics
0.75	50	2	8	0.8	0.5	100K	90	0	Dual Matched	**OP-04A** **OP-04E** **OP-14A** **OP-14E**	**† PMI (844)** **PMI (844)** **† PMI (844)** **PMI (844)**
1.3	7	6	4.5	1.2*	0.25*	120K	100	0	Dual Matched Instrumentation	OP-10C	PMI
2.0	0.10	0.05	10*	4*	13*	50K	80	0	Dual 351A	**LF353A**	**National (784)**
	2	0.2	15	1*	0.3*	50K	85	1	Dual 108	LH2108 LH2208 LH2108 LH2208	† National National † Signetics Signetics
	50	5	—	—	—	100K	80	0	Dual High Performance 741	SSS747 **SSS747**	† AMD **† PMI (844)**
		10	15	1*	—	50K	70	0	Low Power	LM158A	National
									Single Supply	SE532A	† Signetics
		25	5	1.5*	0.8	100K*	100*		Matched Amplifier Pairs	3500MP	Burr-Brown
	60	10	15	1*	10	50K	70	0	High slew rate	SE5535	† Signetics
				—	—	50K	70	1	40 V/µs, G=5	SE5538	† Signetics
	75	5	10	0.8	0.5	50K	90	0	Dual Matched	**OP-04** **OP-04C** **OP-14**	**PMI (844)** **PMI (844)** **† PMI (844)**

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Dual Units (Cont'd)											
2.0	75	5	10	0.8	0.5	50K	90	0	Dual Matched	(Cont'd.) **OP-14C**	**PMI (844)**
		10	15	1*	0.5*	50K	80	1	Dual LM101A High Performance	1501L	†AMD
										1501M	†AMD
										LH2101A	†AMD
										LH2201A	AMD
										LH2101A	Intersil
										LH2101A	†National
										LH2201A	National
										LH2101A	†Signetics
										LH2201A	Signetics
	800	200	—	10*	6*	50K	80	0	Dual 5534	SE5533	†Signetics
3.0	0.05	0.01	8*	4*	13*	50K	80	0	Wideband JFET	µAF772A	†Fairchild
	0.2	0.05	10*	3*	13*	50K	80	0	Low Noise Bipolar-JFET	**TL072AM**	**†TI (988)**
										TL072BC	**TI (988)**
		0.1	10*	1*	3.5*	4K	80	0	Low Power, Bipolar JFET	**TL062AM**	**†TI (985)**
										TL072BC	**TI (988)**
				3*	15*	50K	80	0	Bipolar JFET	**TL082AM**	**†TI (991)**
										TL082BC	TI
	5	3	10*	25*	0.1*	40K	80	0	Programmable	**HA-2730**	**†Harris (718)**
	15	5	—	.25*	0.16*	100K	70	0	Programmable Dual LM4250	LH24250	†National
	20	7.5	5*	0.27*	0.16*	50K	70	0	Low Power Adjustable Current	8022M	†Intersil
	50	5	—	—	—	50K	80	0	Higher Performance	**SSS747B**	**PMI (844)**
	80	15	15	1*	—	50K	70	0	Low Power	LM258A	National
		30	15	0.44	0.3	50K	80	0	Dual 741	µA747AM	†Fairchild
										µA747EC	Fairchild
										LM747A	†National
										LM747E	National
	100	30	8*	8*	2	25K	80	0	High Slew Rate	**HA-2650**	**†Harris (704)**
			20	1*	—	25K	65	0	Low Power, Single Supply	LM358A	National
	750	400	3*	—	2*	20K	70	3	Audio Preamp	µA749C	Fairchild
										µA749M	†Fairchild
	3000	300	10*	1*	.01*	4K	70*	3	General Purpose	MC1535	†Motorola
4.0	1500	300	—	10*	6*	25K	70	1	Dual 5534	NE5533	Signetics
5.0	0.10	0.02	8*	4*	13	50K	80	0	Wideband JFET	µAF772	Fairchild
										µAF772E	Fairchild
		0.20	0.10	10*	4*	13*	50K	0	Dual 351B	**LF353B**	**National (784)**
	7.5	3	3*	1*	15*	200K	70	0	Multi-Purpose Programmable	µA776M	†Fairchild
	10	5	10*	—	0.1*	25K	74	0	Programmable	**HA-2735**	**Harris (718)**
		25	10*	1*	0.6*	50K	70	0	Single Supply, I/O operates to ground	µA798M	†Fairchild
	100	25	—	—	—	50K	70	0	Dual High Performance 741C	SSS747C	AMD
										SSS747C	**PMI (844)**
										SSS747G	**†PMI (844)**
										SSS1458	**PMI (844)**
										SSS1558	**†PMI (844)**
		40	—	0.8*	0.5*	4K	60	0	Low Power	TL022M	†TI
	150	30	7*	1*	—	50K	70	0	Half LM124	LM158	†Motorola
										LM158	†National
										LM258	National
										LM158	†Signetics
										LM258	Signetics
										SE532	†Signetics
										LM158	†TI
			40	6*	1*	10	70	0	High Slew Rate, Dual 535	NE5535	Signetics
					—	—	70	1	60 V/µs, G=5, Dual 538	NE5538	Signetics
	200	60	8*	8*	2	20K	74	0	High Slew Rate	**HA-2655**	**Harris (704)**

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Dual Units (Cont'd)											
5.0	200	(Cont'd.)									
		80	—	0.8*	0.5*	1K	60	0	Low Power	TL022C	TI
	500	50	10*	1*	0.6*	50K	70	0	Single Supply	MC3558	† Motorola
		200	2-15*	1*	0.5*	50K	70	0	Dual 741	747M	† AMD
										1558	† AMD
										XR1558	† Exar
										µA747M	† Fairchild
										µA1558M	† Fairchild
										MC1747	† Motorola
										MC1558	† Motorola
										LM747	† National
										LM1558	† National
										PM747	**† PMI (844)**
										PM1558	**† PMI (844)**
										CA747	† RCA
										CA1558	† RCA
										RM747	† Raytheon
										RM1558	† Raytheon
										MC1558	† Signetics
										TDA1458	Signetics
										µA747	† Signetics
										SG747	† Silicon G
										SG1558	† Silicon G
										µA747M	† TI
										MC1558	† TI
									Low Noise	MC1558N	† Motorola
					0.25	25K	70	3	Dual MC1709	MC1537	† Motorola
			—	2	1.5*	50K	70	0	Dual Wideband 741	RM4558	† Raytheon
										RM4558	† TI
				3	1.5	50K	70	0	3MHz min. Bandwidth	**RM4559**	**† Raytheon (974)**
				2.5	1.5	50K	70	0	Dual Wideband 741	MC4558	† Motorola
										MC4558A	Motorola
				—	10	50K	70	0	High Slew Rate 1558	MC1558S	† Motorola
	5000	500	10*	1*	0.01*	3.5K	70	3	General Purpose	MC1435	Motorola
6.0	0.2	0.05	10*	3*	13*	50K	80	0	Low Noise Bipolar-JFET	**TL072AC**	**TI (988)**
										TL072M	**† TI (988)**
		0.1	10*	1*	3.5*	4K	80	0	Low Power Bipolar-JFET	**TL062AC**	**TI (985)**
										TL062M	**† TI (985)**
				3*	13*	50K	80	0	Bipolar JFET	**TL082AC**	**TI (991)**
										TL082M	**† TI (680)**
										TL083AC	**TI (991)**
										TL083M	**† TI (991)**
	10	6	3*	1*	15*	50K	70	0	Multi-Purpose Programmable	µA776C	Fairchild
	30	10	5*	0.27*	0.16*	50K	70	0	Low Power Adjustable Current	8022C	Intersil
			—	0.25*	0.16*	75K	70	0	Programmable Dual LM4250	LH24250C	National
	250	50	7*	1*	0.6*	25K	65	0	Half LM244/324	LM258	Motorola
										LM358	Motorola
										NE532	Signetics
										SA532	Signetics
		75	10*	1*	0.6*	20K	70	0	Single Supply, I/O operates to ground	µA798C	Fairchild
	500	200	—	1*	0.5*	20-50K	70	0	Dual 741C	1458	AMD
										747C	AMD
										XR1458	Exar
										µA747C	Fairchild
										µA1458C	Fairchild
										MC1458	Motorola
										MC1747C	Motorola
										LM747C	National
										LM1458	National
										µPC251	NEC America

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† Military Temperature Range (−55° to 125°C)

* Typical Values

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Dual Units (Cont'd)											
6.0	500	200	—	1*	0.5*	20-50K	70	0	Dual 741C	(Cont'd.)	
										µPC1458	NEC America
										PM747C	**PMI (844)**
										PM1458	**PMI (844)**
										CA747C	RCA
										CA1458	RCA
										RC747	Raytheon
										RC1458	Raytheon
										µA747C	Signetics
										SA747C	Signetics
										MC1458	Signetics
										SA1458	Signetics
										SG747C	Silicon G
										SG1458	Silicon G
										µA747C	TI
										MC1458	TI
				2	0.5*	20	70	0	Dual Wideband 741C	MC4558C	Motorola
				3	1.5	20K	70	0	3MHz min. Bandwidth	**RC4559**	**Raytheon (974)**
										RV4559	**Raytheon (974)**
				3*	1	20K	70	0	Wideband 741	XR4558	Exar
										µA4558	Fairchild
										µPC4558	NEC America
										RC4558	Raytheon
										RC4558	TI
									Low Noise	XR4739	Exar
										RC4739	Raytheon
			10*	1*	0.8*	20K	70	0	Low Noise	MC1458N	Motorola
					10	20K	70	0	High Slew Rate 1458	MC1458S	Motorola
	1000	500	—	—	—	12K*	70	2	Low Noise	TCA490	Signetics
	2000	1000	—	—	1*	6.5K	70	2	Low Noise	µA739	Fairchild
										TBA231	SGS
7.0	250	50	7*	1*	—	25K	65	0	Half LM224	LM358	National
										LM358	Signetics
										NE532	Signetics
										LM258	TI
										LM358	TI
						100K	50	0	Low Power, Single Supply	LM2904	National
										LM2904	TI
	500	50	—	1*	—	100K*	55*	0	258 type	TDA0358	Signetics
7.5	7	1	30	1*	0.3*	25K	80	1	Dual 308	LH2308	National
	250	50	30	1*	0.5*	25K	70	1	Dual High Performance	1501C	AMD
										LH2301A	AMD
										LH2301A	Intersil
										LH2301A	National
										LH2301A	Signetics
	1500	500	1.5*	1*	0.3*	15K	65	3	Matched Dual 709	RC1437	Raytheon
					0.25*	15K	65	3	Matched Dual MC1709C	MC1437	Motorola
10.0	0.05	0.01	8*	4*	13*	25K	80	0	Wideband JFET	µAF772C	Fairchild
	0.20	0.05	10*	3*	13*	25K	70	0	Low Noise Bipolar-FET	**TL072C**	**TI (988)**
		0.10	10*	4*	13*	25K	70	0	Dual 351, wide band	**LF353**	**National (784)**
	500	50	7*	1	0.6	20K	70	0	Single Supply	MC3458	Motorola
	700	300	15*	1.1*	0.5*	20K	60	0	General Purpose	µA1458CC	Fairchild
										MC1458C	Motorola
	1500	600	—	—	—	10K	70	0	Audio Preamp	µA749D	Fairchild
15.0	0.4	0.2	10*	1*	3.5*	3K	70	0	Low Power Bipolar-JFET	**TL062C**	**TI (985)**
				3*	13*	25K	70	0	Bipolar-JFET	**TL082C**	**TI (991)**
										TL083C	**TI (991)**
		800*	—	—	—	32K*	—	0	Audio 5 watts/channel	DA-101	Delco

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Dual Units (Cont'd)											
20.0	0.02	0.0005*	75	1*	6*	50K	70	0	FET Input Dual	8043M	†Intersil
50.0	0.05	0.0005*	75	1*	6*	20K	70	0	FET Input Dual	8043C	Intersil
Triple Units											
2.0	500	250	5*	10*	—	4K	90*	0	Two amplifiers of triple unit, includes 5v regulator	ZN417	Ferranti
3.0	30	7.5	5*	0.27*	0.16*	50K	70	0	Low Power Programmable	8023M	†Intersil
5.0	70	14	—	0.02*	0.1*	—	70	0	Micropower, Transconductance Amplifier	CA3060	†RCA
	200	50	3.3*	0.6*	0.4*	3K	80	0	Programmable	**L144A**	**†Siliconix (982)**
										L144B	**Siliconix (982)**
	550	100	—	0.045*	1*	—	70	0	Micropower, Transconductance Amplifier	CA3060	†RCA
	5000	1000	—	0.11*	8*	—	70	0	Micropower, Transconductance Amplifier	CA3060	†RCA
6.0	30	10	5*	0.27*	0.16*	50K	70	0	Low Power Programmable	8023C	Intersil
7.0	150	50	—	2*	0.7*	20K	70	0	Low Power, Programmable	SL144C	Siltronics
10.0	250	70	3.3*	0.6*	0.4*	1K	70	0	Programmable	**L144C**	**Siliconix (982)**
	2000	200*	—	5	0.46	4K*	90*	2	Supply ±6 v	TCA220	Signetics
20.0	50	25	-	0.5*	-	4K	90*	0	Low input current amplifier of triple unit includes 5v regulator	ZN417	Ferranti
Quad Units											
0.5	300	20	10	1.5	0.7	100K	100	0	Symmetrical, Matched	**OP-09A**	**†PMI (864)**
										OP-09E	**PMI (864)**
										OP-11A	**†PMI (864)**
										OP-11E	**PMI (864)**
2.0	0.10	0.05	10*	4*	13*	50K	80	0	Wideband, Quad 351A	LF347A	National
	50	10	20	1*	—	50K	70	0	Low Power	LM124A	†AMD
										LM124A	†National
										LM124A	Signetics
2.5	200	75	2*	8*	4*	100K	86	0	Wideband	**HA-4602-2**	**†Harris (728)**
	500	50	15	1.5	0.7	100K	100	0	Symmetrical, Matched	**OP-09B**	**†PMI (864)**
										OP-09F	**PMI (864)**
										OP-11B	**†PMI (864)**
										OP-11F	**PMI (864)**
3.0	0.05	0.01	8*	4*	13*	50K	80	0	Wideband JFET	µAF774A	†Fairchild
	0.2	0.05	10*	3*	13*	50K	80	0	Low Noise, Bipolar-JFET	TLO74AM	†TI
										TLO74BC	TI
										TLO75AM	†TI
										TLO75BC	TI
		0.1	10*	1*	3.5*	4K	80	0	Low Power Bipolar-JFET	**TL064AM**	**†TI (985)**
										TLO64BC	TI
				3*	12*	50K	80	0	JFET	**TL084AM**	**†TI (991)**
										TLO84BC	TI
	80	15	20	1*	—	50K	70	0	Low Power	LM224A	AMD
										LM224A	National
										LM224A	Signetics
	100	30	30	1*	—	25K	65	0	Low Power	LM324A	AMD
										LM324A	National
										LM324A	Signetics
	200	30	5*	3	1.2	25K	80	0	Noise 2µV max	**RM4156**	**†Raytheon (971)**

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† Military Temperature Range (−55° to 125°C) * Typical Values

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Quad Units (Cont'd)											
3.0	200	30	5*	(Cont'd.)							
				3.5*	1.6*	50K	80	0	Quad 741	**HA-4741-2**	**† Harris (735)**
										HA4741-2	† Raytheon
3.5	300	100	2*	8*	4*	75K	80	0	Wideband	**HA-4605-5**	**Harris (728)**
4.0	400	50	5*	1*	1.2*	50K	70	0	LM124 with improved output	RM3503A	† Raytheon
5.0	0.10	0.02	8*	4*	13*	50K	80	0	Wideband JFET	µAF774	† Fairchild
										µAF774E	Fairchild
	0.20	0.10	10*	4*	13*	50K	80	0	Wideband, Quad 351B	LF347B	National
	100	10	—	1*	0.4*	50K	70	0	Programmable	XR146	Exar
										LM146	**† National (766)**
		25	—	1*	0.5*	50K	70	0	Quad 741 with standard npn input stage		
										LM148	† AMD
										µA148	Fairchild
										LM148	† Intersil
										LM148	† National
										LM148	† Raytheon
				4*	2.0*	50K	70	0	Wideband quad 741 for gains >5	LM149	† AMD
										LM149	† Intersil
										LM149	† National
										LM149	† Raytheon
		40	—	0.8*	0.5*	4K	60	0	Low Power	TL044M	† TI
	150	30	7*	1*	—	50K	70	0	Single Supply; I/O Operates to ground		
										LM124	† AMD
										LM224	AMD
										µA124	† Fairchild
										LM124	† Intersil
										LM124	† Motorola
										LM224	Motorola
										LM124	† National
										LM224	National
										LM124	† Raytheon
										CA124	† RCA
										LM124	† Signetics
										LM224	Signetics
										SG124	† Silicon G
										LM124	† TI
										LM224	TI
	250	80	—	0.8	0.5*	1K	60	0	Low Power	TL044C	TI
	300	50	5*	3	1.2	25K	80	0	Noise 2µV max	**RC4156**	**Raytheon (971)**
										RV4156	**Raytheon (971)**
				3.5*	1.6*	25K	80	0	Quad 741	**HA-4741-5**	**Harris (735)**
										HA4741-5	Raytheon
	500	50	10*	1*	0.6*	50K	70	0	Single Supply; I/O Operates to ground		
										XR3503	† Exar
										µA3503M	† Fairchild
										MC3503	† Motorola
										RM3503	† Raytheon
									2 op amps, 2 comparators	MC3505	Motorola
			—	2	1.5*	5K	70	0	Programmable Quad 741	XR4202	Exar
										MC4202	Motorola
					1.6*	20K	70	0	Low Noise, Low Power	XR4212M	† Exar
		200	15*	1	0.5*	50K	70	0	Quad 741	MC4741	† Motorola
			—	3*	1.5*	50K	70	0	Quad 741, High Gain	XR4136M	† Exar
										µA4136M	† Fairchild
										PM4136	**† PMI (864)**
										RM4136	† Raytheon
										RM4136	† TI

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Quad Units (Cont'd)											
6.0	0.2	0.05	—	8	20	50K	80	0	FET, wideband	MC3571	†Motorola
			10*	3*	13*	50K	80	0	Low Noise Bipolar-JFET	**TL074AC**	**TI (988)**
										TL074M	**†TI (988)**
										TL075AC	**TI (988)**
										TL075M	†TI
		0.1	10*	1*	3.5*	4K	80	0	Low Power Bipolar-JFET	**TL064C**	**TI (985)**
										TL064M	**†TI (985)**
				3*	13*	50K	80	0	Bipolar JFET	TL084AC	TI
										TL084M	**†TI (991)**
	200	50	—	1*	0.5*	25K	70	0	Quad 741 with standard npn input stage		
										LM248	AMD
										LM348	AMD
										µA248	Fairchild
										µA348	Fairchild
										LM248	Intersil
										LM348	Intersil
										LM248	National
										LM348	National
										LM248	Raytheon
										LM358	Raytheon
				4*	2*	25K	70	0	Wideband quad for gains>5	LM249	AMD
										LM349	AMD
										µA349	Fairchild
										LM249	Intersil
										LM349	Intersil
										LM249	National
										LM349	National
										LM229	Raytheon
										LM329	Raytheon
	500	50	—	1*	1.2*	25K	70	0	LM324 with improved output	RC3403A	†Raytheon
										RV3403A	Raytheon
				2	1.6	5K	70	0	Quad 741	XR4212C	Exar
		100	—	1*	0.4*	25K	70	0	Programmable	XR246	Exar
										XR346	Exar
									Quad 741	**LM246**	**National (766)**
										LM346	**National (766)**
		200	—	3*	1*	20K	60-70	0	Quad 741	XR4136C	Exar
										µA4136C	Fairchild
										µPC4136	NEC America
										PM4136C	**PMI (864)**
										RC4136	Raytheon
										RV4136	Raytheon
										RC4136	†TI
				1*	0.5*	20K	70	0	Quad 741	MC4741C	Motorola
7.0	250	50	7*	1*	—	25K	65	0	Single Supply; I/O Operates to ground		
										LM324	AMD
										µA224	Fairchild
										µA324	Fairchild
										LM224	Intersil
										LM324	Intersil
										LM324	Motorola
										LM324	National
										CA224	RCA
										CA324	RCA
										LM224	Raytheon
										LM324	Raytheon
										LM224	Signetics
										LM324	Signetics
										SA534	Signetics
										SG224	Silicon G
										SG324	Silicon G
										LM224	TI

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Quad Units (Cont'd)											
7.0	250	50	7*	1*	—	25K	65	0	Single Supply; I/O Operates to ground	(Cont'd.) LM324	TI
						100K*	50	0	Single Supply	LM2902	National
	500	50	—	—	—	100K*	85*	0	324 type	µPC324 µPC451	NEC America NEC America
7.5	500	50	—	1*	—	100K*	85*	0	Single supply, 324 type	TDA0324	Signetics
8.0	500	75	10*	1*	0.6*	20K	70	0	Single Supply: I/O Operates to ground	XR3303 µA330C MC3303	Exar Fairchild Motorola
10.0	0.20	0.05	8*	4*	13*	25K	70	0	Wideband JFET	µAF774C	Fairchild
			10*	3*	13*	25K	70	0	Low Noise Bipolar-JFET	**TL074C** **TL075C**	**TI (988)** **TI (988)**
			0.10	4*	13*	25K	70	0	Bipolar-JFET, Quad 351	**LF347**	**National (764)**
	500	50	10*	1*	0.6*	20K	70	0	Single Supply; I/O Operates to ground	XR3403 µA3403 MC3403 RC3403	Exar Fairchild Motorola Raytheon
									2 op amps, 2 comparators	MC3405	Motorola
			—	1*	2*	15K	70	0	LM224 with improved output	RV3403A	Raytheon
				—	—	100K	85*	0	Extended Temp LM224	LM2902 LM2902 LM2902 LM2902	Motorola Raytheon Signetics TI
	600	300	—	3*	1*	15K	60	0	Quad 741	RC4136C RC4136C	Raytheon TI
15.0	0.20	0.05	—	7*	20	25K	70	0	FET, wideband	MC3471	Motorola
	0.40	0.2	10*	1*	3.5*	3K	70	0	Low Power Bipolar-JFET	**TL064C**	**TI (985)**
				3*	13*	25K	70	0	Bipolar FET	**TL084C**	**TI (991)**
—	100	—	—	2.5*	0.5/20*	2K	—	0	Current Mirror, Single Supply	LM1900	†National
	200	—	—	2.5*	0.5/20*	1.2K	—	0	Current Mirror, Single Supply	LM2900 LM3900 LM2900 LM3900	National National Raytheon Raytheon
	300	—	—	4*	0.6*	1K	—	0	Current Mirror, Single Supply	µA3301C MC3301 RC3301	Fairchild Motorola Raytheon
				2.5*	0.5/20*	1.2K	—	0	Current Mirror, Single Supply	LM3301 LM3401	National National
				5*	0.6*	1K	—	0	Current Mirror, Single Supply	µA3401C MC3401 CA3401 RC3401	Fairchild Motorola †RCA Raytheon

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Phase Locked Loops/Synthesizers

Phase Locked Loop Circuits

Note: Stereo Decoders are listed under Consumer Circuits

Function	Device	Source	Line
Counter Logic Control	SP8790	Plessey	
Counter Control Logic (Use with MC12012 for high frequency programming)	MC12014	Motorola	
Crystal Oscillator (0.1 to 2.0 MHz)	MC12060	Motorola	
	MC12560	† Motorola	10
Crystal Oscillator (2 to 20 MHz)	MC12061	Motorola	
	MC12561	† Motorola	
Current Controlled Oscillator and Phase Comparator	**HA-2820**	**† Harris (750)**	
	HA-2825	**Harris (750)**	
Digital Mixer	MC12000	Motorola	
Double Balanced Mixer	MC12002	Motorola	20
	MC12502	† Motorola	
FSK Modulator/Demodulator	XR210	Exar	
	XR210M	† Exar	
	XR2211	† Exar	
	XR2211M	† Exar	
	XR2211C	Exar	
	XR2211C	Raytheon	
	XR2211M	† Raytheon	
Offset Control System (for synthesizer tuned transceivers)	MC12020	Motorola	30
	MC12021	Motorola	
	MC12520	† Motorola	
	MC12521	Motorola	
Phase Comparator and Programmable Counter	MC14568BA	† Motorola	
	MC14568BC	Motorola	
Phase Frequency Detector	11C44C	Fairchild	40
	MC4044	Motorola	
	MC4344	† Motorola	
	MC12040	Motorola	
	MC12540	† Motorola	
Phase Locked Loop	XR215	Exar	
	XR215M	† Exar	
	M5136	Mitsubishi	
	M51361	Mitsubishi	
	SL652	Plessey	50
	NE564	Signetics	
Phase Locked Loop (CMOS)	F4046BC	Fairchild	
	F4046BM	† Fairchild	
	SIL4046B	† Mitel	
	SIL4046BE	Mitel	
	MC14046BA	† Motorola	
	MC14046BM	Motorola	
	CD4046BC	National	
	CD4046BM	† National	60
	CD4046B	† RCA	
	CD4046BE	RCA	
	SCL4046B	† SSS	
	SCL4046BE	SSS	
	SCL4446	SSS	

Phase Locked Loop Circuits (Cont'd)

Function	Device	Source	Line
Phase Locked Loop Control (Oscillator, programmable divider, phase comparator	SP8760	Plessey	
PLL Peripheral (VCO, mixer, amp for CB)	LM1861	National	70
	LM1862	National	
	AN103	Panasonic	
Prescaler, for FM radio	DS8629	National	
Programmers and Controllers for Citizens Band See Linear Consumer Circuits			
Programmer, for CB Synthesizer	MM57190	National	
Synthesizer, 200 channel, for AM/FM	8X08	Signetics	80
Synthesizer (Programmable Divider, to 1021 channels, adder, phase comparator)	HCTR0320	Hughes	
Synthesizer, Citizens Band	11C84	Fairchild	
	HCTR0347	Hughes	
	MPS7139	Micro Power	
	MPS7149	Micro Power	
	MC3390	Motorola	
	MC145104	Motorola	90
	MC145106	Motorola	
	MC145107	Motorola	
	MC145109	Motorola	
	MC145112	Motorola	
	DS8900	National	
	LM1861	National	
	LM1862	National	
	MM55104	National	
	MM55106	National	
	MM55107	National	100
	MM55108	National	
	MM55109	National	
	MM55110	National	
	MM55114	National	
	MM55116	National	
	μPD861	NEC America	
	NC6400A	Nitron	
	NC6402A	Nitron	
	NC6403	Nitron	
	NC6405A	Nitron	110
	MN6040	Panasonic	
	MN6040A	Panasonic	
	MN6040B	Panasonic	
	SP8920	Plessey	
	SP8921	Plessey	
	SP8922	Plessey	
	SP8923	Plessey	
	TA10336	RCA	
	LC7110	Sanyo	
	NE575	Signetics	120
Synthesizer, CB/Marine Radio, to 82 channels	NC6400	Nitron	
	NC6405A	Nitron	
Synthesizer, T.V., dual 82 channels	NC6410A	Nitron	
Synthesizer, Fixed or Programmable	CRC8100	Rockwell	
Synthesizer, Externally Programmable	NC6423	Nitron	

Phase Locked Loop Circuits (Cont'd)

Function	Device	Source	Line
Synthesizer (Programmable Dividers, Phase Comparator)	S187	Siemens	130
Tone Decoder	XR567C	Exar	
	XR567M	† Exar	
	XR2211C	Exar	
	XR2211M	† Exar	
	LM567	† National	
	LM567C	National	
	XR2211C	Raytheon	140
	XR2211M	† Raytheon	
	NE567	Signetics	
	SE567	† Signetics	
Dual Tone Decoder	XR2567C	Exar	
	XR2567M	† Exar	
	XR2567C	Raytheon	
	XR2567M	† Raytheon	
Dual Tone Decoder/Receiver	MT8820A	† Mitel	150
	MT8820AE	Mitel	
Tone Generator	FX205	CMA	
Two Modulus Prescaler (÷3/4)	SP8720	Plessey	
	SP8725	Plessey	
Two Modulus Prescaler (÷5/6)	11C91C	Fairchild	
	11C91M	† Fairchild	
	95H91C	Fairchild	160
	95H91M	† Fairchild	
	MC12009	Motorola	
	MC12509	† Motorola	
	SP8740	Plessey	
	SP8745	Plessey	
Two Modulus Prescaler (÷6/7)	SP8741	Plessey	
	SP8746	Plessey	
Two Modulus Prescaler (÷8/9)	MC12011	Motorola	170
	MC12511	† Motorola	
	SP8743	Plessey	
	SP8748	Plessey	
Two Modulus Prescaler (÷10/11)	11C90C	Fairchild	
	11C90M	† Fairchild	
	95H90C	Fairchild	
	95H90M	† Fairchild	
	MC12013	Motorola	
	MC12513	† Motorola	180
	SP8640	Plessey	
	SP8641	Plessey	
	SP8642	Plessey	
	SP8643	Plessey	
	SP8646	Plessey	
	SP8647	Plessey	
	SP8685	Plessey	
	SP8690	Plessey	
	SP8695	Plessey	
Two Modulus Prescaler (÷5/6, 10/11, 10/12)	MC12012	Motorola	190
Two Modulus Prescaler (÷248/256)	11C83	Fairchild	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Phase Locked Loops/Synthesizers (Cont'd)

Phase Locked Loop Circuits (Cont'd)

Function	Device	Source	Line
Count Extender, ÷8 (extends division ratio of a Two Modulus Prescaler while retaining the difference, ie÷10/11 becomes ÷80/81)	SP8794A	†Plessey	
	SP8794B	Plessey	
	SP8794M	Plessey	
Count Extender, ÷4, ÷10/11 becomes ÷40/41	SP8790A	†Plessey	
	SP8790B	Plessey	
	SP8790M	Plessey	
For other Prescalers see Digital Special, Dividers			
VCO	11C58C	Fairchild	10
	MC1648	†Motorola	
	MC1658	Motorola	
	SP1648	Plessey	
	SP1658	Plessey	
	SN74LS320	TI	
	SN54LS324	†TI	
	SN74LS324	TI	
VCO and Phase Comparator	LM565	Motorola	
	LM565	National	20
	LM565C	†National	
	NE560	Signetics	
	SE560	†Signetics	
	NE561	Signetics	
	SE561	†Signetics	
	NE562	Signetics	
	SE562	†Signetics	
	NE565	Signetics	
	SE565	†Signetics	
	TA7133	Toshiba	30
VCO Function Generator, (Includes square and triangular waveforms but not sine.)	XR2207	Exar	
	XR2207C	Exar	
	XR2209C	Exar	
	XR2209M	†Exar	
	LM566	National	
	LM566C	†National	
	XR2207C	Raytheon	
	XR2207M	†Raytheon	40
	NE566	Signetics	
	SE566	†Signetics	
VCO Waveform Generator (pulse, sawtooth and triangle)	SSM2030	SSM	
VCO Waveform Generator (Includes sinewave output among its functions)	XR205	Exar	
	XR2206	†Exar	
	XR2206C	Exar	50
	XR2206M	†Exar	
	XR8038	Exar	
	XR3038M	†Exar	
	8038C	Intersil	
	8038M	†Intersil	
VCO, Amplifier, Analog Multiplier	XR-S200	Exar	
	XR205	Exar	
VCO, Phase Comparator, Multiplier	SL651	Plessey	60
VCO, Phase Comparator Multiplier, with Auxiliary Amplifier	SL650	†Plessey	

Phase Locked Loop Circuits (Cont'd)

Function	Device	Source	Line
Dual VCO	11C24C	Fairchild	
	MC4024	Motorola	
	MC4324	†Motorola	
	SN54LS124	†TI	
	SN54S124	†TI	
	SN74LS124	TI	70
	SN74S124	TI	
	SN54LS325	TI	
	SN74LS325	TI	
	SN54LS326	†TI	
	SN74LS326	TI	
	SN54LS327	†TI	
	SN74LS327	TI	

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Telecommunication Circuits

Telecommunication Circuits

Function	Device	Source	Line
Address Selector (Gives output if sequential input is entered in a fixed order within a maximum time interval)	7511-01	Telenetics	
Baseband Modulator/Demodulator (50db carrier suppression)	SL1001	Plessey	
Baseband Channel Amplifier (24 27db amplifier)	SL1020	Plessey	
Coin box Circuit (Coin recognition for pay telephones)	AY5-9300	GI	10
Codec, μ255 Law	**S2563**	**AMI** (380)	
	DF331	**Siliconix** (979)	
	DF332	**Siliconix** (979)	
Codec, A Law	**DF341**	**Siliconix** (978)	
	DF342	**Siliconix** (978)	
Compander (Signal Compressor/Expander)	XR2216	Exar	20
	LM2704	National	
	LM2705	National	
	LM2706	National	
	LM2707	National	
	LS3704	National	
	LM3705	National	
	LM3706	National	
	LM3707	National	
	L150	SGS	
	NE570	Signetics	30
	NE571	Signetics	
Companding Analog to Digital Converter	MN5110	Micro Net	
	NC331	Nitron	
	DF331	**Siliconix** (979)	
	DF341	**Siliconix** (978)	
Companding Digital to Analog Converter	NC332	Nitron	
	DAC-86	**PMI** (935)	
	DAC-87	**PMI** (935)	40
	ST100	Signetics	
	DF332	**Siliconix** (979)	
	DF342	**Siliconix** (978)	
Companding A/D and D/A Converter	LF2700	National	
	MM8100	National	
Delta Modulation System, Continuously Variable Slope	FX209	CMA	
	FX309	CMA	
	HC55516-2	**†Harris** (754)	50
	HC55516-8	**†Harris** (754)	
	HC55516-9	**Harris** (754)	
	HC55532-2	**†Harris** (754)	
	HC55532-8	**†Harris** (754)	
	HC55532-9	**Harris** (754)	
	MC3417	Motorola	
	MC3418	Motorola	
Dialer, Push Button Telephone Dialer Circuit (Converts push button inputs to pulses)	**S2560**	**AMI** (374)	60
	AY5-9100	GI	
	AY5-9106	GI	
	AY5-9110	GI	
	AY5-9118	GI	
	AY5-9120	GI	
	SAH215	ITT	

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Telecommunication Circuits (Cont'd)

Function	Device	Source	Line
Dialer, Push Button Telephone Dialer Circuit (Converts push button inputs to pulses) (Cont'd.)	MC14408	Motorola	
	MC14409	Motorola	70
	MM5393	National	
	NC320	Nitron	
	NC321	Nitron	
	NC322	Nitron	
	CRC8000	Rockwell	
	CRC8001	Rockwell	
	DF320	**Siliconix** (977)	
	DF321	**Siliconix** (977)	
	DF322	**Siliconix** (977)	
Dialer, Repertory	**S2562**	**AMI** (378)	
	AY5-9200	GI	
(Dialer) Clock Generator (for AY5 9100/9200)	AY5-9500	GI	
Tone Decoder (Three tone, 8 combinations sequential code receiver)	FX307	CMA	90
Tone Decoder (Operates from 0.01 Hz to 500 kHz)	XR567	†Exar	
	XR567C	Exar	
	XR2211C	Exar	
	XR2211M	†Exar	
	LM567	†National	
	LM567C	National	
	NC8030	Nitron	
	XR2211C	Raytheon	
	XR2211M	†Raytheon	100
	NE567	Signetics	
	SE567	†Signetics	
Dual Tone Decoder (Operates from 0.01 Hz to 500 kHz)	XR2567	Exar	
	XR2567M	†Exar	
	XR2567C	Raytheon	
	XR2567M	†Raytheon	
Dual Tone Decoder	AY5-9801	GI	110
	AY5-9802	GI	
	AY5-9803	GI	
	AY5-9804	GI	
	AY5-9822	GI	
	AY5-9805	GI	
	AY5-9806	GI	
	AY5-9807	GI	
	AY5-9808	GI	
	AY5-9821	GI	
	AY5-9822	GI	120
	AY5-9823	GI	
	AY5-9824	GI	
	AY5-9825	GI	
	AY5-9826	GI	
	AY5-9827	GI	
	AY5-9828	GI	
	MT8820	Mitel	
	CRC8030	Rockwell	
	7516-01	Telenetics	
Dual Tone Receiver Circuit (combine with filters for touch tone receiver)	MT8820	Mitel	130
	AF104	National	
	AF106	National	
	AF107	National	
	AF108	National	

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Telecommunication Circuits (Cont'd)

Function	Device	Source	Line
Dual Tone Receiver Circuit (combine with filters for touch tone receiver) (Cont'd.)	AF110	National	
Quad Tone Decoder	883-5	Beckman	140
Tone Ringer (operates from ring signal, drives speaker)	**S2561**	**AMI** (376)	
Relay Driver (For 48v telephone relays)	DS1686	†National	
	DS1687	†National	
	DS3686	National	
	DS3687	National	
Encoder 2 of 8 keyboard to Binary Encoder (4 x 4 Key Input to 4 line output)	MC14419	Motorola	150
Low Pass Filter, 3825Hz	ACF7110C	GI	
Bandpass (touchtone) Filters	883-X	†Beckman	
	CH1295	Cermetek	
	CH1296	Cermetek	
	ACF7323C	GI	
	ACF7363C	GI	160
	ACF7383	GI	
	ACF7711C	GI	
	AF101	National	
	AF102	National	
	AF103	National	
	AF111	National	
	AF112	National	
	AF113	National	
	AF114	National	
Bandpass Filters	ACF7310C	GI	170
	ACF7311C	GI	
	ACF7320C	GI	
	AF99	National	
Bandpass Filter and Detector	ACF7300C	GI	
	ACF7301C	GI	
	ACF7302C	GI	
Filter, Dial Tone Suppression	ACF7401C	GI	180
Filter, 2600Hz Suppression	ACF7410C	GI	
Filter, 60Hz Suppression	ACF7480C	GI	
Filter, PCM	ACF7170C	GI	
	ACF7173C	GI	
	ACF7174C	GI	
	ACF7175C	GI	
	ACF7176C	GI	190
Dual Tone Generator (Touchtone Frequencies)	**S2559**	**AMI** (372)	
	ICM7206	Intersil	
	MK5085-1	Mostek	
	MK5085-2	Mostek	
	MK5086-1	Mostek	
	MK5086-2	Mostek	
	MK5089	Mostek	
	MC14410	Motorola	
	MM5395	National	200
	7601-01	Telenetics	

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† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Telecommunication Circuits (Cont'd)

Function	Device	Source	Line
Telecommunication Circuits (Cont'd)			
Dual Tone Generator (Touchtone Frequencies) (Cont'd.)	7603-02	Telenetics	
Dual Tone Generator (Generates 12 16 tone pairs)	AY3-9400	GI	
	AY3-9401	GI	
	AY3-9410	GI	
Gyrator	TCA580	Signetics	
	AF120	National	
Dual Limiter (Touchtone Amplitude Limiter)	883-4	Beckman	10
Modem, Frequency Division Multiplex Transmitter and Receiver	LM1823	National	
	LM1826	National	
Modem (Frequency Shift Keying Modulator/Demodulator)	XR210	Exar	
	XR210M	†Exar	
	MC14412	Motorola	20
Modem, FSK Modulator	XR2206	Exar	
	XR2206M	†Exar	
	XR2207	Exar	
	XR2207M	†Exar	
Modem, FSK Demodulator	XR2211	Exar	
	XR2211M	†Exar	
Modem (For Serial Communications at up to 600 bps)	S6860	AMI	30
	MC6860	Motorola	
Modem Circuits, for 103/113 and other FSK systems	CH1213	Cermetek	
	CH1214	Cermetek	
	CH1223	Cermetek	
	CH1224	Cermetek	
	CH1252	Cermetek	
	CH1257	Cermetek	
	CH1262	Cermetek	
	CH1267	Cermetek	40
	CH1273	Cermetek	
	CH1280	Cermetek	
Modem Circuits, for CCITT FSK System	CH1215	Cermetek	
	CH1216	Cermetek	
	CH1225	Cermetek	
	CH1226	Cermetek	
	CH1253	Cermetek	
	CH1258	Cermetek	
	CH1263	Cermetek	50
	CH1268	Cermetek	
	CH1271	Cermetek	
	CH1276	Cermetek	
Digital Filter Switch (Tone Decoder)	FX105	CMA	
Frequency Sensitive Switch (Provides two set points adjustable with external components.)	FX101	CMA	
Frequency Sensitive Switch (Provides set points with widely adjustable hysteresis)	FX301	CMA	60
Frequency Sensitive Switch (Provides two set points and three state outputs)	FX401	CMA	

Function	Device	Source	Line
Telecommunication Circuits (Cont'd)			
Tone Operated Switch (Bistable tone operated switch)	FX501	CMA	
Tone Operated Monostable Timer (Tone operated for remote switching)	FX601	CMA	
Tone Transmitter (Three tone sequential code transmitter)	FX207	CMA	70
Tone Transceiver (Decodes and encodes 5 sequential tones)	FX407	CMA	
	FX507	CMA	
Tone Transceiver Code Selector (Programs 3 codes for FX407/507)	FX707	CMA	
Tone Transceiver (Single tone transmitter receiver simplex.)	FX107	CMA	80
Crosspoint Array (Double 4 x 4 switch matrix)	MC3466	Motorola	
	RC4444	Raytheon	
	RM4444	Raytheon	
Crosspoint Array (4 x 4 switch matrix)	CD22100	RCA	
Crosspoint Array (8 x 2 switch matrix)	SD5301	Signetics	90
Crosspoint Array (8x4 switch matrix)	MT8804B	†Mitel	
	MT8804BE	Mitel	

Function	Device	Source	Line

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Timers

Timers

Function	Device	Source	Line
Timer			
	NE555	†AMD	
	SE555	AMD	
	XR555C	Exar	
	XR555M	†Exar	
	µA555C	Fairchild	
	NE555	Intersil	
	SE555	†Intersil	
	MCC555	Micro Comp	
	M51843	Mitsubishi	10
	MC1455	Motorola	
	MC1555	†Motorola	
	LM555C	National	
	LM555M	†National	
	µPC1555	NEC America	
	RC555	Raytheon	
	RM555	†Raytheon	
	CA555	†RCA	
	CA555C	RCA	
	NE555	Signetics	20
	SE555	†Signetics	
	TDA0555	Signetics	
	SA555	Signetics	
	SG555	†Silicon G	
	SG555C	Silicon G	
	ULN-3303	Sprague	
	ULN-3304	Sprague	
	355A/C	Teledyne S	
	355B/M	†Teledyne S	
	SE555	†TI	30
	NE555	TI	
Timer, Adjustable Threshold			
	MC1422	Motorola	
Timer, delayed switch ON/OFF (for driving relays, lamps, etc.)			
	PBA3008	RIFA	
	PBA3009	RIFA	
Timer, Detector/Timer, LED Driver, audio oscillator			
	MD4301	Mitel	
Timer, Industrial, with ÷5, ÷6, ÷10, ÷4096 counters, 1 Hz output			40
	CD22017	RCA	
Timer, Internal Current Source			
	XR320	Exar	
	XR320M	†Exar	
Timer, Low Power (Supply 3v)			
	SN76812	TI	
Timer/Microwave Oven Controller			
	TMS1117	TI	
Timer, Precision			50
	ZN1034E	Ferranti	
	LM122	†National	
	LM222	National	
	LM322	National	
	LM2905	National	
	LM3905	National	
Timer with Counter, (time constant 128 RC)			
	XR2242C	Exar	
	XR2242M	†Exar	
Timer, Programmable (includes a counter for long time delays) Binary Control			60
	XR2240C	Exar	
	XR2240M	†Exar	
	µA2240	Fairchild	
	8240	Intersil	
	MC14541BA	†Motorola	

(Continued)

Timers (Cont'd)

Function	Device	Source	Line
Timer, Programmable (includes a counter for long time delays) Binary Control (Cont'd.)			
	MC14541BC	Motorola	
	µA2240C	TI	70
	µA2240M	†TI	
Timer, Programmable (includes counter) Decimal Control			
	8250	Intersil	
Timer, Programmable (includes counter) Hours/Minutes/Seconds Control			
	8260	Intersil	
Dual Timer (dual 555)			
	NE556	AMD	
	SE556	†AMD	80
	XR556C	Exar	
	XR556M	†Exar	
	µA556	Fairchild	
	NE556	Intersil	
	SE556	†Intersil	
	MC3456	Motorola	
	MC3556	†Motorola	
	LM556	†National	
	LM556C	National	
	RC556	Raytheon	90
	RM556	†Raytheon	
	NE556	Signetics	
	SE556	†Signetics	
	SA556	Signetics	
	SG556	†Silicon G	
	SG556C	Silicon G	
Dual Timer (dual 555), pinout variations			
	XR2556C	Exar	
	XR2556M	†Exar	
Dual Set Point Timer (includes timer, selectable time range)			100
	DF215	**Siliconix**	**(981)**
Universal Timer (includes two 4 digit counters, comparator, clock oscillator and divider)			
	MM5865	National	
Dual Monostable Timer			
	FX109	CMA	
Quad Timer, Current Sink Output			
	NE558	Signetics	
	SA558	Signetics	110
	SE558	†Signetics	
Quad Timer, Current Source Output			
	NE559	Signetics	
	SA559	Signetics	
	SE559	†Signetics	
Tone Triggered Timer			
	FX601	CMA	
Other Timer Circuits: See Linear Consumer Circuits, Appliance Timers; Clocks; Watches; Stopwatches; T.V. Timers and Digital CMOS Oscillators/Dividers			120

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators

Fixed, Positive

The output current listed is the maximum current for which load regulation is specified

Output Voltage	Output Current	Device	Source	Line
2.6	100 ma	µA78L26C	Fairchild	
		MC78L02C	Motorola	
		µA78L02C	Signetics	
		µA78L02C	TI	
5	100 ma	µA78L05C	Fairchild	
		MC78L05C	Motorola	
		LM140LA-5	**National (806)**	
		LM240LA-5	National	10
		LM340LA-5	**National (806)**	
		LM78L05C	National	
		µPC78L05	NEC America	
		µA78L05C	Signetics	
		µA78L05C	TI	
	200 ma	LM109G	Motorola	
		LM209G	Motorola	
		LM309G	Motorola	
		LH0075	National	
		LM109H	† National	20
		LM209H	National	
		LM309H	National	
		LM342-5	National	
		SFC2109	† NPC	
		SFC2209	NPC	
		SFC2309	NPC	
		TBA625A	Plessey	
		LM109H	† Raytheon	
		LM209H	Raytheon	
		LM309H	Raytheon	30
		LM209DB	Signetics	
		LM309DB	Signetics	
		SG109T	† Silicon G	
		SG209T	Silicon G	
		SG309T	Silicon G	
		LM109	† TI	
		LM209	TI	
		LM309	TI	
	500 ma	805-V5	† Beckman	
		µA78C05C	Fairchild	40
		µA78M05C	Fairchild	
		µA78M05M	† Fairchild	
		TDD1605	ITT	
		MC7705C	Motorola	
		MC78M05C	Motorola	
		LM341-5	National	
		LM78M05	National	
		µPC78M05	NEC America	
		LM109DA	† Signetics	
		LM209DA	Signetics	50
		LM309DA	Signetics	
		µA78M05	† Signetics	
		µA78M05C	Signetics	
		µA78MHV05	† Signetics	
		µA78MHV05C	Signetics	
		SG7805AT	† Silicon G	
		SG7805ACT	Silicon G	
		µA78M05C	TI	
		µA78M05M	† TI	
	600 ma	L005T1	SGS	60
	750 ma	809-V5	† Beckman	
	850 ma	L129	SGS	
	1 a	µA109M	† Fairchild	
		µA209M	Fairchild	
		µA309C	Fairchild	
		LM109	† Motorola	

(Continued)

Fixed, Positive (Cont'd)

Output Voltage	Output Current	Device	Source	Line
5	1 a	(Cont'd.)		
		LM209K	Motorola	
		LM309	Motorola	
		MC7805C	Motorola	70
		LM109K	† National	
		LM209K	National	
		LM309K	National	
		SFC2109M	NPC	
		LM109K	† Raytheon	
		LM209K	Raytheon	
		LM309K	Raytheon	
		LM209DA	Signetics	
		LM309DA	Signetics	
		SG109K	† Silicon G	80
		SG209K	Silicon G	
		SG309K	Silicon G	
		SG7805AR	† Silicon G	
		SG7805ACR	Silicon G	
		SG7805CR	† Silicon G	
		SG7805R	Silicon G	
	1.2 a	SI3551M	Sanken	
	1.5 a	µA7805C	Fairchild	
		µA7805M	† Fairchild	
		LAS1505	Lambda	90
		LM140-5	**† National (806)**	
		LM140A-5	**† National (806)**	
		LM340-5	**National (806)**	
		LM340A-5	**National (806)**	
		LM7805	National	
		µPC14305	NEC America	
		LM109DB	† Signetics	
		LM209DB	Signetics	
		LM309DB	Signetics	
		µA7805	† Signetics	100
		µA7805C	Signetics	
		µA78HV05	Signetics	
		LM340-5	Signetics	
		SG7805AK	† Silicon G	
		SG7805ACK	Silicon G	
		SG7805ACP	Silicon G	
		SG7805CK	Silicon G	
		SG7805CP	Silicon G	
		SG7805K	† Silicon G	
		LM340-5	TI	110
		TL7805AC	TI	
		TL7805C	TI	
		µA7805M	† TI	
	2 a	SI3150G	Sanken	
		SI3552M	Sanken	
	3 a	µA233	Fairchild	
		SH0323	Fairchild	
		LM123	Motorola	
		LM323	Motorola	
		LAS1405	Lambda	120
		LM123	† National	
		LM223	National	
		LM323	National	
		SI3554M	Sanken	
		SG123	† Silicon G	
		SG223	Silicon G	
		SG323	Silicon G	
	5 a	µA78H05	Fairchild	
		LAS1905	Lambda	
		42050-055	Micropac	130
	10 a	42050-510	Micropac	

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Voltage Regulators (Cont'd)

Output Voltage	Output Current	Device	Source	Line
Fixed, Positive (Cont'd)				
6	100 ma	**LM140LA-6**	**National (806)**	
		LM240LA-6	National	
		LM340LA-6	**National (806)**	
		LM78L06C	National	
	200 ma	PC521	† GI	
		LH0075	National	
		LM342-6	National	
	500 ma	805-V6	† Beckman	
		µA78C06C	Fairchild	
		µA78M06C	Fairchild	10
		µA78M06M	† Fairchild	
		TDD1606	ITT	
		MC7706C	Motorola	
		MC78M06C	Motorola	
		LM341-6	National	
		LM78M06	National	
		SG7806AT	† Silicon G	
		SG7806ACT	Silicon G	
		SG7806T	† Silicon G	
		SG7806CT	Silicon G	20
		µA78M06C	Signetics	
		µA78M06M	† Signetics	
		µA78MHV06	† Signetics	
		µA78MHV06C	Signetics	
		µA78M06C	TI	
		µA78M06M	† TI	
	750 ma	809-V6	† Beckman	
	1 a	SG7806ACR	Silicon G	
		SG7806AR	† Silicon G	
		SG7806CR	Silicon G	30
		SG7806R	† Silicon G	
	1.5 a	µA7806C	Fairchild	
		µA7806M	† Fairchild	
		LAS1506	Lambda	
		MC7806C	Motorola	
		LM140-6	**† National (806)**	
		LM140A-6	**† National (806)**	
		LM340-6	**National (806)**	
		LM340A-6	**National (806)**	
		LM7806	National	40
		SG7806AK	† Silicon G	
		SG7806ACK	Silicon G	
		SG7806CK	Silicon G	
		SG7806K	† Silicon G	
		SG7806ACP	Silicon G	
		SG7806CP	Silicon G	
		µA78HV06	Signetics	
		µA7806	† Signetics	
		µA7806C	Signetics	
		LM340-6	Signetics	50
		LM340-6	TI	
		µA7806C	TI	
		µA7806M	† TI	
	2 a	CJSE017	Solitron	
		CJSE019	Solitron	
		CJSE021	Solitron	
	3 a	LAS1406	Lambda	
	10 a	42050-610	Micropac	
6.2	100 ma	µA78L62C	Fairchild	
		µA78L06C	Signetics	
		µA78L06C	TI	60
7	10 a	42050-710	Micropac	
8	100 ma	DVR-8	Delco	
		µA78L08C	Fairchild	

(Continued)

Output Voltage	Output Current	Device	Source	Line
Fixed, Positive (Cont'd)				
8	100 ma	(Cont'd.)		
		MC78L08C	Motorola	
		LM140LA-8	**† National (806)**	
		LM240LA-8	National	
		LM340LA-8	**National (806)**	
		LM78L08C	National	70
		µPC78L08	NEC America	
		µA78L08	TI	
	200 ma	LH0075	National	
		LM342-8	National	
	500 ma	**µA78C08C**	**Fairchild (635)**	
		µA78M08C	Fairchild	
		µA78M08M	† Fairchild	
		MC7708C	Motorola	
		MC78M08C	Motorola	
		LM341-8	National	80
		LM78M08	National	
		µPC78M08	NEC America	
		µA78M08C	Signetics	
		µA78M08M	† Signetics	
		µA78MHV08	Signetics	
		µA78MHV08C	† Signetics	
		SG7808AT	† Silicon G	
		SG7808ACT	Silicon G	
		SG7808T	† Silicon G	
		SG7808CT	Silicon G	90
		µA78M08C	TI	
		µA78M08M	† TI	
	1 a	SG7808AR	† Silicon G	
		SG7808ACR	Silicon G	
		SG7808R	† Silicon G	
		SG7808CR	Silicon G	
	1.5 a	µA7808C	Fairchild	
		µA7808M	† Fairchild	
		LAS1508	Lambda	
		MC7808C	Motorola	100
		LM140-8	**† National (806)**	
		LM140A-8	**† National (806)**	
		LM340-8	**National (806)**	
		LM340A-8	**National (806)**	
		LM7808	National	
		µPC14308	NEC America	
		µA7808	† Signetics	
		µA7808C	Signetics	
		µA78HV08	Signetics	
		LM340-8	Signetics	110
		SG7808AK	† Silicon G	
		SG7808ACK	Silicon G	
		SG7808CK	Silicon G	
		SG7808K	† Silicon G	
		SL7808ACP	Silicon G	
		SL7808CP	Silicon G	
		LM340-8	TI	
		µA7808M	† TI	
		µA7808C	TI	
	3 a	LAS1408	Lambda	120
	10 a	42050-810	Micropac	
8.2	100 ma	**µA78C82C**	**Fairchild (635)**	
		µA78L82C	Fairchild	
8.5	200 ma	TBA435	Plessey	
	500 ma	TDD1608	ITT	
	1 a	µA7885	Fairchild	
		µA7885C	TI	
		µA7885M	† TI	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Fixed, Positive (Cont'd)

Output Voltage	Output Current	Device	Source	Line
9	100 ma	µA78L09C	Fairchild	
	500 ma	801-V9	† Beckman	
	750 ma	809-V9	† Beckman	
10	100 ma	**LM140LA-10**	**† National (806)**	
		LM240LA-10	National	
		LM340LA-10	**National (806)**	
		LM78L10C	National	
	200 ma	LH0075	National	
		LM342-10	National	
	500 ma	**µA78C10C**	**Fairchild (635)**	10
		TDD1610	ITT	
		LM78M10	National	
	1.5 a	LAS1510	Lambda	
		LM140-10	**† National (806)**	
		LM140A-10	**† National (806)**	
		LM340-10	**National (806)**	
		LM340A-10	**National (806)**	
		LM7810	National	
		LM340-10	TI	
	3 a	LAS1410	Lambda	20
	9 a	42050-109	Micropac	
12	100 ma	µA78L12C	Fairchild	
		MC78L12C	Motorola	
		LM140LA-12	**† National (806)**	
		LM240LA-12	National	
		LM340LA-12	**National (806)**	
		LM78L12C	National	
		µPC78L12	NEC America	
		µA78L12C	Signetics	
		µA78L12C	TI	30
	200 ma	PC501	† GI	
		LH0075	National	
		LM342-12	National	
		TBA625B	Plessey	
	500 ma	801-V12	† Beckman	
		µA78C12C	**Fairchild (635)**	
		µA78M12C	Fairchild	
		µA78M12M	† Fairchild	
		TDD1612	ITT	
		MC7712C	Motorola	40
		MC78M12C	Motorola	
		LM341-12	National	
		LM78M12	National	
		µPC78M12	NEC America	
		L036T1	SGS	
		SG7812AT	† Silicon G	
		SG7812CT	Silicon G	
		SG7812T	† Silicon G	
		µA78M12C	Signetics	
		µA78M12M	† Signetics	50
		µA78MHV12	† Signetics	
		µA78MHV12C	Signetics	
		µA78M12M	† TI	
		µA78M12C	TI	
	720 ma	L130	SGS	
	750 ma	809-V12	† Beckman	
	1 a	SI3120E	Sanken	
		SI3120T	Sanken	
		STK521	Sanyo	
		STK541	Sanyo	60
		SG7812AR	† Silicon G	
		SG7812ACR	Silicon G	
		SG7812CR	Silicon G	

(Continued)

Fixed, Positive (Cont'd)

Output Voltage	Output Current	Device	Source	Line
12	1 a	(Cont'd.)		
		SG7812R	† Silicon G	
	1.5 a	µA7812C	Fairchild	
		µA7812M	† Fairchild	
		LAS1512	Lambda	
		MC7812C	Motorola	
		LM140-12	**† National (806)**	70
		LM140A-12	**† National (806)**	
		LM340-12	**National (806)**	
		LM340A-12	**National (806)**	
		LM7812	National	
		µPC14312	NEC America	
		SI3120G	Sanken	
		SI3120M	Sanken	
		µA7812	† Signetics	
		µA7812C	Signetics	
		µA78HV12	Signetics	80
		LM340-12	Signetics	
		SG7812K	† Silicon G	
		SG7812AK	† Silicon G	
		SG7812ACK	Silicon G	
		SG7812CK	Silicon G	
		SG7812ACP	Silicon G	
		SG7812CP	Silicon G	
		µA7812C	TI	
		µA7812M	† TI	
		LM340-12	TI	90
	2 a	STK531	Sanyo	
	3 a	LAS1412	Lambda	
	5 a	µA78H12	Fairchild	
	8 a	42050-128	Micropac	
13.8	1.5a	µA7814	† Signetics	
		µA7814C	Signetics	
	2a	µA78CB	Fairchild	
		LAS15CB	Lambda	
	3 a	LAS14CB	Lambda	
14	8 a	42050-148	Micropac	100
15	400 µa	L037T1	SGS	
	100 ma	µA78L15C	Fairchild	
		MC78L15C	Motorola	
		LM140LA-15	**† National (806)**	
		LM240LA-15	National	
		LM340LA-15	**National (806)**	
		LM78L15C	National	
		µPC78L15	NEC America	
		µA78L15C	Signetics	
		µA78L15C	TI	110
	200 ma	LH0075	National	
		LM342-15	National	
		TBA625C	Plessey	
	400 ma	TDD1615	ITT	
	500 ma	801-V15	† Beckman	
		µA78C15C	**Fairchild (635)**	
		µA78M15C	Fairchild	
		µA78M15M	† Fairchild	
		MC7715C	Motorola	
		MC78M15C	Motorola	120
		LM341-15	National	
		LM78M15	National	
		µPC78M15	NEC America	
		µA78M15	† Signetics	
		µA78M15C	Signetics	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Voltage Regulators (Cont'd)

Fixed, Positive (Cont'd)

Output Voltage	Output Current	Device	Source	Line
15	500 ma	(Cont'd.)		
		SG7815AT	† Silicon G	
		SG7815ACT	Silicon G	
		SG7815CT	Silicon G	
		SG7815T	† Silicon G	
		µA78MHV15	† Signetics	
		µA78MHV15C	Signetics	
		µA78M15C	TI	
		µA78M15M	† TI	
	600 ma	L131	SGS	10
	750 ma	809-V15	† Beckman	
	1 a	SI3150E	Sanken	
		SI3150T	Sanken	
		SG7815AR	† Silicon G	
		SG7815ACR	Silicon G	
		SG7815R	† Silicon G	
		SG7815CR	Silicon G	
	1.5 a	µA7815C	Fairchild	
		µA7815M	† Fairchild	
		LAS1515	Lambda	20
		MC7815C	Motorola	
		LM140-15	**† National (806)**	
		LM140A-15	**† National (806)**	
		LM340-15	**National (806)**	
		LM340A-15	**National (806)**	
		LM7815	National	
		µPC14315	NEC America	
		SI3150G	Sanken	
		SI3150M	Sanken	
		µA7815	† Signetics	30
		µA7815C	Signetics	
		µA78HV15	Signetics	
		LM340-15	Signetics	
		SG7815AK	† Silicon G	
		SG7815ACK	Silicon G	
		SG7815CK	Silicon G	
		SG7815K	† Silicon G	
		SG7815ACP	Silicon G	
		SG7815CP	Silicon G	
		µA7815C	TI	40
		µA7815M	† TI	
		LM340-15	TI	
	2 a	CJSE001	Solitron	
		CJSE003	Solitron	
		CJSE005	Solitron	
	3 a	LAS1415	Lambda	
	5 a	µA78H15	Fairchild	
	8 a	42050-158	Micropac	
16	8 a	42050-168	Micropac	
17	500 ma	**µA78C17C**	**Fairchild (635)**	50
18	100 ma	µA78L18	Fairchild	
		MC78L18C	Motorola	
		LM140LA-18	**† National (806)**	
		LM240LA-18	National	
		LM340LA-18	**National (806)**	
		LM78L18C	National	
	200 ma	LH0075	National	
		LM342-18	National	
	300 ma	TDD1618	ITT	
	500 ma	801-V18	† Beckman	60
		µA78C18C	**Fairchild (635)**	
		MC7718C	Motorola	

(Continued)

Fixed, Positive (Cont'd)

Output Voltage	Output Current	Device	Source	Line
18	500 ma	(Cont'd.)		
		MC78M18C	Motorola	
		LM341-18	National	
		LM78M18	National	
		µPC78M18	NEC America	
	1 a	STK522	Sanyo	
		STK542	Sanyo	
		SG7818AT	† Silicon G	70
		SG7818ACT	Silicon G	
		SG7818CT	Silicon G	
		SG7818T	† Silicon G	
		SG7818AR	† Silicon G	
		SG7818ACR	Silicon G	
		SG7818R	† Silicon G	
		SG7818CR	Silicon G	
	1.5 a	µA7818C	Fairchild	
		µA7818M	† Fairchild	
		MC7818C	Motorola	80
		LM140-18	**† National (806)**	
		LM140A-18	**† National (806)**	
		LAS1518	Lambda	
		LM340-18	**National (806)**	
		LM340A-18	**National (806)**	
		LM7818	National	
		µPC14318	NEC America	
		LM340-18	Signetics	
		µA7818	† Signetics	
		µA7818C	Signetics	90
		µA78HV18	Signetics	
		SG7818AK	† Silicon G	
		SG7818ACK	Silicon G	
		SG7818CK	Silicon G	
		SG7818K	† Silicon G	
		SG7818ACP	Silicon G	
		SG7818CP	Silicon G	
		µA7818M	† TI	
		µA7818C	TI	
		LM340-18	TI	100
	2 a	STK532	Sanyo	
	8 a	42050-188	Micropac	
20	500 ma	**µA78C20C**	**Fairchild (635)**	
		µA78M20C	Fairchild	
		µA78M20M	† Fairchild	
		MC7720C	Motorola	
		MC78M20C	Motorola	
		µA78M20C	Signetics	
		µA78M20M	† Signetics	
		µA78MHV20	† Signetics	110
		µA78MHV20C	Signetics	
		µA78M20C	TI	
		µA78M20M	† TI	
	1.5 a	LAS1520	Lambda	
	2 a	CJSE009	Solitron	
		CJSE011	Solitron	
		CJSE013	Solitron	
	8 a	42050-208	Micropac	
22	500 ma	µA78C22	Fairchild	
	4 a	42050-224	Micropac	120
24	100 ma	µA78L24	Fairchild	
		MC78L24C	Motorola	
		LM140LA-24	**† National (806)**	
		LM240LA-24	National	
		LM340LA-24	**National (806)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Output Voltage	Output Current	Device	Source	Line
Fixed, Positive (Cont'd)				
24	100 ma	(Cont'd.)		
		LM78L24C	National	
	200 ma	PC502	† GI	
		TDD1624	ITT	
		LM342-24	National	
	300 ma	STK507	Sanyo	
	500 ma	**μA78C24C**	**Fairchild**	**(635)**
		μA78M24C	Fairchild	
		μA78M24M	† Fairchild	
		MC7724C	Motorola	10
		MC78M24C	Motorola	
		SG7824AT	† Silicon G	
		SG7824ACT	Silicon G	
		SG7824T	† Silicon G	
		SG7824CT	Silicon G	
		LM341-24	National	
		LM78M24	National	
		μPC78M24	NEC America	
		μA78M24	† Signetics	
		μA78M24C	Signetics	20
		μA78MHV24	† Signetics	
		μA78MHV24C	Signetics	
		μA78M24C	TI	
		μA78M24M	† TI	
	1 a	SI3240E	Sanken	
		SI3240T	Sanken	
		STK523	Sanyo	
		STK543	Sanyo	
		SG7824AR	† Silicon G	
		SG7824ACR	Silicon G	30
		SG7824R	† Silicon G	
		SG782CR	Silicon G	
	1.5 a	μA7824C	Fairchild	
		μA7824M	† Fairchild	
		LAS1524	Lambda	
		MC7824C	Motorola	
		LM140-24	**† National**	**(806)**
		LM140A-24	**† National**	**(806)**
		LM340-24	**National**	**(806)**
		LM340A-24	**National**	**(806)**
		LM7824	National	40
		μPC14324	NEC America	
		SI3240T	Sanken	
		μA7824	† Signetics	
		μA7824C	Signetics	
		LM340-24	Signetics	
		SG7824AK	† Silicon G	
		SG7824ACK	Silicon G	
		SG7824K	† Silicon G	
		SG7824CK	Silicon G	50
		SG7824ACP	Silicon G	
		SG7824CP	Silicon G	
		μA7824C	TI	
		μA7824M	† TI	
		LM340-24	TI	
	2 a	STK533	Sanyo	
	4 a	42050-244	Micropac	
26	4 a	42050-264	Micropac	
28	1.5 a	LAS1528	Lambda	
	4 a	42050-284	Micropac	60
30	4 a	42050-304	Micropac	
31	Shunt	TAA550	National	
		TBA271A	SGS	
	(Continued)			

Output Voltage	Output Current	Device	Source	Line
Fixed, Positive (Cont'd)				
31	Shunt	(Cont'd.)		
		TAA550	Signetics	
32	Shunt	AN155	Panasonic	
	4 a	42050-324	Micropac	
33	Shunt	TAA550	National	
		TBA271B	SGS	
		TAA550	Signetics	70
34	4 a	42050-344	Micropac	
35	Shunt	TAA550	National	
		TBA271C	SGS	
		TAA550	Signetics	
36	4 a	42050-364	Micropac	
Fixed, Negative				
2	1 a	MC7902C	Motorola	
	1.5 a	LAS1802	Lambda	
	2 a	μA79E02	† Fairchild	
		μA79E02C	Fairchild	
3	100 ma	MC79L03C	Motorola	80
	200 ma	LH0076	National	
5	100 ma	MC79L05C	Motorola	
		LM79L05	National	
		LM320L05	National	
	200 ma	LH0076	National	
	250 ma	LM320ML05	National	
	500 ma	μA79M05C	Fairchild	
		LM120H5.0	† National	
		LM220H5.0	National	
		LM320H5.0	National	90
		LM320MP5.0	National	
		LM79M05	National	
		μA79M05	† Signetics	
		μA79M05C	Signetics	
		SG120-05T	† Silicon G	
		SG220-05T	Silicon G	
		SG320-05T	Silicon G	
		μA79M05	TI	
	750 ma	859-V5	† Beckman	
	1 a	SG170-05R	† Silicon G	100
		SG270-05R	Silicon G	
		SG370-05R	Silicon G	
	1.5 a	μA7905C	Fairchild	
		LM7905	National	
		MC7905C	Motorola	
		LM120K5.0	† National	
		LM220K5.0	National	
		LM320K5.0	National	
		LM320T5.0	National	
		LAS1805	Lambda	110
		μA7905	† Signetics	
		μA7905C	Signetics	
		SG120-05K	† Silicon G	
		SG220-05K	Silicon G	
		SG220-05P	Silicon G	
		SG320-05K	Silicon G	
		SG320-05P	Silicon G	
		μA7905C	TI	
		μA7905M	† TI	
	2 a	μA79E05	† Fairchild	120
	(Continued)			

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Voltage Regulators (Cont'd)

Output Voltage	Output Current	Device	Source	Line
Fixed, Negative (Cont'd)				
5	2 a	(Cont'd.)		
		µA79E05C	Fairchild	
	3 a	LM145K5.0	† National	
		LM245K5.0	National	
		LM345K5.0	National	
	5 a	42051-055	Micropac	
5.2	100 ma	LM320L5.2	National	
	250 ma	LM320ML5.2	National	
	500 ma	LM120H5.2	† National	
		LM220H5.2	National	10
		LM320H5.2	National	
		LM320MP5.2	National	
		LM79M05.2	National	
		µA79M05.2	† Signetics	
		µA79M05.2C	Signetics	
		SG120-5.2T	† Silicon G	
		SG220-5.2T	Silicon G	
		SG320-5.2T	Silicon G	
		LM7905.2	National	
	1 a	SG120-5.2R	† Silicon G	20
		SG220-5.2R	Silicon G	
		SG320-5.2R	Silicon G	
	1.5 a	LAS18052	Lambda	
		MC7905.2C	Motorola	
		LM120K5.2	† National	
		LM220K5.2	National	
		LM320K5.2	National	
		LM320T5.2	National	
		LM7905.2	National	
		µA7905.2	† Signetics	30
		µA7905.2C	Signetics	
		SG120-5.2K	Silicon G	
		SG220-5.2K	Silicon G	
		SG220-5.2P	Silicon G	
		SG320-5.2K	Silicon G	
		SG320-5.2P	Silicon G	
	3 a	LM145K5.2	† National	
		LM245K5.2	National	
		LM345K5.2	National	
6	100 ma	LM320L06	National	40
	200 ma	PC523	GI	
		LM0076	National	
	250 ma	LM320ML06	National	
	500 ma	µA79M06C	Fairchild	
		LM120H6.0	† National	
		LM220H6.0	National	
		LM320H6.0	National	
		LM320MP6.0	National	
		LM79M06	National	
		µA79M06	† Signetics	50
		µA79M06C	Signetics	
		µA79M06	TI	
	750 ma	859-V6	† Beckman	
	1.5 a	µA7906C	Fairchild	
		LAS1806	Lambda	
		MC7906C	Motorola	
		LM7906	National	
		LM120K6.0	† National	
		LM220K6.0	National	
		LM320K6.0	National	60
		LM320T6.0	National	
		µA7906	† Signetics	

(Continued)

Output Voltage	Output Current	Device	Source	Line
Fixed, Negative (Cont'd)				
6	1.5 a	(Cont'd.)		
		µA7906C	Signetics	
		µA7906C	TI	
		µA7908M	† TI	
	2 a	CJSE018	Solitron	
		CJSE020	Solitron	
	5 a	42051-065	Micropac	
7	5 a	42051-075	Micropac	70
8	100 ma	LM320L08	National	
	200 ma	LM0076	National	
	250 ma	LM320ML08	National	
	500 ma	µA79M08C	Fairchild	
		LM120H8.0	† National	
		LM220H8.0	National	
		LM320H8.0	National	
		LM320MP8.0	National	
		LM79M08	National	
		µA79M08	† Signetics	80
		µA79M08C	Signetics	
		µA79M08	TI	
	1.5 a	µA7908C	Fairchild	
		LAS1808	Lambda	
		MC7908C	Motorola	
		LM7908	National	
		LM120K8.0	† National	
		LM220K8.0	National	
		LM320K8.0	National	
		LM320T8.0	National	90
		µA7908	† Signetics	
		µA7908C	Signetics	
		µA7908C	TI	
		µA7908M	† TI	
	5 a	42051-085	Micropac	
9	100 ma	LM320L09	National	
	200 ma	LM120H9.0	† National	
		LM220H9.0	National	
		LM320H9.0	National	
		LH0076	National	100
	500 ma	851-V9	† Beckman	
		LM320MP9.0	National	
	750 ma	859-V9	† Beckman	
	1 a	LM120K9.0	† National	
		LM220K9.0	National	
		LM320K9.0	National	
		LM320T9.0	National	
	1.5 a	42051-095	Micropac	
10	100 ma	LM320L10	National	
	250 ma	LM320ML10	National	110
	1.5 a	LAS1810	Lambda	
	5 a	42051-105	Micropac	
12	100 ma	MC79L12C	Motorola	
		LM320L12	National	
		LM79L12	National	
	200 ma	PC503	† GI	
		LH0076	National	
		LM120H12	† National	
		LM220H12	National	
		LM320H12	National	120
		SG120-12T	† Silicon G	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Fixed, Negative (Cont'd)

Output Voltage	Output Current	Device	Source	Line
12	200 ma	(Cont'd.)		
		SG220-12T	Silicon G	
		SG320-12T	Silicon G	
	250 ma	LM320L12	National	
	500 ma	851-V12	† Beckman	
		μA79M12C	Fairchild	
		LM320MP12	National	
		LM79M12	National	
		μA79M12	† Signetics	
		μA79M12C	Signetics	10
		μA79M12	TI	
	750 ma	859-V12	† Beckman	
	1 a	LM120K12	† National	
		LM220K12	National	
		LM320K12	National	
		LM320T12	National	
		SG120-12R	† Silicon G	
		SG220-12R	Silicon G	
		SG320-12R	Silicon G	
	1.5 a	μA7912C	Fairchild	20
		LAS1812	Lambda	
		MC7912C	Motorola	
		LM7912	National	
		μA7912	† Signetics	
		μA7912C	Signetics	
		SG120-12K	† Silicon G	
		SG220-12K	Silicon G	
		SG220-12P	Silicon G	
		SG320-12K	Silicon G	
		SG320-12P	Silicon G	30
		μA7912C	TI	
		μA7912M	† TI	
	4 a	42051-124	Micropac	
14	4 a	42051-144	Micropac	
15	100 ma	MC79L15C	Motorola	
		LM320L15	National	
		LM79L15	National	
	200 ma	LH0076	National	
		LM120H15	† National	
		LM220H15	National	
		LM320H15	National	40
		SG120-15T	† Silicon G	
		SG220-15T	Silicon G	
		SG320-15T	Silicon G	
	250 ma	LM320ML15	National	
	500 ma	851-V15	† Beckman	
		μA79M15C	Fairchild	
		LM320MP15	National	
		LM79M15	National	
		μA79M15	Signetics	50
		μA79M15C	† Signetics	
		μA79M15	TI	
	750 ma	859-V15	† Beckman	
	1 a	LM120K15	† National	
		LM220K15	National	
		LM320K15	National	
		LM320T15	National	
		SG120-15R	† Silicon G	
		SG220-15R	Silicon G	
		SG320-15R	Silicon G	60
	1.5 a	μA7915C	Fairchild	
		LAS1815	Lambda	

(Continued)

Fixed, Negative (Cont'd)

Output Voltage	Output Current	Device	Source	Line
15	1.5 a	(Cont'd.)		
		MC7915C	Motorola	
		LM7915	National	
		μA7915	† Signetics	
		μA7915C	Signetics	
		SG120-15K	† Silicon G	
		SG220-15K	Silicon G	
		SG220-15P	Silicon G	70
		SG320-15K	Silicon G	
		SG320-15P	Silicon G	
		μA7915C	TI	
		μA7915	† TI	
	2 a	CJSE002	Solitron	
		CJSE004	Solitron	
		CJSE006	Solitron	
	4 a	42051-154	Micropac	
16	4 a	42051-164	Micropac	
18	100 ma	MC79L18C	Motorola	80
		LM320L18	National	
		LM79L18	National	
	200 ma	LH0076	National	
		LM120H18	† National	
		LM220H18	National	
		LM320H18	National	
	250 ma	LM320ML18	National	
	500 ma	LM320MP18	National	
		LM79M18	National	
		μA79M18	† Signetics	90
		μA79M18C	Signetics	
	1 a	LM120K18	† National	
		LM220K18	National	
		LM320K18	National	
		LM320T18	National	
	1.5 a	μA7918C	Fairchild	
		LAS1818	Lambda	
		MC7918C	Motorola	
		LM7918	National	
		μA7918	† Signetics	100
		μA7918C	Signetics	
		μA7918C	TI	
		μA7918M	† TI	
	4 a	42051-184	Micropac	
20	500 ma	μA79M20C	Fairchild	
		μA79M20	TI	
	1.5 a	LAS1820	Lambda	
	2 a	CJSE010	Solitron	
		CJSE012	Solitron	
		CJSE014	Solitron	110
	3 a	42051-204	Micropac	
22	3 a	42051-223	Micropac	
24	100 ma	MC79L24C	Motorola	
		LM320L24	National	
		LM79L24	National	
	200 ma	LM120H24	† National	
		LM220H24	National	
		LM320H24	National	
	250 ma	LM320ML24	National	
	500 ma	μA79M24C	Fairchild	120
		LM320MP24	National	
		LM79M24	National	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Voltage Regulators (Cont'd)

Output Voltage	Output Current	Device	Source	Line
Fixed, Negative (Cont'd)				
24	500 ma	(Cont'd.)		
		µA79M24	† Signetics	
		µA79M24C	Signetics	
		µA79M24	TI	
	1 a	LM120K24	† National	
		LM220K24	National	
		LM320K24	National	
		LM320T24	National	
	1.5 a	µA7924C	Fairchild	
		LAS1824	Lambda	10
		MC7924C	Motorola	
		LM7924	National	
		µA7924	† Signetics	
		µA7924C	Signetics	
		µA7924C	TI	
		µA7924M	† TI	
	3 a	42051-243	Micropac	
26	3 a	42051-263	Micropac	
28	1.5 a	LAS1828	Lambda	
	3 a	42051-283	Micropac	20
30	3 a	42051-303	Micropac	
31	Shunt	TAA550	National	
		TBA271A	SGS	
		TAA550	Signetics	
32	Shunt	AN155	Panasonic	
	3 a	42051-323	Micropac	
33	Shunt	TAA550	National	
		TBA271B	SGS	
		TAA550	Signetics	
34	3 a	42051-343	Micropac	30
35	Shunt	TAA550	National	
		TBA271C	SGS	
		TAA550	Signetics	
36	3 a	42051-363	Micropac	
Fixed, Dual				
±5	200 ma	NE5551	Signetics	
		SE5551	† Signetics	
±6	200 ma	NE5552	Signetics	
		SE5552	† Signetics	
	5 a	42051	Micropac	
±12	100 ma	LM126	† National	40
		LM226	National	
		LM326	National	
	200 ma	NE5553	Signetics	
		SE5553	† Signetics	
-12,5	100 ma	LM127	† National	
		LM227	National	
		LM327	National	
	200 ma	NE5555	Signetics	
		SE5555	† Signetics	
±15	100 ma	XR4195	Exar	50
		MC1468	Motorola	
		MC1568	† Motorola	
		LM125	† National	
		LM225	National	
		LM325	National	
		RC4195	Raytheon	

(Continued)

Output Voltage	Output Current	Device	Source	Line
Fixed, Dual (Cont'd)				
±15	100 ma	(Cont'd.)		
		RM4195	† Raytheon	
		SG1468	Silicon G	
		SG1568	† Silicon G	60
		SG4501	Silicon G	
	200 ma	NE5554	Signetics	
		SE5554	† Signetics	
		SG1501A	† Silicon G	
		SG2501A	Silicon G	
		SG3501A	Silicon G	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Adjustable, Positive

Arranged in sequence by Output Voltage High, Output Current, and then Output Voltage Low.

Output Voltage Hi	Output Voltage Low	Output Current	Device	Source	Line
7	1	50 ma	NC520	† GI	
		200 ma	NC521	† GI	
9	3	500 ma	806	† Beckman	
15	2.6	300 ma	LAS14U	Lambda	
	5	1.5 a	SI3580M	Sanken	
20	2	20 ma	300	Intersil	
			LM300	National	
			SFC2300	NPC	10
			SG300	Silicon G	
	10	800 ma	NC562	† GI	
	5	5a	µA78HG	Fairchild	
21	9	500 ma	802	† Beckman	
26	1.8	12 ma	CA3085	† RCA	
27	0	200ma	LH0075	† National	
			LH0075C	National	
30	3	Shunt	TL430	TI	
	4.5	12 ma	LM305	AMD	
			µA305C	Fairchild	20
			305	Intersil	
			LM305	Motorola	
			LM305	National	
			µPC141	NEC America	
			µPC325	NEC America	
			LM305	Raytheon	
			SG305	Silicon G	
			LM305	TI	
	2	20 ma	100	† Intersil	
			200	Intersil	30
			LM100	† National	
			LM200	National	
			SFC2100	† NPC	
			SFC2200	NPC	
			SG100	† Silicon G	
			SG200	Silicon G	
	5	500 ma	µA78MG	Fairchild	
			µA78MG	† Signetics	
			µA78MGC	Signetics	
		1 a	µA78G	Fairchild	40
			µA78G	† Signetics	
			µA78GC	Signetics	
	4	1.5 a	LAS15U	Lambda	
	3	1.8a	L200	SGS	
	2.6	3 a	LAS14U	Lambda	
	5	5 a	µA78HG	Fairchild	
32	—	200 ma	M5199	Mitsubishi	
	2.5	200 ma	MC1469G	Motorola	
		500 ma	MC1469R	Motorola	
			TA7184	Toshiba	50
	20	500 ma	804	† Beckman	
	—	1a	M5199A	Mitsubishi	
35	1.2	3a	**LM150**	**† National (814)**	
			LM250	**National (814)**	
			LM350	**National (814)**	
36	1.7	100 ma	CA3085A	† RCA	
37	5	25 ma	µA376C	Fairchild	
			LM376	National	

(Continued)

Adjustable, Positive (Cont'd)

Output Voltage Hi	Output Voltage Low	Output Current	Device	Source	Line
37	5	25 ma	(Cont'd.)		
			LM376	TI	60
		50 ma	SE550	† Signetics	
	2	150 ma	723	† AMD	
			723C	AMD	
			µA723C	Fairchild	
			µA723M	† Fairchild	
			HA17723	Hitachi	
			723	† Intersil	
			723C	Intersil	
			MC1723	† Motorola	
			MC1723C	Motorola	70
			LM723	† National	
			LM723C	National	
			SFC2723C	† NPC	
			SFC2723EC	NPC	
			CA723	† RCA	
			CA723C	RCA	
			RC723	Raytheon	
			RM723	† Raytheon	
			µA723	† Signetics	
			µA723C	Signetics	80
			SA723C	Signetics	
			TDA0723	Signetics	
			SG723	† Silicon G	
			SG723C	Silicon G	
			TL1723	† Telefunken	
			TL1723C	Telefunken	
			TL3723	Telefunken	
			µA723C	TI	
			µA723M	† TI	
	2.5	200 ma	MC1561G	† Motorola	90
			MC1569G	† Motorola	
	1.2	500ma	SG117T	† Silicon G	
			SG217T	Silicon G	
			SG317T	Silicon G	
	2.5	500 ma	MC1561R	† Motorola	
			MC1569R	† Motorola	
	1.2	1.5 a	LM117	† Motorola	
			LM317	Motorola	
			LM117	**† National (828)**	
			LM217	**National (828)**	100
			LM317	**National (828)**	
			SG117K	† Silicon G	
			SG217K	Silicon G	
			SG317K	Silicon G	
			LM117	† TI	
			LM217	TI	
			LM317	TI	
38	2	100 ma	SG3532	Silicon G	
		150 ma	LAS723	Lambda	
			LAS1000	Lambda	110
	8	250 ma	NC501	† GI	
			NC511	† GI	
			PC511	† GI	
	13	250 ma	NC572	† GI	
40	4.5	12 ma	LM105	AMD	
			LM205	AMD	
			µA105M	† Fairchild	
			105	† Intersil	
			205	Intersil	
			LM105	† Motorola	120
			LM205	Motorola	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Voltage Regulators (Cont'd)

Adjustable, Positive (Cont'd)

Output Voltage Hi	Output Voltage Low	Output Current	Device	Source	Line
40	4.5	12 ma	(Cont'd.)		
			LM105	† National	
			LM205	National	
			SFC2105	† NPC	
			SFC2205	NPC	
			LM105	† Raytheon	
			LM205	Raytheon	
			SG105	† Silicon G	
			SG205	Silicon G	
			LM105	† TI	10
			LM205	TI	
		45 ma	LM305A	AMD	
			µA305AC	Fairchild	
			305A	Intersil	
			LM305A	National	
			SFC2305	NPC	
			SG305A	Silicon G	
			LM305A	Raytheon	
			LM305A	TI	
	2	50 ma	NE550	Signetics	20
		150 ma	SE550L	† Signetics	
46	1.7	100 ma	CA3085B	† RCA	
48	2	100 ma	SG1532	† Silicon G	
			SG2532	Silicon G	
		150 ma	LAS723B	Lambda	
			LAS1100	Lambda	
56	8	1 a	CJCA001	Solitron	
			CJCA007	Solitron	
57	1.2	1.5 a	LM117HV	National	
			LM317HV	National	30
1000	0	100 ma	MC1466	Motorola	
			MC1566	† Motorola	

Adjustable, Negative

21	9	500 ma	852	† Beckman	
27	0	200ma	LH0076	† National	
			LH0076C	National	
30	0.035	20 ma	µA304C	Fairchild	
			LM304G	Motorola	
			LM304	National	
			µPC142	NEC America	
			LM304	Raytheon	40
			SG304	Silicon G	
			LM304	TI	
	2.2	500 ma	µA79MG	Fairchild	
			µA79MG	† Signetics	
			µA79MGC	Signetics	
		1 a	µA79G	Fairchild	
			µA79G	† Signetics	
			µA79GC	Signetics	
	2.6	1.5 a	LAS18U	Lambda	
32	3.8	200 ma	MC1463G	Motorola	
			MC1463R	Motorola	50
		500 ma	MC1463R	Motorola	
			TA7085	Toshiba	
37	2	50 ma	SG1511	† Silicon G	
			SG3511	Silicon G	
	3.6	200 ma	MC1563G	† Motorola	
		500 ma	MC1563R	† Motorola	

(Continued)

Adjustable, Negative (Cont'd)

Output Voltage Hi	Output Voltage Low	Output Current	Device	Source	Line
37	(Cont'd.)				
	1.2	1.5 a	**LM137**	**† National (822)**	
			LM237	**National (822)**	60
			LM337	**National (822)**	
38	8	250 ma	NC513	GI	
			PC513	GI	
40	0.015	20 ma	µA104M	† Fairchild	
			LM104G	† Motorola	
			LM204G	Motorola	
			LM104	† National	
			LM204	National	
			SFC2104	† NPC	
			SFC2204	NPC	70
			LM104	† Raytheon	
			LM204	Raytheon	
			SG104	† Silicon G	
			SG204	Silicon G	
			SG304	Silicon G	
			LM104	† TI	
			LM204	TI	
56	8	1 a	CJCA002	Solitron	
			CJCA008	Solitron	
57	1.2	1.5 a	LM137HV	† National	80
			LM337HV	National	

Adjustable, Dual

±20	±8	100 ma	MC1468L	Motorola	
			MC1568L	† Motorola	
			SG1468J	Silicon G	
			SG1568J	† Silicon G	
	±14.5	100 ma	MC1568R	† Motorola	
			MC1468R	Motorola	
			SG1468T	Silicon G	
			SG1568T	† Silicon G	
	±5	200 ma	NE5554	Signetics	90
±28	±10	100 ma	SG1501	† Silicon G	
			SG2501	Silicon G	
			SG3501	Silicon G	
			SG4501	Silicon G	
			SG3502	Silicon G	
			SG1502	† Silicon G	
			SG2502	Silicon G	
±32	±0.05	100 ma	RC4194D	Raytheon	
			SG4194CJ	Silicon G	
		200 ma	RC4194TK	Raytheon	100
			SG4194CR	Silicon G	
±42	±0.05	100 ma	XR4194M	† Exar	
			RM4194D	† Raytheon	
			SG4194MJ	† Silicon G	
		200 ma	XR4194MK	† Exar	
			RM4194TK	† Raytheon	
			SG4194MR	† Silicon G	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Switching Regulators

Switching Regulator Circuits

Output Voltage Hi	Output Voltage Low	Output Current	Device	Source		Line
			XR1524	†Exar		
			XR2524	Exar		
			XR3524	Exar		
			ZN1066	Ferranti		
			μA78S40	**Fairchild**	**(622)**	
			μA78S60	Fairchild		
			MC3380	Motorola		
			MC3420	Motorola		
			MC3520	†Motorola		10
			LN1524	†National		
			LN3524	National		
			SL442	Plessey		
			CA3085	RCA		
			TDA1060	Signetics		
			TDA2640	Signetics		
			SG1524	†Silicon G		
			SG2524	Silicon G		
			SG3524	Silicon G		
			SG1524	†TI		20
			SG3524	TI		
			TL494C	**TI**	**(994)**	
			TL494M	**†TI**	**(994)**	
			TL497I	TI		
			TL497M	†TI		
			TL495	TI		

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Other Devices

Other Linear Devices

Function	Device	Source
AC Amplifier, Quad, Single Supply	CA3048	RCA
AC Detector (Detects presence or absence of ac signals, includes adjustable threshold and time delay.)	3050	Intech/FMI
Active Filters (See also Linear Telecommunications Circuits)	881	Beckman
	μAF11	Burr-Brown
	μAF11H	† Burr-Brown
	μAF15	Burr-Brown
	μAF15H	† Burr-Brown
	UAF21	Burr-Brown
	UAF21H	† Burr-Brown
	UAF25	Burr-Brown
	UAF25H	† Burr-Brown
	UAF31	Burr-Brown
	UAF41	Burr-Brown
	CH1290	Cermetek
	CH1295	Cermetek
	CH1296	Cermetek
	FLT-U2	Datel
	ACF7032C	GI
	ACF7092C	GI
	AF100	† National
	AF150	National
	AF151	National
Active Filters, Bandpass, Adjusts 60 270 Hz	AF99	National
Active Filter, Voltage Controlled, 4 stage	SSM2040	SSM
Alarm Circuit	**S2561**	**AMI** **(376)**
	MD4301A	Mitel
	MD4301B	Mitel
	M5170	Mitsubishi
	L911	**Siliconix** **(983)**
Alarm Circuits, Triple Alert/Alarm (Each circuit has two inputs, when the first one is low an open collector LED driver is turned on. When the second one is low independent of the first the output is flashed at an adjustable rate).	3020	Intech/FMI
Alarm Circuits, Temperature	3030	Intech/FMI
Alarm Circuits, Tone Alarm (Comparator with ac output)	3010	Intech/FMI
Alarms, Voltage. See Voltage Alarms below.		
Amplifiers: See Linear Amplifiers, Special Purpose and Operational Amplifiers		
Amplifier Detector (for firing SCR's or operating relays)	ULN-2301	Sprague
Amplifier SCR firing Circuit	ULN-2300	Sprague
Analog Digital Control Circuit (Wide bandwidth op amp and high speed, dual threshold comparator)	MC1407	Motorola
	MC1507	† Motorola
Analog to Digital Converter and vice versa (See Linear Telecommunication Circuits: Delta Modulation and Companding A/D Converters		

Other Linear Devices (Cont'd)

Function	Device	Source
Analog Shift Register, 130x2, with storage (See also Serial Analog Delay below)	CCD311	Fairchild
Analog Shift Register (455x2)	CCD321	Fairchild
Analog Shift Register, 185 stage, 190x2 stage	S10110	AMI
	S10111	AMI
	TCA350	ITT
	TCA380	ITT
Analog Shift Register, 455 stage, video delay	R5102	Reticon
Analog Shift Register, 910 stage, video delay	R5103	Reticon
Analog Shift Register, 2000 stage, audio delay	R5101	Reticon
Analog Shift Register, (Bucket Brigade Device) (Dual 64 stage, acts as a variable delay line in the audio range)	MN3003	Panasonic
Analog Shift Register, (Bucket Brigade Device) (512 stage)	MN3002	Panasonic
	MN3004	Panasonic
	NE502	Signetics
	NE503	Signetics
Analog Shift Register, (Bucket Brigade Device) Dual 512 stage, acts as a variable delay line in the audio frequency range)	MN3001	Panasonic
Analog Shift Register, (Bucket Brigade Device) (4096 stage)	MN3005	Panasonic
Balanced Modulator/Demodulator	μA796C	Fairchild
	MC1496	Motorola
	MC1596	† Motorola
	MC12002	Motorola
	MC12502	† Motorola
	LM1496	National
	LM1596	† National
	AN610	Panasonic
	SL640C	Plessey
	SL641C	Plessey
	SL1001A	Plessey
	SL1001B	Plessey
	SL1496	Plessey
	SL1596	† Plessey
	SL1640	Plessey
	SL1641	Plessey
	L025	SGS
	S042	Siemens
	MC1496	Signetics
	MC1596	† Signetics
	N5596	Signetics
	TCA820	Signetics
	TCA240	Signetics
	SG1496	Silicon G
	SG1596	Silicon G
Double Balanced Modulator/Demodulator	SL1696	Plessey
	SL1796	Plessey
Ring Modulator, four transistor	SL355	Plessey
	TBA673	Plessey

(Continued)

Other Linear Devices (Cont'd)

Function	Device	Source
Ring Modulator, four transistor (Cont'd.)	TBA673	Signetics
Blowout Resistant Transistor (simulates 40 v transistor with special protection)	LM195	† National
	LM295	National
	LM395	National
Bucket Brigade Devices, See Analog Shift Registers this section		
Crystal Oscillators	SL680	Plessey
Comparators, Programmable with Memory (High/Low Comparator)	CA3098	† RCA
	CA3099	† RCA
Current Limiter, 225 ma	MC3422	Motorola
Constant Current Source, 1 μa to 10 ma	LM134	† National
	LM234	National
	LM334	National
Constant Current Supply, to 0.6a	TDA1251	SGS
Correlator, Binary to Analog	R5401	Reticon
	TDC1004	TRW
Customized Arrays (Linear and Digital circuits, customized in final metalization)	XR-CHIP	Exar
	XR-IIL-CHIP	Exar
	ULA	Ferranti
	MONOCHIP	Interdesign
	ECL-ARRAY	Plessey
	TTL-ARRAY	Plessey
	RTL-ARRAY	Plessey
Data Acquisition System, 8 channel (expandable), sample/hold, 8 bit conversion	MN7100	Micro Net
	MN7100H	† Micro Net
	MN7110	Micro Net
	MN7110H	† Micro Net
	MN7120	Micro Net
	MN7120H	† Micro Net
Data Acquisition System, 16 channel 8 bit conversion	ADC0816	National
	ADC0817	National
Data Acquisition System, 8 channel differential, sample/hold, 12 bit conversion	**HDAS-8M**	**Datel** **(382)**
Data Acquisition System, 16 channel, sample/hold, 12 bit conversion	**HDAS-16M**	**Datel** **(382)**
DC to DC Converter	MCC138	Micro Comp
	MCC139	Micro Comp
DC to DC Converter: See Regulators, Switching, under Linear Voltage Regulators.		
Demodulator, Phase Sensitive, for synchro or resolver systems	MN2120	Micro Net
Divider (See also Multipliers/Dividers below)	4291	Burr-Brown

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Other Devices (Cont'd)

Function	Device	Source	Line
Other Linear Devices (Cont'd)			
Dual Transistors, Monolithic, Matched, See Linear Arrays			
DVM Circuits See Interface Analog to Digital Converters, also Digital Special			
Flasher (LED)	LM3909	National	
	LM3909	**Siliconix (984)**	
Fluid Detector (oscillator, balance detector)	LM1830	National	
Frequency Switch, Programmable	MC3344	Motorola	
Frequency/Tone Operated Devices See Linear Telecommunication Circuits			10
Frequency to Voltage Converter (tachometer speed switch)	LM2907	National	
	LM2917	National	
Frequency to Voltage (Pulse) Converter	SAK140	Signetics	
Frequency to Voltage Converter	MC3315	Motorola	
Frequency to Voltage Converter, Dual	MC3316	Motorola	20
	MC3317	Motorola	
Frequency to Voltage/Voltage to Frequency Converter	VFC32	Burr-Brown	
	VFC32M	† Burr-Brown	
	VFQ-1	Datel	
	XR4151C	Exar	
	XR4151M	† Exar	
	A8400	Intech/FMI	
	A8400ET-1	Intech/FMI	
	A8402	Intech/FMI	30
	A8402ET-1	Intech/FMI	
	A8404	Intech/FMI	
	RC4151	Raytheon	
	RM4151	† Raytheon	
	RV4151	Raytheon	
	RC4152	**Raytheon (968)**	
	RM4152	**† Raytheon (968)**	
	RV4152	**Raytheon (968)**	
	9400	Teledyne S	
Function Generator (Counter, ROM, D/A), See also Linear Phase Locked Loop Circuits	MN350	Micro Net	40
	MN351	Micro Net	
	MN352	Micro Net	
Hall Effect Devices (Sense magnetic field) See also Digital Other Digital Devices	DN835	Panasonic	
	TCA450	Signetics	
	ULN-3006	Sprague	
	ULN-3008	Sprague	50
Image Sensor, Circular, Self Scanning	RO64	Reticon	
	RO720A	Reticon	
Image Sensor, 256x1, CCD	CCD110	Fairchild	
Image Sensor, CC Photodiode, 256x1	CCPD256	Reticon	
Image Sensor, 500x1, CCD	CCD101	Fairchild	
Image Sensor, 1024x1, CCD	CCD131	Fairchild	60
Image Sensor, CC Photodiode, 1024x1	CCPD1024	Reticon	
Image Sensor, 1728x1, CCD	CCD121	Fairchild	
Image sensor, CC Photodiode, 1728x1	CCPD1728	Reticon	
Image Sensor, Linear Self Scanning	IPL3010	IPI	
	IPL3016	IPI	70
	IPL3032	IPI	
	IPL4050	IPI	
	IPL4064	IPI	
	IPL4100	IPI	
	IPL4128	IPI	
	IPL4256	IPI	
	IPL7050	IPI	
	IPL7064	IPI	
	IPL7100	IPI	
	IPL7128	IPI	80
	IPL7256	IPI	
	M128	IPI	
	M256	IPI	
	M512	IPI	
	M768	IPI	
	M1024	IPI	
	MEL512	Panasonic	
	RL16	Reticon	
	RL64	Reticon	
	RL128	Reticon	90
	RL256	Reticon	
	RL512	Reticon	
	RL936	Reticon	
	RL1024	Reticon	
	RL1728	Reticon	
	RL1872	Reticon	
	RL2048	Reticon	
Image Area Sensor, Self Scanning	2D1	IPI	
	RA32X32	Reticon	100
	RA50X50	Reticon	
	RA100X100	Reticon	
Image Area Sensor, 100x100, CCD	CCD201	Fairchild	
	CCD202	Fairchild	
Image Area Sensor, 190x224, CCD	CCD211	Fairchild	
Impedance Converter (Gyrator)	AF120	National	
	TCA580	Signetics	110
LED, Constant Current	NSL4944	National	
Level Detector, Precision, (with internal reference, Schmitt trigger action)	MCC127	Micro Comp	
	MCC401	Micro Comp	
	MCC402	Micro Comp	
	MCC450	Micro Comp	
	M54101	Mitsubishi	
	TL560C	TI	120
Level Detector, Precision Dual	MCC122	Micro Comp	
	MCC129	Micro Comp	
	MCC130	Micro Comp	
Level Meter, analog input drives a bar of LED's	LB1405	Sanyo	
	UAA170	Siemens	
	UAA180	Siemens	
Light to Current Converter	LM1890	National	130
	LM1891	National	
	LM1892	National	
Light to Frequency Converter	IPL13	IPI	
Light Detector (with buffer amplifier)	IPL16	IPI	
	MCC401	Micro Comp	
	μPC558	NEC America	
	CA3062	RCA	
	U103	Telefunken	140
Light Activated Switch	ZNP100	Ferranti	
	IPL15	IPI	
	IPL17	IPI	
	PS12	IPI	
	PS24	IPI	
	MCC401	Micro Comp	
	MCC402	Micro Comp	
	MCC450	Micro Comp	
	U102	Telefunken	150
	U221	Telefunken	
Low Battery Indicator, triggers on 3v (for use with 3 NiCd cells)	ICM7201	Intersil	
Motor Load Control	PT-107	Photo Therm	
Motor, Stepping Motor Driver	SAA1027	Signetics	
Motor Speed Regulator (for small dc motors)	μA7391	Fairchild	160
	MCC140	Micro Comp	
	LM1815	National	
	SL440	Plessey	
	TCA900	SGS	
	TCA910	SGS	
	TDA1003A	Signetics	
	TDA1006	Signetics	
Multipliers	XR2208	Exar	
	XR2208M	† Exar	170
	A8495	Intech/FMI	
	A8595	† Intech/FMI	
	8013C	Intersil	
	8013M	† Intersil	
	MC1494	Motorola	
	MC1594	† Motorola	
	MC1495	Motorola	
	MC1595	† Motorola	
	SL1495	Plessey	
	SL1595	† Plessey	180
	CA3091	† RCA	
	SG1402	† Silicon G	
	SG2402	Silicon G	
	SG3402	Silicon G	
	SG1495	Silicon G	
	SG1595	† Silicon G	
	TA7158	Toshiba	
Multiplier, Dual (Linear Antilog Voltage Controlled Amplifier)	SSM2000	SSM	190

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Other Devices (Cont'd)

Function	Device	Source	Line
Other Linear Devices (Cont'd)			
Multiplier, Dual (Linear Antilog Voltage Controlled Amplifier) (Cont'd.)	SSM2020	SSM	
Multipliers/Dividers	AD530	AD	
	AD530S	† AD	
	AD532	AD	
	AD532S	† AD	
	AD533	AD	
	AD533S	† AD	10
	AD534J	AD	
	AD534K	AD	
	AD534L	AD	
	AD534S	† AD	
	AD534T	† AD	
	4201	Burr-Brown	
	4203	Burr-Brown	
	4203S	† Burr-Brown	
	4204	Burr-Brown	
	4204S	† Burr-Brown	20
	4205	Burr-Brown	
	4205S	† Burr-Brown	
	4206	Burr-Brown	
	4213	Burr-Brown	
	4213S	† Burr-Brown	
Multifunction Convertors (XY/Z)expM	AD531J	AD	
	AD531K	AD	
	AD531L	AD	
	AD531S	† AD	30
	4301	Burr-Brown	
	4302	Burr-Brown	
Noise Generator (psuedo random sequence generator for audio)	S2688	AMI	
	MM5837	National	
Oscillator/Buffer	LM175	† National	
	LM275	National	
	LM375	National	40
Oscillator, Quadrature	4423	Burr-Brown	
Overvoltage Protector	L2OV5	Lambda	
	L2OV6	Lambda	
	L2OV9	Lambda	
	L2OV12	Lambda	
	L2OV15	Lambda	
	L2OV20	Lambda	
	L2OV24	Lambda	50
	L2OV28	Lambda	
	L6OV5	Lambda	
	L6OV6	Lambda	
	L6OV9	Lambda	
	L6OV10	Lambda	
	L6OV12	Lambda	
	L6OV15	Lambda	
	L6OV16	Lambda	
	L6OV20	Lambda	
	L6OV24	Lambda	60
	L6OV28	Lambda	
	MC3423	Motorola	
	MC3523	† Motorola	
	MC3423	TI	
	MC3523	† TI	
Peak Detector (senses and holds peak)	4085	Burr-Brown	
(Continued)			

Function	Device	Source	Line
Other Linear Devices (Cont'd)			
Peak Detector (senses and holds peak) (Cont'd.)	4085M	† Burr-Brown	
	5902	† OEI	70
Phase Shifter, 90°, audio	CH1410	Cermetek	
	CH1411	Cermetek	
Phase Sensitive Demodulator	MN2120	Micro Net	
	MN2120H	† Micro Net	
PIN Diode Switch Driver	DH0035	† National	
	DH0035C	National	
Power Supply Control (Oscillator with variable mark/space for switching supplies) See Linear Voltage Regulators, Switching	SL442	Plessey	80
Pressure Transducers, Absolute	LX1400A	National	
	LX1600A	National	
	LM1700A	National	
Pressure Transducers, Gage	LX1600G	National	
	LX1700G	National	90
Pressure Transducers, Differential	LX1600D	National	
	LX1700D	National	
Pulse Width (and PRF) to Voltage Converter	3910	OEI	
Read Amplifier/Preamplifier (for magnetic tape memories)	MC3467	Motorola	
	MC3468	Motorola	
Reference Diode Voltage (two terminal active circuit) 1.220v ±5%	MPS5010	Micro Power	100
	LM113	† National	
	LM313	National	
Reference Voltage, 1.26v (two terminal active circuit)	ZN423	Ferranti	
Reference Voltage Diode, 2.45v (two terminal active circuit)	ZN458	Ferranti	
Reference Voltage, 2.5v	AD580	† AD	110
	LN136	† National	
	LN236	National	
	LN336	National	
Reference Voltage, 5v	MC1403	Motorola	
	MC1503	† Motorola	
	REF-02	**† PMI** (894)	
	REF-02A	**† PMI** (894)	
	REF-02C	**PMI** (894)	
	REF-02D	**PMI** (894)	
	REF-02E	**PMI** (894)	
	REF-02H	**PMI** (894)	
Reference Voltage, 6.9v temperature stabilized	LM129	† National	
	LM329	National	
	LM199	† National	
	LM299	National	
	LM399	National	
	LM199A	† National	130
(Continued)			

Function	Device	Source	Line
Other Linear Devices (Cont'd)			
Reference Voltage, 6.9v temperature stabilized (Cont'd.)	LM299A	National	
	LM399A	National	
	LM3999	National	
	LM129	† Raytheon	
	LM329	Raytheon	
	LM199	† Raytheon	
	LM299	Raytheon	
	LM399	Raytheon	
	LM199A	† Raytheon	140
	LM299A	Raytheon	
	LM399A	Raytheon	
	LM3999	Raytheon	
Reference Voltage, 10v	AD2700L	AD	
	AD2700U	† AD	
	AD2701L	AD	
	AD2701U	† AD	
	AD581	† AD	
	840-T1	Beckman	150
	840-T2	Beckman	
	R675	† Hybrid Sys.	
	MN2000	Micro Net	
	MN2000H	† Micro Net	
	MN2001	Micro Net	
	MN2001H	† Micro Net	
	MN2002	Micro Net	
	MN2002H	† Micro Net	
	MN2003	Micro Net	
	MN2003H	† Micro Net	160
	LH0070	† National	
	REF-01	**† PMI** (890,894)	
	REF-01A	**† PMI** (890,894)	
	REF-01C	**PMI** (890)	
	REF-01D	**PMI** (890)	
	REF-01E	**PMI** (890)	
	REF-01H	**PMI** (890)	
Reference Voltage, 10.24v	LH0071	National	170
Reference Voltage, ±10v	AD2702L	AD	
	AD2702U	† AD	
	R675-3	Hybrid Sys.	
	R675-6	Hybrid Sys.	
	MN2004	Micro Net	
	MN2004H	† Micro Net	
	MN2005	Micro Net	
	MN2005H	† Micro Net	180
Reference Voltage, Adjustable	TL430	TI	
Regulator Diode (two terminal active circuit) 1.8 to 5.6v	LM103	† National	
Regulator Diode (two terminal active circuit)	ZTE1.5	ITT	
	ZTE2	ITT	
	ZTE2.4	ITT	
	ZTE2.7	ITT	190
	ZTE3	ITT	
	ZTE3.3	ITT	
	ZTE3.6	ITT	
	ZTE3.9	ITT	
	ZTE4.3	ITT	
	ZTE4.7	ITT	
	ZTE5.1	ITT	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Other Devices (Cont'd)

Other Linear Devices (Cont'd)

Function	Device	Source	
Regulator Diode with Amplifier (6.8 to 11v)			
	MCA Series	Motorola	
Resolver Systems: See Phase Sensitive Demodulator above			
	HRCDX-14	DDC	
	HRDC-10	DDC	
	HRDC-14	DDC	
	HRCT-14	DDC	
	HSCDX-14	DDC	
	HSCT-14	DDC	
	HSDC-10	DDC	
	HSDC-14	DDC	
	HSDC-360	DDC	
	HXCDX-14	DDC	
	HXCT-14	DDC	
	HXDC-10	DDC	
	HXDC-14	DDC	
RMS to DC Converter			
	AD536J	AD	
	AD536K	AD	
	4340	Burr-Brown	
	4341	Burr-Brown	
	LH0091	† National	
	LH0091C	National	
Sample and Hold Circuits			
	LF198	AMD	
	LF298	AMD	
	LF398	† AMD	
	AD582	AD	
	AD583K	AD	
	AD583S	† AD	
	SHC23	Burr-Brown	
	SHC23ET	† Burr-Brown	
	SHC80	Burr-Brown	
	SHC85	Burr-Brown	
	SHC85ET	Burr-Brown	
	SHM-HU	Datel	
	SHM-HUM	† Datel	
	SHM-IC-1	**Datel**	**(393)**
	SHM-IC-1M	**† Datel**	**(393)**
	SHM-LM-2	**Datel**	**(393)**
	SHM-LM-2M	**† Datel**	**(393)**
	SHM-6	Datel	
	SHM-6M	† Datel	
	SH-8518	DDC	
	HA-2420	**Harris**	**(746)**
	HA-2425	**† Harris**	**(746)**
	SH703	Hybrid Sys.	
	IH5110	† Intersil	
	IH5111	† Intersil	
	MN343	Micro Net	
	MN343H	† Micro Net	
	MN344	Micro Net	
	MN344H	† Micro Net	
	MN346	Micro Net	
	MN346H	† Micro Net	
	MN347	Micro Net	
	MN7130	Micro Net	
	LH0023	† National	
	LH0023C	National	
	LH0043	† National	
	LH0043C	National	
	LH0053	† National	
	LH0053C	National	
	SHM6401	National	
	LF198	† National	
	LF298	National	
	LF398	National	
	SMP81E	**PMI**	**(899)**

(Continued)

Other Linear Devices (Cont'd)

Function	Device	Source	
Sample and Hold Circuits (Cont'd.)			
	SMP81F	**PMI**	**(899)**
	CSH101A	† Teledyne C	
	4856	Teledyne P.	
Sample and Hold Circuit, with multiplexer			
	MN7130	Micro Net	
SCR/TRIAC Control (Burst Control)			
	L121	SGS	
SCR/TRIAC Control (Phase Control)			
	SL440	Plessey	
	L120	SGS	
	UAA145	Telefunken	
Serial Analog Delay (Analog storage units with read in/read out shift register) (See also Analog Shift Registers above)			
	SAD100	Reticon	
	SAD512	Reticon	
	SAD512D	Reticon	
	SAD1024A	Reticon	
(Serial) Analog Delay, Tapped (Bucket Brigade with 32 taps)			
	TAD32A	Reticon	
Serial Analog Memory (Analog storage with independent read in and read out shift registers)			
	SAM64	Reticon	
	SAM128LR	Reticon	
	SAM128V	Reticon	
Resolver System: Digital to Synchro Resolver Converter			
	9517	DDC	
	9518	DDC	
	ARAM64	Reticon	
Servo Amplifier, for motor control			
	NE543	Signetics	
	NE544	Signetics	
	NE644	Signetics	
Servo Controller, for VTR or dc servos			
	M51401	Mitsubishi	
Servo Controller, Proportional Control			
	XR2264	Exar	
	XR2265	Exar	
Sinewave Generator: See also Linear Phase Locked Loop Circuits			
	FX205	CMA	
Smoke Detectors: See Linear Consumer Circuit			
Sonar Transceiver			
	LM1812	National	
Square Law Device (two quadrant)			
	SL645C	Plessey	
Switch Driver, for power transistors			
	SG1629	† Silicon G	
	SG3629	Silicon G	
Switching Regulators. See Linear Voltage Regulators, Switching			
Tachometer: See Frequency to Voltage and Frequency Switch above			
Temperature Controlled Differential Pair			
	µA726C	Fairchild	
	µA726M	† Fairchild	

Other Linear Devices (Cont'd)

Function	Device	Source	
Temperature Transducers			
	AD590	AD	
	REF-02	**† PMI**	**(894)**
	REF-02A	**† PMI**	**(894)**
	REF-02C	**PMI**	**(894)**
	REF-02D	**PMI**	**(894)**
	REF-02E	**PMI**	**(894)**
	REF-02H	**PMI**	**(894)**
	LM134	† National	
	LM234	National	
	LM334	National	
	LM135	† National	
	LM235	National	
	LM335	National	
	LM3911	National	
	LX5600	† National	
	LX5700	† National	
	µPC3911	NEC America	
Thermal Controller, for electric blankets			
	M5172	Mitsubishi	
Thermal Converter (matched transistors, diffused resistors)			
	4131	Burr-Brown	
Threshold Switch (2/3 supply voltage)			
	MCC102	Micro Comp	
	MCC560	Micro Comp	
	MCC550	Micro Comp	
	TCA345	Siemens	
Tone Ringer (Generates ringing sound to operate a speaker)			
	S2561	**AMI**	**(376)**
Transversal Filter (Mask Programmed Weighting)			
	R5602	Reticon	
Transversal Filter, Quad Chirped (for discrete Fourier Transform and power spectral density applications)			
	R5601-1	Reticon	
	R5601-2	Reticon	
Timers: See Linear Timers			
Track and Hold			
	ADH-050	DDC	
	ADH-051	DDC	
Dual Voltage Level Alarm (activated if either input differs by more than ±5 to ±25% of selected value)			
	3041	Intech/FMI	
Quad Voltage Level Monitor/Alarm (activated if any of 4 inputs differs by more than ±5, ±10 or ±20% of selected value)			
	3040	Intech/FMI	
Voltage Detector, Indicator, Regulator, (Programmable Zener)			
	ICL8211C	Intersil	
	ICL8211M	† Intersil	
	ICL8212C	Intersil	
	ICL8212M	† Intersil	
Voltage Overvoltage Protector. (Crowbar) See Overvoltage Protector above			
Voltage to Frequency Converter			
	AD537J	AD	
	AD537K	AD	
	AD537S	† AD	
	3930	OEI	
Voltage to Frequency/Frequency to Voltage Converter			
	VFC32	Burr-Brown	
	VFC32M	† Burr-Brown	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Other Devices (Cont'd)

Other Linear Devices (Cont'd)

Function	Device	Source	Line
Voltage to Frequency/Frequency to Voltage Converter (Cont'd.)			
	VFQ-1	Datel	
	XR4151	Exar	
	XR4151M	†Exar	
	μA4151	**Fairchild** (617)	
	μA7151	**Fairchild** (617)	
	A8400	Intech/FMI	
	A8400ET-1	Intech/FMI	
	A8402	Intech/FMI	
	A8402ET-1	Intech/FMI	10
	A8404	Intech/FMI	
	3930	†OEI	
	RC4151	Raytheon	
	RM4151	†Raytheon	
	RV4151	Raytheon	
	RC4152	**Raytheon** (968)	
	RM4152	**†Raytheon** (968)	
	RV4152	**Raytheon** (968)	
	9400	Teledyne S	
Zero Voltage and Zero Crossing Triggers (Triac and SCR control)			20
	XR742	Exar	
	μA742C	Fairchild	
	M5172	Mitsubishi	
	MC3370	Motorola	
	SL447	Plessey	
	SL448	Plessey	
	SL449	†Plessey	
	CA3058	†RCA	
	CA3059	†RCA	30
	CA3079	†RCA	
	TCA280	Signetics	
	TDA1023	Signetics	
	TDA1024	Signetics	
	SG3058	†Silicon G	
	SG3059	Silicon G	
	SG3079	Silicon G	
	U106	Telefunken	
	U112	Telefunken	
	7601-01	Telenetics	40
	7603-02	Telenetics	
	TL440C	TI	
	SG7812ACT	Silicon G	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

μA4151 • μA7151

VOLTAGE-TO-FREQUENCY CONVERTER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

DESCRIPTION – The μA4151 is a monolithic building block used to convert dc voltage to digital pulses. The frequency of the output pulses is proportional to the dc input voltage.

The μA4151 consists of a voltage comparator, a monostable multivibrator and a precision switched current source (see block diagram).

The μA7151 is the same device as the μA4151 with a high performance operational amplifier on the same chip. The single supply op amp conditions the input signal and provides a significant improvement in system performance.

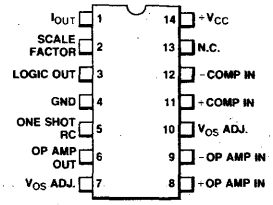
- **SINGLE SUPPLY (+8 V_{DC} TO +30 V_{DC})**
- **LINEARITY TO ±0.5%**
- **PROGRAMMABLE SCALE FACTOR**
- **PULSE OUTPUT COMPATIBLE WITH ANY LOGIC FORM**
- **TEMPERATURE STABILITY TYPICALLY ±100 ppm/°C**
- **HIGH NOISE REJECTION**
- **EASILY TRANSMITTABLE OUTPUT**
- **SIMPLE FULL-SCALE TRIM**
- **SINGLE-ENDED INPUT, REFERENCED TO GROUND**
- **ALSO PROVIDES FREQUENCY-TO-VOLTAGE CONVERSION**
- **HIGH PERFORMANCE OP AMP INCLUDED IN μA7151**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	32 V
Internal Power Dissipation	670 mW
Input Voltage (Comparator)	−0.2 V to $+V_{CC}$
Input Voltage (Op Amp)	−0.2 V to $+V_{CC}$
Logic Out Shorted-to-Ground	continuous
Op Amp Out Shorted-to-Ground	continuous
Op Amp Input Common Mode Voltage Range	+13 V to $-V_S$
Op Amp Output Voltage Range, R_L = 10 kΩ	+2 V to +13 V
Operating Temperature Range	
Military	−55°C to −125°C
Commercial	0°C to +70°C
Automotive	−45°C to +85°C
Storage Temperature Range	
Military	−65°C to +150°C
Automotive and Commercial	−55°C to +125°C
Lead Temperatures	
Molded DIP (Soldering, 10 s)	260°C
Hermetic DIP (Soldering, 60 s)	300°C

CONNECTION DIAGRAMS

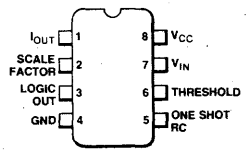
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES C P



ORDER INFORMATION

TYPE	PART NO.
μA7151	μA7151DM
μA7151	μA7151DV
μA7151	μA7151DC
μA7151	μA7151PV
μA7151	μA7151PC

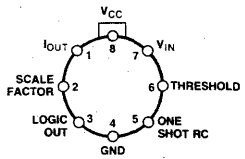
8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINES 6T 9T
PACKAGE CODES R T



ORDER INFORMATION

TYPE	PART NO.
μA4151	μA4151RM
μA4151	μA4151RV
μA4151	μA4151RC
μA4151	μA4151TV
μA4151	μA4151TC

8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA4151	μA4151HM
μA4151	μA4151HV
μA4151	μA4151HC

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464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA, 94042 (415) 962-5011/TWX 910-379-6435

FAIRCHILD

ELECTRICAL CHARACTERISTICS: V_{CC} = +15 V, T_A = 25°C unless otherwise specified.
The following specs apply to the Converter Section only.

CHARACTERISTIC	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	8.0 V < V_{CC} < 15 V	3.0	4.5	7.0	mA
	15 V < V_{CC} < 22 V	3.0	5.5	8.5	
	221 V < V_{CC} < 30 V	3.0	6.5	10.5	
Conversion Accuracy					
Scale Factor	Circuit Figure 1, V_1 = 10 V, R_S = 14 k	0.90	1.0	1.10	kHz/V
Drift with Temperature	Circuit Figure 1, V_1 = 10 V		±100		ppm/°C
Drift with V_{CC}	8.0 V < V_{CC} < 18 V		0.2		%/V
Input Comparator					
Offset Voltage			5.0	10	mV
Offset Current			±50	±100	nA
Input Bias Current			−100	−300	nA
Common Mode Range (Note 1)		0	0 to V_{CC}−2	V_{CC}−3.0	V
One-Shot					
Threshold Voltage, Pin 5		0.63	0.667	0.70	xV_{CC}
Input Bias Current, Pin 5			−100	−500	nA
Reset V_{sat}	Pin 5, 1 −2.2 mA		0.15	0.50	V
Current Source					
Output Current (V_S − 14 kΩ)	Pin 1, Figure 1, V = 0		138.7		μA
Change with Voltage	Pin 1, V = 0 V to V = 10 V		1.0	2.5	μA
Off Leakage	Pin 1, V = 0 V		1.0	50	nA
Reference Voltage	Pin 2, Figure 1	1.70	1.9	2.08	V
Logic Output					
V_{sat}	Pin 3, I = 3.0 mA		0.15	0.50	V
V_{sat}	I = 2.0 mA		0.10	0.35	V
Off Leakage			0.1	1.0	μA

NOTE:
Figure 1A – corresponds to the μA7151
Figure 1B – corresponds to the μA4151

ELECTRICAL CHARACTERISTICS: V_S = +15 V and ground T_A = 25°C unless otherwise specified.

CHARACTERISTIC	MIN	TYP	MAX	UNITS
Input Offset Voltage		2.0	5.0	mV
Input Offset Current		10	50	nA
Input Bias Current		−50	−250	nA
Input Impedance		1.0		MΩ
Common Mode Rejection Ratio	70	90		dB
Large Signal Voltage Gain, R_L = 10 k	50	200		V/mV
Slew Rate		0.6		V/μs
Power Supply Rejection Ratio		15	100	μV/V
Output Short Circuit Current	10		40	mA

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CIRCUIT DESCRIPTION

The μA7151 consists of five circuit blocks as shown in Figure 1. The blocks may be connected in a variety of ways to construct voltage-to-frequency converters (VFC), frequency-to-voltage converters (FVC), or other circuit functions. The circuit blocks are:

1. A differential input comparator featuring very high gain, low offsets, and a common mode range which includes ground.
2. A one-shot multivibrator with the time constant set by an external RC (T = 1.1RC) connected to the RC terminal, triggered by the output of the comparator being high.
3. A precision switched current source that is turned on to the value of I_{REF} when the one-shot is on and goes to zero when the one-shot is off. The current I_{REF} is set by an external R_S, connected from the scale factor terminal-to-ground and is equal to the reference voltage divided by R_S and is optimized when set to 138 μA.
4. An open collector output that provides a buffered output from the one-shot.
5. An operational amplifier whose common mode range includes ground and has offset null capability. The op amp has high gain, low offset voltage, low input currents, good PSRR and CMRR, and low drift.

PRINCIPLE OF OPERATION

Voltage to Frequency Conversion (VFC)

As a voltage to frequency converter the μA7151/4151 can be connected in several configurations depending on the input voltage, required accuracy, and response time. In all the applications we will see that the input voltage is converted to a current and the circuit will turn the switched current source on at the rate necessary so that the average current from the current source is equal to the input current. As the input voltage (and current) increases, the current source must turn on more often, and the output frequency increases.

SELECTING COMPONENTS FOR THE VFC

Voltage-to-frequency converters can be used for full scale voltages of 100 mV or greater and full scale frequencies of 1 Hz to 100 Hz. Input voltages in excess of $V_{CC}+$ can be accomodated with appropriate resistor dividers to attenuate the voltages. The following components selection guidelines should be used.

1. R_S should be approximately 14 kΩ to optimize the system performance versus temperature. R_S is normally a 12 kΩ fixed resistor and a 5 kΩ pot to be used to adjust the full scale output frequency. Small variations in R_S have minimal effect on system temperature performance. $I_{REF} = V_{REF}/R_S = 1.95\ V/R_S$
2. $R_0\ C_0$ sets the one-shot pulse width, $T_0 = 1.1\ R_0\ C_0$. This pulse width must be shorter than the minimum period of the maximum frequency ie, set it equal to .75 $(1/f_0)$. Therefore, $R_0\ C_0 = .68\ (1/f_0)$. Values of R_0 should be between 6.8 kΩ and 680 kΩ and C_0 should be from .001 μF to 1 μF.
3. R_B should be as low as possible for the highest accuracy, (this reduces the effect of current source R_{OUT}) but must be large enough to insure that the current source output is greater than $V_{IN}\ max/R_B$. Therefore, choose R_B such that $R_B \sim 1.33\ V_{IN}\ max/I_0$.
4. C_B for Figure 2 must be chosen to trade-off between accuracy and response time. Larger values of C_B give greater system accuracy but response time is limited by the $R_B\ D_B$ time constant. A good choice for D_B is $10^{-2}/f_0$.
5. C_1 for Figures 3 and 4 can be selected depending on the output frequency. The smaller C_1 is the faster the system response wil be. C_1 must be large enough to limit the amplifier swing. The op amp will swing a voltage set by I_0T_0/C_1, so if the comparator is biased at 2/3 $V_{CC}+$ this constrains $C_1 > 3\ I_0T_0/2\ V_{CC}+$. A nominal value of $C_1 = 5 \times 10^{-5}/f_0$ meets this requirement.

COMPARISON OF VOLTAGE TO FREQUENCY CIRCUITS

Table I shows a comparison of the three basic circuits set-up for a 0 to 10 V input range and a full scale output of 10 kHz.

FREQUENCY TO VOLTAGE CONVERSION

The μA7151/4151 can be connected as frequency-to-voltage converter (FVC). This circuit basically works by putting out a current pulse per cycle of input frequency and intergrating the current pulses across an output resistor to give an output voltage which is proportional to the average value of I_0 $(I_0T_0f_{IN})$.

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TABLE I

	Figure 2	Figure 3	Figure 4
Linearity	1.0%	0.2%	0.05%
Frequency Offset	+10 Hz	0	0
Response Time	135 μs	200 μs	10 μs
Input Voltage	+	+	−
Single Supply	yes	yes	yes
Split Supply	−	−	yes

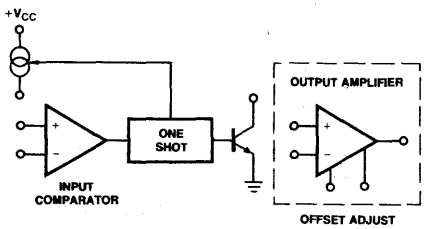


Fig. 1

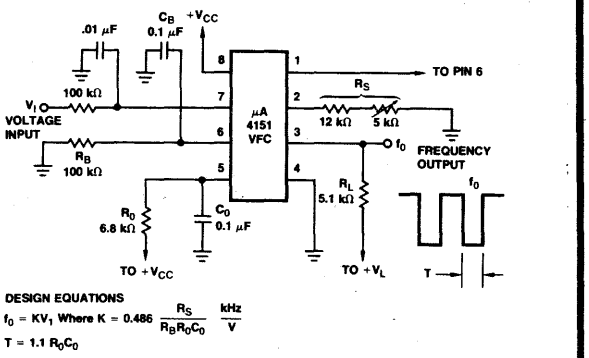


Fig. 2

PRECISION VOLTAGE TO FREQUENCY CONVERTER FOR POSITIVE INPUTS

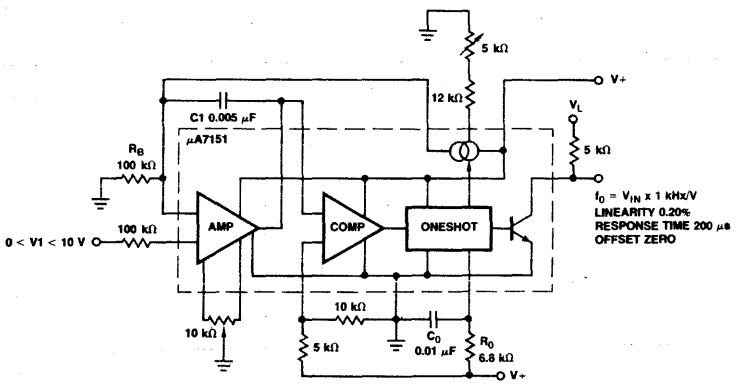


Fig. 3

PRECISION VOLTAGE TO FREQUENCY CONVERTER FOR NEGATIVE INPUTS

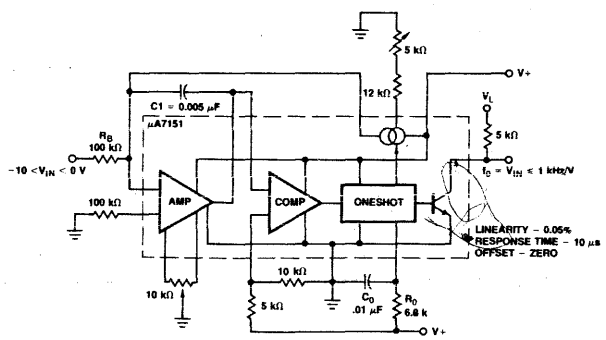


Fig. 4

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SINGLE SUPPLY FREQUENCY-TO-VOLTAGE CONVERTER

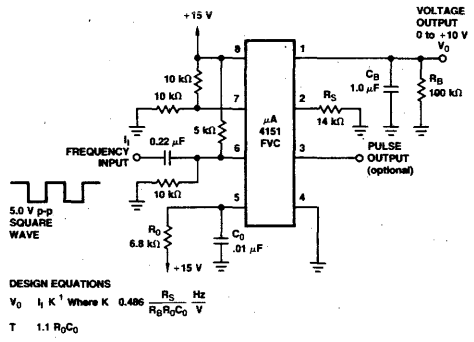


Fig. 5

PRECISION FREQUENCY TO VOLTAGE CONVERTER

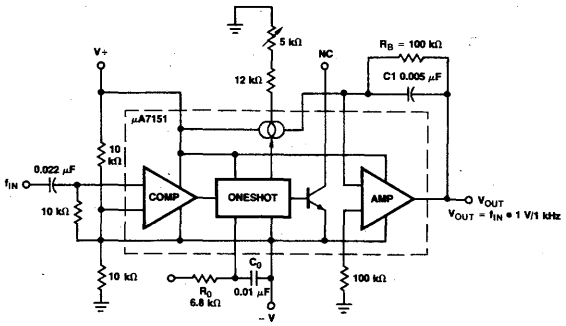


Fig. 6

LOW COST, REMOTE SENSED 8-BIT A/D CONVERTER

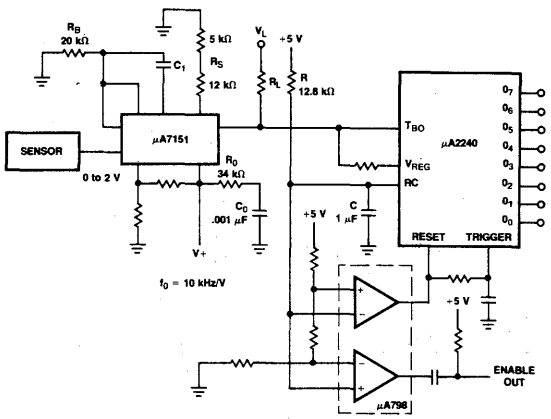


Fig. 7

MOTOR SPEED CONTROLLER

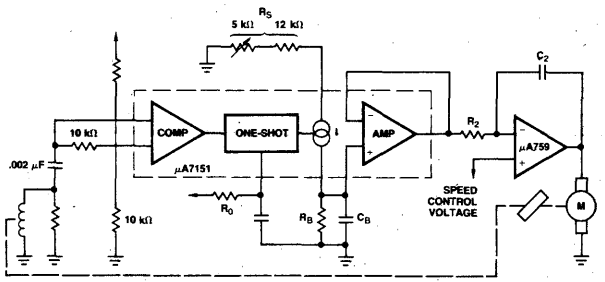


Fig. 8

FSK DEMODULATOR

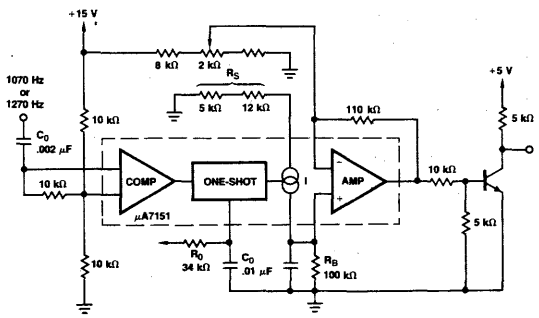


Fig. 9

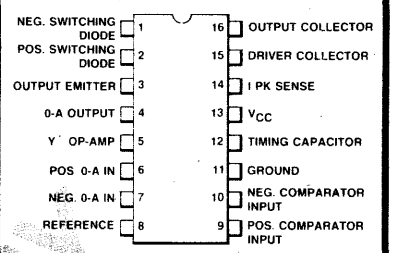
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μA78S40
UNIVERSAL SWITCHING REGULATOR SUBSYSTEM

DESCRIPTION: The uA78S40 is a Monolithic Regulator Subsystem consisting of all the active building blocks necessary for switching regulator systems. The device consists of a temperature compensated voltage reference, a duty cycle controllable oscillator with an active current limit circuit, an error amplifier, high current, high voltage output switch, a power diode and an uncommitted operational amplifier. The device can drive external npn or pnp transistors when currents in excess of 1.5 A or voltages in excess of 40 V are required. The device can be used for step down, step up or inverting switching regulators as well as for series pass regulators. It features wide supply voltage range, low standby power dissipation, high efficiency and low drift. It is useful for any stand alone, low part count switching system and works extremely well in battery operated systems.

- **STEP UP, STEP DOWN OR INVERTING SWITCHING REGULATORS**
- **OUTPUT ADJUSTABLE FROM 1.3 to 40 V**
- **OUTPUT CURRENTS TO 1.5 A WITHOUT EXTERNAL TRANSISTORS**
- **OPERATION FROM 2.5 TO 40 V INPUT**
- **LOW STANDBY CURRENT DRAIN**
- **80 dB LINE AND LOAD REGULATION**
- **HIGH GAIN, HIGH CURRENT, INDEPENDENT OP-AMP**

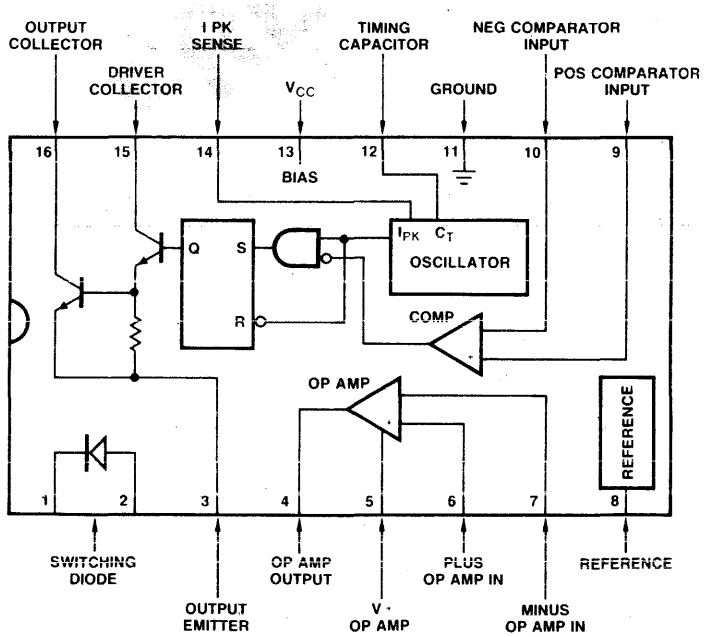
CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA78S40	μA78S40DM
μA78S40	μA78S40DC
μA78S40	μA78S40PC

EQUIVALENT CIRCUIT



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ABSOLUTE MAXIMUM RATINGS

Input voltage from V^+ to V^-	40 V	Current through Power Switch	1.5 A
Input voltage from V^+ op amp to V^-	40 V	Current through Power Diode	1.5 A
Common mode input range (Error Amplifier and Op Amp)	$-.3$ to V^+	Internal Power Dissipation (Note 2)	
Differential input voltage (Note 1)	±30 V	Plastic DIP	1500 mW
Output Short Circuit Duration (Op Amp)	continuous	Hermetic DIP	1000 mW
Current from V_{REF}	10 mA	Storage Temperature Range	−65°C to + 150°C
Voltage from Switch Collectors to GND	40 V	Operating Temperature Range	
Voltage from Switch Emitters to GND	40 V	Military (μA78S40)	−55°C to 125°C
Voltage from Switch Collectors to Emitter	40 V	Commercial (μA78S40C)	0°C to 70°C
Voltage from Power Diode to GND	40 V	Lead Temperature	
Reverse Power Diode Voltage	40 V	Hermetic DIP (Soldering, 60 s)	300°C
		Plastic DIP (Soldering, 10 s)	260°C

Note:
1. For supply voltages less than 30 V, the absolute maximum voltage is equal to the supply voltage.
2. Ratings apply to 25°C. Above 25°C ambient derate hermetic DIP at 8 mW/°C and plastic DIP at 14mW/°C.

μA78S40

ELECTRICAL CHARACTERISTICS: V_{IN} =5.0 V, $V_{Op\ Amp}$ = 5.0 V, T_A = 25°C unless otherwise noted:

CHARACTERISTIC	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS					
Supply Voltage		2.5		40	V
Supply Current	V_{IN} = 5.0 V		1.8	2.5	mA
(Op Amp Disconnected)	V_{IN} = 40 V		2.3	3.5	mA
Supply Current Op Amp	V_{IN} = 5.0 V		0.4	1.0	
	V_{IN} = 40 V		0.5	1.5	
REFERENCE SECTION					
Reference Voltage	I_{REF} = 1.0 mA	1.180	1.245	1.310	V
Reference Voltage Temperature Coefficient	I_{REF} = 1.0 mA		100		ppm/°C
Reference Voltage Line Regulation	V_{IN} = 3.0 V to V_{IN} = 40 V, I_{REF} = 1.0 mA		0.04	0.2	mV/V
Reference Voltage Load Regulation	I_{REF} = 1.0 mA to I_{REF} = 10 mA		0.2	0.2	mV/mA
OSCILLATOR SECTION					
Charging Current			25		μA
ON Time	C_T = 0.01 μF		200		μs
Discharge Current			225		μA
OFF Time	C_T = 0.01 μF		22		μs
Oscillator Voltage Swing			0.5		V
CURRENT LIMIT SECTION					
Current Limit Sense Voltage			330		mV
OUTPUT SWITCH SECTION					
Output Saturation Voltage 1	I_{SW} = 1.0 A, See Figure 1		1.1	1.3	V
Output Saturation Voltage 2	I_{SW} = 1.0 A, See Figure 2		0.45	0.7	V
Output Transistor h_{FE}	I_C = 1.0 A, V_{CE} = 5.0 V		70		
Output Leakage Current	V_{OUT} = 40 V		10		nA

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μA78S40 (Cont'd)

ELECTRICAL CHARACTERISTICS: V_{IN} =5.0 V, $V_{Op\ Amp}$ = 5.0 V, T_A = 25°C unless otherwise noted:

CHARACTERISTIC	CONDITIONS	MIN	TYP	MAX	UNITS
POWER DIODE					
Forward Voltage Drop	I_D = 1.0 A		1.25	1.5	V
Diode Leakage Current	V_D = 40 V		10		nA
COMPARATOR					
Input Offset Voltage	$V_{CM} = V_{REF}$		1.5	10	mV
Input Bias Current	$V_{CM} = V_{REF}$		35	200	nA
Input Offset Current	$V_{CM} = V_{REF}$		5.0	75	nA
Common Mode Voltage Range		0		$V^+ - 2$	V
PSRR	V_{IN} = 3.0 V to 40 V	70	96		dB
OUTPUT OPERATIONAL AMPLIFIER					
Input Offset Voltage	V_{CM} = 2.5 V		4.0	10	mV
Input Bias Current	V_{CM} = 2.5 V		30	200	mA
Input Offset Current	V_{CM} = 2.5 V		5.0	75	mA
Voltage Gain +	R_L = 2.0 k to Gnd; V_O = 1.0 to 2.5 V	25 k	250 k		V/V
Voltage Gain −	R_L = 2.0 k to V^+ Op Amp; V_O = 1.0 to 2.5 V	25 k	250 k		V/V
Common Mode Voltage Range		0		$V^+ - 2$	V
CMRR	V_{CM} = 0 to 3.0 V	76	100		dB
PSRR	V^+ Op Amp = 3.0 to 40 V	76	100		dB
Output Source Current		100	150		mA
Output Sink Current		10	35		mA
Slew Rate			0.6		V/μs
V_{OL}	I_L = −5.0 mA			1.0	V
V_{OH}	I_L = 50 mA	V^+ Op Amp −2.5 V			V

78S40 DESIGN FORMULAS

CHARACTERISTIC	STEP DOWN	STEP UP	INVERTING
I_P	$2\ I_{O\ max}$	$2\ I_{O\ max} \cdot \frac{(V_{OUT} + V_D - V_S)}{(V_{IN} - V_S)}$	$2\ I_{O\ max} \cdot \frac{(V_{IN} + V_{OUT} + V_D - V_S)}{(V_{IN} - V_S)}$
R_{SC} *	$0.33\ V/I_P$	$0.33\ V/I_P$	$0.33\ V/I_P$
t_{on}/t_{off}	$\frac{V_{OUT} + V_D}{V_{IN} - V_S - V_{OUT}}$	$\frac{V_{OUT} + V_D - V_{IN}}{V_{IN} - V_S}$	$\frac{[V_{OUT}] + V_D}{V_{IN} - V_S}$
L *	$\frac{V_{OUT} + V_D}{I_P} \cdot t_{off}$	$\frac{(V_{OUT} + V_D - V_{IN})}{I_P} \cdot t_{off}$	$\frac{([V_{OUT} + V_D])}{I_P} \cdot t_{off}$
t_{off}	$\frac{I_P \cdot L}{V_{OUT} + V_D}$	$\frac{I_P \cdot L}{V_{OUT} + V_D - V_{IN}}$	$\frac{I_P \cdot L}{[V_{OUT}] + V_D}$
C_T *	$45 \times 10^{-5}\ t_{off}$	$45 \times 10^{-5}\ t_{off}$	$45 \times 10^{-5}\ t_{off}$
C_O *	$\frac{I_P \cdot (t_{on} + t_{off})}{8\ V_{ripple}}$	$\frac{(I_P - I_{OUT})^2 \cdot t_{off}}{2\ I_P \cdot V_{ripple}}$	$\frac{(I_P - I_{OUT})^2 \cdot t_{off}}{2\ I_P \cdot V_{ripple}}$
Efficiency	$\frac{(V_{IN} - V_S + V_D)}{V_{IN}} \cdot \frac{V_{OUT}}{(V_{OUT} + V_D)}$	$\frac{(V_{IN} - V_S)}{V_{IN}} \cdot \frac{V_{OUT}}{(V_{OUT} + V_D - V_S)}$	$\frac{(V_{IN} - V_S)}{V_{IN}} \quad \frac{[V_{OUT}]}{[V_{OUT}] + V_D}$
$I_{IN\ ave}$ (Max load condition)	$\frac{I_P}{2} \cdot \frac{(V_{OUT} + V_D)}{(V_{IN} - V_S + V_D)}$	$\frac{I_P}{2}$	$\frac{I_P}{2} \cdot \frac{[V_{OUT}] + V_D}{V_{IN} + [V_{OUT}] + V_D - V_S}$

* Denotes Component Values

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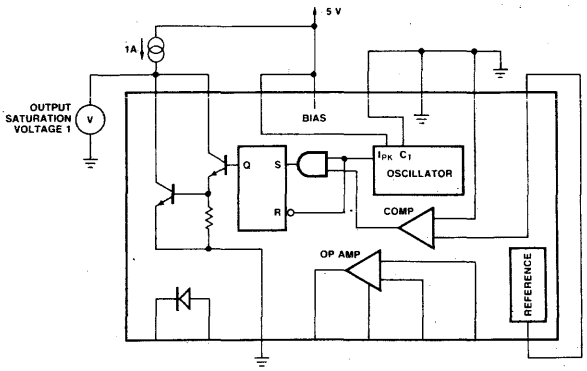


FIGURE 1

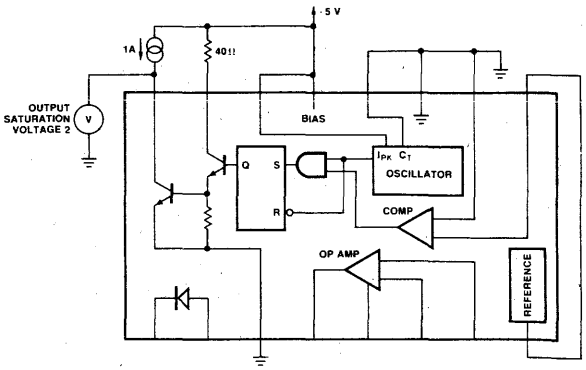
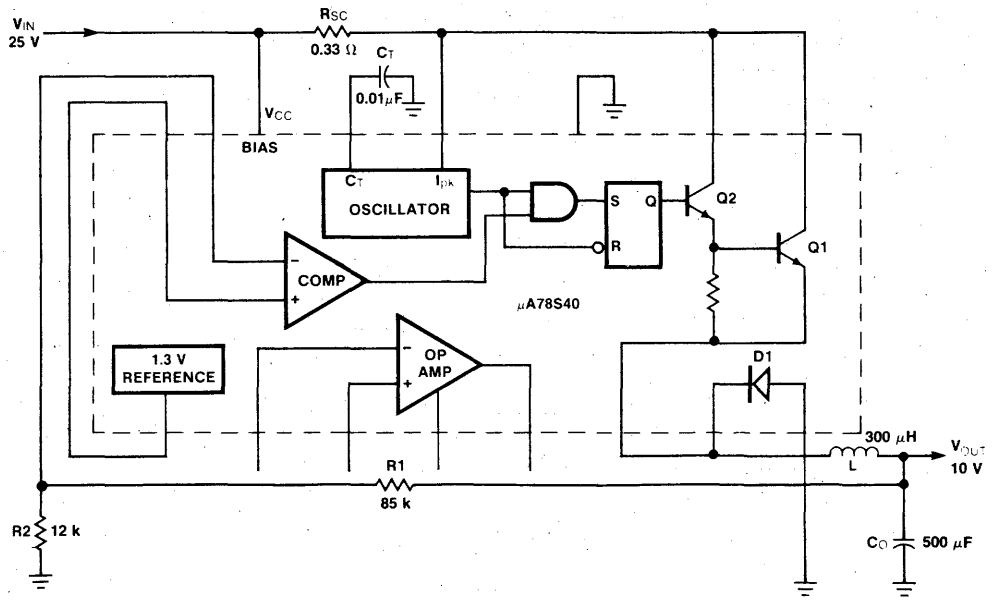


FIGURE 2

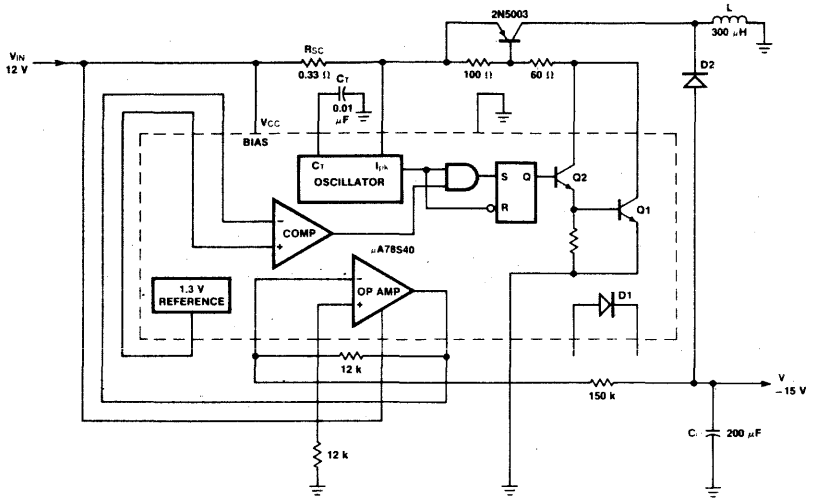


TYPICAL STEP-DOWN OPERATIONAL PERFORMANCE

T_A = 25°C

CHARACTERISTIC	CONDITION	TYPICAL VALUE
OUTPUT VOLTAGE	I_{OUT} = 200 mA	10 V
LINE REGULATION	20 ≤ V_{IN} ≤ 30 V	1.5 mV
LOAD REGULATION	5 mA ≤ I_{OUT} ≤ 300 mA	3.0 mV
MAX OUTPUT CURRENT	V_{OUT} = 9.5 V	500 mA
OUTPUT RIPPLE	I_{OUT} = 200 mA	50 mV
EFFICIENCY	I_{OUT} = 200 mA	74%
STANDBY CURRENT		2.8 mA

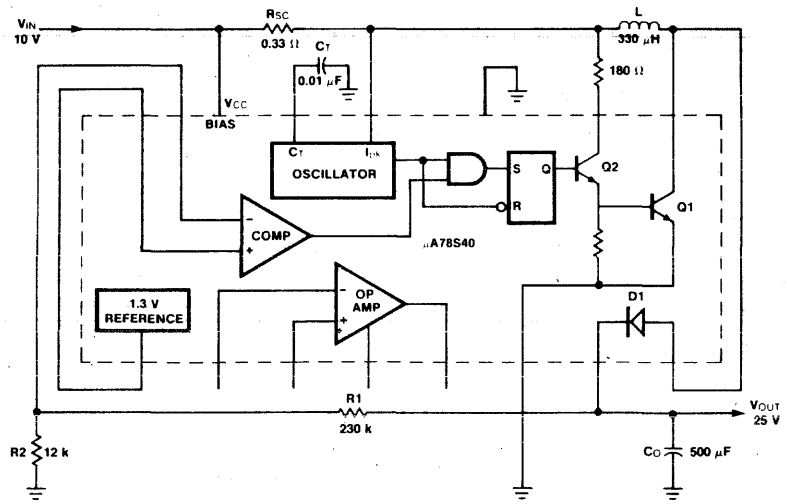
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TYPICAL INVERSION OPERATIONAL PERFORMANCE

T_A = 25°C

CHARACTERISTIC	CONDITIONS	TYPICAL VALUE
OUTPUT VOLTAGE	I_{OUT} = 100 mA	−15 V
LINE REGULATION	8 V ≤ V_{IN} ≤ 18 V	5.0 mV
LOAD REGULATION	5 mA ≤ I_{OUT} ≤ 150 mA	3.0 mV
MAX OUTPUT CURRENT	V_{OUT} = 14.25	160 mA
OUTPUT RIPPLE	I_{OUT} = 100 mA	20 mV
EFFICIENCY	I_{OUT} = 100 mA	70%
STANDBY CURRENT		2.3 mA



TYPICAL STEP-UP OPERATIONAL PERFORMANCE

T_A = 25°C

CHARACTERISTIC	CONDITION	TYPICAL VALUE
OUTPUT VOLTAGE	I_{OUT} = 500mA	25V
LINE REGULATION	5V ≤ V_{IN} ≤ 15V	4.0 mV
LOAD REGULATION	5 mA ≤ I_{OUT} ≤ 100 mA	2.0 mV
MAX OUTPUT CURRENT	V_{OUT} = 23.75	160 mA
OUTPUT RIPPLE	I_{OUT} = 50 mA	30 mV
EFFICIENCY	I_{OUT} = 50 mA	79%
STANDBY CURRENT		2.6 mA

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μA714

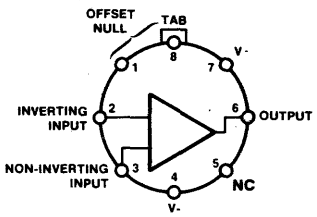
PRECISION OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

DESCRIPTION – The μA714 is a Monolithic Instrumentation Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for precise, low level signal amplification applications where low noise, low drift and accurate closed loop gain are required. The offset null capability, low power consumption, very high voltage gain as well as wide power supply voltage range provide superior performance for a wide range of instrumentation applications.

- **LOW INPUT NOISE CURRENT... 0.17 pA/√Hz @1.0 kHz max**
- **HIGH OPEN LOOP GAIN... 500,000 typically**
- **LOW INPUT OFFSET CURRENT... 2.8 nA max for μA714**
- **LOW INPUT VOLTAGE DRIFT... 0.6 μV/°C for μA714A**
- **HIGH COMMON MODE REJECTION... 100 dB min for μA714 and 714A**
- **WIDE POWER SUPPLY RANGE... ±22V**
- **OFFSET NULL CAPABILITY.**

CONNECTION DIAGRAM
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5B

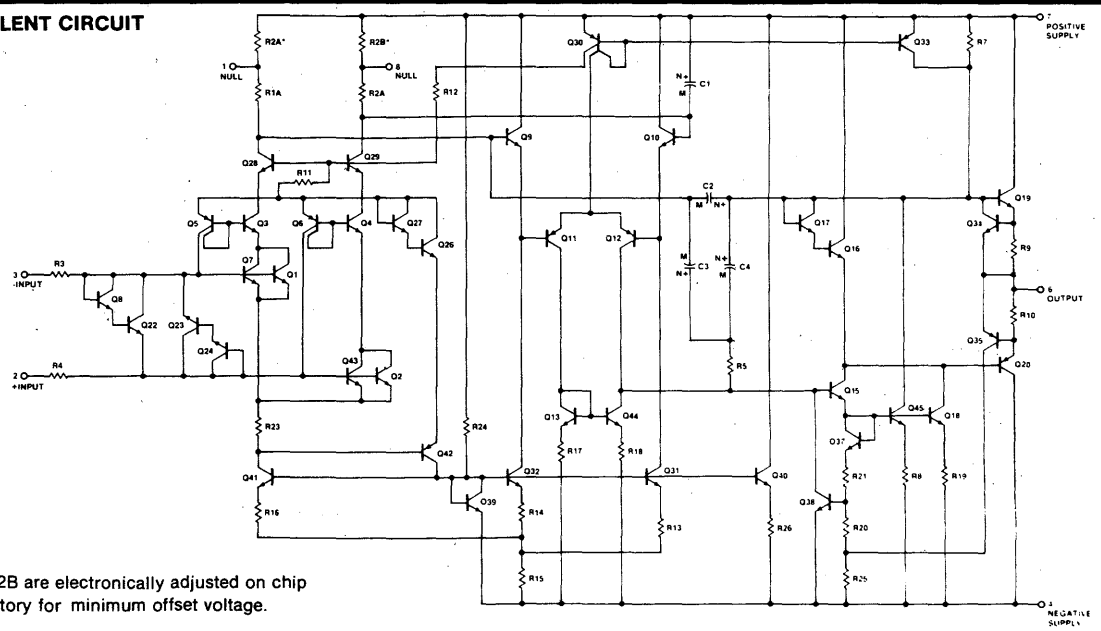


ABSOLUTE MAXIMUM RATINGS Notes on following pages	μA714A, μA714 μA714E, μA714C	μA714L
Supply Voltage	±22 V	±18 V
Internal Power Dissipation (Note 1)		
Metal Can	500 mW	500 mW
Differential Input Voltage	±30 V	±30 V
Input Voltage (Note 2)	±22 V	±18 V
Storage Temperature Range		
Metal Can	-65° to +150°C	-65°C to +150°C
Operating Temperature Range		
Military	-55°C to +125°C	
Commercial	0°C to +70°C	0° to +70°C
Lead Temperature		
Metal Can (Soldering, 60 s)	300°C	300°C

ORDER INFORMATION

TYPE	PART NO.
714	μA714HM
714A	μA714AHM
714C	μA714HC
714E	μA714EHC
714L	μA714LHC

EQUIVALENT CIRCUIT



*Note:
R2A and R2B are electronically adjusted on chip at the factory for minimum offset voltage.

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*Planar is a patented Fairchild process

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FAIRCHILD

ELECTRICAL CHARACTERISTICS μA714

These specifications apply for V_S = ±15 V, T_A = 25°C, unless otherwise noted.

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	Note 1		30	75	μV
Input Offset Current			0.4	2.8	nA
Input Bias Current			±1.0	±3.0	nA
Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.35	0.6	μV_{p-p}
Input Noise Voltage Density	f_O = 10 Hz (Note 3) f_O = 100 Hz (Note 3) f_O = 1000 Hz (Note 3)		10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
Input Noise Current	0.1 Hz to 10 Hz (Note 3)		14	30	pA p-p
Input Noise Current Density	f_O = 10 Hz (Note 3) f_O = 100 Hz (Note 3) f_O = 1000 Hz (Note 3)		0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
Input Resistance – Differential Mode		20	60		MΩ
Input Resistance – Common Mode			200		GΩ
Input Voltage Range		±13.0	±14.0		V
Common Mode Rejection Ratio	V_{CM} = ± CMVR	110	126		dB
Power Supply Rejection Ratio	V_S = ±3.0 V to ±18 V	100	110		dB
Large Signal Voltage Gain	$R_L \geq$ 2.0 kΩ, V_O = −10 V to +10 V $R_L \geq$ 500 Ω, V_O = −0.5 V to +0.5 V V_S = ±3.0 V	200 150	500 500		V/mV
Maximum Output Voltage Swing	$R_L \geq$ 10 kΩ $R_L \geq$ 2.0 kΩ $R_L \geq$ 1.0 kΩ	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		V
Slewing Rate	$R_L \geq$ 2.0 kΩ		0.25		V/μsec
Closed Loop Bandwidth	A_{VCL} = +1.0		1.2		MHz
Open Loop Output Resistance	V_O =0, I_O = 0		60		Ω
Power Consumption	V_S = ±3.0 V		75 4.0	120 6.0	mW
Offset Adjustment Range	R_P = 20 kΩ		±4.0		mV
The following specifications apply for V_S = ±15 V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.					
Input Offset Voltage	Note 1		60	200	μV
Average Input Offset Voltage Drift Without External Trim With External Trim	R_P = 20 kΩ		 0.3 0.3	 1.3 1.3	 μV/°C μV/°C
Input Offset Current			1.2	5.6	nA
Average Input Offset Current Drift			8.0	50	pA/°C
Input Bias Current			±2.0	±6.0	nA
Average Input Bias Current Drift			13	50	pA/°C
Input Voltage Range		±13.0	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ± CMVR	106	123		dB
Power Supply Rejection Ratio	V_S = ±3.0 V to ±18 V	94	106		dB
Large Signal Voltage Gain	$R_L \geq$ 2.0 kΩ, V_O = −10 V to +10 V	150	400		V/mV
Maximum Output Voltage Swing	$R_L \geq$ 2.0 kΩ	±12.0	±12.6		V

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. For supply voltage less than ±22 volts, the absolute maximum input voltage is equal to the supply voltage.
3. Parameter is not 100% tested; 90% of units meet this specification.

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ELECTRICAL CHARACTERISTICS **μA714A**

These specifications apply for $V_S = \pm 15$ V, $T_A = 25°C$, unless otherwise noted.

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	Note 1		10	25	μV
Input Offset Current			0.3	2.0	nA
Input Bias Current			±0.7	±2.0	nA
Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.35	0.6	μV_{p-p}
Input Noise Voltage Density	f_O = 10 Hz (Note 3) f_O = 100 Hz (Note 3) f_O = 1000 Hz (Note 3)		10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
Input Noise Current	0.1 Hz to 10 Hz (Note 3)		14	30	pA p-p
Input Noise Current Density	f_O = 10 Hz (Note 3) f_O = 100 Hz (Note 3) f_O = 1000 Hz (Note 3)		0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
Input Resistance – Differential Mode		30	80		MΩ
Input Resistance – Common Mode			200		GΩ
Input Voltage Range		±13.0	±14.0		V
Common Mode Rejection Ratio	V_{CM} = ± CMVR	110	126		dB
Power Supply Rejection Ratio	V_S = ±3.0 V to ±18 V	100	110		dB
Large Signal Voltage Gain	$R_L \geq$ 2.0 kΩ, V_O = −10 V to +10 V $R_L \geq$ 500 Ω, V_O = −0.5 V to +0.5 V V_S = ±3.0 V	300 150	500 500		V/mV
Maximum Output Voltage Swing	$R_L \geq$ 10 kΩ $R_L \geq$ 2.0 kΩ $R_L \geq$ 1.0 kΩ	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		V
Slewing Rate	$R_L \geq$ 2.0 kΩ		0.25		V/μsec
Closed Loop Bandwidth	A_{VCL} = +1.0		1.2		MHz
Open Loop Output Resistance	V_O =0, I_O = 0		60		Ω
Power Consumption	V_S = ±3.0 V		75 4.0	120 6.0	mW
Offset Adjustment Range	R_P = 20 kΩ		±4.0		mV
The following specifications apply for $V_S = \pm 15$ V, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.					
Input Offset Voltage	Note 1		25	60	μV
Average Input Offset Voltage Drift Without External Trim With External Trim	R_P = 20 kΩ		 0.2 0.2	 0.6 0.6	 μV/°C μV/°C
Input Offset Current			0.8	4.0	nA
Average Input Offset Current Drift			5.0	25	pA/°C
Input Bias Current			±1.0	±4.0	nA
Average Input Bias Current Drift			8.0	25	pA/°C
Input Voltage Range		±13.0	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ± CMVR	106	123		dB
Power Supply Rejection Ratio	V_S = ±3.0 V to ±18 V	94	106		dB
Large Signal Voltage Gain	$R_L \geq$ 2.0 kΩ, V_O = −10 V to +10 V	200	400		V/mV
Maximum Output Voltage Swing	$R_L \geq$ 2.0 kΩ	±12.0	±12.6		V

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. For supply voltage less than ±22 volts, the absolute maximum input voltage is equal to the supply voltage.
3. Parameter is not 100% tested; 90% of units meet this specification.

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ELECTRICAL CHARACTERISTICS **μA714C**

These specifications apply for $V_S = \pm 15$ V, $T_A = 25°C$, unless otherwise noted.

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	Note 1		60	150	μV
Input Offset Current			0.8	6.0	nA
Input Bias Current			±1.8	±7.0	nA
Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.38	0.65	μV_{p-p}
Input Noise Voltage Density	f_O = 10 Hz (Note 3) f_O = 100 Hz (Note 3) f_O = 1000 Hz (Note 3)		10.5 10.2 9.8	20.0 13.5 11.5	$nV/\sqrt{Hz}$
Input Noise Current	0.1 Hz to 10 Hz (Note 3)		15	35	pA p-p
Input Noise Current Density	f_O = 10 Hz (Note 3) f_O = 100 Hz (Note 3) f_O = 1000 Hz (Note 3)		0.35 0.15 0.13	0.90 0.27 0.18	$pA/\sqrt{Hz}$
Input Resistance – Differential Mode		8.0	33		MΩ
Input Resistance – Common Mode			120		GΩ
Input Voltage Range		±13.0	±14.0		V
Common Mode Rejection Ratio	V_{CM} = ± CMVR	100	120		dB
Power Supply Rejection Ratio	V_S = ±3.0 V to ±18 V	90	104		dB
Large Signal Voltage Gain	$R_L \geq 2.0$ kΩ, V_O = −10 V to +10 V $R_L \geq 500$ Ω, V_O = −0.5 V to +0.5 V V_S = ±3.0 V	120 100	400 400		V/mV
Maximum Output Voltage Swing	$R_L \geq 10$ kΩ $R_L \geq 2.0$ kΩ $R_L \geq 1.0$ kΩ	±12.0 ±11.5	±13.0 ±12.8 ±12.0		V
Slewing Rate	$R_L \geq 2.0$ kΩ		0.25		V/μsec
Closed Loop Bandwidth	A_{VCL} = +1.0		1.2		MHz
Open Loop Output Resistance	V_O =0, I_O = 0		60		Ω
Power Consumption	V_S = ±3.0 V		80 4.0	150 8.0	mW
Offset Adjustment Range	R_P = 20 kΩ		±4.0		mV
The following specifications apply for V_S = ±15 V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.					
Input Offset Voltage	Note 1		85	250	μV
Average Input Offset Voltage Drift Without External Trim With External Trim	R_P = 20 kΩ		 0.5 0.4	(Note 3) 1.8 1.6 (Note 3)	 μV/°C μV/°C
Input Offset Current			1.6	8.0	nA
Average Input Offset Current Drift	Note 3		12	50	pA/°C
Input Bias Current			±2.2	±9.0	nA
Average Input Bias Current Drift	Note 3		18	50	pA/°C
Input Voltage Range		±13.0	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ± CMVR	97	120		dB
Power Supply Rejection Ratio	V_S = ±3.0 V to ±18 V	86	100		dB
Large Signal Voltage Gain	$R_L \geq 2.0$ kΩ, V_O = −10 V to +10 V	100	400		V/mV
Maximum Output Voltage Swing	$R_L \geq 2.0$ kΩ	±11.0	±12.6		V

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. For supply voltage less than ±22 volts, the absolute maximum input voltage is equal to the supply voltage.
3. Parameter is not 100% tested; 90% of units meet this specification.

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ELECTRICAL CHARACTERISTICS **μA714E**

These specifications apply for V_S = ±15 V, T_A = 25°C, unless otherwise noted.

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	Note 1		30	75	μV
Input Offset Current			0.5	3.8	nA
Input Bias Current			±1.2	±4.0	nA
Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.35	0.6	μV_{p-p}
Input Noise Voltage Density	f_O = 10 Hz (Note 3) f_O = 100 Hz (Note 3) f_O = 1000 Hz (Note 3)		10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
Input Noise Current	0.1 Hz to 10 Hz (Note 3)		14	30	pA p-p
Input Noise Current Density	f_O = 10 Hz (Note 3) f_O = 100 Hz (Note 3) f_O = 1000 Hz (Note 3)		0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
Input Resistance – Differential Mode		15	50		MΩ
Input Resistance – Common Mode			160		GΩ
Input Voltage Range		±13.0	±14.0		V
Common Mode Rejection Ratio	V_{CM} = ± CMVR	106	123		dB
Power Supply Rejection Ratio	V_S = ±3.0 V to ±18 V	94	107		dB
Large Signal Voltage Gain	$R_L \geq$ 2.0 kΩ, V_O = −10 V to +10 V $R_L \geq$ 500 Ω, V_O = −0.5 V to +0.5 V V_S = ±3.0 V	200 150	500 500		V/mV
Maximum Output Voltage Swing	$R_L \geq$ 10 kΩ $R_L \geq$ 2.0 kΩ $R_L \geq$ 1.0 kΩ	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0		V
Slewing Rate	$R_L \geq$ 2.0 kΩ		0.25		V/μsec
Closed Loop Bandwidth	A_{VCL} = +1.0		1.2		MHz
Open Loop Output Resistance	V_O =0, I_O = 0		60		Ω
Power Consumption	V_S = ±3.0 V		75 4.0	120 6.0	mW
Offset Adjustment Range	R_P = 20 kΩ		±4.0		mV
The following specifications apply for V_S = ±15 V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.					
Input Offset Voltage	Note 1		45	130	μV
Average Input Offset Voltage Drift Without External Trim With External Trim	R_P = 20 kΩ		 0.3 0.3	 1.3 1.3	 μV/°C μV/°C
Input Offset Current			0.9	5.3	nA
Average Input Offset Current Drift	Note 3		8.0	35	pA/°C
Input Bias Current			±1.5	±5.5	nA
Average Input Bias Current Drift	Note 3		13	35	pA/°C
Input Voltage Range		±13.0	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ± CMVR	103	123		dB
Power Supply Rejection Ratio	V_S = ±3.0 V to ±18 V	90	104		dB
Large Signal Voltage Gain	$R_L \geq$ 2.0 kΩ, V_O = −10 V to +10 V	180	450		V/mV
Maximum Output Voltage Swing	$R_L \geq$ 2.0 kΩ	±12.0	±12.6		V

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. For supply voltage less than ±22 volts, the absolute maximum input voltage is equal to the supply voltage.
3. Parameter is not 100% tested; 90% of units meet this specification.

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ELECTRICAL CHARACTERISTICS **μA714L**

These specifications apply for V_S = ±15 V, T_A = 25°C, unless otherwise noted.

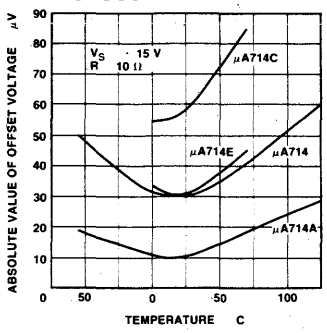
CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	Note 1		100	250	μV
Input Offset Current			5.0	20	nA
Input Bias Current			6.0	±30	nA
Input Noise Voltage Density	f_O = 10 Hz (Note 3) f_O = 100 Hz (Note 3) f_O = 1000 Hz (Note 3)		10.5 10.2 9.8		
Input Noise Current	0.1 Hz to 10 Hz (Note 3)		15		pA p-p
Input Noise Current Density	f_O = 10 Hz (Note 3) f_O = 100 Hz (Note 3) f_O = 1000 Hz (Note 3)		0.35 0.15 0.13		
Input Resistance – Differential Mode		8.0	33		MΩ
Input Resistance – Common Mode			120		GΩ
Input Voltage Range		±13.0	±14.0		V
Common Mode Rejection Ratio	V_{CM} = ± CMVR	100	120		dB
Power Supply Rejection Ratio	V_S = ±3.0 V to ±18 V	90	104		dB
Large Signal Voltage Gain	$R_L \geq$ 2.0 kΩ, V_O = −10 V to +10 V $R_L \geq$ 500 Ω, V_O = −0.5 V to +0.5 V V_S = ±3.0 V	100 50	300 150		V/mV
Maximum Output Voltage Swing	$R_L \geq$ 10 kΩ $R_L \geq$ 2.0 kΩ $R_L \geq$ 1.0 kΩ	±12.0 ±11.0	±13.0 ±12.8 ±12.0		V
Slewing Rate	$R_L \geq$ 2.0 kΩ		0.25		V/μsec
Closed Loop Bandwidth	A_{VCL} = +1.0		1.2		MHz
Open Loop Output Resistance	V_O =0, I_O = 0		60		Ω
Power Consumption	V_S = ±3.0 V		100 5.0	180 12	mW
Offset Adjustment Range	R_P = 20 kΩ		±4.0		mV
The following specifications apply for V_S = ±15 V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.					
Input Offset Voltage	Note 1			400	μV
Average Input Offset Voltage Drift Without External Trim			 1.0	(Note 3) 3.0	 μV/°C
Input Offset Current				40	nA
Average Input Offset Current Drift	Note 3		20	100	pA/°C
Input Bias Current				60	nA
Average Input Bias Current Drift	Note 3		35	150	pA/°C
Input Voltage Range		±13.0	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ± CMVR	94	120		dB
Power Supply Rejection Ratio	V_S = ±3.0 V to ±18 V	83	100		dB
Large Signal Voltage Gain	$R_L \geq$ 2.0 kΩ, V_O = −10 V to +10 V	80	400		V/mV
Maximum Output Voltage Swing	$R_L \geq$ 2.0 kΩ	±10.0	±12.6		V

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. For supply voltage less than ±22 volts, the absolute maximum input voltage is equal to the supply voltage.
3. Parameter is not 100% tested; 90% of units meet this specification.

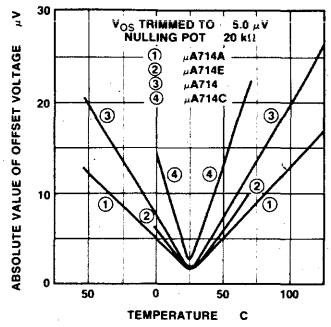
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TYPICAL PERFORMANCE CURVES

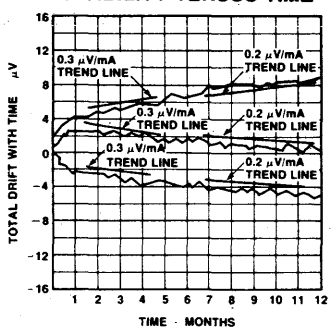
UNTRIMMED OFFSET VOLTAGE VERSUS TEMPERATURE



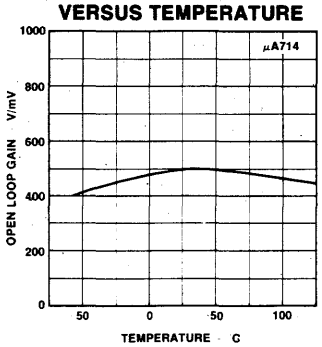
TRIMMED OFFSET VOLTAGE VERSUS TEMPERATURE



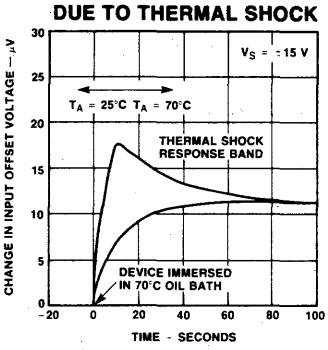
OFFSET VOLTAGE STABILITY VERSUS TIME



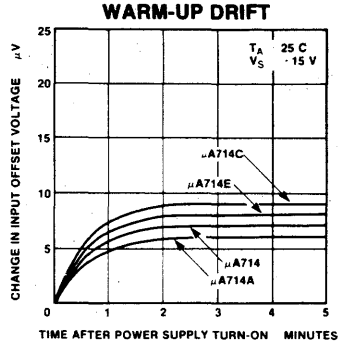
OPEN LOOP GAIN VERSUS TEMPERATURE



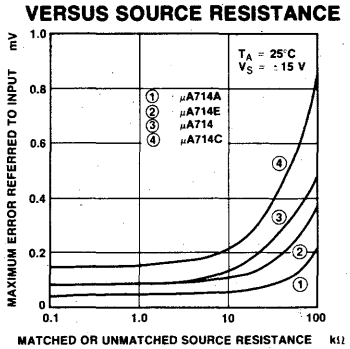
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



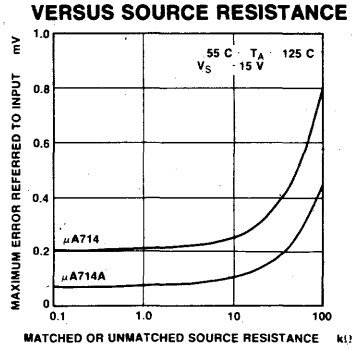
WARM-UP DRIFT



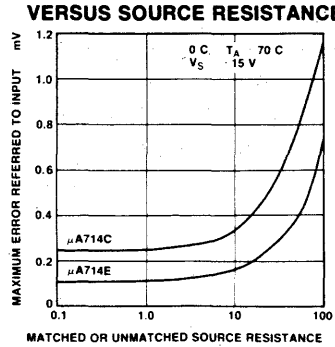
MAXIMUM ERROR VERSUS SOURCE RESISTANCE



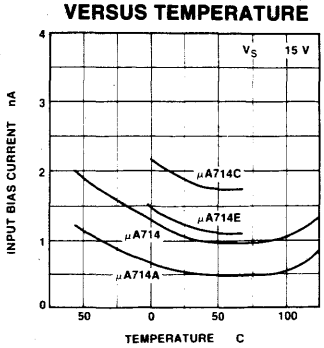
MAXIMUM ERROR VERSUS SOURCE RESISTANCE



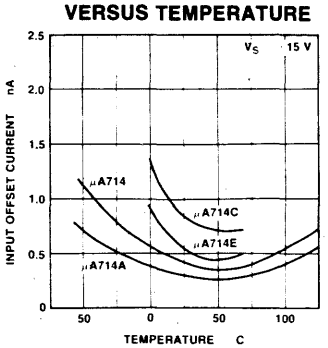
MAXIMUM ERROR VERSUS SOURCE RESISTANCE



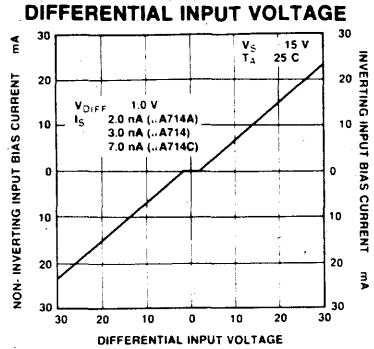
INPUT BIAS CURRENT VERSUS TEMPERATURE



INPUT OFFSET CURRENT VERSUS TEMPERATURE



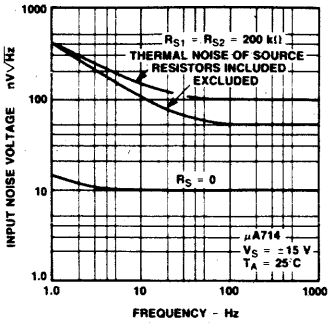
INPUT BIAS CURRENT VERSUS DIFFERENTIAL INPUT VOLTAGE



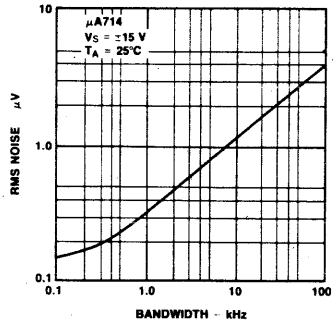
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TYPICAL PERFORMANCE CURVES

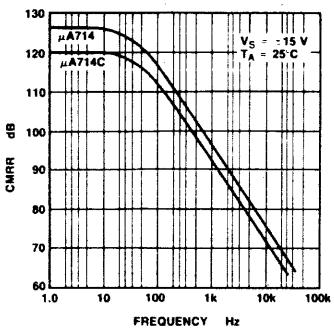
INPUT SPOT NOISE VOLTAGE VERSUS FREQUENCY



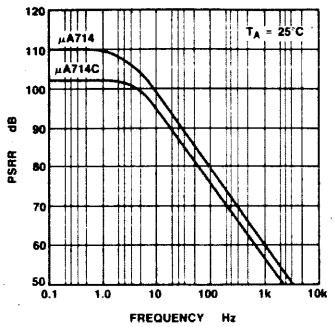
INPUT WIDEBAND NOISE VERSUS BANDWIDTH (0.1 Hz TO FREQUENCY INDICATED)



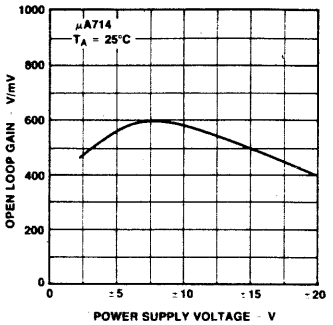
CMRR VERSUS FREQUENCY



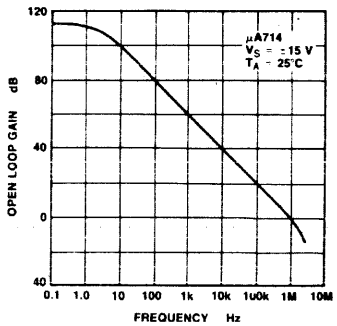
PSRR VERSUS FREQUENCY



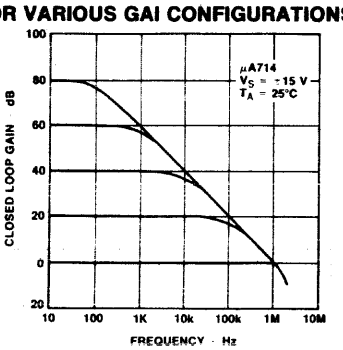
OPEN LOOP GAIN VERSUS POWER SUPPLY VOLTAGE



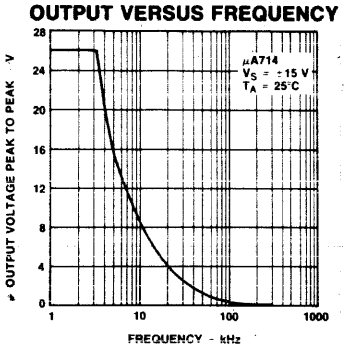
OPEN LOOP FREQUENCY RESPONSE



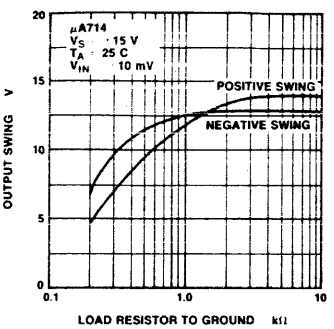
CLOSED LOOP RESPONSE FOR VARIOUS GAI CONFIGURATIONS



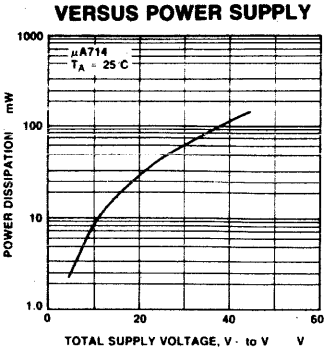
MAXIMUM UNDISTORTED OUTPUT VERSUS FREQUENCY



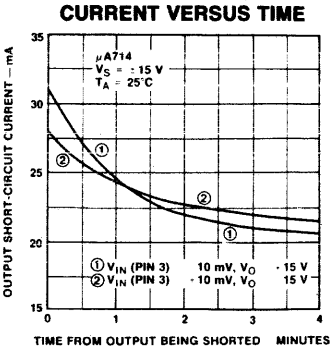
OUTPUT VOLTAGE VERSUS LOAD RESISTANCE



POWER CONSUMPTION VERSUS POWER SUPPLY



OUTPUT SHORT CIRCUIT CURRENT VERSUS TIME



Fairchild cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in a Fairchild product. No other circuit patent licenses are implied.
Manufactured under one of the following U.S. Patents: 2981877, 3015048, 3064167, 3108359, 3117260; other patents pending.

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μA78C00 SERIES

3-TERMINAL POSITIVE VOLTAGE REGULATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA78C00 series of 3-Terminal Positive Voltage Regulators is constructed using the Fairchild Planar* epitaxial process. This series is designed to meet the special environmental reliability and low drift requirements for high volume cost effective product applications. On card regulation eliminates the distribution problems associated with a central power supply. The 3-terminal IC voltage regulators employ internal current limiting, thermal shutdown and safe area compensation that make these IC voltage regulators virtually indestructable. The 78C00 provides improved line and load regulation as well as high ripple rejection. The performance standards meet all Domestic, Continental and Far East consumer product electrical standards.

The fixed voltage series designated 78C00 is available in 12 options from 8-24 V and is capable of delivering 500 mA.

A 0.33 μF decoupling capacitor should be used at the input pin. A 0.1 μF capacitor at the output pin will improve the transient response.

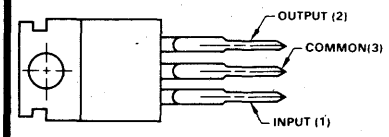
- **OUTPUT CURRENT IN EXCESS OF 0.5 A**
- **EXCELLENT TRANSIENT RESPONSE**
- **1/2% LOAD AND LINE REGULATION**
- **MAX DROPOUT VOLTAGE 2.5 V**
- **NO EXTERNAL COMPONENTS REQUIRED**
- **OUTPUT TRANSISTOR SAFE AREA PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT LIMIT**
- **LOW OUTPUT IMPEDANCE**

ABSOLUTE MAXIMUM RATINGS

Input Voltage	
(V_O 8 V thru 18 V)	35 V
(V_O 20 V thru 24 V)	40 V
Internal Power Dissipation	Internally Limited
Operating Temperature Range	0°C to +125°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 s)	230°C
Maximum Power Dissipation (P_D)	7.5 W

*Planar is a patented Fairchild process.

CONNECTION DIAGRAM
TO-220 Package
(TOP VIEW)
PACKAGE OUTLINE GH
PACKAGE CODE U



ORDER INFORMATION

TYPE	PART NO.
8.0 V	μA78C08UC
8.2 V	μA78C82UC
10.0 V	μA78C10UC
12.0 V	μA78C12UC
15.0 V	μA78C15UC
17.0 V	μA78C17UC
18.0 V	μA78C18UC
20.0 V	μA78C20UC
22.0 V	μA78C22UC
24.0 V	μA78C24UC

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464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA, 94042 (415) 962-5011/TWX 910-379-6435

FAIRCHILD

ELECTRICAL CHARACTERISTICS: I_O = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.3 μF, C_O = 0.1 μF, V_{IN} = V_O + 5 V unless otherwise specified (Note 1)

SYMBOL	CHARACTERISTIC	CONDITIONS	8 V			8.2 V			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	T_J = 25°C	7.7	8.0	8.3	7.9	8.2	8.5	V
		5 mA ≤ I_O ≤ 350 mA 2.5 V ≤ V_{IN} - V_O ≤ 15 V (V_{IN} Max = 35 V)	7.6		8.4	7.8		8.6	V
ΔV_O	Line Regulation	T_J = 25°C, V_{IN} = 8 -25 V V_{IN} = 9 -25 V V_{IN} = 11-21 V			 50			50	mV
ΔV_O	Load Regulation	T_J = 25°C, 5 mA < I_O < 500 mA			80			82	mV
		T_J = 25°C, 100 mA < I_O < 300 mA			40			40	mV
I_O	Quiescent Current	T_J = 25°C, I_O = 0		2.5	6.0		2.5	6.0	mA
ΔI_O	Quiescent Current Change	3 V ≤ V_{IN} - V_O ≤ 13 V			0.8			0.8	mA
		5 mA to 500 mA			0.5			0.5	mA
e_n	Output Noise Voltage	T_J = 25°C, 10 Hz ≤ f ≤ 100 kHz		200			200		μV
$\frac{\Delta V_{IN}}{\Delta V_O}$	Ripple Rejection	T_J = 25°C, 3 V ≤ V_{IN} -V_O≤ 13 V (V_{IN} Max = 39 V), f = 120 Hz	46	54		46	54		dB
	Dropout Voltage V_{IN} - V_O	T_J = 25°C, Note 3			2.5			2.5	V
I_{SC}	Short Circuit Current	T_J = 25°C, V_{IN} = 35 V, Note 2		400			400		mA
I_O Max	Peak Output Current	T_J= 25°C, V_{IN} - V_O= 8 V		1.0			1.0		A
$\frac{\Delta V_O}{\Delta T}$	Avg. Temp. Coefficient of Output Voltage			-2.1			-2.2		mV/°C
Cont'd)			10 V			12 V			
V_O	Output Voltage	T_J = 25°C	9.6	10	10.4	11.5	11	12.5	V
		5 mA ≤ I_O ≤ 350 mA 2.5 V ≤ V_{IN} - V_O ≤ 15 V (V_{IN} Max = 35 V)	9.5		10.5	11.4		12.6	V
ΔV_O	Line Regulation	T_J = 25°C, V_{IN} = 12-22 V V_{IN} = 14-24 V V_{IN} = 15-25 V			50			 50	mV
ΔV_O	Load Regulation	T_J = 25°C, 5 mA < I_O < 500 mA			100			120	mV
		T_J = 25°C, 100 mA < I_O < 300 mA			50			60	mV
I_O	Quiescent Current	T_J = 25°C, I_O = 0		2.5	6.0		2.5	6.0	mA
ΔI_O	Quiescent Current Change	3 V ≤ V_{IN} - V_O ≤ 13 V			0.8			0.8	mA
		5 mA to 500 mA			0.5			0.5	mA
e_n	Output Noise Voltage	T_J = 25°C, 10 Hz ≤ f ≤ 100 kHz		250			300		μV
$\frac{\Delta V_{IN}}{\Delta V_O}$	Ripple Rejection	T_J = 25°C, 3 V ≤ V_{IN} - V_O ≤ 13 V, (V_{IN} Max = 39 V), f = 120 Hz	46	54		46	54		dB
	Dropout Voltage V_{IN} - V_O	T_J = 25°C, Note 3			2.5			2.5	V
I_{SC}	Short Circuit Current	T_J = 25°C, V_{IN} = 35 V, Note 2		400			400		mA
I_O Max	Peak Output Current	T_J = 25°C, V_{IN} - V_O = 8 V		1.0			1.0		A
$\frac{\Delta V_O}{\Delta T}$	Avg. Temp. Coefficient of Output Voltage			-2.3			-2.3		mV/°C

NOTES:
1. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.
2. Refer to peak output current vs Δ(V_{IN} - V_{OUT}) curves for temperature relationships.
3. Dropout voltage is defined as that input-output voltage differential which causes the output voltage to decrease by 5% of its initial value.

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ELECTRICAL CHARACTERISTICS: I_O = 350 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.3 μF, C_O = 0.1 μF, V_{IN} = V_O + 5 V unless otherwise specified (Note 1)

SYMBOL	CHARACTERISTIC	CONDITIONS	15 V			17 V			18 V			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	T_J = 25°C	14.4	15	15.6	16.3	17	17.7	17.3	18	18.7	V
		5 mA ≤ I_O ≤ 350 mA 2.5 V ≤ V_{IN} − V_O ≤ 15 V (V_{IN} Max = 39 V)	14.25		15.75	16.15		17.85	17.1		18.9	V
ΔV_O	Line Regulation	T_J = 25°C, V_{IN} = 20-30 V V_{IN} = 21-31 V V_{IN} = 22-32 V			50			50			50	mV
ΔV_O	Load Regulation	T_J = 25°C, 5 mA < I_O < 500 mA			150			170			180	mV
		T_J = 25°C, 100 mA < I_O < 300 mA			75			85			90	mV
I_O	Quiescent Current	T_J = 25°C, I_O = 0		2.5	6.0		2.5	6.0		2.5	6.0	mA
ΔI_O	Quiescent Current Change	3 V ≤ V_{IN} − V_O ≤ 13 V			0.8			0.8			0.8	mA
		5 mA to 500 mA			0.5			0.5			0.5	mA
e_n	Output Noise Voltage	T_J = 25°C, 10 Hz ≤ f ≤ 100 kHz		375			400			450		μV
$\frac{\Delta V_{IN}}{\Delta V_O}$	Ripple Rejection	T_J = 25°C, 3 V ≤ V_{IN}−V_O ≤ 13 V (V_{IN} Max = 39 V), f = 120 Hz	46	54		46	54		46	54		dB
	Dropout Voltage V_{IN} − V_O	T_J = 25°C, Note 3			2.5			2.5			2.5	V
I_{SC}	Short Circuit Current	T_J = 25°C, V_{IN} = 35 V, Note 2		400			400			400		mA
I_OMax	Peak Output Current	T_J = 25°C, V_{IN} − V_O = 8 V		1.0			1.0			1.0		A
$\frac{\Delta V_O}{\Delta T}$	Avg. Temp. Coefficient of Output Voltage			−4.0			−4.5			−4.8		mV/°C

(Cont'd)			20 V			22 V			24 V			
V_O	Output Voltage	T_J = 25°C	19.2	20	20.8	21.1	22	22.9	23	24	25	V
		5 mA ≤ I_O ≤ 350 mA 2.5 V ≤ V_{IN} − V_O ≤ 15 V (V_{IN} Max = 39 V)	19		21	20.9		23.1	22.8		25.2	V
ΔV_O	Line Regulation	T_J = 25°C, V_{IN} = 24-34 V V_{IN} = 26-36 V V_{IN} = 28-38 V			50			50			50	mV
ΔV_O	Load Regulation	T_J = 25°C, 5 mA < I_O < 500 mA			200			220			240	mV
		T_J = 25°C, 100 mA < I_O < 300 mA			100			110			120	mV
I_O	Quiescent Current	T_J = 25°C, I_O = 0		2.5	6.0		2.5	6.0		2.5	6.0	mA
ΔI_O	Quiescent Current Change	3 V ≤ V_{IN} − V_O ≤ 13 V			0.8			0.8			0.8	mA
		5 mA to 500 mA			0.5			0.5			0.5	mA
e_n	Output Noise Voltage	T_J = 25°C, 10 Hz ≤ f ≤ 100 kHz		500			550			600		μV
$\frac{\Delta V_{IN}}{\Delta V_O}$	Ripple Rejection	T_J = 25°C, 3 V ≤ V_{IN}−V_O ≤ 13 V (V_{IN} Max = 39 V), f = 120 Hz	46	54		46	54		46	54		dB
	Dropout Voltage V_{IN} − V_O	T_J = 25°C, Note 3			2.5			2.5			2.5	V
I_{SC}	Short Circuit Current	T_J = 25°C, V_{IN} = 35 V, Note 2		400			400			400		mA
I_OMax	Peak Output Current	T_J = 25°C, V_{IN} − V_O = 8 V		1.0			1.0			1.0		A
$\frac{\Delta V_O}{\Delta T}$	Avg. Temp. Coefficient of Output Voltage			−5.3			−6.0			−6.4		mV/°C

NOTES:
1. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.
2. Refer to peak output current vs Δ(V_{IN} − V_{OUT}) curves for temperature relationships.
3. Dropout voltage is defined as that input-output voltage differential which causes the output voltage to decrease by 5% of its initial value.

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DESIGN CONSIDERATIONS

The μA78C00 fixed voltage regulator series has thermal overload protection from excessive power, internal short circuit protection which limits the circuit's maximum current, and output transistor safe area compensation for reducing the output short circuit current as the voltage across the pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (125°C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

PACKAGE	TYP θ_{JC}	MAX θ_{JC}	TYP θ_{JA}	MAX θ_{JA}
Power Watt	4.0	7.0	75	80

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \text{ (Without a heat sink)}$$

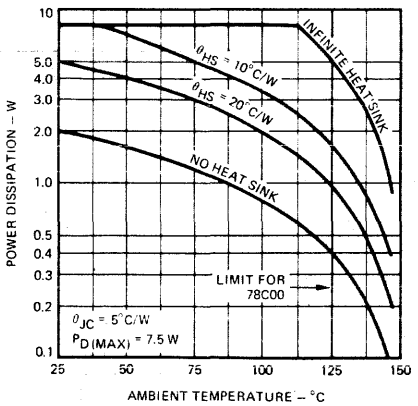
$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving for T_J: $T_J = T_A + P_D (\theta_{JC} + \theta_{CA})$ or $T_A + P_D \theta_{JA}$ (Without heat sink)

Where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JA} = Junction to ambient thermal resistance
θ_{JC} = Junction to case thermal resistance
θ_{CA} = Case to ambient thermal resistance
θ_{CS} = Case to heat sink resistance
θ_{SA} = Heat sink to ambient thermal resistance

WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

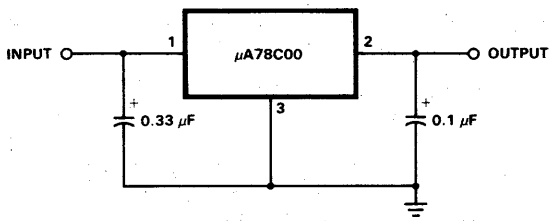


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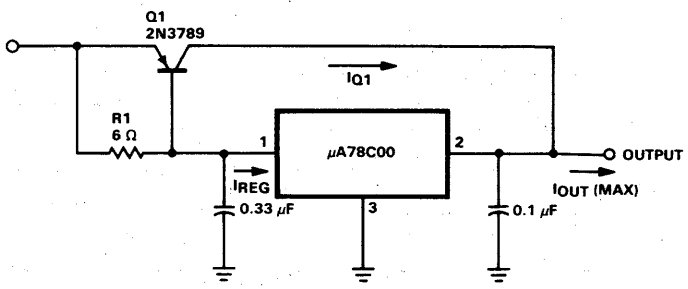
TYPICAL APPLICATIONS

In many μA78C00 applications, compensation capacitors may not be required. However, for stable operation of the regulator over all input voltage and output current ranges, bypassing of the input and output (0.33 μF and 0.1 μF, respectfully) is recommended. Input bypassing is necessary if the regulator is located far from the filter capacitor of the power supply. Bypassing the output will improve the transient response of the regulator.

FIXED OUTPUT REGULATOR



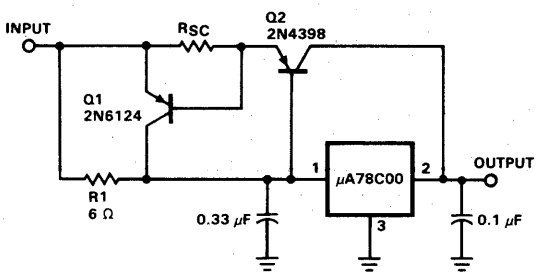
HIGH CURRENT VOLTAGE REGULATOR



$$R1 = \frac{V_{BE(Q1)}}{I_{REG}} = \frac{\beta V_{BE(Q1)}}{I_{REQ(MAX)}\ (\beta + 1) - I_{OUT(MAX)}}$$

$$\beta_{Q1} \geqslant \frac{I_{OUT}}{I_{REG}}$$

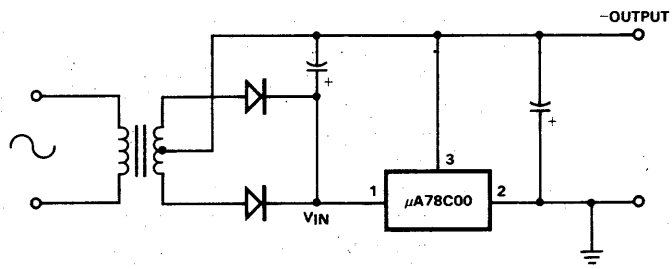
HIGH OUTPUT CURRENT, SHORT CIRCUIT PROTECTED



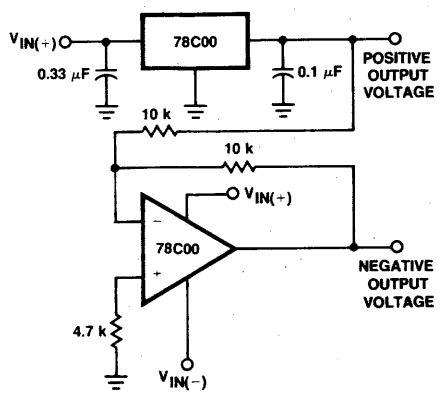
$$R1 = \frac{\beta V_{BE(Q1)}}{I_{REQ(MAX)}\ (\beta + 1) - I_{OUT(MAX)}}$$

$$R_{SC} = \frac{V_{BE(Q1)}}{I_{OUT(MAX)}}$$

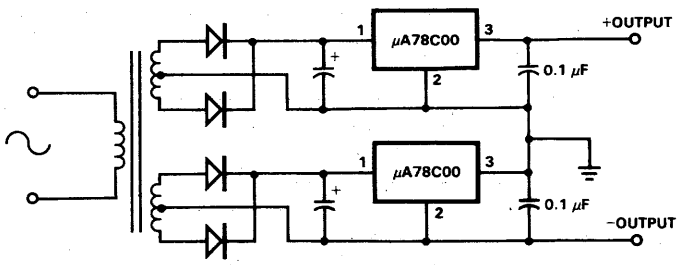
NEGATIVE OUTPUT VOLTAGE CIRCUIT



± TRACKING VOLTAGE REGULATOR



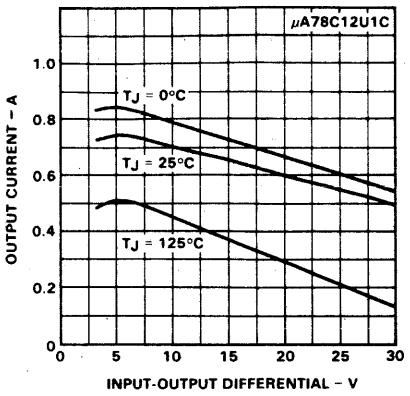
POSITIVE AND NEGATIVE REGULATOR



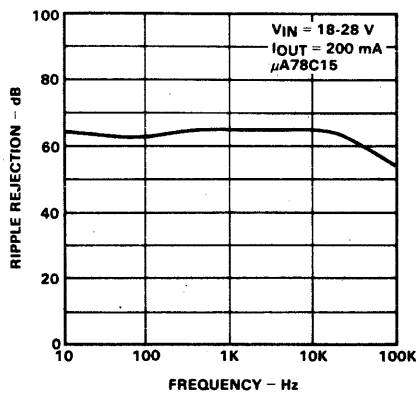
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ELECTRICAL PERFORMANCE CURVES

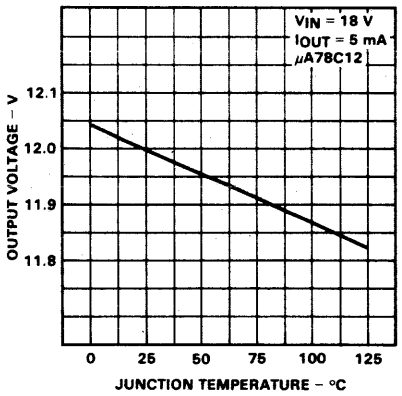
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE



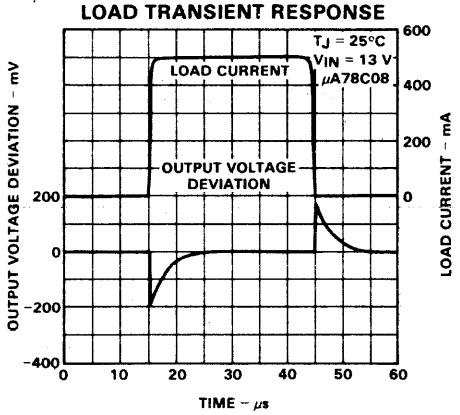
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



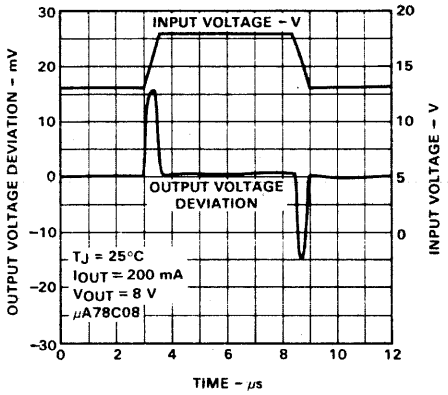
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



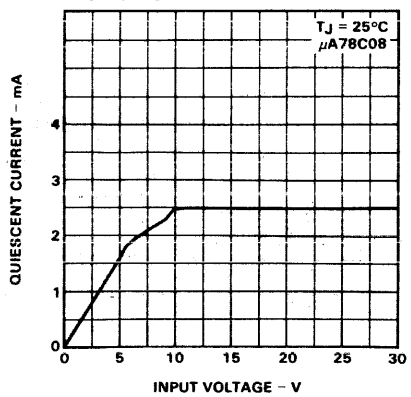
LOAD TRANSIENT RESPONSE



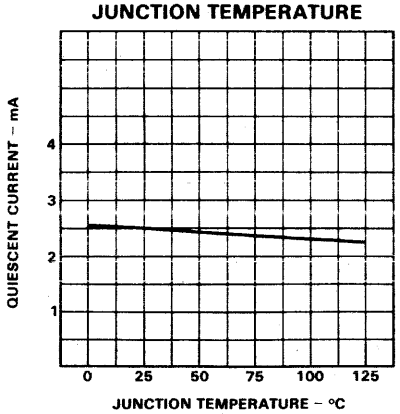
LINE TRANSIENT RESPONSE



QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



QUIESCENT CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE



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μA78C00 FIXED VOLTAGE VOLTAGE REGULATOR

Figure 1 shows the equivalent circuit of the μA78C00 regulator. The reference is derived from Zener diode D1 and compensated by the base-emitter voltage of the error amplifier Q4. Additional gain is provided by Q7 and Q8 to the Darlington-connected emitter-follower output stage of Q10 and Q11. The output stage is compensated by capacitor C1. A positive start-up condition is ensured by FET transistor Q1 to provide base current to transistors Q2 and Q5. Q2, Q5 and Q6 then form a positive feedback loop which raises the base voltage of Q2 until the reference Zener D1 conducts. Thermal overload protection is achieved by transistor Q3. The bias to the base-emitter voltage of Q3 is derived from D1 via Q2 and the divider network of R1 and R2. At high junction temperatures, Q3 turns on and removes the drive to the output stage. Current-limit transistor Q9 protects the device against accidental shorts by sensing the voltage drop across R7 while Zener diode D2 along with Q9 and resistors R5, R6 and R7 limit the power dissipation to a safe value.

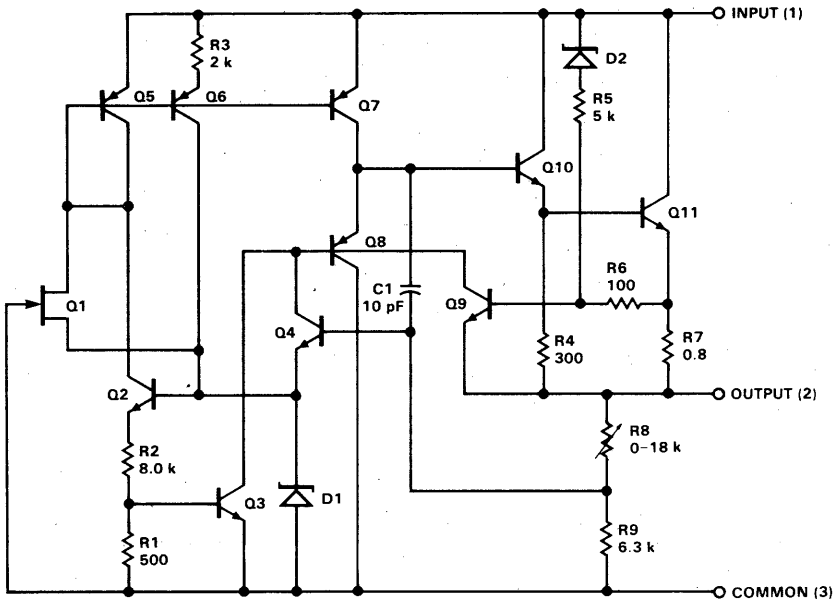
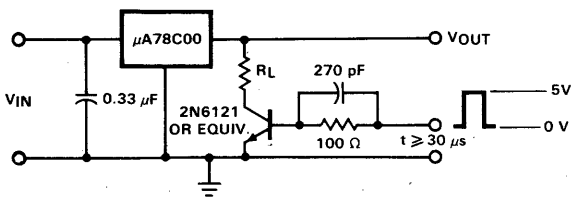
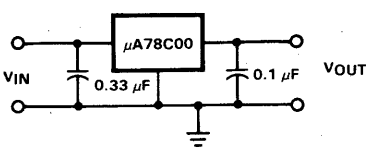


Fig. 1
SCHEMATIC DIAGRAM
FIXED VOLTAGE 3-TERMINAL VOLTAGE REGULATOR

TEST CIRCUITS



LOAD REGULATION TEST CIRCUIT

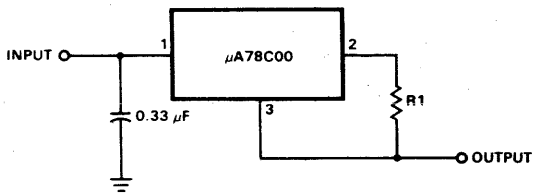


DC PARAMETER TEST CIRCUIT

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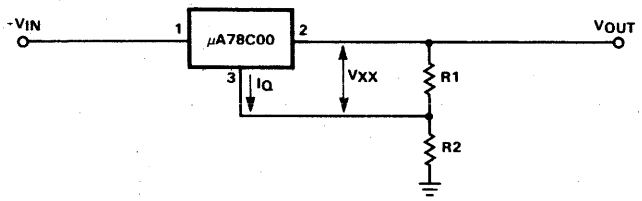
TYPICAL APPLICATIONS (Cont'd)

CURRENT REGULATOR



$$\text{Output Current} = \frac{V_{OUT}}{R1}$$

CIRCUIT FOR INCREASING OUTPUT VOLTAGE



$$V_{OUT} = V_{XX}\left(1 + \frac{R2}{R1}\right) + I_Q R2$$

Fairchild cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in a Fairchild product. No other circuit patent licenses are implied.
Manufactured under one of the following U.S. Patents: 2981877, 3015048, 3064167, 3108359, 3117260; other patents pending.

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TDA2002 • TDA2002A

8 WATT AUDIO POWER AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

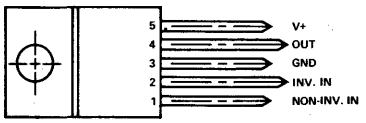
GENERAL DESCRIPTION – The TDA2002 and TDA2002A are monolithic integrated circuits designed for class B audio power amplifier applications using low impedance loads (down to 1.6 Ω). They are constructed using the Fairchild Planar* epitaxial process. The devices typically provide 8 W at 14.4 V, 2 Ω and 6.5 W at 16 V, 4 Ω.

The TDA2002 and TDA2002A are provided in a 5-pin power package, with two pin configurations (H and V) for ease in mounting either horizontally or vertically in the PC board.

The TDA2002A is the same electrically as the TDA2002 except it does not include the overvoltage (Load dump) protection circuit.

- **THERMAL SHUT DOWN**
- **SHORT CIRCUIT PROTECTION**
- **OVERVOLTAGE PROTECTION (TDA2002)**
- **LOW EXTERNAL COMPONENTS**
- **HIGH CURRENT CAPABILITY (3.5 A)**
- **MINIMUM SPACE REQUIREMENT**
- **WIDE SUPPLY VOLTAGE RANGE (8 V to 18 V)**

CONNECTION DIAGRAM
5-PIN POWER PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GO
PACKAGE CODE H, V



ORDER INFORMATION

TYPE	PART NO.
2002H	TDA2002H
2002V	TDA2002V
2002AH	TDA2002AH
2002AV	TDA2002AV

ABSOLUTE MAXIMUM RATINGS

	TDA2002	TDA2002A
Peak Supply Voltage (50 ms)	40 V	---
Supply Voltage	28 V	28 V
Operating Supply Voltage	18 V	18 V
Output Current (Repetitive)	3.5 A	3.5 A
Output Current (Non-Repetitive)	4.5 A	4.5 A
Power Dissipation: at $T_C = 90^\circ C$	15 W	15 W
Storage Temperature	–40 to 150°C	–40 to 150°C
Lead Temperature (Soldering 10 s)	260°C	260°C

* Planar is a patented Fairchild Process.

THERMAL DATA

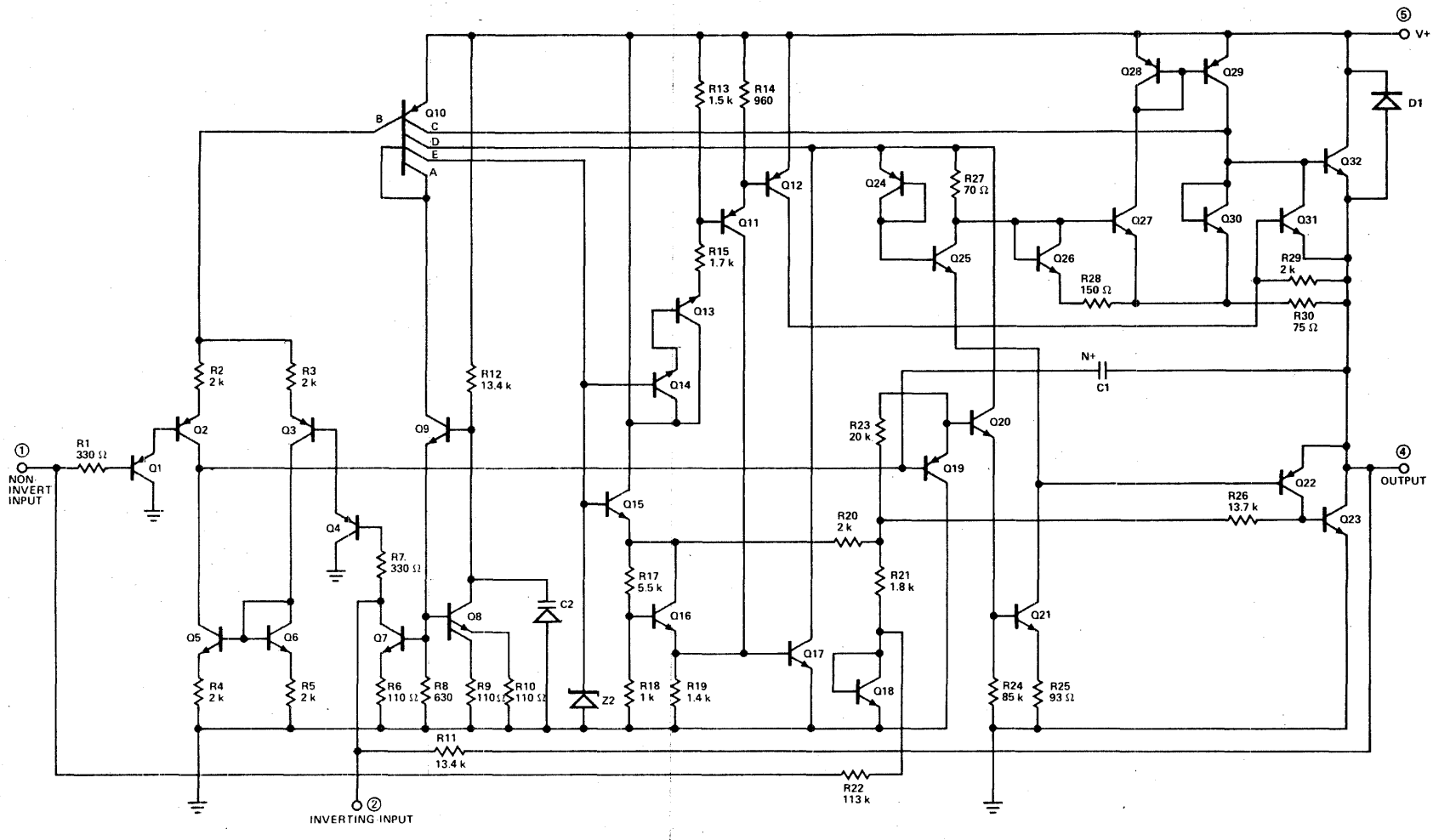
θ_{JC} Thermal resistance junction to case (max) 4°C/W

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464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA, 94042 (415) 962-5011/TWX 910-379-6435

FAIRCHILD

EQUIVALENT CIRCUIT



GND = Pin 3
○ = Pin Numbers

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ELECTRICAL CHARACTERISTICS: V+ = 14.4 V, T_A + 25°C, unless otherwise specified; see test circuit

CHARACTERISTIC	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Output Voltage (Pin 4)		6.4	7.2	8.0	V
Quiescent Drain Current (Pin 5)			45	80	mA
Power Output	THD = 10% A_V = 100 f = 1 kHz				
	V+ = 16 V R_L = 4 Ω		6.5		W
	V+ = 16 V R_L = 2 Ω		10		W
	V+ = 14.4 V R_L = 4 Ω	4.8	5.2		W
	V+ = 14.4 V R_L = 2 Ω	7	8		W
Input Saturation Voltage (rms)		600			mV
Input Sensitivity	A_V = 100 f = 1 kHz				
	P_{OUT} = .5 W R_L = 4 Ω		15		mV
	P_{OUT} = .5 W R_L = 2 Ω		11		mV
	P_{OUT} = 5.2 W R_L = 4 Ω		55		mV
	P_{OUT} = 8 W R_L = 2 Ω		50		mV
Frequency Response (−3 dB)	R_L = 4 Ω C_{FB} = 39 nF R_{FB} = 39 Ω See Figs 15, 19		40–15000		Hz
Total Harmonic Distortion	A_V = 100 f = 1 kHz				
	P_{OUT} = 0.05-3.5 W (R_L = 4 Ω)		0.2		%
	P_{OUT} = 0.05-5 W (R_L = 2 Ω)		0.2		%
Input Resistance (Pin 1)	f = 1 kHz	70	150		kΩ
Voltage Gain					
(open loop)	f = 1 kHz R_L = 4 Ω		80		dB
(closed loop)		39.5	40	40.5	dB
Input Noise Voltage	BW (−3dB) = 40–15000 Hz Note 1		4		μV
Input Noise Current			60		pA
Efficiency	A_V = 100 f = 1 kHz				
	P_{OUT} = 5.2 W R_L = 4 Ω		68		%
	P_{OUT} = 8 W R_L = 4 Ω		58		%
Supply Voltage Rejection Ratio	AV = 100 R_L = 4 Ω R_g = 10 kΩ f_{ripple} = 100 Hz V_{ripple} = 0.5 V	30	35		dB

Note 1: Bandwidth (−3 dB) of test equipment = 10-25000 Hz

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TYPICAL PERFORMANCE CURVES

QUIESCENT OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

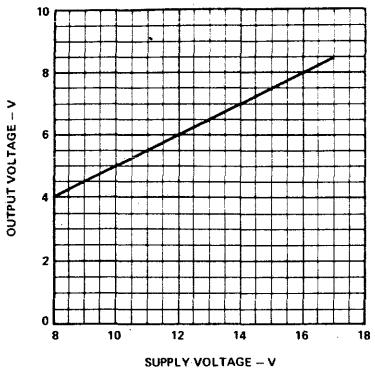


Fig. 1

QUIESCENT DRAIN CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

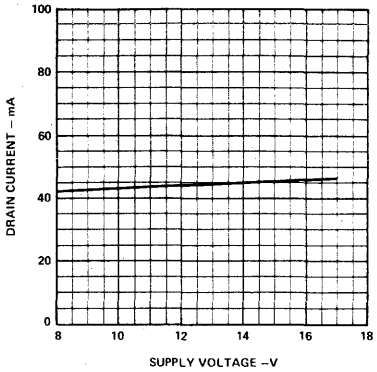


Fig. 2

OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE

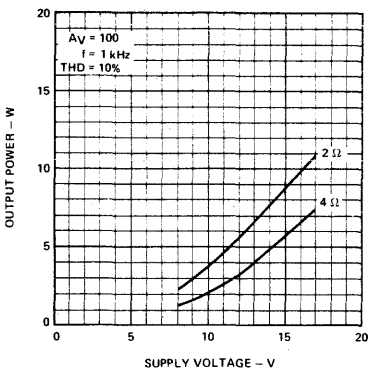


Fig. 3

OUTPUT POWER AS A FUNCTION OF LOAD RESISTANCE (RL)

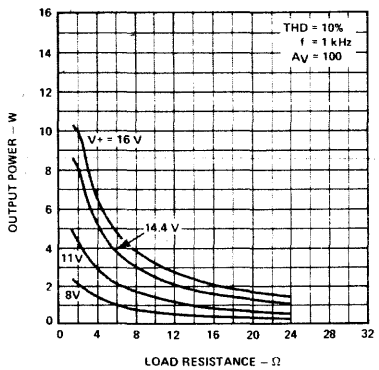


Fig. 4

INPUT VOLTAGE AS A FUNCTION OF VOLTAGE GAIN (R_L = 4 Ω)

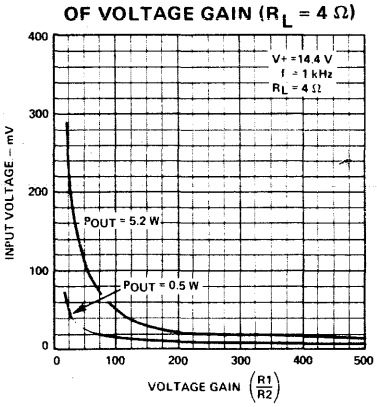


Fig. 5

INPUT VOLTAGE AS A FUNCTION OF VOLTAGE GAIN (R_L = 2 Ω)

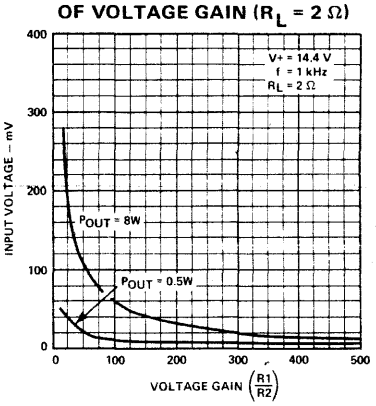


Fig. 6

TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT POWER

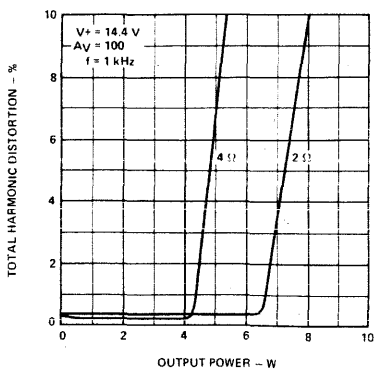


Fig. 7

TOTAL HARMONIC DISTORTION AS A FUNCTION OF FREQUENCY (R_L = 2 Ω; R_L = 4 Ω)

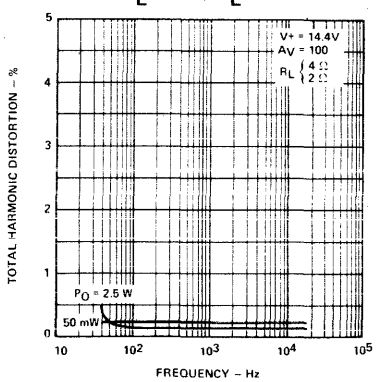


Fig. 8

SUPPLY VOLTAGE REJECTION AS A FUNCTION OF VOLTAGE GAIN

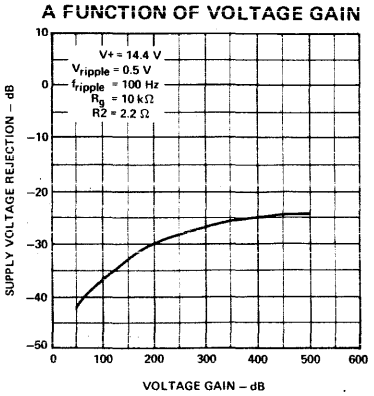


Fig. 9

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TYPICAL PERFORMANCE CURVES (Cont'd)

SUPPLY VOLTAGE REJECTION AS A FUNCTION OF FREQUENCY

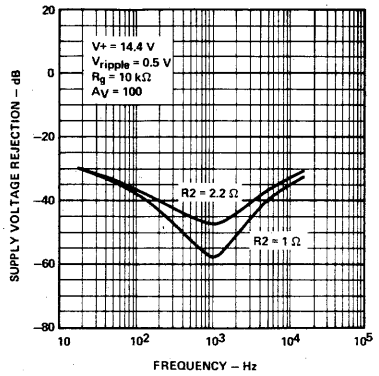


Fig. 10

POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF OUTPUT POWER (R_L = 4 Ω)

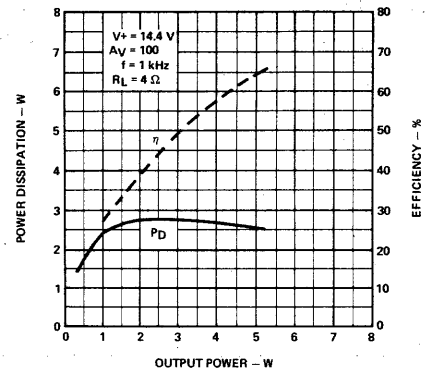


Fig. 11

POWER DISSIPATION AND EFFIECIENCY AS A FUNCTION OF OUTPUT POWER (R_L = 2 Ω)

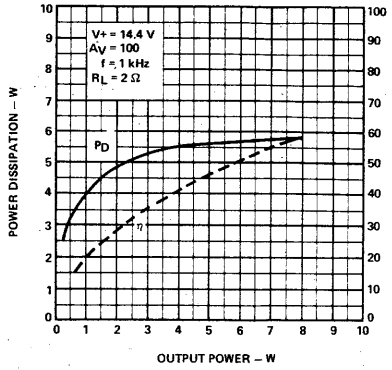


Fig. 12

MAXIMUM POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE (SINE WAVE OPERATION)

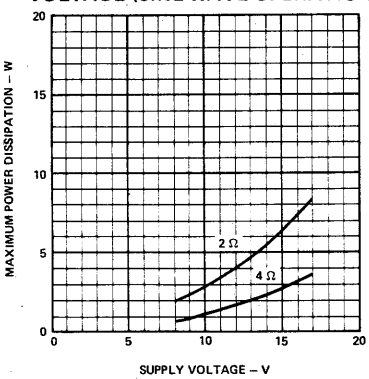


Fig. 13

MAXIMUM ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

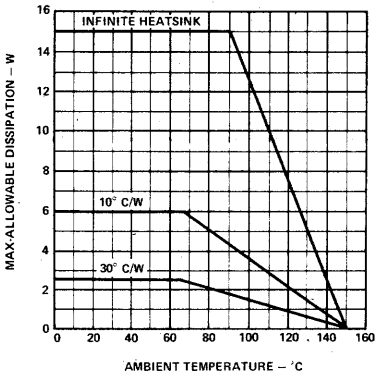


Fig. 14

CAPACITOR (CFB) AS A FUNCTION OF GAIN (VARIOUS BANDWIDTHS)

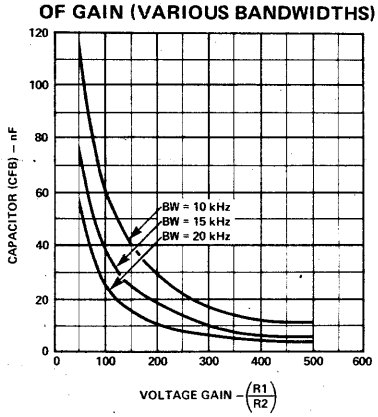


Fig. 15

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

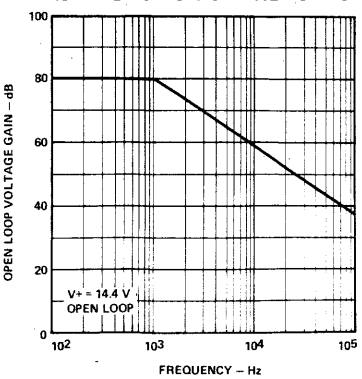


Fig. 16

OUTPUT POWER AND DRAIN CURRENT AS A FUNCTION OF CASE TEMPERATURE (R_L = 4 Ω)

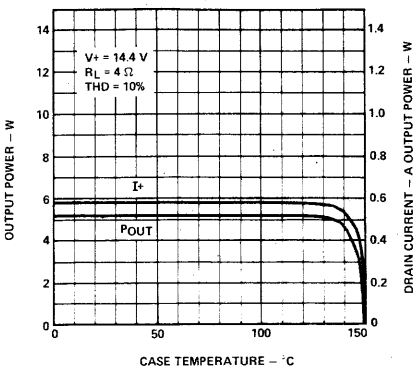


Fig. 17

OUTPUT POWER AND DRAIN CURRENT AS A FUNCTION OF CASE TEMPERATURE (R_L = 2 Ω)

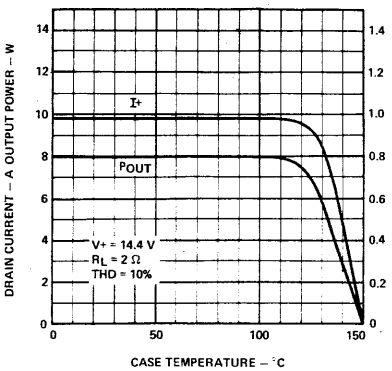


Fig. 18

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DESIGN CONSIDERATIONS

The board layout of the TDA2002 and TDA2002A is critical to assure good stability. The layout shown in Figure 20 is recommended. If a different layout is used, it is important that the ground points of inputs 1 and 2 be well decoupled from the ground of the output. Pin lengths should be as short as possible.

The component values shown on the applications schematics are recommended. However, other values may be used, and Table 1 is intended to serve as a guide for the designer on the effect of changing component values.

No electrical insulation is needed between the package tab and the heat sink, if the heat sink is electrically isolated or is at ground potential.

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
C1	10 μF	Input DC decoupling		Noise at switch-on, switch-off
C2	470 μF	Ripple rejection		Degradation of PSRR
C3	0.1 μF	Supply bypassing		Danger of oscillation
C4	1000 μF	Output coupling to load		Higher low frequency cutoff
C5	0.1 μF	Frequency stability		Danger of oscillation at high frequencies with inductive loads
CF_B	$\simeq \frac{1}{2\pi B R 1}$	Upper frequency cutoff	Lower bandwidth	Larger bandwidth
R1	$(A_V - 1) \cdot R2$	Closed loop gain determination		Increase of drain current
R2	2.2 Ω	Closed loop gain and PSRR determination	Degradation of PSRR	
R3	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R_{FB}	$\cong$ 20 R2	Upper frequency cutoff	Poor high frequency attenuation	Danger of oscillation

TABLE 1

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APPLICATIONS INFORMATION:

Several typical applications of the TDA2002 and TDA2002A are shown in this section, together with printed circuit board layouts.

Figures 19 and 20 show a typical circuit with CFB, RFB shown dashed. CFB and RFB may be used to adjust the bandwidth after the gain has been set by the ratio R1/R2. (See Figure 15).

Figures 23 and 24 show a typical 15 watt bridge circuit utilizing two devices. A potentiometer (P1) is included to balance the offset voltages between the two devices.

TYPICAL APPLICATION CIRCUIT

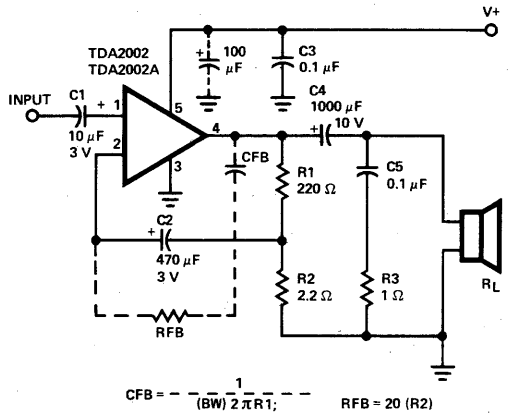


Fig. 19

P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 19 (1:1 SCALE)

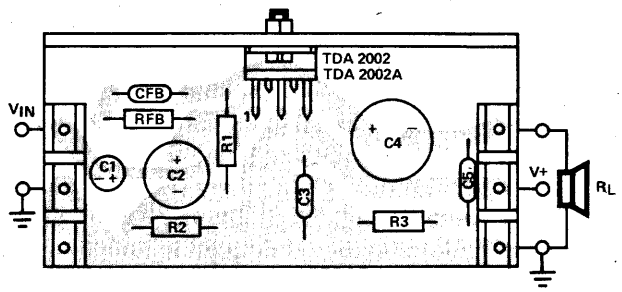


Fig. 20

LOW COST APPLICATION CIRCUIT

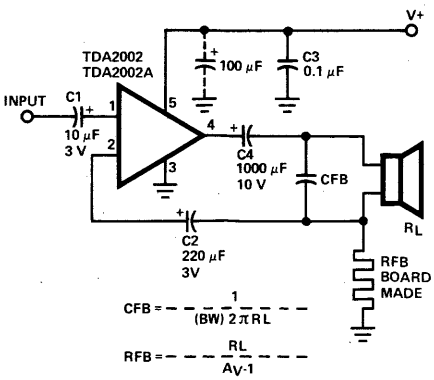


Fig. 21

P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 21 (1:1 SCALE)

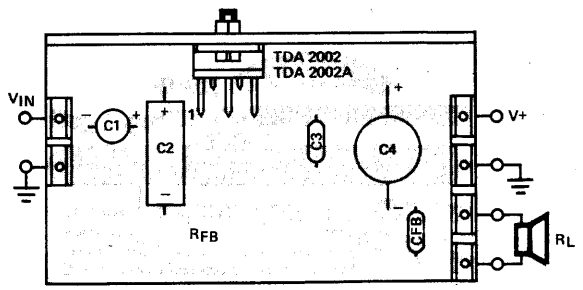


Fig. 22

15 WATT BRIDGE CIRCUIT

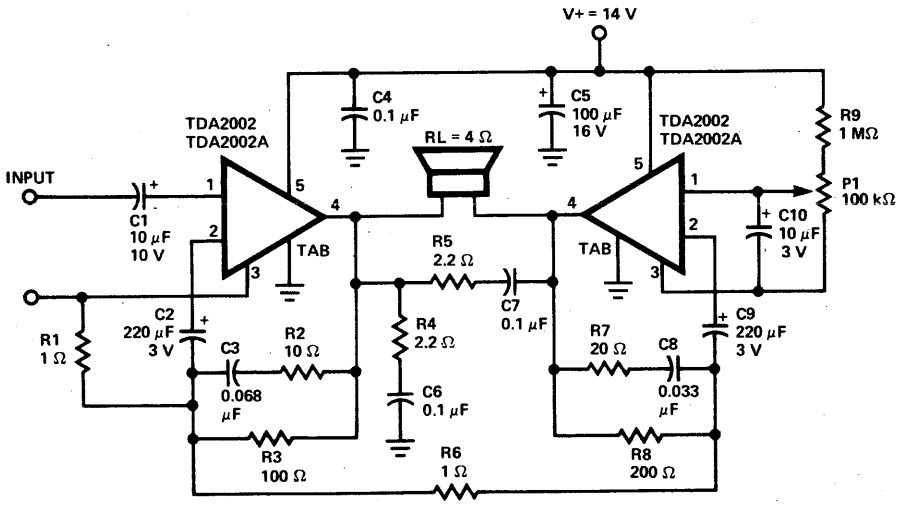


Fig. 23

P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 23 (1:1 SCALE)

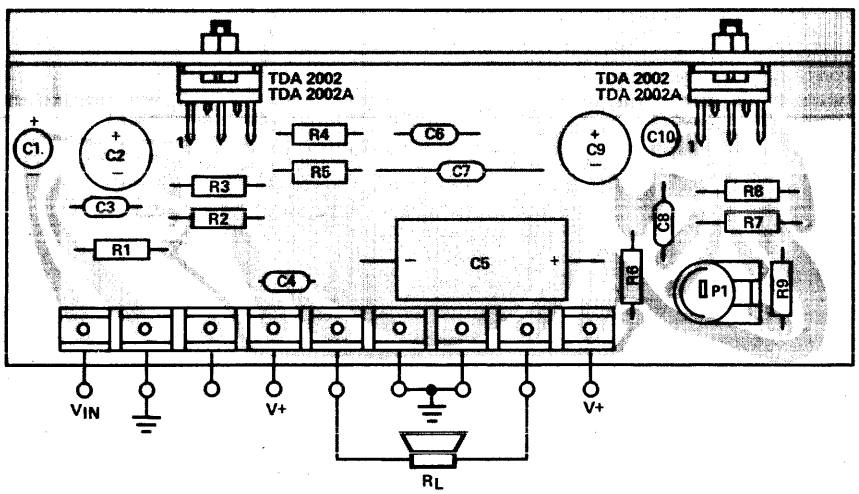


Fig. 24

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THERMAL SHUTDOWN

Both the TDA2002 and TDA2002A have been designed with a thermal shutdown feature. Typical curves of output power and supply current as a function of case temperature are shown in Figures 17 and 18. The thermal overload circuit reduces the drive to the output stage when the junction temperature exceeds the design threshold. The result is a reduced supply current and power output consistent with maintaining the junction temperature at the design limit.

The thermal overload feature offers several important advantages to the circuit designer:

1. The device can withstand excessive ambient temperatures (below 150° C) and temporary or permanent overloads on the output.
2. The safety margin on the heat sink design may be reduced because the device will not be damaged by excessive junction temperature (below 150° C). The only result of this increased junction temperature will be a reduction in output power and supply current.

OVERVOLTAGE (LOAD DUMP) PROTECTION

The TDA2002 has been designed with a built-in circuit which enables this device to withstand a series of voltage spikes (see Figure 25). The load dump feature starts at about 18 V, so the operating voltage must not exceed 18 V.

This feature is particularly important in automobile applications, and the pulse train shown in Figure 25 is intended to simulate the voltage spikes which often occur on the supply line in automotive applications.

If the supply voltage peaks exceed 40 V, then an LC network must be inserted between the supply and Pin 5 to assure that the pulses at Pin 5 will not exceed the limits shown in Figure 25. A typical LC network is shown in Figure 26. With this network a train of pulses up to 120 V and 2 ms wide can be applied from the supply line.

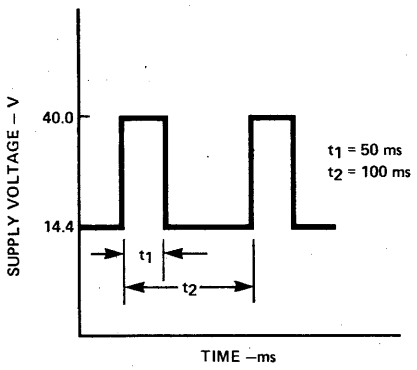


Fig. 25

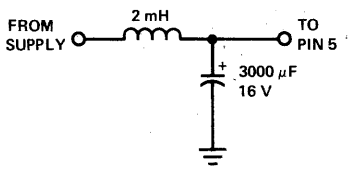
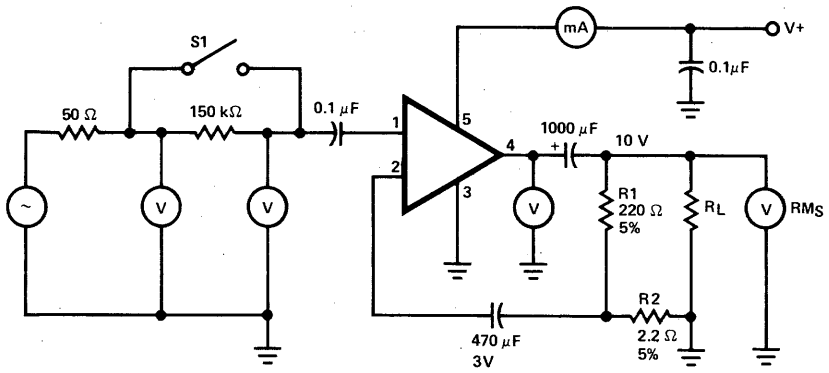


Fig. 26

TEST CIRCUIT



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9643 • 9643A • 9644 • 9644A

DUAL TTL TO MOS DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 9643 and 9644 are dual positive logic "AND" and "NAND" TTL-to-MOS drivers respectively. The 9643 DC/PC is a functional replacement of the SN75322 with one important exception: the two external PNP transistors are no longer needed for operation. The 9643 DC/PC is also a functional replacement for the 75363 with the important exception that the V_{CC3} supply is not needed. The 9644 is a logical inversion of the 9643 and is a functional replacement for the 75361. The pin connections normally used for the external PNP transistors are purposely not internally connected to the 9643 DC/PC.

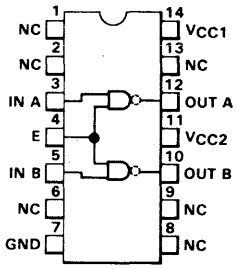
Both devices have separate driver address inputs with common strobe. Both devices accept standard TTL and DTL input signals and provide high-current and high-voltage output levels suitable for driving MOS circuits. The 9643 may be used to drive the chip-enable clock of the TMS4030 MOS RAM. The 9644 is suitable for driving both clock and address inputs for the TMS4062 and 1103 RAM. The 9643 and 9644 operate from the TTL 5 V supply and the MOS supply.

The 9643A and 9644A are high voltage versions of the 9643 and 9644. The "A" version is capable of withstanding V_{CC2} voltages up to 18 V_{DC} max.

The 9643A and 9644A are available in 8-pin DIPs for increased board efficiency.

- **DUAL POSITIVE-LOGIC TTL-TO-MOS DRIVERS**
- **VERSATILE INTERFACE CIRCUIT FOR USE BETWEEN TTL AND HIGH-CURRENT, HIGH-VOLTAGE SYSTEMS**
- **OPERATES FROM STANDARD BIPOLAR AND MOS SUPPLY VOLTAGES**
- **HIGH SPEED SWITCHING**
- **TTL AND DTL COMPATIBLE INPUTS**
- **SEPARATE DRIVER ADDRESS INPUTS WITH COMMON STROBE**
- **V_{OH} AND V_{OL} COMPATIBLE WITH POPULAR MOS RAMs**
- **DOES NOT REQUIRE EXTERNAL PNP TRANSISTORS OR V_{CC3}**
- **V_{OH} MINIMUM IS V_{CC2} – 0.5 V**

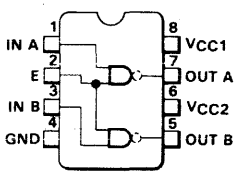
CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
9643	9643DC
9643	9643PC

CONNECTION DIAGRAM
8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



ORDER INFORMATION

TYPE	PART NO.
9643	9643RC
9643	9643TC
9643A	9643ARC
9643A	9643ATC
9644	9644RC
9644	9644TC
9644A	9644ARC
9644A	9644ATC

ABSOLUTE MAXIMUM RATINGS: Over operating ambient temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1)	−0.5 V to 7 V
Supply voltage range of V_{CC2} 9643/9644	−0.5 V to 15 V
9643A/9644A	−0.5 V to 18 V
Input voltage	5.5 V
Inter-input voltage (see Note 2)	5.5 V
Continuous total dissipation at (or below) 25°C ambient temperature	1000 mW
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature	
Molded dip (Soldering, 10 s)	260°C
Hermetic dip (Soldering, 30 s)	300°C

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. This rating applies between any two inputs of any one of the gates.

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464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA, 94042 (415) 962-5011/TWX 910-379-6435

FAIRCHILD

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RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNITS
Supply Voltage, V_{CC1}		4.75	5.0	5.25	V
Supply Voltage, V_{CC2}	9643, 9644	4.75	12	15	V
	9643A, 9644A		15	18	
Operating Temperature, T_A				70	°C

ELECTRICAL CHARACTERISTICS: Over recommended ranges of V_{CC1}, V_{CC2} and operating ambient temperature unless otherwise noted.

SYMBOL	CHARACTERISTIC	CONDITIONS			MIN	TYP (Note 1)	MAX	UNITS
V_{IH}	Input HIGH Voltage				2.0			V
V_{IL}	Input LOW Voltage						0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = -400 μA			V_{CC2} -0.5	V_{CC2} -0.2		V
V_{OL}	Output LOW Voltage	I_{OL} = 10 mA				0.4	0.5	V
		I_{OL} = 1.0 mA				0.2	0.3	V
I_{IN}	Input Current at Maximum Input Voltage	V_{CC1} = 5.25 V, V_{CC2} = 11.4 V V_{IN} = 5.25 V					0.1	mA
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V	A Inputs				40	μA
			E Inputs				80	
I_{IL}	Input LOW Current	V_{IN} = 0.4 V	A Inputs	9643 9643A			0.5	mA
				9644 9644A			0.8	
			E Inputs	9643 9643A			-1.0	
				9644 9644A			-1.6	
$I_{CC1(L)}$	Supply Current from V_{CC1} All Outputs LOW	V_{CC1} = 5.25 V V_{CC2} = 12.6 V	No Load	9643 9643A		15	19	mA
				9644 9644A		14	17	
$I_{CC2(L)}$	Supply Current from V_{CC2} All Outputs LOW	V_{CC2} = 12.6 V	V_{CC1} = 5.25 V	9643 9644		5.5	9.5	mA
		V_{CC2} = 15.75 V	No Load	9643A 9644A		7.0	11.5	
$I_{CC1(H)}$	Supply Current from V_{CC1} All Outputs HIGH	V_{CC1} = 5.5 V V_{CC2} = 13.2 V	No Load	9643 9643A		9.0	13	mA
				9644 9644A		4.0	6.0	
$I_{CC2(H)}$	Supply Current from V_{CC2} All Outputs HIGH	V_{CC2} = 12.6 V	V_{CC1} = 5.25 V	9643 9644		5.5	9.5	mA
		V_{CC2} = 15.75 V	No Load	9643A 9644A				

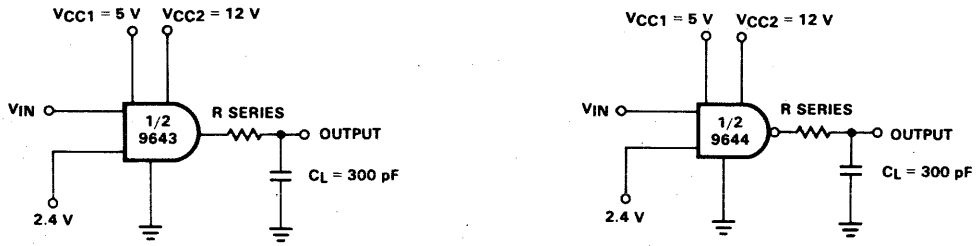
NOTE 1: All typical values are at V_{CC1} = 5.0 V, V_{CC2} = 12 V, and T_A = 25°C unless otherwise noted.

AC CHARACTERISTICS: V_{CC1} = 5.0 V, V_{CC2} = 12 V, T_A = 25°C

SYMBOL	CHARACTERISTIC		CONDITIONS (See Figure 1)		MIN	TYP	MAX	UNITS
t_{DLH}	Delay Time	9643 9644	C_L = 300 pF		5.0 3.0	9.0 6.0	17 15	ns ns
t_{DHL}	Delay Time	9643 9644			5.0 3.0	9.0 6.0	17 15	ns ns
t_{TLH}	Rise Time		R_{SERIES} = 0	C_L = 300 pF	6.0	11	17	ns
t_{THL}	Fall Time				6.0	11	17	ns
t_{TLH}	Rise Time		R_{SERIES} = 10Ω		9.0	14	20	ns
t_{THL}	Fall Time				9.0	14	20	ns
$t_{PLH_A} - t_{PLH_B}$ $t_{PHL_A} - t_{PHL_B}$	Skew between outputs A and B					0.5		ns

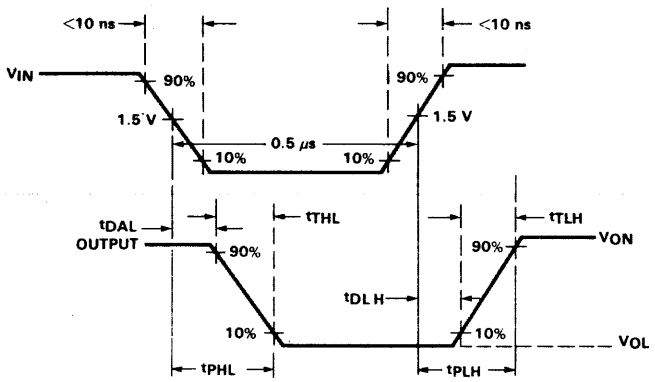
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AC TEST CIRCUIT AND VOLTAGE WAVEFORMS



AC TEST NOTES:

1. The pulse generator has the following characteristics:
   PRR = 1 MHz, Z_{OUT} = 50 Ω
2. C_L includes probe and jig capacitance.



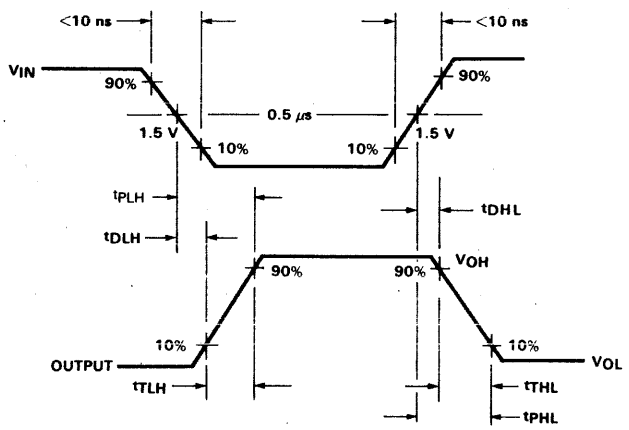


Fig. 1

Fairchild cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in a Fairchild product. No other circuit patent licenses are implied.

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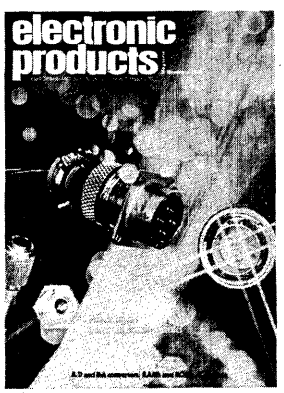
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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-909/911

Wideband, Low Noise, Operational Amplifiers

FEATURES

- LOW BROADBAND NOISE — 1μV R.M.S.
- LOW NOISE VOLTAGE — $7nV/\sqrt{Hz}$
- LOW OFFSET VOLTAGE — 2mV
- WIDE BANDWIDTH — 7MHz
- POWER BANDWIDTH — 20kHz
- SUPPLY RANGE — ±5V TO ±20V
- INTERNALLY COMPENSATED

APPLICATIONS

- HIGH Q, WIDEBAND FILTERS
- AUDIO AMPLIFIERS
- SIGNAL GENERATORS

DESCRIPTION

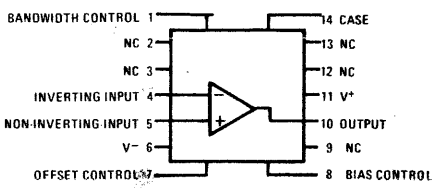
HA-909 and HA-911 are monolithic ampliifers delivering very low noise and excellent bandwidth specifications without the need for external compensation. Additional features of these dielectrically isolated devices include low offset voltage, offset trim capabitlity (14-pin flat package only), and high output current drive capabitlity.

With 7MHz bandwidth and internal compensation these amplifiers are extremely useful in many active filter designs. In audio circuitry requiring quiet operation these devices offer 1 μ V typical broadband noise (10Hz to 1kHz) and 20kHz power bandwidth. 2mV typical offset voltage, offset trim capability, and 20mA output current drive capability (±10.0V swing) make these amplifiers useful in signal conditioning circuits.

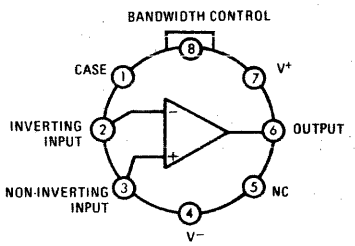
HA-909 and HA-911 are available in metal can (TO-99) and 14-pin flat packages. HA-909 is specified over the -55°C to +125°C range. HA-911 is specified from 0°C to +75°C.

PINOUT

TO-86 — TOP VIEW — **Package Code 9V**

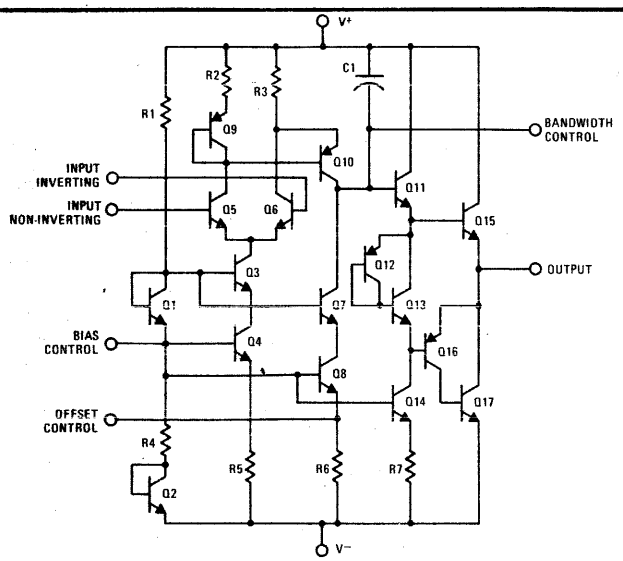


TO-99 — TOP VIEW — **Package Code 2A**



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SCHEMATIC



SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals		50.0V
Differential Input Voltage		±7.0V
Peak Output Current		±50mA
Internal Power Dissipation (Note 10)		300mW
Operating Temperature Range –	HA-909	$-55^oC \leq T_A \leq +125^oC$
	HA-911	$0^oC \leq T_A \leq +75^oC$
Storage Temperature Range		$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: V_{Supply} = ±15.0V unless otherwise specified.

PARAMETER	TEMP.	HA-909 -55°C to +125°C MIN.	HA-909 TYP.	HA-909 MAX.	HA-911 0°C to +75°C MIN.	HA-911 TYP.	HA-911 MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		2.0	5.0		2.0	6.0	mV
	Full			6.0			7.5	mV
Equivalent Input Noise (Note 9)	+25°C		1.0	5.0		1.0		μV
Input Noise Voltage	+25°C		7			7		$nV/\sqrt{Hz}$
* Bias Current	+25°C		87	300		200	500	nA
	Full			750		300	750	nA
* Offset Current	+25°C		25	150		100	300	nA
	Full		50	300		150	450	nA
Offset Current Average Drift	Full		1.0			1.0		nA/°C
Input Resistance	+25°C	200	600		100	250		KΩ
	Full	100	300					KΩ
Common Mode Range	Full	+12.0			+12.0			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Notes 1, 4)	+25°C	25K	45K		20K	45K		V/V
	Full	25K	45K		15K	45K		V/V
Full Power BW	+25°C		20			20		KHz
* Common Mode Rejection Ratio (Note 2)	Full	80	96		74	90		dB
Unity Gain Bandwidth (Note 3)	+25°C		7			7		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	+12.0			+11.0			V
* Output Current (Note 4)	+25°C	+20			+15			mA
Output Resistance	+25°C		150			500		Ohms
TRANSIENT RESPONSE								
Rise Time (Notes 1, 5, 6 & 8)	+25°C		40	75		40	75	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		15	40		15	40	%
* Slew Rate (Notes 1, 5 & 8)	+25°C	+3.5	+5.0			+5.0		V/μs
		-1.2	-2.0			-2.0		
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		1.8	2.5		1.8	2.5	mA
* Power Supply Rejection Ratio (Note 7)	Full	80	92		74	90		dB

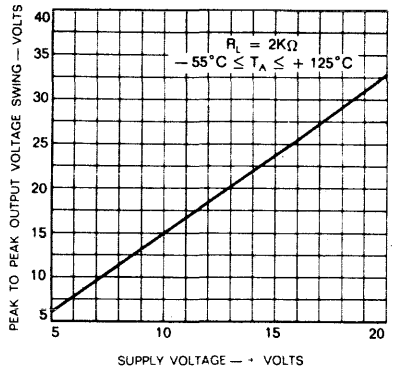
NOTES:
1. R_L = 2KΩ
2. V_{CM} = ±5.0V
3. V_O < 90mV
4. V_O = ±10.0V
5. C_L = 100pF
6. V_O = ±200mV
7. V_{Sup} = ±9.0V to ±15.0V
8. See Transient Response test circuits and waveforms – page 3.
9. 10 – 1000Hz, R_S = 10K
10. Derate by 6.6mW/°C above 105°C

*100% Tested For DASH 8

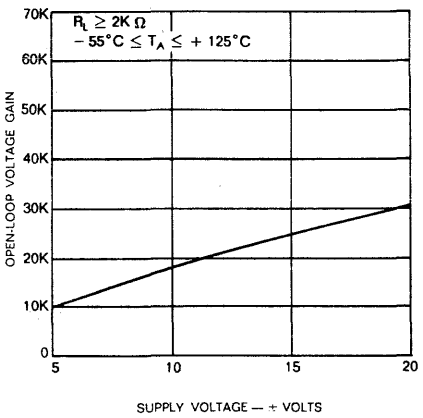
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GUARANTEED ELECTRICAL CHARACTERISTICS

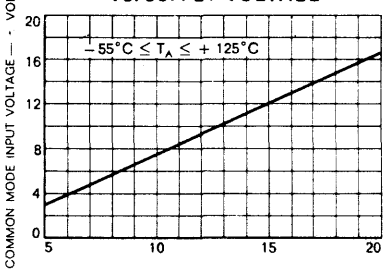
OUTPUT VOLTAGE SWING VS. SUPPLY VOLTAGE



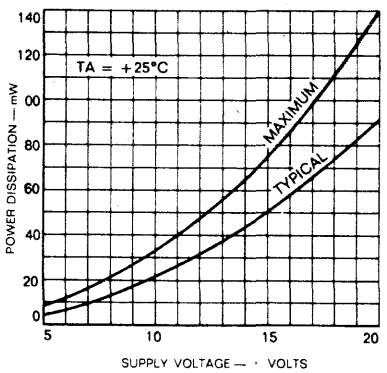
OPEN LOOP VOLTAGE GAIN VS. SUPPLY VOLTAGE



COMMON MODE INPUT VOLTAGE VS. SUPPLY VOLTAGE

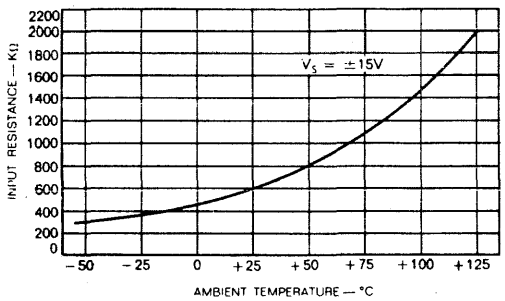


POWER DISSIPATION VS. SUPPLY VOLTAGE

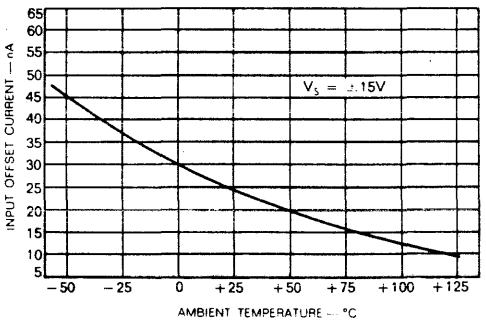


TYPICAL PERFORMANCE CURVES

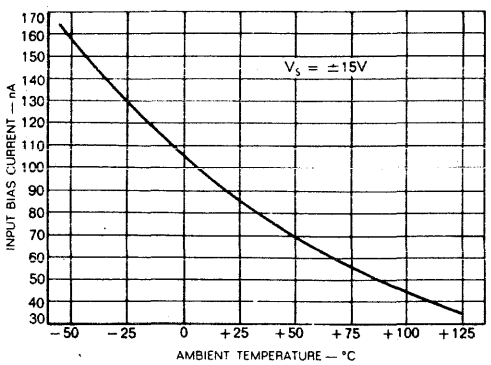
INPUT RESISTANCE VS. AMBIENT TEMPERATURE



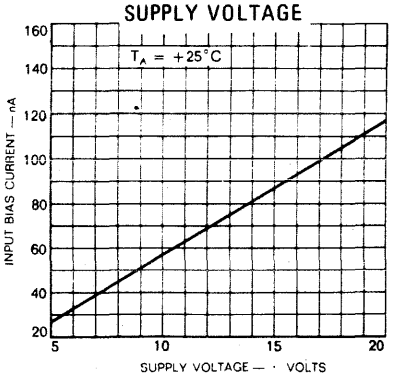
INPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE

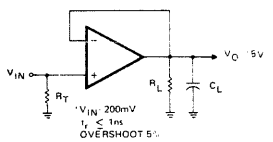


INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE

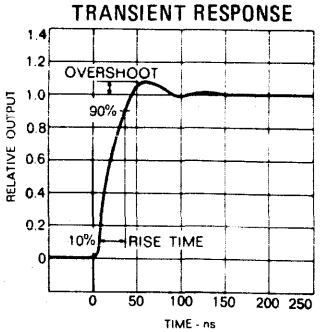


INPUT BIAS CURRENT VS. SUPPLY VOLTAGE





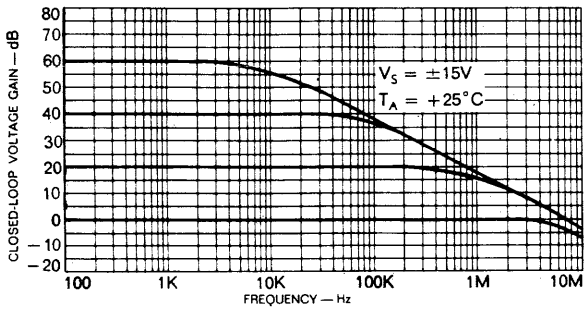
TRANSIENT RESPONSE



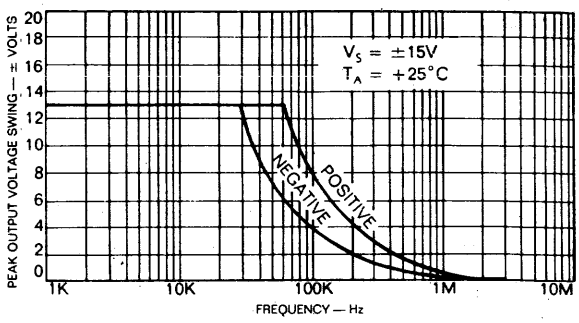
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TYPICAL PERFORMANCE CURVES(continued)

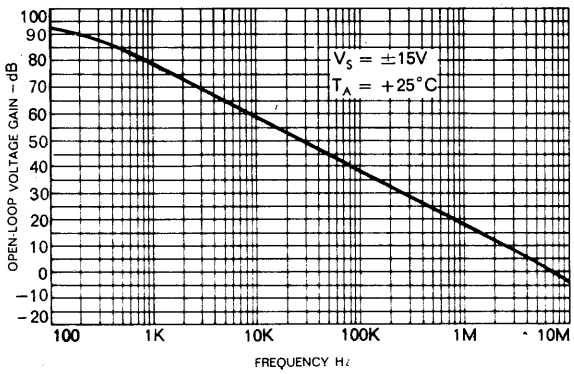
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



OUTPUT VOLTAGE SWING VS. FREQUENCY



OPEN LOOP FREQUENCY RESPONSE



DEFINITIONS

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT – The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE – The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE – The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO – The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING – The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE – The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE – The ratio of the change in output voltage to the change in output current.

POSITIVE OUTPUT VOLTAGE SWING – The peak positive output voltage swing, referred to ground, that can be obtained without clipping.

NEGATIVE OUTPUT VOLTAGE SWING – The peak negative output voltage swing, referred to ground, that can be obtained without clipping.

VOLTAGE GAIN – The ratio of the change in output voltage to the change in input voltage producing it.

BANDWIDTH – The frequency at which the voltage gain is 3dB below its low frequency value.

UNITY GAIN BANDWIDTH – The frequency at which the voltage gain of the amplifier is unity.

POWER SUPPLY REJECTION RATIO – The ratio of the change in input offset voltage to the change in power supply voltage producing it.

TRANSIENT RESPONSE – The closed loop step function response of the amplifier under small signal conditions.

PHASE MARGIN – $(180^o - (\phi_1 - \phi_2))$ where ϕ_1 is the phase shift at the frequency where the absolute magnitude of gain is unity ϕ_2 is the phase shift at a frequency much lower than the open loop bandwidth.

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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2050/2055/2050A/2055A

High Slew Rate F.E.T. Input Operational Amplifiers

FEATURES

- HIGH SLEW RATE — 120V/μs
- FAST SETTLING — 400ns
- WIDE POWER BANDWIDTH — 2MHz
- HIGH GAIN BANDWIDTH — 20MHz
- HIGH INPUT IMPEDANCE — 10^{12} OHMS
- LOW BIAS CURRENT — 1pA
- TRUE OP AMP – CAN BE OPERATED INVERTING OR NON-INVERTING

APPLICATIONS

- DATA ACQUISITION
- SIGNAL CONDITIONING
- R.F. AND VIDEO AMPLIFICATION

DESCRIPTION

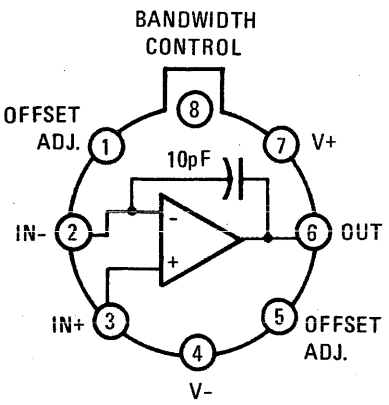
The HA-2050/2055 is an operational amplifier combining the advantages of very high slew rate and wide bandwidth with ultra-low input current and high input resistance. These devices are ideal for use in sample-and-hold circuits, A/D, D/A and sampled data systems; and for use in wide band R.F. or video systems where wide bandwidth at high output levels is required. The device may be operated inverting or noninverting; and external compensation is required only when operated at closed loop gains less than three. An internal feedback capacitor is provided to cancel phase shift in the feedback loop due to input capacitance.

The HA-2050 is guaranteed for operation from -55°C to +125°C and the HA-2055 is guaranteed from 0°C to +75°C.

PINOUT

TO-99 **Package Code 2A**

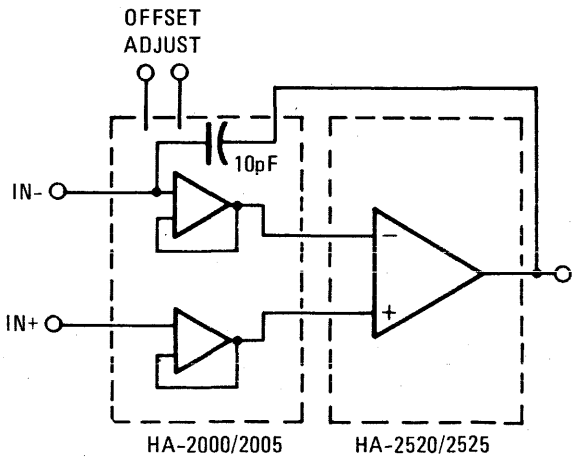
Top View



Case Connected to V+

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

FUNCTIONAL DIAGRAM



SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V– Terminals	35.0V	Internal Power Dissipation (Note 10)	300mW	
Differential Input Voltage	±15.0V	Operating Temp. Range	$-55^{o}C \leq T_A \leq +125^{o}C$	(HA-2050)
Output Current	50mA		$0^{o}C \leq T_A \leq +75^{o}C$	(HA-2055)
		Storage Temp. Range	$-65^{o}C \leq T_A \leq +150^{o}C$	

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ unless otherwise specified.

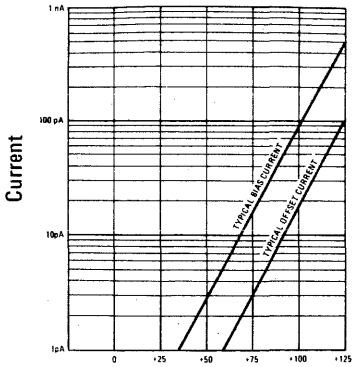
PARAMETER	TEMP.	HA-2050/HA-2050A -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2055/HA-2055A 0°C to +75°C LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage (Note 1)								
HA-2050 / HA-2055	+25°C		15	25		30	60	mV
	Full			30			65	mV
HA-2050A / HA-2055A	+25°C		7	14		7	14	mV
	Full			17			17	mV
Bias Current	+25°C		1	20		1	20	ρA
* (125°C)	Full		0.5	10		0.02	1	nA
Offset Current	+25°C		0.5	20		0.5	20	ρA
* (125°C)	Full		0.1	5		.005	0.5	nA
Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Capacitance	+25°C		5			5		ρF
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 2,5)	+25°C	7.5K	15K		7.5K	15K		V/V
	Full	5K			5K			V/V
* Common Mode Rejection Ratio (Note 3)	Full	74	90		70	90		dB
Gain Bandwidth Product (Note 4)	+25°C		20			20		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		V
* Output Current	+25°C	±10	±20		±10	±20		mA
Full Power Bandwidth (Note 5)	+25°C		2,000			2,000		kHz
TRANSIENT RESPONSE (NOTES 2, 8, 9)								
Rise Time (Note 6)	+25°C		50			50		ns
Overshoot (Note 6)	+25°C		25			25		%
Slew Rate (Note 5)	+25°C		120			120		V/μs
Settling Time	+25°C		0.4			0.4		μs
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		6.0	8.0		6.0	8.0	mA
* Power Supply Rejection Ratio (Note 7)	Full	74	90		70	90		dB

NOTES:
1. Adjustable to zero with 100KΩ pot between pins 1 and 5; wiper to V+.
2. $R_L = 2K$
3. $V_{CM} = \pm 5.0V$
4. $A_V > 10$
5. $V_O = \pm 10V$
6. $V_O = \pm 200mV$
7. $\Delta V = \pm 5.0V$
8. $C_L = 50pF$
9. $A_V = +3$, See transient response test circuit and wave forms, page 4.
10. Derate by 6.6mW/°C above 105°C

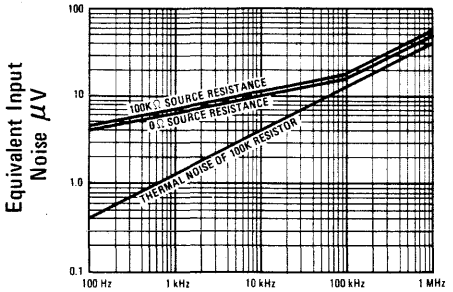
*100% Tested for DASH 8

V+ = 15 VDC, V- = 15 VDC, T_A = 25°C UNLESS OTHERWISE STATED.

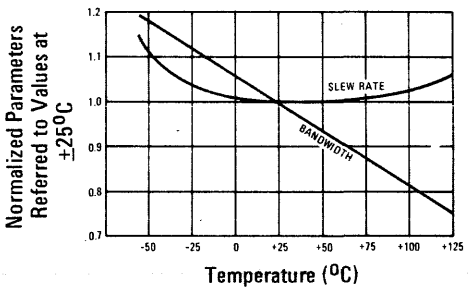
INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



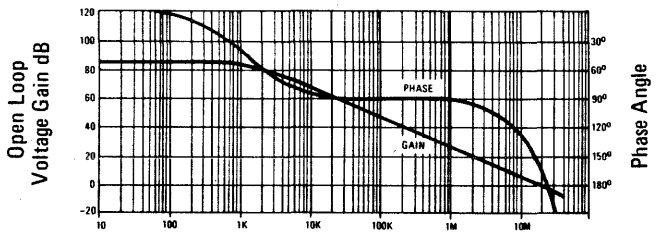
EQUIVALENT INPUT NOISE VS. BANDWIDTH



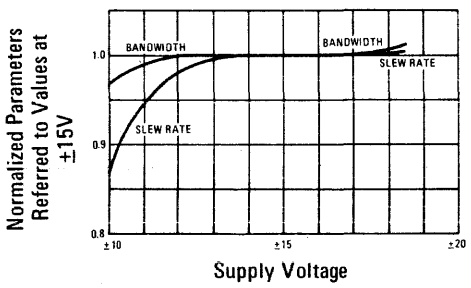
NORMALIZED AC PARAMETERS VS. TEMPERATURE



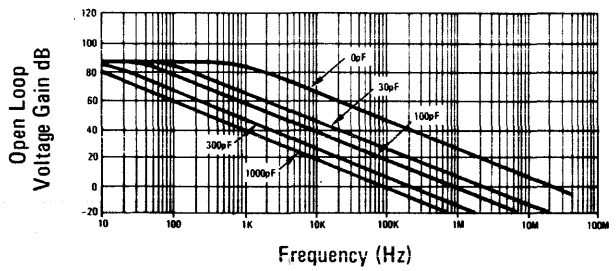
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



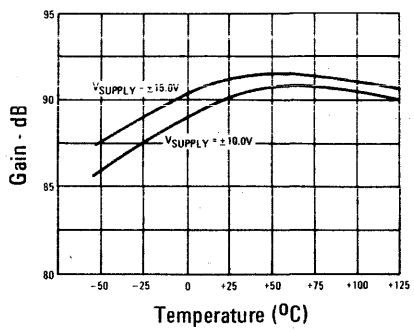
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE AT +25°C



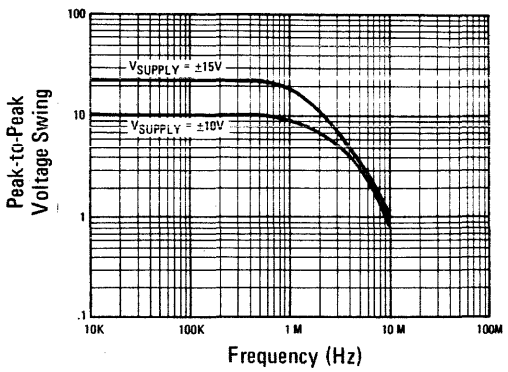
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE

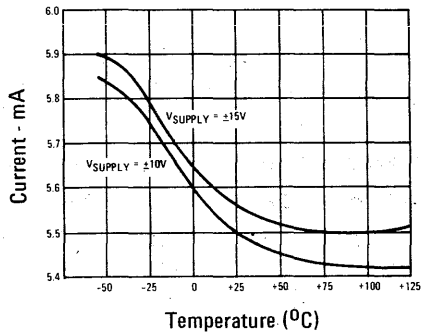


OUTPUT VOLTAGE SWING VS. FREQUENCY AT +25°C

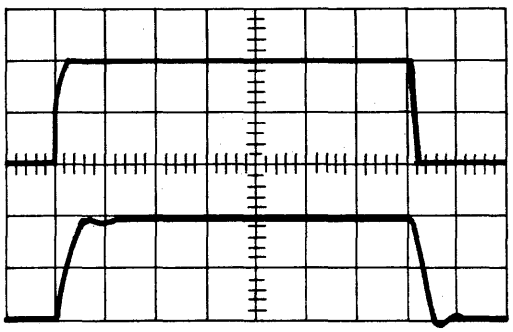


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POWER SUPPLY CURRENT
VS. TEMPERATURE

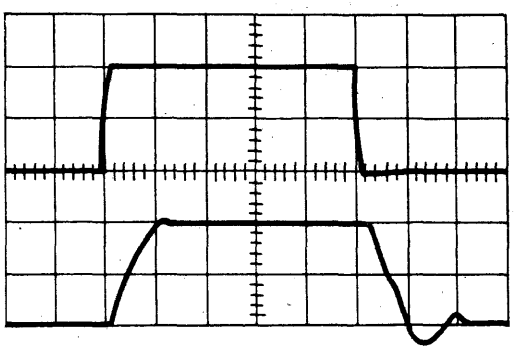


TRANSIENT RESPONSE; $A_V = +3$



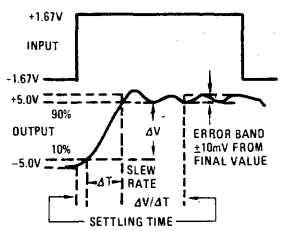
R_L = 2K Ohms, C_L = 50pF
Upper Trace: Input; 33mV/Div.
Lower Trace: Output; 100mV/Div.
Horizontal = 100ns/Div.
$T_A = +25^oC$, $V_S = \pm 15V$

SLEWING WAVEFORM

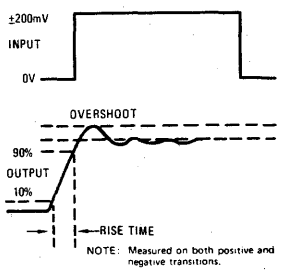


Horizontal Scale: 100ns/Div.
Upper Trace: Input; 1.67V/Div.
Lower Trace: Output; 5.0V/Div.
Gain = +3, R_L = 2K Ohms, C_L = 50pF

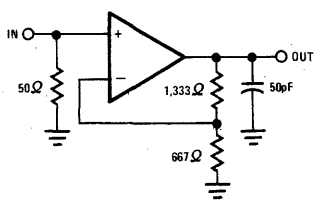
SLEWING RATE AND
SETTLING TIME



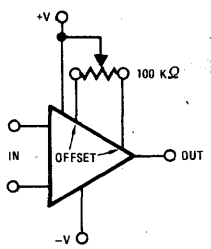
TRANSIENT
RESPONSE



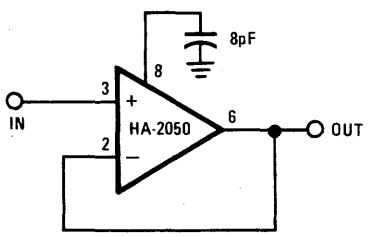
SLEW RATE AND
TRANSIENT RESPONSE



SUGGESTED
OFFSET ZERO
ADJUST HOOK-UP



TYPICAL APPLICATIONS



COMPENSATION CIRCUIT FOR UNITY GAIN

Slew Rate ≈ 40V/μs

Bandwidth ≈ 8 MHz

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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2060/2065/ 2060A/2065A

Wide Band F.E.T. Input Operational Amplifier

FEATURES

- GAIN BANDWIDTH PRODUCT — 100MHz
- HIGH INPUT IMPEDANCE — 10^{12} OHMS
- LOW BIAS CURRENT — 1pA
- HIGH SLEW RATE — 35V/μs
- WIDE POWER BANDWIDTH — 600kHz
- TRUE OP AMP – CAN BE OPERATED INVERTING OR NON-INVERTING

APPLICATIONS

- SIGNAL CONDITIONING
- ACTIVE FILTERS
- SIGNAL GENERATORS

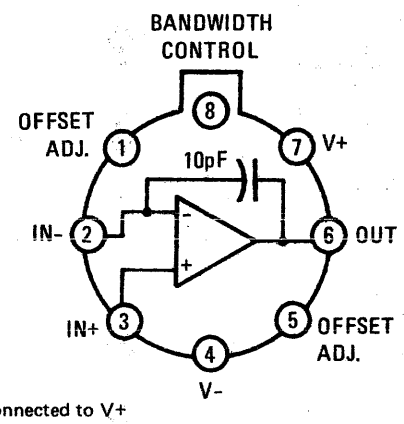
DESCRIPTION

The HA-2060/2065 is an operational amplifier combining the advantages of very wide bandwidth and high slew rate with ultra-low input current and high input resistance. These devices are ideal for use in sample-and-hold circuits, active filters, wide band amplifiers, high gain amplifiers with superior bandwidth, and wherever very low closed loop gain and phase shift errors are required. The device may be operated inverting or noninverting; and external compensation is required only when operating at closed loop gains less than five. An internal feedback capacitor is provided to cancel phase shift in the feedback loop due to input capacitance.

The HA-2060 is guaranteed for operation from -55°C to +125°C and the HA-2065 is guaranteed from 0°C to +75°C.

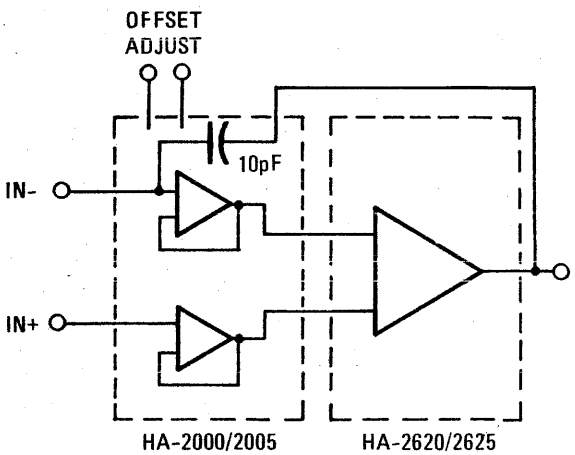
PINOUT

TO-99 Top View **Package Code 2A**



Case Connected to V+

FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	35.0V	Internal Power Dissipation (Note 10)	300mW
Differential Input Voltage	±12V	Operating Temp. Range	$-55^{o}C \leq T_A \leq +125^{o}C$ (HA-2060)
Output Current / Full Short Circuit Protection			$0^{o}C \leq T_A \leq +75^{o}C$ (HA-2065)
		Storage Temp. Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ unless otherwise specified.

PARAMETER	TEMP.	HA-2060/HA-2060A -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2065/HA-2065A 0°C to +75°C LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage (Note 1)								
HA-2060 / HA-2065	+25°C		15	25		15	60	mV
	Full			30			65	mV
HA-2060A / HA-2065A	+25°C		7	12		7	12	mV
	Full			15			15	mV
Bias Current	+25°C		1	20		1	20	pA
* (125°C)	Full		0.5	10		0.02	1	nA
Offset Current	+25°C		0.5	20		0.5	20	pA
* (125°C)	Full		0.1	5		.005	.5	nA
Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Capacitance	+25°C		5			5		pF
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 2 5)	+25°C	80K	150K		80K	150K		V/V
	Full	60K			70K			V/V
* Common Mode Rejection Ratio (Note 3)	Full	74	90		70	90		dB
Gain Bandwidth Product (Note 4)	+25°C		100			100		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		V
* Output Current	+25°C	±10	±18		±10	±18		mA
Full Power Bandwidth (Note 5)	+25°C		600			600		kHz
TRANSIENT RESPONSE (NOTES 2, 8, 9)								
Rise Time (Note 6)	+25°C		50			50		ns
Overshoot (Note 6)	+25°C		25			25		%
Slew Rate (Note 5)	+25°C		35			35		V/μs
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		4.0	6.0		4.0	6.0	mA
* Power Supply Rejection Ratio (Note 7)	Full	74	90		70	90		dB

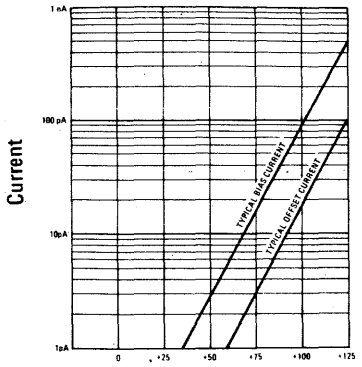
NOTES:
1. Adjustable to zero with 100KΩ pot between pins 1 and 5; wiper to V+.
2. $R_L = 2K$
3. $V_{CM} = \pm 5.0V$
4. $A_V > 10$
5. $V_O = \pm 10V$
6. $V_O = \pm 200mV$
7. $\Delta V = \pm 5.0V$
8. $C_L = 50pF$
9. $A_V = +5$, See transient response test circuits and waveforms, page 4.
10. Derate by 6.6mW/°C above 105°C

*100% Tested for DASH 8

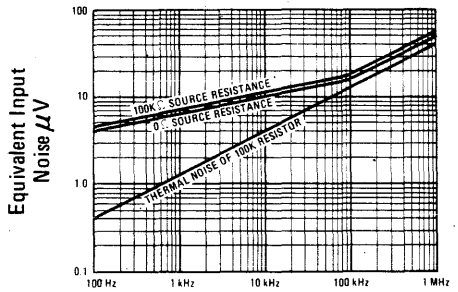
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V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE

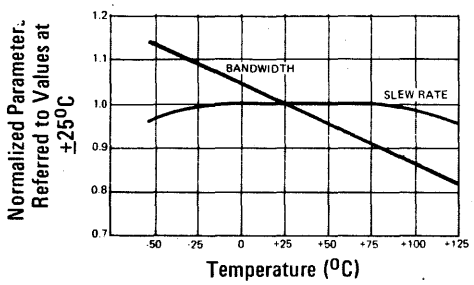


EQUIVALENT INPUT NOISE VS. BANDWIDTH

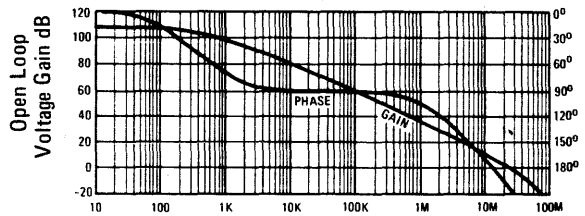


Upper 3dB Frequency
Lower 3dB Frequency - 10 Hz

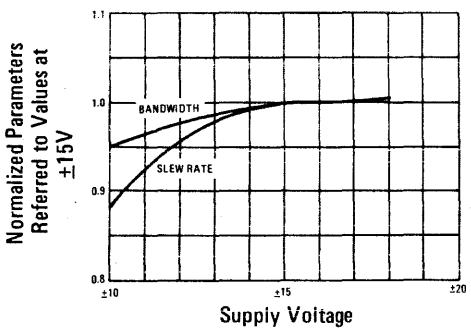
NORMALIZED AC PARAMETERS VS. TEMPERATURE



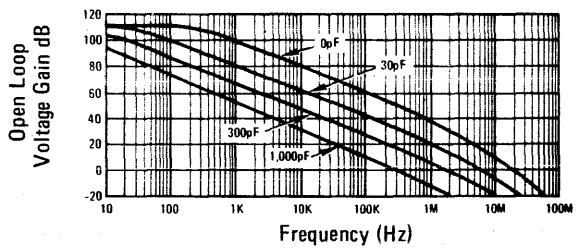
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



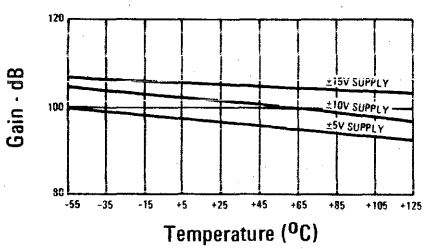
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE AT +25°C



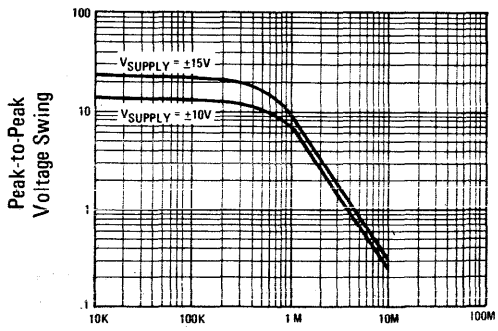
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE



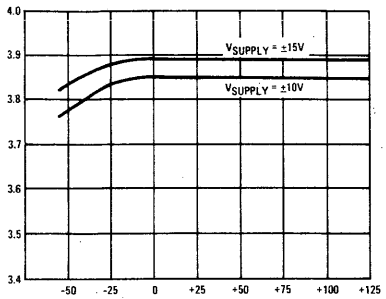
OUTPUT VOLTAGE SWING VS. FREQUENCY AT +25°C



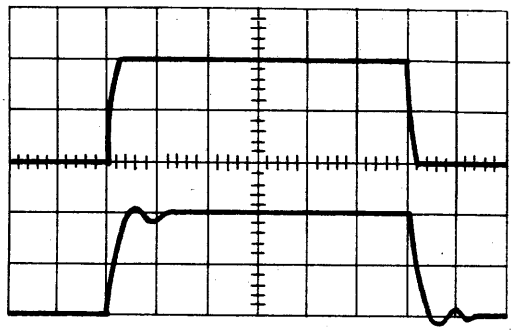
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PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT VS. TEMPERATURE

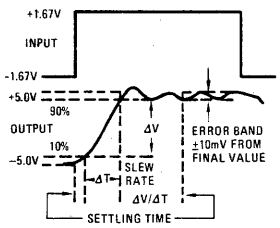


TRANSIENT RESPONSE; A_V = +5

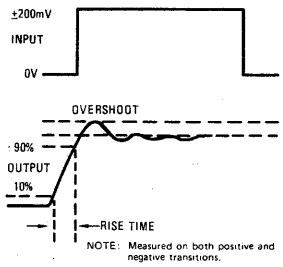


R_L = 2K Ohms, C_L = 50pF
Upper Trace: Input; 20mV/Div.
Lower Trace: Output; 100mV/Div.
Horizontal = 100ns/Div.
T_A = +25°C, V_S = ±15V

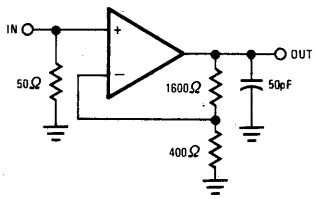
SLEW RATE AND SETTLING TIME



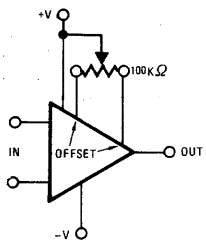
TRANSIENT RESPONSE



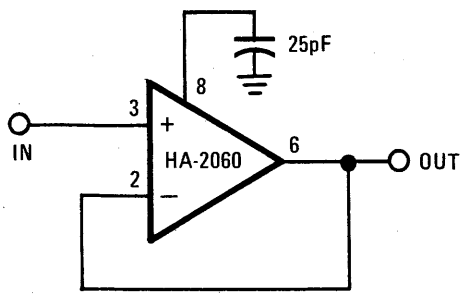
SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST HOOK-UP



TYPICAL APPLICATIONS



COMPENSATION CIRCUIT FOR UNITY GAIN

SLEW RATE ≈ 5 V/μs

BANDWIDTH ≈ 10 MHz

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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2400/2404/2405

PRAM™ Four Channel Programmable Amplifier

FEATURES

- PROGRAMMABILITY
- HIGH SLEW RATE 30V/μs
- WIDE GAIN BANDWIDTH 40MHz
- HIGH GAIN 150,000
- LOW OFFSET CURRENT 5nA
- HIGH INPUT IMPEDANCE 30MΩ
- SINGLE CAPACITOR COMPENSATION
- DTL/TTL COMPATIBLE INPUTS

APPLICATIONS

- THOUSANDS OF NEW APPLICATIONS; PROGRAM
  - SIGNAL SELECTION/MULTIPLEXING
  - OP AMP GAIN
  - OSCILLATOR FREQUENCY
  - FILTER CHARACTERISTICS
  - ADD-SUBTRACT FUNCTIONS
  - INTEGRATOR CHARACTERISTICS
  - COMPARATOR LEVELS

DESCRIPTION

HA-2400/2404/2405 comprise a series of four-channel programmable amplifiers providing a level of versatility unsurpassed by any other monolithic operational amplifier. Versatility is achieved by employing four input amplifier channels, any one (or none) of which may be electronically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected pair of inputs is an op amp which delivers excellent slew rate, gain bandwidth and power bandwidth performance. Other advantageous features for these dielectrically isolated amplifiers include high voltage gain and input impedance coupled with low input offset voltage and offset current. External compensation is not required on this device at closed loop gains greater than 10.

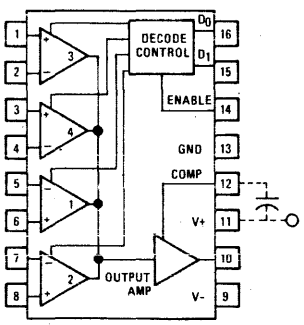
Each channel of the HA-2400/2404/2405 can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This specialization makes these amplifiers excellent components for multiplexing, signal selection, and mathematical function designs. With 30V/μs slew rate, 40MHz gain bandwidth, and 30M ohms input impedance these devices are ideal building blocks for signal generators, active filters, and data acquisition designs. Programmability coupled with 2mV typical offset voltage and 5nA offset current makes these amplifiers outstanding components for signal conditioning circuits.

HA-2400/2404/2405 are available in a 16 pin dual-in-line package. HA-2400 is specified from -55°C to +125°C. HA-2404 is specified over the -25°C to +85°C range, while HA-2405 operates from 0°C to +75°C.

PINOUT

(TOP VIEW)

Package Code 4B



TRUTH TABLE

D_1	D_0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	NONE

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SCHEMATIC

Condensed circuit diagram for a programmable amplifier (PRAM HA-2400)

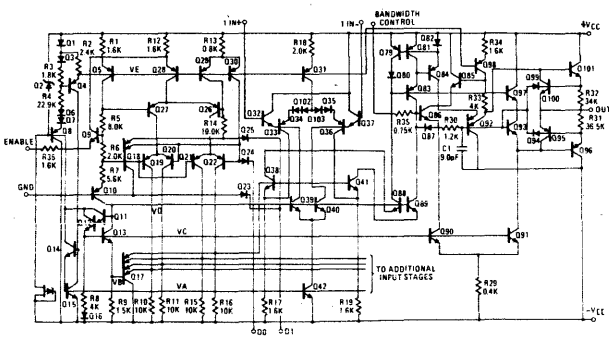


Diagram includes: ONE INPUT STAGE, DECODE CONTROL, BIAS NETWORK AND OUTPUT STAGE

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V− Terminals	45.0V	Internal Power Dissipation (Note 13)	300mW
Differential Input Voltage	$\pm V_{Supply}$	Operating Temperature Range	$-55^oC \leq T_A \leq +125^oC$ (HA-2400)
Digital Input Voltage	−0.76V to +10.0V		$-25^oC \leq T_A \leq +85^oC$ (HA-2404)
Output Current	Short Circuit Protected		$0^oC \leq T_A \leq +75^oC$ (HA-2405)
		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ unless otherwise specified.

Digital inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4V$
Limits apply to each of the four channels, when addressed.

PARAMETER	TEMP.	HA-2400/HA-2404 LIMITS MIN.	TYP.	MAX.	HA-2405 LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		2	5		4	9	mV
	Full			7			11	mV
* Bias Current (Note 12)	+25°C		50	200		50	250	nA
	Full			400			500	nA
* Offset Current (Note 12)	+25°C		5	50		5	50	nA
	Full			100			100	nA
Input Resistance (Note 12)	+25°C		30			30		MΩ
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 1,5)	+25°C	50K	150K		50K	150K		V/V
	Full	25K			25K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		dB
Gain Bandwidth (Note 3)	+25°C		40			40		MHz
(Note 4)	+25°C		8			8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		V
Output Current	+25°C		20			20		mA
Full Power Bandwidth (Notes 3, 5)	+25°C		500			500		kHz
(Notes 4,5)	+25°C		200			200		kHz
TRANSIENT RESPONSE								
Rise Time (Notes 4,6)	+25°C		20			20		ns
Overshoot (Notes 4,6)	+25°C		25			25		%
Slew Rate (Notes 3,7)	+25°C		30			30		V/μs
(Notes 4,7)	+25°C		8			8		V/μs
Settling Time (Notes 4, 7, 8)	+25°C		1.5			1.5		μs
CHANNEL SELECT CHARACTERISTICS								
Digital Input Current ($V_{IN} = 0V$)	Full		1			1		mA
Digital Input Current ($V_{IN} = +5.0V$)	Full		5			5		nA
Output Delay (Note 9)	+25°C		100			100		ns
Crosstalk (Note 10)	+25°C	-80	-110		-74	-110		dB
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		4.8	6.0		4.8	6.0	mA
* Power Supply Rejection Ratio (Note 11)	Full	74	90		74	90		dB

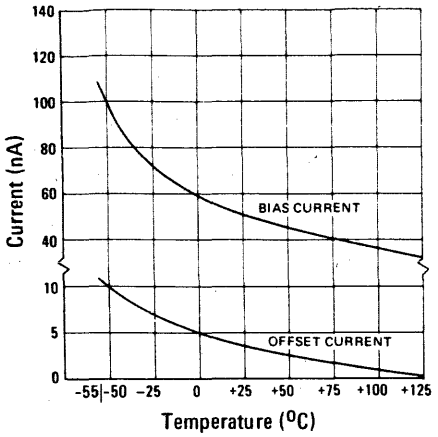
NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 5$ V.D.C.
3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2K\Omega$, $C_L = 50pF$
4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2K\Omega$, $C_L = 50pF$
5. $V_{OUT} = 20V$ peak-to-peak
6. $V_{OUT} = 400$ mV peak-to-peak
7. $V_{OUT} = 10.0V$ peak-to-peak
8. To 0.1% of final value
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output; $V_{IN} = \pm 10$ V.D.C.
11. $V_{SUPP} = \pm 10$V.D.C. to ± 20V.D.C.
12. Unselected channels have approximately the same input parameters.
13. Derate by 4.3mW/°C above 105°C

*100% Tested For DASH 8

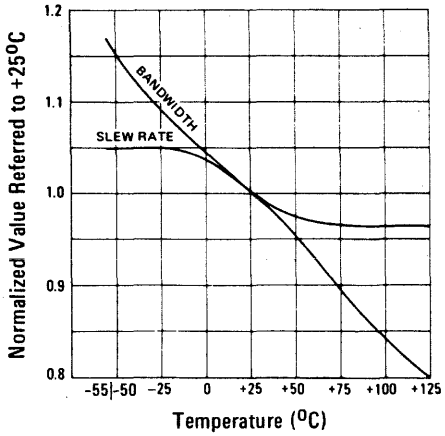
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V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.

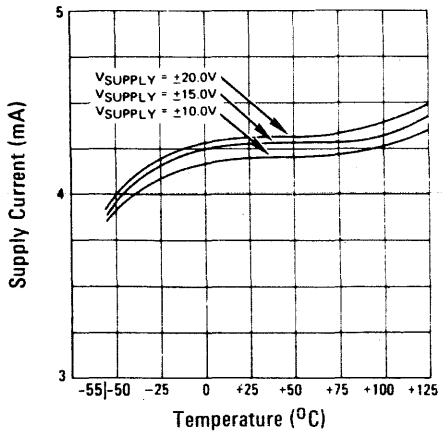
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



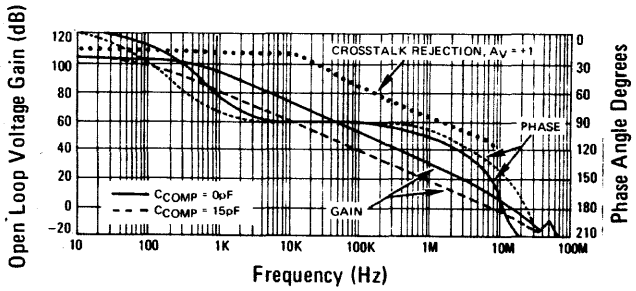
NORMALIZED A.C. PARAMETERS VS. TEMPERATURE



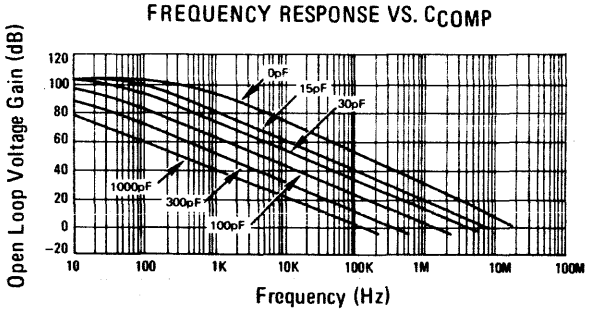
POWER SUPPLY CURRENT DRAIN AS A FUNCTION OF TEMPERATURE



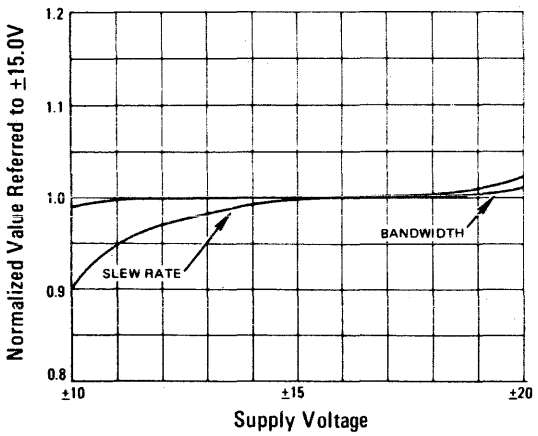
OPEN LOOP FREQUENCY AND PHASE RESPONSE



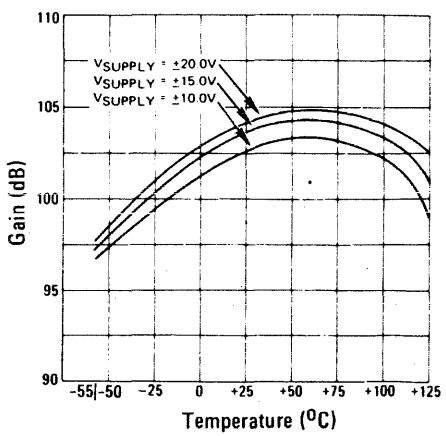
FREQUENCY RESPONSE VS. C_{COMP}



NORMALIZED A.C. PARAMETERS VS. SUPPLY VOLTAGE



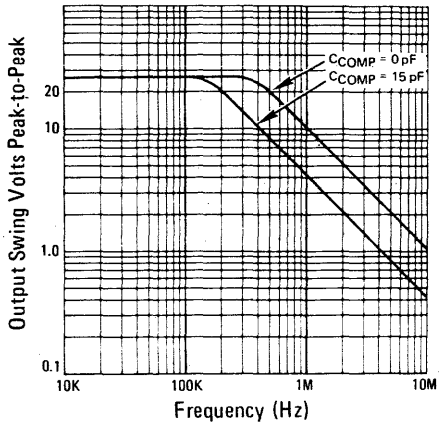
OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE



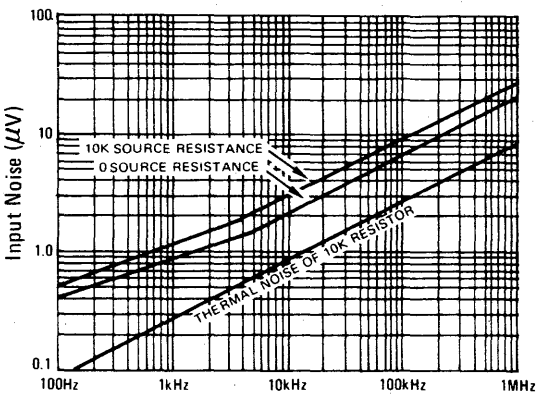
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CHARACTERISTIC CURVES (continued)

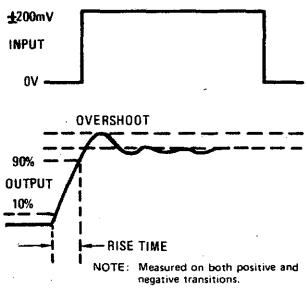
OUTPUT VOLTAGE SWING VS. FREQUENCY



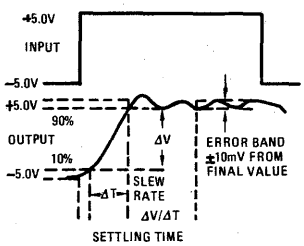
EQUIVALENT INPUT NOISE VS. BANDWIDTH



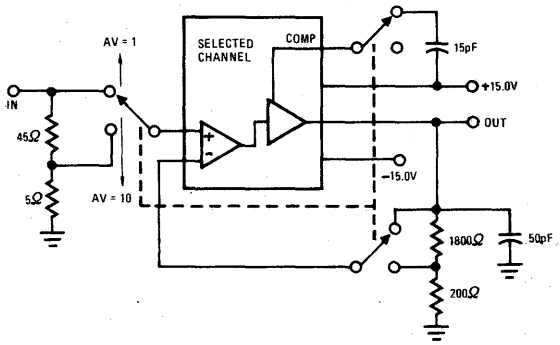
TRANSIENT RESPONSE



SLEW RATE AND SETTLING

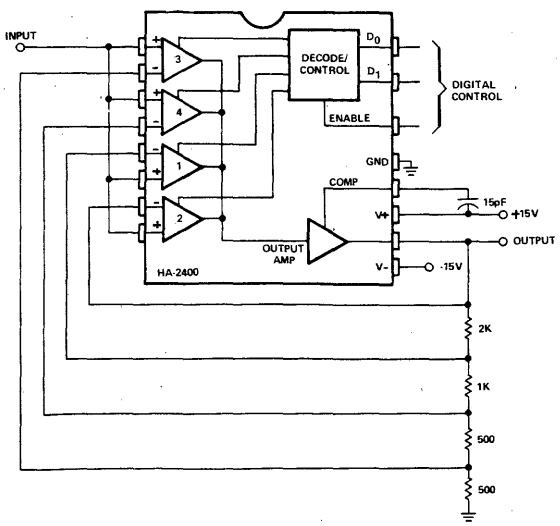


SLEW RATE AND TRANSIENT RESPONSE

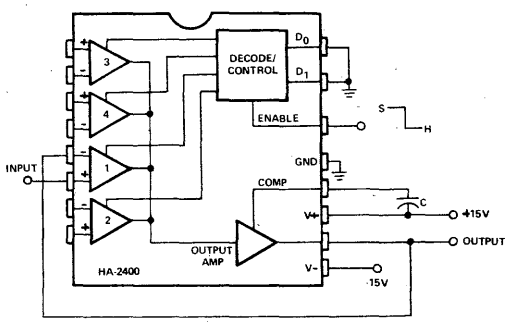


TYPICAL APPLICATIONS

AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN



SAMPLE AND HOLD



Sample charging rate = $\frac{I_1}{C}$ V/sec.

Hold drift rate = $\frac{I_2}{C}$ V/sec.

Switch pedistal error = $\frac{Q}{C}$ Volts

$I_1 \approx 150 \times 10^{-6}$ A

$I_2 \approx 200 \times 10^{-9}$ A @ +25°C

$\approx 600 \times 10^{-9}$ A @ -55°C

$\approx 100 \times 10^{-9}$ A @ +125°C

$Q \approx 2 \times 10^{-12}$ Coul.

FOR MORE EXAMPLES, SEE HARRIS APPLICATION NOTE 514

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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2500/02/05

Precision High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE 30V/μS
- FAST SETTLING 330ns
- WIDE POWER BANDWIDTH 500kHz
- HIGH GAIN BANDWIDTH 12MHz
- HIGH INPUT IMPEDANCE 100MΩ
- LOW OFFSET CURRENT 10nA
- INTERNALLY COMPENSATED

APPLICATIONS

- DATA ACQUISTION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

HA-2500/2502/2505 comprise a series of monolithic operational amplifiers whose designs are optimized to deliver excellent slew rate, bandwidth, and settling time specifications. The outstanding dynamic features of this internally compensated device are complemented with low offset voltage and offset current.

These dielectrically isolated amplifiers are ideally suited for applications such as data acquisition, R.F., video, and pulse conditioning circuits. Slew rate of ±25V/μs and 330ns (0.1%) settling time make these devices excellent components in fast, accurate data acquisition and pulse amplification designs. 12 MHz bandwidth and 500kHz power bandwidth make these devices well suited to R.F. and video applications. With 2mV typical offset voltage plus offset trim capability and 10nA offset current, HA-2500/2502/2505 are particularly useful components in signal conditioning designs.

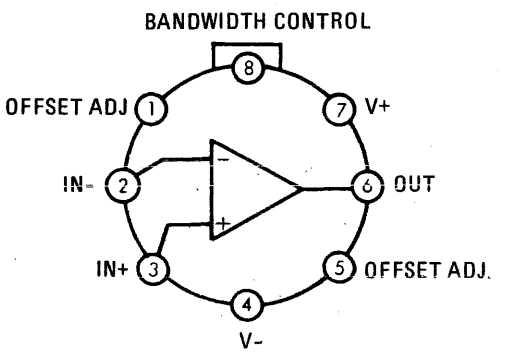
The gain and offset voltage figures of the HA-2500 series are optimized by internal component value changes while the similar design of the HA-2510 series is maximized for slew rate.

HA-2500/2502/2505 are available in metal can (TO-99) packages. HA-2500 and HA-2502 are specified over the -55°C to +125°C range. HA-2505 is specified from 0°C to +75°C.

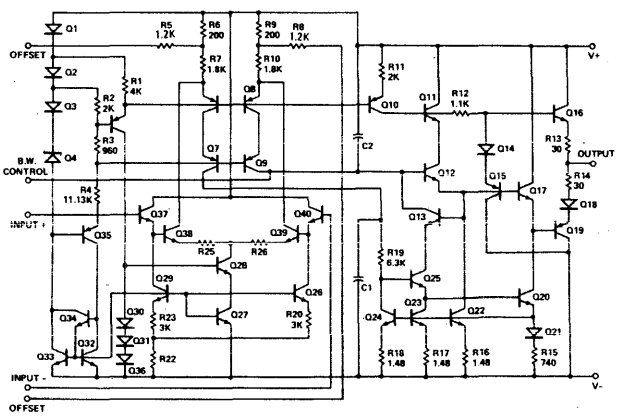
PINOUT

TO-99 **Package Code 2A**

Top View



SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range –	HA-2500/HA-2502	$-55^oC \leq T_A \leq +125^oC$
Differential Input Voltage	±15.0V		HA-2505	$0^oC \leq T_A \leq +75^oC$
Peak Output Current	50mA	Storage Temperature Range		$-65^oC \leq T_A \leq +150^oC$
Internal Power Dissipation	300mW			

ELECTRICAL CHARACTERISTICS

V+ = +15V D.C., V- = -15V D.C.

PARAMETER	TEMP.	HA-2500 -55°C to +125°C LIMITS MIN.	HA-2500 TYP.	HA-2500 MAX.	HA-2502 -55°C to +125°C LIMITS MIN.	HA-2502 TYP.	HA-2502 MAX.	HA-2505 0°C to +75°C LIMITS MIN.	HA-2505 TYP.	HA-2505 MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C		2	5		4	8		4	8	mV
	Full			8			10			10	mV
Offset Voltage Average Drift	Full		20			20			20		µV/°C
* Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
* Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance	+25°C	25	50		20	50		20	50		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Note 1,4)	+25°C	20K	30K		15K	25K		15K	25K		V/V
	Full	15K			10K			10K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	350	500		300	500		300	500		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
* Slew Rate (Notes 1,4,5 & 8)	+25°C	±25	±30		±20	±30		±20	±30		V/µs
Settling Time to 0.1% (Notes 1,4,5 & 8)	+25°C		0.33			0.33			0.33		µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		4	6		4	6		4	6	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

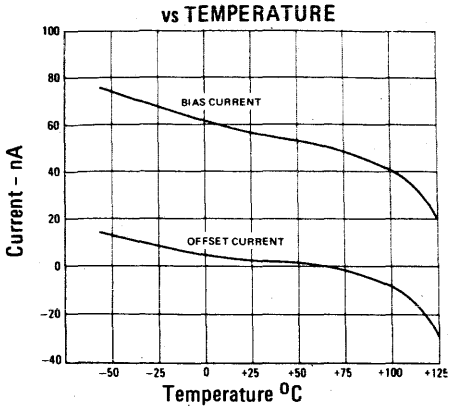
NOTES:
1. R_L = 2K
2. V_{CM} = ±5.0V
3. A_V >10
4. V_O = ±10.0V
5. C_L = 50pF
6. V_O = ±400mV
7. V_O = ±600mV
8. See transient response test circuits and waveforms page four.
9. ΔV = ±5.0V

100% Tested For DASH 8

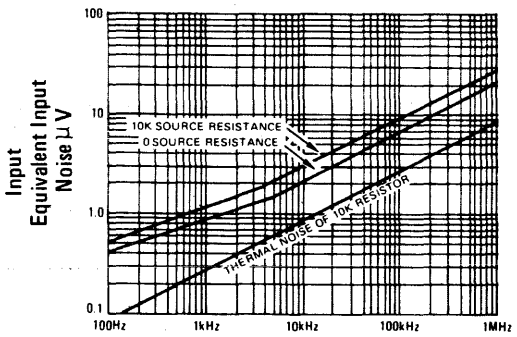
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V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

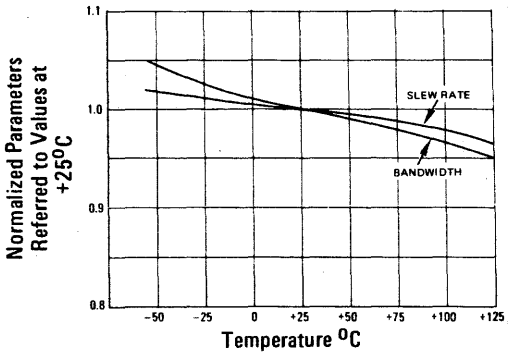
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



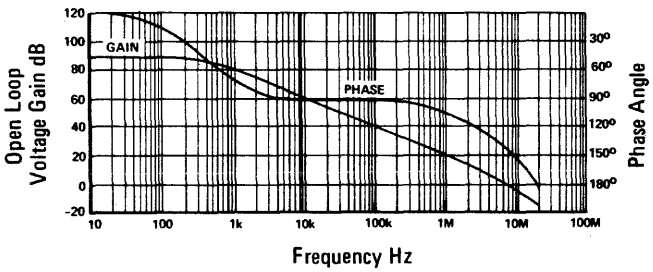
EQUIVALENT INPUT NOISE vs BANDWIDTH



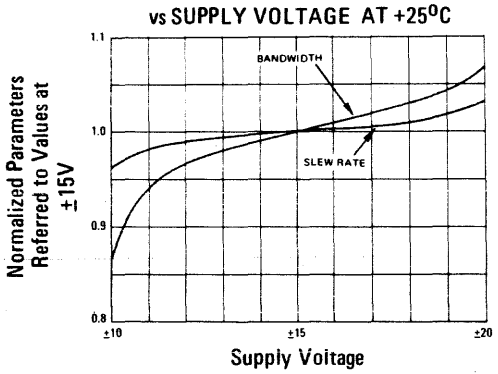
NORMALIZED AC PARAMETERS vs TEMPERATURE



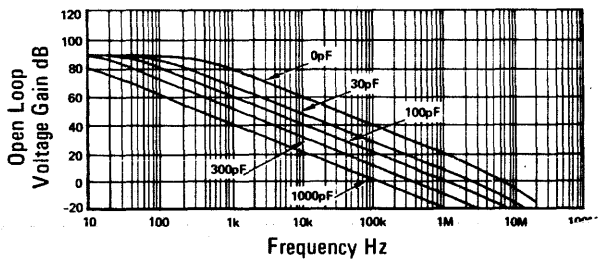
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C

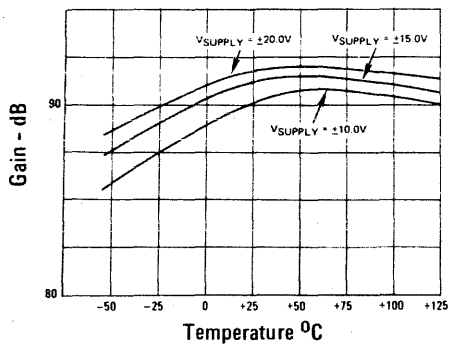


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

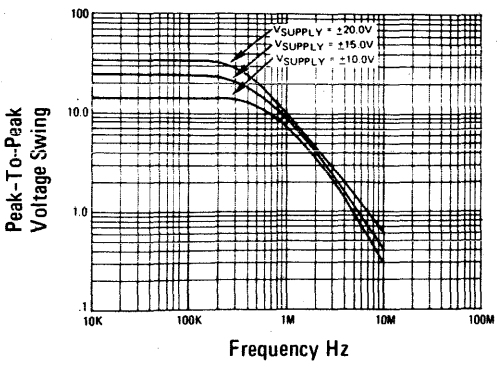


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

OPEN LOOP VOLTAGE GAIN vs TEMPERATURE



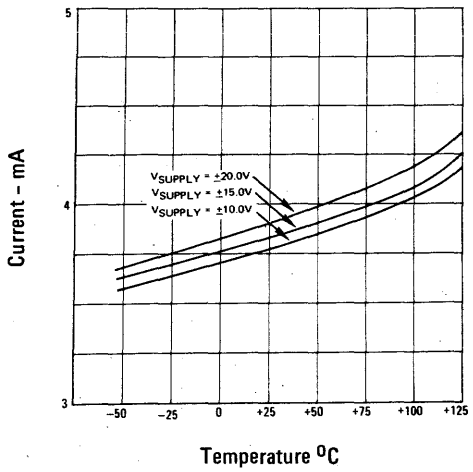
OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C



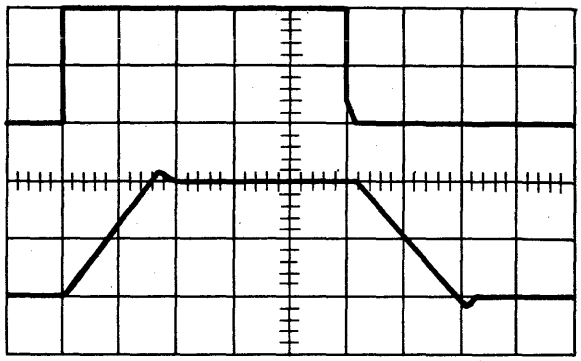
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PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT vs TEMPERATURE



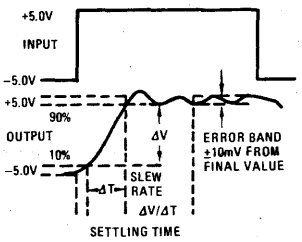
VOLTAGE FOLLOWER PULSE RESPONSE



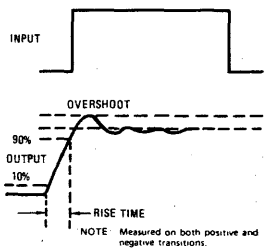
R_L = 2KΩ, C_L = 50pF
Upper Trace: Input
Lower Trace: Output

Vertical = 5V/Div.
Horizontal = 200ns/Div.
T_A = +25°C, V_S = ±15.0V

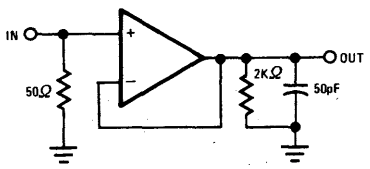
SLEW RATE AND SETTLING TIME



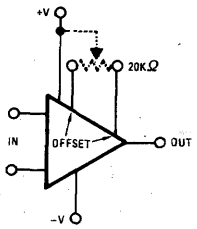
TRANSIENT RESPONSE



SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST HOOK-UP



DEFINITIONS

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT – The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE – The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE – The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

TRANSIENT RESPONSE – The closed loop step function response of the amplifier under small signal conditions.

GAIN BANDWIDTH PRODUCT – The product of the gain and the bandwidth at a given gain.

SLEW RATE (Rating Limiting) – The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing) . . . restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

SETTLING TIME – Time required for output waveform to remain within 0.1 percent of final value.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2510/2512/2515

High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE — 60V/μs
- FAST SETTLING — 250ns
- WIDE POWER BANDWIDTH — 1,000kHz
- HIGH GAIN BANDWIDTH — 12MHz
- HIGH INPUT IMPEDANCE — 100MΩ
- LOW OFFSET CURRENT — 10nA
- INTERNALLY COMPENSATED

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

The HA-2510/2512/2515 are a series of high performance operational amplifiers which set the standards for maximum slew rate, highest accuracy and widest bandwidth for internally compensated monolithic devices. In addition to excellent dynamic characteristics, these dielectrically isolated amplifiers also offer low offset current and high input impedance.

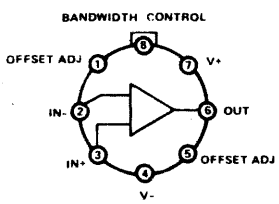
The ±60V/ μs slew rate and 250ns (0.1%) settling time of these amplifiers is ideally suited for high speed D/A, A/D, and pulse amplification designs. HA-2510/2512/2515's superior 12MHz gain bandwidth and 1000kHz power bandwidth is extremely useful in R.F. and video applications. For accurate signal conditioning these amplifiers also provide 10nA offset current, coupled with 100MΩ input impedance, and offset trim capability.

The HA-2510/2512 are available in metal can (TO-99) and 14-pin flat packages. HA-2510 and HA-2512 are specified from -55°C to +125°C. HA-2515 is specified over the 0°C to +75°C range, and is available in the TO-99 package.

PINOUT

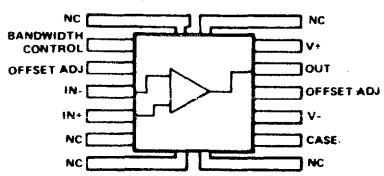
TO-99 TOP VIEW

Package Code 2A

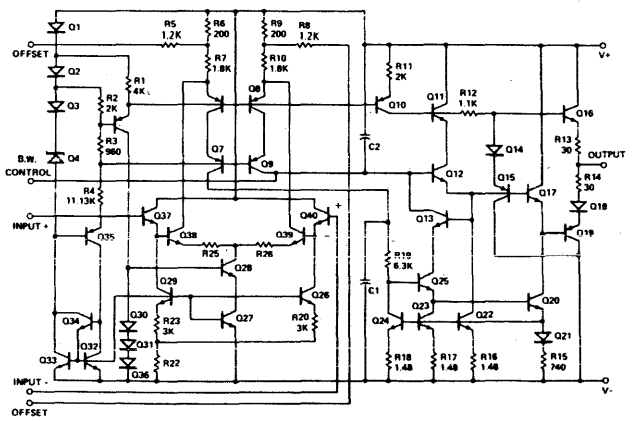


TO-86 TOP VIEW

Package Code 9V
(HA-2510/2512 Only)



SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
HA-2510/HA-2512	$-55^oC \leq T_A \leq +125^oC$		
HA-2515	$0^oC \leq T_A \leq +75^oC$		

ELECTRICAL CHARACTERISTICS

V+ = +15V D.C., V– = 15V D.C.

PARAMETER	TEMP.	HA-2510 -55°C to +125°C LIMITS MIN.	HA-2510 TYP.	HA-2510 MAX.	HA-2512 -55°C to +125°C LIMITS MIN.	HA-2512 TYP.	HA-2512 MAX.	HA-2515 0°C to +75°C LIMITS MIN.	HA-2515 TYP.	HA-2515 MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
* Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
* Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Note 1,4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	750	1000		600	1000		600	1000		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
* Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±50	±65		±40	±60		±40	±60		V/µs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		0.25			0.25			0.25		µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		4	6		4	6		4	6	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

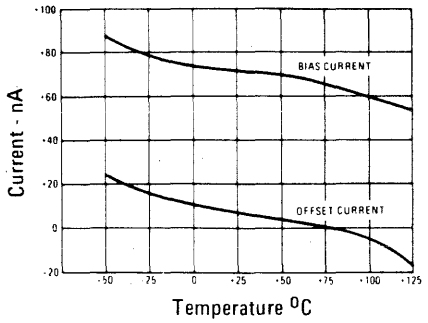
NOTES:
1. R_L = 2K
2. $V_{CM} = \pm 5.0V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. C_L = 50pF
6. $V_O = \pm 400mV$
7. $V_O = \pm 600mV$
8. See transient response test circuits and waveforms page four.
9. $\Delta V = \pm 5.0V$

*100% Tested For DASH 8

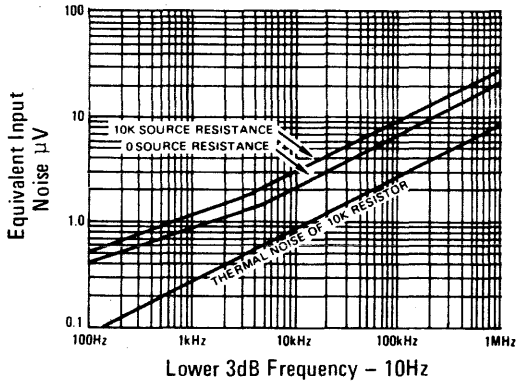
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V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.

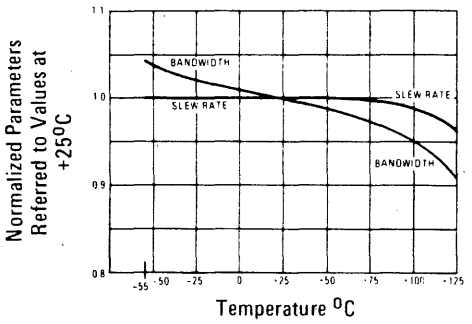
INPUT BIAS AND OFFSET CURRENT
vs TEMPERATURE



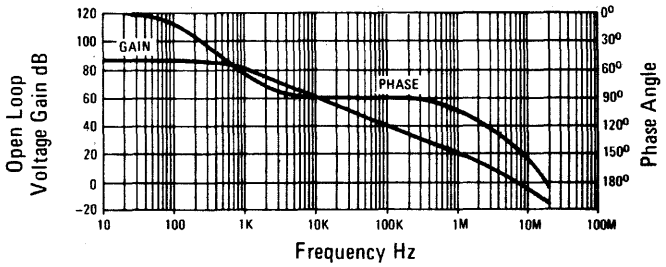
EQUIVALENT INPUT NOISE
vs BANDWIDTH



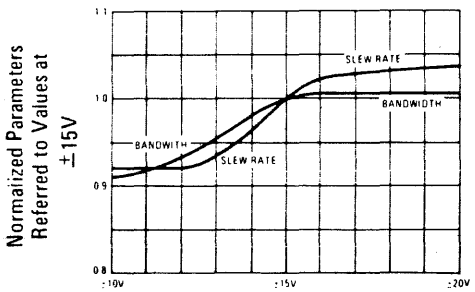
NORMALIZED AC PARAMETERS
vs TEMPERATURE



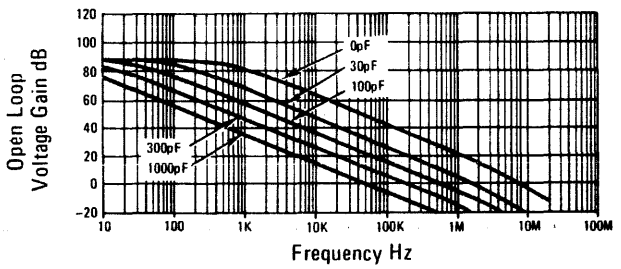
OPEN LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS
vs SUPPLY VOLTAGE

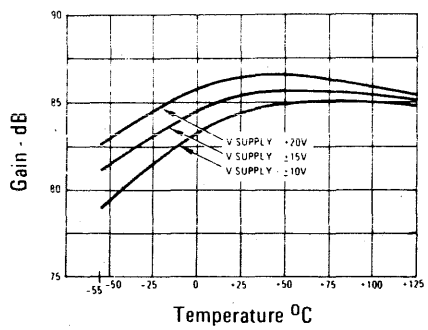


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

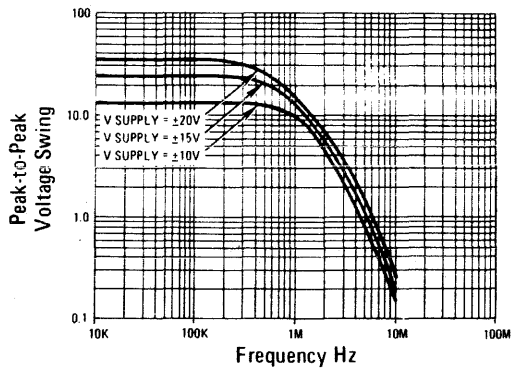


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

OPEN LOOP VOLTAGE GAIN
vs TEMPERATURE



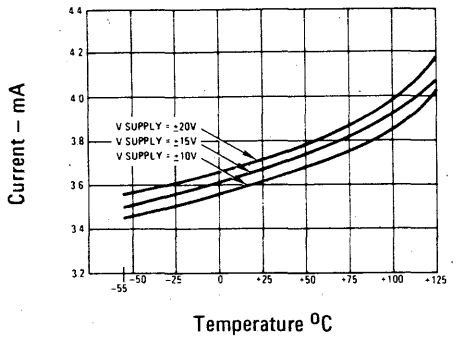
OUTPUT VOLTAGE SWING
vs FREQUENCY AT +25°C



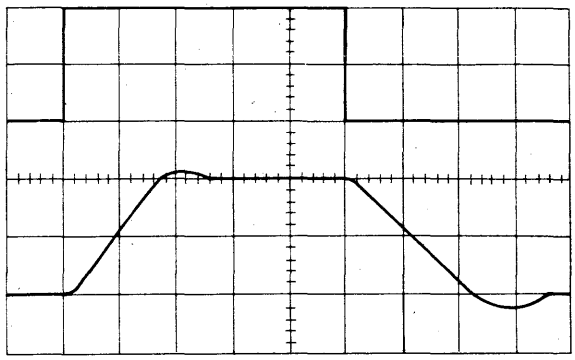
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PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT
VS
TEMPERATURE



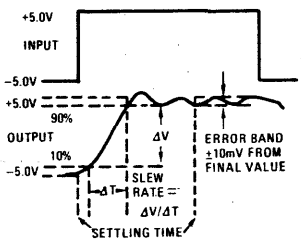
VOLTAGE FOLLOWER PULSE RESPONSE



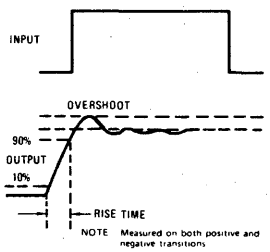
$R_L = 2K\,\Omega$, $C_L = 50pF$
Upper Trace: Input
Lower Trace: Output

Vertical = 5V/Div.
Horizontal = 100n/Div.
$T_A = +25^oC$, $V_S = \pm 15.0V$

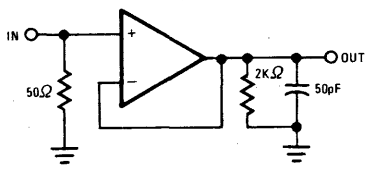
SLEW RATE AND
SETTLING TIME



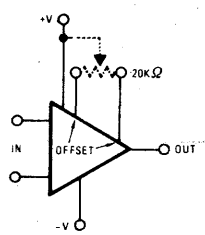
TRANSIENT RESPONSE



SLEW RATE AND
TRANSIENT RESPONSE



SUGGESTED
OFFSET ZERO
ADJUST HOOK-UP



DEFINITIONS

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT – The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE – The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE – The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO – The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING – The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE – The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE – The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN – The ratio of the change in output voltage to the change in input voltage producing it.

UNITY GAIN BANDWIDTH – The frequency at which the voltage gain of the amplifier is unity.

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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2520/22/25

Uncompensated High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE — 120V/μs
- FAST SETTLING — 200ns
- WIDE POWER BANDWIDTH — 2,000kHz
- HIGH GAIN BANDWIDTH — 20MHz
- HIGH INPUT IMPEDANCE — 100MΩ
- LOW OFFSET CURRENT — 10nA

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

HA-2520/2522/2525 comprise a series of monolithic operational amplifiers delivering an unsurpassed combination of specifications for slew rate, bandwidth and settling time. These dielectrically isolated amplifiers are controlled at closed loop gains greater than 3 without external compensation. In additon, these high performance components also provide low offset current and high input impedance.

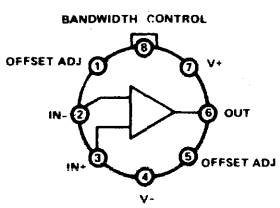
120V/μs slew rate and 200ns (0.1%) settling time of these amplifiers make them ideal components for pulse amplification and data acquisition designs. These devices are valuable components for R.F. and video circuitry requiring up to 20MHz gain bandwidth and 2MHz power bandwidth. For accurate signal conditioning designs the HA-2520/2522/2525's superior dynamic specifications are complimented by 10nA offset current, 100MΩ input impedance and offset trim capability.

The HA-2520/2522 are available in metal can (TO-99) and 14-pin flat packages. HA-2520 and HA-2522 are specified over -55°C to +125°C range. HA-2525 is specified from 0°C to +75°C, and is available in the TO-99 package.

PINOUT

TO-99

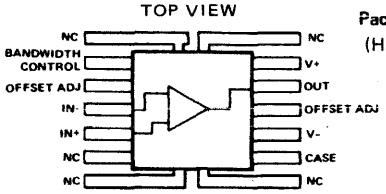
TOP VIEW



Package Code 2A

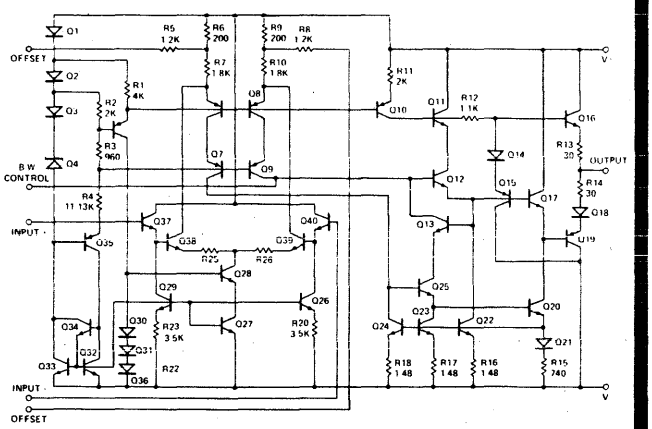
TO-86

TOP VIEW



Package Code 9V
(HA-2520/2522 Only)

SCHEMATIC



SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range			
HA-2520/2522	$-55^oC \leq T_A \leq +125^oC$	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
HA-2525	$0^oC \leq T_A \leq +75^oC$		

ELECTRICAL CHARACTERISTICS

$V+ = +15V$ D.C., $V- = -15V$ D.C.

PARAMETER	TEMP.	HA-2520 -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2522 -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2525 0°C to +75°C LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
* Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
* Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Note 1,4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		20			20			20		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	1500	2000		1200	1600		1200	1600		kHz
TRANSIENT RESPONSE ($A_V = +3$)											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		25	40		25	50		25	50	%
* Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±100	±120		±80	±120		±80	±120		V/µs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		0.20			0.20			0.20		µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		4	6		4	6		4	6	mA
* Power Supply Rejection Ratio (Note 7)	Full	80	90		74	90		74	90		dB

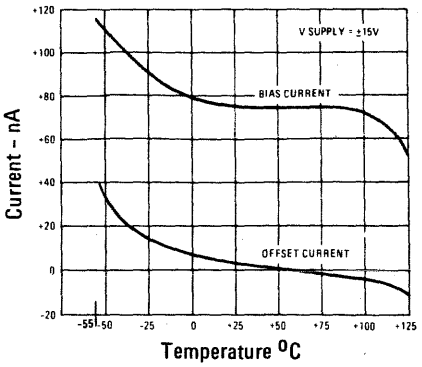
NOTES:
1. $R_L = 2K$
2. $V_{CM} = \pm 5.0V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$
7. $\Delta V = \pm 5.0V$
8. See transient response test circuits and waveforms page four.

*100% Tested For DASH 8

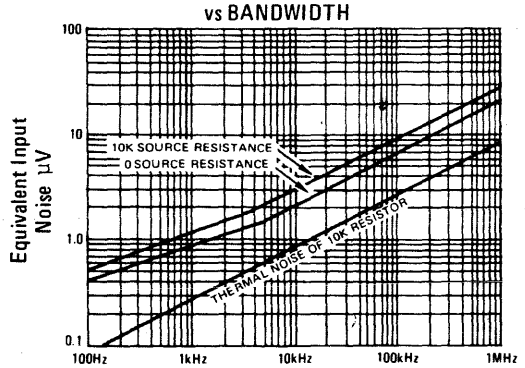
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V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

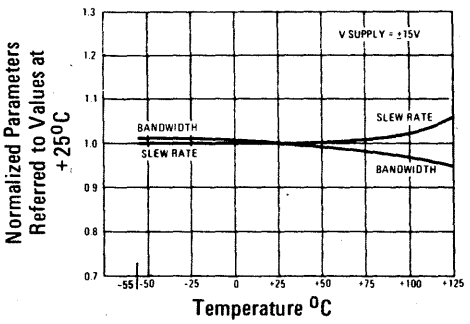
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



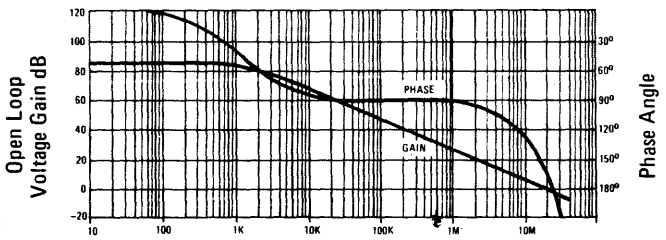
EQUIVALENT INPUT NOISE vs BANDWIDTH



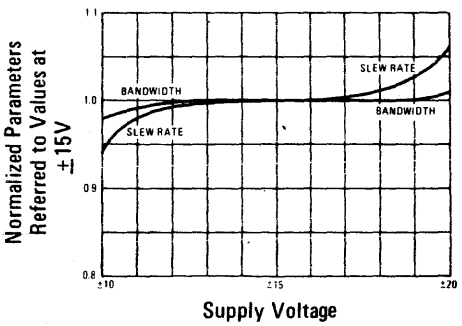
NORMALIZED AC PARAMETERS vs TEMPERATURE



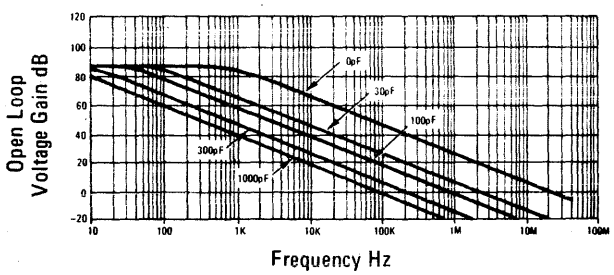
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



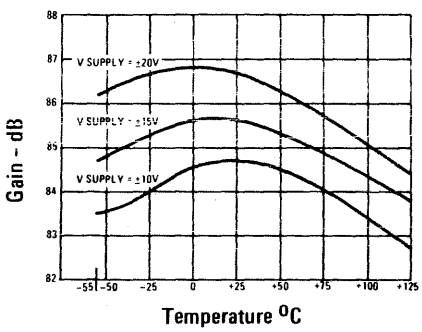
NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C



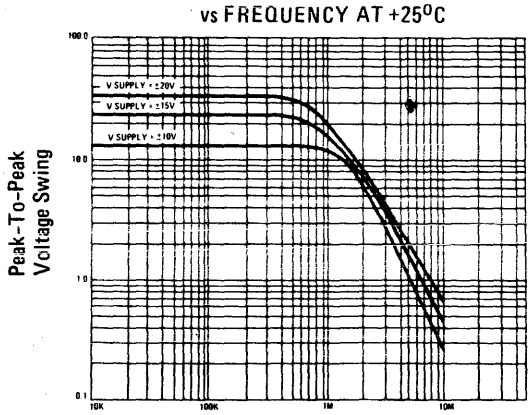
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



OPEN LOOP VOLTAGE GAIN vs TEMPERATURE



OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C



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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range			
HA-2520/2522	$-55^oC \leq T_A \leq +125^oC$	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
HA-2525	$0^oC \leq T_A \leq +75^oC$		

ELECTRICAL CHARACTERISTICS

V+ = +15V D.C., V- = -15V D.C.

PARAMETER	TEMP.	HA-2520 -55°C to +125°C LIMITS MIN.	HA-2520 TYP.	HA-2520 MAX.	HA-2522 -55°C to +125°C LIMITS MIN.	HA-2522 TYP.	HA-2522 MAX.	HA-2525 0°C to +75°C LIMITS MIN.	HA-2525 TYP.	HA-2525 MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
* Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
* Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Note 1,4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		20			20			20		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	1500	2000		1200	1600		1200	1600		kHz
TRANSIENT RESPONSE (A_V = +3)											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		25	40		25	50		25	50	%
* Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±100	±120		±80	±120		±80	±120		V/µs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		0.20			0.20			0.20		µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		4	6		4	6		4	6	mA
* Power Supply Rejection Ratio (Note 7)	Full	80	90		74	90		74	90		dB

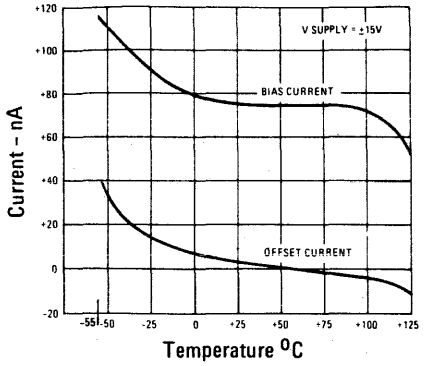
NOTES:
1. R_L = 2K
2. V_{CM} = ±5.0V
3. $A_V > 10$
4. V_O = ±10.0V
5. C_L = 50pF
6. V_O = ±200mV
7. ΔV = ±5.0V
8. See transient response test circuits and waveforms page four.

*100% Tested For DASH 8

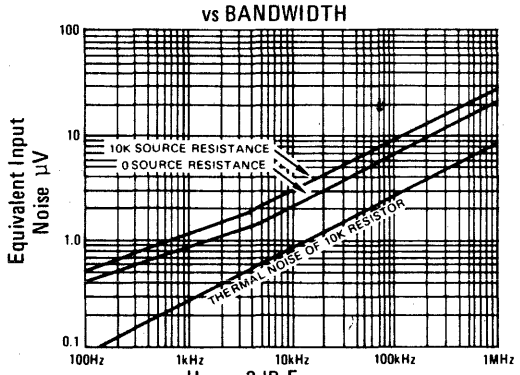
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V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

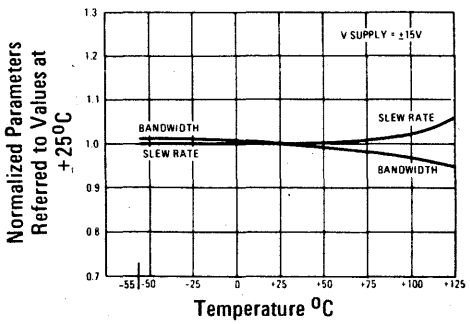
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



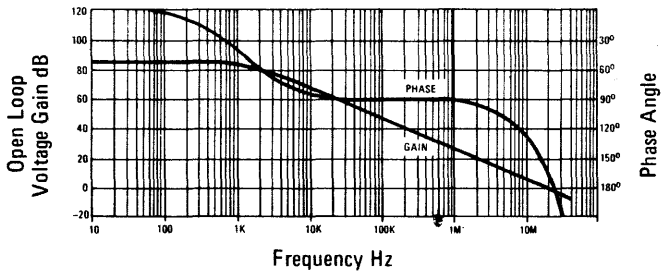
EQUIVALENT INPUT NOISE vs BANDWIDTH



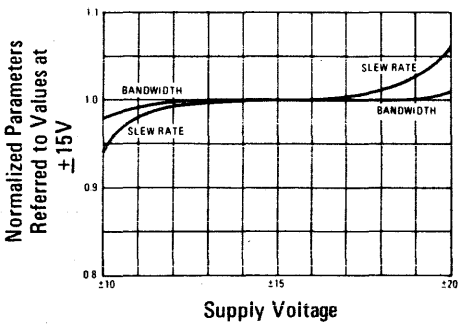
NORMALIZED AC PARAMETERS vs TEMPERATURE



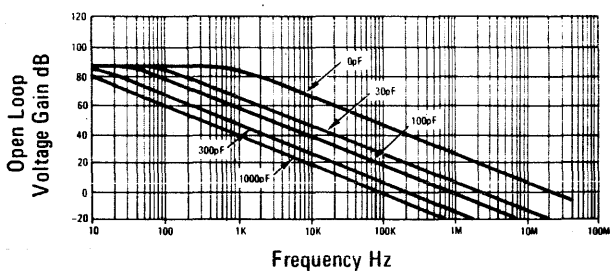
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



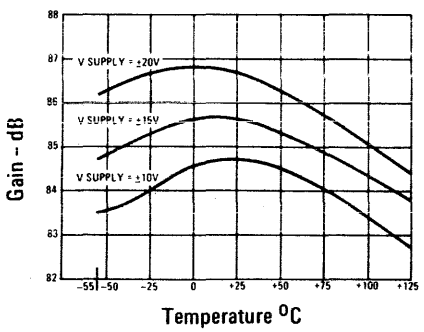
NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C



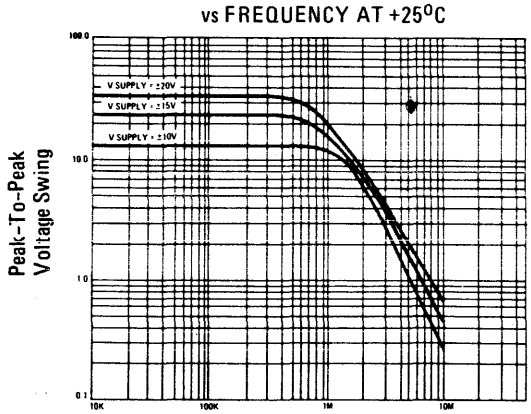
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



OPEN LOOP VOLTAGE GAIN vs TEMPERATURE



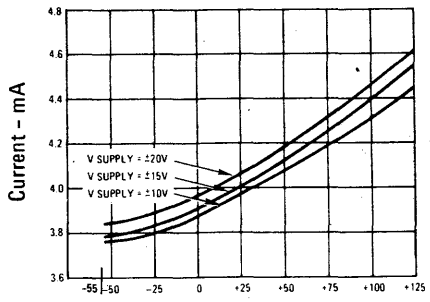
OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C



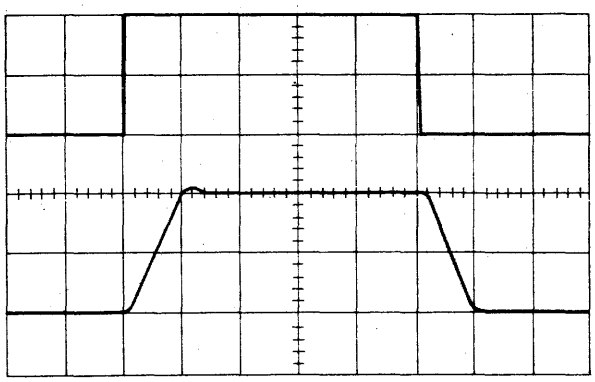
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PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT vs TEMPERATURE



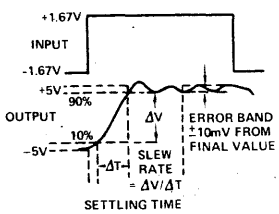
VOLTAGE FOLLOWER PULSE RESPONSE



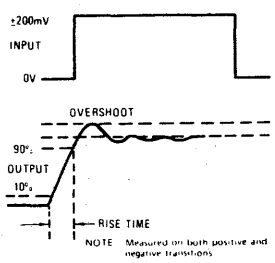
$R_L = 2K\Omega$, $C_L = 50pF$
Upper Trace: Input; 1.33V/Div.
Lower Trace: Output; 5V/Div.

Horizontal = 100ns/Div.
$T_A = +25^oC$, $V_S = \pm 15V$

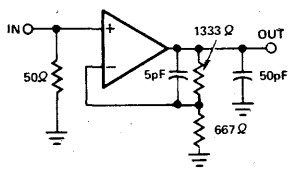
SLEW RATE AND SETTLING TIME



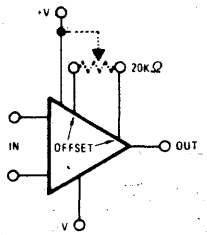
TRANSIENT RESPONSE



SLEW RATE AND TRANSIENT RESPONSE

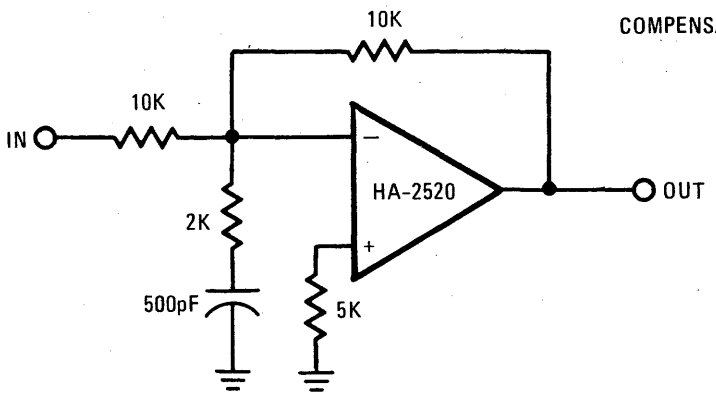


SUGGESTED OFFSET ZERO ADJUST HOOK-UP



TYPICAL APPLICATIONS

COMPENSATION CIRCUIT FOR INVERTING UNITY GAIN



Slew Rate	≈	120V/μs
Bandwidth	≈	10MHz
Settling Time	≈	500ns

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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2530/2535

High Slew Rate, Wideband Inverting Amplifier

FEATURES

- HIGH SLEW RATE ±320V/μs
- FAST SETTLING TIME 550ns
- WIDE POWER BANDWIDTH 5MHz
- HIGH GAIN BANDWIDTH PRODUCT 70MHz
- LOW OFFSET VOLTAGE 0.8mV
- LOW POWER SUPPLY CURRENT 3.5mA

APPLICATIONS

- PULSE AMPLIFICATION
- SIGNAL CONDITIONING
- SIGNAL GENERATORS
- COAXIAL CABLE DRIVERS
- INTEGRATORS

DESCRIPTION

HA-2530 and HA-2535 are monolithic high speed inverting amplifiers which deliver superior slew rate, bandwidth, and accuracy specifications compared to any other amplifier in its class. Designs of these dielectrically isolated amplifiers utilize the feed forward amplifier technique to produce excellent dynamic and DC specifications coupled with low power consumption. These devices require no external compensation at closed loop gains greater than 10.

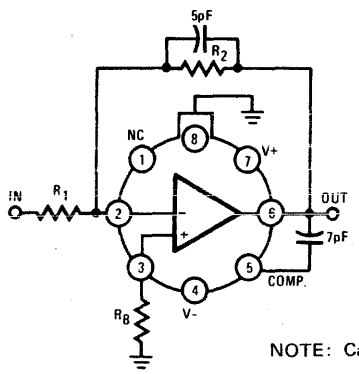
These amplifiers are excellent components for pulse circuits, data acquisition designs, and high speed integrators that can take advantage of the ±320V/μs slew rate and 550ns (0.1%) settling time. 70MHz gain bandwidth product, 5MHz power bandwidth coupled with 0.8mV offset voltage and ±50mA typical output current levels make these amplifiers ideally suited for signal conditioning, signal generation, and coaxial driver applications.

The HA-2530 and HA-2535 are available in metal can (TO-99) packages. HA-2530 is specified over the -55°C to +125°C range while HA-2535 is specified from 0°C to +75°C.

PINOUT

TO-99 **Package Code 2A**

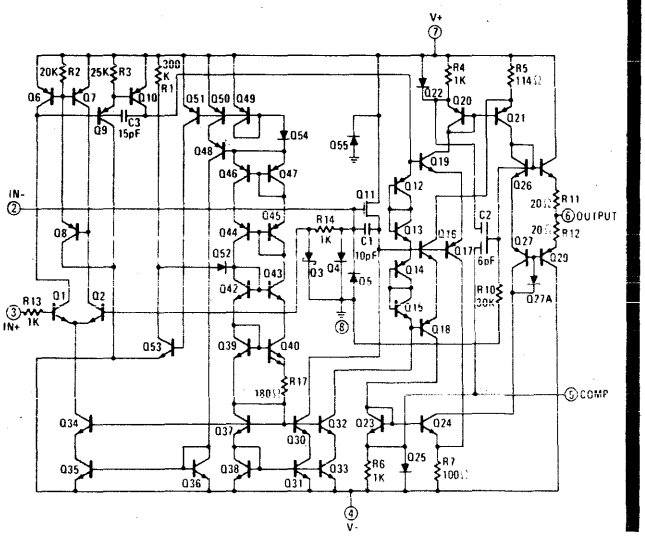
Top View



NOTE: Case tied to V-

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SCHEMATIC



SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V	Internal Power Dissipation (Note 1)	550mW
		Operating Temperature Range	$-55^{o}C \leq T_A \leq +125^{o}C$ (HA-2530)
Peak Output Current	±100mA		$0^{o}C \leq T_A \leq +75^{o}C$ (HA-2535)
		Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{Supply} = ±15.0V Unless Otherwise Specified.

		HA-2530 -55°C to +125°C LIMITS			HA-2535 0°C to +75°C LIMITS			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		0.8			0.8		mV
	Full			3			5	mV
Average Offset Voltage Drift	Full		5			5		µV/°C
* Bias Current	+25°C		15			15		nA
	Full			100			200	nA
* Offset Current	+25°C		5			5		nA
	Full			20			20	nA
Input Resistance	+25°C		2			2		MΩ
Input Capacitance	+25°C		10			10		pF
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 2,5)	+25°C		$2X10^6$			$2X10^6$		V/V
*	Full	10^5			10^5			V/V
* Common-Mode Rejection Ratio (Note 3)	Full	86	100		80	100		dB
Gain Bandwidth Product (Note 4)	+25°C		70			70		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		V
* Output Current (Note 5)	+25°C	±25	±50		±25	±50		mA
Full Power Bandwidth (Note 5)	+25°C	4	5		4	5		MHz
TRANSIENT RESPONSE (NOTES 6&7)								
* Rise Time	+25°C		20	40		20	40	ns
* Overshoot	+25°C		30	45		30	50	%
* Slew Rate	+25°C	±280	±320		±250	±320		V/µs
Settling Time	+25°C		500			500		ns
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		3.5	6		3.5	6	mA
* Power Supply Rejection Ratio (Note 8)	Full	86	100		80	100		dB

NOTES:
1. Derate at 5.5mW/°C for Operation at Ambient Temperature Above 75°C.
2. R_L = 2K
3. V_{CM} = ±5.0V
4. A_V >10
5. V_O = ±10V
6. C_L = 50pF
7. See Transient Response Test Circuit and Wave Forms, Page 4.
8. ΔV = ±5.0V

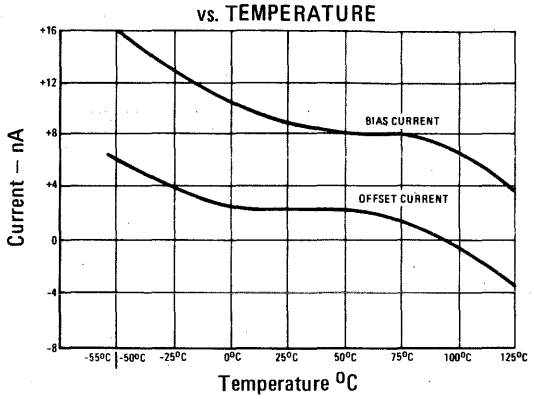
*100% Tested For DASH 8

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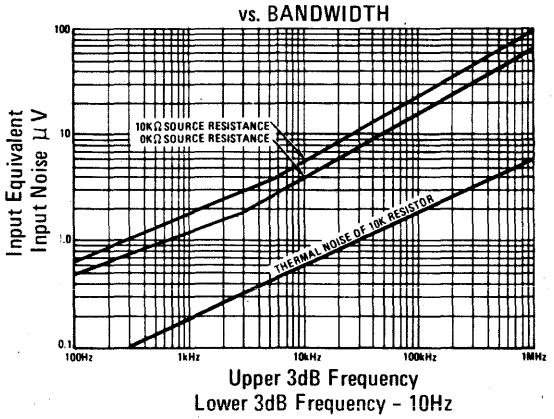
PERFORMANCE CURVES

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

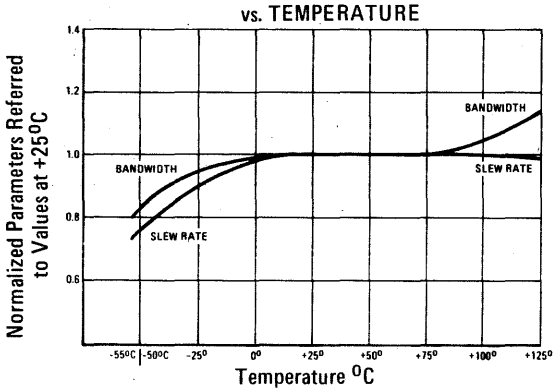
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



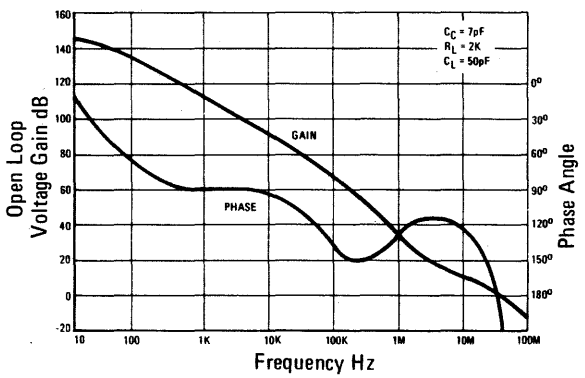
EQUIVALENT INPUT NOISE vs. BANDWIDTH



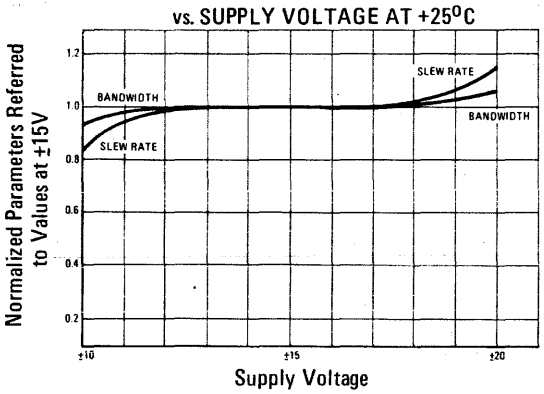
NORMALIZED AC PARAMETERS vs. TEMPERATURE



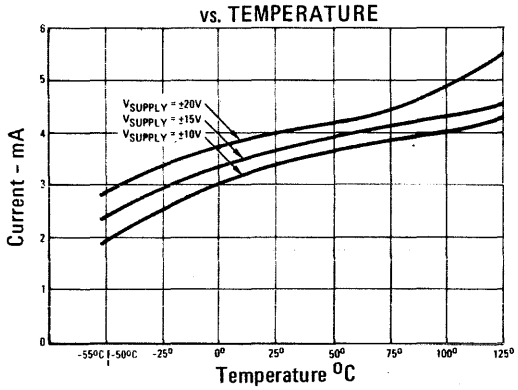
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



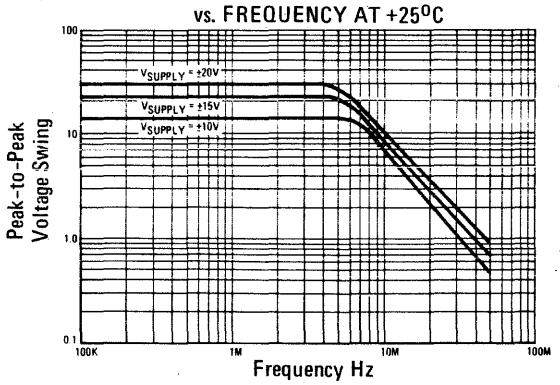
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE AT +25°C



POWER SUPPLY CURRENT vs. TEMPERATURE



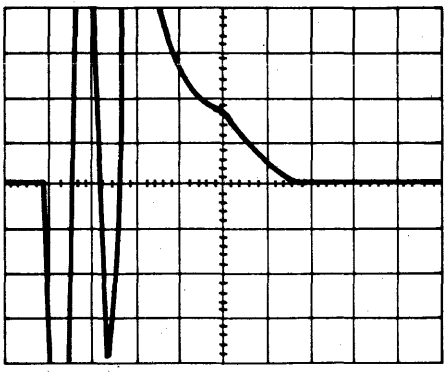
OUTPUT VOLTAGE SWING vs. FREQUENCY AT +25°C



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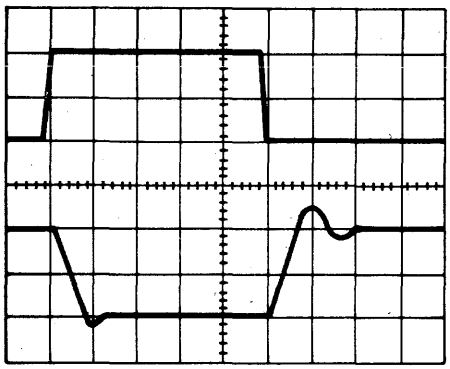
PERFORMANCE CURVES (continued)

SETTLING TIME MEASUREMENT *1



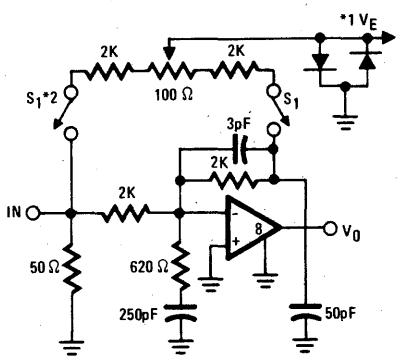
VERTICAL = 5mV/DIV.
HORIZONTAL = 100ns/DIV.
$T_A = +25^oC$, $V_S = \pm 15V$

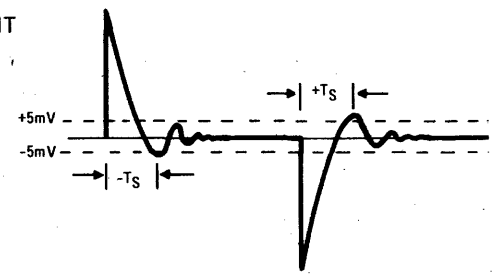
UNITY GAIN PULSE RESPONSE



UPPER TRACE: INPUT VERTICAL = 5V/DIV.
LOWER TRACE: OUTPUT HORIZONTAL = 50ns/DIV.
$T_A = +25^oC$, $V_S = \pm 15V$

SLEW RATE/SETTLING TIME/TRANSIENT RESPONSE TEST CIRCUIT

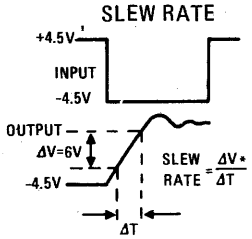




*1 Settling time (T_S) is measured using a high speed high recovery oscilloscope to display the error voltage V_E. When V_E is within ±5mV of final value the output V_O will be within ±10mV (0.1%).

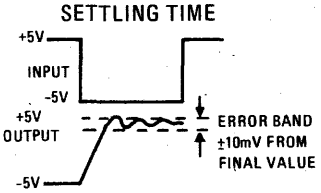
*2 S_1 closed for settling time.

SLEW RATE

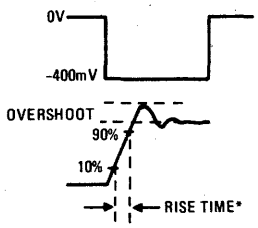


* MEASURED ON BOTH POSITIVE AND NEGATIVE EXCURSIONS.

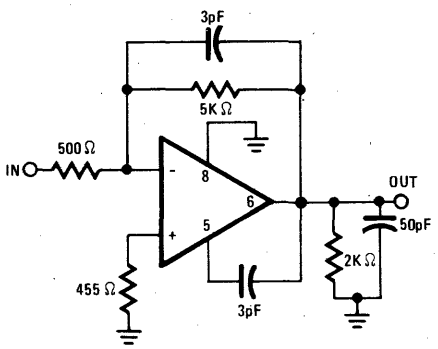
SETTLING TIME



TRANSIENT RESPONSE



5MHz VIDEO AMPLIFIER (A_V = 10)



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2600/2602/2605

Wide Band, High Impedance Operational Amplifier

FEATURES

- WIDE BANDWIDTH — 12MHz
- HIGH INPUT IMPEDANCE — 500MΩ
- LOW INPUT BIAS CURRENT — 1nA
- LOW INPUT OFFSET CURRENT — 1nA
- LOW INPUT OFFSET VOLTAGE — 0.5mV
- HIGH GAIN — 150K V/V
- HIGH SLEW RATE — 7V/μs
- OUTPUT SHORT CIRCUIT PROTECTION

APPLICATIONS

- VIDEO AMPLIFIER
- PULSE AMPLIFIER
- AUDIO AMPLIFIERS AND FILTERS
- HIGH-Q ACTIVE FILTERS
- HIGH-SPEED COMPARATORS
- LOW DISTORTION OSCILLATORS

DESCRIPTION

HA-2600/2602/2605 are internally compensated bipolar operational amplifiers that feature very high input impedance (500 MΩ, HA-2600) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2600) and low bias and offset current (1nA, HA-2600) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 12MHz unity gain-bandwidth product, 7V/μs slew rate and 150,000V/V open-loop gain enables HA-2600/2602/2605 to perform high-gain amplification of fast, wideband signals. These dynamic characterisitics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

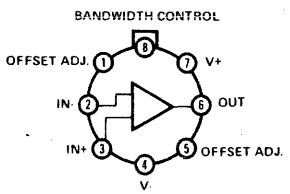
In addition to its application in pulse and video amplifier designs, HA-2600/2602/2605 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators.

HA-2600 and HA-2602 are guaranteed over -55°C to +125°C. HA-2605 is specified from 0°C to +75°C. All devices are available in TO-99 cans, and HA-2600/2602 are available in 10 lead flat packages.

PINOUT

TO-99 TOP VIEW

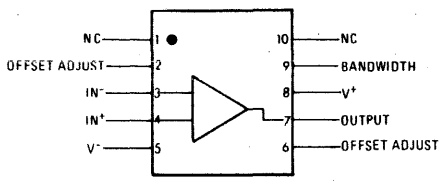
Package Code 2A



Case Connected to V-

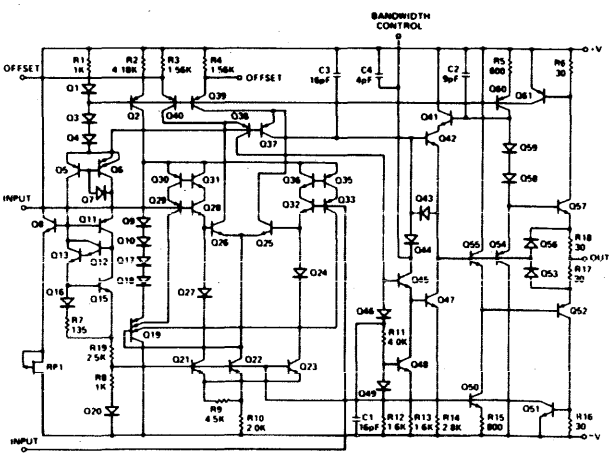
TO-91 TOP VIEW

Package Code 9V
(HA-2600/2602 Only)



Case Connected to V-

SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Operating Temperature Range – HA-2600/HA-2602	$-55^oC \leq T_A \leq +125^oC$
HA-2605	$0^o \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS V+=+15VDC, V- = -15VDC

PARAMETER	TEMP.	HA-2600 −55°C to +125°C LIMITS MIN.	HA-2600 TYP.	HA-2600 MAX.	HA-2602 −55°C to +125°C LIMITS MIN.	HA-2602 TYP.	HA-2602 MAX.	HA-2605 0°C to +75°C LIMITS MIN.	HA-2605 TYP.	HA-2605 MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C		0.5	4		3	5		3	5	mV
	Full		2	6			7			7	mV
Offset Voltage Average Drift	Full		5								µV/°C
* Bias Current	+25°C		1	10		15	25		5	25	nA
	Full		10	30			60			40	nA
* Offset Current	+25°C		1	10		5	25		5	25	nA
	Full		5	30			60			40	nA
Input Resistance	+25°C	100	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Notes 1, 4)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		74	100		dB
Unity Gain Bandwidth (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Note 4)	+25°C	50	75		50	75		50	75		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		30	60		30	60		30	60	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	40		25	40	%
* Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±4	±7		±4	±7		±4	±7		V/µs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		1.5			1.5			1.5		µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

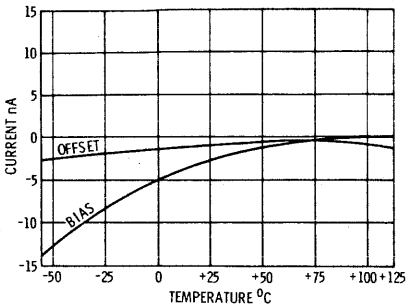
TEST CONDITIONS

NOTES:
1. R_L = 2K
2. V_{CM} = ±5.0V
3. V_O <90mV
4. V_O = ±10V
5. C_L = 100pF
6. V_O = ±200mV
7. V_O = ±400mV
8. See Transient response test circuits and waveforms page three.
9. V_S = ±9.0V to ±15V

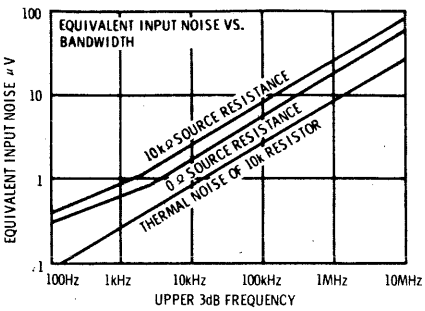
*100% Tested For DASH 8

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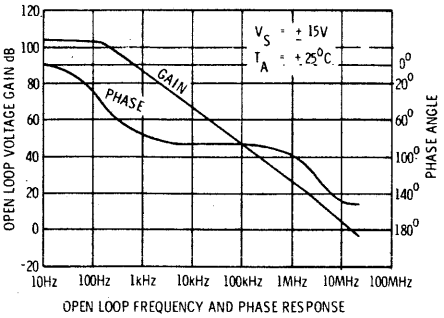
V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.

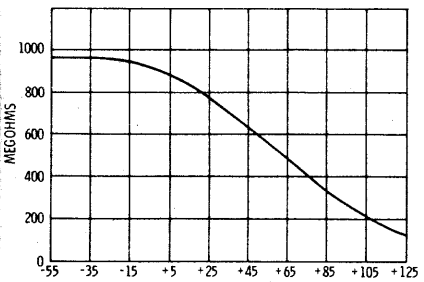


INPUT BIAS CURRENT AND OFFSET CURRENT
AS A FUNCTION OF TEMPERATURE

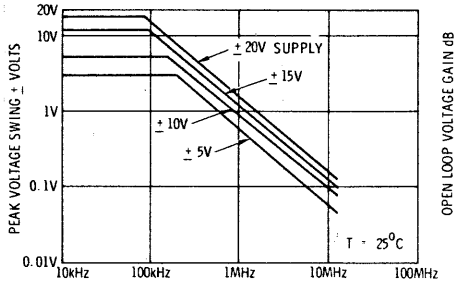


BROADBAND NOISE CHARACTERISTICS

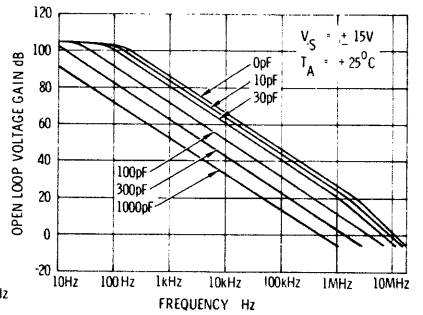




INPUT IMPEDANCE VS. TEMPERATURE, 100Hz

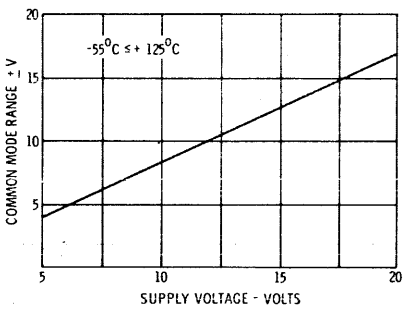


OUTPUT VOLTAGE SWING VS. FREQUENCY

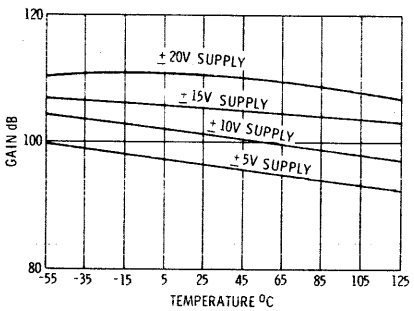


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

Note: External Compensation Components are not Required for Stability, But May be Added to Reduce Bandwidth if Desired. If External Compensation is Used, Also Connect 100pF Capacitor From Output to Ground.

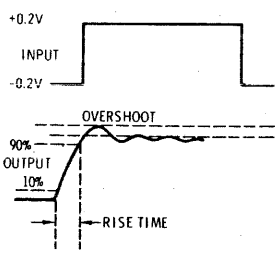


COMMON MODE VOLTAGE RANGE
AS A FUNCTION OF SUPPLY VOLTAGE



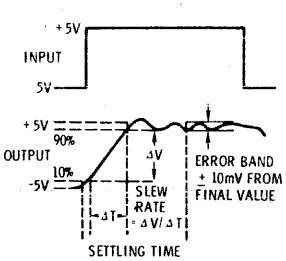
OPEN-LOOP VOLTAGE GAIN VS. TEMPERATURE

TRANSIENT RESPONSE

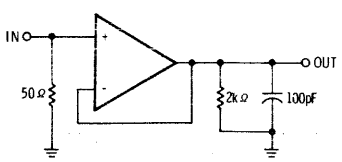


NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSITIONS.

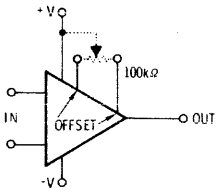
SLEW RATE AND SETTLING TIME



SLEW RATE AND TRANSIENT RESPONSE



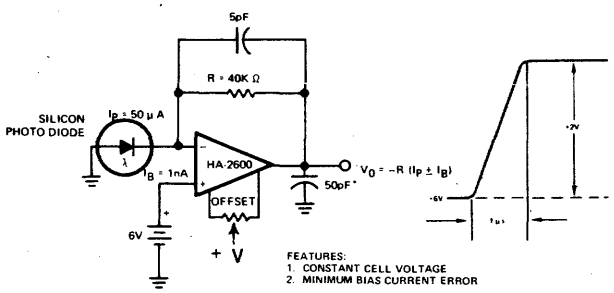
SUGGESTED OFFSET ZERO ADJUST HOOK-UP



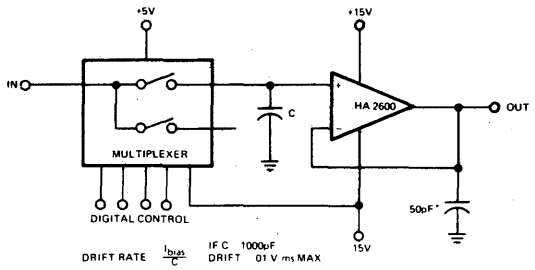
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TYPICAL APPLICATIONS

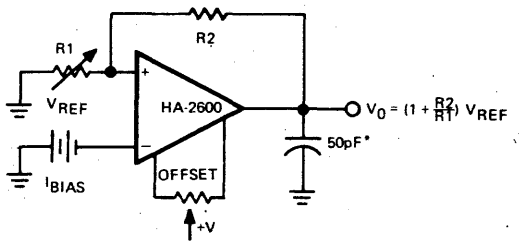
PHOTO-CURRENT TO VOLTAGE CONVERTER



SAMPLE – AND – HOLD

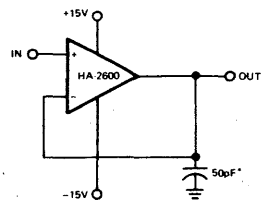


REFERENCE VOLTAGE AMPLIFIER



FEATURES:
1. MINIMUM BIAS CURRENT IN REFERENCE CELL
2. SHORT-CIRCUIT PROTECTION

VOLTAGE FOLLOWER



1.000 GAIN 0.9999
Z_{in} = 10^{12} MIN.
Z_{out} = .01 MAX.
SLEW RATE = 4V/ μ s MIN.
B.W. = 12MHz TYP
OUTPUT SWING = ± 10V MIN. TO 50kHz

*A small load capacitance is recommended in all applications where practical to prevent possible high frequency oscillations resulting from external wiring parasitics. Capacitance up to 100pF has negligible effect on the bandwidth or slew rate.

DEFINITIONS

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT – The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE – The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE – The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO – The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING – The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE – The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE – The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN – The ratio of the change in output voltage to the change in input voltage producing it.

BANDWIDTH – The frequency at which the voltage gain is 3dB below its low frequency value.

UNITY GAIN BANDWIDTH – The frequency at which the voltage gain of the amplifier is unity.

POWER SUPPLY REJECTION RATIO – The ratio of the change in input offset voltage to the change in power supply voltage producing it.

TRANSIENT RESPONSE – The closed loop step function response of the amplifier under small signal conditions.

PHASE MARGIN – $(180^o - (\phi_1 - \phi_2))$ where ϕ_1 is the phase shift at the frequency where the absolute magnitude of gain is unity ϕ_2 is the phase shift at a frequency much lower than the open loop bandwidth.

SLEW RATE (Rate Limiting) – The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing) . . . restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

SETTLING TIME – Time required for output waveform to remain within 0.1% of final value.

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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2620/2622/2625

Very Wide Band, Uncompensated Operational Amplifiers

FEATURES

- GAIN BANDWIDTH PRODUCT(A_V = 5) 100MHz
- HIGH INPUT IMPEDANCE 500MΩ
- LOW INPUT BIAS CURRENT 1nA
- LOW INPUT OFFSET CURRENT 1nA
- LOW INPUT OFFSET VOLTAGE 0.5mV
- HIGH GAIN 150K V/V
- HIGH SLEW RATE 35V/μs
- OUTPUT SHORT CIRCUIT PROTECTION

APPLICATIONS

- VIDEO AND R.F. AMPLIFIERS
- PULSE AMPLIFIER
- AUDIO AMPLIFIERS AND FILTERS
- HIGH-Q ACTIVE FILTERS
- HIGH-SPEED COMPARATORS
- LOW DISTORTION OSCILLATORS

DESCRIPTION

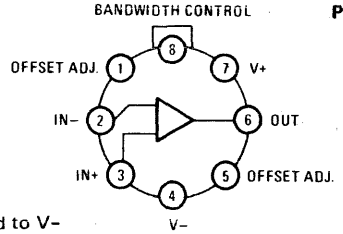
HA-2620/2622/2625 are bipolar operational amplifiers that feature very high input impedance (500MΩ, HA-2620) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2620) and low bias and offset current (1nA, HA-2620) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 100MHz gain-bandwidth product (HA-2620/2622/2625 are stable for closed loop gains greater than 5), 35V/ μs slew rate and 150,000V/V open-loop gain enables HA-2620/2622/2625 to perform high-gain amplification of very fast, wideband signals. These dynamic characterisitcs, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequiency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs HA-2620/2622/2625 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators.

HA-2620 and HA-2622 are guaranteed over -55°C to +125°C. HA-2625 is specified from 0°C to +75°C. All devices are available in TO-99 cans, and 14 lead D.I.P. packages.

PINOUT

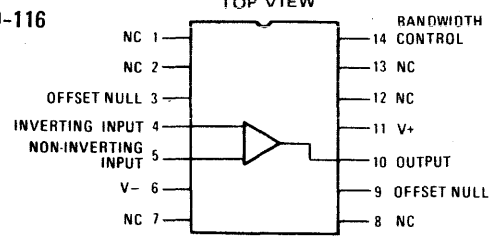
TO-99 TOP VIEW



Package Code 2A

Case Connected to V-

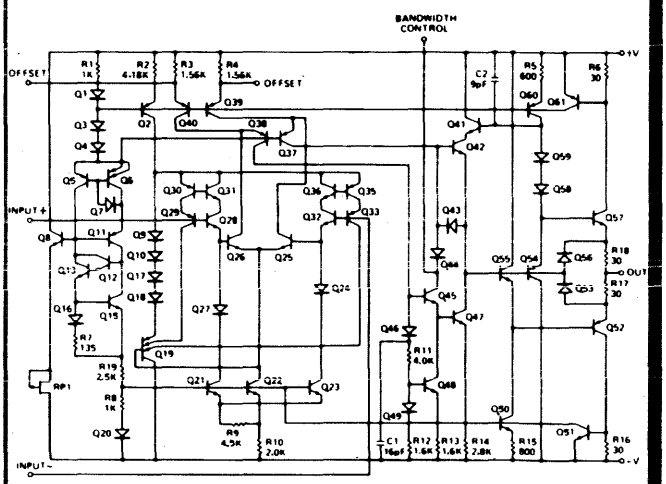
TO-116 TOP VIEW



Package Code 4U

Case Connected to V-

SCHEMATIC



SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

$V^+ = +15$ VDC, $V^- = -15$ VDC

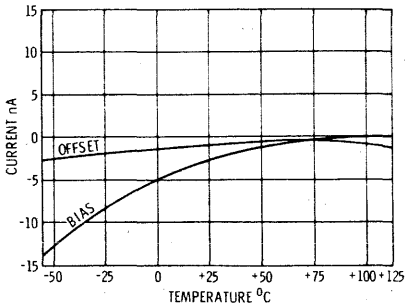
PARAMETER	TEMPERATURE	HA-2620 −55°C to +125°C MIN.	HA-2620 TYP.	HA-2620 MAX.	HA-2622 −55°C to +125°C MIN.	HA-2622 TYP.	HA-2622 MAX.	HA-2625 0°C to +75°C MIN.	HA-2625 TYP.	HA-2625 MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage (Note 1)	+25°C		0.5	4		3	5		3	5	mV
	Full			6			7			7	mV
* Bias Current	+25°C		1	15		5	25		5	25	nA
	Full		10	35			60			40	nA
* Offset Current	+25°C		1	15		5	25		5	25	nA
	Full		5	35			60			40	nA
Input Resistance	+25°C	65	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Notes 2 & 3)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
* Common Mode Rejection Ratio (Note 4)	Full	80	100		74	100		74	100		dB
Gain Bandwidth Product (Notes 2, 5, &6)	+25°C		100			100			100		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 3)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Notes 2, 3 & 7)	+25°C	400	600		320	600		320	600		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 2, 5, 7 & 8)	+25°C		17	45		17	45		17	45	ns
* Slew Rate (Notes 2, 7, 8 & 10)	+25°C	±25	±35		± 20	±35		± 20	±35		V/μs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

NOTES:
1. Offset may be externally adjusted to zero.
2. $R_L = 2K\Omega$, $C_L = 50pF$
3. $V_O = \pm 10.0V$
4. $V_{CM} = \pm 5.0V$
5. $V_O < 90mV$
6. 40dB Gain
7. See transient response test circuits and waveforms page 3.
8. $A_V = 5.0V$ (The HA-2620 family is not stable at unity gain without external compensation.)
9. $V_{Sup} = \pm 9.0V$ to $\pm 15.0V$
10. $V_O = 5.0V$

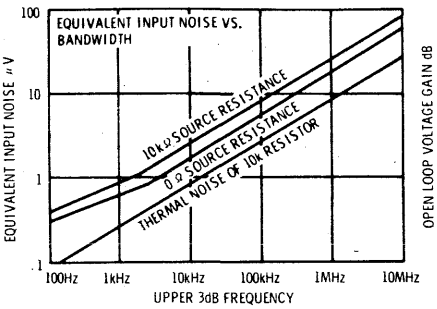
*100% Tested For DASH 8

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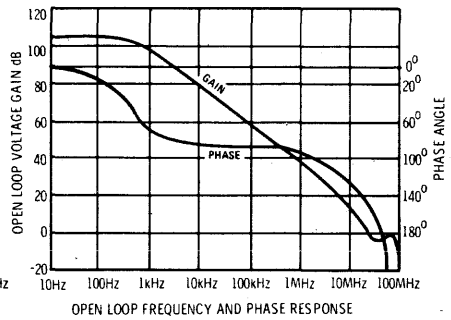
V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.



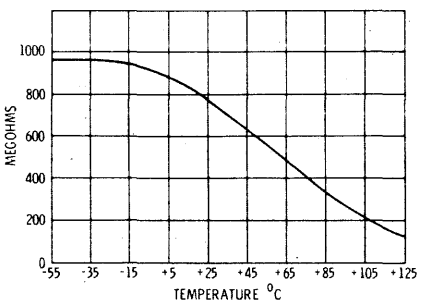
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



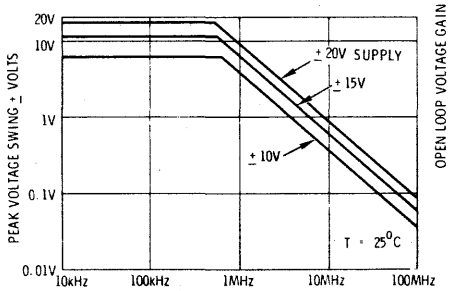
BROADBAND NOISE CHARACTERISTICS



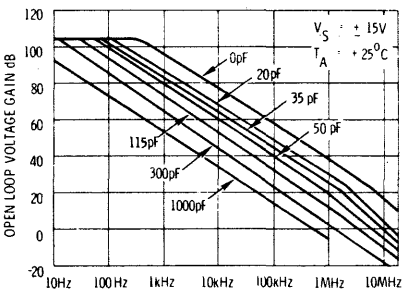
OPEN LOOP FREQUENCY AND PHASE RESPONSE



INPUT IMPEDANCE VS. TEMPERATURE, 100Hz

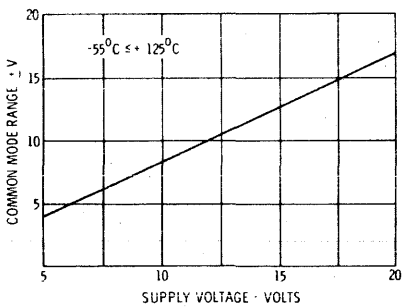


OUTPUT VOLTAGE SWING VS. FREQUENCY

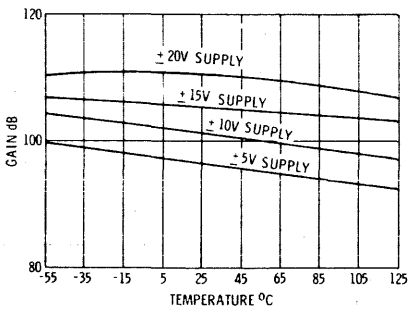


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

Note: External Compensation is Required For Closed Loop Gain <5. If External Compensation is Used, Also Connect 100 pF Capacitor From Output to Ground.

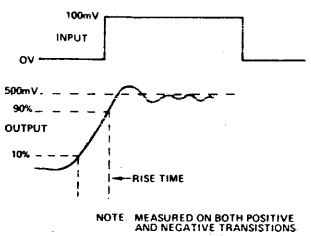


COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



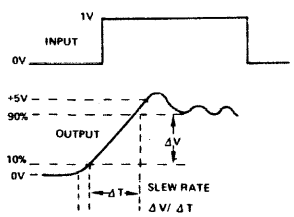
OPEN-LOOP VOLTAGE GAIN VS. TEMPERATURE

TRANSIENT RESPONSE

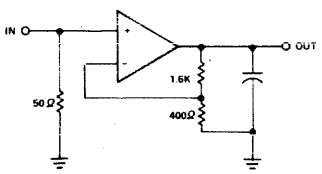


NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSISTIONS.

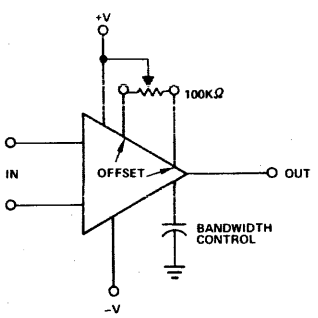
SLEW RATE



SLEW RATE AND TRANSIENT RESPONSE



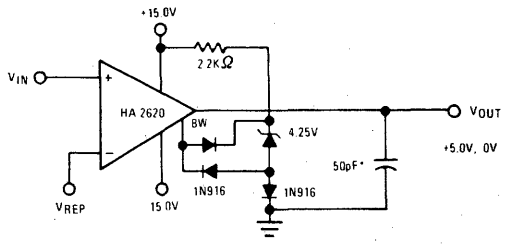
SUGGESTED OFFSET ZERO ADJUST AND BANDWIDTH CONTROL HOOK-UP



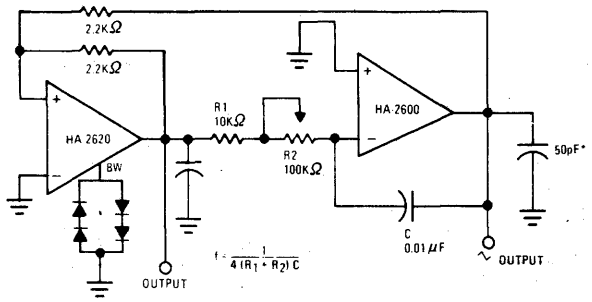
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TYPICAL APPLICATIONS

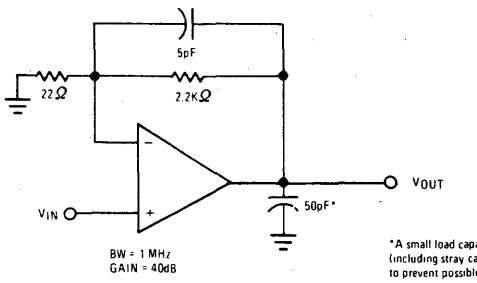
HIGH IMPEDANCE COMPARATOR



FUNCTION GENERATOR



VIDEO AMPLIFIER



*A small load capacitance of at least 30pF (including stray capacitance) is recommended to prevent possible high frequency oscillations.

DEFINITIONS

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT—The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE—The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE—The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO—The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING—The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE—The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE—The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN—The ratio of the change in output voltage to the change in input voltage producing it.

UNITY GAIN BANDWIDTH—The frequency at which the voltage gain of the amplifier is unity.

POWER SUPPLY REJECTION RATIO—The ratio of the change in input offset voltage to the change in power supply voltage producing it.

TRANSIENT RESPONSE—The closed loop step function response of the amplifier under small signal conditions.

GAIN BANDWIDTH PRODUCT—The product of the gain and the bandwidth at a given gain.

SLEW RATE (Rate Limiting)—The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing)...restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2630/2635

High Performance Current Booster

FEATURES

- OUTPUT CURRENT ±400mA
- SLEW RATE 500V/μs
- BANDWIDTH 8MHz
- FULL POWER BANDWIDTH 8MHz
- INPUT RESISTANCE $2.0 \times 10^6 \Omega$
- OUTPUT RESISTANCE 2.0Ω
- POWER SUPPLY RANGE ±5V to ±20V
- PACKAGE IS ELECTRICALLY ISOLATED

APPLICATIONS

- COAXIAL CABLE DRIVERS
- AUDIO OUTPUT AMPLIFIERS
- SERVO MOTOR DRIVERS
- POWER SUPPLIES (BIPOLAR)
- PRECISION DATA RECORDING

DESCRIPTION

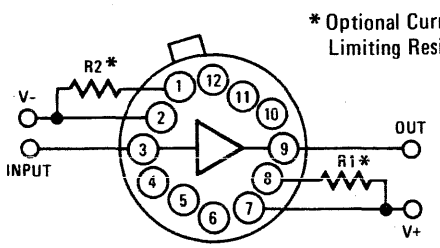
HA-2630 and HA-2635 are monolithic, unity voltage gain current amplifiers delivering extremely high slew rate, wide bandwidth, and full power bandwidth even under heavy output loading conditions. This dielectrically isolated current booster also offers high input impedance and low output resistance. These devices are intended to be used in series with an operational amplifier and inside the feedback loop whenever additional output current is required. Output current levels are programmable by selecting two optional external resistors.

These current amplifiers offer an exceptional 500V/μs slew rate and 8MHz bandwidth which allows them to be used with many high performance op amps in precision data recording and high speed coaxial cable driver designs. 2.0M ohm input resistance and 2 ohm output resistance coupled with ±400mA output current make HA-2630 and HA-2635 ideal components in high fidelity audio output amplifier designs.

HA-2630 and HA-2635 are available in an electrically isolated TO-8 type can for ease of mounting with or without a heat sink. HA-2630 is specified over the -55°C to +125°C range. HA-2635 is specified from 0°C to +75°C.

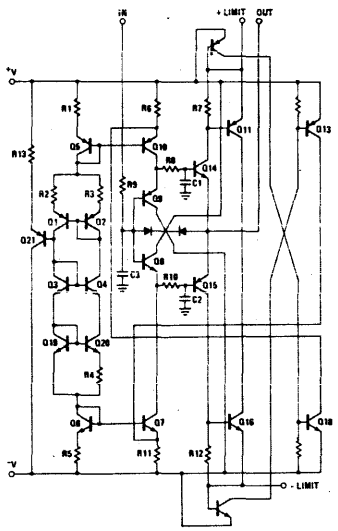
PINOUT

TO-8 **Package Code 2G**



Top View

SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V
Input Voltage Range	± V Supply
Output Current (Note 2)	±700mA
Internal Power Dissipation (Note 6) Free Air:	1W
In Heat Sink:	4W

Operating Temperature Range:
$-55^{o}C \leq T_A \leq +125^{o}C$ (HA-2630)
$0^{o}C \leq T_A \leq +75^{o}C$ (HA-2635)
Storage Temperature Range:
$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

$V_{Supply} = \pm 15$ Volts $R_L = 50$ Ohms $R_1 = R_2 = 0$ Ohms Unless otherwise specified.

PARAMETER	TEMP.	HA-2630 -55°C to +125°C MIN.	HA-2630 TYP.	HA-2630 MAX.	HA-2635 0°C to +75°C MIN.	HA-2635 TYP.	HA-2635 MAX.	UNITS
INPUT CHARACTERISTICS								
*Bias Current	+25°C		30	150		30	150	µA
	Full			200			200	µA
Input Resistance	+25°C		2.0			2.0		MΩ
Input Capacitance	+25°C		5.0			5.0		pF
TRANSFER CHARACTERISTICS								
Voltage Gain (Note 1)	Full	.85	.95		.85	.95		V/V
*Offset Voltage ($V_{OUT} - V_{IN}$)	+25°C		70	±200		70	±200	mV
	Full			±300			±300	mV
Bandwidth (-3dB)	+25°C		8.0			8.0		MHz
OUTPUT CHARACTERISTICS								
*Output Voltage Swing	Full	±10			±10			V
*Output Current (Note 1)	Full	±300	±400		±300	±400		mA
Output Resistance	+25°C		2.0			2.0		Ω
Full Power Bandwidth (Note 1)	+25°C		8.0			8.0		MHz
TRANSIENT RESPONSE								
Rise Time (Note 3)	+25°C		30			30		ns
Slew Rate (Note 4)	+25°C	200	500		200	500		V/µs
POWER SUPPLY CHARACTERISTICS								
*Supply Current	Full		15	20		15	23	mA
Supply Voltage Range	Full	±5		±20	±5		±20	V
Power Supply Rejection Ratio (Note 5)	Full		66			66		dB

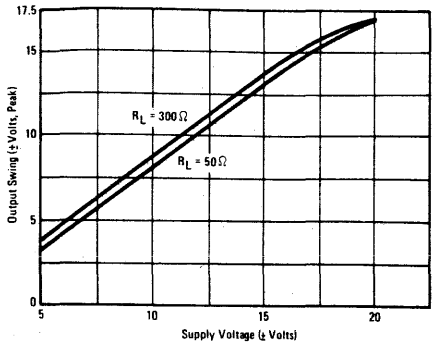
NOTES:
1. $V_O = \pm 10V$
2. Heat sink is required for continuous short circuit protection, regardless of current limit setting.
3. $V_O = 0.4V$ p-p.
4. $V_O = 10V$ p-p.
5. $\Delta V_{SUPPLY} = \pm 5V$.
6. Without heat sink, derate by 14mW/°C ambient temperature above 100°C ambient, with heat sink, derate by 67mW/°C case temperature above 115°C case.

*100% Tested For DASH 8

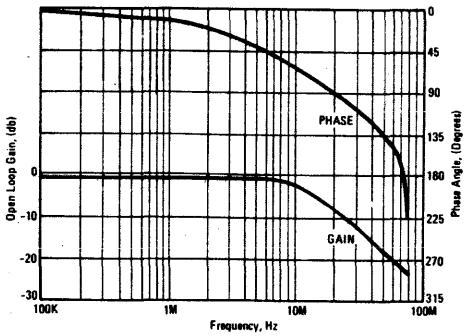
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V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

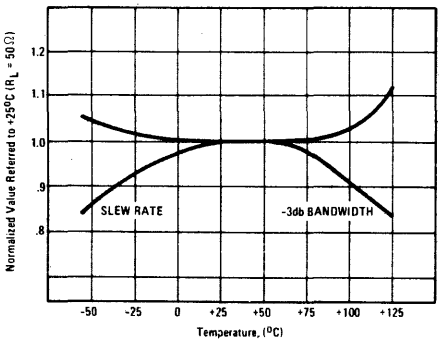
OUTPUT SWING (R_{LIMIT} = 0Ω)



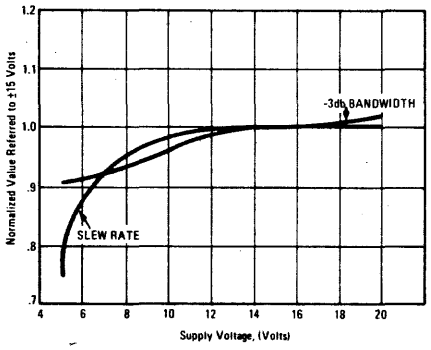
OPEN LOOP FREQUENCY AND PHASE RESPONSE (R_L = 50Ω, C_L ≈10pf)



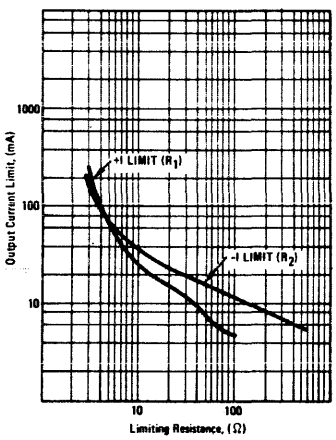
NORMALIZED AC PARAMETERS vs. TEMPERATURE (R_L = 50Ω)



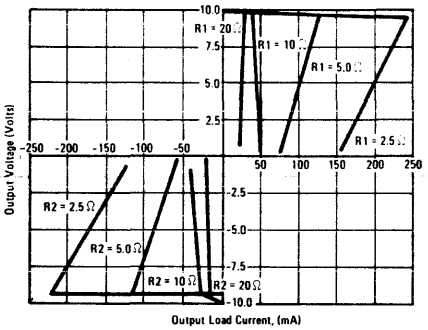
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE (R_L = 50Ω)



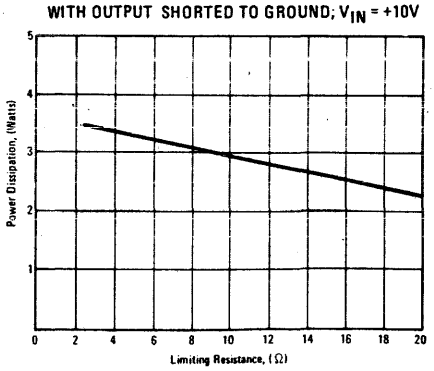
OUTPUT CURRENT LIMITING vs. LIMITING RESISTANCE



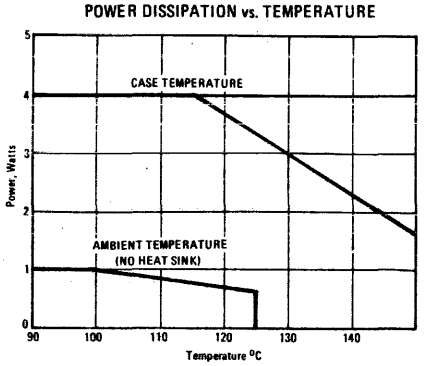
OUTPUT CURRENT CHARACTERISTIC



POWER DISSIPATION vs. LIMITING RESISTANCE WITH OUTPUT SHORTED TO GROUND; V_{IN} = +10V



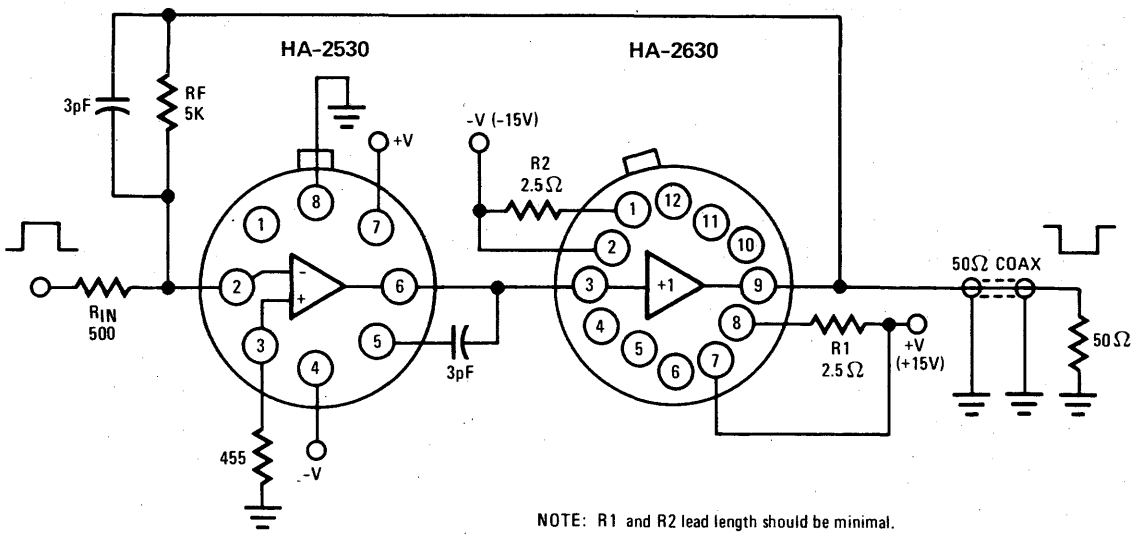
MAXIMUM ALLOWABLE INTERNAL POWER DISSIPATION vs. TEMPERATURE



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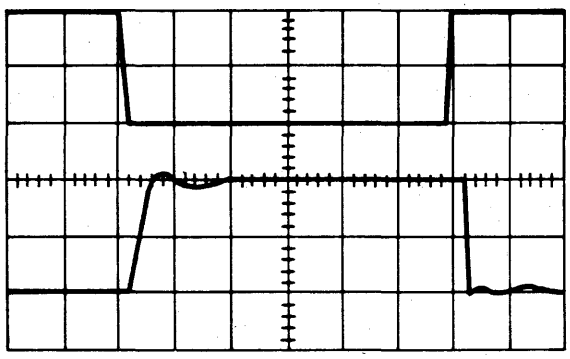
TYPICAL APPLICATION

20db, 5MHz VIDEO COAXIAL LINE DRIVER



NOTE: R1 and R2 lead length should be minimal.

LINE DRIVER PULSE RESPONSE



Horizontal Scale = 200ns/Div.
Upper Trace: Input, 200mV/Div.
Lower Trace: Output, 2V/Div.

SOME OTHER APPLICATIONS

- BIPOLAR POWER SUPPLY
- FUNCTION GENERATOR OUTPUT
- DEFLECTION COIL DRIVE
- AUDIO OUTPUT AMPLIFIER

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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2640/2645

High Voltage Operational Amplifier

FEATURES

- OUTPUT VOLTAGE SWING ±35V
- SUPPLY VOLTAGE ±10V TO ±40V
- OFFSET CURRENT 5nA
- BANDWIDTH 4MHz
- SLEW RATE 5V/μs
- COMMON MODE INPUT VOLTAGE SWING ±35V
- OUTPUT OVERLOAD PROTECTION

APPLICATIONS

- INDUSTRIAL CONTROL SYSTEMS
- POWER SUPPLIES
- HIGH VOLTAGE REGULATORS
- RESOLVER EXCITATION
- SIGNAL CONDITIONING

DESCRIPTION

HA-2640 and HA-2645 are monolithic operational amplifiers which are designed to deliver unprecedented dynamic specifications for a high voltage internally compensated device. These dielectrically isolated devices offer very low values for offset voltage and offset current coupled with large output voltage swing and common mode input voltage.

For maximum reliability, these amplifiers offer unconditional output overload protection through current limiting and a chip temperature sensing circuit. This sensing device turns the amplifier "off", when the chip reaches a certain temperature level.

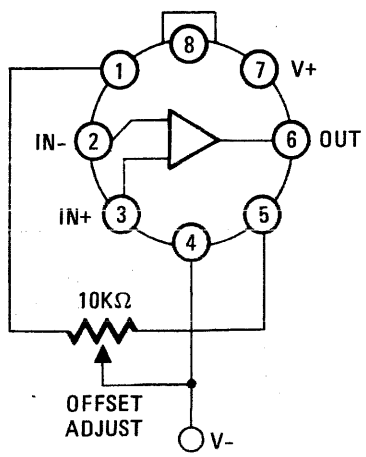
These amplifers deliver ±35V common mode input voltage swing, ±35V output voltage swing, and up to ±40V supply range for use in such designs as regulators, power supplies, and industrial control systems. 4MHz gain bandwidth and 5V/μs slew rate make these devices excellent components for high performance signal conditioning applications. Outstanding input and output voltage swings coupled with a low 5nA offset current make these amplifiers excellent components for resolver excitation designs.

HA-2640 and HA-2645 are available in metal can (TO-99) packages and can be used as high performance pin-to-pin replacements for many general purpose op amps. HA-2640 is specified from -55°C to +125°C and HA-2645 is specified over the 0°C to +75°C range.

PINOUT

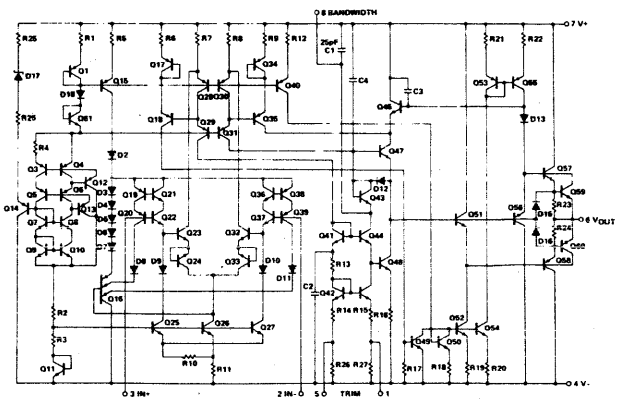
TO-99 **Package Code 2A**

Top View



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SCHEMATIC



SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals 100V
Input Voltage Range ±37V
Output Current/Full Short Circuit Protection
Internal Power Dissipation 680mW*

*Derate by 4.6mW/°C above +25°C

Operating Temperature Range
$-55^{\circ}C \leq T_A \leq +125^{\circ}C$ (HA-2640)
$0^{\circ}C \leq T_A \leq +75^{\circ}C$ (HA-2645)
Storage Temperature Range
$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

ELECTRICAL CHARACTERISTICS

$V_{Supply} = \pm 40V$, $R_L = 5K$, Unless Otherwise Specified.

PARAMETER	TEMP.	HA-2640 -55°C to +125°C MIN.	HA-2640 -55°C to +125°C TYP.	HA-2640 -55°C to +125°C MAX.	HA-2645 0°C to +75°C MIN.	HA-2645 0°C to +75°C TYP.	HA-2645 0°C to +75°C MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		2	4		2	6	mV
	Full			6			7	mV
Offset Voltage Average Drift	Full		15			15		µV/°C
* Bias Current	+25°C		10	25		12	30	nA
	Full			50			50	nA
* Offset Current	+25°C		5	12		15	30	nA
	Full			35			50	nA
Input Resistance	+25°C	50	250		40	200		MΩ
Common Mode Range	Full	±35			±35			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 8)	+25°C	100K	200K		100K	200K		V/V
	Full	75K			75K			V/V
* Common Mode Rejection Ratio (Note 1)	Full	80	100		74	100		dB
Unity Gain Bandwidth (Note 2)	+25°C		4			4		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing	Full	±35			±35			V
* Output Current (Note 9)	+25°C	±12	±15		±10	±12		mA
Output Resistance	+25°C		500			500		Ω
Full Power Bandwidth (Note 3)	+25°C		23			23		kHz
TRANSIENT RESPONSE (Note 7)								
Rise Time (Notes 4, 6)	+25°C		60			60		ns
Overshoot (Notes 4, 6)	+25°C		15			15		%
Slew Rate (Note 6)	+25°C		5			5		V/µs
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		3.2	3.8		3.2	4.5	mA
Supply Voltage Range	Full	±10		±40	±10		±40	V
* Power Supply Rejection Ratio (Note 5)	Full	80	90		74	90		dB

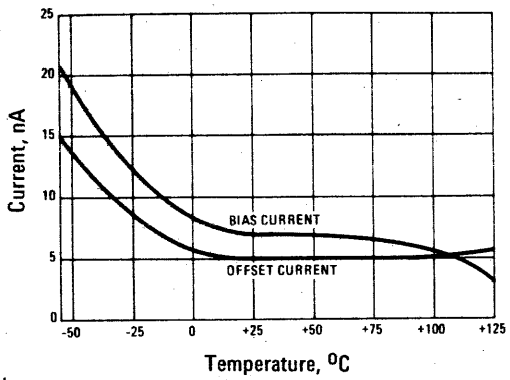
*100% Tested For DASH 8

NOTES: 1. $V_{CM} = \pm 30V$
2. $V_O = 90mV$
3. $V_O = \pm 35V$
4. $V_O = \pm 200mV$
5. $V_S = \pm 10V$ to $\pm 40V$
6. $A_V = 1$
7. $C_L = 50pF$
8. $\Delta V_O =$
9. $R_L = 1K\Omega$

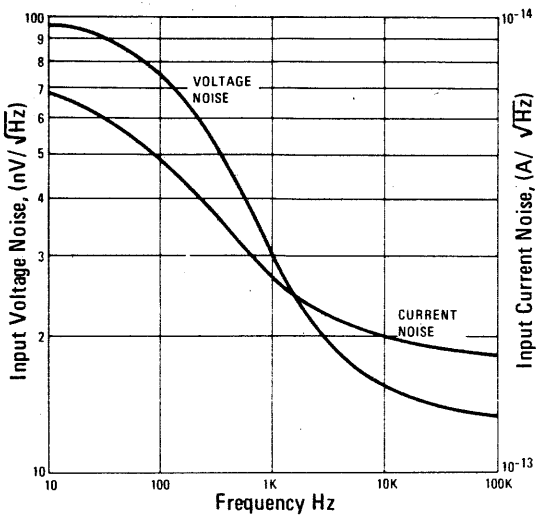
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V+ = V- = 40VDC, T_A = +25°C UNLESS OTHERWISE STATED

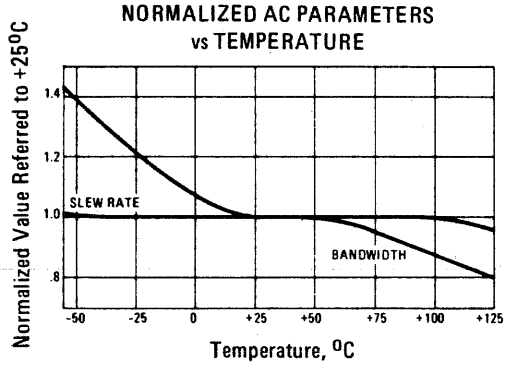
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



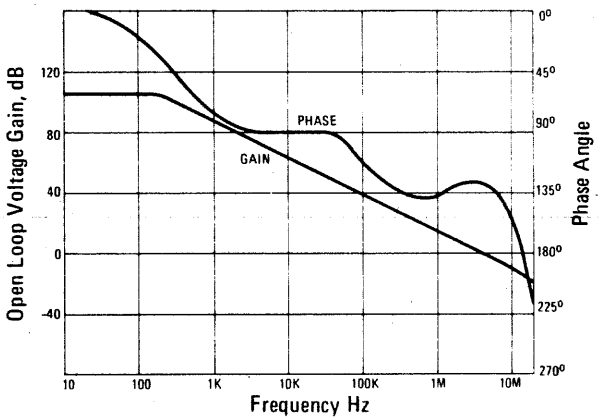
INPUT NOISE CHARACTERISTICS



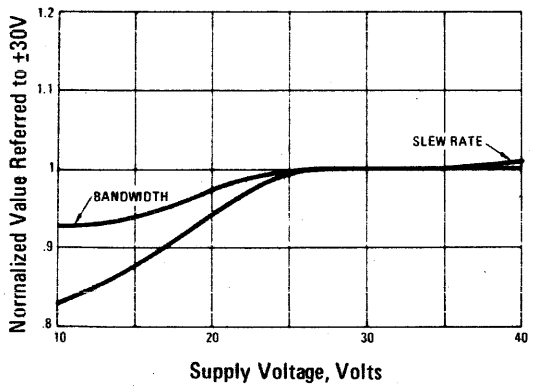
NORMALIZED AC PARAMETERS vs TEMPERATURE



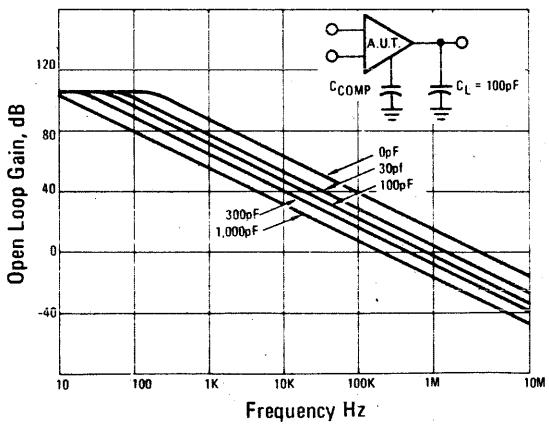
OPEN LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C



OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

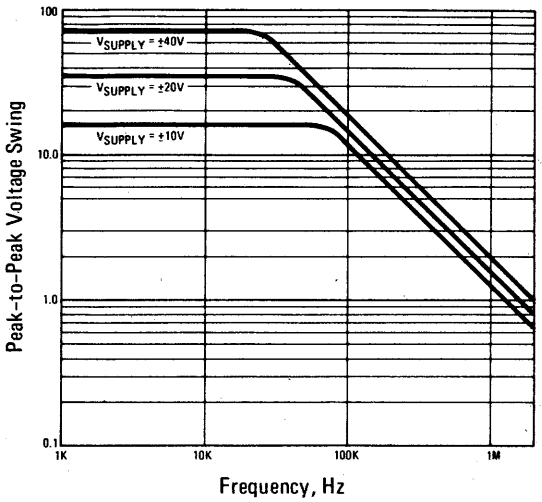


NOTE: External Compensation Components are not Required for Stability. But May be Added to Reduce Bandwidth if Desided. C_L = 100pF is Also Required for Stability Only if External Compensation Capacitor is Used.

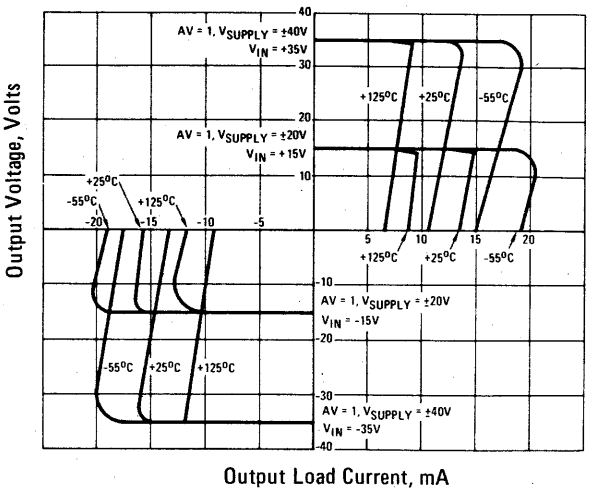
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PERFORMANCE CURVES (continued)

OUTPUT VOLTAGE SWING
vs FREQUENCY AT +25°C

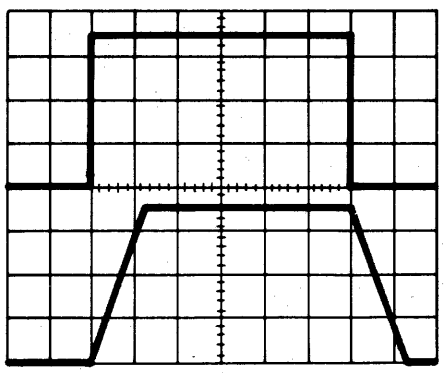


OUTPUT CURRENT CHARACTERISTIC



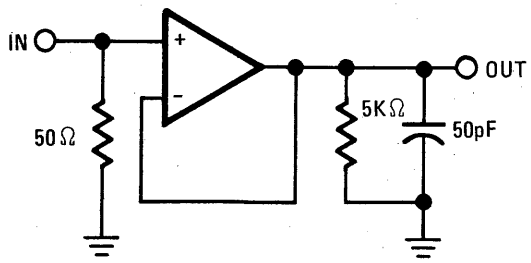
SWITCHING WAVEFORM AND TEST CIRCUIT

VOLTAGE FOLLOWER
PULSE RESPONSE



R_L = 5K, C_L = 50pF
Vertical = 10V/Div. T_A = +25°C
Horizontal = 5µs/Div. V_S = ±40V

SLEW RATE AND TRANSIENT
RESPONSE TEST CIRCUIT



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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2650/2655

Dual High Performance Operational Amplifier

FEATURES

- SLEW RATE — 5V/μs
- BANDWIDTH — 8MHz
- BIAS CURRENT — 35nA
- AV. OFFSET VOLTAGE DRIFT — 8μV/°C
- POWER CONSUMPTION — 75mW
- SUPPLY VOLTAGE RANGE — ±2V TO ±20V

APPLICATIONS

- VIDEO AMPLIFIERS
- HIGH IMPEDANCE, WIDEBAND BUFFERS
- INTEGRATORS
- AUDIO AMPLIFIERS
- ACTIVE FILTERS

DESCRIPTION

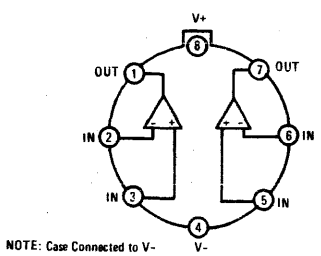
HA-2650/2655 contains two internally compensated operational amplifiers offering high slew rate and high frequency performance combined with exceptional DC characteristics. 5V/μ sec slew rate and 8MHz bandwidth make these amplifiers suitable for processing fast, wideband signals extending into the video frequency spectrum. Signal processing accuracy is enhanced by front-end performance that includes 1.5mV offset voltage, 8 μ V/°C offset voltage drift and low offset and bias current (1nA and 35nA respectively). Offset voltage can be trimmed to zero on the devices offered in dual-in-line packages. Signal conditioning is further enhanced by 500MΩ input impedance.

Applications for HA-2650/2655 include video circuit designs such as high impedance buffers, integrators, tone generators and filters. These amplifiers are also ideal components for active filtering of audio and voice signals.

HA-2650/2655 are offered in 14 pin D.I.P. and metal TO-99 packages and are also available in dice form. HA-2650 is specified from -55°C to +125°C. HA-2655 operates from 0°C to +75°C.

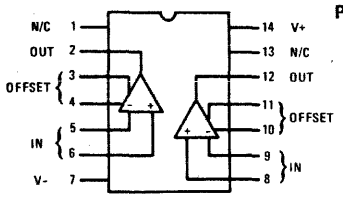
PINOUT

TO-99 — TOP VIEW — Package Code 2A



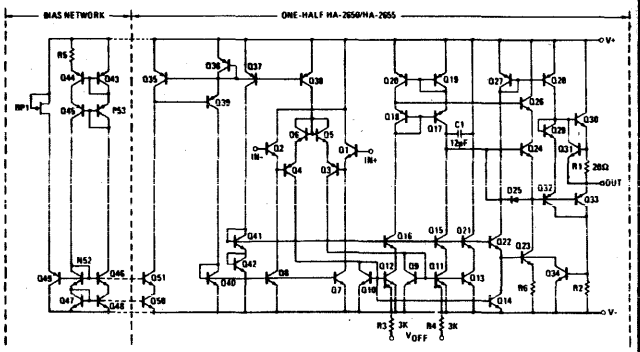
NOTE: Case Connected to V-

TO-116 — TOP VIEW — Package Code 4U



NOTE: Bottom of package is connected to V-.

SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
Output Short Circuit Duration	Indefinite

Power Dissipation (Note 2)	TO-99	300 mW
	TO-116	300 mW
Operating Temperature Range:		
HA-2650		$-55^oC \leq T_A \leq +125^oC$
HA-2655		$0^oC \leq T_A \leq +75^oC$
Storage Temperature Range		$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

V+ = 15V V- = -15V

PARAMETER	TEMP.	HA-2650 -55°C to +125°C MIN.	TYP.	MAX.	HA-2655 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
*Offset Voltage	+25°C		1.5	3		2	5	mV
	Full			5			7	mV
Av. Offset Voltage Drift	Full		8			8		µV/°C
*Bias Current	+25°C		35	100		50	200	nA
	Full			200			300	nA
*Offset Current	+25°C		1	30		2	60	nA
	Full			60			100	nA
Common Mode Range	Full	±13			±13			V
Differential Input Resistance	+25°C	5	20		5	20		MΩ
Common Mode Input Resistance	+25°C		500			500		MΩ
Input Capacitance	+25°C		5			5		pF
TRANSFER CHARACTERISTICS								
*Large Signal Voltage Gain (Note 3ab)	+25°C	25K	40K		20K	40K		V/V
	Full	20K			15K			V/V
*Common Mode Rejection Ratio (Note 4)	+25°C	80	100		74	100		dB
	Full	80			74			dB
OUTPUT CHARACTERISTICS								
*Output Voltage Swing (Note 3c)	+25°C	±13	±14		±13	±14		V
	Full	±13			±13			V
Full Power Bandwidth (Note 5)	+25°C	30	80		30	80		KHz
Output Current (Note 3a)	+25°C		±20			±18		mA
Output Resistance	+25°C		100			100		Ω
TRANSIENT RESPONSE (Note 6)								
Rise Time (Note 7)	+25°C		40			40		ns
Overshoot (Note 7)	+25°C		15			15		%
Slew Rate	+25°C	±2	±5		±2	±5		V/µs
POWER SUPPLY CHARACTERISTICS								
*Supply Current	+25°C		2.5	3		3	4	mA
*Power Supply Rejection Ratio (Note 8)	+25°C	80	100		74	100		dB
	Full	80			74			dB

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Derate at 4.7mW/°C at ambient temperatures above +110°C.
3. (a) V_O = ±10V (b) R_L = 2K (c) R_L = 10K
4. V_{CM} = ±5.0V
5. A_V = 1, R_L = 2K, V_O = $20V_{pp}$
6. See transient response/slew rate circuit.
7. V_{in} = 200mV
8. Δ V = ±5.0V

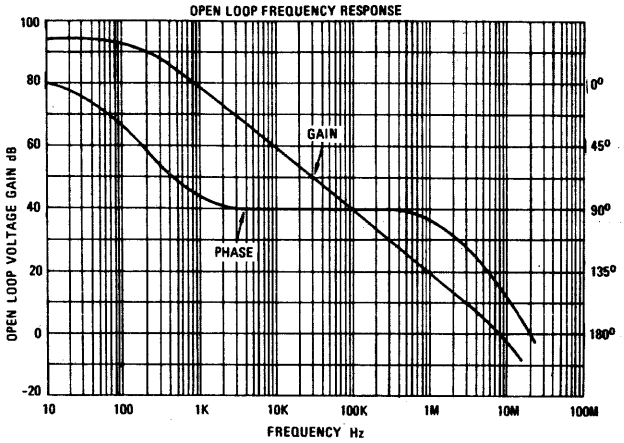
*100% Tested For DASH 8

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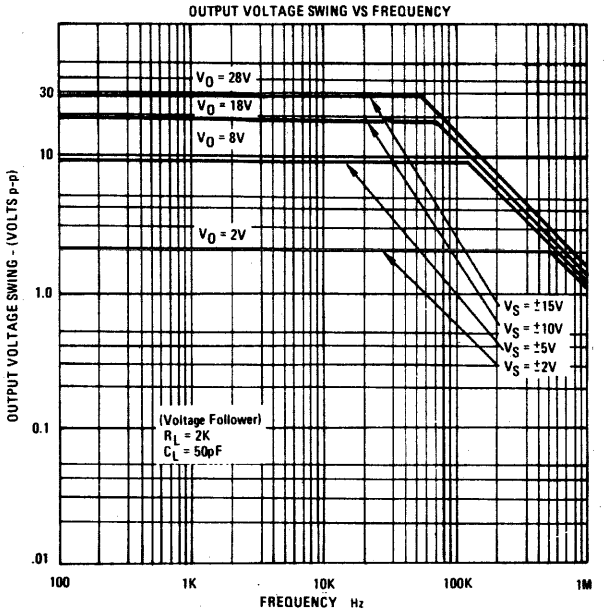
PERFORMANCE CURVES

V+ = +15V, V- = -15V, T_A = +25°C Unless Otherwise Stated.

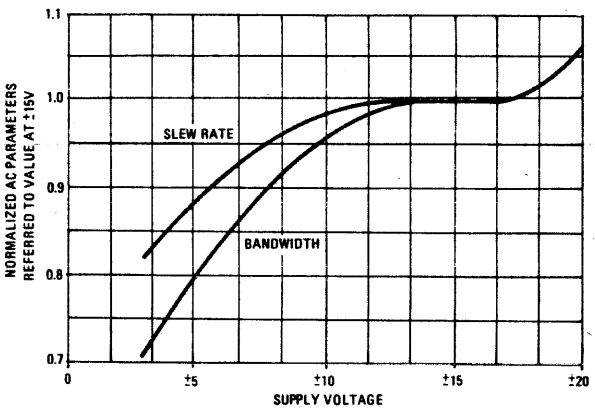
OPEN LOOP FREQUENCY RESPONSE



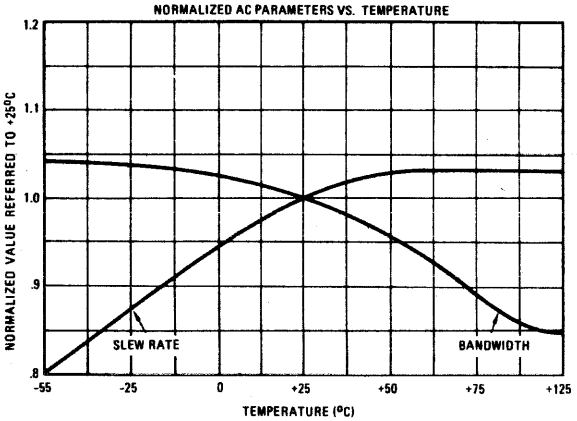
OUTPUT VOLTAGE SWING VS FREQUENCY



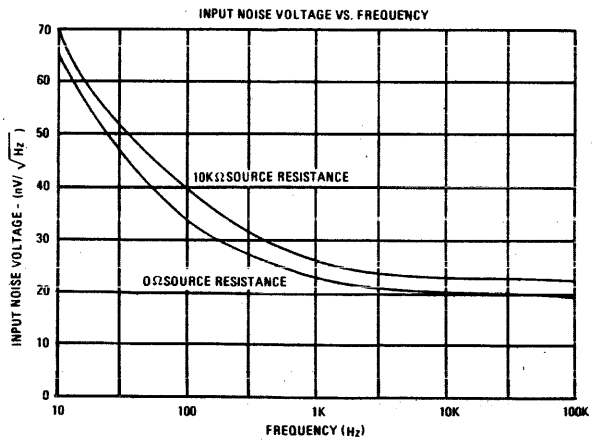
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



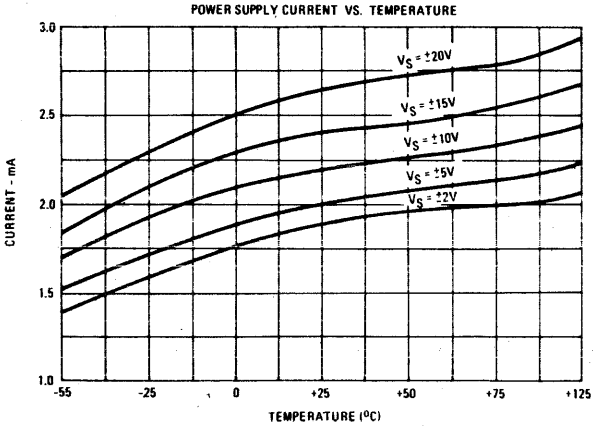
NORMALIZED AC PARAMETERS VS. TEMPERATURE



INPUT NOISE VOLTAGE VS. FREQUENCY



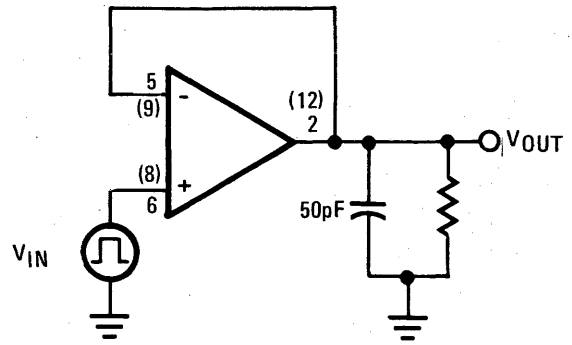
POWER SUPPLY CURRENT VS. TEMPERATURE



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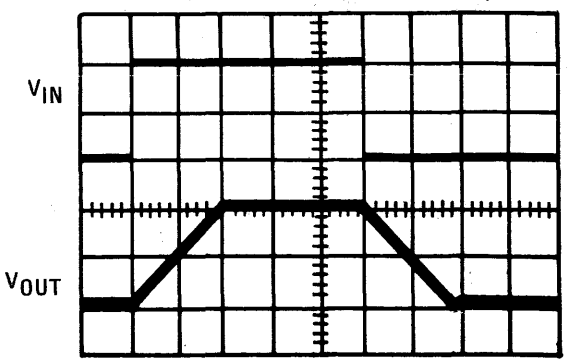
PERFORMANCE CHARACTERISTICS

TRANSIENT RESPONSE/SLEW RATE CIRCUIT



Note: Numbers in parentheses refer to the second half of TO-116 package.

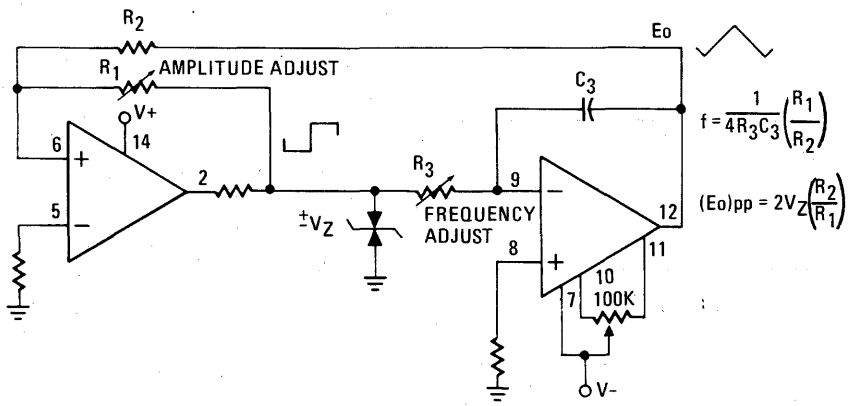
SLEWING WAVEFORM



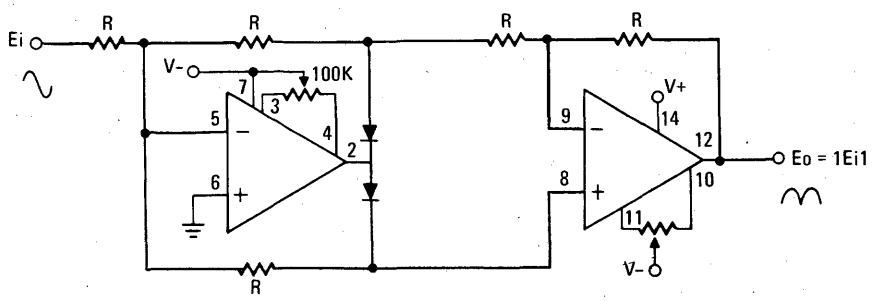
VERTICAL 5V/DIV. HORIZONTAL 1 μs/DIV.

TYPICAL APPLICATIONS

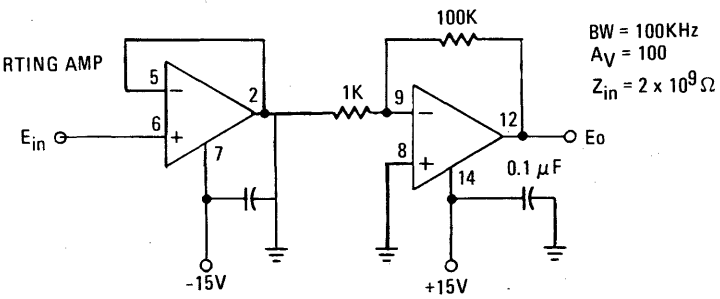
LOW COST HIGH FREQUENCY GENERATOR



ABSOLUTE-VALUE CIRCUIT



HIGH IMPEDANCE
HIGH GAIN
HIGH FREQUENCY INVERTING AMP



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2700/2704/2705

Low Power, High Performance Operational Amplifiers

FEATURES

- LOW POWER DISSIPATION — 2.24mW AT ±15.0V
- HIGH SLEW RATE — 20V/μs
- HIGH OPEN LOOP GAIN — 300K(R_L = 2KΩ)
- LOW INPUT BIAS CURRENT — 5nA
- LOW OFFSET VOLTAGE — 0.5mV
- HIGH CM_{rr} — 106dB
- WIDE POWER SUPPLY RANGE — ±5.5V TO ±20.0V

APPLICATIONS

- HIGH GAIN AMPLIFIER
- INSTRUMENTATION AMPLIFIERS
- ACTIVE FILTERS
- TELEMETRY SYSTEMS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

HA-2700/2704/2705 are internally compensated operational amplifiers which employ dielectric isolation to achieve excellent DC and dynamic performance with very low quiescent power consumption.

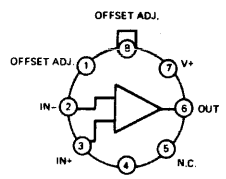
DC performance of the amplifier input is characterized by high CMRR (106dB), low offset voltage (0.5mV, HA-2700 and HA-2704; 1mV, HA-2705) along with low bias and offset current (5.0nA and 2.5nA respectively). These input specifications, in conjunction with offset null capability and open-loop gain of 300,000V/V, enable HA-2700/2704/2705 to provide accurate, high-gain signal amplification. Gain bandwidth 1MHz and slew rate of 20V/μs allow for processing of fast, wideband signals. Input and output signal amplitudes of at least ±11 volts can be accomodated while providing output drive capability of 10mA. For maximum reliability, the output is protected in the event of short circuits to ground.

These amplifiers operate from a wide range of supplies (±5.5V to ±20V) with a maximum quiescent supply drain of only 150μA. HA-2700/2704/2705 are, therefore, ideally suited to low-power instrumentation and filtering applications that require fast, accurate response over a wide range of signal frequency.

These amplifers are available in three performance grades: HA-2700 is rated for operation from -55°C to +125°C; HA-2704 is specified over -25°C to +85°C; HA-2705 is specified from 0°C to +75°C. All three devices are available in TO-99 cans or 14 lead D.I.P. packages.

PINOUT

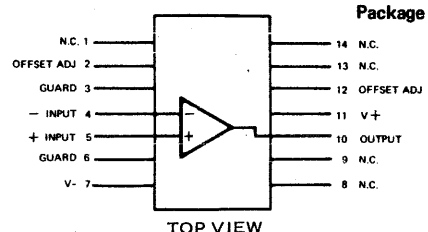
TO-99 — **Package Code 2A**



Case Connected to V-

TOP VIEW

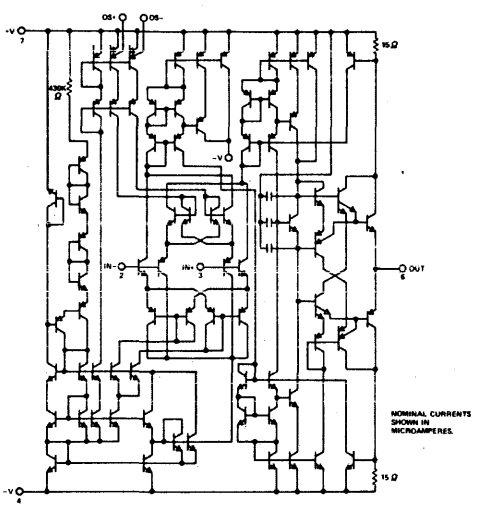
TO-116 — **Package Code 4U**



Case Connected to V-

TOP VIEW

SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	44.0V
Differential Input Voltage	±18.0V
Internal Power Dissipation (Note 7)	300mW
Storage Temperature	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

$V^+ = +15.0$ V.D.C. $V^- = -15.0$ V.D.C.

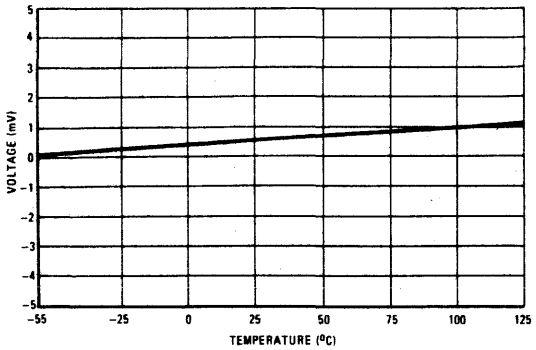
PARAMETER	TEMP.	HA-2700 −55°C to +125°C MIN.	HA-2700 TYP.	HA-2700 MAX.	HA-2704 −25°C to +85°C MIN.	HA-2704 TYP.	HA-2704 MAX.	HA-2705 0°C to +75°C MIN.	HA-2705 TYP.	HA-2705 MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage (Note 1)	+25°C		0.5	3.0		0.5	3.0		1.0	5.0	mV
	Full			5.0			6.0			7.0	mV
* Bias Current	+25°C		5.0	20.0		5.0	20.0		5.0	40.0	nA
	Full			50.0			50.0			70.0	nA
* Offset Current	+25°C		2.5	10.0		2.5	10.0		2.5	15.0	nA
	Full			30.0			30.0			40.0	nA
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Notes 2 & 3)	+25°C	200K	300K		200K	300K		200K	300K		V/V
	Full	100K			100K			100K			V/V
* Common Mode Rejection Ratio (Note 4)	Full	86	106		86	106		80	106		dB
Gain Bandwidth Product (Note 2)	+25°C		1.0			1.0			1.0		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	+25°C	±12.0	±13.0		±12.0	±13.0		±12.0	±13.0		V
	Full	±11.0			±11.0			±11.0			V
Output Current (Note 3)	+25°C		10			10			10		mA
TRANSIENT RESPONSE CHARACTERISTICS											
* Slew Rate (Notes 2 & 6)	+25°C	10	20		10	20		10	20		V/µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		75	150		75	150		75	150	µA
* Power Supply Rejection Ratio (Note 5)	Full	86	100		86	100		80	100		dB

NOTES:
1. Can be adjusted to zero with 1 megohm pot between Pins 1 and 8 with the tap to Pin 7.
2. $R_L = 2K$, $C_L = 100pF$
3. $V_O = \pm 10.0V$
4. $V_{CM} = \pm 5.0V$
5. $V_S = \pm 10.0V$ to $\pm 20.0V$
6. $A_V = 5$
7. Derate by 6.6 mW/°C above 105°C.

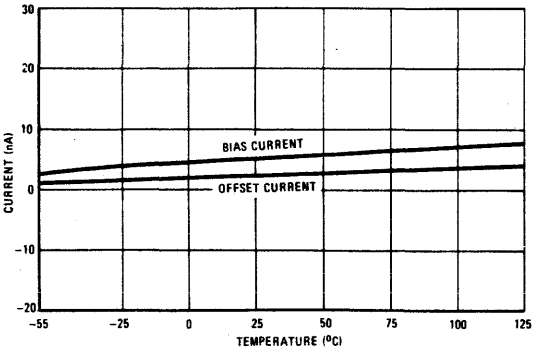
*100% Tested For DASH 8

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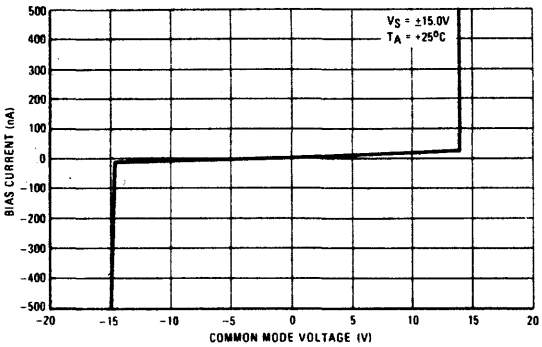
OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



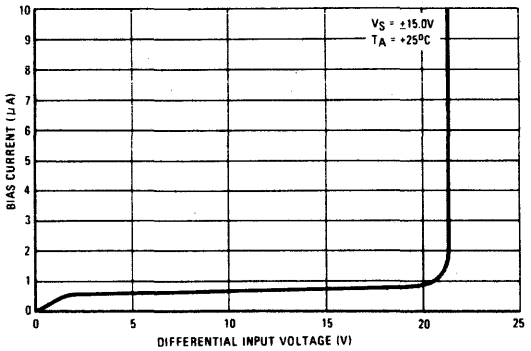
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



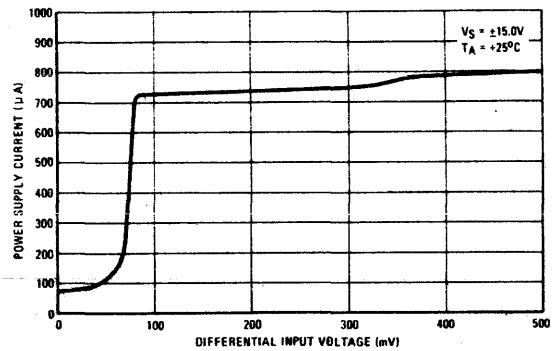
BIAS CURRENT AS A FUNCTION OF COMMON MODE VOLTAGE



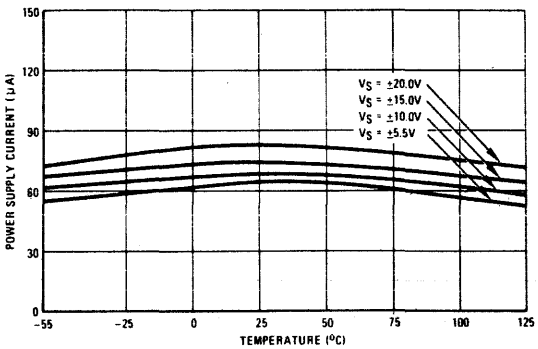
BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



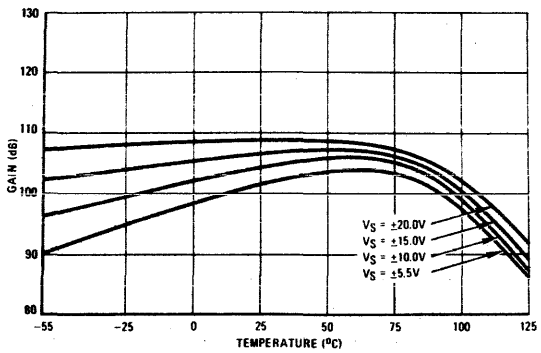
POWER SUPPLY CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



POWER SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE

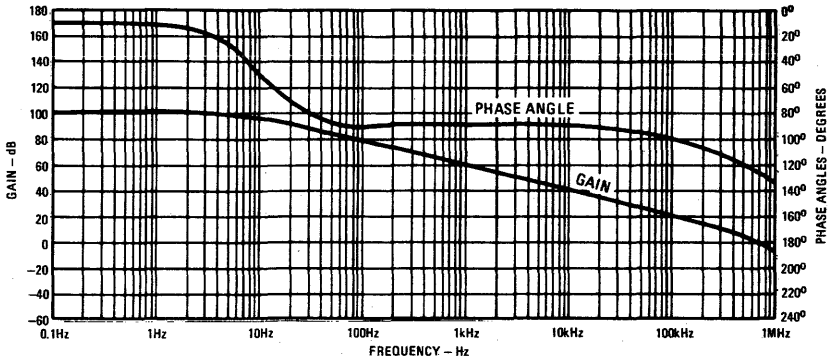


NOTE: Open loop (comparator) applications are not recommended, because of the above characteristic.

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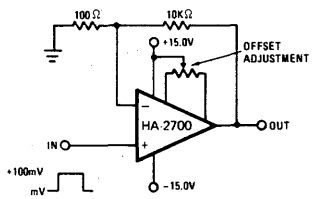
TYPICAL PERFORMANCE CURVES (continued)

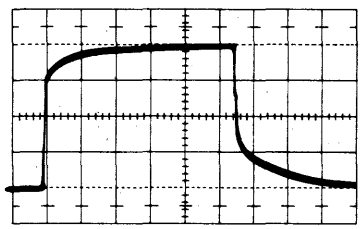
PHASE-FREQUENCY RESPONSE FOR THE HA-2700



TYPICAL APPLICATIONS

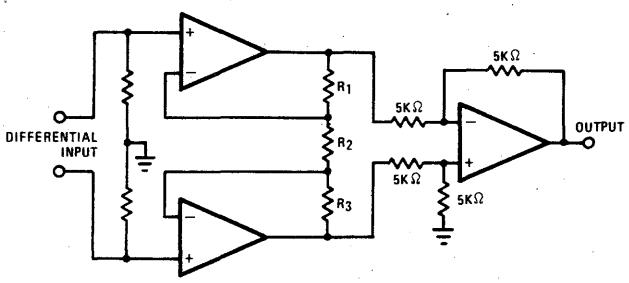
HIGH GAIN AMPLIFIER (100 V/V)





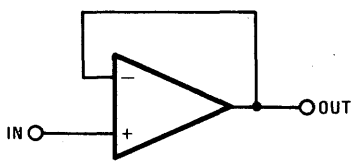
SCALE:
Horizontal – 20μs/division
Vertical – 5.0V/division

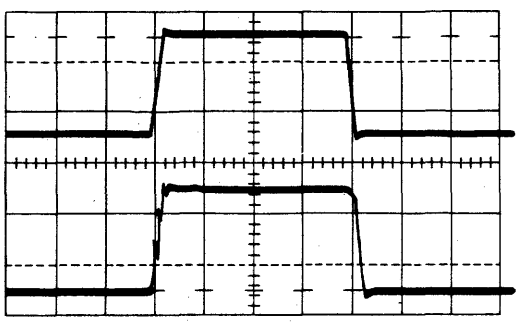
DIFFERENTIAL INPUT INSTRUMENTATION AMPLIFIER



THE GAIN IS GIVEN BY: $\frac{(R_1 + R_2 + R_3)}{R_2} = G$

UNITY GAIN VOLTAGE FOLLOWER





Non-inverting unity gain with a 2KΩ and 100pF load
TOP: V_{IN} = 10.0V Peak to Peak
BOTTOM: V_{OUT}
SCALE: Horizontal -1 μs/division
Vertical -5.0V/division

NOTE: Faster increase rise and fall time and increase distortion on output wave form.

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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2720/25

Wide Range Programmable Operational Amplifier

FEATURES

- WIDE PROGRAMMING RANGE

SLEW RATE	0.06 TO 6V/μs
BANDWIDTH	5kHz TO 10MHz
BIAS CURRENT	0.4 TO 50nA
SUPPLY CURRENT	1μA TO 1.5mA

- WIDE POWER SUPPLY RANGE ±1.2 TO ±18V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

HA-2720/2725 programmable amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. This versatile adjustment capability enables HA-2720/2725 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2720 and HA-2725 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting their programming current.

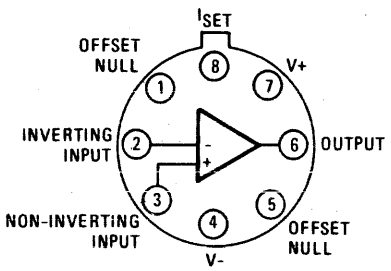
A major advantage of HA-2720/2725 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipment. A primary application for HA-2720/2725 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, HA-2720/2725 can be used for designs such as current controlled oscillators modulators, sample and hold circuits and variable active filters.

HA-2720 is guaranteed over -55°C to +125°C. HA-2725 is specified from 0°C to +75°C. Both parts are available in TO-99 cans or dice form.

PINOUT

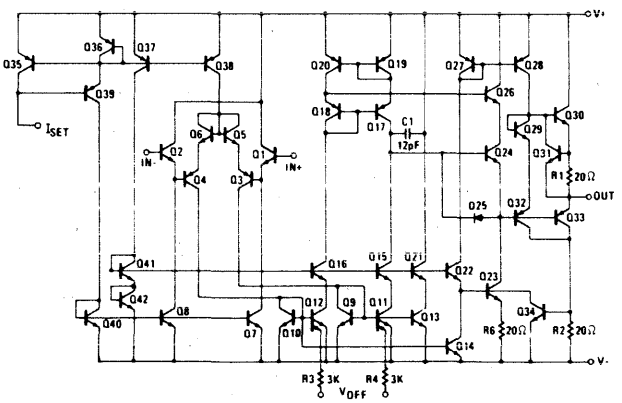
TO-99 **Package Code 2A**

Top View



NOTE: Case tied to V⁻

SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Power Dissipation (Note 2)	300mW
Differential Input Voltage	±30.0V	Operating Temperature Range:	
Input Voltage (Note 1)	±15.0V	HA-2720	$-55^{o}C \leq T_A \leq +125^{o}C$
I_{SET} (Current at I_{SET})	500μA	HA-2725	$0^{o}C \leq T_A \leq +75^{o}C$
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0V \leq V_{SET} \leq V+$	Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

V+ = +3.0V, V- = -3.0V

		HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
*Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
*Large Signal Voltage Gain (Note 9)	25°C	20K	40K		20K	40K		15K	40K		15K	40K		V/V
	Full	15K			15K			10K			10K			V/V
*Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±1.9			±2.0			±2.0			V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		μs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C		15			170			15			170		μA
	Full			20			200			20			200	μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

*100% Tested For DASH 8

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ELECTRICAL CHARACTERISTICS

V+ = +15.0V, V- = -15.0V

PARAMETER	TEMP.	HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						UNITS
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
*Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
*Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
*Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
*Large Signal Voltage Gain (Notes 3 & 9)	25°C	40K	100K		40K	120K		25K	100K		25K	120K		V/V
	Full	25K			25K			20K			20K			V/V
*Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	Full	±10			±10			±10			±10			V
Output Current (Note 5)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
*Supply Current	25°C		20			210			20			210		μA
	Full			25			250			25			250	μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

NOTES:
1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 6.8mW/°C for operation ambient temperatures above 75°C.

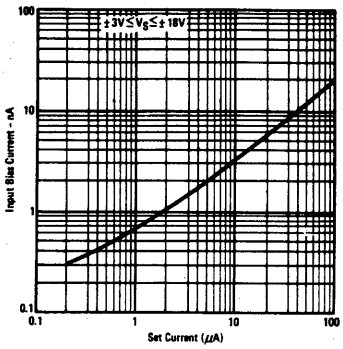
	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5μA	I_{SET} = 15μA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
	—	T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	← A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF →			
7.	V_O = ±2.0V	V_O = ±10.0V	RR$_L$ = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

*100% Tested For DASH 8

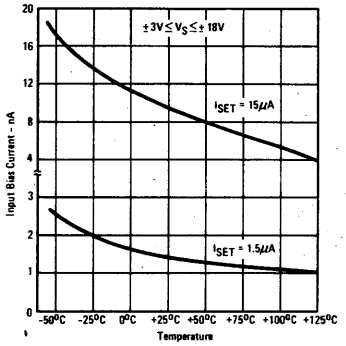
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UNLESS OTHERWISE NOTED: $T_A = 25^oC$, $V_S = \pm 15VDC$

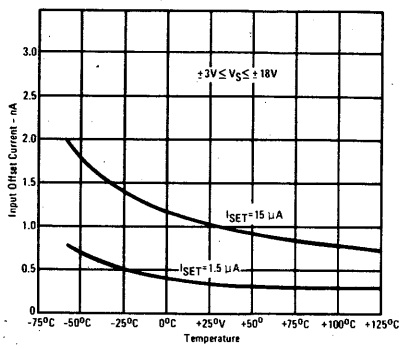
INPUT BIAS CURRENT vs. SET CURRENT



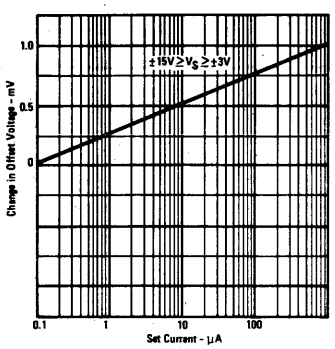
INPUT BIAS CURRENT vs. TEMPERATURE



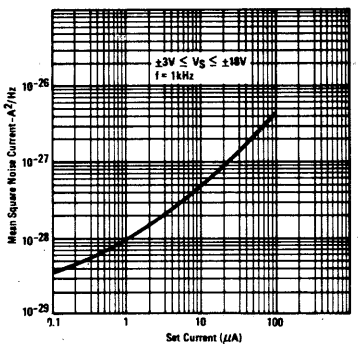
INPUT OFFSET CURRENT vs. TEMPERATURE



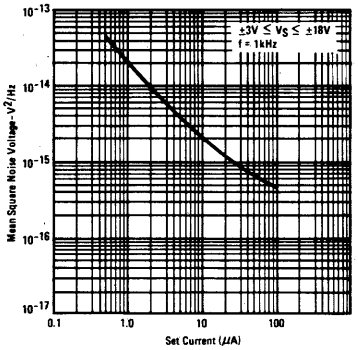
CHANGE IN OFFSET VOLTAGE vs. I_{SET} (UNNULLED)



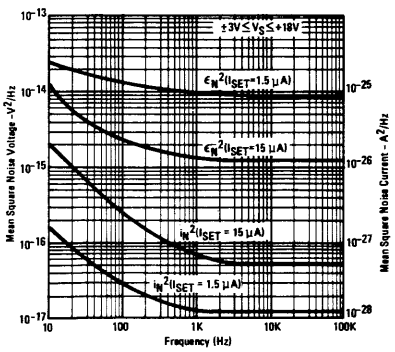
INPUT NOISE CURRENT vs. I_{SET}



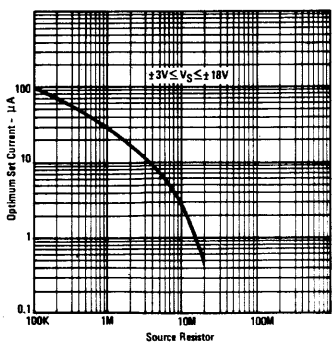
INPUT NOISE VOLTAGE vs. I_{SET}



INPUT NOISE VOLTAGE AND CURRENT vs. FREQUENCY



OPTIMUM SET CURRENT FOR MINIMUM NOISE vs. SOURCE RESISTOR

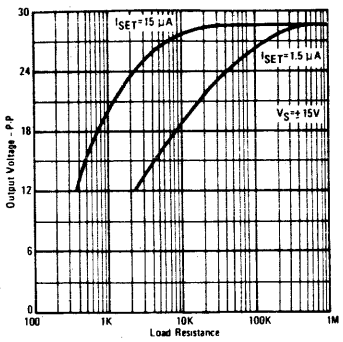


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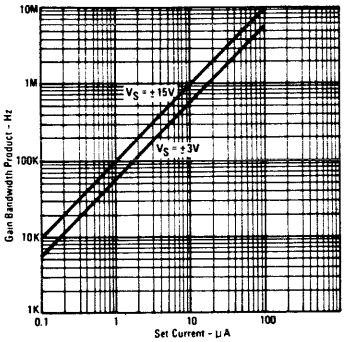
PERFORMANCE CURVES

UNLESS OTHERWISE NOTED: $T_A = +25^0C$, $V_S = \pm 15VDC$

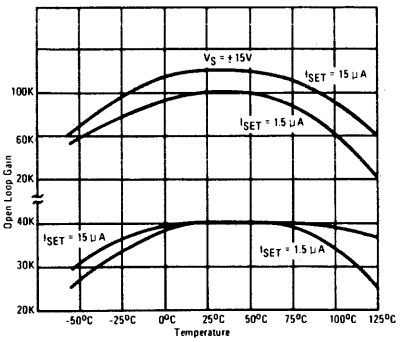
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



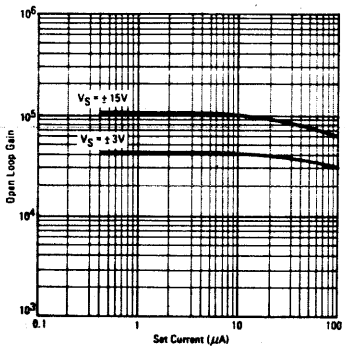
GAIN BANDWIDTH PRODUCT vs. I_{SET}



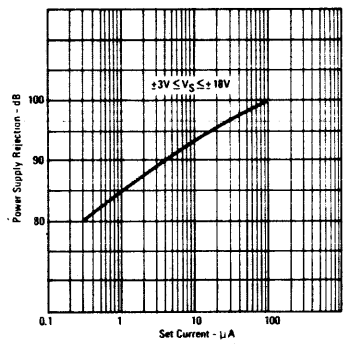
OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE



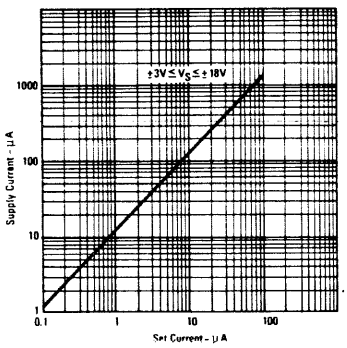
OPEN LOOP VOLTAGE GAIN vs. I_{SET}



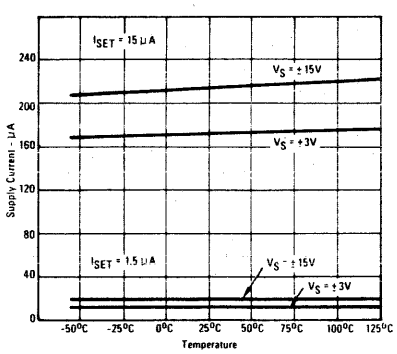
POWER SUPPLY REJECTION vs. I_{SET}



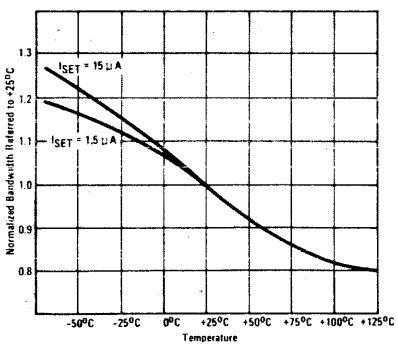
STANDBY SUPPLY CURRENT vs. I_{SET}



SUPPLY CURRENT vs. TEMPERATURE



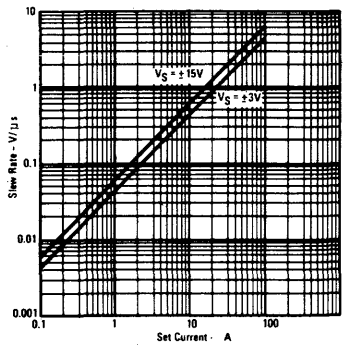
NORMALIZED BANDWIDTH vs. TEMPERATURE



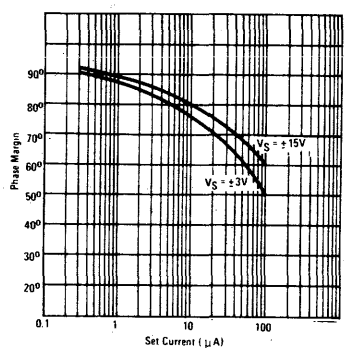
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PERFORMANCE CURVES

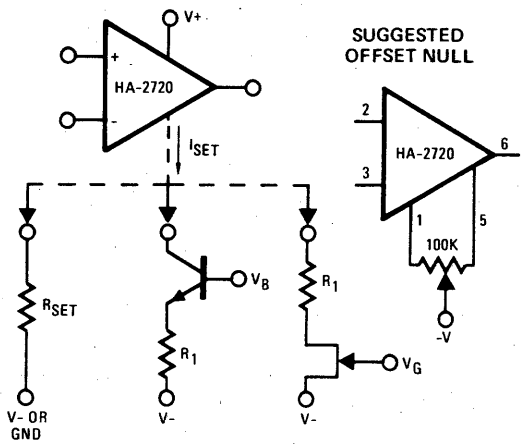
SLEW RATE vs. I_{SET}



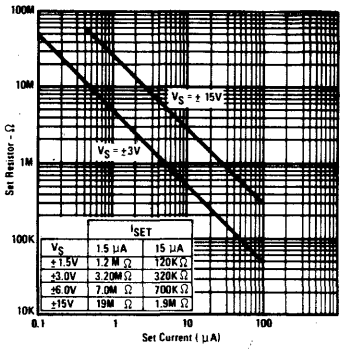
PHASE MARGIN vs. SET CURRENT



TYPICAL BIASING CIRCUITS

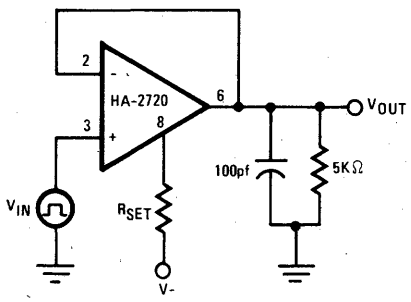


SET CURRENT VS. SET RESISTOR

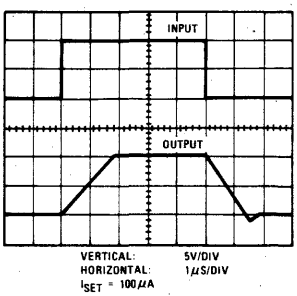


I_{SET} / V_S	1.5 µA	15 µA
±1.5V	1.2M Ω	120KΩ
±3.0V	3.20M Ω	320KΩ
±6.0V	7.0M Ω	700KΩ
±15V	19M Ω	1.9M Ω

TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEWING WAVEFORM



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2730/35

Wide Range Dual Programmable Operational Amplifier

FEATURES

- WIDE PROGRAMMING RANGE

SET CURRENT	0.1 TO 100μA
SLEW RATE	0.06 TO 6V/μs
BANDWIDTH	5kHz TO 10MHz
BIAS CURRENT	0.4 TO 50nA
SUPPLY CURRENT	1μA TO 1.5mA

- WIDE POWER SUPPLY RANGE $^{+}$1.2 TO $^{+}$18V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

HA-2730/2735 Dual Programmable Amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. Each amplifier on the chip can be adjusted independently. This versatile adjustment capability enables HA-2730/2735 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2730/2735 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting their programming current.

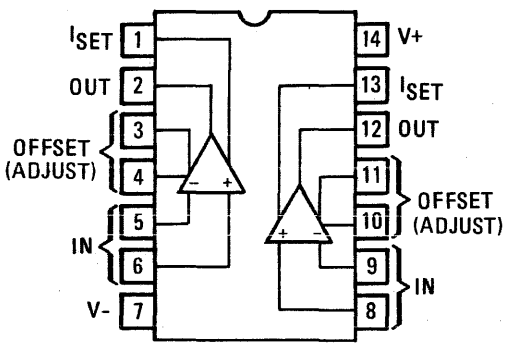
A major advantage of HA-2730/2735 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipement. A primary application for HA-2730/2735 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, HA-2730/2735 can be used for designs such as current controlled oscillators, modulators, sample and hold circuits and variable active filters.

HA-2730 is guaranteed over -55°C to +125°C. HA-2735 is specified from 0°C to +75°C. Both parts are available in 14 lead D.I.P. package or dice form.

PINOUT

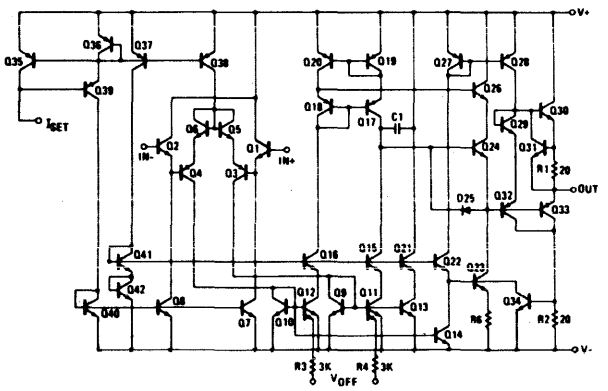
Package Code 4U

Top View



NOTE: Bottom of package is connected to V-.

SCHEMATIC



(ONE HALF ONLY)
HA-2730/35

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Power Dissipation (Note 2)	500mW
Differential Input Voltage	±30.0V	Operating Temperature Range:	
Input Voltage (Note 1)	±15.0V	HA-2730	$-55^{o}C \leq T_A \leq +125^{o}C$
I_{SET} (Current at I_{SET})	500μA	HA-2735	$0^{o}C \leq T_A \leq +75^{o}C$
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0V \leq V_{SET} \leq V+$	Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS (Each Side)

V+ = +3.0V, V- = -3.0V

		HA-2730 -55°C to +125°C						HA-2735 0°C to +75°C						
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
*Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
*Large Signal Voltage Gain (Notes 3 & 9)	25°C	20K	40K		20K	40K		15K	40K		15K	40K		V/V
	Full	15K			15K			10K			10K			V/V
*Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±1.9			±2.0			±2.0			V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		μs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/μs
POWER SUPPLY CHARACTERISTICS														
*Supply Current (Each Amp)	25°C		15			170			15			170		μA
	Full			20			200			20			200	μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

*100% Tested For DASH 8

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ELECTRICAL CHARACTERISTICS (Each Side)

V+ = +15.0V, V- = -15.0V

PARAMETER	TEMP.	HA-2730 -55°C to +125°C						HA-2735 0°C to +75°C						UNITS
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
*Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
*Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
*Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
*Large Signal Voltage Gain (Notes 3 & 9)	25°C	40K	100K		40K	120K		25K	100K		25K	120K		V/V
	Full	25K			25K			20K			20K			V/V
*Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	Full	±10			±10			±10			±10			V
Output Current (Note 5)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
*Supply Current (Each Amp)	25°C		20			210			20			210		μA
	Full			25			250			25			250	μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

NOTES:
1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 4.7mW/°C at ambient temperatures above 68°C.

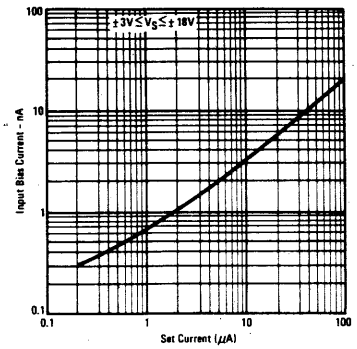
	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5μA	I_{SET} = 15μA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
	—	T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	← A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF →			
7.	V_O = ±2.0V	V_O = ±10.0V	RR_L = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

*100% Tested For DASH 8

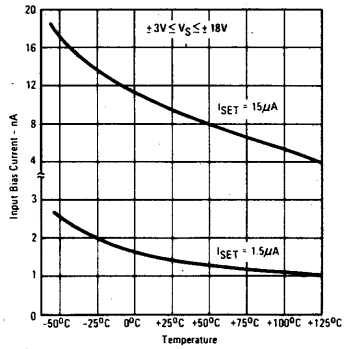
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UNLESS OTHERWISE NOTED: $T_A = +25^oC$, $V_S = \pm 15VDC$

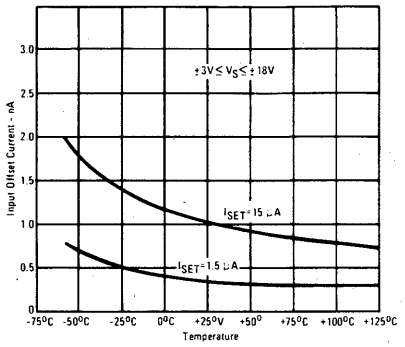
INPUT BIAS CURRENT
vs. SET CURRENT



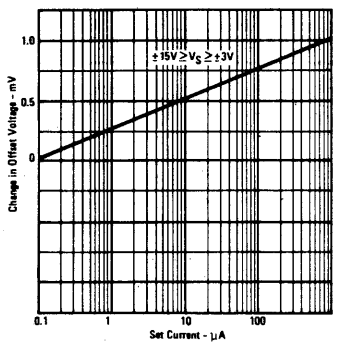
INPUT BIAS CURRENT
vs. TEMPERATURE



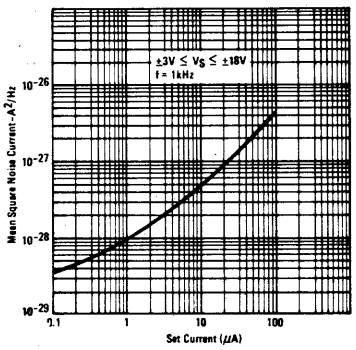
INPUT OFFSET CURRENT
vs. TEMPERATURE



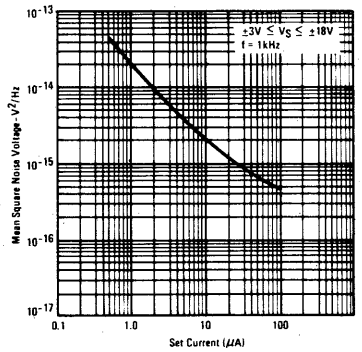
CHANGE IN OFFSET VOLTAGE
vs. I_{SET} (UNNULLED)



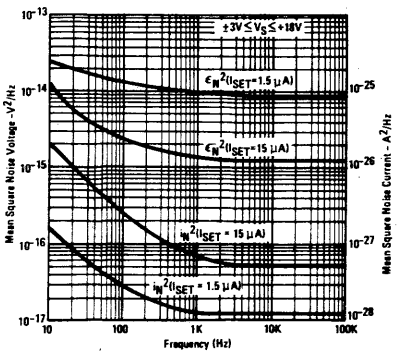
INPUT NOISE CURRENT
vs. I_{SET}



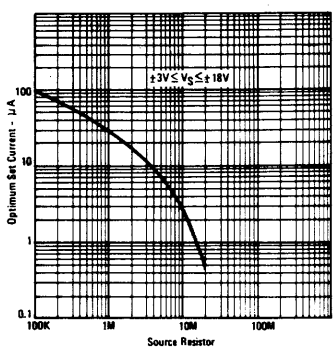
INPUT NOISE VOLTAGE
vs. I_{SET}



INPUT NOISE VOLTAGE AND CURRENT
vs. FREQUENCY



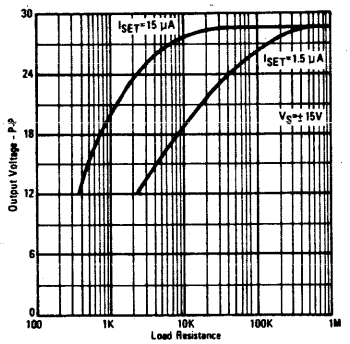
OPTIMUM SET CURRENT FOR MINIMUM
NOISE vs. SOURCE RESISTOR



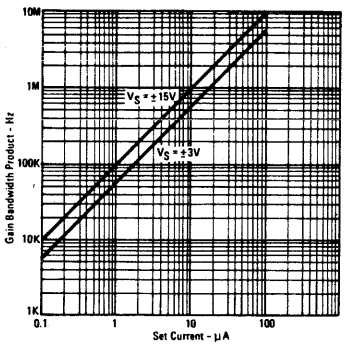
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UNLESS OTHERWISE NOTED: $T_A = 25^oC$, $V_S = \pm 15VDC$

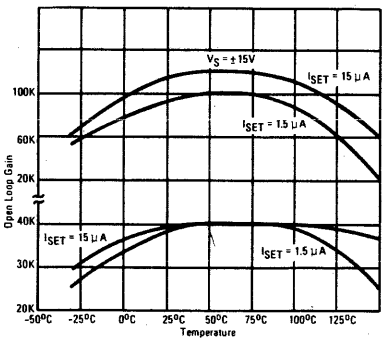
MAXIMUM OUTPUT VOLTAGE SWING
vs. LOAD RESISTANCE



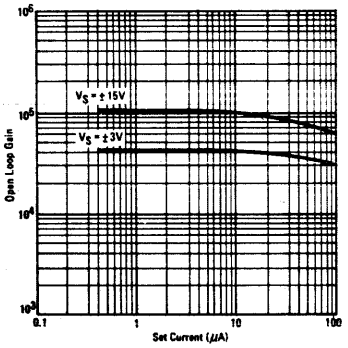
GAIN BANDWIDTH PRODUCT
vs. I_{SET}



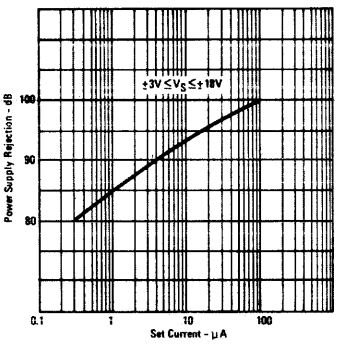
OPEN LOOP VOLTAGE GAIN
vs. TEMPERATURE



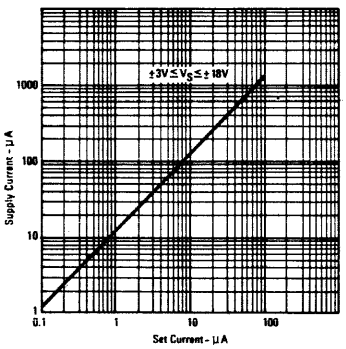
OPEN LOOP VOLTAGE GAIN
vs. I_{SET}



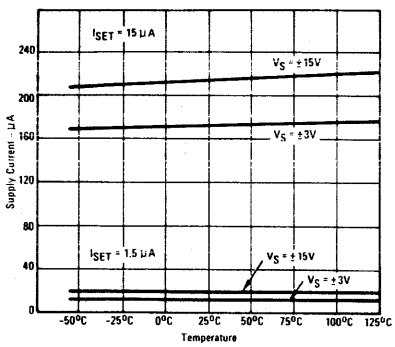
POWER SUPPLY REJECTION
vs. I_{SET}



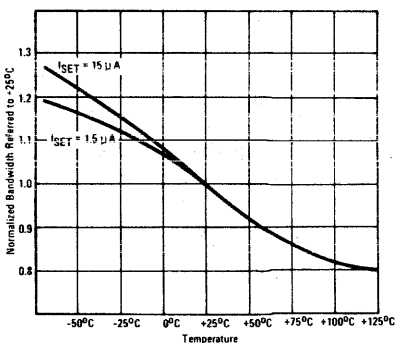
STANDBY SUPPLY CURRENT
vs. I_{SET}



SUPPLY CURRENT vs.
TEMPERATURE



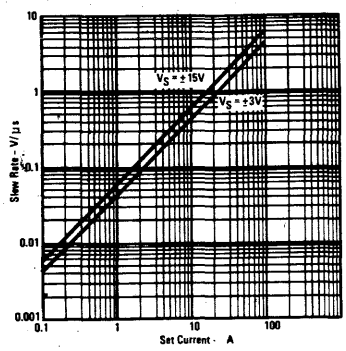
NORMALIZED BANDWIDTH
vs. TEMPERATURE



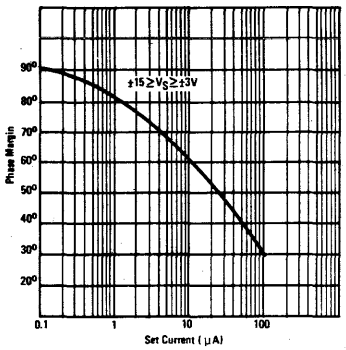
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PERFORMANCE CURVES

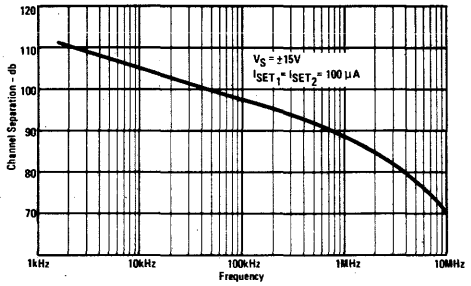
SLEW RATE vs. I_{SET}



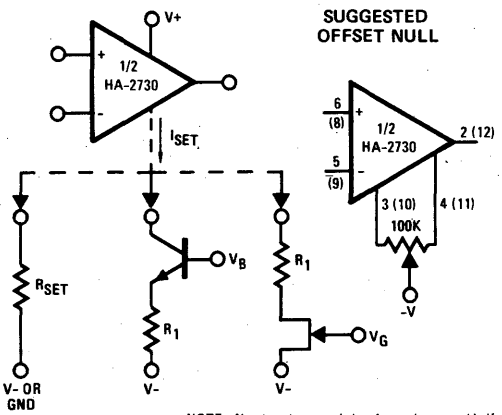
PHASE MARGIN vs. SET CURRENT



CHANNEL SEPARATION vs. FREQUENCY

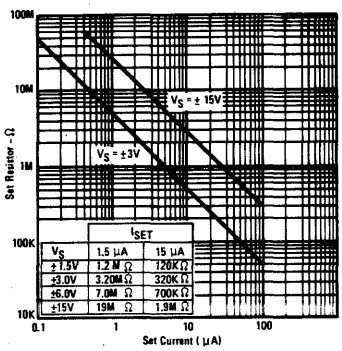


TYPICAL BIASING CIRCUITS



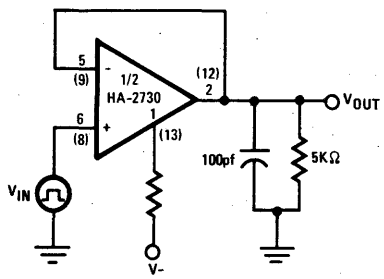
NOTE: Numbers in parenthsis refer to the second half.

SET CURRENT VS. SET RESISTOR



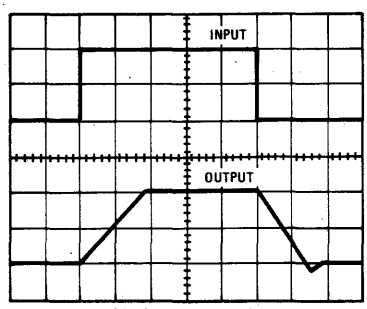
V_S	I_{SET} 1.5 µA	15 µA
±1.5V	1.2 MΩ	120KΩ
±3.0V	3.20MΩ	320KΩ
±6.0V	7.0MΩ	700KΩ
±15V	19MΩ	1.9MΩ

TRANSIENT RESPONSE/SLEW RATE CIRCUIT



NOTE: Numbers in parenthsis refer to the second half.

SLEWING WAVEFORM



VERTICAL: 5V/DIV
HORIZONTAL: 1µS/DIV
I_{SET} = 100µA

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2900/04/05

Chopper Stabilized Operational Amplifier

FEATURES

- OFFSET VOLTAGE DRIFT — 0.2 μV/°C
- OFFSET CURRENT DRIFT — 1pA/°C
- OPEN LOOP GAIN — 5×10^8
- BANDWIDTH — 3MHz
- SLEW RATE — 2.5V/μs
- TRUE DIFFERENTIAL INPUTS

APPLICATIONS

- HIGH-GAIN DC INSTRUMENTATION
- HIGH-ACCURACY WEIGHING EQUIPMENT
- BIOMEDICAL AMPLIFIERS
- PRECISION INTEGRATORS AND TIMERS

DESCRIPTION

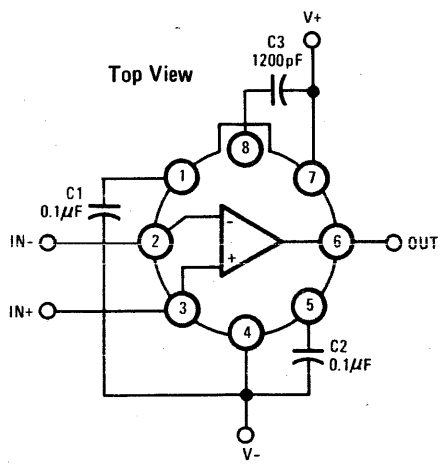
HA-2900/2904/2905 are monolithic chopper-stabilized operational amplifiers that employ dielectric isolation achieving superior offset drift, extremely low input currents and excellent AC performance. Input drift is characterized by offset voltage drift of 0.2 μV/°C and offset current drift of 1pA/°C. Initial offset voltage is only 20 μV while offset current is 50pA. These input specifications make HA-2900/2904/2905 ideally suited to high accuracy applications such as high-gain DC instrumentation, and precision integration. The amplifiers can be used to replace other op amps in designs where much lower errors are required without external adjustments. 3MHz gain-bandwidth product makes HA-2900/2904/2905 valuable for processing wide band signals as well as for low frequency measurements.

In addition to offering high-accuracy performance, these "choppers" also offer versatility by virtue of their symmetrical, differential inputs which permit operation in any op amp configuration – inverting, non-inverting or balanced. These devices require only three external capacitors for proper operation.

HA-2900 is guaranteed over -55°C to +125°C; HA-2904 operates from -25°C to +85°C; HA-2905 operates from 0°C to +75°C. All devices are available in a hermetically sealed metal can.

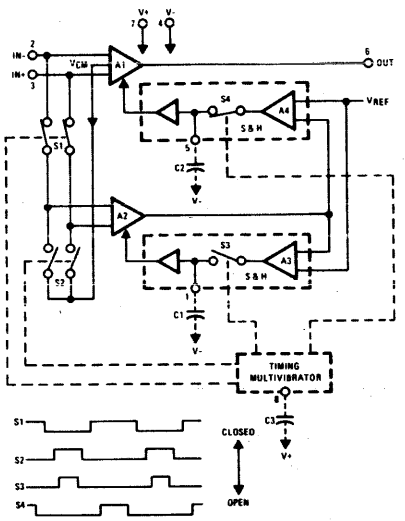
PINOUT AND SUGGESTED HOOKUP

TO-99 — Package Code 2E



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

FUNCTIONAL DIAGRAM



SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	42.0V	Operating Temperature Range	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$ (HA-2900)
Differential Input Voltage (Note 1)	±15V		$-25^{\circ}C \leq T_A \leq +85^{\circ}C$ (HA-2904)
Output Current/Full Short Circuit Protection		Storage Temperature Range	$0^{\circ}C \leq T_A \leq +75^{\circ}C$ (HA-2905)
Internal Power Dissipation	300mW*		$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

*Derate by 6.6mW/°C above +105°C

ELECTRICAL CHARACTERISTICS

Test Conditions: C1 = C2 = 0.1μF, C3 = 1500pF, V_{Supply} = ±15.0V unless otherwise specified.

		HA-2900 -55°C to +125°C			HA-2904 -25°C to +85°C			HA-2905 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
*Offset Voltage	+25°C		20			20			20		μV
	Full			60			50			80	μV
Offset Voltage Average Drift	Full		0.3	0.6		0.2	0.4		0.2		μV/°C
*Bias Current	+25°C		150			150			150		pA
	Full			1,000			1,000			1,000	pA
*Offset Current	+25°C		50			50			50		pA
	Full			500			500			500	pA
Offset Current Average Drift	Full		1	4		1	3		1		pA/°C
Input Resistance	+25°C		100			100			100		MΩ
Input Capacitance	+25°C		10			10			10		pF
Common Mode Range	Full	±10			±10			±10			V
TRANSFER CHARACTERISTICS											
*Large Signal Voltage Gain (Note 2)	+25°C		$5x10^8$			5×10^8			5×10^8		V/V
	Full	10^6			10^7			10^6			V/V
Chopper Frequency	+25°C		750			750			750		Hz
*Common Mode Rejection Ratio (Note 3)	Full	120	160		130	160		120	160		dB
Gain Bandwidth Product (Note 4)	+25°C		3			3			3		MHz
OUTPUT CHARACTERISTICS											
*Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		±10	±12		V
*Output Current	+25°C	±10			±10			±7			mA
Output Resistance	Full		200			200			200		Ω
Full Power Bandwidth (Note 5)	+25°C		40			40			40		kHz
TRANSIENT RESPONSE (NOTES 2, 8, and 9)											
Rise Time (Note 6)	+25°C		200			200			200		ns
Overshoot (Note 6)	+25°C		20			20			20		%
Slew Rate (Note 5)	+25°C		2.5			2.5			2.5		V/μs
POWER SUPPLY CHARACTERISTICS											
*Supply Current	+25°C		3.5	5.0		3.5	5.0		3.5	5.0	mA
*Supply Voltage Range	Full	±12		±20	±10		±20	±12		±20	V
*Power Supply Rejection Ratio (Note 7)	Full	120	160		130	160		120	160		dB

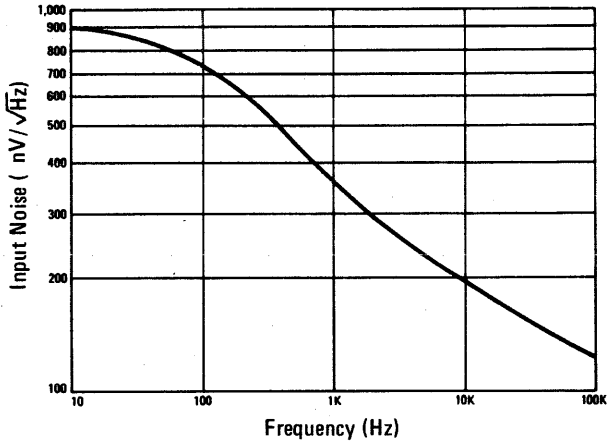
NOTES:
1. Input terminals should be protected against static discharge during handling and installation. Input voltage should never exceed supply voltages.
2. R_L = 2K
3. V_{CM} = ±5.0V
4. A_V = 10
5. V_O = ±10V
6. V_O = ±200mV
7. ΔV_S = ±5V
8. C_L = 50pF
9. A_V = +1 See transient response test circuits and waveforms, page 4.

*100% Tested For DASH 8

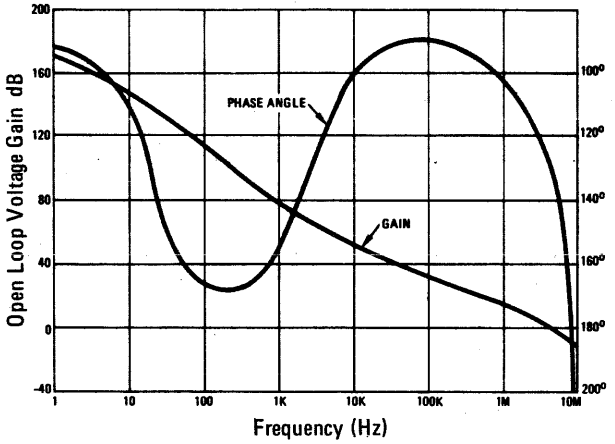
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V+ = V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

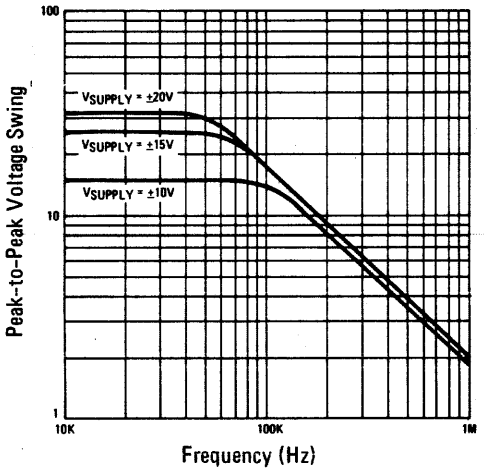
INPUT VOLTAGE NOISE



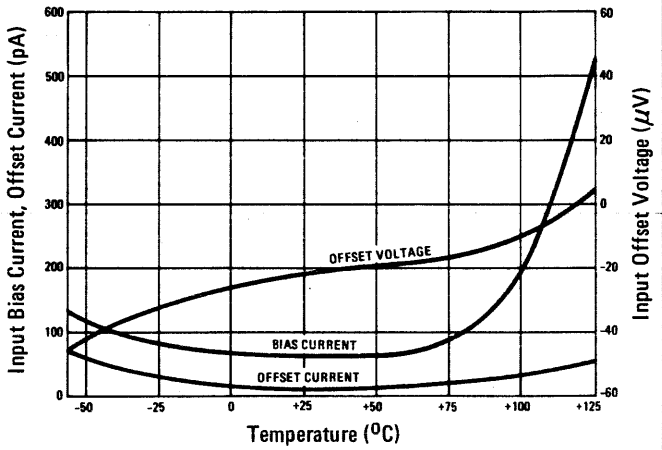
OPEN LOOP FREQUENCY AND PHASE RESPONSE



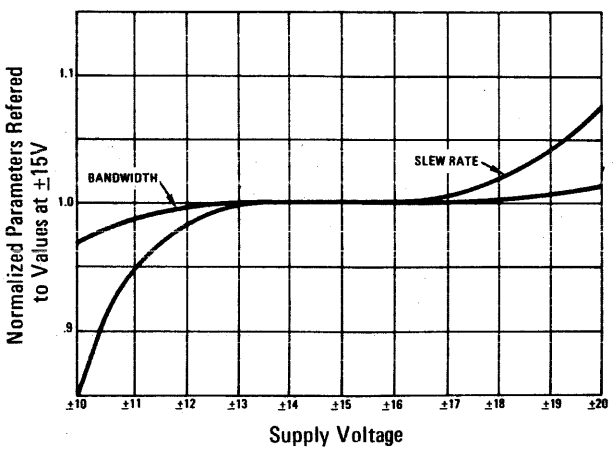
OUTPUT VOLTAGE SWING vs. FREQUENCY



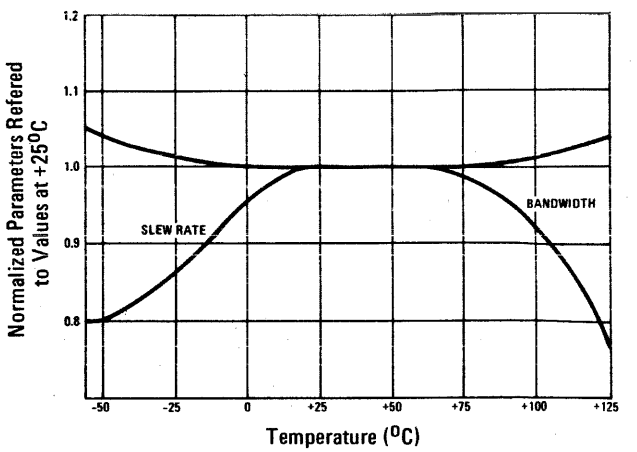
TYPICAL INPUT CHARACTERISTICS vs. TEMPERATURE



NORMALIZED A.C. PARAMETERS vs. SUPPLY VOLTAGE



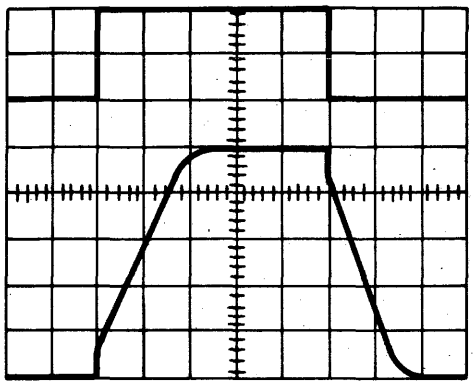
NORMALIZED A.C. PARAMETERS vs. TEMPERATURE



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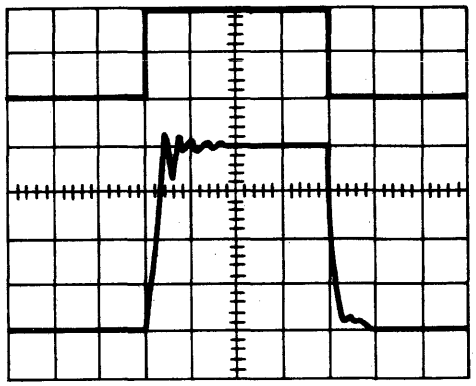
PERFORMANCE CURVES (continued)

VOLTAGE FOLLOWER
SLEWING WAVEFORM



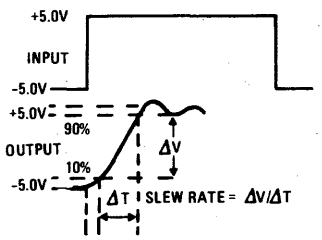
Upper Trace: Input: 5V/Div.
Lower Trace: Output; 2V/Div.
Horizontal: 2μS/Div.

VOLTAGE FOLLOWER
TRANSIENT RESPONSE WAVEFORM

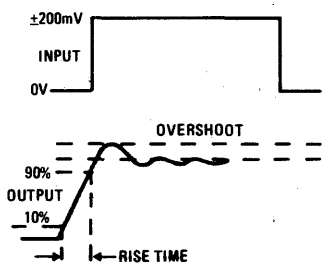


Upper Trace: Input; 100mV/Div.
Lower Trace: Output; 50mV/Div.
Horizontal: 500ns/Div.

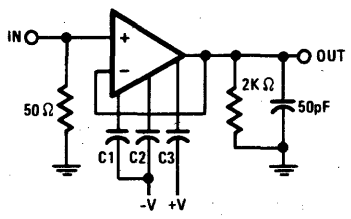
SLEW RATE



TRANSIENT RESPONSE



SLEW RATE AND
TRANSIENT RESPONSE



NOTE: Measured on both positive and negative transitions.

APPLICATION TIPS

(1) Device inputs should be protected against exceeding either supply voltage from static discharge or inadvertent connection, particularly when wired directly to a connector or instrument panel.

(2) External capacitors C1, C2, and C3 should have good temperature stability, low leakage, and low dielectric absorption. Polystyrene (below +85°C), teflon types or polycarbonate are recommended. C3 could also be silver mica.

(3) Particular care must be exercised in system layout and material and component selection to realize the full performance potential of the HA-2900/2904/2905. External sources of drift error may include the thermocouple and electrochemical EMF's generated at junctions of dissimilar metals, leakage across insulating materials, static charges created by moving air, and improper grounding and shielding practices.

(4) Chopper noise is present chiefly as a common mode input current signal, and may be minimized by matching the impedances at the two inputs. Random noise may be reduced at the expense of bandwidth using active or passive filtering.

(5) Input frequencies near the chopper frequency (750Hz) or its harmonics may result in small components of difference frequency in the output. This effect should be checked in the individual application, and if objectionable, a low pass filter may be added in series with the input.

(6) When operating at closed loop gains between 70 dB and 140 dB, compensation networks may be required, because of open loop phase shift in this gain region. In most cases, a capacitor placed in parallel with the feedback resistor to yield a gain-bandwidth product < 2MHz will be sufficient.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-4602/4605

High Performance Quad Operational Amplifier

FEATURES

- LOW OFFSET VOLTAGE 0.3mV
- HIGH SLEW RATE ±4V/μs
- WIDE BANDWIDTH 8MHz
- LOW DRIFT 2μV/°C
- FAST SETTLING (0.01%, 10V STEP) 4.2μs
- LOW POWER CONSUMPTION 35mW/AMP
- SUPPLY RANGE ±5V TO ±20V

APPLICATIONS

- HIGH Q, WIDE BAND FILTERS
- INSTRUMENTATION AMPLIFIERS
- AUDIO AMPLIFIERS
- DATA ACQUISITION SYSTEMS
- INTEGRATORS
- ABSOLUTE VALUE CIRCUITS
- TONE DETECTORS

DESCRIPTION

The HA-4602 and HA-4605 are high performance dielectrically isolated monolithic quad operational amplifiers with superior specifications not previously available in a quad amplifier. These amplifiers offer excellent dynamic performance coupled with low values for offset voltage and drift, input noise voltage and power consumption.

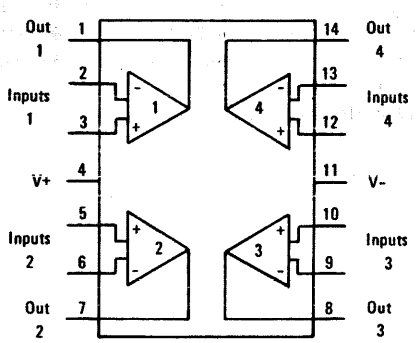
A wide range of applications can be achieved by using the features made available by the HA-4602/4605. With wide bandwidth (8MHz), low power (35mW/amp), and internal compensation, these devices are ideally suited for precision active filter designs. For audio applications these amplifiers offer low noise ($8nV/\sqrt{Hz}$) and excellent full power bandwidth (60kHz). The HA-4602/4605 is particularly useful in designs requiring low offset voltage (0.3mV) and drift (2 μV/°C), such as instrumentation and signal conditioning circuits. The high slew rate (4V/μs) and fast settling time (4.2 μs to 0.01%, 10V step) makes these amplifiers useful components in fast, accurate data acquisition systems.

The HA-4602 and 4605's are available in 14 pin CERDIP packages which are interchangeable with most other quad op amps. HA-4602 is specified from -55°C to +125°C, and HA-4605 is specified over 0°C to +75°C range.

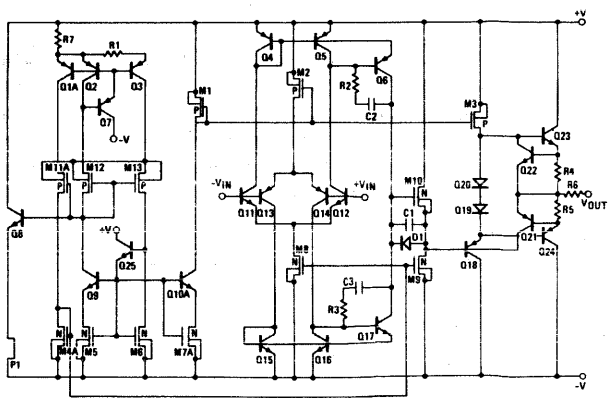
PINOUT

Package Code 4U

TOP VIEW



SCHEMATIC



ONE FOURTH ONLY (HA-4602/4605)

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V	Power Dissipation (Note 4)	880mW
Differential Input Voltage	±7V	Operating Temperature Range	
Input Voltage (Note 2)	±15.0V	HA-4602-2	$-55^oC \leq T_A \leq +125^oC$
Output Short Circuit Duration (Note 3)	Indefinite	HA-4605-5	$0^oC \leq T_A \leq +75^oC$
		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

V+ = 15V, V- = -15V

PARAMETER	TEMP.	HA-4602-2 -55°C to +125°C MIN.	HA-4602-2 -55°C to +125°C TYP.	HA-4602-2 -55°C to +125°C MAX.	HA-4605-5 0°C to +75°C MIN.	HA-4605-5 0°C to +75°C TYP.	HA-4605-5 0°C to +75°C MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		0.3	2.5		0.5	3.5	mV
	Full			3.0			4.0	mV
Av. Offset Voltage Drift	Full		2			2		µV/°C
* Bias Current	+25°C		130	200		130	300	nA
	Full			325			400	nA
* Offset Current	+25°C		30	75		30	100	nA
	Full			125			120	nA
Common Mode Range	Full	±12			±12			V
Input Noise Voltage (f = 1KHz)	+25°C		8			8		$nV/\sqrt{Hz}$
Input Resistance			500			500		KΩ
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 5)	Full	100K	250K		75K	250K		V/V
* Common Mode Rejection Ratio (Note 9)	Full	86			80			dB
Channel Separation (Note 6)	+25°C		-108			-108		dB
Small Signal Bandwidth	+25°C		8			8		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (R_L = 10K)	Full	±12	±13		±12	±13		V
(R_L = 2K)	Full	±10	±12		±10	±12		V
Full Power Bandwidth (Note 5)	+25°C		60			60		KHz
Output Current (Note 7)	Full	±10	±15		±8	±15		mA
Output Resistance	+25°C		200			200		Ω
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		50			50		ns
Overshoot	+25°C		30			30		%
Slew Rate	+25°C		±4			±4		V/µs
Settling Time (Note 10)			4.2			4.2		µs
POWER SUPPLY CHARACTERISTICS								
* Supply Current (I^+ or I^-)	+25°C		4.6	5.5		5.0	6.5	mA
* Power Supply Rejection Ratio (Note 9)	Full	86			80			dB

*100% tested for HA1-4602-8

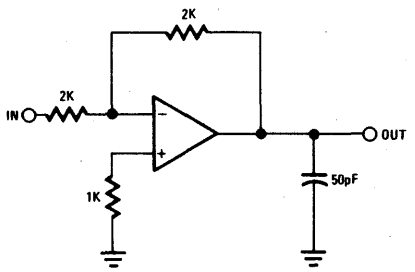
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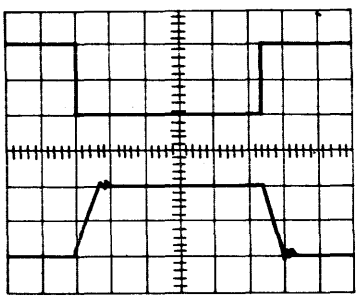
NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V; R_L = 2K ohms.
6. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak-to-peak; R_S = 1K ohms. (Refer to Channel Separation vs. Frequency Curve for test circuits.)
7. Output current is measured with V_{OUT} = ±5 volts. The output current specified can also be applied to V_{OUT} = ±10V.
8. For transient response test circuits and measurement conditions refer to Test Circuits section of the data sheet.
9. ΔV = ±5.0 volts.
10. Settling time is measured to 0.01% of final value for a 10 volt input step, A_V = -1.

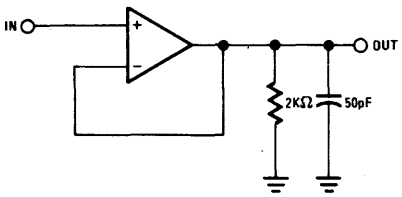
TEST CIRCUITS

LARGE SIGNAL RESPONSE CIRCUIT (Volts: 5V/Div., Time: 5μs/Div.)

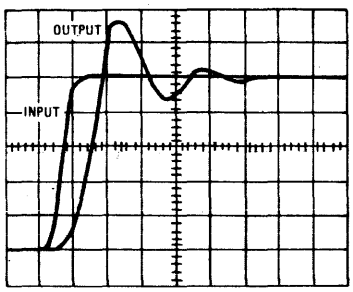




VERT. 5V/DIV.
HORZ. 5 μs/DIV.

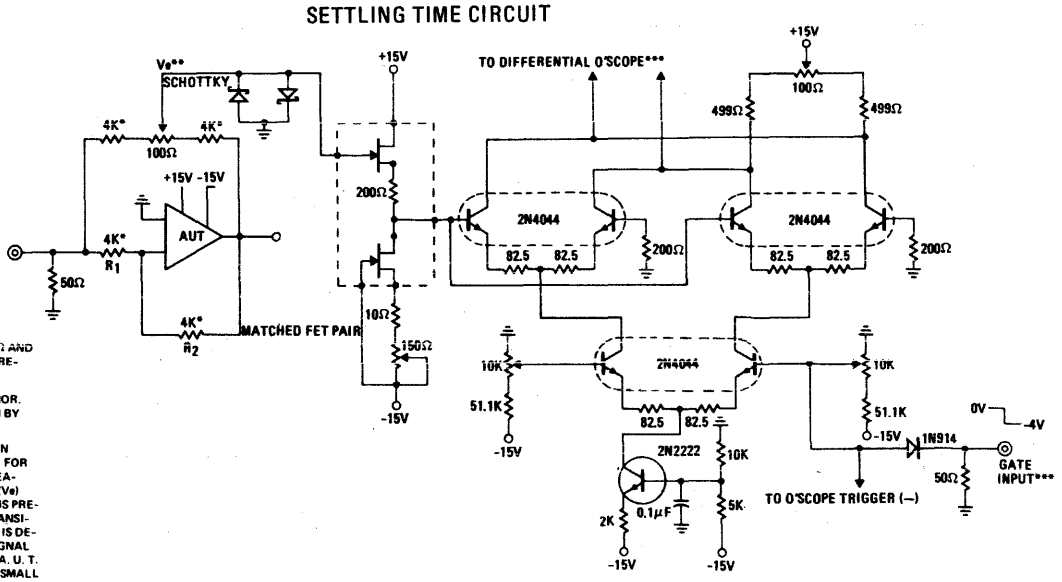


SMALL SIGNAL RESPONSE CIRCUIT (Volts: 10mV/Div., Time: 50ns/Div.)



HORIZONTAL: 50 NSEC/DIV.
VERTICAL: 10mV/DIV

SETTLING TIME CIRCUIT



* SHOWN FOR AV = -1. USE 800Ω AND 400Ω FOR AV = -5, AV = -10, RESPECTIVELY.

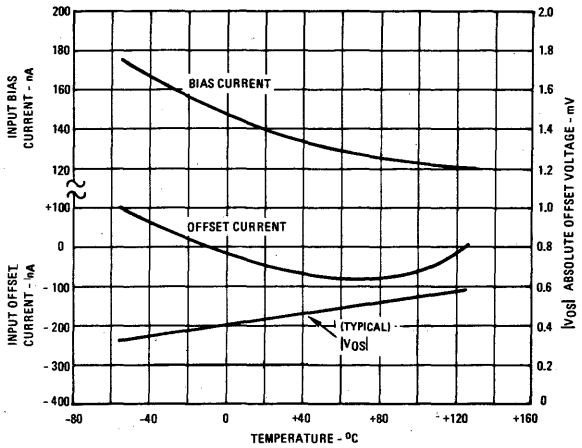
** THIS IS SUMMING POINT ERROR. OUTPUT ERROR, ε, IS GIVEN BY ε = (1 + AV) Ve.

*** MEASUREMENT IS 5*Ve WHEN GATE INPUT IS "LOW" (-4V). FOR GATE INPUT "HIGH" (0V), MEASUREMENT IGNORES INPUT (Ve) SO THAT SCOPE OVERLOAD IS PREVENTED DURING LARGE TRANSITIONS. GATE INPUT SIGNAL IS DELAYED WITH RESPECT TO SIGNAL INPUT TO ALLOW TIME FOR A. U. T. SLEWING AND SETTLING TO SMALL ERROR VOLTAGES.

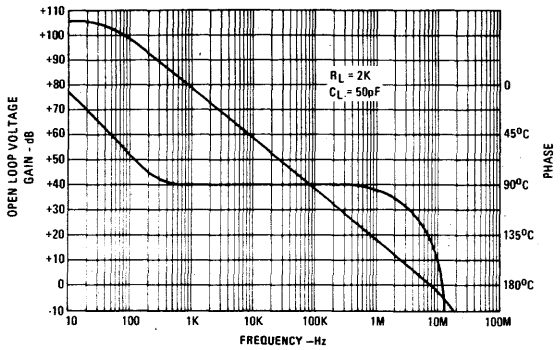
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V+ = +15V, V- = -15V, T_A = +25°C Unless Otherwise Stated.

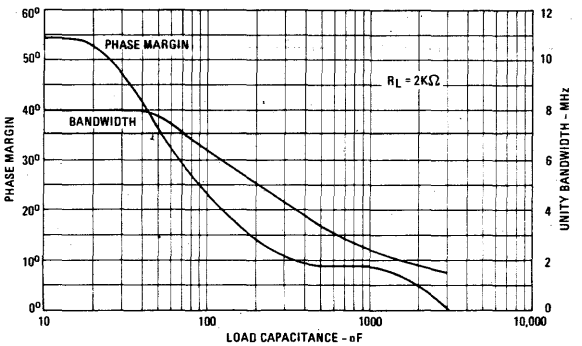
OFFSET VOLTAGE INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



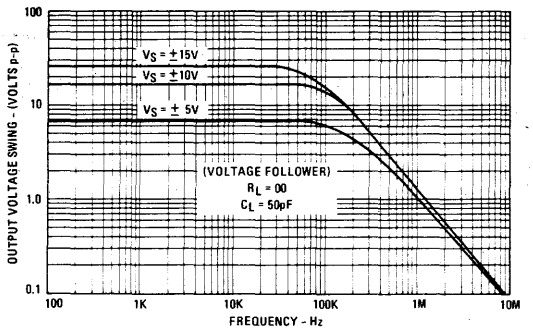
OPEN LOOP FREQUENCY RESPONSE



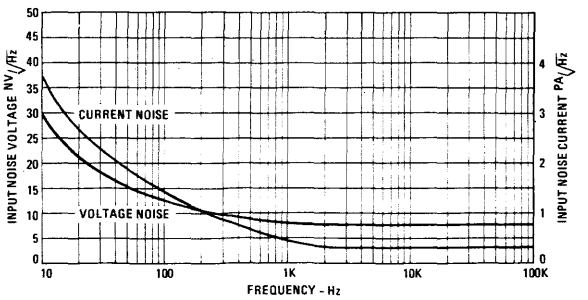
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



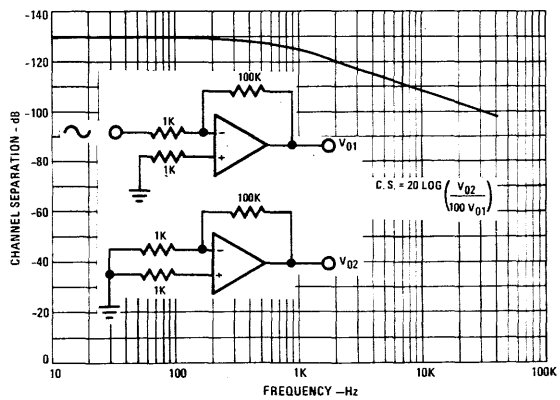
OUTPUT VOLTAGE SWING VS. FREQUENCY AND SUPPLY VOLTAGE



INPUT NOISE VS. FREQUENCY

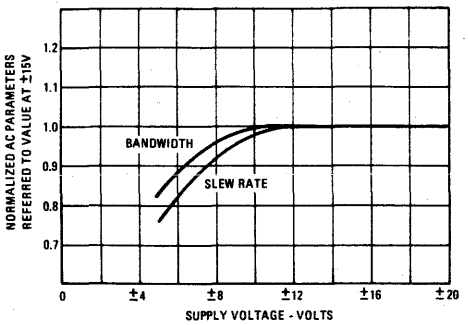


CHANNEL SEPARATION VS. FREQUENCY

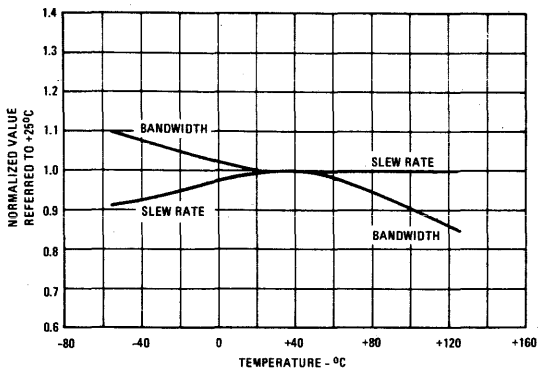


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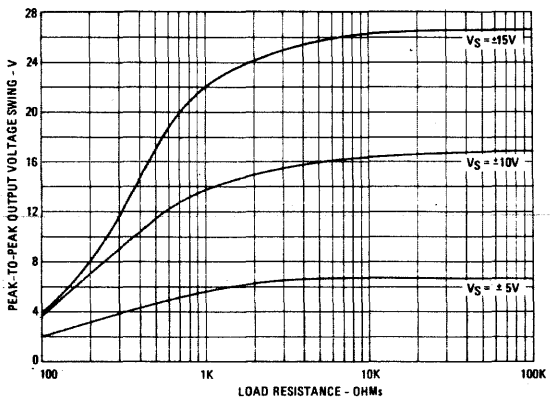
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



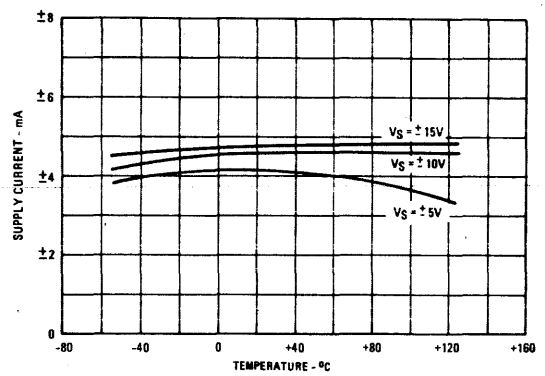
NORMALIZED AC PARAMETERS VS. TEMPERATURE



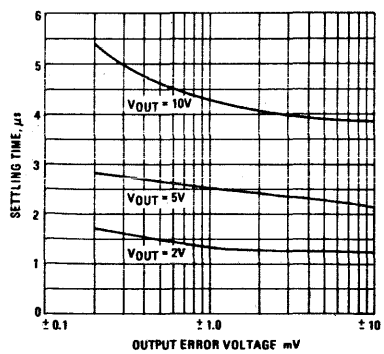
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SUPPLY VOLTAGE



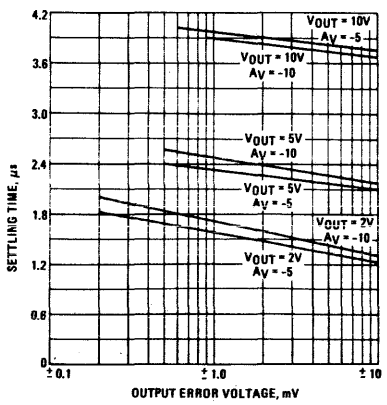
POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE



SETTLING TIME VS. OUTPUT AMPLITUDE (A_V = -1)



SETTLING TIME VS. OUTPUT AMPLITUDE AND SIGNAL GAIN (A_V = -5 AND A_V = -10)



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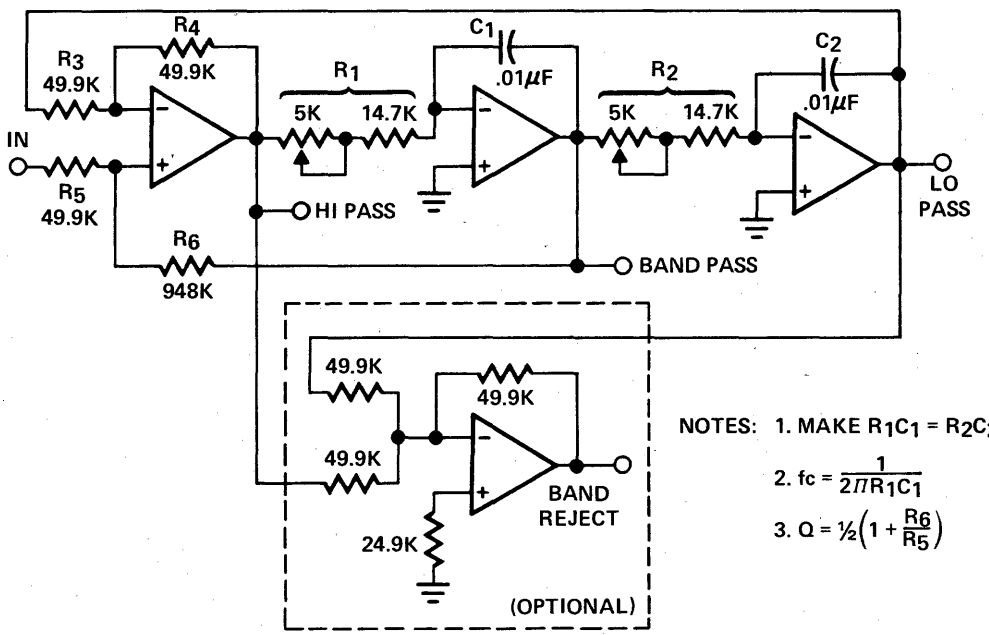
1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01 μ F ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. UNUSED OP AMPS: Unused op amp sections should be connected in a non-inverting follower configuration with the (+) input tied to ground in order to insure optimum performance of devices being used.

3. In high frequency applications where large value feedback resistors are used, a small capacitor (3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by input capacitance.

APPLICATIONS

2ND ORDER STATE VARIABLE FILTER (1kHz, Q = 10)



NOTES: 1. MAKE $R_1C_1 = R_2C_2$

2. $f_c = \frac{1}{2\pi R_1 C_1}$

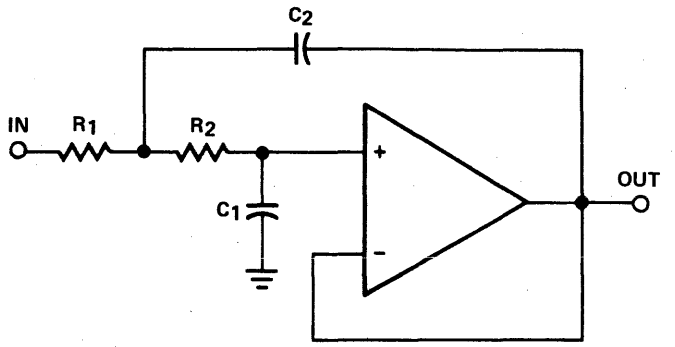
3. $Q = \frac{1}{2}\left(1 + \frac{R_6}{R_5}\right)$

The state variable filter is relatively insensitive to component changes (changes can be adjusted out with potentiometers) and also has low sensitivity to amplifier bandwidths. (Amplifier gain bandwidth product should be $\gg Q \times f_C$). The bandwidth criteria will determine whether a general purpose op amp like Harris HA-4741 or the wide band HA-4602/4605 should be used.

This filter finds wide application because multiple filtering functions are available simultaneously (High pass, Lo pass, Band pass, Band reject). In this circuit the various RC products are matched with pot adjustments allowing for non-interactive adjustment of Q and f_C. This allows capacitors (C_1, C_2) with loose tolerances to be used. To tune for f_C, apply a sine wave at f_C to the input, adjust R_1 for equal amplitudes at the Hi pass and Band pass terminals (they will be phased 90° apart) then adjust R_2 for equal amplitudes at the Band pass and Lo pass terminals.

The state variable filter is often used as building blocks in multiple pole Butterworth of Chebyshev filters. Many references contain normalized tables indicating settings for Q and f_C of each pole-pair section.

SALLEN AND KEY 2ND ORDER LO PASS FILTER



NOTES:

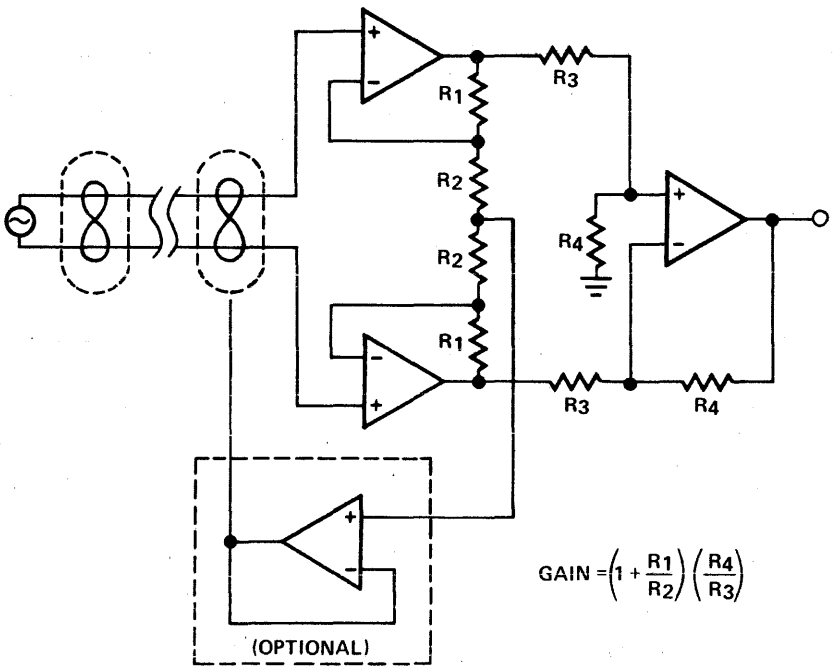
1. Make $R_1 = R_2$
2. $f_c = \frac{1}{2\pi R_1\sqrt{C_1C_2}}$
3. $Q = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}$

The advantage of using the Sallen and Key filter is simplicity, but in any application this must be weighed against the state-variable type filter for accuracy, practicality, and cost. Amplifier bandwidth limitations are much more apparent at moderate frequencies and Q values with this filter design. (For accuracy, amplifier gain-bandwidth product should be $\gg f_C \times Q^2$). The wide bandwidth of the HA-4602/4605 is particularly advantageous in this design even at audio frequencies.

In this filter all component values affect both Q and f_C. Precision, temperature stable resistors and capacitors must be used.

For economy, this filter could be used in the low Q stages of multiple-pole filter design, while the state variable type is used in the more critical stages.

INSTRUMENTATION AMPLIFIER



Instrumentation amplifiers (differential amplifiers) are specifically designed to extract and amplify small differential signals from much larger common mode voltages.

To serve as building blocks in instrumentation amplifiers, op amps must have very low offset voltage drift, high gain and wide bandwidth. The HA-4602/4605 is ideally suited for this application, delivering superior input and speed characteristics.

The optional circuitry makes use of the fourth amplifier section as a shield driver which enhances the AC common mode rejection by nullifying the effects of capacitance-to-ground mismatch between input conductors.

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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-4741

Quad Operational Amplifier

FEATURES

- SLEW RATE 1.6V/μs (TYP.)
- BANDWIDTH 3.5MHz (TYP.)
- INPUT VOLTAGE NOISE 9nV/$\sqrt{Hz}$ (TYP.)
- INPUT OFFSET VOLTAGE 0.5mV (TYP.)
- INPUT BIAS CURRENT 60nA (TYP.)
- SUPPLY RANGE ±2V TO ±20V
- NO CROSSOVER DISTORTION
- STANDARD QUAD PIN-OUT

APPLICATIONS

- UNIVERSAL ACTIVE FILTERS
- D3 COMMUNICATIONS FILTERS
- AUDIO AMPLIFIERS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

The HA-4741, which contains four amplifiers on a monolithic chip, provides a new measure of performance for general purpose operational amplifiers. Each amplifier in the HA-4741 has operating specifications that equal or exceed those of the 741-type amplifier in all categories of performance.

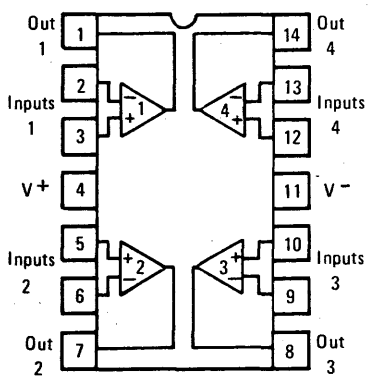
HA-4741 is well suited to applications requiring accurate signal processing by virtue of its low values of input offset voltage (0.5mV), input bias current (60nA) and input voltage noise (9nV/ $\sqrt{Hz}$ at 1kHz). 3.5MHz bandwidth, coupled with high open-loop gain, allow the HA-4741 to be used in designs requiring amplification of wide band signals, such as audio amplifiers. Audio application is further enhanced by the HA-4741's negligible output crossover distortion. These excellent dynamic characteristics also make the HA-4741 ideal for a wide range of active filter designs. Performance integrity of multi-channel designs is assured by a high level of amplifier-to-amplifier isolation (108dB at 1kHz).

A wide range of supply voltages (±2V to ±20V) can be used to power the HA-4741, making it compatible with almost any system including battery-powered equipment.

The HA-4741 has guaranteed operation over -55°C to +125°C and can be furnished to meet MIL-STD-883 (HA-4741-8). The HA-4741-5 is guaranteed over 0°C to +75°C and is available in ceramic and plastic dual-in-line packages and in dice form.

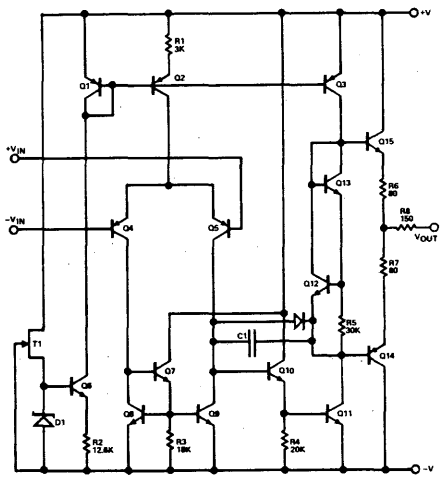
PINOUT

Package Code 4U
Package Code 3B (-5 Only)



QUAD OP AMP

SCHEMATIC



(¼) HA-4741

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V− Terminals	40.0V	Power Dissipation (Note 3)	880mW
Differential Input Voltage	±30.0V	Operating Temperature Range	
Input Voltage (Note 1)	±15.0V	HA-4741-2	−55°C≤T_A≤+125°C
Output Short Circuit Duration (Note 2)	Indefinite	HA-4741-5	0°C≤T_A≤+75°C
		Storage Temperature Range	−65°C≤T_A≤+150°C

ELECTRICAL CHARACTERISTICS

V+ = 15V, V− = −15V

PARAMETER	TEMP.	HA-4741-2 −55°C to +125°C MIN.	TYP.	MAX.	HA-4741-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		0.5	3.0		1.0	5.0	mV
	Full		4.0	5.0		5.0	6.5	mV
Av. Offset Voltage Drift	Full		5			5		µV/°C
* Bias Current	+25°C		60	200		60	300	nA
	Full			325			400	nA
* Offset Current	+25°C		15	30		30	50	nA
	Full			75			100	nA
Common Mode Range	Full	±12			±12			V
Differential Input Resistance	+25°C		5			5		MΩ
Input Noise Voltage (f = 1KHz)	+25°C		9			9		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 4)	+25°C	50K	100K		25K	50K		V/V
	Full	25K			15K			V/V
* Common Mode Rejection Ratio (Note 8)	+25°C	80			80			dB
	Full	74			74			dB
Channel Separation (Note 5)	+25°C		−108			−108		dB
Small Signal Bandwidth	+25°C		3.5			3.5		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (R_L = 10K)	Full	±12	±13.7		±12	±13.7		V
(R_L = 2K)	Full	±10	±12.5		±10	±12.5		V
Full Power Bandwidth (Note 4)	+25°C		25			25		KHz
Output Current (Note 6)	Full	±5	±15		±5	±15		mA
Output Resistance	+25°C		300			300		Ω
TRANSIENT RESPONSE (Note 7)								
Rise Time	+25°C		75			75		ns
Overshoot	+25°C		25			25		%
Slew Rate	+25°C		±1.6			±1.6		V/µs
POWER SUPPLY CHARACTERISTICS								
* Supply Current (I^+ or I^-)	+25°C			5.0			7.0	mA
* Power Supply Rejection Ratio (Note 8)	Full	80			80			dB

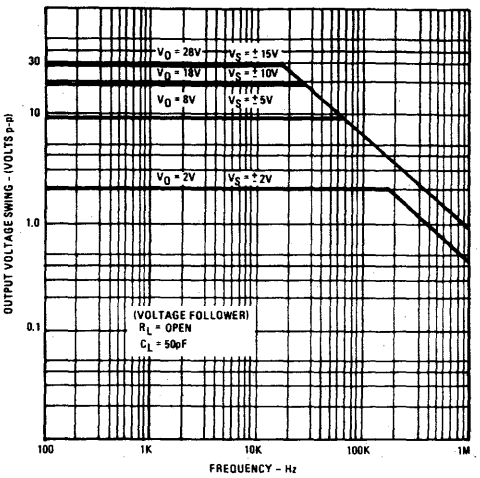
NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. One amplifier may be shorted to ground indefinitely.
3. Derate 5.8mW/°C above T_A = +25°C.
4. V_{OUT} = ±10, R_L = 2K
5. Referred to input; f = 10KHz, R_S = 1K
6. V_{OUT} = ±10
7. See pulse response characteristics
8. ΔV = ±5.0V

*100% Tested for DASH 8.

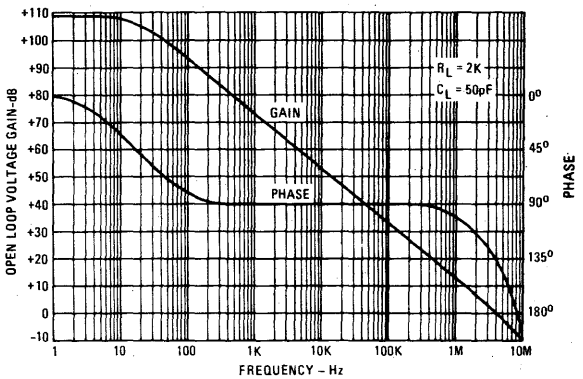
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$V+ = +15V$, $V- = -15V$, $T_A = +25^oC$
Unless Otherwise Stated.

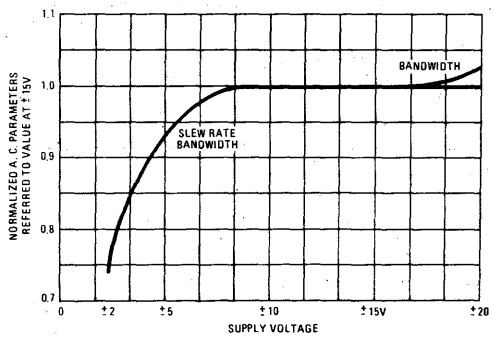
OUTPUT VOLTAGE SWING VS. FREQUENCY



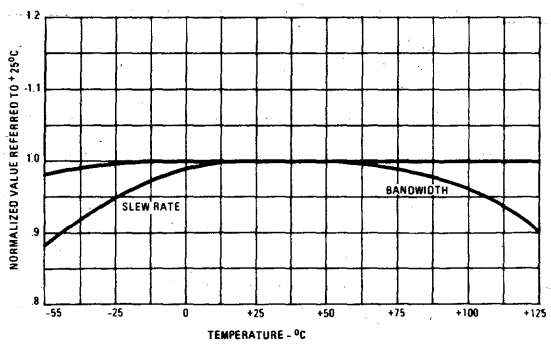
OPEN LOOP FREQUENCY RESPONSE



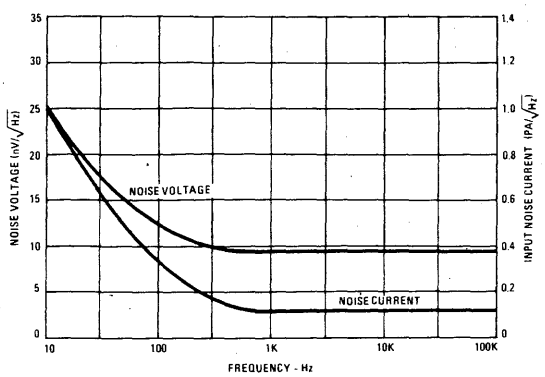
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



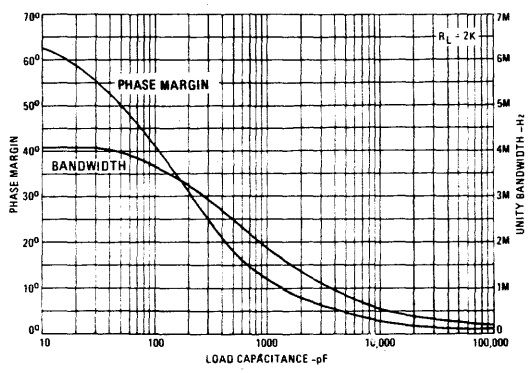
NORMALIZED AC PARAMETERS VS. TEMPERATURE



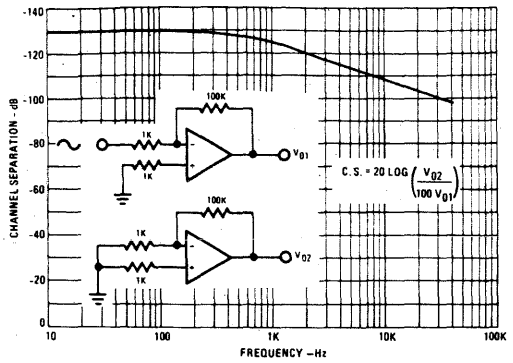
INPUT NOISE VS. FREQUENCY



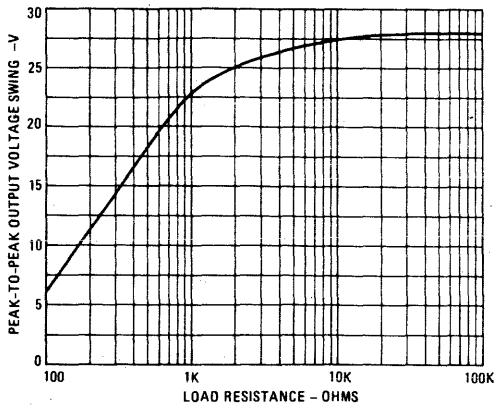
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



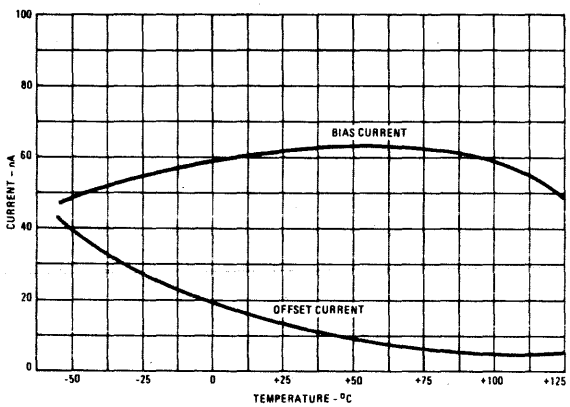
CHANNEL SEPARATION VS. FREQUENCY



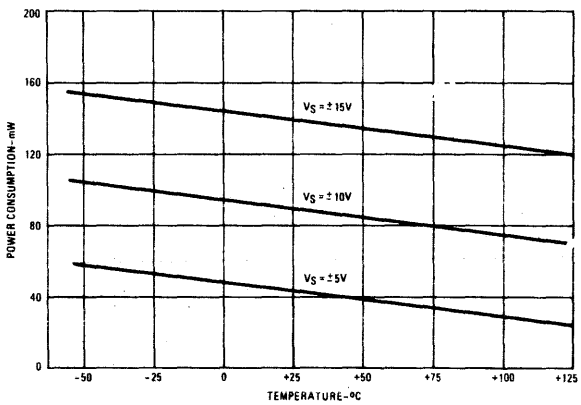
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE

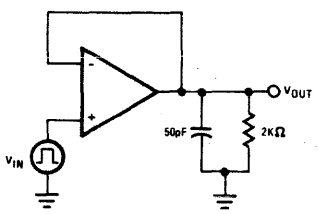


POWER CONSUMPTION VS. TEMPERATURE

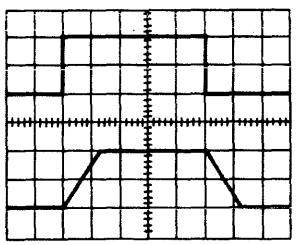


PULSE RESPONSE

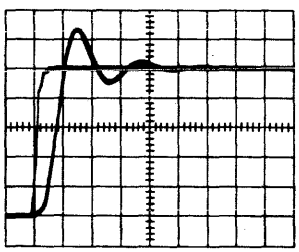
TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEW RESPONSE (Volts: 5V/Div, Time: 5 μs/Div)



TRANSIENT RESPONSE (Volts: 10mV/Div , Time: 100ns/Div)



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Harris Semiconductor
LINEAR

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-4900/4905

Precision Quad Comparator

FEATURES

- FAST RESPONSE TIME 130ns
- LOW OFFSET VOLTAGE 2.0mV
- LOW OFFSET CURRENT 10nA
- SINGLE OR DUAL-VOLTAGE SUPPLY OPERATION
- SELECTABLE OUTPUT LOGIC LEVELS
- ACTIVE PULL-UP/PULL-DOWN OUTPUT CIRCUIT - NO EXTERNAL RESISTORS REQUIRED

APPLICATIONS

- THRESHOLD DETECTOR
- ZERO-CROSSING DETECTOR
- WINDOW DETECTOR
- ANALOG INTERFACES FOR MICROPROCESSORS
- HIGH STABILITY OSCILLATORS
- LOGIC SYSTEM INTERFACES

DESCRIPTION

The HA-4900/4905 are monolithic, quad, precision comparators offering fast response time, low offset voltage, low offset current, and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. These comparators can sense signals at ground level while being operated from either a single +5 volt supply (digital systems) or from dual supplies (analog networks) up to ±15 volts. The HA-4900/4905 contains a unique current driven output stage which can be connected to logic system supplies (V_{Logic}+ and V_{Logic}-) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems, the design employed in the HA-4900/4905 input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

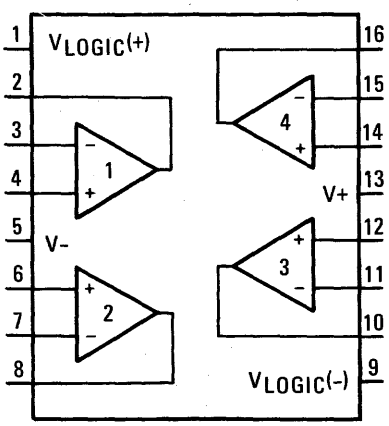
These comparators' combination of features makes them ideal components for signal detection and processing in data acquisition systems, test equipment, and microprocessor/analog signal interface networks.

Both devices are available in 16 pin dual-in-line ceramic packages. The HA-4900 operates from -55°C to +125°C and the HA-4905 operates over a 0°C to +75°C temperature range.

PIN OUT

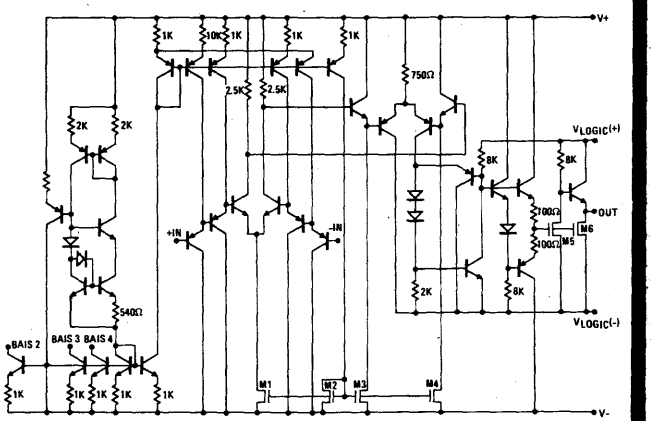
Package Code 4B

Top View



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SCHEMATIC



One Fourth Only (HA-4900/4905)

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V-	33V
Voltage Between $V_{Logic}(+)$ and $V_{Logic}(-)$	18V
Differential Input Voltage	±15V
Peak Output Current	±50mA
Internal Power Dissipation (Note 7, 8)	580mW
Storage Temperature Range	$-65^oC \leq T_A \leq 150^oC$

ELECTRICAL CHARACTERISTICS

V+ = +15.0V
V- = -15.0V
$V_{Logic}(+)$ = 5.0V
$V_{Logic}(-)$ = GND.

PARAMETER	TEMP.	HA-4900 -55°C to +125°C MIN.	HA-4900 -55°C to +125°C TYP.	HA-4900 -55°C to +125°C MAX.	HA-4905 0°C to +75°C MIN.	HA-4905 0°C to +75°C TYP.	HA-4905 0°C to +75°C MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage (Note 2)	25°C		2.0	3.0		4.0	7.5	mV
	Full			4.0			10.0	mV
* Offset Current	25°C		10	25		25	50	nA
	Full			35			70	nA
* Bias Current (Note 3)	25°C		50	75		100	150	nA
	Full			150			300	nA
Input Sensitivity (Note 4)	25°C			3.1			7.6	mV
	Full			4.1			10.1	mV
* Common Mode Range	Full	V-		V+ -2.4	V-		V+ -2.4	V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain	25°C		400K			400K		V/V
Response Time (T_{pd0}) (Note 5)	25°C		130			130		ns
Response Time (T_{pd1}) (Note 5)	25°C		180			180		ns
OUTPUT CHARACTERISTICS								
* Output Voltage Level								
Logic "Low State" (V_{OL}) (Note6)	Full		0.2	0.4		0.2	0.4	V
Logic "High State" (V_{OH}) (Note6)	Full	3.5	4.2		3.5	4.2		V
Output Current								
I_{Sink}	Full	3.5			3.5			mA
I_{Source}	Full	3.0			3.0			mA
POWER SUPPLY CHARACTERISTICS								
* Supply Current, $I_{ps}(+)$	25°C		6.5	12		7	13	mA
* Supply Current, $I_{ps}(-)$	25°C		4	6		5	7	mA
* Supply Current, I_{ps}(Logic)	25°C		1.7	2.0		1.7	2.5	mA
Supply Voltage Range								
V+	Full	+5.0		+15.0	+5.0		+15.0	V
V-	Full	-15.0		0	-15.0		0	V
$V_{Logic}(+)$ (Note 7)	Full	0		+15.0	0		+15.0	V
$V_{Logic}(-)$ (Note 7)	Full	-15.0		0	-15.0		0	V

*100% tested for HA1-4900-8.

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NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

2. Minimum differential input voltage required to ensure a defined output state.

3. Input bias currents are essentially constant with differential input voltages up to ±9 volts. With differential input voltages from ±9 to ±15 volts, bias current on the more negative input can rise to approximately 500 μA.

4. $R_S \leq 200$ ohms; $V_{in} \leq$ Common Mode Range. Input sensitivity is the worst case minimum differential input voltage required to guarantee a given output logic state. This parameter includes the effects of offset voltage, offset current, common mode rejection, and voltage gain.

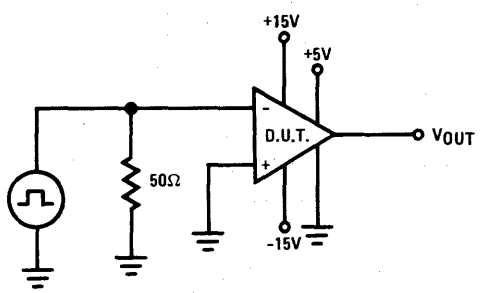
5. For $T_{pd}(1)$; 100mV input step,-5mV overdrive. For $T_{pd}(0)$; -100mV input step, 5mV overdrive. Frequency $\approx$ 100Hz; Duty Cycle $\approx$ 50%; Inverting input driven. See Test Circuit below.

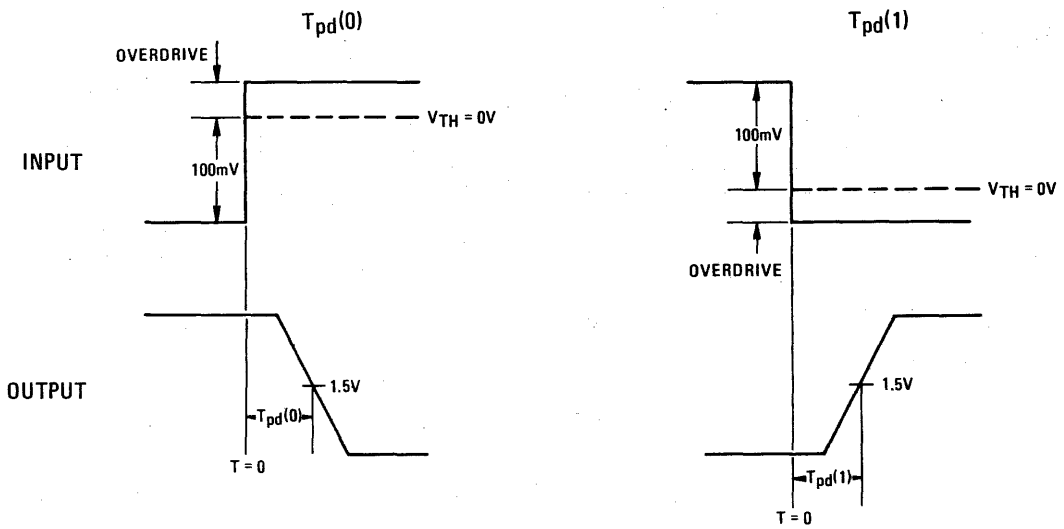
6. For V_{OH} and V_{OL}: I_{Sink} = 3.5mA, I_{Source} = 3.0mA. For other values of V_{Logic}; V_{OH} (min.) = V_{Logic} + -1.5V.

7. Total Power Dissipation (T.P.D.) is the sum of individual dissipation contributions of V+, V- and V_{Logic} shown in curves of Power Dissipation vs. Supply Voltages (see page 5). The calculated T.P.D. is then located on the graph of Maximum Allowable Package Dissipation vs. Ambient Temperature (see page 5) to determine ambient temperature operating limits imposed by the calculated T.P.D.. For instance, the combination of +15V, -15V, +5V, 0V (V+, V-, V_{Logic}^+, V_{Logic}^-) gives a T.P.D. of 350mW which allows operation to +125°C; the combination +15V, -15V, +15V, 0V gives a T.P.D. of 450mW and an operating limit of T_A = +95°C.

8. Derate by 5.8mW/°C above T_A = +75°C.

RESPONSE TIME TEST CIRCUITS



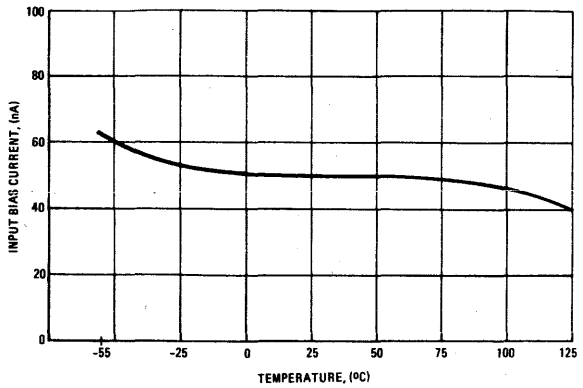


Input and output voltage waveforms for various input overdrives is shown on page 5 .

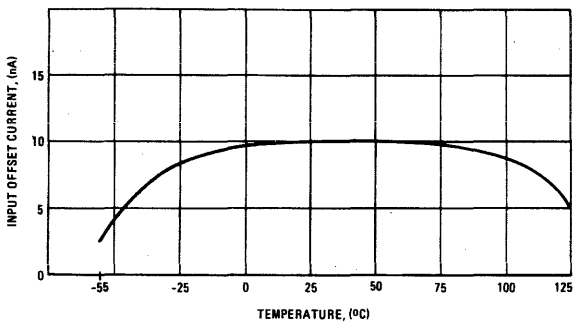
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V+ = 15V, V- = -15V, $V_{Logic}(+)$ = 5.0V, $V_{Logic}(-)$ = 0V, T_A = +25°C, Unless Otherwise Stated.

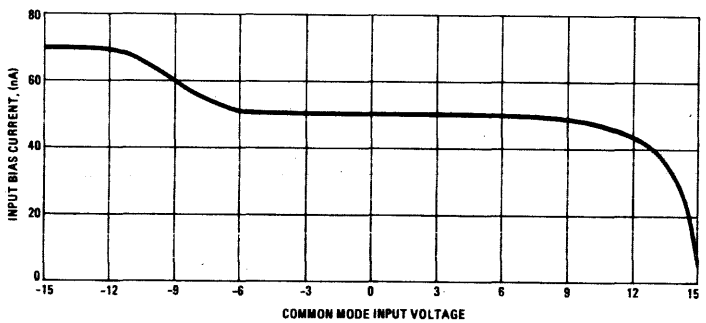
INPUT BIAS CURRENT vs. TEMPERATURE



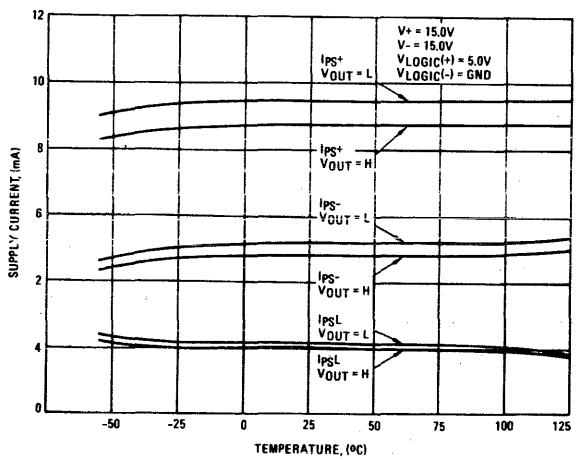
INPUT OFFSET CURRENT vs. TEMPERATURE



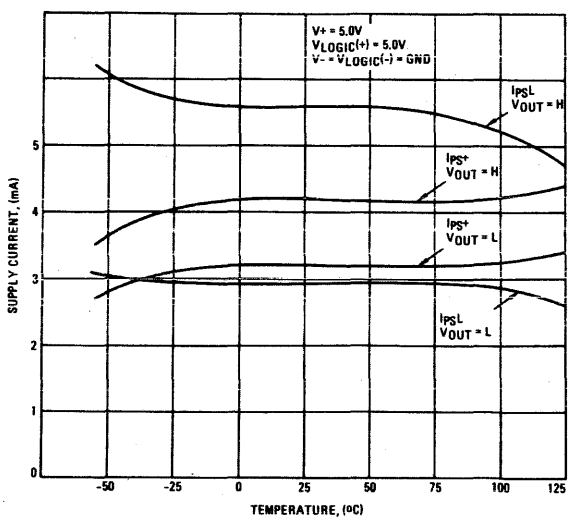
INPUT BIAS CURRENT vs. COMMON MODE INPUT VOLTAGE
($V_{DIFF.}$ = 0V)



SUPPLY CURRENT vs. TEMPERATURE
FOR ±15V SUPPLIES AND +5V LOGIC SUPPLY



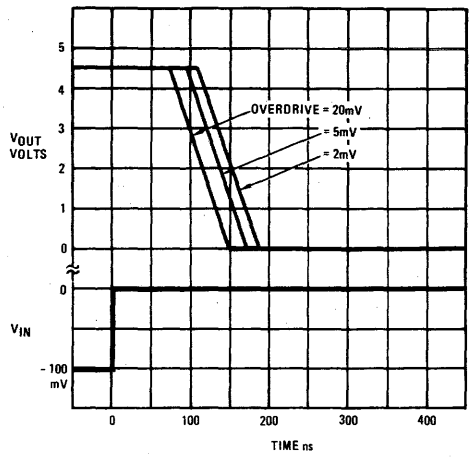
SUPPLY CURRENT vs. TEMPERATURE
FOR SINGLE +5V OPERATION

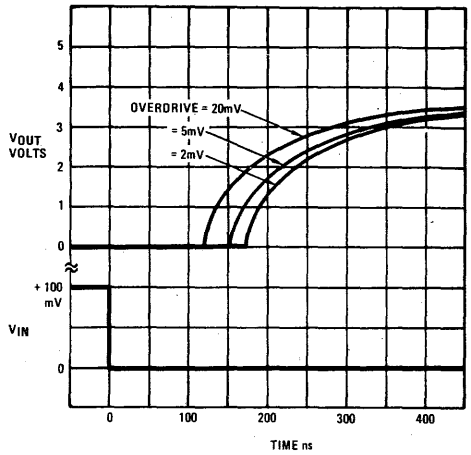


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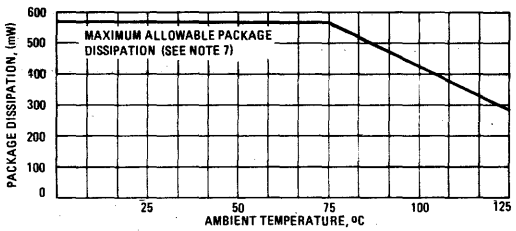
PERFORMANCE CURVES (continued)

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

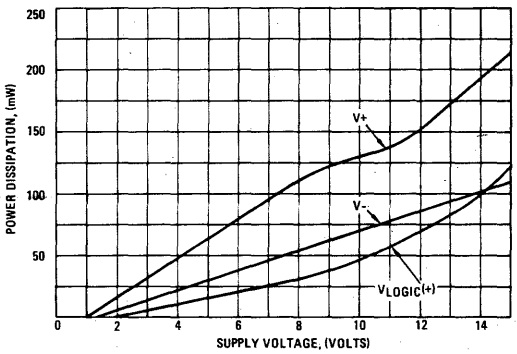




MAXIMUM PACKAGE DISSIPATION vs. $T_{AMBIENT}$



MAXIMUM POWER DISSIPATION vs. SUPPLY VOLTAGE (NO LOAD CONDITION)



APPLYING THE HA-4900/4905 COMPARATORS

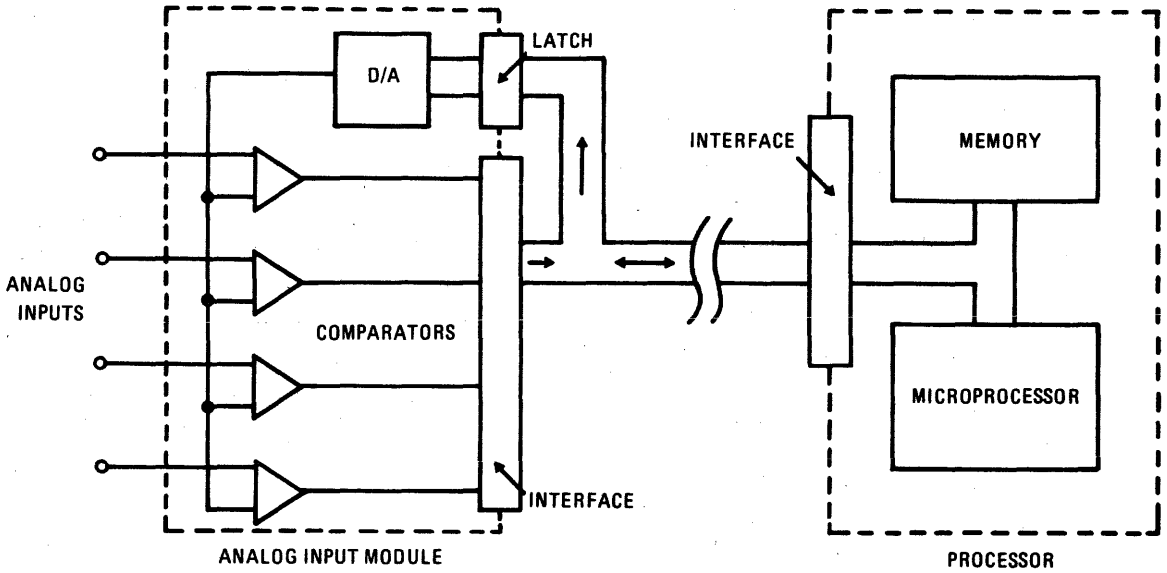
1. SUPPLY CONNECTIONS: This device is exceptionally versatile in working with most available power supplies. The voltage applied to the V+ and V- terminals determines the allowable input signal range; while the voltage applied to the V_L+ and V_L- determines the output swing. In systems where dual analog supplies are available, these would be connected to V+ and V-, while the logic supply and return would be connected to V_{Logic}+ and V_{Logic}-. The analog and logic supply commons can be connected together at one point in the system, since the comparator is immune to noise on the logic supply ground. A negative output swing may be obtained by connecting V_L+ to ground and V_L- to a negative supply. Bipolar output swings (15V P-P, max.) may be obtained using dual supplies. In systems where only a single logic supply is available (+5V to +15V), V+ and V_{Logic}+ may be connected together to the positive supply while V- and V_{Logic}- are grounded. If an input signal could swing negative with respect the V- terminal, a resistor should be connected in series with the input to limit input current to $< 5mA$ since the C-B junction of the input transistor would be forward biased.

2. UNUSED INPUTS: Inputs of unused comparator sections should be tied to a differential voltage source to prevent output "chatter".

3. CROSSTALK: Simultaneous high frequency operation of all other channels in the package will not affect the output logic state of a given channel, provided that its differential input voltage is sufficient to define a given logic state ($\Delta V_{IN} \geq \pm V_{OS}$). Low level or high impedance input lines should be shielded from other signal sources to reduce crosstalk and interference.

4. POWER SUPPLY DECOUPLING: Decouple all power supply lines with .01 μ F ceramic capacitors to a ground line located near the package to reduce coupling between channnels or from external sources.

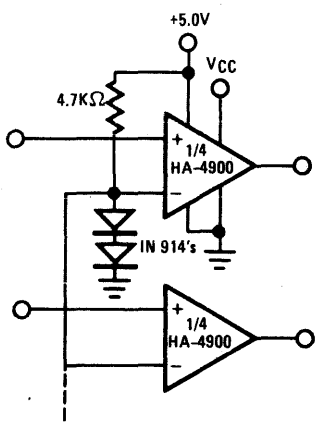
5. RESPONSE TIME: Fast rise time ($< 200ns$) input pulses of several volts amplitude may result in delay times somewhat longer than those illustrated for 100mV steps. Operating speed is optimized by limiting the maximum differential input voltage applied, with resistor-diode clamping networks.



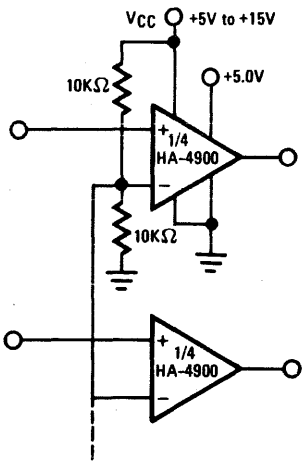
DATA ACQUISITION SYSTEM

In this circuit the HA-4900/4905 is used in conjunction with a D to A converter to form a simple, versatile, multi-channel analog input for a data acquisition system. In operation the processor first sends an address to the D to A, then the processor reads the digital word generated by the comparator outputs.

To perform a simple comparison, the processor sets the D to A to a given reference level, then examines one or more comparator outputs to determine if their inputs are above or below the reference. A window comparison consists of two such cycles with 2 reference levels set by the D to A. One way to digitize the inputs would be for the processor to increment the D to A in steps. The D to A address, as each comparator switches, is the digitized level of the input. While stairstepping the D to A is slower than successive approximation, all channels are digitized during one staircase ramp.



TTL TO CMOS



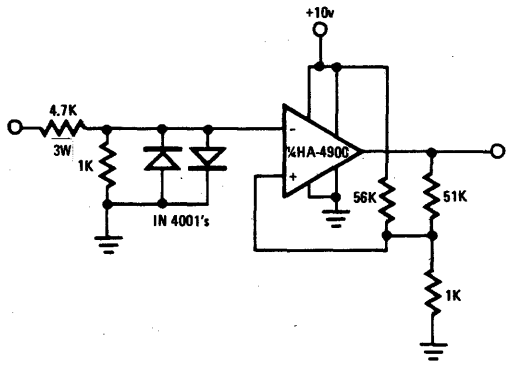
CMOS TO TTL

LOGIC LEVEL TRANSLATORS

The HA-4900/4905 comparators can be used as versatile logic interface devices as shown in the circuits above. Negative logic devices may also be interfaced with appropriate supply connections.

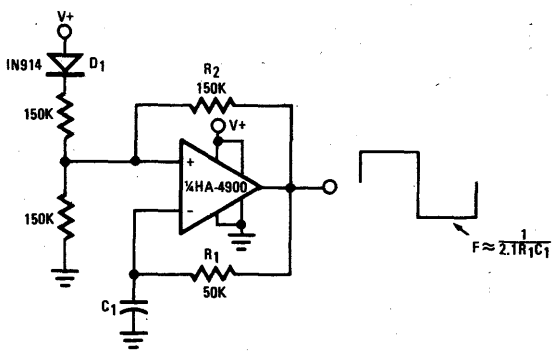
If separate supplies are used for V- and V_{Logic}-, these logic level translators will tolerate several volts of ground line differential noise.

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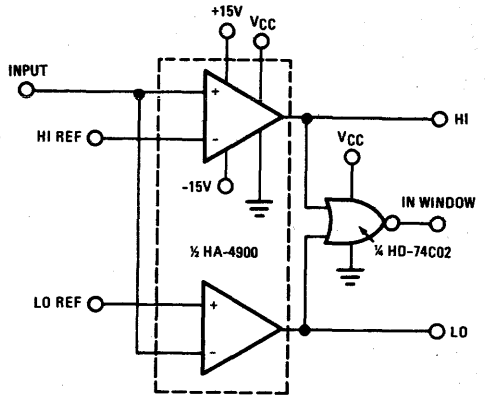
RS-232 TO CMOS LINE RECEIVER

This RS-232 type line receiver to drive CMOS logic uses a Schmitt trigger feedback network to give about 1 volt input hysteresis for added noise immunity. A possible problem in an interface which connects two equipments, each plugged into a different AC receptacle, is that the power line voltage may appear at the receiver input when the interface connection is made or broken. The two diodes and a 3 watt input resistor will protect the inputs under these conditions.



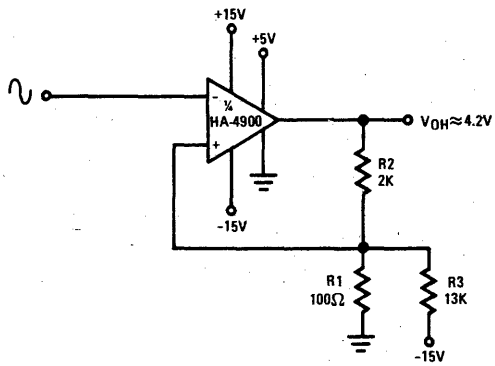
OSCILLATOR/CLOCK GENERATOR

This self-starting fixed frequency oscillator circuit gives excellent frequency stability. R_1 and C_1 comprise the frequency determining network while R_2 provides the regenerative feedback. Diode D_1 enhances the stability by compensating for the difference between V_{OH} and V_{Supply}. In applications where a precision clock generator up to 100kHz is required, such as in automatic test equipment, C_1 may be replaced by a crystal.



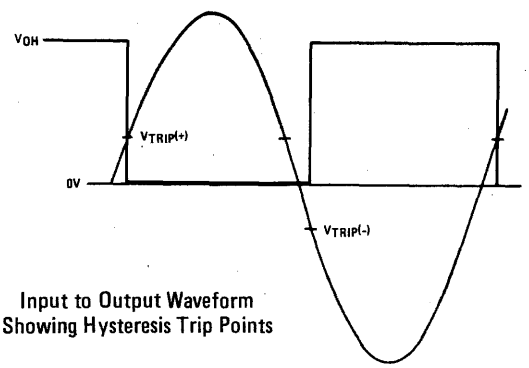
WINDOW DETECTOR

The high switching speed, low offset current and low offset voltage of the HA-4900/4905 makes this window detector circuit extremely well suited to applications requiring fast, accurate, decision-making. The circuit above is ideal for industrial process system feedback controllers or "out-of-limit" alarm indicators.



SCHMITT TRIGGER (ZERO CROSSING DETECTOR WITH HYSTERESIS)

This circuit has a 100mV hysteresis which can be used in applications where very fast transition times are required at the output even though the signal input is very slow. The hysteresis loop also reduces false triggering due to noise on the input. The waveforms below show the trip points developed by the hysteresis loop.



Input to Output Waveform
Showing Hysteresis Trip Points

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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2420/2425

Fast Sample and Hold Gated Operational Amplifier

FEATURES

- SAMPLE CURRENT/HOLD RATIO 10^6
- ACQUISITION TIME (0.01%) 5μs
- SLEW RATE 5V/μs
- BANDWIDTH 2MHz
- APERTURE DELAY 50ns
- LOW CHARGE TRANSFER 10pC
- DTL/TTL COMPATIBLE CONTROL INPUT

APPLICATIONS

- A TO D INPUT (TO 13 BITS)
- D TO A DEGLITCHER
- AUTO ZERO SYSTEMS
- PEAK DETECTOR
- GATED OP AMP

DESCRIPTION

The HA-2420/2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and a MOSFET input unity gain amplifier.

With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

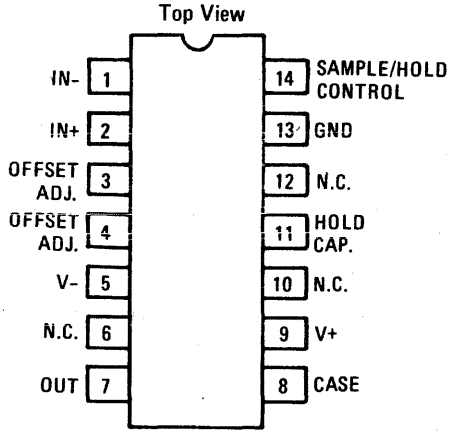
Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.

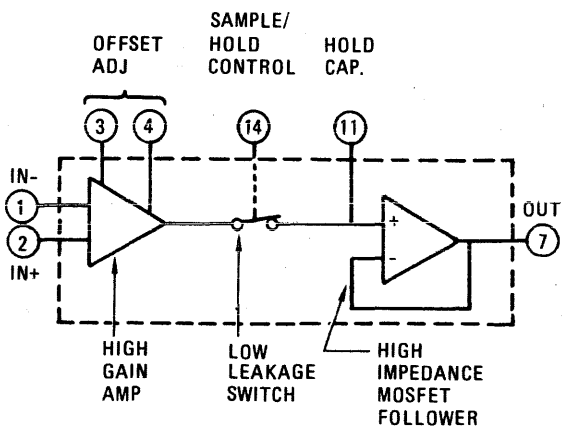
PINOUT

Package Code 4U

Top View



FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V	Internal Power Dissipation	300mW (Note 7)
Differential Input Voltage	±30V	Operating Temperature Range	
Digital Input Voltage (Pin 14)	+8V, -15V	HA-2420	$-55^{o}C \leq T_A \leq +125^{o}C$
Output Current	Short Circuit Protected	HA-2425	$0^{o}C \leq T_A \leq +75^{o}C$
		Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

Test Conditions $V_{Supply} = \pm 15.0V$, $C_H = 1000pF$ Unless Otherwise Specified. Digital Input (Pin 14) $V_{IL} = +0.8V$ (Sample), $V_{IH} = +2.0V$ (Hold)

PARAMETER	TEMP.	HA-2420 MIN.	HA-2420 TYP.	HA-2420 MAX.	HA-2425 MIN.	HA-2425 TYP.	HA-2425 MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		2	4		3	6	mV
	Full		3	6		4	8	mV
*Bias Current	+25°C		50	200		50	200	nA
	Full			400			400	nA
*Offset Current	+25°C		10	50		10	50	nA
	Full			100			100	nA
Input Resistance	+25°C	5	10		5	10		MΩ
Common Mode Range	Full	±10			±10			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 1, 4)	Full	25K	50K		25K	50K		V/V
*Common Mode Rejection (Note 2)	Full	80	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		2			2		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (Note 1)	Full	±10			±10			V
Output Current	+25°C	±10			±10			mA
Full Power Bandwidth (Note 3, 4)	+25°C		70			70		kHz
Output Resistance	+25°C		5			5		Ω
TRANSIENT RESPONSE								
Rise Time (Note 3, 5)	+25°C		100			100		ns
Overshoot (Note 3, 5)	+25°C		20			20		%
Slew Rate (Note 3, 6)	+25°C		5			5		V/μs
DIGITAL INPUT CHARACTERISTICS								
Digital Input Current (V_{IN} = 0V)	Full			0.8			0.8	mA
Digital Input Current (V_{IN} = +5.0V)	Full			20			20	μA
Digital Input Voltage (Low)	Full			0.8			0.8	V
Digital Input Voltage (High)	Full	2.0			2.0			V
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time to .1% 10V Step (3)	+25°C		4			4		μs
Acquisition Time to .01% 10V Step (3)	+25°C		5			5		μs
Aperture Delay	+25°C		50			50		ns
Aperture Uncertainty	+25°C		5			5		ns
* Drift Current	+25°C		5			5		pA
	Full		0.5	10		.05	1.0	nA
* Charge Transfer	+25°C		10	20		10	20	pC
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		2.5	5.0		2.5	5.0	mA
* Power Supply Rejection Ratio	Full	80	90		74	90		dB

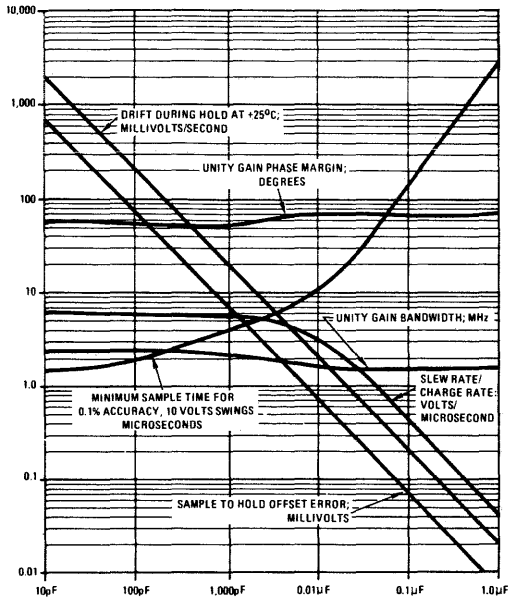
NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 10VDC$
3. $A_V = +1$, $R_L = 2K\Omega$, $C_L = 50pF$
4. V_{OUT} = 20V peak-to-peak
5. V_{OUT} = 400mV peak-to-peak
6. V_{OUT} = 10.0V peak-to-peak
7. Derate Power Dissipation by 4.3mW/°C above +105°C Ambient Temperature.

*100% Tested For DASH 8

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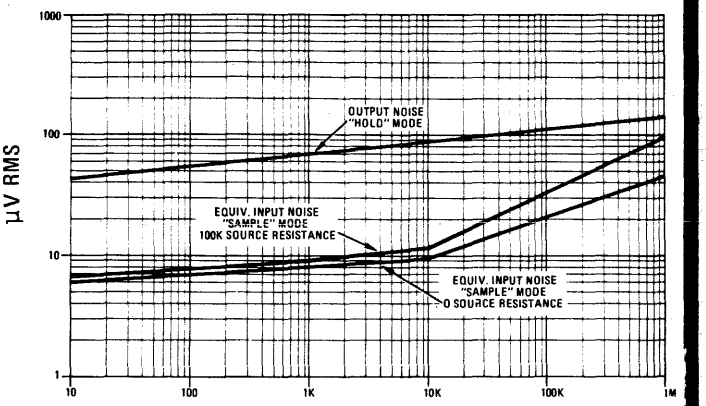
V_{SUPPLY} = ±15VDC, T_A = +25°C, C_H = 1,000pF UNLESS OTHERWISE SPECIFIED

TYPICAL SAMPLE-AND-HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITANCE



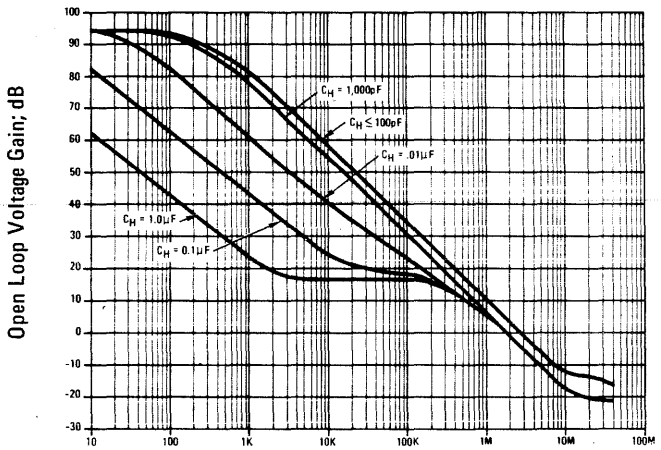
C_H Value

BROADBAND NOISE CHARACTERISTICS



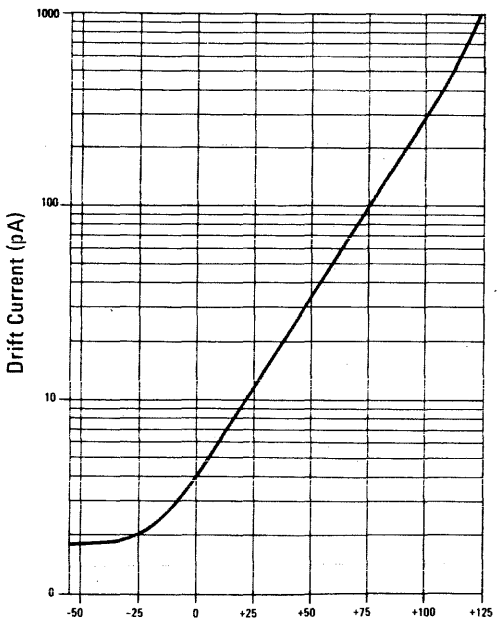
Bandwidth
(Lower 3db Frequency = 10Hz)

OPEN LOOP FREQUENCY RESPONSE



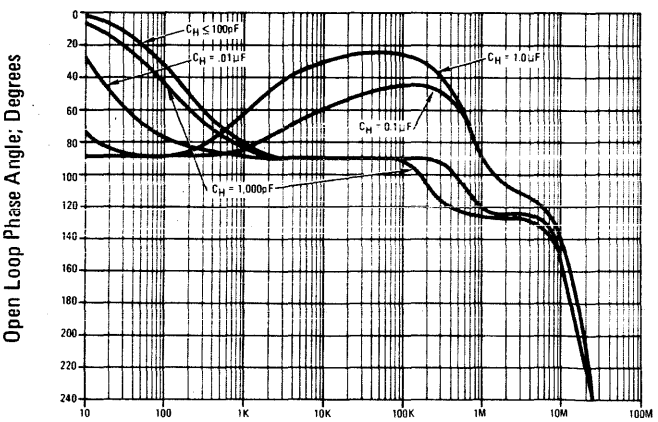
Frequency, Hz

DRIFT CURRENT vs TEMPERATURE



Temperature, (Degrees C)

OPEN LOOP PHASE RESPONSE



Frequency, Hz

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APPLICATIONS

BASIC SAMPLE-AND-HOLD

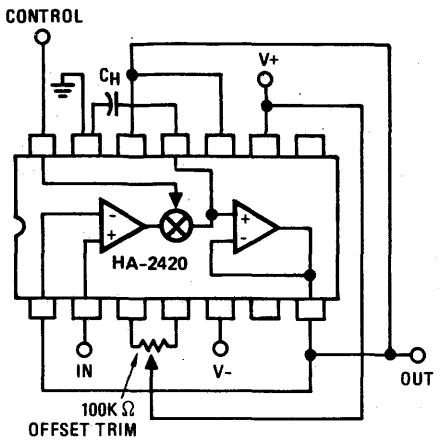


Figure 1

GUARD RING LAYOUT (BOTTOM VIEW)

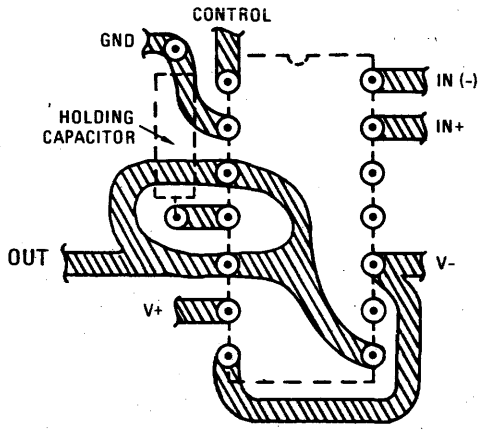


Figure 2

NOTES:
1) Figure 1 shows a typical unity gain circuit, with offset zeroing. All of the other normal op amp feedback configurations may be used with the HA-2420/2425. The input amplifier may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.
2) The method used to reduce leakage paths on the P.C. board and the device package is shown in Figure 2. This guard ring is recommended to minimize the drift during hold characteristic.
3) The holding capacitor should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below +85°C), Teflon, or Parlene types are recommended.

For more applications, consult Harris Application Note 517.

GLOSSARY OF TERMS

ACQUISITION TIME:
The time required by the device after the "sample" command to reach its final value within ±0.1% or ±0.01%. This time includes switch delay time, slewing time and settling time. This is the minimum sample time required to obtain a given accuracy.

CHARGE TRANSFER:
The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the Hold mode. Sample-to-Hold offset error is directly proportional to this charge, where:

$$\text{Offset Error (V)} = \frac{\text{Charge (pC)}}{C_H(\text{pF})}$$

APERTURE DELAY:
The time required after the "hold" command until the switch is fully open. This delays the effective sample timing with rapidly changing input signals.

DRIFT CURRENT:
Leakage currents from the holding capacitor during the Hold mode which cause the output voltage to drift. Drift rate (droop rate) can be calculated from drift current values using the formula:

$$\frac{\Delta V}{\Delta T}\,(\text{Volts/Sec}) = \frac{I(\text{pA})}{C_H(\text{pF})}$$

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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2820/2825

Phase Locked Loop

FEATURES

- FREQUENCY RANGE 0.01Hz tTO 3MHz
- INDEPENDENT PHASE DETECTOR AND OSCILLATOR FOR VERSATILITY
- TWO ISOLATED PHASE DETECTOR OUTPUTS
- DTL/TTL COMPATIBLE OSCILLATOR OUTPUT

APPLICATIONS

- DISCRIMINATORS
- RECEIVERS
- DATA DECODERS (DATA MODEMS)
- DATA SYNCHRONIZERS

DESCRIPTION

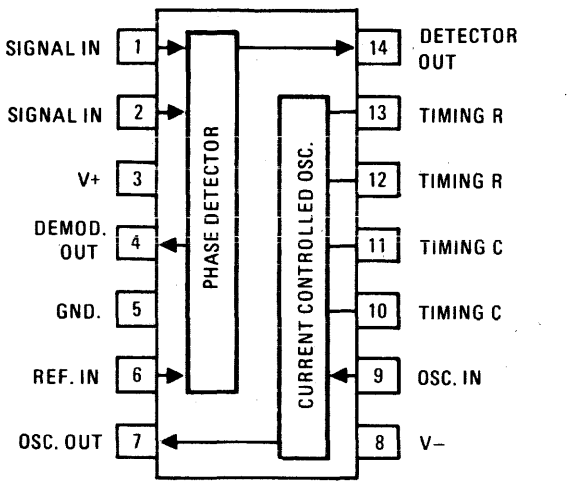
The HA-2820/2825 Phase Locked Loop is useful for many operations in the frequency domain in the sub-audio to low R. F. bands. It features a number of functional and parametric improvements over other similar monolithic circuits.

A major feature is a high impedance current source phase detector output with provisions for external connection to the oscillator input which is a low impedance current sink. This allows connection of complex passive or active filters, amplifiers, sweep circuits, etc. within the loop. Also, the two phase detector outputs are isolated from one another so that different filter functions can be connected at the two outputs without interaction. The capability of independently adjusting loop bandwidth allows phase modulation detectors to be constructed.

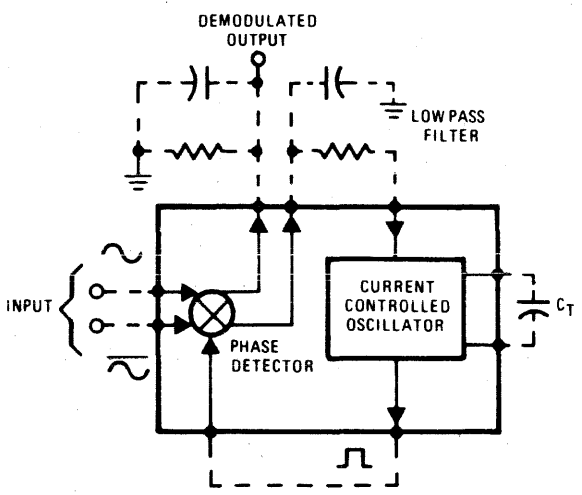
Applications include modulators and demodulators for F.M., phase modulation, and F.S.K.. frequency multiplication; data synchronization. tracking filters. and speed controls.

PINOUT

Top View — Package Code 4U



FUNCTIONAL DIAGRAM



SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	27.0V	Power Dissipation	300mW (Note 3)
Input Voltage	2 VRMS	Operating Temperature	
		HA-2820	$-55^{o}C > T_A > +125^{o}C$
		HA-2825	$0^{o}C > T_A > +75^{o}C$
Output Current, Pin 7	10mA	Storage Temperature	$-65^{o}C > T_A > +150^{o}C$

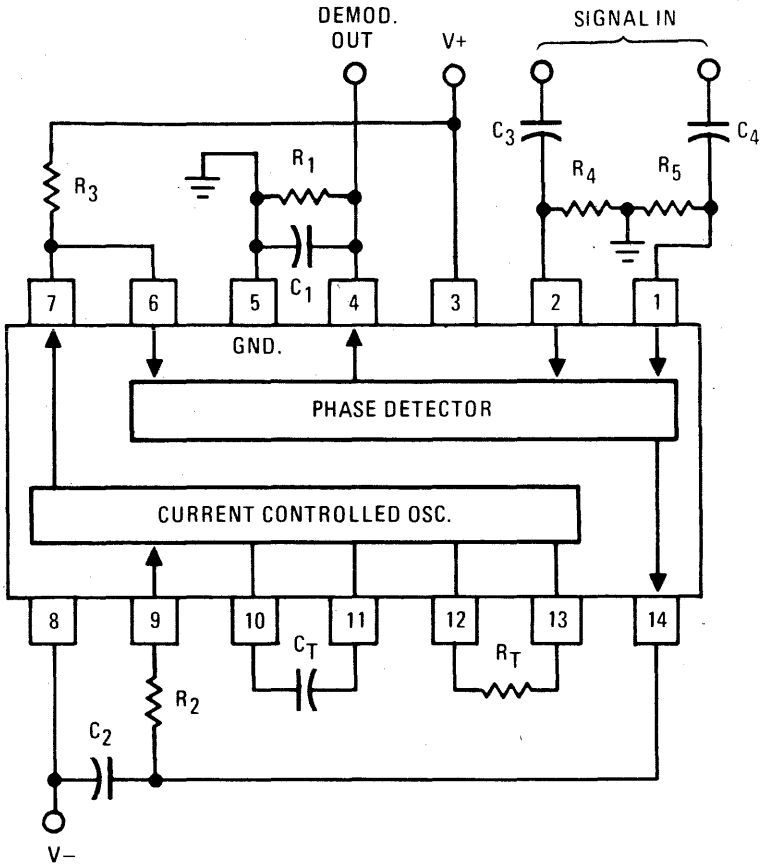
ELECTRICAL CHARACTERISTICS

V+ = +6.0V, V- = -6.0V, Pin 5 = Ground; V_{IN} = 100mV RMS, $F_O \approx$ 50kHz, See Test Circuit, Page 3. Unless otherwise specified

PARAMETER	TEMP.	HA-2820 -55°C to +125°C LIMITS MIN.	HA-2820 TYP.	HA-2820 MAX.	HA-2825 0°C to +75°C LIMITS MIN.	HA-2825 TYP.	HA-2825 MAX.	UNITS
PHASE DETECTOR								
Input Impedance, Pins 1 - 2	+25°C		100K			100K		Ω
Input Voltage Range, Pins 1 - 2 (Note 1)	Full	10	5		10	5		mV RMS
Output Impedance, Pins 4 & 14	+25°C		10			10		MΩ
Output Offset Current, Pins 4 & 14	+25°C		10	15		10	15	μA
Output Offset Current, Pins 4 & 14	Full			20			20	μA
Conversion Gain, Pins 4 & 14	+25°C		50			50		μA/Radian
CURRENT CONTROLLED OSCILLATOR								
Maximum Frequency	Full	3	5		3	5		MHz
Frequency Drift	Full		200			200		ppm/°C
Frequency Change with Supply Voltage (Note 4)	Full		.01			.01		%/V
Input Resistance, Pin 9	+25°C		500			500		Ω
Input Open Circuit Voltage, Pin 9	+25°C		-3.5			-3.5		V
Conversion Gain	+25°C		1.0			1.0		% Δf/μA
Output Voltage, High	+25°C	+1.9			+1.9			V
Output Voltage, Low	+25°C			+0.4			+0.4	V
Output Rise Time	+25°C		100			100		ns
Output Fall Time	+25°C		125			125		ns
CLOSED LOOP CHARACTERISTICS								
Loop Gain	+25°C		50			50		% Δf/Radian
Tracking Range	+25°C		50			50		%Δf
Demod. Output Swing, Pin 4 (Note 5)	+25°C		±700			±700		mV
Frequency Drift	Full		200			200		ppm/°C
POWER SUPPLY CHARACTERISTICS								
Supply Current, V+	Full		3	5		3	5	mA
Supply Current, V-	Full		7	10		7	10	mA
Supply Voltage Range (Notes 2, 3)	Full	±6		±12	±6		±12	V

NOTES
1. For ± 10% Tracking range.
2. +5.0V,-7.0V may be used alternatively.
3. Derate power dissipation by 6.6mW/°C above +105°C ambient temperature.
4. $\Delta V_S = \pm 2V$
5. When not in use pin 4 should be grounded.

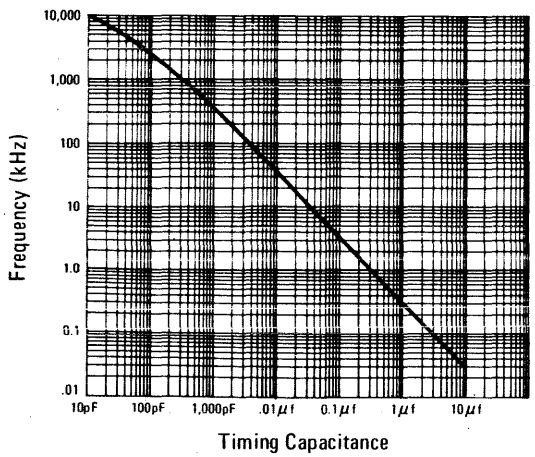
TEST CIRCUIT



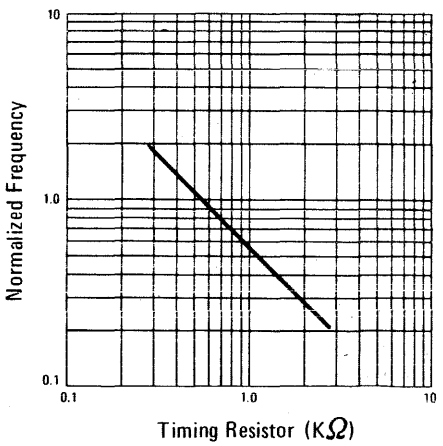
Unless otherwise specified: V+ = +6.0V; V- = -6.0V; $R_1 = R_3 = 10K\Omega$; $R_2 = 1K\Omega$; $R_4 = R_5 = 300\Omega$; $R_T = 540\Omega$; $C_1 = .015\mu f$; $C_2 = C_3 = C_4 = 0.1\mu f$; $C_T = 0.01\mu f$ ($f_o \approx 50kHz$); $V_{IN} = 100mV$ RMS; $T_A = +25^oC$

PERFORMANCE CURVES

CENTER FREQUENCY, f_o vs. TIMING CAPACITOR, C_T ($R_T = 540\Omega$)



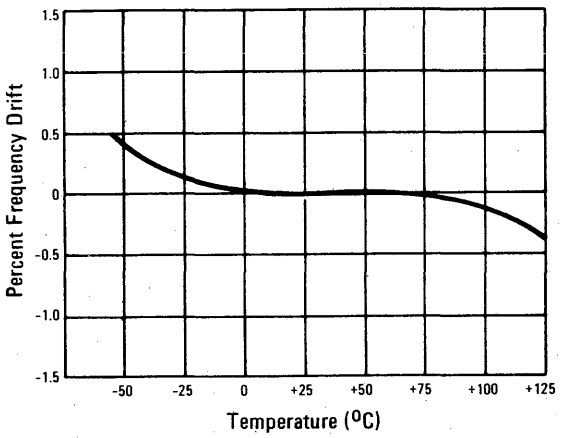
CENTER FREQUENCY, f_o vs. TIMING RESISTOR, R_T ($C_T = .01\mu f$)



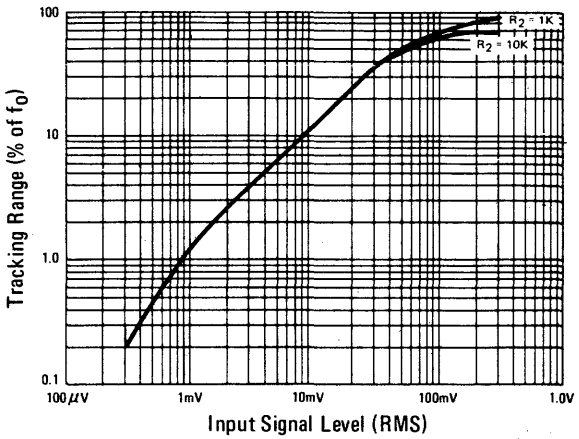
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PERFORMANCE CURVES (continued)

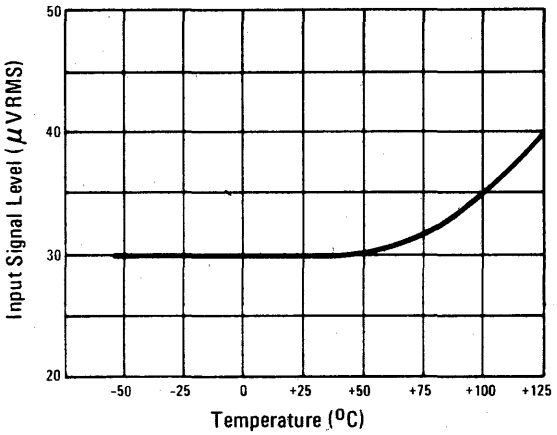
CENTER FREQUENCY DRIFT vs. TEMPERATURE



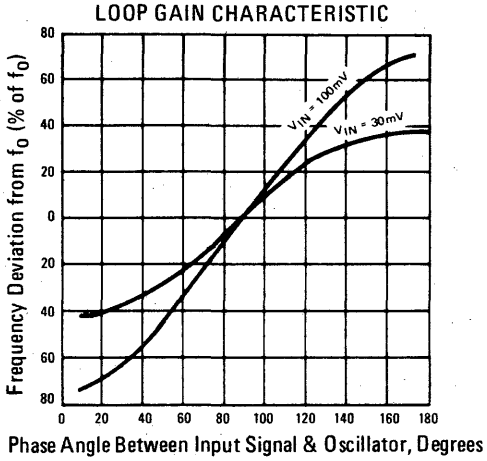
TRACKING RANGE vs. INPUT SIGNAL LEVEL



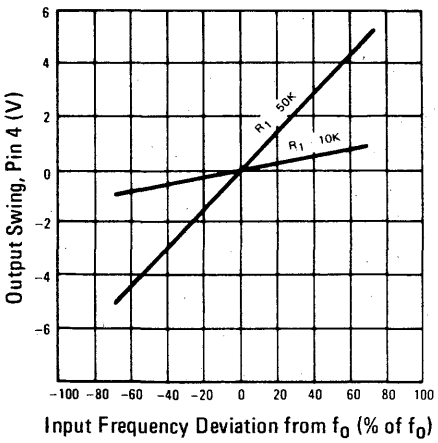
MINIMUM SIGNAL TO MAINTAIN LOCK



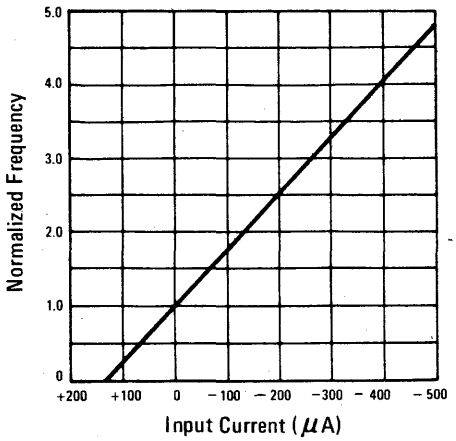
LOOP GAIN CHARACTERISTIC



DEMODULATED OUTPUT SWING



OSCILLATOR FREQUENCY vs. INPUT CURRENT, PIN 9 (f_0 = 50kHz)



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HC-55516/55532

All-Digital Continuously Variable Slope Delta Modulator (CVSD)

FEATURES

- REQUIRES FEWER EXTERNAL PARTS
- LOW POWER DRAIN: 6mW FROM SINGLE 5V-7V SUPPLY
- TIME CONSTANTS DETERMINED BY CLOCK FREQUENCY; NO CALIBRATION OR DRIFT PROBLEMS; AUTOMATIC OFFSET ADJUSTMENT
- HALF DUPLEX OPERATION BY DIGITAL CONTROL
- FILTER RESET BY DIGITAL CONTROL
- AUTOMATIC OVERLOAD RECOVERY
- AUTOMATIC "QUIET" PATTERN GENERATION
- AGC CONTROL SIGNAL AVAILABLE

APPLICATIONS

- VOICE TRANSMISSION OVER DATA CHANNELS
- VOICE ENCRYPTION/SCRAMBLING
- VOICE I/O FOR DIGITAL SYSTEMS
- AUDIO MANIPULATIONS: DELAY LINES, TIME COMPRESSION, ECHO GENERATION/ SURPRESSION, SPECIAL EFFECTS, ETC.

DESCRIPTION

The HC-55516 and HC-55532 are half duplex modulator/ demodulator CMOS integrated circuits used to convert voice signals into serial NRZ digital data, and to reconvert that data into voice. The conversion is by delta modulation, using the continuously variable slope (CVSD) method of companding.

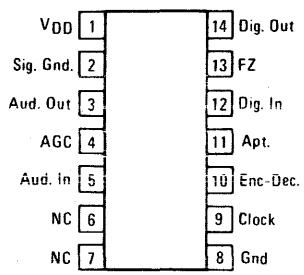
While signals are compatible with other CVSD circuits, internal design is unique. The analog loop filters have been replaced by digital filters, using very low power, and requiring no external timing components. This approach allows inclusion of many desirable features which would be difficult to implement using other approaches.

The HC-55516 has internal time constants optimized for 16K bits/sec data rate and is usable down to 9K bits/sec. The HC-55532 is optimized for 32K bits/sec and is usable beyond 64K bits/sec. Both units are available in 14 pin D.I.P. (HC1) or flat packages (HC9) in two temperature ranges; -55°C to +125°C (-2 or -8) and -40°C to +85°C (-9).

PINOUT

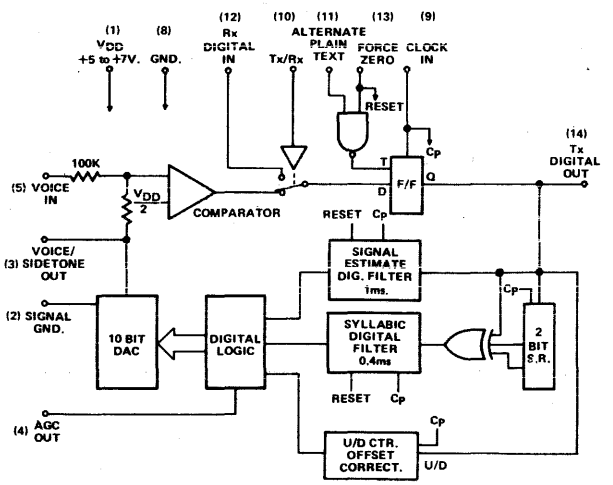
Package Code 9R, 4Q

Top View



14 PIN D.I.P. AND FLAT PACK

FUNCTIONAL DIAGRAM



SEE PAGES 759-762 FOR PACKAGE SELECTION GUIDE

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PIN # 14-LEAD F.P. & D.I.P.	SYMBOL	ACTIVE* LEVEL	DESCRIPTION
1	V_{DD}		Positive supply voltage.
2	Sig. Gnd.		Ground connection to D/A ladders and comparator; i.e. audio ground.
3	Aud. Out		Recovered audio out. May be used as side tone at the transmitter. Presents approximately 100 kilohm source. Zero signal reference is $V_{DD}/2$.
4	AGC		A logic "Low" level will appear at this output when the recovered signal excursion reaches one-half of full scale value.
5	Aud. In		Audio input. Should be externally AC coupled. Presents approximately 100 kilohms in series with $V_{DD}/2$.
6,7			No internal connection is made to these pins.
8	Gnd.		Logic ground. Negative supply voltage.
9	Clock		Receiver clock must be phased with digital input such that a positive clock transition occurs near the middle of each received data bit.
10	Encode (Decode)	Low (High)	A single CVSD can provide half-duplex operation. The encode and decode functions are selected by the logic level applied to this input. A low level selects the encode mode, a high level, the decode mode.
11	APT.	Low	Activating this input causes an "alternate plain text" (quieting pattern) to be transmitted without affecting the internal operation of the CVSD.
12	Dig. In		Input for the received digital data.
13	FZ	Low	Activating this input forces the transmitted output, the internal logic, and the recovered audio output into the "quieting" condition.
14	Dig. Out		Output for transmitted digital data.

*Note: No active input should be left in a "floating condition".

ABSOLUTE MAXIMUM RATINGS

Voltage At Any Pin	-3.0V to V_{DD} +0.3V	Operating Temperature (-9)	-40°C to +85°C
		(-2)	-55°C to +125°C
Maximum V_{DD} Voltage	+7.0V	(-8)	-55°C to +125°C
Operating V_{DD} Range	+5.0V to +7.0V	Storage Temperature	-65°C to +150°C

ELECTRICAL CHARACTERISTICS @ T_A = 25°C

Test Conditions V_{DD} = 6.0V, Bit Rate = 16Kb/s, (HC-55516)
Bit Rate = 32Kb/s, (HC-55532)

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Clock Bit Rate	0		64	Kb/s	(1)
Clock Duty Cycle	30		70	%	
Supply Voltage	+5.0		+7.0	V	
Supply Current		1.0		mA	
Digital "1" Input		4.5		V	(2)
Digital "0" Input		1.5		V	(2)
Digital "1" Output		5.5		V	(3)
Digital "0" Output		0.5		V	(3)
Audio Input Voltage		0.5	1.4	Vrms	(4)
Audio Output Voltage		0.5	1.4	Vrms	(5)
Audio Input Impedance		100		KΩ	(6)
Audio Output Impedance		100		KΩ	(7)
Transfer Gain	-0.5		+0.5	dB	(8)
Syllabic Time Constant		4.0		mS	(9)
L.P. Filter Time Constant (55516)		0.94		mS	(9)
(55532)		0.47		mS	
Step Size Ratio (55516)		24		dB	(10)
(55532)		18		dB	
Resolution (55516)		0.1		%	(11)
(55532)		0.2		%	
Min. Step Size (55516)		0.2		%	(12)
(55532)		0.4		%	
Slope Overload		Fig. 1			(13)
Signal/Noise Ratio			Tab. 1		(14)
Quieting Pattern Amplitude (55516)		12		mV P-P	(15)
(55532)		24		mV P-P	
AGC Threshold		0.5		F.S.	(16)
Clamping Threshold		0.75		F.S.	(17)

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1. There is one NRZ data bit per clock period. Clock must be phased with digital data such that a positive clock transition occurs in the middle of each received data bit; i.e., the transmitter and receiver clock are in phase.

2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.

3. Logic outputs are CMOS compatible at supply voltage and withstand short-circuits to V_{DD} or ground. Digital data output is NRZ and changes with negative clock transitions.

4. Recommended voice input range for best voice performance.

5. May be used for side-tone in encode mode.

6. Should be externally AC coupled. Presents 100 Kilohms in series with $V_{DD}/2$.

7. Presents 100 Kilohms in series with recovered audio voltage. Zero-signal references is $V_{DD}/2$.

8. Unloaded, for linear signals.

9. Note that filter time constants are inversely proportional to clock rate.

10. Step size compression ratio of the syllabic filter is defined as the ratio of the filter output, with an equal 1-0 bit density input to the filter, to its minimum output.

11. Minimum quantization voltage level expressed as a percentage of supply voltage.

12. The minimum step size between levels is twice the resolution.

13. For large signal amplitudes or high frequencies, the encoder may become slope-overloaded. Figure 1 shows the frequency response at various signal levels,measured with a 3kHz low-pass filter having a 130dB/octave roll-off to -50dB. See Table II.

14. Table I shows the SNR under various conditions, using the output filter described in 13 (above) at a bit rate of 16Kb/s. See Table II.

15. The "quieting" pattern or idle-channel audio output steps at one-half the bit rate, changing state on negative clock transitions.

16. A logic "0" will appear at the AGC output pin when the recovered signal reaches one-half of full-scale value (positive or negative).

17. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

TABLE I

INPUT FREQUENCY Hz	INPUT AMPLITUDE mV RMS	OUTPUT SNR dB MIN.
300	1400	20
300	45	15
1000	500	14
1000	16	9

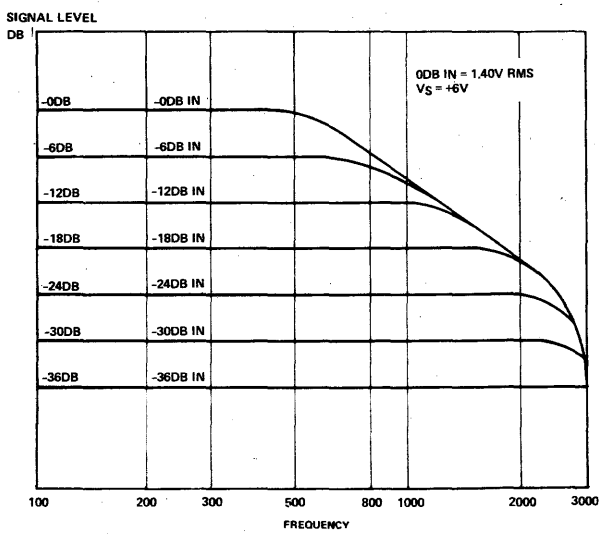


Figure 1 — Transfer Function for CVSD at 16KB

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TABLE II

INPUT FILTER FREQUENCY RESPONSE		OUTPUT FILTER FREQUENCY RESPONSE	
FREQUENCY	RELATIVE OUTPUT	FREQUENCY	RELATIVE OUTPUT
100Hz	0±0.5dB	100Hz to 1500Hz	0±1.5dB
200Hz	0±0.1dB	1500Hz to 3000Hz	0±2.5dB
1000Hz	0±0.1dB	3800Hz to 100KHz	Less Than -45dB
3000Hz	-3±0.5dB		
9000Hz	-20±2.0dB		

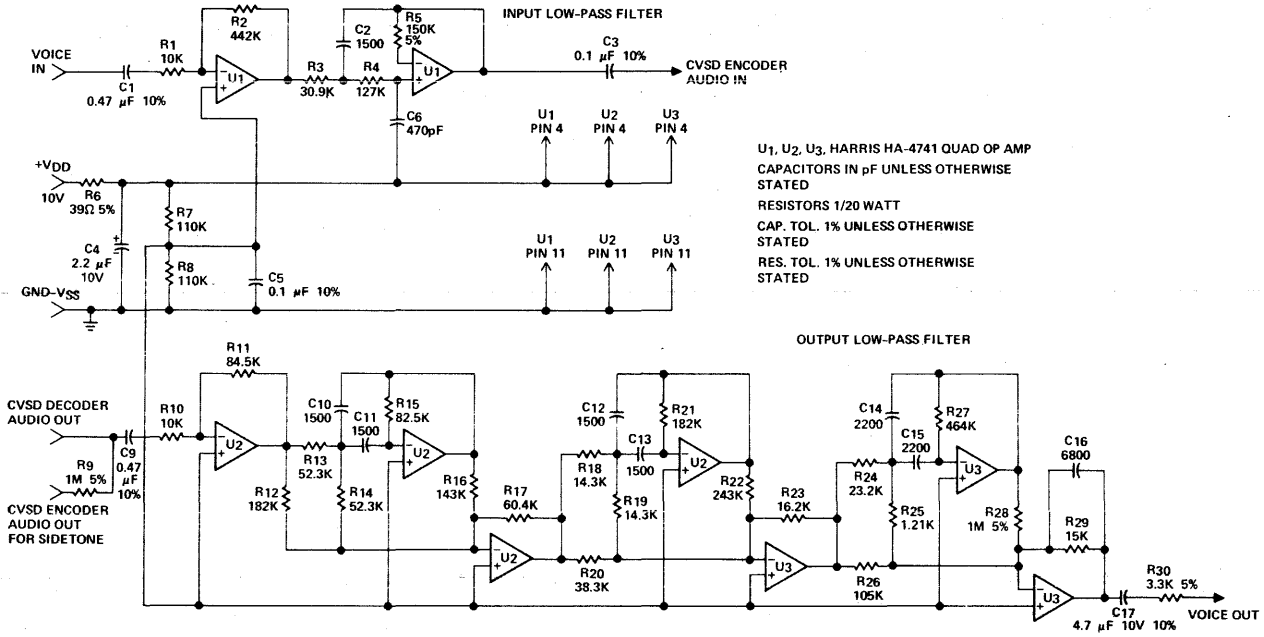


Figure 2 – Suggested Input/Output Audio Filters for SNR Measurement

NOTE: An output filter similar to the input filter section above will generally suffice for good voice intelligibility.

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HARRIS SEMICONDUCTOR
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Harris Package Selection Guide

PART NUMBER	PACKAGE CODE (See Note)		
	CAN	FLATPACK	D.I.P.
HA-909/911	2A	9V	
HA-2050/2055/2050A/2055A	2A		
HA-2060/2065/2060A/2065A	2A		
HA-2400/2404/2405			4B
HA-2420/2425			4U
HA-2500/2502/2505	2A		
HA-2510/2512/2515	2A	9V*	
HA-2520/2522/2525	2A	9V*	
HA-2530/2535	2A		
HA-2600/2602/2605	2A	9W*	
HA-2620/2622/2625	2A		4U
HA-2630/2635	2G		
HA-2640/2645	2A		
HA-2650/2655	2A		4U
HA-2700/2704/2705	2A		4U
HA-2720/2725	2A		
HA-2730/2735			4U
HA-2820/2825			4U
HA-2900/2904/2905	2E		
HA-4602/4605			4U
HA-4741			4U, 3B†
HA-4900/4905			4B
HC-55516/55532		9R	4Q
HD-0165			4K
HD-245/545		9V	1S
HD-246/546/249/549		9V	1S
HD-248/548		9V	1S
HI-200	2D		
HI-201			4B
HI-506/507/506A/507A			1M
HI-508A/509A			4B
HI-562			1H
HI-1080/1085			4K
HI-1800A			4B
HI-1818A/1828A			4B
HI-1840			1M
HI-5040 thru HI-5051			4B

NOTE: "Package Code" references drawings on the following pages. Note that these do not correspond with the general package designations to be used in constructing the part number, which is explained in Ordering Information at the front of this book.

* Flatpack not available for commercial temperature range.

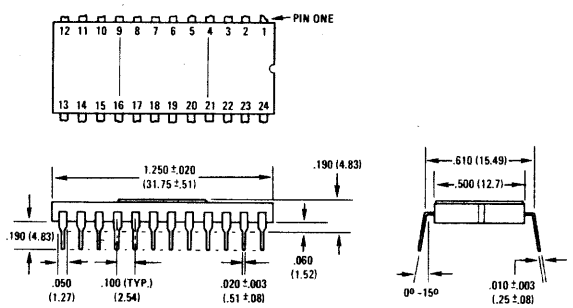
† 3B (Plastic D.I.P.) not available for military temperature range.

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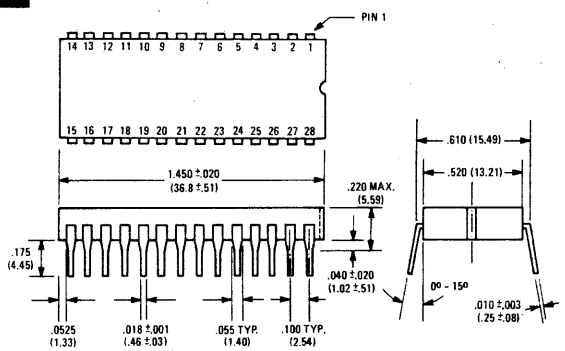
Package Dimensions

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.
3. Package codes are shown in black squares.

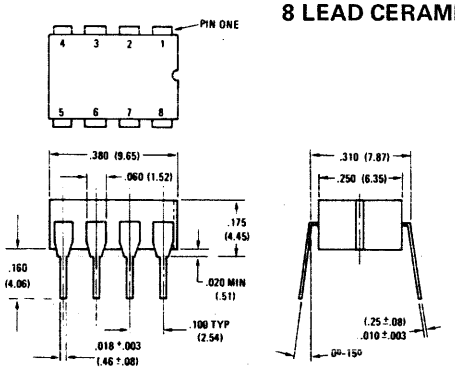
1H — 24 LEAD D.I.P.



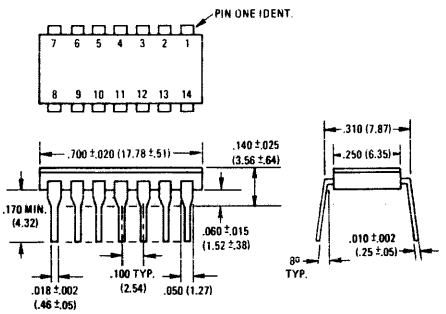
1M — 28 LEAD CERAMIC D.I.P.



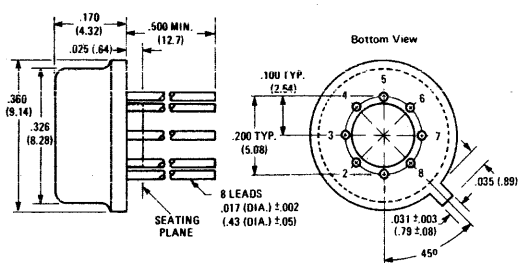
1N — 8 LEAD CERAMIC D.I.P.



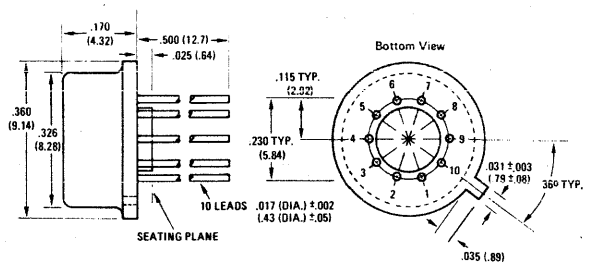
1S — 14 LEAD BRAZED D.I.P.



2A — TO-99 [.200 PC] (5.08 PC)

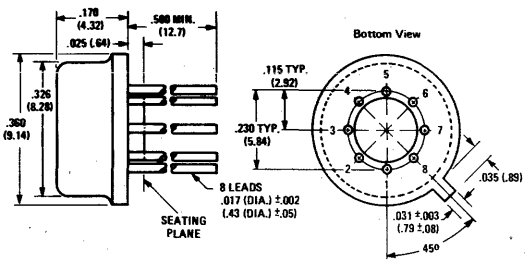


2D — TO-100 (10 LEAD)

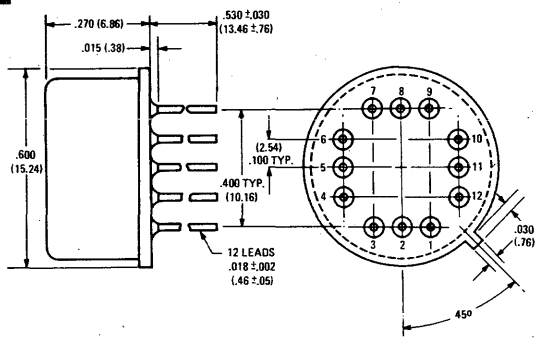


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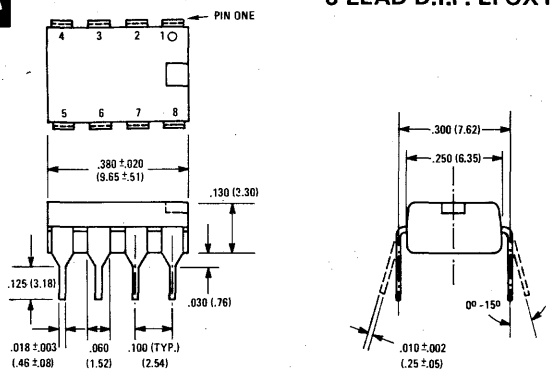
2E TO-99 [.230 PC] (5.84 PC)



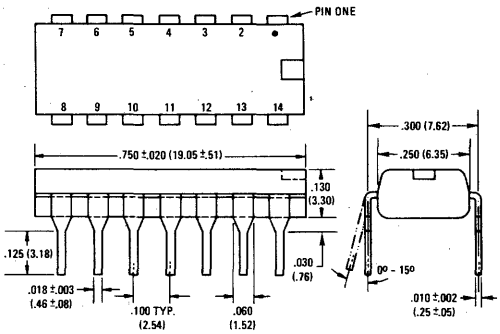
2G TO-8 (12 LEAD)



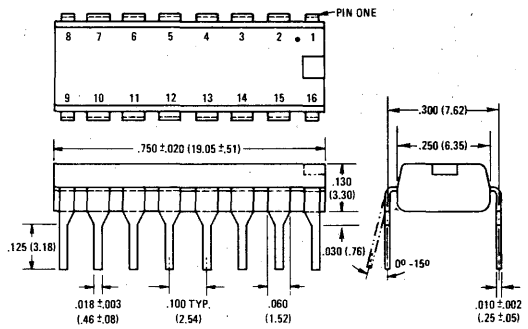
3A 8 LEAD D.I.P. EPOXY



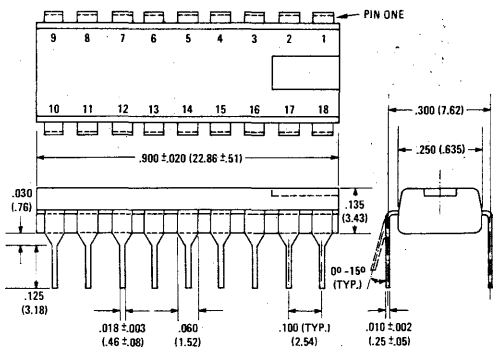
3B 14 LEAD D.I.P. EPOXY



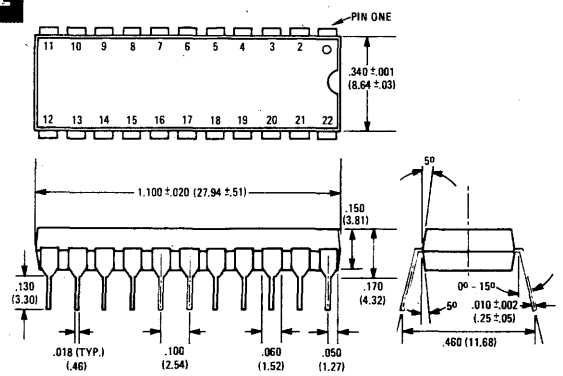
3C 16 LEAD D.I.P. EPOXY



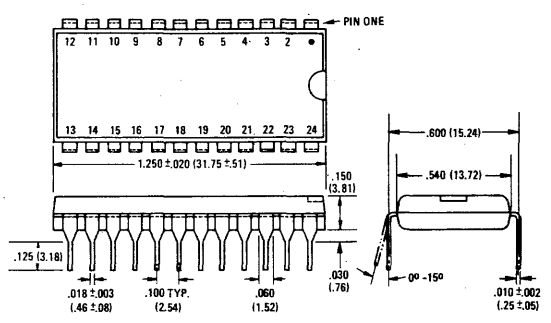
3D 18 LEAD D.I.P. EPOXY



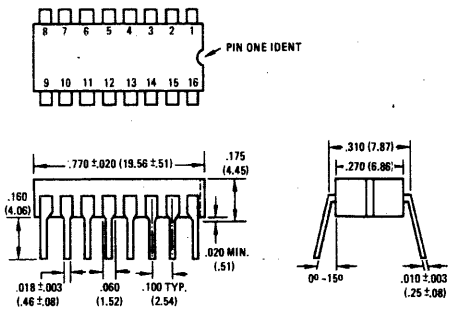
3E 22 LEAD D.I.P. EPOXY



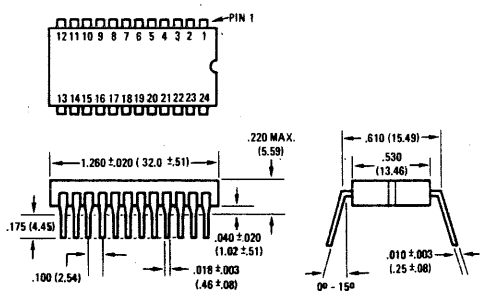
3F 24 LEAD D.I.P. EPOXY



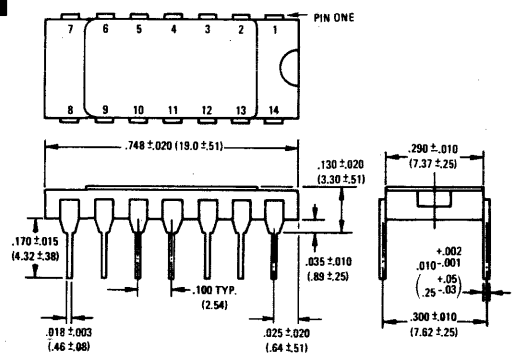
4B 16 LEAD CERAMIC D.I.P.



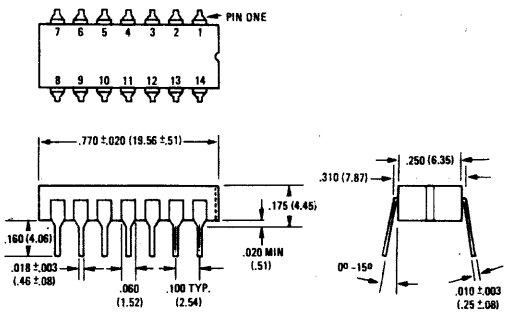
4K 24 LEAD CERAMIC D.I.P.



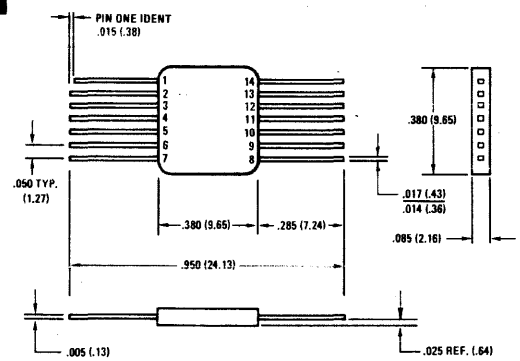
4Q 14 LEAD D.I.P. SIDE BRAZE



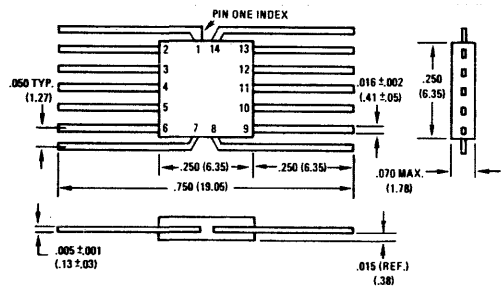
4U 14 LEAD CERAMIC D.I.P.



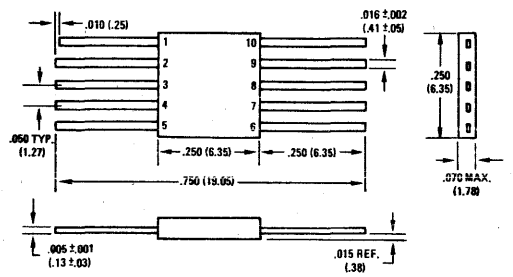
9R 14 LEAD METAL GLASS FLATPACK



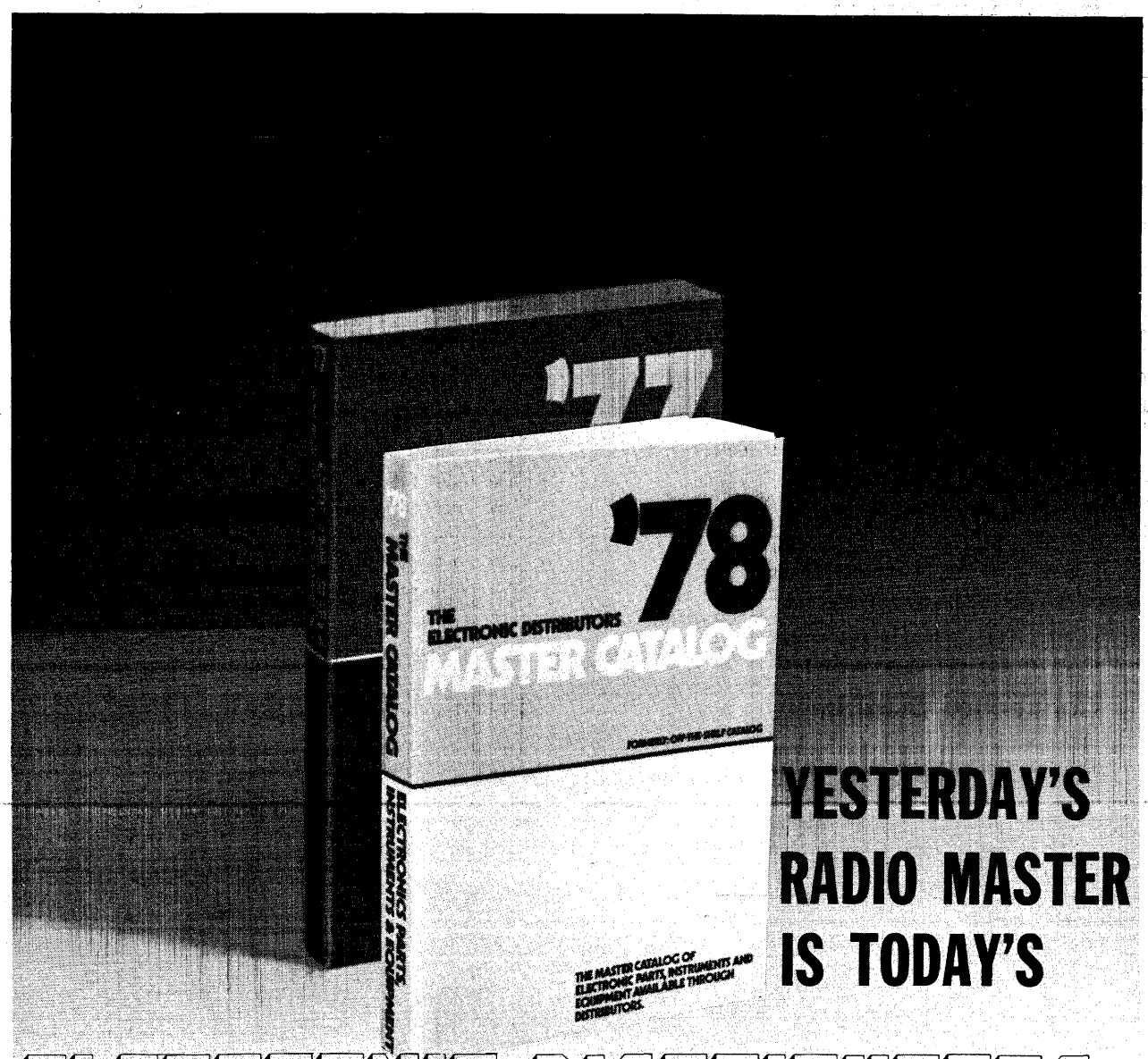
9V TO-86 METAL BOTTOM



9W TO-91



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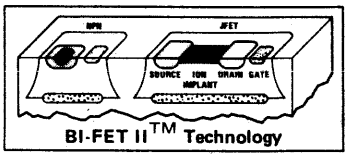
The **MANUFACTURERS' CATALOG SECTION** is a collection of their respective product pages, alphabetically by manufacturer, again including addresses and phone numbers.

The **MANUFACTURERS DIRECTORY** is an alphabetical listing of all manufacturers whose products information is shown. Page numbers are referenced. Sales offices, representatives and distributors are included for many manufacturers.

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National Semiconductor



BI-FET II™ Technology

LF347 Wide Bandwidth Quad JFET Input Operational Amplifier

General Description

The LF347 is a low cost high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF347 is pin compatible with the standard LM348.

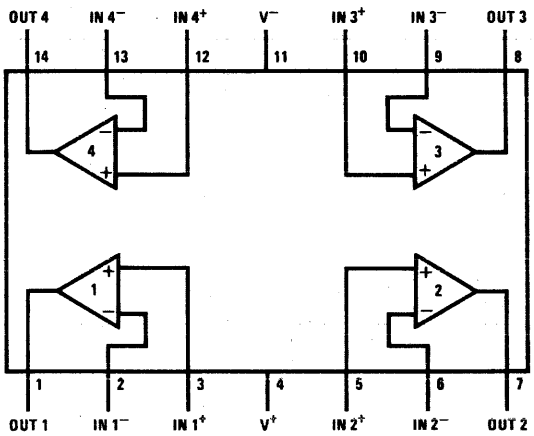
The LF347 may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits, active filters and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

- Internally trimmed offset voltage — 2 mV
- Low input bias current — 50 pA
- Low input noise voltage — 16 nV/$\sqrt{Hz}$
- Low input noise current — 0.01 pA/$\sqrt{Hz}$
- Wide gain bandwidth — 4 MHz
- High slew rate — 13 V/μs
- Low supply current — 7.2 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp-p, BW = 20 Hz–20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

Connection Diagram

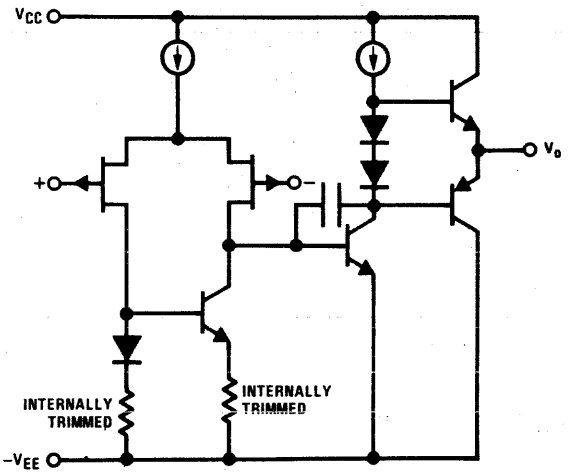
Dual-In-Line Package



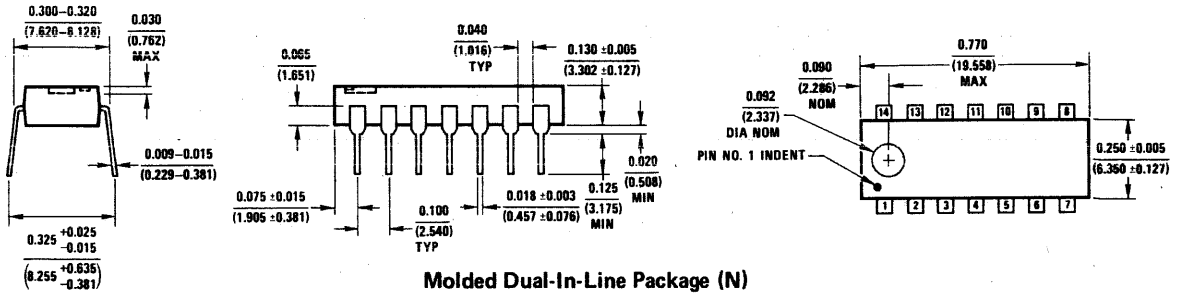
TOP VIEW

Simplified Schematic

1/4 Quad



Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number LF347AN, LF347BN, or LF347N
NS Package Number N14A

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IM-B10M97/Printed in U.S.A.

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Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	0°C to +70°C
T_j(MAX)	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF347A			LF347B			LF347			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C		1	2		3	5		5	10	mV
		Over Temperature			4			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10			10			10		µV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 3, 4)		25	50		25	100		25	100	pA
		$T_j \leq 70°C$			2			4			4	nA
I_B	Input Bias Current	T_j = 25°C, (Notes 3, 4)		50	100		50	200		50	200	pA
		$T_j \leq 70°C$			4			8			8	nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C	50	100		50	100		25	100		V/mV
		V_O = ±10V, R_L = 2 kΩ										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15		±11	+15		±11	+15		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10$ kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	80	100		80	100		70	100		dB
I_S	Supply Current			7.2	11		7.2	11		7.2	12	mA

AC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF347A			LF347B			LF347			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	V_S = ±15V, T_A = 25°C		13			13			13		V/µs
GBW	Gain-Bandwidth Product	V_S = ±15V, T_A = 25°C		4			4			4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		16			16			16		nV/√Hz
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01			0.01			0.01		pA/√Hz

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 125°C/W junction to ambient.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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National does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied; and National reserves the right, at any time without notice, to change said circuitry.

National Semiconductor

LM146/LM246/LM346
Programmable Quad Operational Amplifiers

General Description

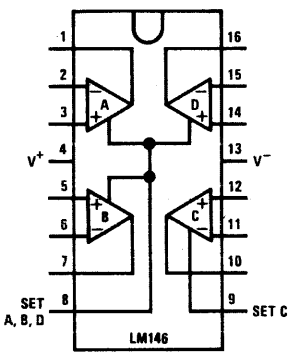
The LM146 series of quad op amps consists of four independent, high gain, internally compensated, low power, programmable amplifiers. Two external resistors (R_{SET}) allow the user to program the gain bandwidth product, slew rate, supply current, input bias current, input offset current and input noise. For example, the user can trade-off supply current for bandwidth or optimize noise figure for a given source resistance. In a similar way, other amplifier characteristics can be tailored to the application. Except for the two programming pins at the end of the package, the LM146 pin-out is the same as the LM124 and LM148.

Features (I_{SET} = 10 μA)

- Programmable electrical characteristics
- Battery-powered operation
- Low supply current — 350 μA amplifier
- Guaranteed gain bandwidth product — 0.8 MHz min
- Large DC voltage gain — 120 dB
- Low noise voltage — 28 nV/√Hz
- Wide power supply range — ±1.5V to ±22V
- Class AB output stage—no crossover distortion
- Ideal pin out for Biquad active filters
- Overload protection for inputs and outputs

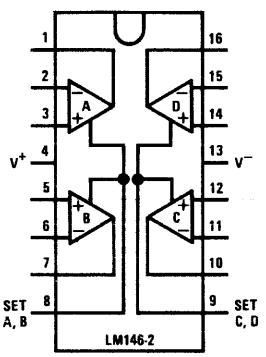
Connection Diagrams

Dual-In-Line Package



TOP VIEW

Dual-In-Line Package



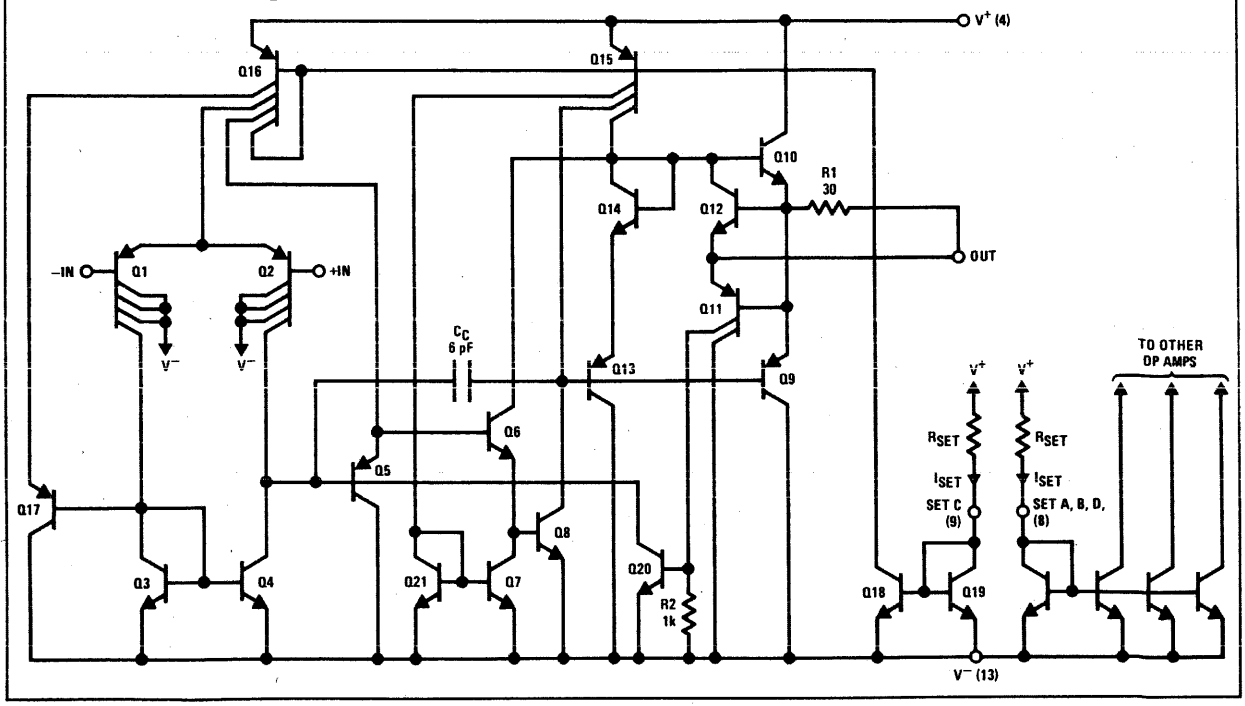
TOP VIEW

PROGRAMMING EQUATIONS

Total Supply Current = 1.4 mA (I_{SET}/10 μA)
Gain Bandwidth Product = 1 MHz (I_{SET}/10 μA)
Slew Rate = 0.4V/μs (I_{SET}/10 μA)
Input Bias Current ≃ 50 nA (I_{SET}/10 μA)
I_{SET} = Current into pin 8, pin 9 (see schematic diagram)

$$I_{SET} = \frac{V^+ - V^- - 0.6V}{R_{SET}}$$

Schematic Diagram



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IM-B20M107/Printed in U.S.A.

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Absolute Maximum Ratings (Note 1)

	LM146	LM246	LM346
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage (Note 1)	±30V	±30V	±30V
CM Input Voltage (Note 1)	±15V	±15V	±15V
Power Dissipation (Note 2)	900 mW	500 mW	500 mW
Output Short-Circuit Duration (Note 3)	Indefinite	Indefinite	Indefinite
Operating Temperature Range	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
Maximum Junction Temperature	150°C	110°C	100°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C
Thermal Resistance (θ_{jA}), (Note 2)			
Cavity DIP (D) (J) P_d	900 mW	900 mW	900 mW
θ_{jA}	90°C/W	90°C/W	90°C/W
Molded DIP (N) P_d			500 mW
θ_{jA}			140°C/W

DC Electrical Characteristics (V_S = ±15V, I_{SET} = 10 μA, Note 4)

PARAMETER	CONDITIONS	LM146			LM246/LM346			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{CM} = 0V, $R_S \leq 50\ \Omega$, T_A = 25°C		0.5	5		0.5	6	mV
Input Offset Current	V_{CM} = 0V, T_A = 25°C		2	20		2	100	nA
Input Bias Current	V_{CM} = 0V, T_A = 25°C		50	100		50	250	nA
Supply Current (4 Op Amps)	T_A = 25°C		1.4	2.0		1.4	2.5	mA
Large Signal Voltage Gain	R_L = 10 kΩ, ΔV_{OUT} = ±10V, T_A = 25°C	100	1000		50	1000		V/mV
Input CM Range	T_A = 25°C	±13.5	±14		±13.5	±14		V
CM Rejection Ratio	$R_S \leq 10$ kΩ, T_A = 25°C	80	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ, T_A = 25°C	80	100		74	100		dB
Output Voltage Swing	$R_L \geq 10$ kΩ, T_A = 25°C	±12	±14		±12	±14		V
Short-Circuit Current	T_A = 25°C	5	20	30	5	20	30	mA
Gain Bandwidth Product	T_A = 25°C	0.8	1.2		0.5	1.2		MHz
Phase Margin	T_A = 25°C		60			60		Deg
Slew Rate	T_A = 25°C		0.4			0.4		V/μs
Input Noise Voltage	f = 1 kHz, T_A = 25°C		28			28		$nV/\sqrt{Hz}$
Channel Separation	R_L = 10 kΩ, ΔV_{OUT} = 0V to ±12V, T_A = 25°C		120			120		dB
Input Resistance	T_A = 25°C		1.0			1.0		MΩ
Input Capacitance	T_A = 25°C		2.0			2.0		pF
Input Offset Voltage	V_{CM} = 0V, $R_S \leq 50\ \Omega$		0.5	6		0.5	7.5	mV
Input Offset Current	V_{CM} = 0V		2	25		2	100	nA
Input Bias Current	V_{CM} = 0V		50	100		50	250	nA
Supply Current (4 Op Amps)			1.5	2.0		1.5	2.5	mA
Large Signal Voltage Gain	R_L = 10 kΩ, ΔV_{OUT} = ±10V	50	1000		25	1000		V/mV
Input CM Range		±13.5	±14		±13.5	±14		V
CM Rejection Ratio	$R_S \leq 50\ \Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 50\ \Omega$	76	100		74	100		dB
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V

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DC Electrical Characteristics ($V_S = \pm 15V$, $I_{SET} = 1\ \mu A$)

PARAMETER	CONDITIONS	LM146			LM246/LM346			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\ \Omega$, $T_A = 25°C$		0.5	5		0.5	6	mV
Input Bias Current	$V_{CM} = 0V$, $T_A = 25°C$		7.5	20		7.5	100	nA
Supply Current (4 Op Amps)	$T_A = 25°C$		140	250		140	300	μA
Gain Bandwidth Product	$T_A = 25°C$	80	100		50	100		kHz

DC Electrical Characteristics ($V_S = \pm 1.5V$, $I_{SET} = 10\ \mu A$)

PARAMETER	CONDITIONS	LM146			LM246/LM346			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\ \Omega$, $T_A = 25°C$		0.5	5		0.5	7	mV
Input CM Range	$T_A = 25°C$	±0.7			±0.7			V
CM Rejection Ratio	$R_S \leq 50\ \Omega$, $T_A = 25°C$		80			80		dB
Output Voltage Swing	$R_L \geq 10\ k\Omega$, $T_A = 25°C$	±0.6			±0.6			V

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

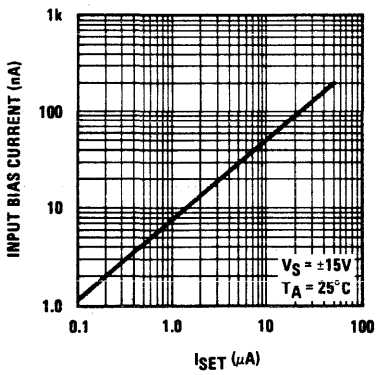
Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 3: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

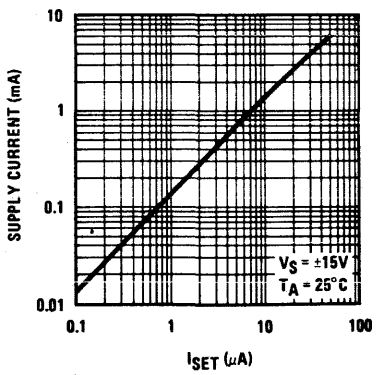
Note 4: These specifications apply over the absolute maximum operating temperature range unless otherwise noted.

Typical Performance Characteristics

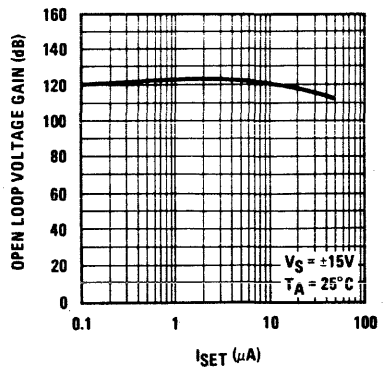
Input Bias Current vs I_{SET}



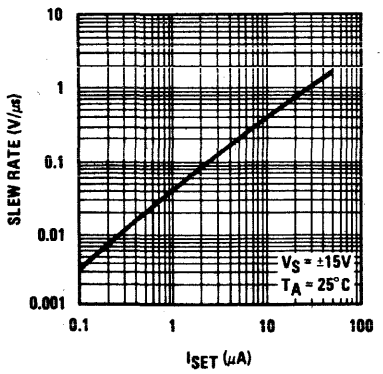
Supply Current vs I_{SET}



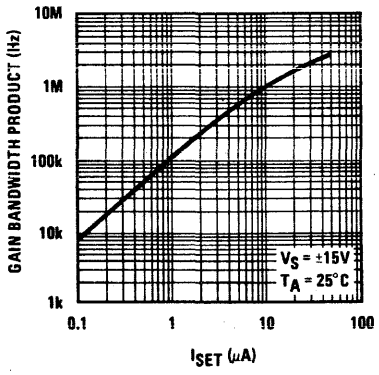
Open Loop Voltage Gain vs I_{SET}



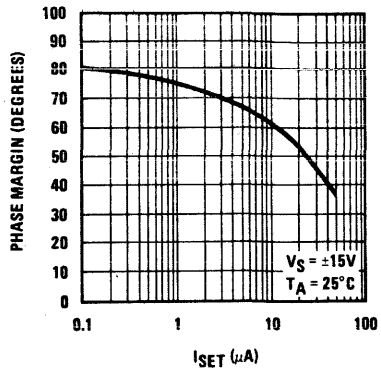
Slew Rate vs I_{SET}



Gain Bandwidth Product vs I_{SET}



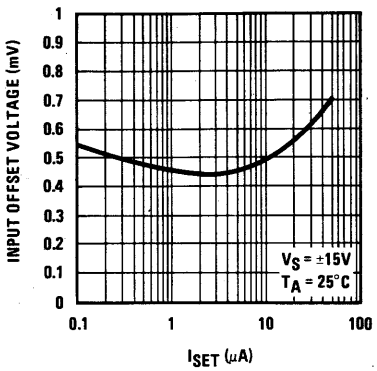
Phase Margin vs I_{SET}



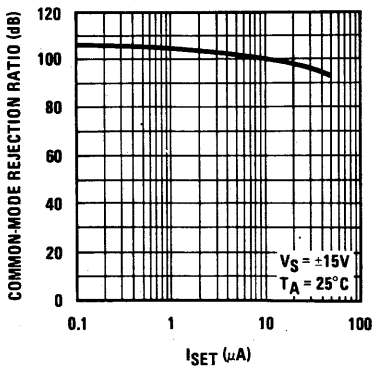
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Typical Performance Characteristics (Continued)

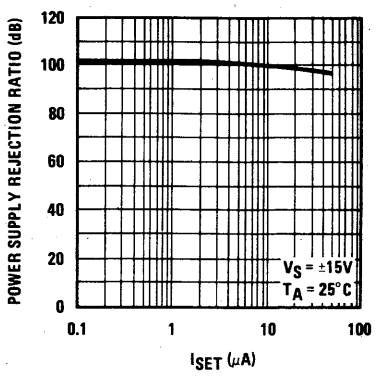
Input Offset Voltage vs I_{SET}



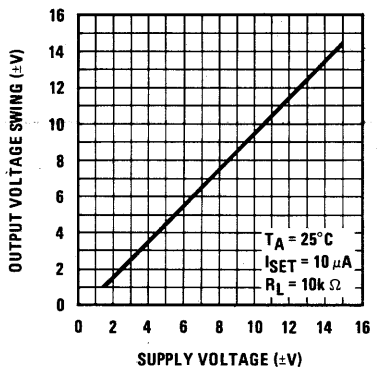
Common-Mode Rejection Ratio vs I_{SET}



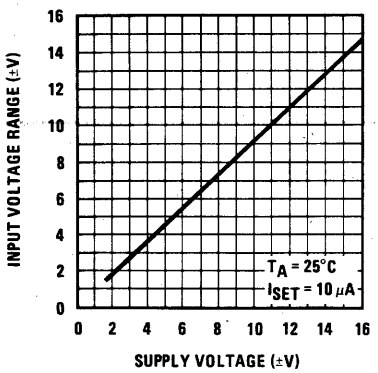
Power Supply Rejection Ratio vs I_{SET}



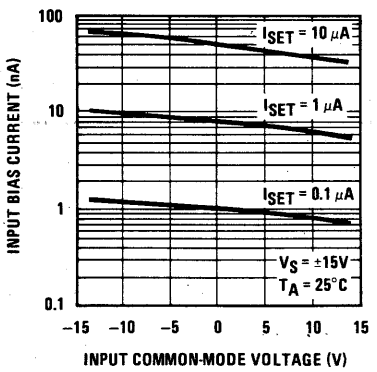
Output Voltage Swing vs Supply Voltage



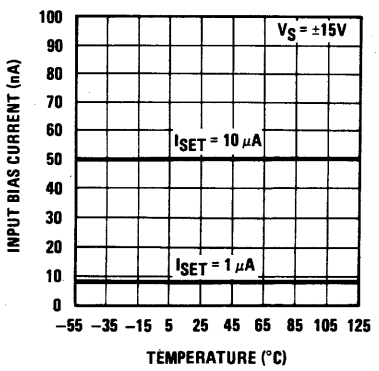
Input Voltage Range vs Supply Voltage



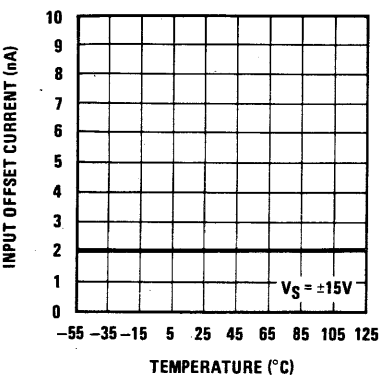
Input Bias Current vs Input Common-Mode Voltage



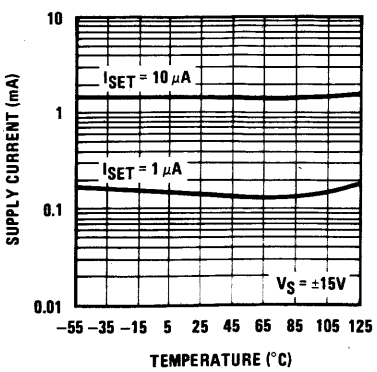
Input Bias Current vs Temperature



Input Offset Current vs Temperature



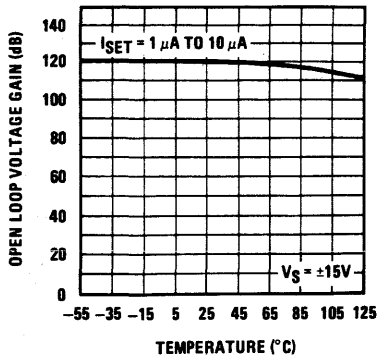
Supply Current vs Temperature



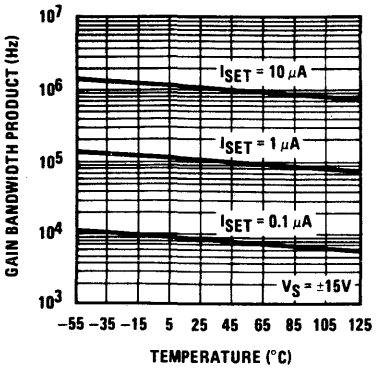
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Typical Performance Characteristics (Continued)

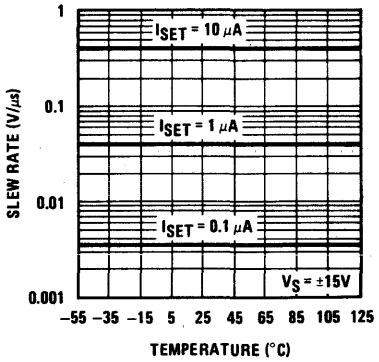
Open Loop Voltage Gain vs Temperature



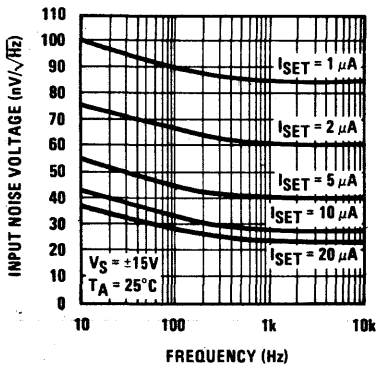
Gain Bandwidth Product vs Temperature



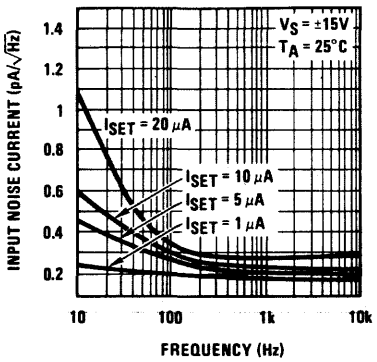
Slew Rate vs Temperature



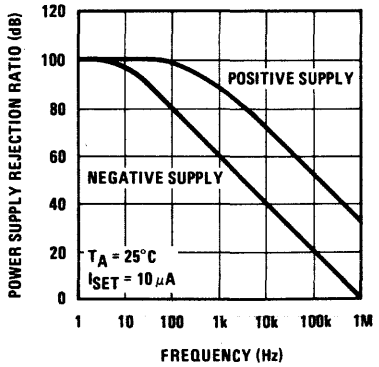
Input Noise Voltage vs Frequency



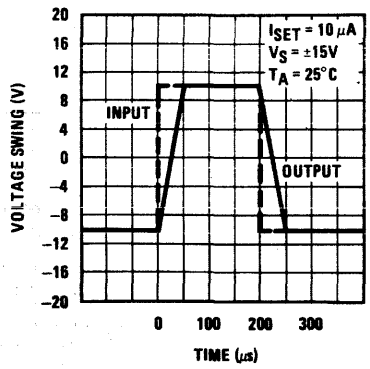
Input Noise Current vs Frequency



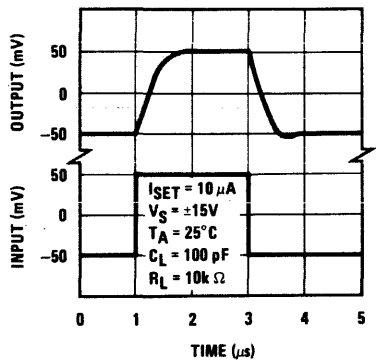
Power Supply Rejection Ratio vs Frequency



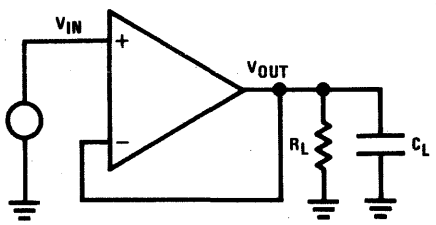
Voltage Follower Pulse Response



Voltage Follower Transient Response



Transient Response Test Circuit



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Application Hints

Avoid reversing the power supply polarity, the device will fail.

Common-Mode Input Voltage: The negative common-mode voltage limit is one diode drop above the negative supply voltage. Exceeding this limit on either input will result in an output phase reversal. The positive common-mode limit is typically 1V below the positive supply voltage. No output phase reversal will occur if this limit is exceeded by either input.

Output Voltage Swing vs I_{SET}: For a desired output voltage swing the value of the minimum load depends on the positive and negative output curent capability of the op amp. The maximum available positive output current, (I_{CL+}), of the device increases with I_{SET} whereas the negative output current (I_{CL-}) is independent of I_{SET}. *Figure 1* illustrates the above.

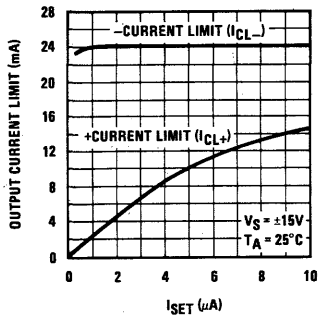


FIGURE 1. Output Current Limit vs I_{SET}

Input Capacitance: The input capacitance, C_{IN}, of the LM146 is approximately 2 pF; any stray capacitance, C_S, (due to external circuit circuit layout) will add to C_{IN}. When resistive or active feedback is applied, an additional pole is added to the open loop frequency response of the device. For instance with resistive feedback *(Figure 2)*, this pole occurs at $1/2\pi$ (R1||R2) (C_{IN} + C_S). Make sure that this pole occurs at least 2 octaves beyond the expected −3 dB frequency corner of the closed loop gain of the amplifier; if not, place a lead capacitor in the feedback such that the time constant of this capacitor and the resistance it parallels is equal to the $R_I(C_S + C_{IN})$, where R_I is the input resistance of the circuit.

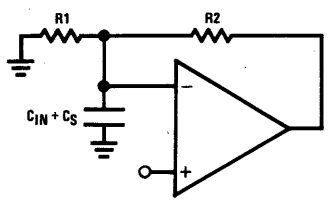


FIGURE 2

Temperature Effect on the GBW: The GBW (gain bandwidth product), of the LM146 is directly proportional to I_{SET} and inversely proportional to the absolute temperature. When using resistors to set the bias current, I_{SET}, of the device, the GBW product will decrease with increasing temperature. Compensation can be provided by creating an I_{SET} current directly proportional to temperature (see typical applications).

Isolation Between Amplifiers: The LM146 die is isothermally layed out such that crosstalk between *all 4* amplifiers is in excess of −105 dB (DC). Optimum isolation (better than −110 dB) occurs between amplifiers A and D, B and C; that is, if amplifier A dissipates power on its output stage, amplifier D is the one which will be affected the least, and vice versa. Same argument holds for amplifiers B and C.

LM146 Typical Performance Summary: The LM146 typical behavior is shown in *Figure 3*. The device is fully predictable. As the set current, I_{SET}, increases, the speed, the bias current, and the supply current increase while the noise power decreases proportionally and the V_{OS} remains constant. The usable GBW range of the op amp is 10 kHz to 3.5–4 MHz.

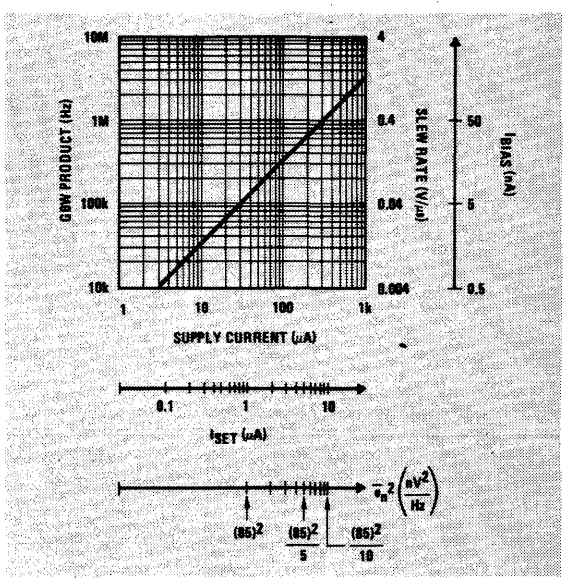


FIGURE 3. LM146 Typical Characteristics

Low Power Supply Operation: The quad op amp operates down to ±1.3V supply. Also, since the internal circuitry is biased through programmable current sources, no degradation of the device speed will occur.

Speed vs Power Consumption: LM146 vs LM4250 (single programmable). Through *Figure 4*, we observe that the LM146's power consumption has been optimized for GBW products above 200 kHz, whereas the LM4250 will reach a GBW of no more than 300 kHz, for GBW products below 200 kHz, the LM4250 will consume less.

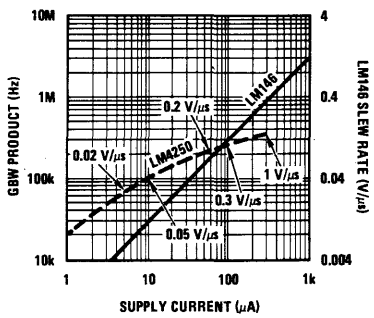
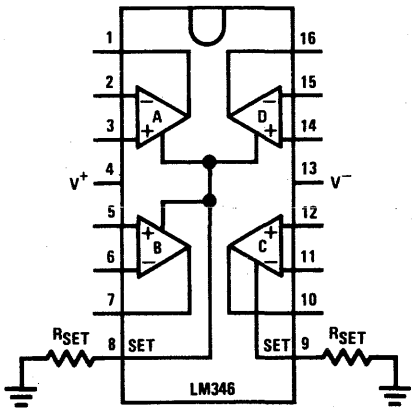


FIGURE 4. LM146 vs LM4250

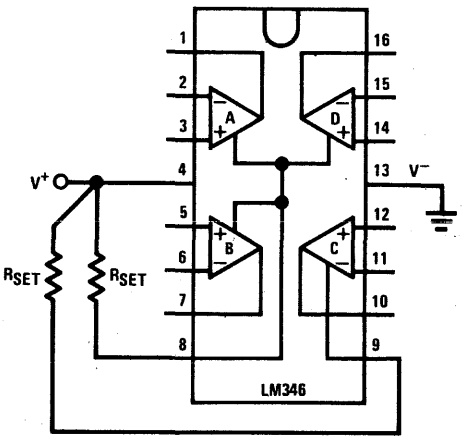
Typical Applications

Dual Supply or Negative Supply Biasing



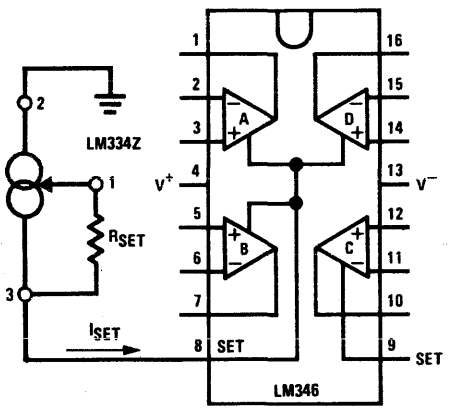
$$I_{SET} \simeq \frac{|V^-| - 0.6V}{R_{SET}}$$

Single (Positive) Supply Biasing



$$I_{SET} \simeq \frac{V^+ - 0.6V}{R_{SET}}$$

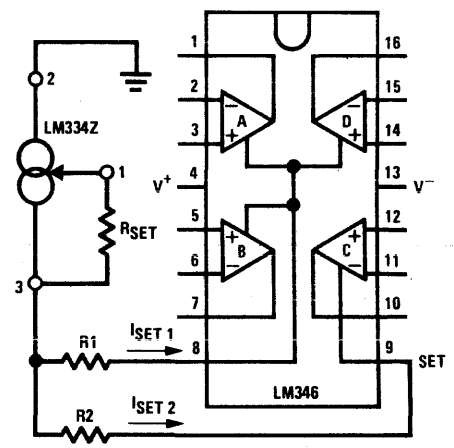
Current Source Biasing with Temperature Compensation



$$I_{SET} = \frac{67.7\ mV}{R_{SET}}$$

- The LM344 provides an I_{SET} directly proportional to absolute temperature. This cancels the slight GBW product temperature coefficient of the LM346.

Biasing all 4 Amplifiers with Single Current Source



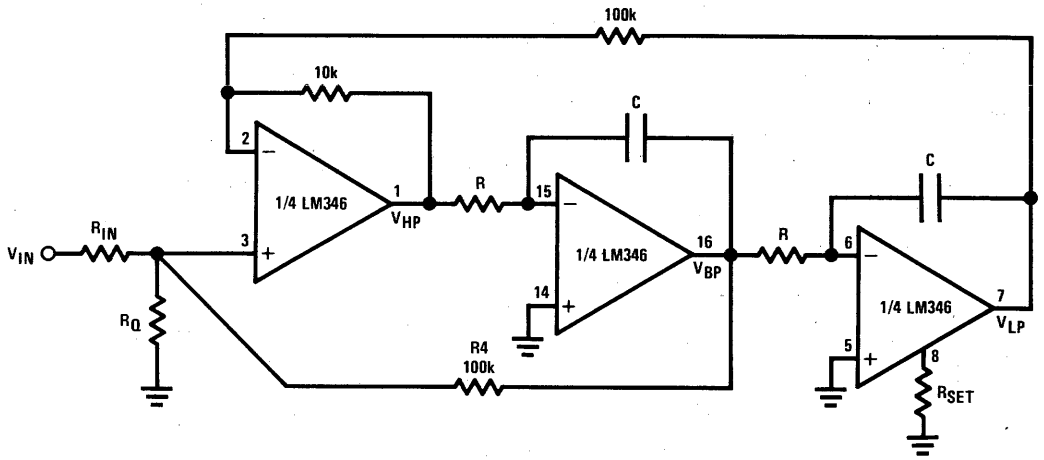
$$\frac{I_{SET1}}{I_{SET2}} = \frac{R2}{R1},\ I_{SET1} + I_{SET2} = \frac{67.7\ mV}{R_{SET}}$$

- For $I_{SET1} \simeq I_{SET2}$ resistors R1 and R2 are not required if a slight error between the 2 set currents can be tolerated. If not, then use R1 = R2 to create a 100 mV drop across them.

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Active Filters Applications

Basic (Non-Inverting "State Variable") Active Filter Building Block



- The LM146 quad programmable op amp is especially suited for active filters because of their adequate GBW product and low power consumption.

  Circuit synthesis equations (for circuit analysis equations, consult with the AF100 and LM148 data sheet).

  Need to know desired: f_o = center frequency measured at the BP output
  Q_o = quality factor measured at the BP output
  H_o = gain at the output of interest (BP or HP or LP or all of them)

  ▲ Relation between different gains: $H_{o(BP)} = 0.316 \times Q_o \times H_{o(LP)}$; $H_{o(LP)} = 10 \times H_{o(HP)}$

  ▲ $R \times C = \dfrac{5.033 \times 10^{-2}}{f_o}$ (sec)

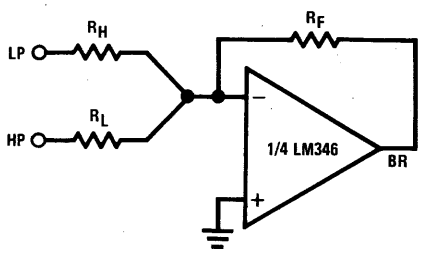
  ▲ For BP output: $R_Q = \left(\dfrac{3.478\, Q_o - H_{o(BP)}}{10^5} - \dfrac{H_{o(BP)}}{10^5 \times 3.478 \times Q_o} \right)^{-1}$; $R_{IN} = \dfrac{\left(\dfrac{3.478\, Q_o}{H_{o(BP)}} - 1 \right)}{\dfrac{1}{R_Q} + 10^{-5}}$

  ▲ For HP output: $R_Q = \dfrac{1.1 \times 10^5}{3.478\, Q_o\, (1.1 - H_{o(HP)}) - H_{o(HP)}}$; $R_{IN} = \dfrac{\dfrac{1.1}{H_{o(HP)}} - 1}{\dfrac{1}{R_Q} + 10^{-5}}$

  Note. All resistor values are given in ohms.

  ▲ For LP output: $R_Q = \dfrac{11 \times 10^5}{3.478\, Q_o\, (11 - H_{o(LP)}) - H_{o(LP)}}$; $R_{IN} = \dfrac{\dfrac{11}{H_{o(LP)}} - 1}{\dfrac{1}{R_Q} + 10^{-5}}$

  ▲ For BR (notch) output: Use the 4th amplifier of the LM146 to sum the LP and HP outputs of the basic filter.



$$\sqrt{\frac{R_H}{R_L}} = 0.316\ \frac{f_{notch}}{f_o}$$

Determine R_F according to the desired gains: $H_{o(BR)}\big|_{f << f_{notch}} = \dfrac{R_F}{R_L} H_{o(LP)}$, $H_{o(BR)}\big|_{f >> f_{notch}} = \dfrac{R_F}{R_H} H_{o(HP)}$

- **Where to use amplifier C:** Examine the above gain relations and determine the dynamics of the filter. Do not allow slew rate limiting in any output (V_{HP}, V_{BP}, V_{LP}), that is:

$$V_{IN(peak)} < 63.66 \times 10^3 \times \frac{I_{SET}}{10\,\mu A} \times \frac{1}{f_o \times H_o}\ \text{(Volts)}$$

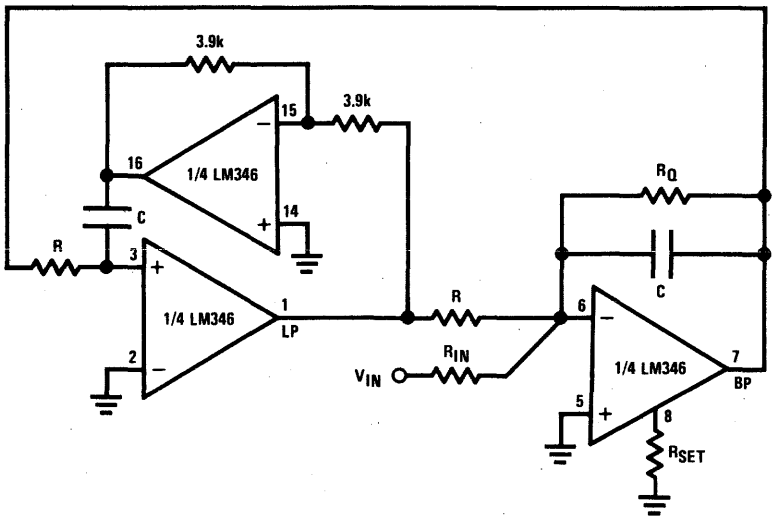
If necessary, use amplifier C, biased at higher I_{SET}, where you get the largest output swing.

Deviation from Theoretical Predictions: Due to the finite GBW products of the op amps the f_o, Q_o will be slightly different from the theoretical predictions.

$$f_{real} \simeq \frac{f_o}{1 + \dfrac{2\, f_o}{GBW}}\ ,\quad Q_{real} \simeq \frac{Q_o}{1 - \dfrac{3.2\, f_o \times Q_o}{GBW}}$$

Active Filters Applications (Continued)

A Simple to Design BP, LP Filter Building Block



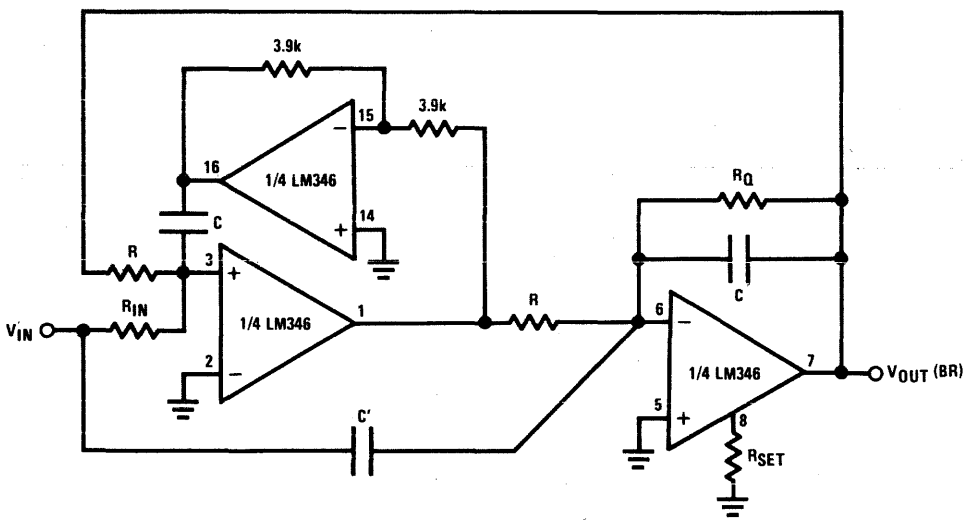
- If resistive biasing is used to set the LM346 performance, the Q_o of this filter building block is nearly insensitive to the op amp's GBW product temperature drift; it has also better noise performance than the state variable filter.

Circuit Synthesis Equations

$$H_{o(BP)} = Q_o H_{o(LP)};\ R \times C = \frac{0.159}{f_o};\ R_Q = Q_o \times R;\ R_{IN} = \frac{R_Q}{H_{o(BP)}} = \frac{R}{H_{o(LP)}}$$

- For the eventual use of amplifier C, see comments on the previous page.

A 3-Amplifier Notch Filter (or Elliptic Filter Building Block)



Circuit Synthesis Equations

$$R \times C = \frac{0.159}{f_o};\ R_Q = Q_o \times R;\ R_{IN} = \frac{0.159 \times f_o}{C' \times f^2_{notch}}$$

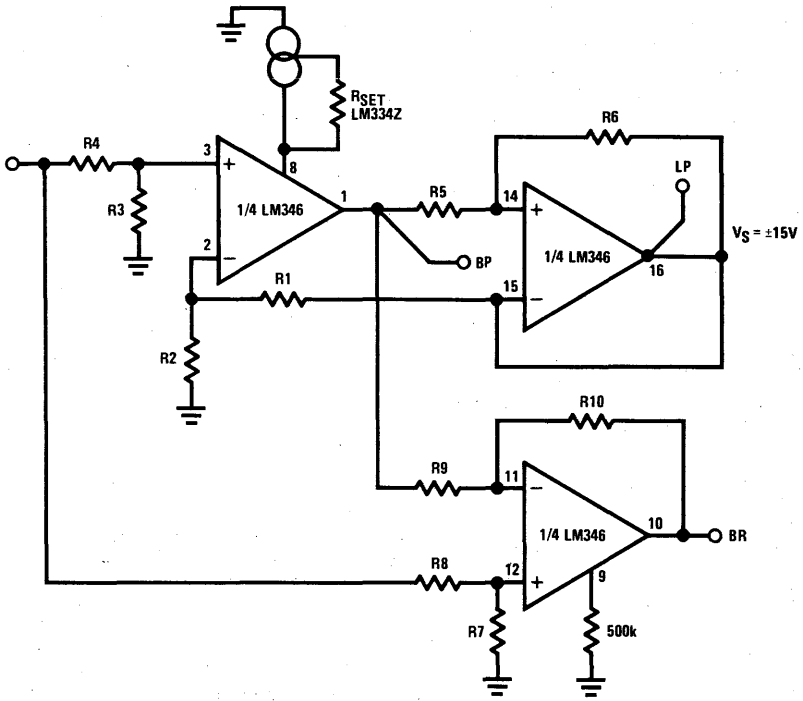
$$H_{o(BR)}\Big|_{f << f_{notch}} = \frac{R}{R_{IN}} H_{o(BR)}\Big|_{f >> f_{notch}} = \frac{C'}{C}$$

- For nothing but a notch output: $R_{IN} = R$, $C' = C$.

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Active Filters Applications (Continued)

Capacitorless Active Filters (Basic Circuit)

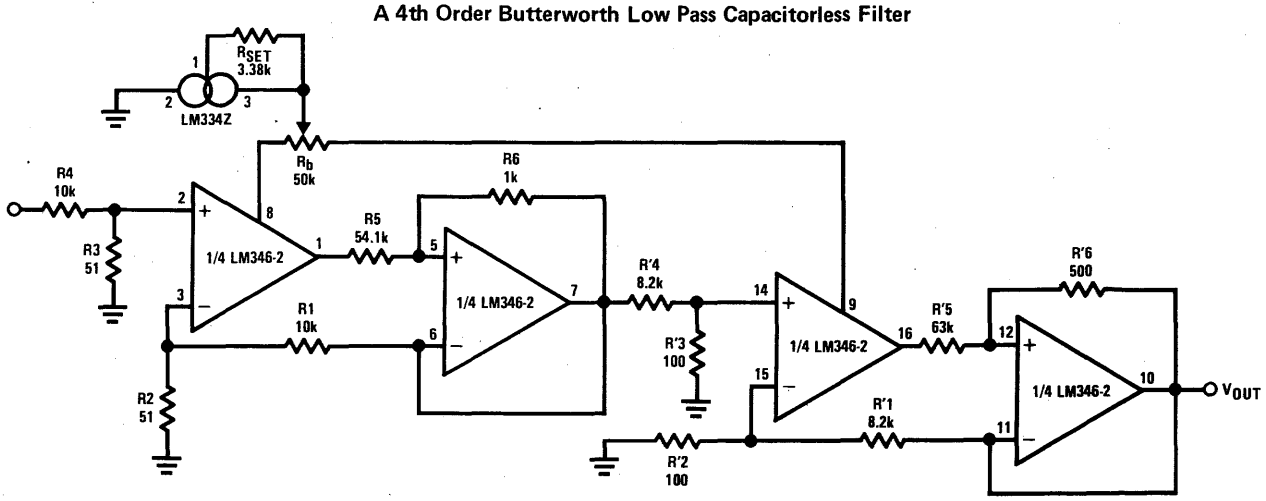


- This is a BP, LP, BR filter. The filter characteristics are created by using the tunable frequency response of the LM346.
- **Limitations:** $Q_o < 10$, $f_o \times Q_o < 1.5$ MHz, output voltage should not exceed $V_{peak(out)} \leq \frac{63.66 \times 10^3}{f_o} \times \frac{I_{SET}\ (\mu A)}{10\ \mu A}$ (V)
- Design equations: $a = \frac{R6 + R5}{R6}$, $b = \frac{R2}{R1 + R2}$, $c = \frac{R3}{R3 + R4}$, $d = \frac{R7}{R8 + R7}$, $e = \frac{R10}{R9 + R10}$, $f_{o(BP)} = f_u \sqrt{\frac{b}{a}}$, $H_{o(BP)} = a \times c$,

  $H_{o(LP)} = \frac{c}{b}$, $Q_o = \sqrt{a \times b}$

  $f_{o(BR)} = f_{o(BP)} \left(1 - \frac{c}{b}\right) \simeq f_{o(BP)}$ $(C << 1)$ provided that $d = H_{o(BP)} \times e$, $H_{o(BR)} = \frac{R10}{R9}$.
- Advantage: f_o, Q_o, H_o can be independently adjusted; that is, the filter is extremely easy to tune.
- Tuning procedure (ex. BP tuning)
  1. Pick up a convenient value for b; $(b < 1)$
  2. Adjust Q_o through R5
  3. Adjust $H_{o(BP)}$ through R4
  4. Adjust f_o through R_{SET}

A 4th Order Butterworth Low Pass Capacitorless Filter

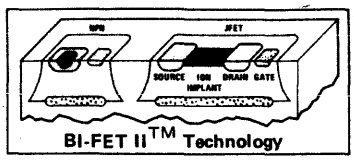


Ex: $f_c = 20$ kHz, H_o (gain of the filter) = 1, $Q_{o1} = 0.541$, $Q_{o2} = 1.306$.

- Since for this filter the GBW product of all 4 amplifiers has been designed to be the same (~1 MHz) only one current source can be used to bias the circuit. Fine tuning can be further accomplished through R_b.

National Semiconductor

LF351 Wide Bandwidth JFET Input Operational Amplifiers



General Description

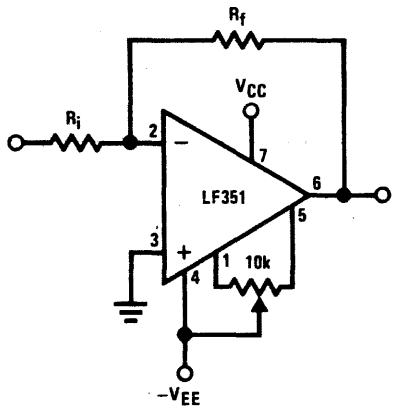
The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the LF351 is the better choice.

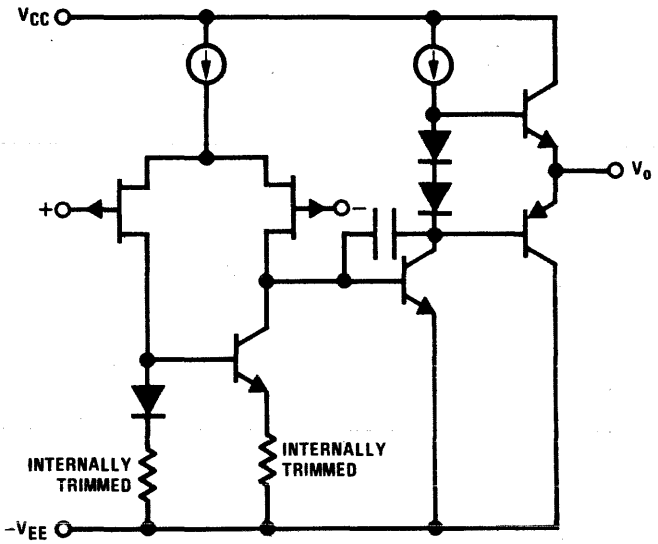
Features

- Internally trimmed offset voltage — 2 mV
- Low input bias current — 50 pA
- Low input noise voltage — 16 nV/$\sqrt{Hz}$
- Low input noise current — 0.01 pA/$\sqrt{Hz}$
- Wide gain bandwidth — 4 MHz
- High slew rate — 13 V/μs
- Low supply current — 1.8 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp-p, BW = 20 Hz–20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

Typical Connection

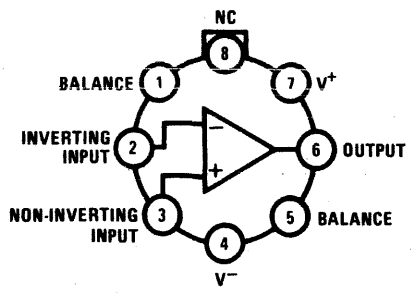


Simplified Schematic



Connection Diagrams

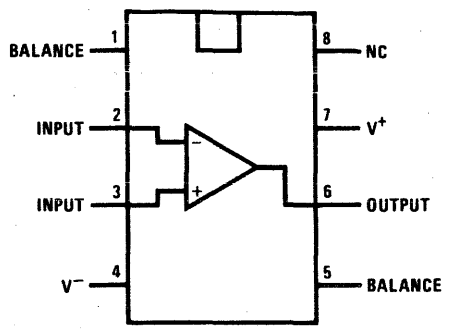
Metal Can Package



TOP VIEW

Note. Pin 4 connected to case.

Dual-In-Line Package



TOP VIEW

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IM-B20M97/Printed in U.S.A.

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF351A			LF351B			LF351			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C		1	2		3	5		5	10	mV
		Over Temperature			4			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10			10			10		µV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 3, 4)		25	50		25	100		25	100	pA
		$T_j \leq 70°C$			2			4			4	nA
I_B	Input Bias Current	T_j = 25°C, (Notes 3, 4)		50	100		50	200		50	200	pA
		$T_j \leq 70°C$			4			8			8	nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C	50	100		50	100		25	100		V/mV
		V_O = ±10V, R_L = 2 kΩ										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15		±11	+15		±11	+15		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10$ kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	80	100		80	100		70	100		dB
I_S	Supply Current			1.8	2.8		1.8	2.8		1.8	3.4	mA

AC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF351A			LF351B			LF351			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	V_S = ±15V, T_A = 25°C		13			13			13		V/µs
GBW	Gain Bandwidth Product	V_S = ±15V, T_A = 25°C		4			4			4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		16			16			16		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

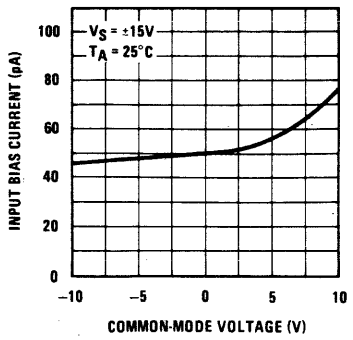
Note 3: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

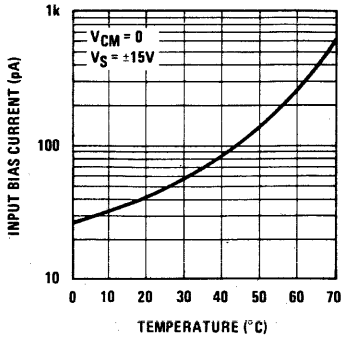
Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

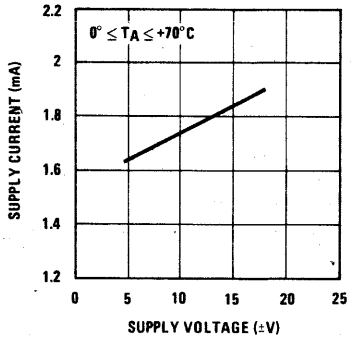
Input Bias Current



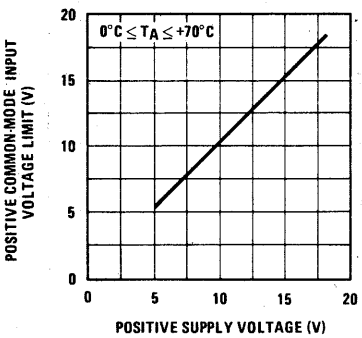
Input Bias Current



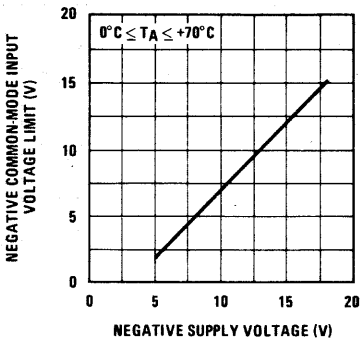
Supply Current



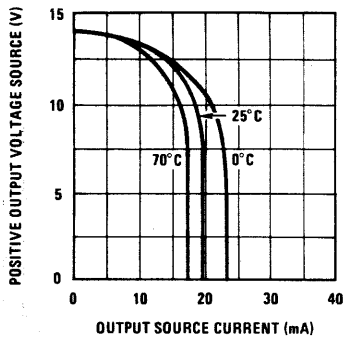
Positive Common-Mode Input Voltage Limit



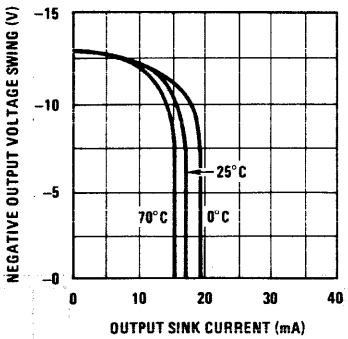
Negative Common-Mode Input Voltage Limit



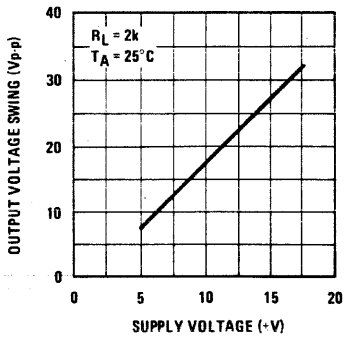
Positive Current Limit



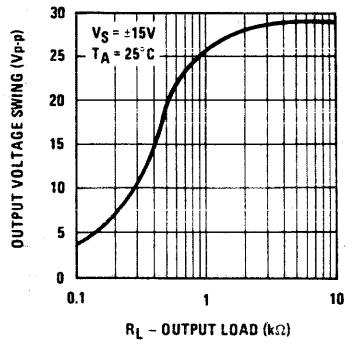
Negative Current Limit



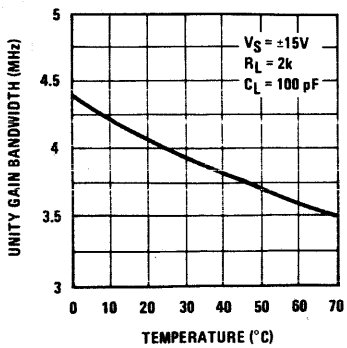
Voltage Swing



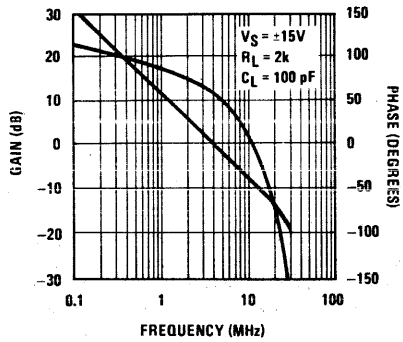
Output Voltage Swing



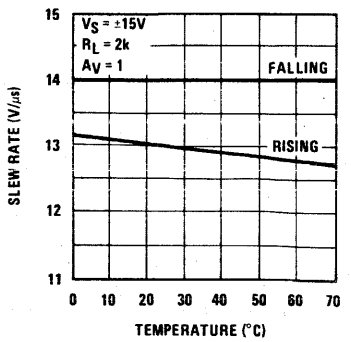
Gain Bandwidth



Bode Plot



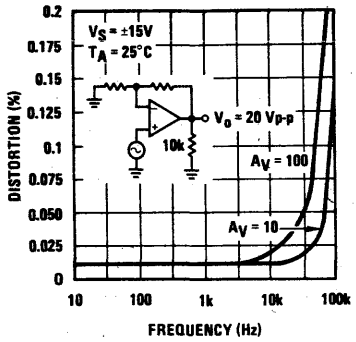
Slew Rate



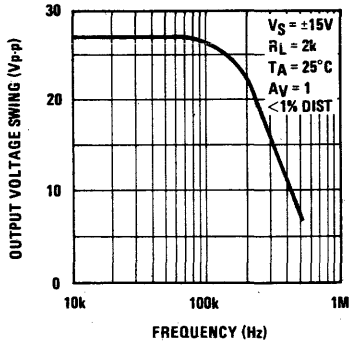
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Typical Performance Characteristics (Continued)

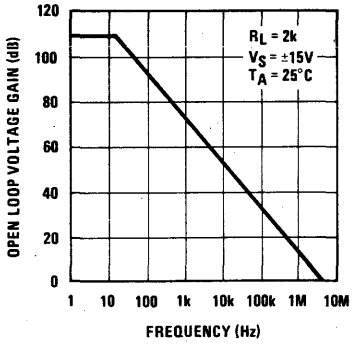
Distortion vs Frequency



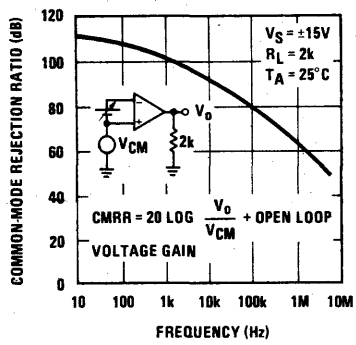
Undistorted Output Voltage Swing



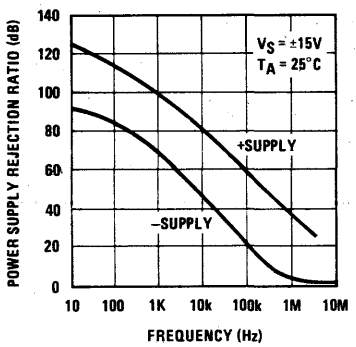
Open Loop Frequency Response



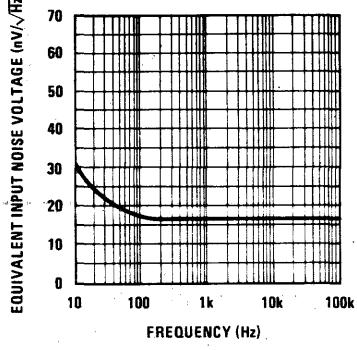
Common-Mode Rejection Ratio



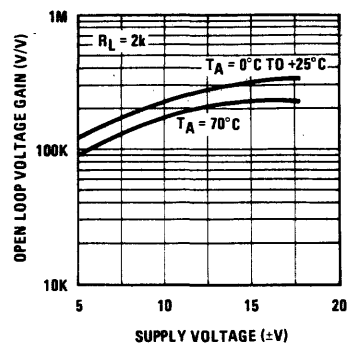
Power Supply Rejection Ratio



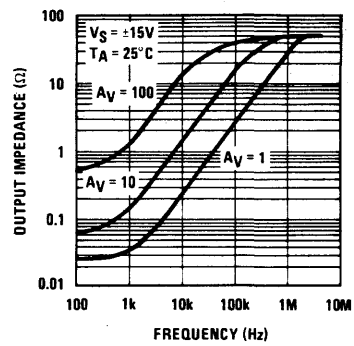
Equivalent Input Noise Voltage



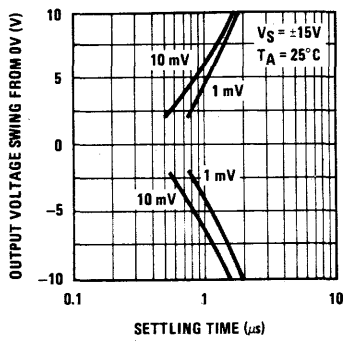
Open Loop Voltage Gain (V/V)



Output Impedance



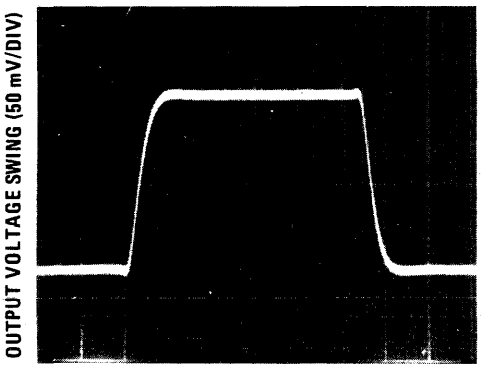
Inverter Settling Time



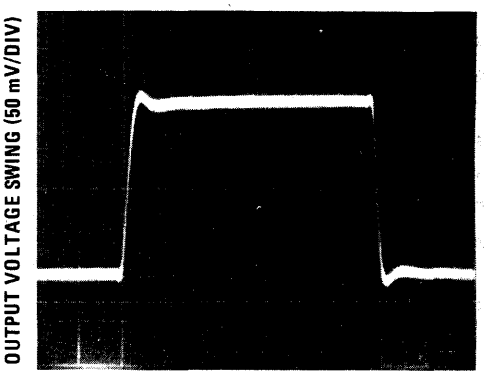
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Pulse Response

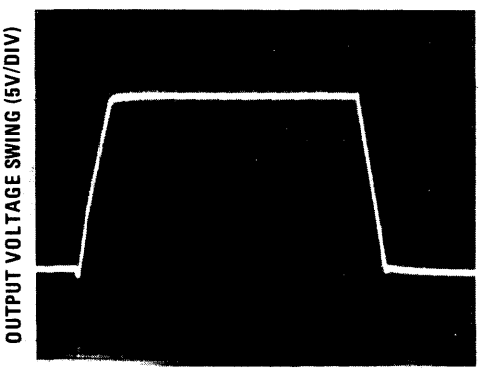
Small Signal Inverting



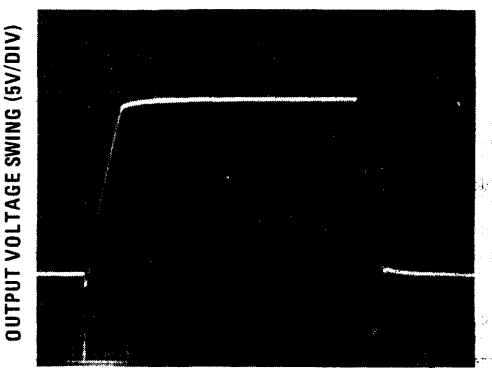
Small Signal Non-Inverting



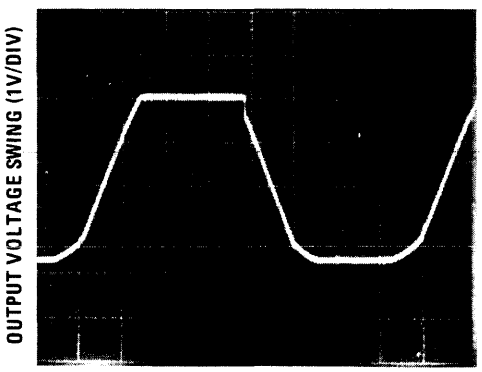
Large Signal Inverting



Large Signal Non-Inverting



Current Limit (R_L = 100Ω)



Application Hints

The LF351 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a

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Application Hints (Continued)

high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF351 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF351 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

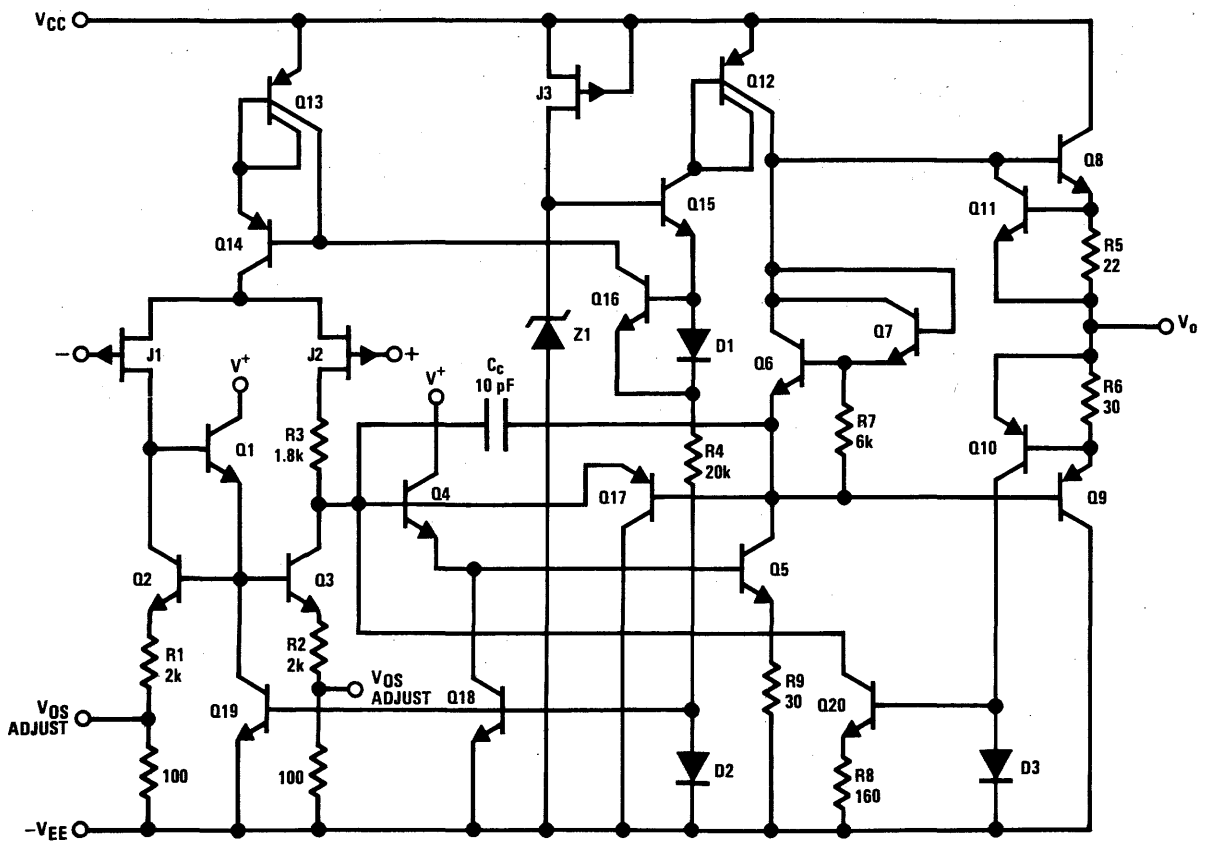
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

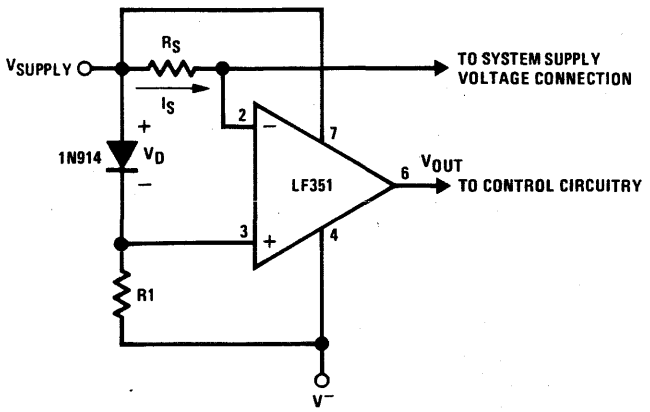
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



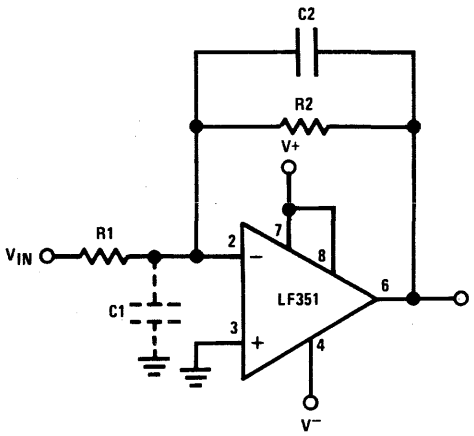
Typical Applications

Supply Current Indicator/Limiter



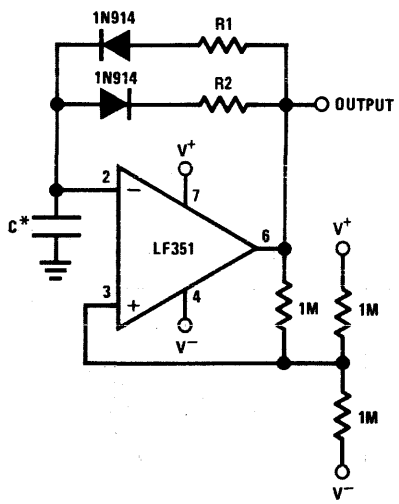
- V_{OUT} switches high when $R_S I_S > V_D$

Hi-Z_{IN} Inverting Amplifier



Parasitic input capacitance C1 ≅ (3 pF for LF351 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≅ R1C1.

Ultra-Low (or High) Duty Cycle Pulse Generator

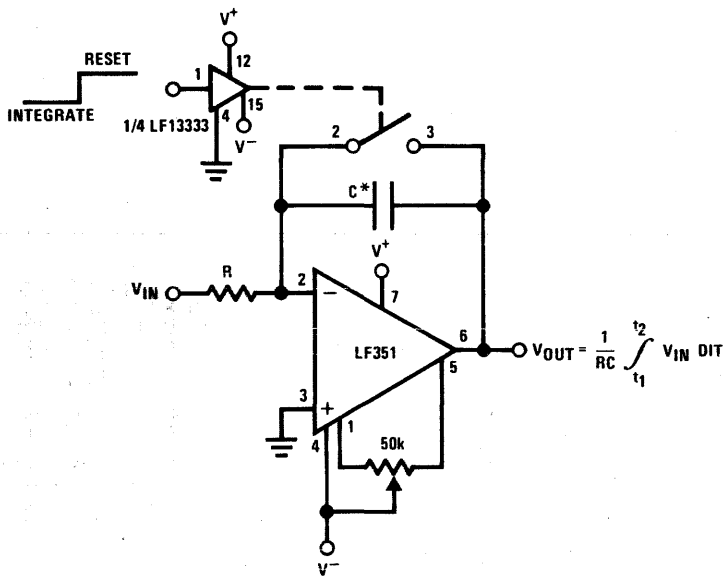


- $t_{OUTPUT\ HIGH} \approx R1C \ln \frac{4.8 - 2V_S}{4.8 - V_S}$
- $t_{OUTPUT\ LOW} \approx R2C \ln \frac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V^-|$

*low leakage capacitor

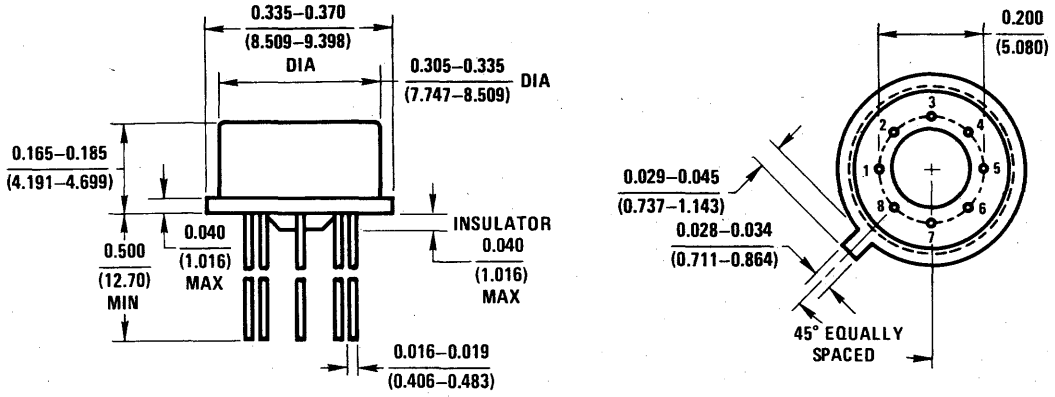
Long Time Integrator



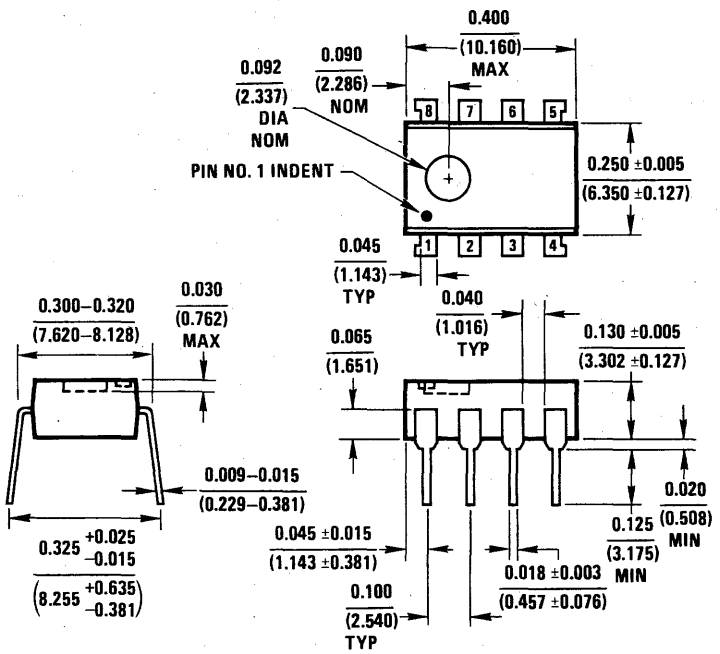
* Low leakage capacitor
- 50k pot used for less sensitive V_{OS} adjust

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Physical Dimensions inches (millimeters)



TO-5 Metal Can Package (H)
Order Number LF351AH, LF351BH
or LF351H



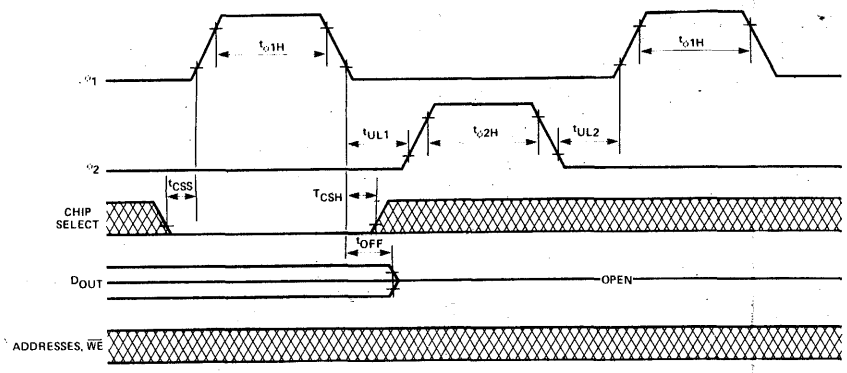
Molded Dual-in-Line Package (N)
Order Number LF351AN, LF351BN
or LF351N
NS Package Number N08A

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

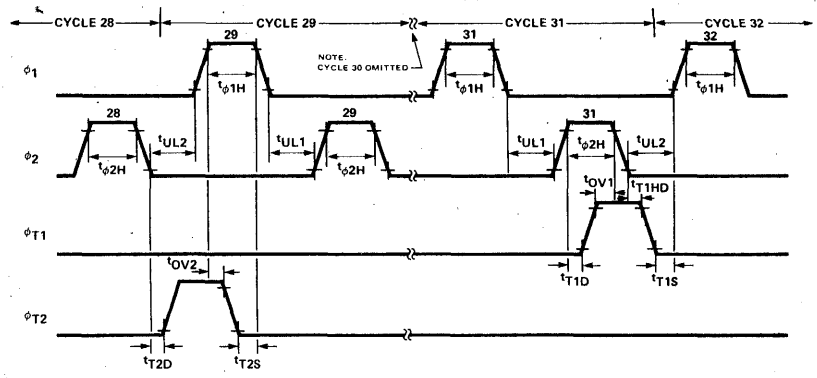
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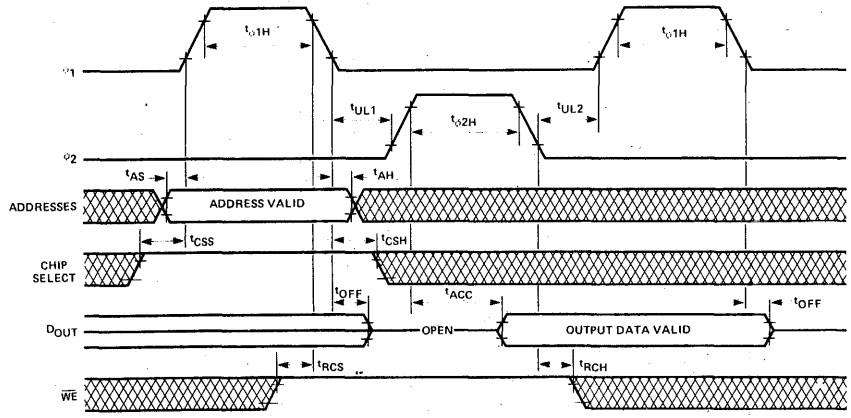
RECIRCULATE-ONLY CYCLE (STANDBY)

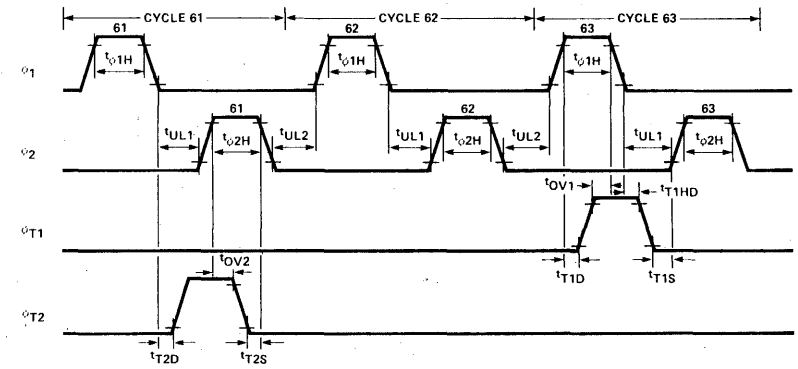


SERIAL AND TRANSFER CLOCKS



READ-RECIRCULATE-CYCLE

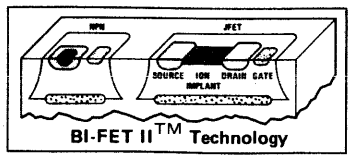




DON'T CARE CONDITION

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National Semiconductor



LF353 Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

The LF353 is a low cost high speed dual JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558.

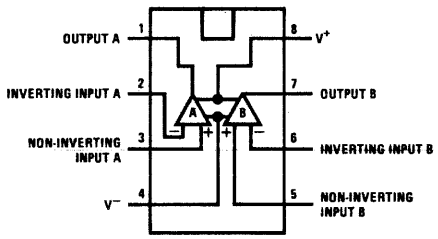
The LF353 may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

- Internally trimmed offset voltage — 2 mV
- Low input bias current — 50 pA
- Low input noise voltage — 16 nV/$\sqrt{Hz}$
- Low input noise current — 0.01 pA/$\sqrt{Hz}$
- Wide gain bandwidth — 4 MHz
- High slew rate — 13 V/μs
- Low supply current — 3.6 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp-p, BW = 20 Hz–20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

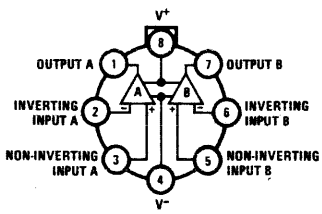
Connection Diagrams

Dual-In-Line Package



TOP VIEW

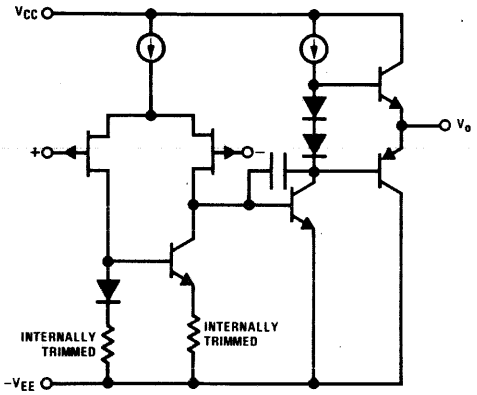
Metal Can Package (H)



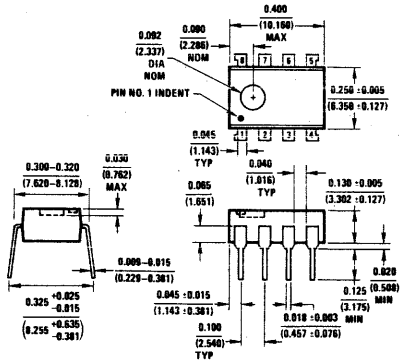
TOP VIEW

Simplified Schematic

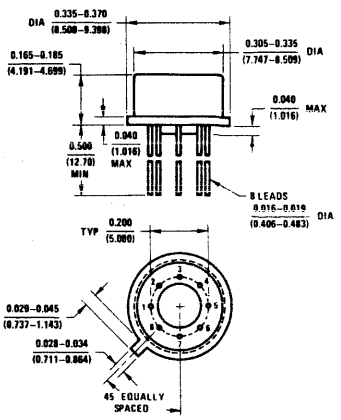
1/2 Dual



Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number LF353AN, LF353BN, or LF353N
NS Package Number N8A



TO-5 Metal Can Package (H)
Order Number LF353AH, LF353BH or LF353H
NS Package Number H08C

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IM-B10M97/Printed in U.S.A.

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Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF353A			LF353B			LF353			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C		1	2		3	5		5	10	mV
		Over Temperature			4			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10			10			10		µV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 3, 4)		25	50		25	100		25	100	pA
		$T_j \leq$ 70°C			2			4			4	nA
I_B	Input Bias Current	T_j = 25°C, (Notes 3, 4)		50	100		50	200		50	200	pA
		$T_j \leq$ 70°C			4			8			8	nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C	50	100		50	100		25	100		V/mV
		V_O = ±10V, R_L = 2 kΩ										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15		±11	+15		±11	+15		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	80	100		80	100		70	100		dB
I_S	Supply Current			3.6	5.6		3.6	5.6		3.6	6.5	mA

AC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF353A			LF353B			LF353			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	V_S = ±15V, T_A = 25°C		13			13			13		V/µs
GBW	Gain-Bandwidth Product	V_S = ±15V, T_A = 25°C		4			4			4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		16			16			16		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 135°C/W junction to ambient for the N package, and 150°C/W junction to ambient for the H package.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

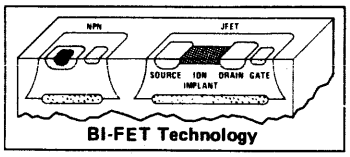
Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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National Semiconductor



BI-FET Technology

LF155/LF156/LF157 Monolithic JFET Input Operational Amplifiers

LF155, LF155A, LF255, LF355, LF355A, LF355B low supply current
LF156, LF156A, LF256, LF356, LF356A, LF356B wide band
LF157, LF157A, LF257, LF357, LF357A, LF357B wide band decompensated ($A_{V_{MIN}}$ = 5)

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET Technology). These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

Common Features

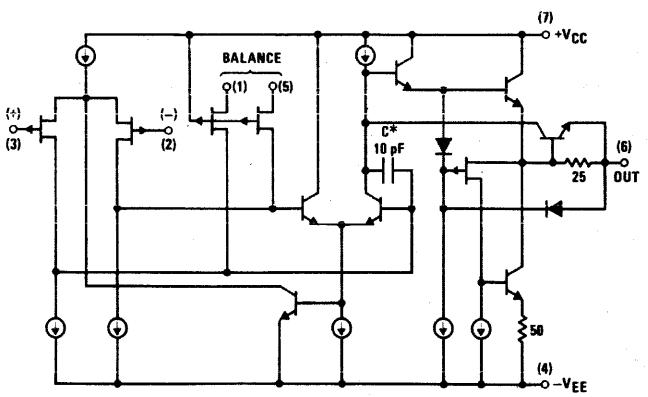
(LF155A, LF156A, LF157A)

- Low input bias current — 30 pA
- Low Input Offset Current — 3 pA
- High input impedance — $10^{12}\Omega$
- Low input offset voltage — 1 mV
- Low input offset voltage temperature drift — 3μV/°C
- Low input noise current — 0.01 pA/√Hz
- High common-mode rejection ratio — 100 dB
- Large dc voltage gain — 106 dB

Uncommon Features

	LF155A	LF156A	LF157A (A_V = 5)*	UNITS
■ Extremely fast settling time to 0.01%	4	1.5	1.5	μs
■ Fast slew rate	5	12	50	V/μs
■ Wide gain bandwidth	2.5	5	20	MHz
■ Low input noise voltage	20	12	12	nV/√Hz

Simplified Schematic



*C = 2 pF on LF157

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IM-B20M67/Printed in U.S.A.

Absolute Maximum Ratings

	LF155A/6A/7A	LF155/6/7	LF355B/6B/7B LF255/6/7 LF355B/6B/7B	LF355A/6A/7A LF355/6/7
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (P_d at 25°C) and Thermal Resistance (θ_{jA}) (Note 1)				
T_{jMAX}				
(H and J Package)	150°C	150°C	115°C	115°C
(N Package)			100°C	100°C
(H Package) P_d	670 mW	670 mW	570 mW	570 mW
θ_{jA}	150°C/W	150°C/W	150°C/W	150°C/W
(J Package) P_d	670 mW	670 mW	570 mW	570 mW
θ_{jA}	140°C/W	140°C/W	140°C/W	140°C/W
(N Package) P_d			500 mW	500 mW
θ_{jA}			155°C/W	155°C/W
Differential Input Voltage	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF155A/6A/7A			LF355A/6A/7A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		1	2		1	2	mV
		Over Temperature			2.5			2.3	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3	5		3	5	$\mu V/°C$
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		$\mu V/°C$ per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5)		3	10		3	10	pA
		$T_j \leq T_{HIGH}$			10			1	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3, 5)		30	50		30	50	pA
		$T_J \leq T_{HIGH}$			25			5	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$	50	200		50	200		V/mV
		$V_O = \pm10V$, $R_L = 2k$							
		Over Temperature	25			25			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k$	±12	±13		±12	±13		V
		$V_S = \pm15V$, $R_L = 2k$	±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15.1		±11	+15.1		V
				−12			−12		V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm15V$

SYMBOL	PARAMETER	CONDITIONS	LF155A/355A			LF156A/356A			LF157A/357A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	LF155A/6A; $A_V = 1$,	3	5		10	12					V/μs
		LF157A; $A_V = 5$							40	50		V/μs
GBW	Gain Bandwidth Product			2.5		4	4.5		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		4			1.5			1.5		μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$										
		f = 100 Hz		25			15			15		$nV/\sqrt{Hz}$
		f = 1000 Hz		25			12			12		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	f = 100 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
		f = 1000 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			3			3			3		pF

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DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF155/6/7			LF255/6/7 LF355B/6B/7B			LF355/6/7			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		3	5		3	5		3	10	mV
		Over Temperature			7			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5			5			5		$\mu V/°C$
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		$\mu V/°C$ per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5)		3	20		3	20		3	50	pA
		$T_j \leq T_{HIGH}$			20			1			2	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3, 5)		30	100		30	100		30	200	pA
		$T_J \leq T_{HIGH}$			50			5			8	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}			10^{12}		Ω
AV_{OL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$ $V_O = \pm10V$, $R_L = 2k$	50	200		50	200		25	200		V/mV
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k$	±12	±13		±12	±13		±12	±13		V
		$V_S = \pm15V$, $R_L = 2k$	±10	±12		±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15.1		±11	+15.1		±10	+15.1		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC Electrical Characteristics $T_A = 25°C$, $V_S = \pm15V$

PARAMETER	LF155A/155, LF255, LF355A/355B		LF355		LF156A/156, LF256/356B		LF356A/356		LF157A/157 LF257/357B		LF357A/357		UNITS
	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
Supply Current	2	4	2	4	5	7	5	10	5	7	5	10	mA

AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm15V$

SYMBOL	PARAMETER	CONDITIONS	LF155/255/ 355/355B	LF156/256, LF356B	LF156/256/ 356/356B	LF157/257, LF357B	LF157/257/ 357/357B	UNITS
			TYP	MIN	TYP	MIN	TYP	
SR	Slew Rate	LF155/6: $A_V = 1$,	5	7.5	12			V/μs
		LF157: $A_V = 5$				30	50	V/μs
GBW	Gain Bandwidth Product		2.5		5		20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$						
		f = 100 Hz	25		15		15	$nV/\sqrt{Hz}$
		f = 1000 Hz	20		12		12	$nV/\sqrt{Hz}$
i_n	Equivalent Input Current Noise	f = 100 Hz	0.01		0.01		0.01	$pA/\sqrt{Hz}$
		f = 1000 Hz	0.01		0.01		0.01	$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance		3		3		3	pF

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Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

	LF155A/6A/7A LF155/6/7	LF255/6/7	LF355A/6A/7A	LF355B/6B/7B	LF355/6/7
Supply Voltage, V_S	$\pm15V \le V_S \le \pm20V$	$\pm15V \le V_S \le \pm20V$	$\pm15V \le V_S \le \pm18V$	$\pm15V \le V_S \pm20V$	$V_S = \pm15V$
T_A	$-55°C \le T_A \le +125°C$	$-25°C \le T_A \le +85°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$
T_{HIGH}	+125°C	+85°C	+70°C	+70°C	+70°C

and V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \Theta_{jA}$ Pd where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

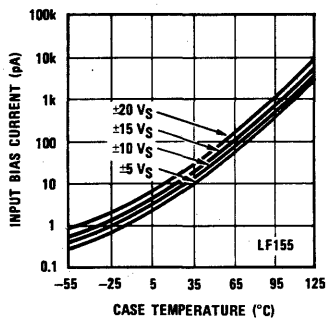
Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2 kΩ and the output step is 10V (See Settling Time Test Circuit, page 9).

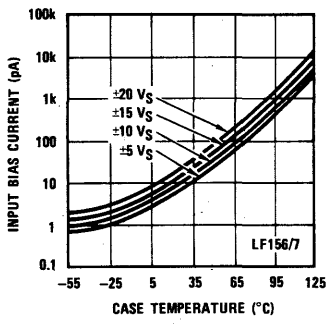
Typical DC Performance Characteristics

Curves are for LF155, LF156 and LF157 unless otherwise specified.

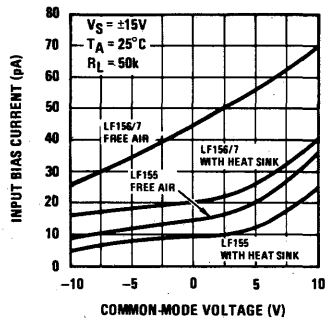
Input Bias Current



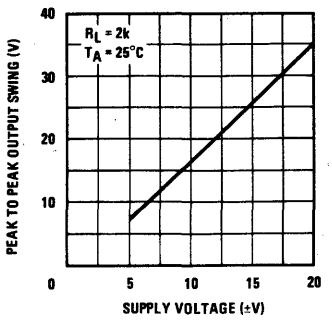
Input Bias Current



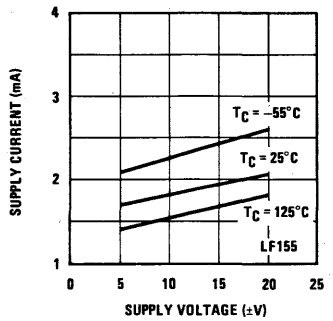
Input Bias Current



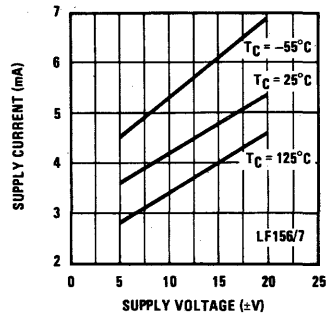
Voltage Swing



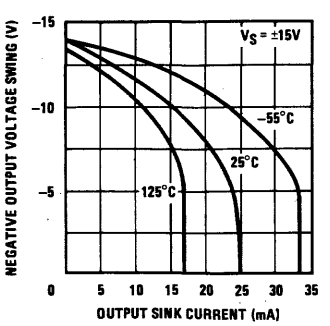
Supply Current



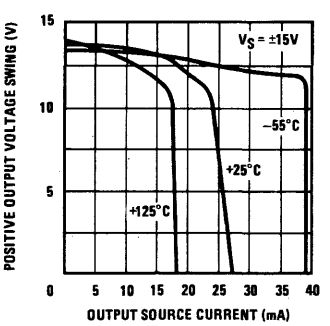
Supply Current



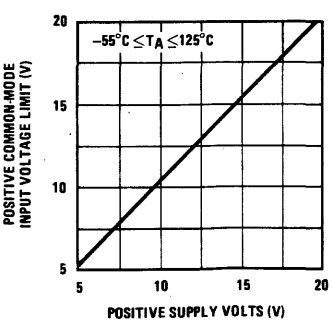
Negative Current Limit



Positive Current Limit



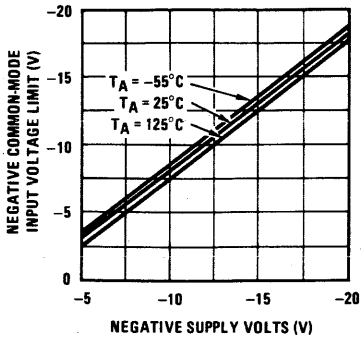
Positive Common-Mode Input Voltage Limit



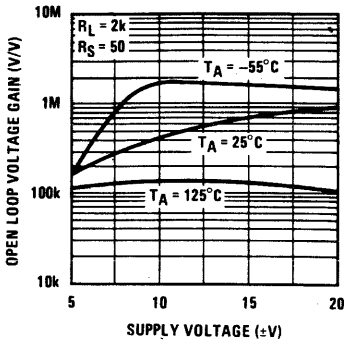
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Typical DC Performance Characteristics (Continued)

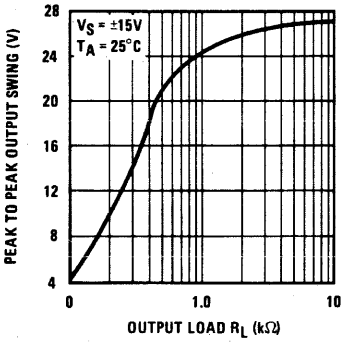
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain

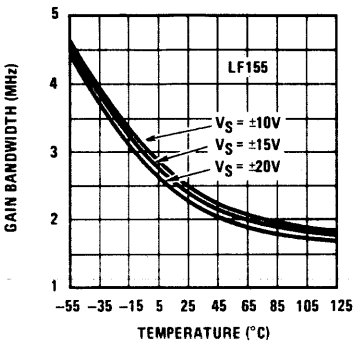


Output Voltage Swing

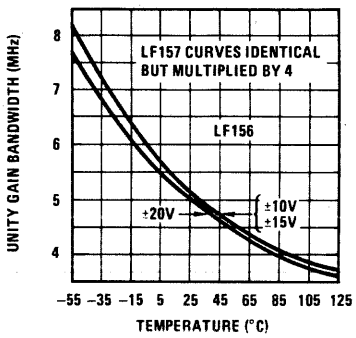


Typical AC Performance Characteristics

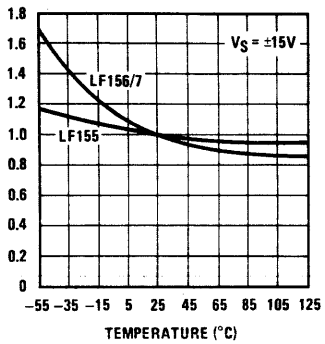
Gain Bandwidth



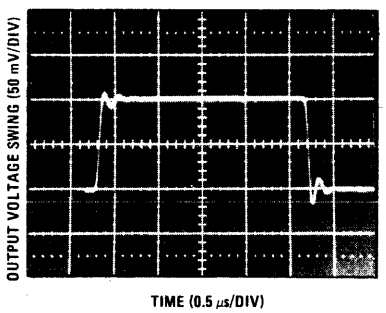
Gain Bandwidth



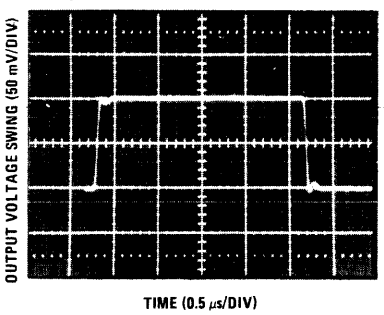
Normalized Slew Rate



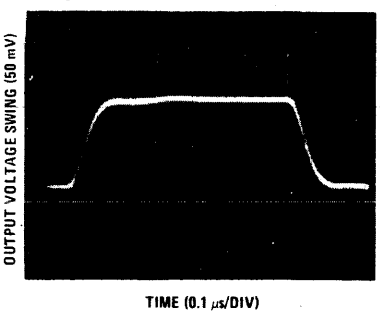
LF155 Small Signal Pulse Response, A_V = +1



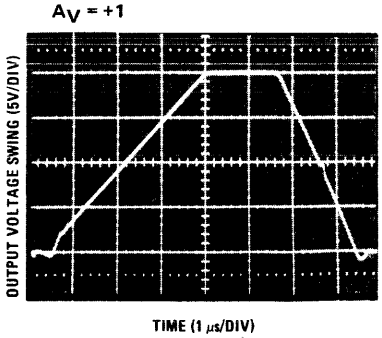
LF156 Small Signal Pulse Response, A_V = +1



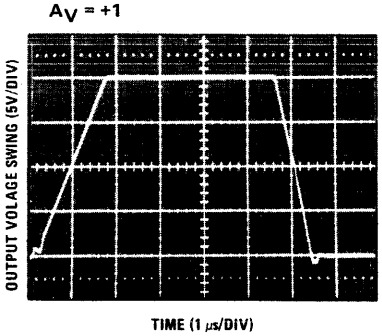
LF157 Small Signal Pulse Response, A_V = +5



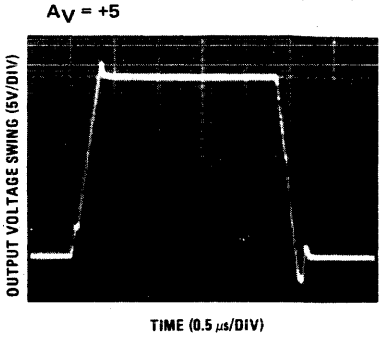
LF155 Large Signal Pulse Response, A_V = +1



LF156 Large Signal Pulse Response, A_V = +1



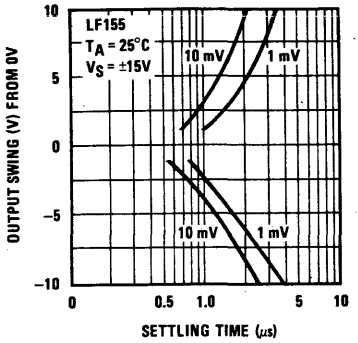
LF157 Large Signal Pulse Response, A_V = +5



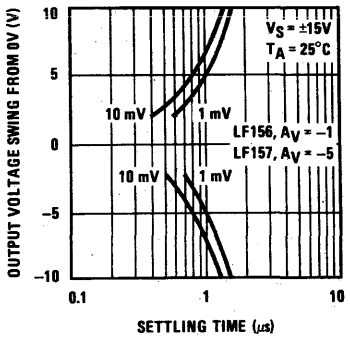
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Typical AC Performance Characteristics (Continued)

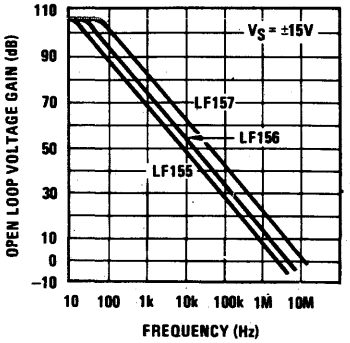
Inverter Settling Time



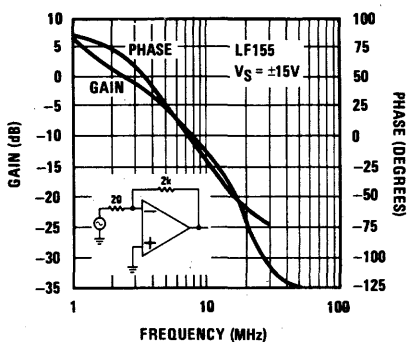
Inverter Settling Time



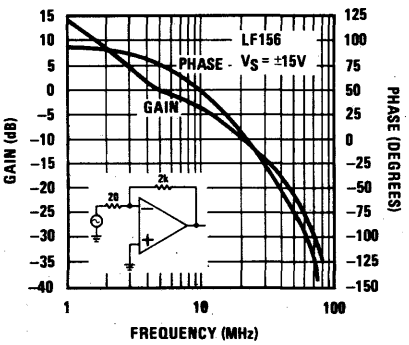
Open Loop Frequency Response



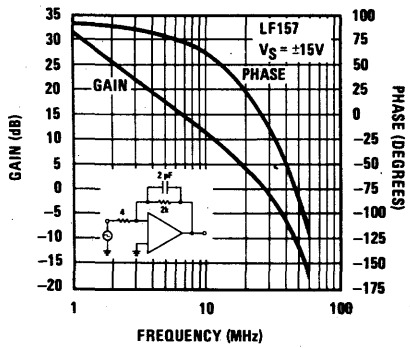
Bode Plot



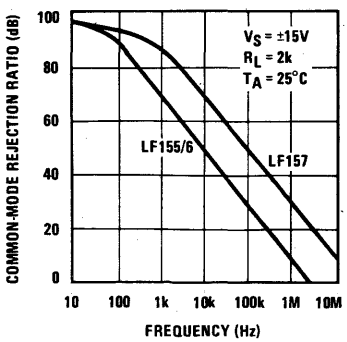
Bode Plot



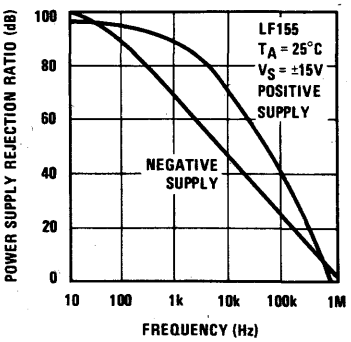
Bode Plot



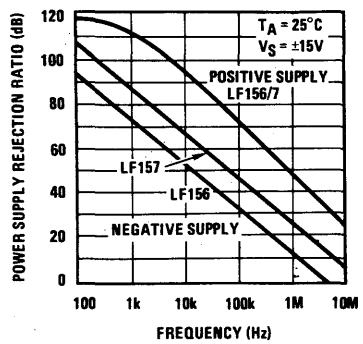
Common-Mode Rejection Ratio



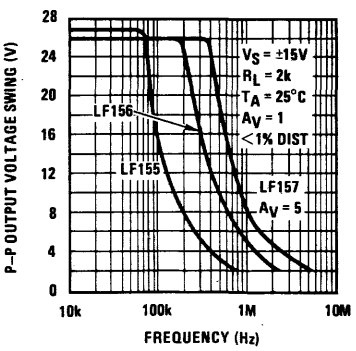
Power Supply Rejection Ratio



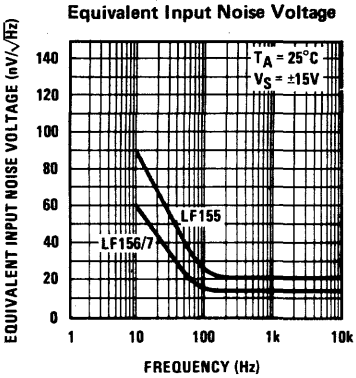
Power Supply Rejection Ratio



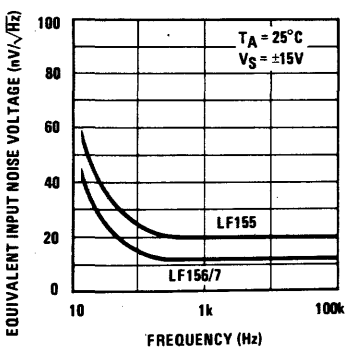
Undistorted Output Voltage Swing



Equivalent Input Noise Voltage



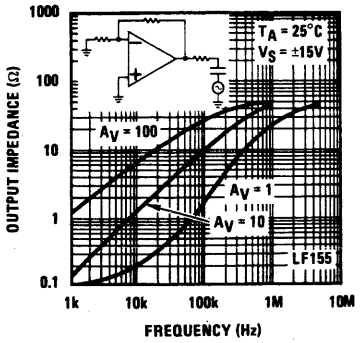
Equivalent Input Noise Voltage (Expanded Scale)



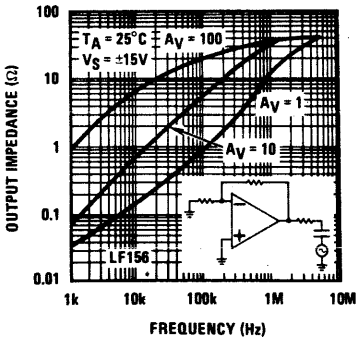
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Typical AC Performance Characteristics (Continued)

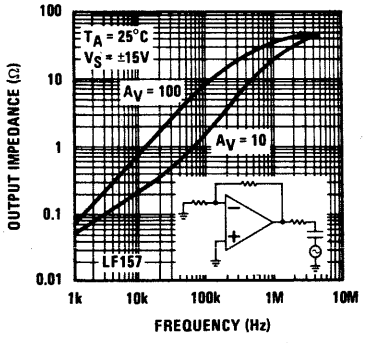
Output Impedance



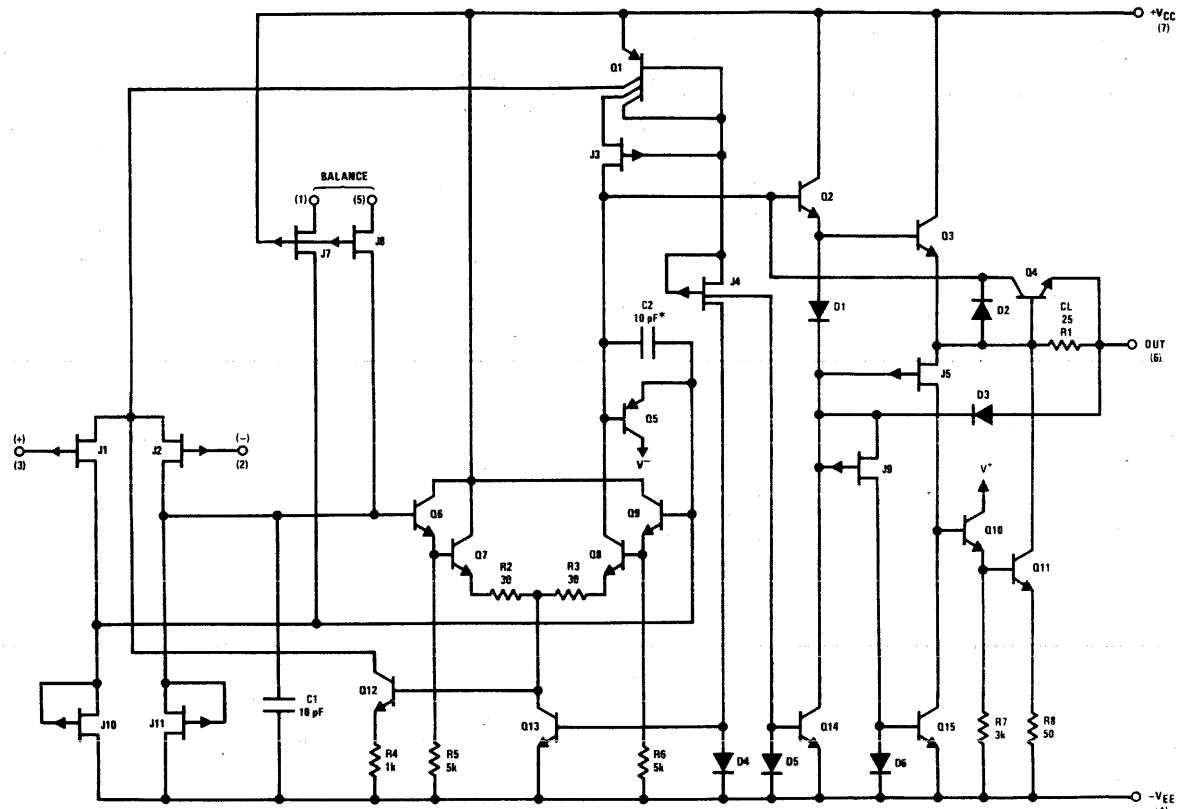
Output Impedance



Output Impedance



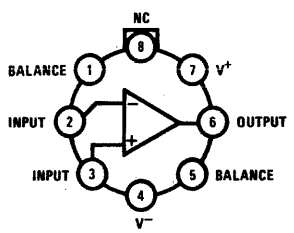
Detailed Schematic



*C = 2 pF on LF157

Connection Diagrams

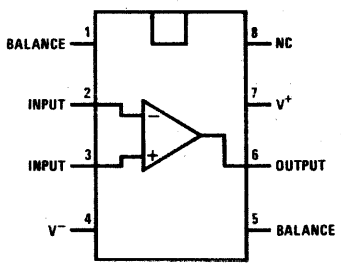
Metal Can Package (H)



Note 4: Pin 4 connected to case.

TOP VIEW

Dual-in-Line Package (N or J)



TOP VIEW

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Application Hints

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

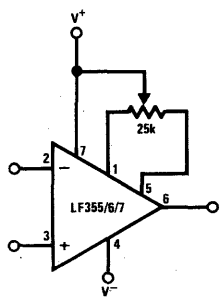
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

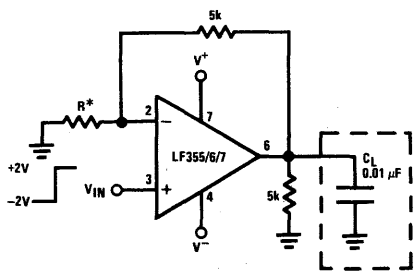
Typical Circuit Connections

V_{OS} Adjustment



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 μV/°C/mV of adjustment
- Typical overall drift: 5 μV/°C ±(0.5 μV/°C/mV of adj.)

Driving Capacitive Loads



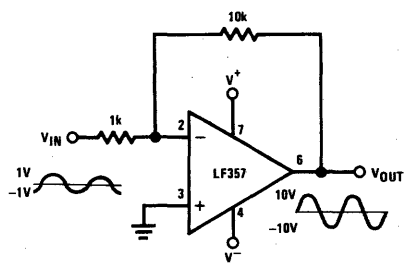
*LF155/6 R = 5k
LF157 R = 1.25k

Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \cong 0.01\ \mu F$.

Overshoot ≤ 20%

Settling time (t_s) ≅ 5 μs

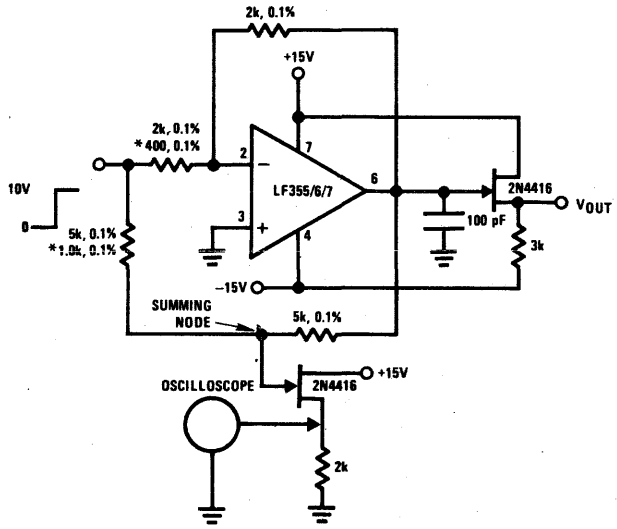
LF157. A Large Power BW Amplifier



For distortion ≤ 1% and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500 kHz.

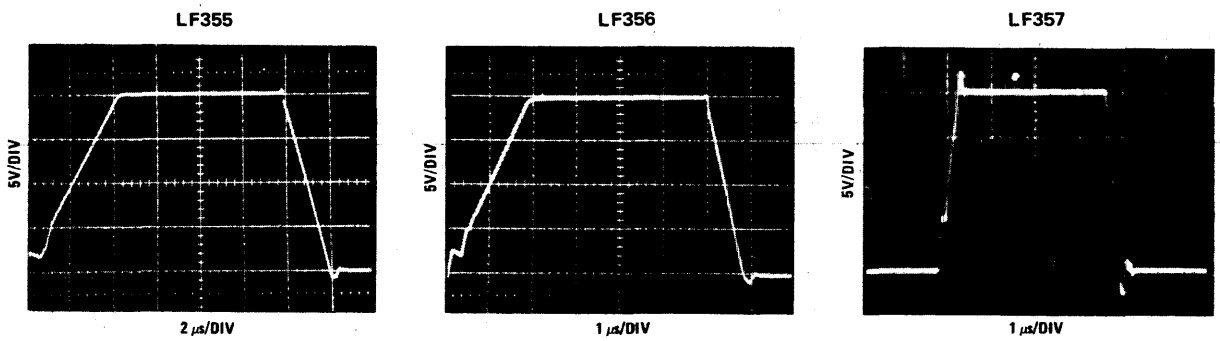
Typical Applications

Settling Time Test Circuit

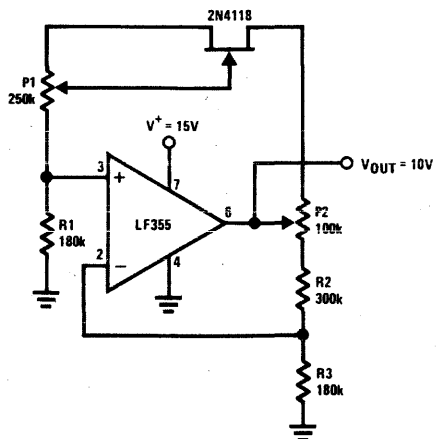


- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_V = -5$ for LF157

Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)



Low Drift Adjustable Voltage Reference

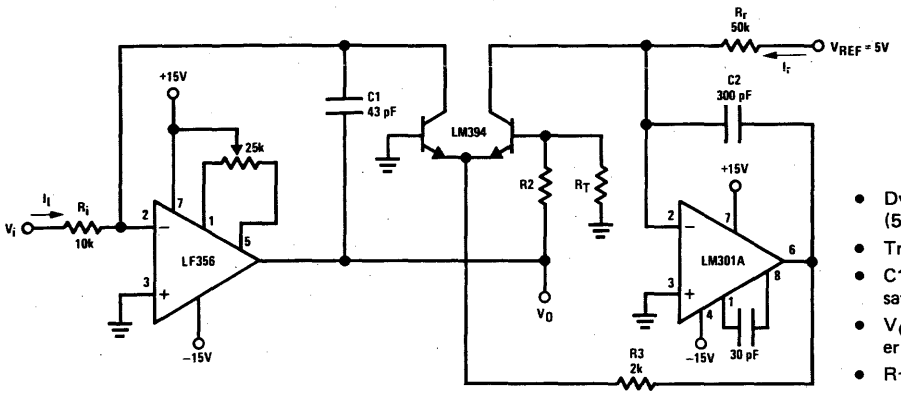


- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/°C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF155 for
  - ▲ Low I_B
  - ▲ Low drift
  - ▲ Low supply current

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Typical Applications (Continued)

Fast Logarithmic Converter

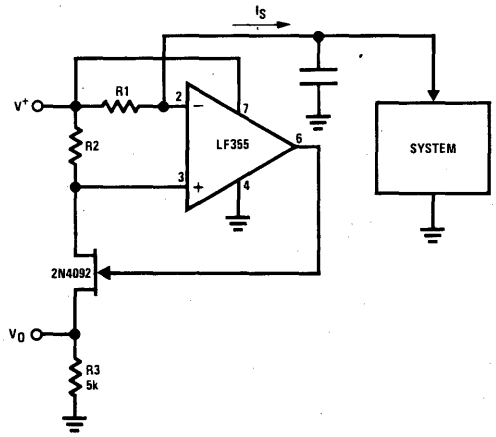


- Dynamic range: 100 μA ≤ I_i ≤ 1 mA (5 decades), $|V_O|$ = 1V/decade
- Transient response: 3 μs for ΔI_i = 1 decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C

$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right] \frac{kT}{q} \ln V_i \left[\frac{R_r}{V_{REF}\, R_i}\right] = \log V_i \frac{1}{R_i\, I_r}$$

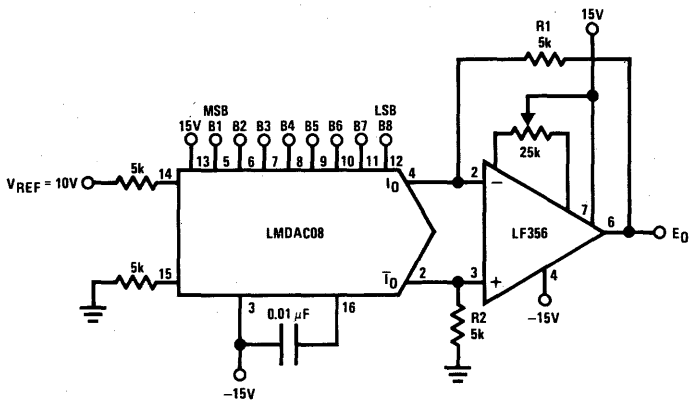
R2 = 15.7k, R_T = 1k, 0.3%/°C (for temperature compensation)

Precision Current Monitor



- V_O = 5 R1/R2 (V/mA of I_S)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
  - Common-mode range to supply range
  - Low I_B
  - Low V_{OS}
  - Low supply current

8-Bit D/A Converter with Symmetrical Offset Binary Operation



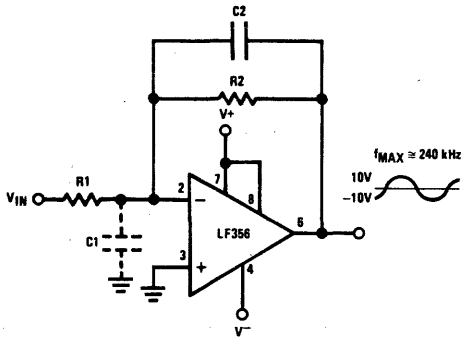
- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3 μs

E_O	B1	B2	B3	B4	B5	B6	B7	B8	COMMENTS
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
−0.040	0	1	1	1	1	1	1	1	(−) Zero-Scale
−9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

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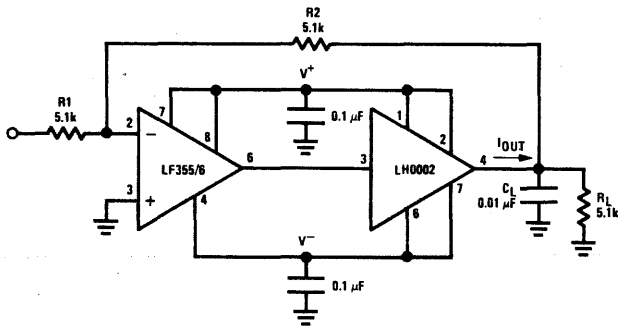
Typical Applications (Continued)

Wide BW Low Noise, Low Drift Amplifier



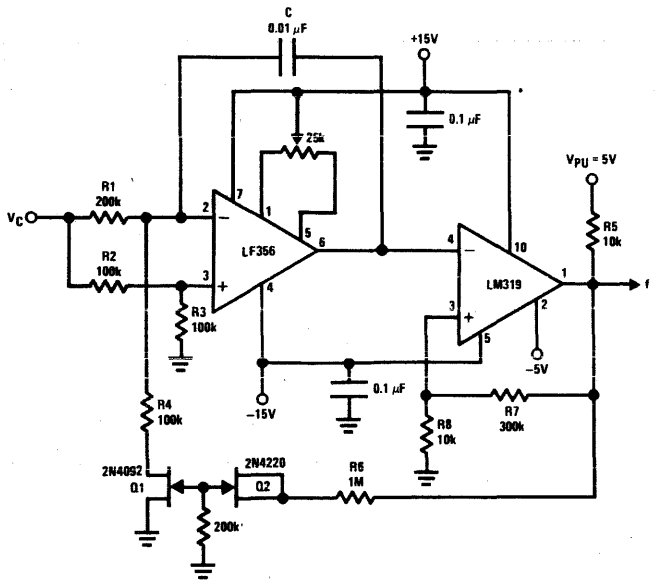
- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_P} \cong 240$ kHz
- Parasitic input capacitance C1 ≅ (3 pF for LF155, LF156 and LF157 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

Boosting the LF156 with a Current Amplifier



- $I_{OUT(MAX)} \cong 150$ mA (will drive $R_L \geq 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}}$ V/μs (with C_L shown)
- No additional phase shift added by the current amplifier

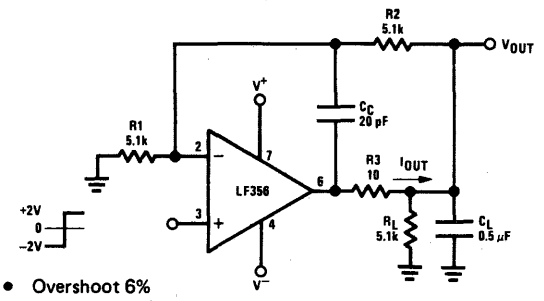
3 Decades VCO



$$f = \frac{V_C\,(R8+R7)}{[8\,V_{PU}\,R8\,R1]\,C}, \quad 0 \leq V_C \leq 30V,\ 10\text{ Hz} \leq f \leq 10\text{ kHz}$$

R1, R4 matched. Linearity 0.1% over 2 decades.

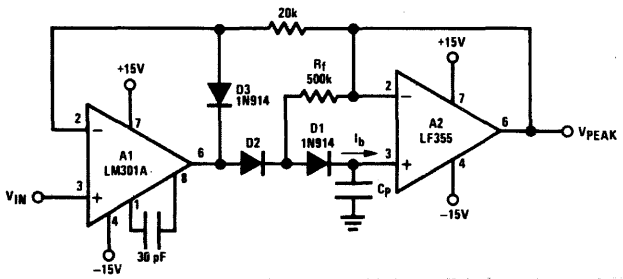
Isolating Large Capacitive Loads



- Overshoot 6%
- t_s 10 μs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

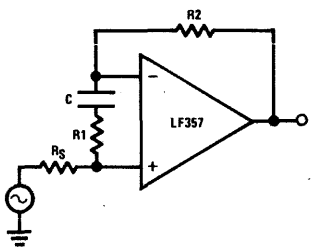
$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5}\ \text{V/μs} = 0.04\ \text{V/μs (with } C_L \text{ shown)}$$

Low Drift Peak Detector



- By adding D1 and R_f, V_{D1} = 0 during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is essentially I_b (LF155, LF156) plus capacitor leakage of C_P.
- Diode D3 clamps V_{OUT} (A1) to $V_{IN}-V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be $<< 1/2\pi R_f C_{D2}$ where C_{D2} is the shunt capacitance of D2.

Non-Inverting Unity Gain Operation for LF157



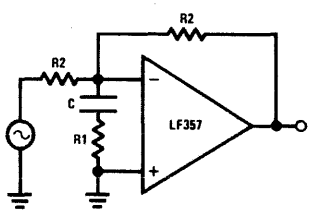
$$R1C \geq \frac{1}{(2\pi)\ (5\text{ MHz})}$$

$$R1 = \frac{R2 + R_S}{4}$$

$A_{V(DC)} = 1$

$f_{-3\text{ dB}} \approx 5$ MHz

Inverting Unity Gain for LF157



$$R1C \geq \frac{1}{(2\pi)\ (5\text{ MHz})}$$

$$R1 = \frac{R2}{4}$$

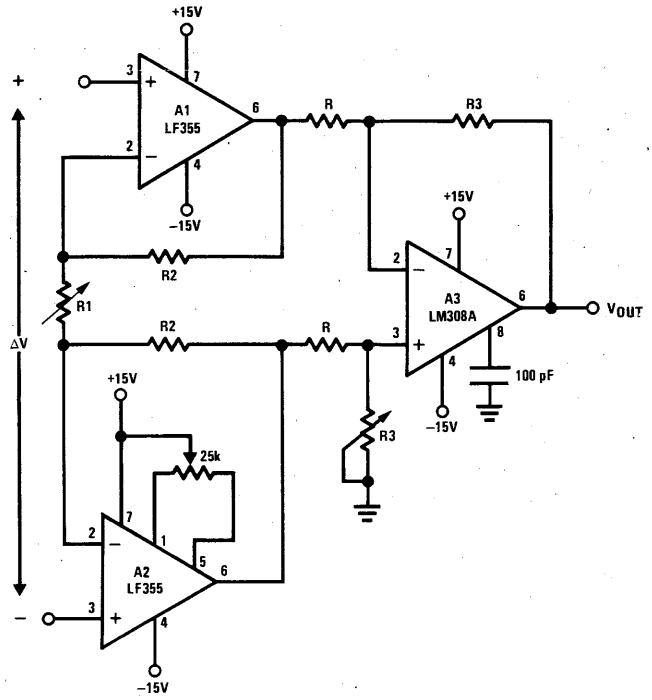
$A_{V(DC)} = -1$

$f_{-3\text{ dB}} \approx 5$ MHz

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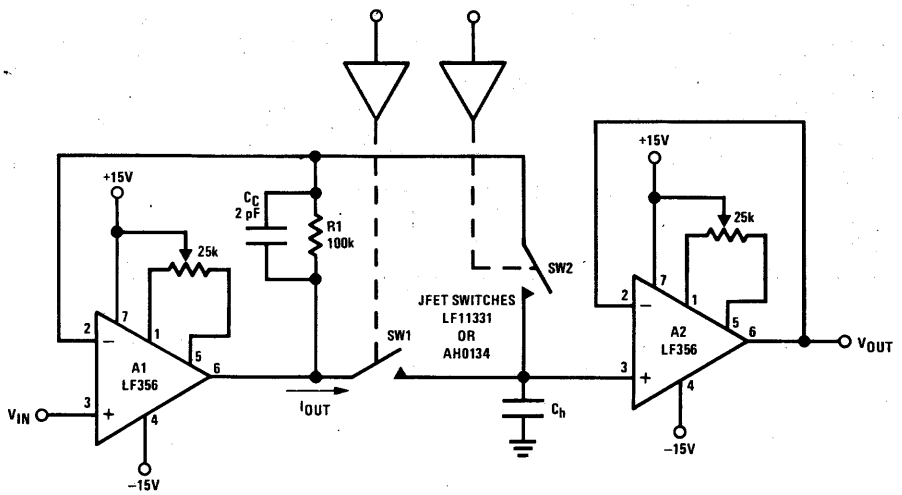
Typical Applications (Continued)

High Impedance, Low Drift Instrumentation Amplifier



- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right] \Delta V, V^- + 2V \leq V_{IN}$ common-mode $\leq V^+$
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier Resistor array RA201 (National Semiconductor) recommended

Fast Sample and Hold



- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

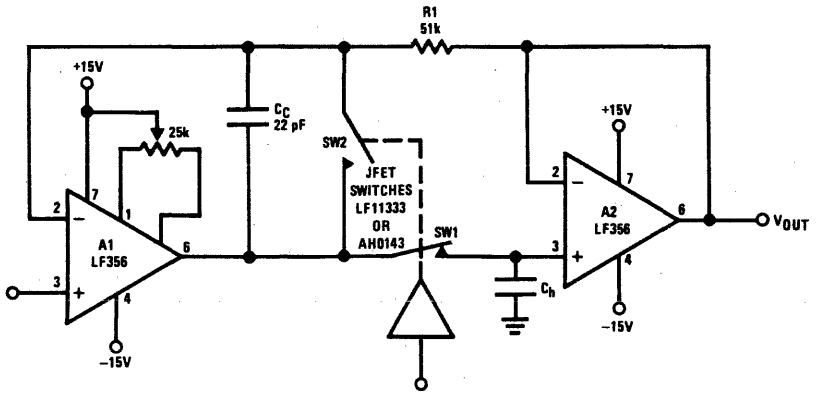
  $T_A \cong \left[\frac{2R_{ON} \cdot V_{IN} \cdot C_h}{S_r}\right]^{1/2}$ provided that:

  $V_{IN} < 2\pi S_r R_{ON} C_h$ and $T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}}$, R_{ON} is of SW1

  If inequality not satisfied: $T_A \cong \frac{V_{IN} C_h}{20\ mA}$
- LF156 developes full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

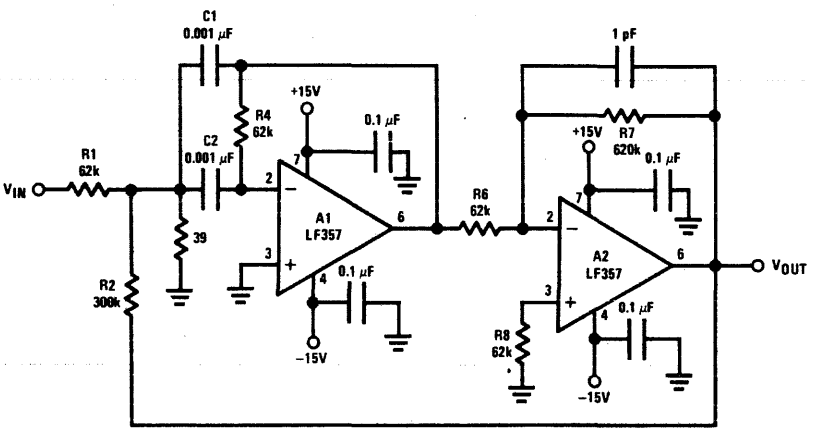
Typical Applications (Continued)

High Accuracy Sample and Hold



- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - ▲ Fast settling time
  - ▲ Low V_{OS}

High Q Band Pass Filter

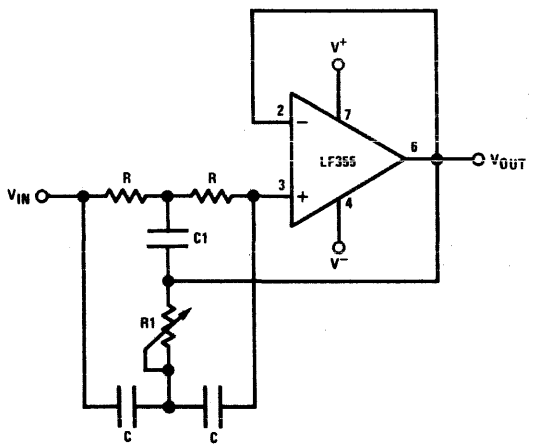


- By adding positive feedback (R2) Q increases to 40
- f_{BP} = 100 kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

- Clean layout recommended
- Response to a 1 Vp-p tone burst: 300 μs

High Q Notch Filter



- 2R1 = R = 10 MΩ
  2C = C1 = 300 pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120 Hz, notch = −55 dB, Q > 100
- Use LF155 for
  - ▲ Low I_B
  - ▲ Low supply current

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Definition of Terms

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Bias Current: The average of the two input currents.

Input Common-Mode Voltage Range: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Common-Mode Rejection Ratio: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

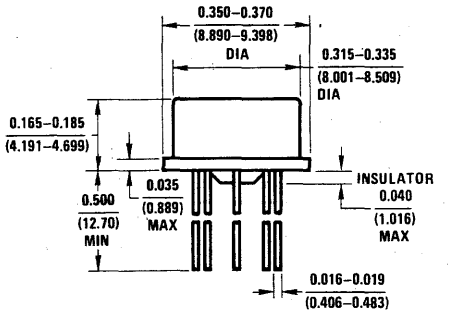
Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

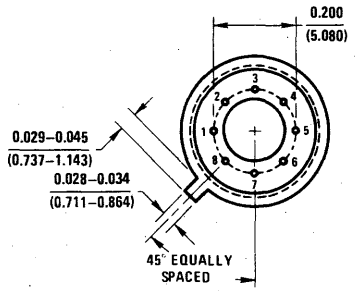
Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Power Supply Rejection Ratio: The ratio of the change in input offset voltage to the change in power supply voltage producing it. The typical curves in this sheet show values for each supply independently changed. The electrical specification, however, is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Settling Time: The time required for the error between input and output to settle to within a specified limit after an input is applied to the test circuit shown in typical applications.

Physical Dimensions inches (millimeters)

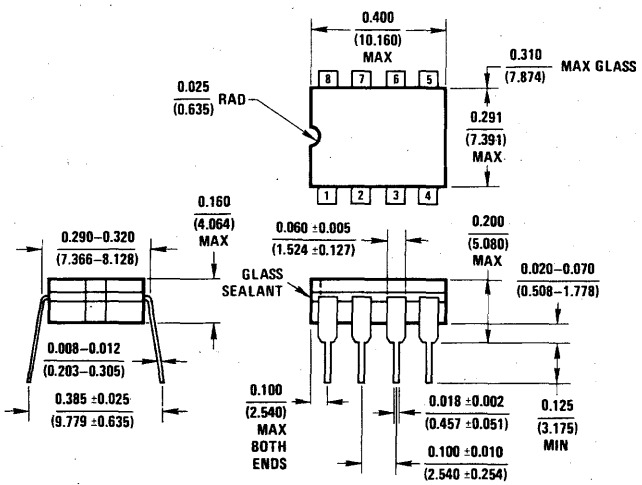




TO-99 Metal Can Package (H)
Order Number:

LF155AH	LF355AH
LF156AH	LF356AH
LF157AH	LF357AH
LF155H	LF355H
LF156H	LF356H
LF157H	LF357H
LF255H	LF355BH
LF256H	LF356BH
LF257H	LF357BH

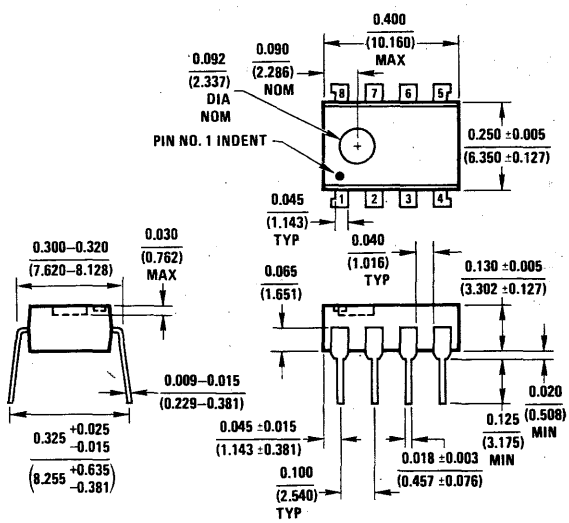
NS Package Number H08B



Cavity Dual-In-Line Package (J)
Order Number:

LF155J	LF255J	LF355J	LF355BJ
LF156J	LF256J	LF356J	LF356BJ
LF157J	LF257J	LF357J	LF357BJ

NS Package Number J08A



Molded Dual-In-Line Package (N)
Order Number:

LF355N	LF355BN	
LF356N	LF356BN	
LF357N	LF357BN	

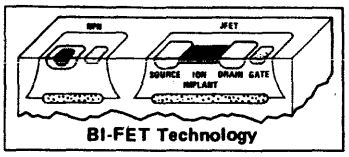
NS Package Number N08A

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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National Semiconductor



LFT155/LFT156, LFT355/LFT356 Low Offset Monolithic JFET Input Operational Amplifiers

General Description

These monolithic JFET input operational amplifiers have guaranteed low offset voltage and offset voltage drift along with high common-mode rejection which allows their use in applications requiring precision to 0.01%. In addition, they have the same low bias and offset currents, high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and low 1/f corner as do the normal LF155/LF156 BI-FET operational amplifier families.

Advantages

- Ultra-low offset—12-bit accuracy without adjust
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Output amplifiers in 10 and 12-bit current mode D/A converters
- Data acquisition front-end amplifiers: (DC coupled difference amplifier, buffer)
- Output buffer in S/H circuits
- Low pass filters with DC gain
- Amplifier for auto-zeroing loops
- Long time integrators
- Precise analog computer amplifiers and integrators
- Replace op amps in existing systems requiring:
  - Offset voltage adjustment
  - Drift selection
  - Fast settling
  - Low noise
  - Low bias current

Features

LFT155/LFT156

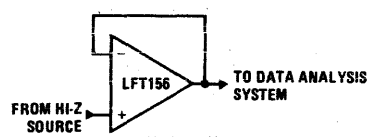
Low input offset voltage	0.5 mV max
Low input offset voltage temperature drift	5 μV/°C max
Low input bias current	50 pA max
Low input offset current	10 pA max
High common-mode rejection ratio	95 dB min
High input impedance	$10^{12}\Omega$
Low input noise current	0.01 pA/$\sqrt{Hz}$
Large DC voltage gain	106 dB

LFT156/LFT356

Fast slew rate	10 V/μs min
Wide gain bandwidth	4 MHz min
Extremely fast settling	1.5 μs to 0.01%
Low input noise voltage	12 nV/$\sqrt{Hz}$

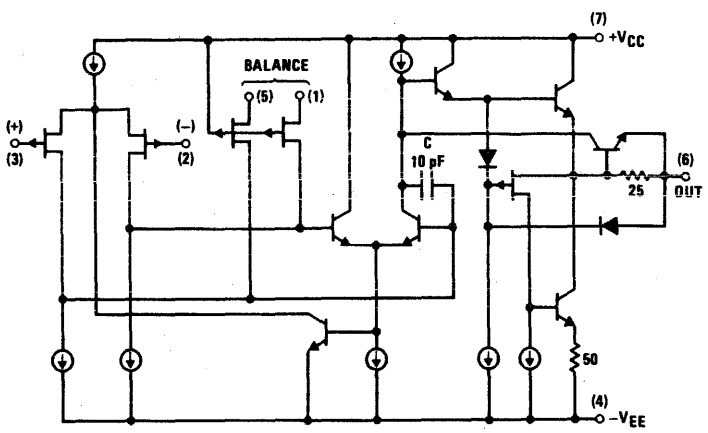
Typical Application

12-Bit Accurate Buffer



Greater than 12-bit accuracy without adjustment

Simplified Schematic



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IM-B20M107/Printed in U.S.A.

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Absolute Maximum Ratings

	LFT155/LFT156	LFT355/LFT356
Supply Voltage	±22V	±18V
Power Dissipation (P_d at 25°C)	670 mW	570 mW
and Thermal Resistance (θ_{jA}) (Note 1)	150°C/W	150°C/W
T_{jMAX}	150°C	115°C
Differential Input Voltage	±40V	±30V
Input Voltage Range (Note 2)	±20V	±16V
Output Short-Circuit Duration	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LFT155/LFT156 LFT355/LFT356			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$			0.5	mV
		Over Temperature			1.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3	5	$\mu V/°C$
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5		$\mu V/°C$ per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5)		3	10	pA
		$T_j \leq T_{HIGH}$			1	nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 5)		30	50	pA
		$T_j \leq T_{HIGH}$			5	nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$ $V_O = \pm10V$, $R_L = 2k$	50	200		V/mV
		Over Temperature	25			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k$	±12	±13		V
		$V_S = \pm15V$, $R_L = 2k$	±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15		V
				−12		V
CMRR	Common-Mode Rejection Ratio		95			dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		dB

$T_A = 25°C$, $V_S = \pm15V$

SYMBOL	PARAMETER	LFT155, LFT355			LFT156, LFT356			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
I_S	Supply Current		2	4		5	7	mA

AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm15V$

SYMBOL	PARAMETER	CONDITIONS	LFT155, LFT355			LFT156, LFT356			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	$A_V = 1$	3	5		10	12		V/μs
GBW	Gain Bandwidth Product			2.5		4	4.5		MHz
t_s	Settling Time to 0.01%	(Note 7)		4			1.5		μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$							
		f = 100 Hz		25			15		$nV/\sqrt{Hz}$
		f = 1000 Hz		20			12		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	f = 100 Hz		0.01			0.01		$pA/\sqrt{Hz}$
		f = 1000 Hz		0.01			0.01		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			3			3		pF

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Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

	LFT155/LFT156	LFT355/LFT356
Supply Voltage, V_S	$\pm 15V \leq V_S \leq \pm 20V$	$\pm 15V \leq V_S \leq \pm 18V$
T_A	$-55°C \leq T_A \leq +125°C$	$0°C \leq T_A \leq +70°C$
T_{HIGH}	+125°C	+70°C

and V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5 $\mu V/°C$ typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_d. $T_j = T_A + \Theta_{jA} P_d$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

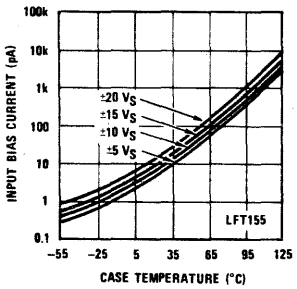
Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7; Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. See Settling Time Test Circuit.

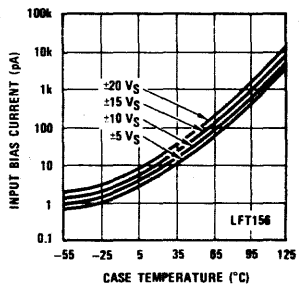
Typical DC Performance Characteristics

Curves are for LFT155 and LFT156 unless otherwise specified.

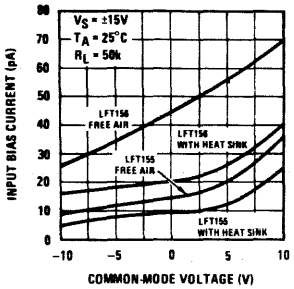
Input Bias Current



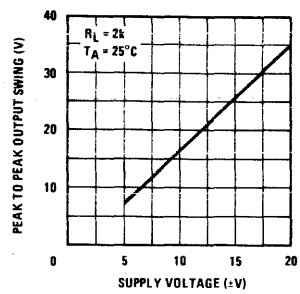
Input Bias Current



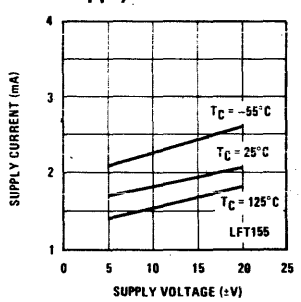
Input Bias Current



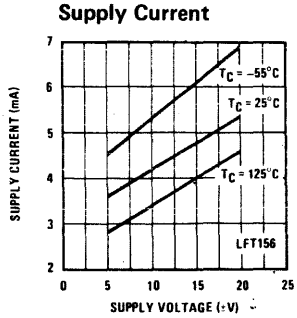
Voltage Swing



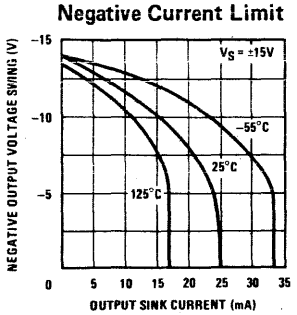
Supply Current



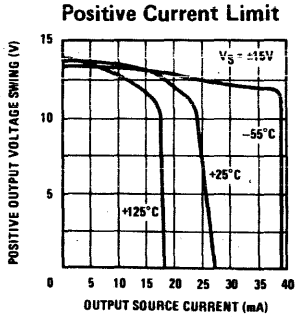
Supply Current



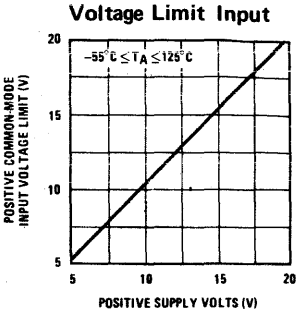
Negative Current Limit



Positive Current Limit



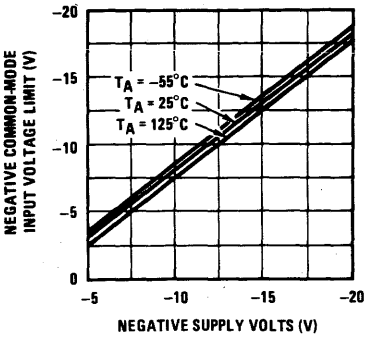
Positive Common-Mode Voltage Limit Input



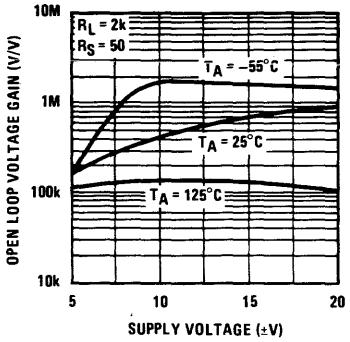
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Typical DC Performance Characteristics (Continued)

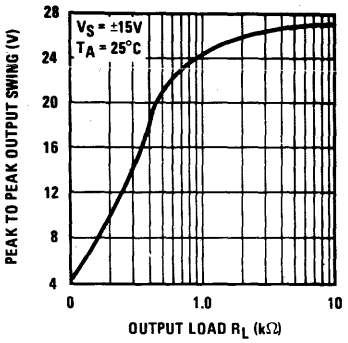
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain

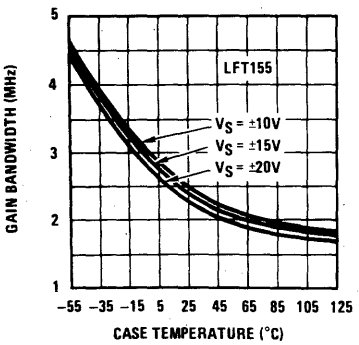


Output Voltage Swing

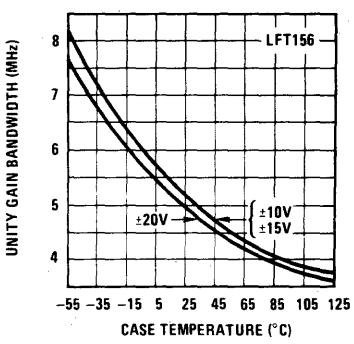


Typical AC Performance Characteristics

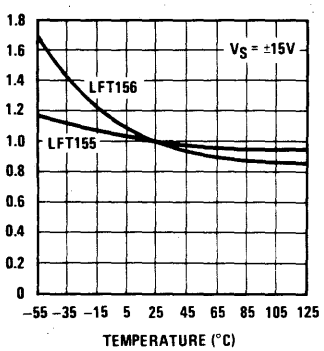
Gain Bandwidth



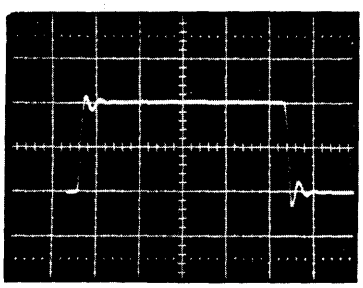
Gain Bandwidth



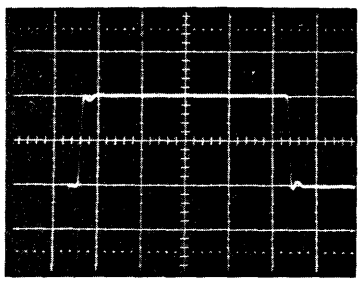
Normalized Slew Rate



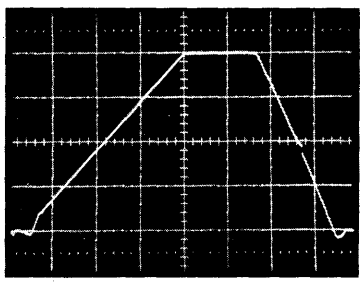
LFT155 Small Signal Pulse Response, A_V = 1



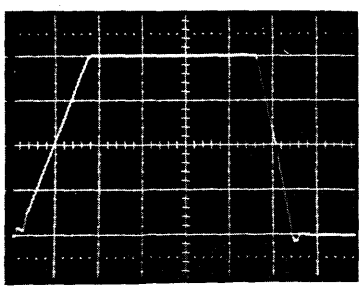
LFT156 Small Signal Pulse Response, A_V = 1



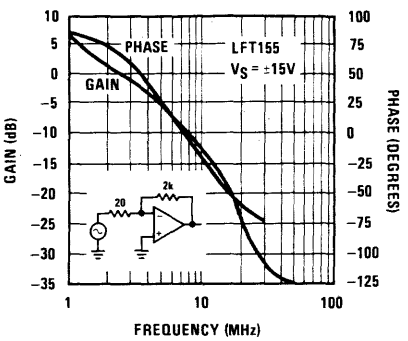
LFT155 Large Signal Pulse Response, A_V = 1



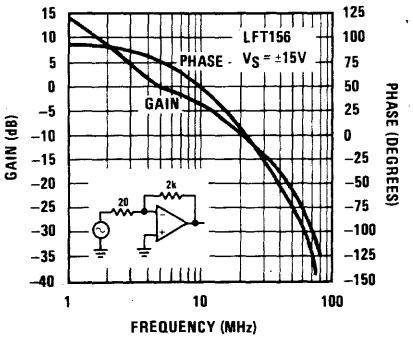
LFT156 Large Signal Pulse Response, A_V = 1



Bode Plot



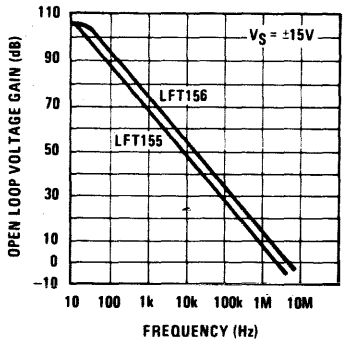
Bode Plot



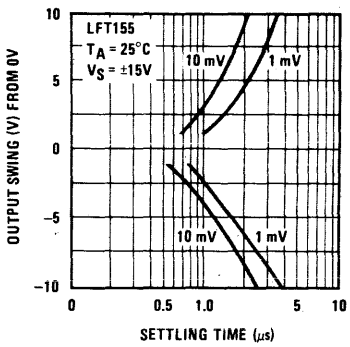
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Typical AC Performance Characteristics (Continued)

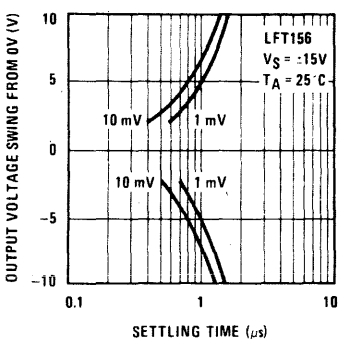
Open Loop Frequency Response



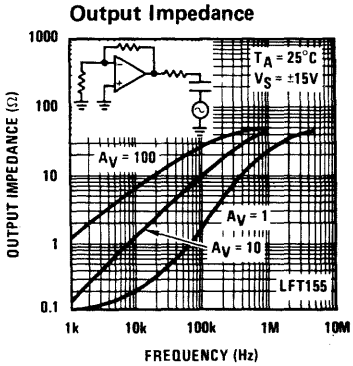
Inverter Settling Time



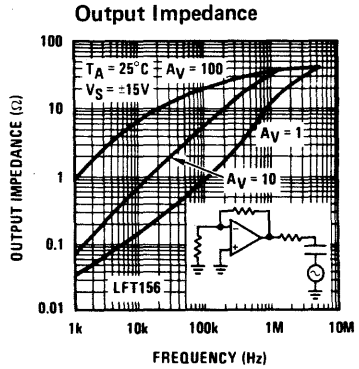
Inverter Settling Time



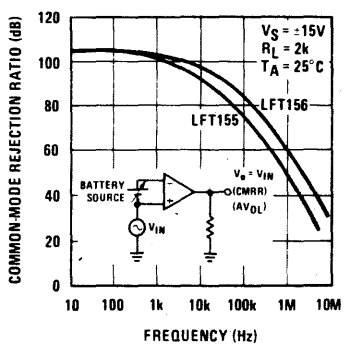
Output Impedance



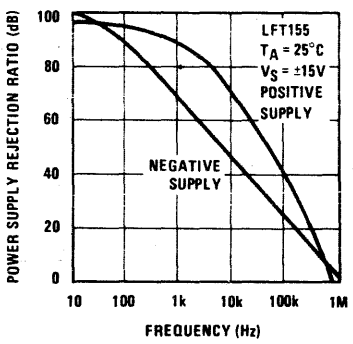
Output Impedance



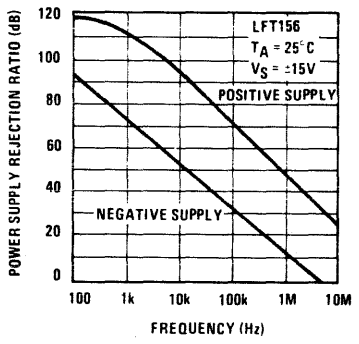
Common-Mode Rejection Ratio



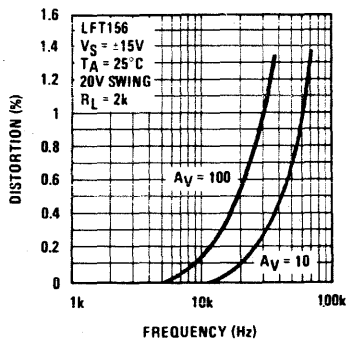
Power Supply Rejection Ratio



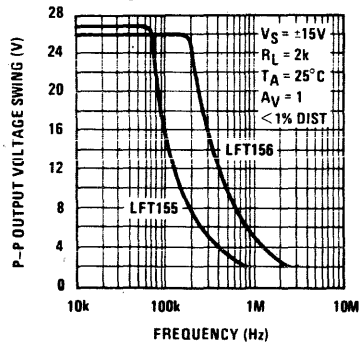
Power Supply Rejection Ratio



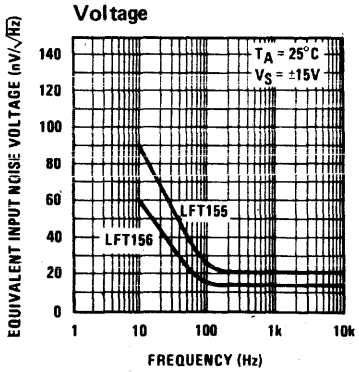
Distortion



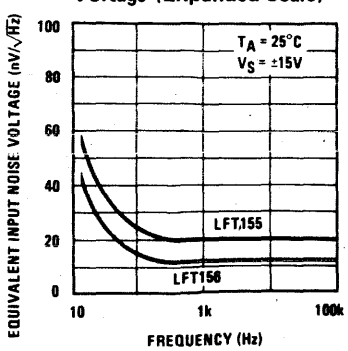
Undistorted Output Voltage Swing



Equivalent Input Noise Voltage

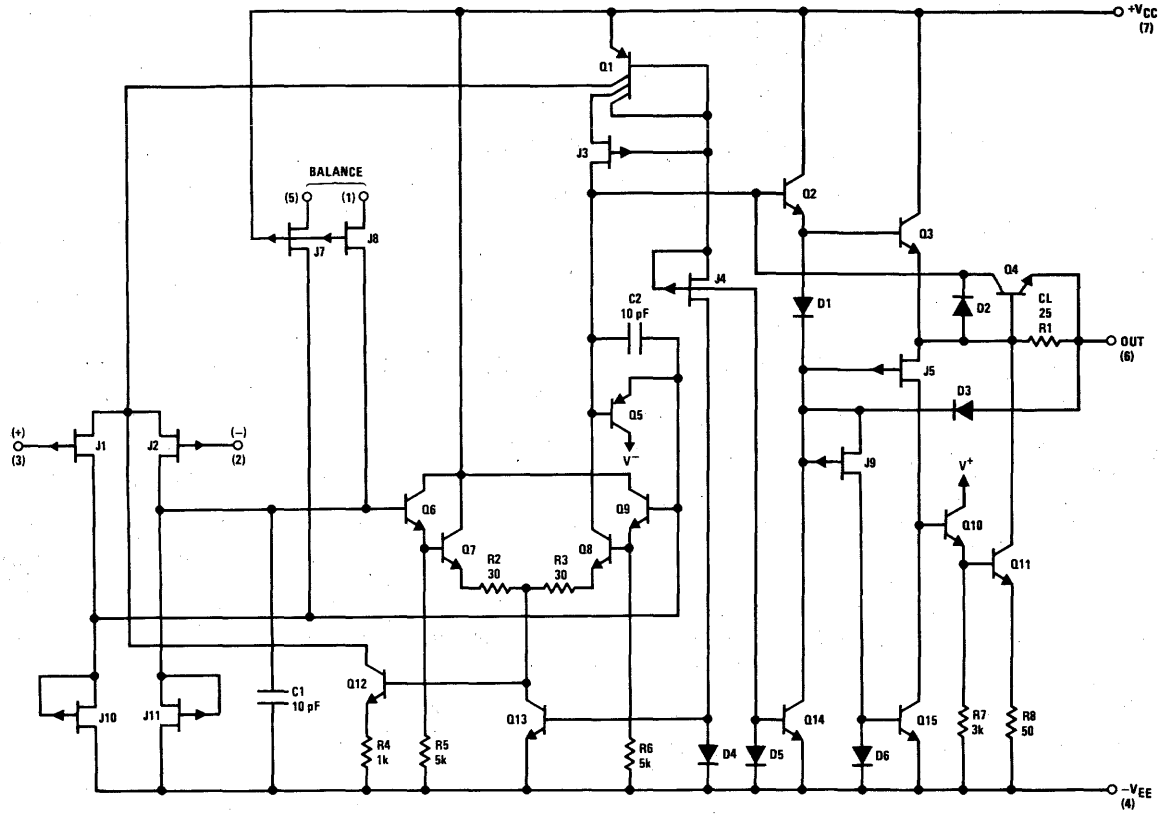


Equivalent Input Noise Voltage (Expanded Scale)



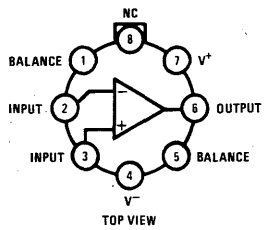
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Detailed Schematic



Connection Diagram

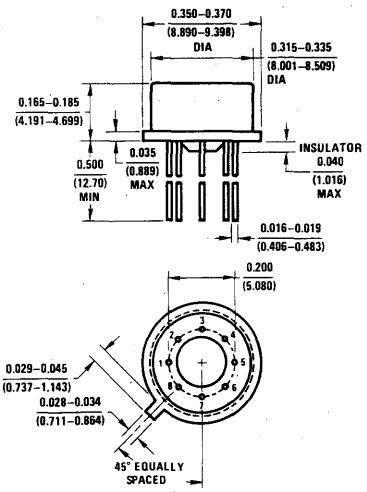
Metal Can Package



TOP VIEW

Note. Pin 4 connected to case.

Physical Dimensions inches (millimeters)



TO-99 Metal Can Package (H)
Order Number LFT155H, LFT156H, LFT355H or LFT356H
NS Package Number H08B

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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Larkfield Industrial Estate, Greenock, Scotland, Tele. (0475) 33251/Telex 778-632

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National Semiconductor

LM140A/LM140/LM340A/LM340 Series 3-Terminal Positive Regulators

General Description

The LM140A/LM140/LM340A/LM340 series of positive 3-terminal voltage regulators are designed to provide superior performance as compared to the previously available 78XX series regulator. Computer programs were used to optimize the electrical and thermal performance of the packaged IC which results in outstanding ripple rejection, superior line and load regulation in high power applications (over 15W).

With these advances in design, the LM340 is now guaranteed to have line and load regulation that is a factor of 2 better than previously available devices. Also, all parameters are guaranteed at 1A vs 0.5A output current. The LM140A/LM340A provide tighter output voltage tolerance, ±2% along with 0.01%/V line regulation and 0.3%/A load regulation.

Current limiting is included to limit peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over limiting die temperature.

Considerable effort was expended to make the LM140-XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

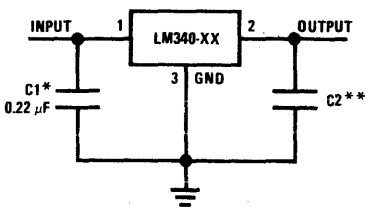
The entire LM140A/LM140/LM340A/LM340 series of regulators is available in the metal TO-3 power package and the LM340A/LM340 series is also available in the TO-220 plastic power package.

Features

- Complete specifications at 1A load
- Output voltage tolerances of ±2% at T_j = 25°C and ±4% over the temperature range (LM140A/LM340A)
- Fixed output voltages available 5, 6, 8, 10 12, 15, 18 and 24V
- Line regulation of 0.01% of V_{OUT}/V ΔV_{IN} at 1A load (LM140A/LM340A)
- Load regulation of 0.3% of V_{OUT}/A ΔI_{LOAD} (LM140A/LM340A)
- Internal thermal overload protection
- Internal short-circuit current limit
- Output transistor safe area protection

Typical Applications

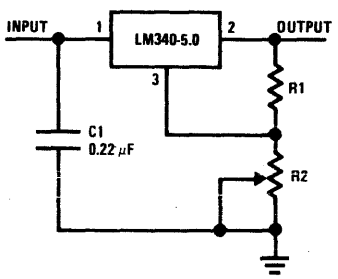
Fixed Output Regulator



*Required if the regulator is located far from the power supply filter

**Although no output capacitor is needed for stability, it does help transient response. (If needed, use 0.1 μF, ceramic disc)

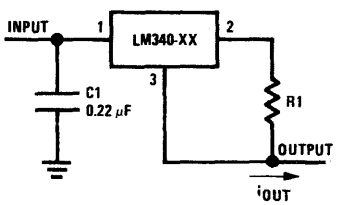
Adjustable Output Regulator



$V_{OUT} = 5V + (5V/R1 + I_Q)\,R2$

$5V/R1 > 3\,I_Q$, load regulation $(L_r) \approx [(R1 + R2)/R1]\,(L_r$ of LM340-5)

Current Regulator



$$I_{OUT} = \frac{V2\text{-}3}{R1} + I_Q$$

ΔI_Q = 1.3 mA over line and load changes

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Absolute Maximum Ratings

Input Voltage (V_O = 5V Through 18V)	35V
(V_O = 24V)	40V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range (T_A)	
LM140A/LM140	−55°C to +125°C
LM340A/LM340	0°C to +70°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	
TO-3 Package K, KC	300°C
TO-220 Package T	230°C

Electrical Characteristics LM140A/LM340A (Note 2)

I_{OUT} = 1A, −55°C ≤ T_j ≤ +150°C (LM140A), or 0°C ≤ T_j ≤ +125°C (LM340A) unless otherwise specified.

OUTPUT VOLTAGE			5V			6V			8V			10V			12V			15V			18V			24V			
INPUT VOLTAGE (unless otherwise noted)			10V			11V			14V			17V			19V			23V			27V			33V			UNITS
PARAMETER		CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	T_j = 25°C	4.9	5	5.1	5.88	6	6.12	7.84	8	8.16	9.8	10	10.2	11.75	12	12.25	14.7	15	15.3	17.64	18	18.36	23.5	24	24.5	V
		$P_D \leq$ 15W, 5 mA ≤ I_O ≤ 1A	4.8		5.2	5.76		6.24	7.7		8.3	9.6		10.4	11.5		12.5	14.4		15.6	17.3		18.7	23.0		25.0	V
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$	(7.5 ≤ V_{IN} ≤ 20)			(8.6 ≤ V_{IN} ≤ 21)			(10.6 ≤ V_{IN} ≤ 23)			(12.7 ≤ V_{IN} ≤ 25)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)			(21 ≤ V_{IN} ≤ 33)			(27.3 ≤ V_{IN} ≤ 38)			V
ΔV_O	Line Regulation	I_O = 500 mA			10			11			13			16			18			22			31			36	mV
		ΔV_{IN}	(7.5 ≤ V_{IN} ≤ 20)			(8.6 ≤ V_{IN} ≤ 21)			(10.6 ≤ V_{IN} ≤ 23)			(12.7 ≤ V_{IN} ≤ 25)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)			(21 ≤ V_{IN} ≤ 33)			(27.3 ≤ V_{IN} ≤ 38)			V
		T_j = 25°C		3	10		3	11		4	13		4	16		4	18		4	22		4	31		6	36	mV
		ΔV_{IN}	(7.3 ≤ V_{IN} ≤ 20)			(8.3 ≤ V_{IN} ≤ 21)			(10.4 ≤ V_{IN} ≤ 23)			(12.4 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 27)			(17.5 ≤ V_{IN} ≤ 30)			(20.6 ≤ V_{IN} ≤ 33)			(26.7 ≤ V_{IN} ≤ 38)			V
		T_j = 25°C			4			5			6			8			9			10			15			19	mV
		Over Temperature			12			15			20			25			30			30			45			60	mV
		ΔV_{IN}	(8 ≤ V_{IN} ≤ 12)			(9 ≤ V_{IN} ≤ 13)			(11 ≤ V_{IN} ≤ 17)			(14 ≤ V_{IN} ≤ 20)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)			(24 ≤ V_{IN} ≤ 30)			(30 ≤ V_{IN} ≤ 36)			V
ΔV_O	Load Regulation	T_j = 25°C, 5 mA ≤ I_O ≤ 1.5A		10	25		12	26		12	28		12	30		12	32		12	35		12	38		12	44	mV
		250 mA ≤ I_O ≤ 750 mA			15			16			17			18			19			21			23			26	mV
		Over Temperature, 5 mA ≤ I_O ≤ 1A			25			30			40			50			60			75			90			120	mV
I_Q	Quiescent Current	T_j = 25°C			6			6			6			6			6			6			6			6	mA
		Over Temperature			6.5			6.5			6.5			6.5			6.5			6.5			6.5			6.5	mA
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A			0.5			0.5			0.5			0.5			0.5			0.5			0.5			0.5	mA
		T_j = 25°C, I_O = 1A			0.8			0.8			0.8			0.8			0.8			0.8			0.8			0.8	mA
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$	(7.5 ≤ V_{IN} ≤ 20)			(8.6 ≤ V_{IN} ≤ 21)			(10.6 ≤ V_{IN} ≤ 23)			(12.7 ≤ V_{IN} ≤ 25)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)			(21 ≤ V_{IN} ≤ 33)			(27.3 ≤ V_{IN} ≤ 38)			V
		I_O = 500 mA			0.8			0.8			0.8			0.8			0.8			0.8			0.8			0.8	mA
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$	(8 ≤ V_{IN} ≤ 25)			(9 ≤ V_{IN} ≤ 25)			(11 ≤ V_{IN} ≤ 25)			(12.7 ≤ V_{IN} ≤ 25)			(15 ≤ V_{IN} ≤ 30)			(17.9 ≤ V_{IN} ≤ 30)			(21 ≤ V_{IN} ≤ 33)			(27.3 ≤ V_{IN} ≤ 38)			V
V_N	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 Hz		40			45			52			70			75			90			110			170		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	T_j = 25°C, f = 120 Hz, I_O = 1A or	68	80		65	78		62	76		61	74		61	72		60	70		59	69		56	66		dB
		f = 120 Hz, I_O = 500 mA,	68			65			62			61			61			60			59			56			dB
		Over Temperature,																									
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$	(8 ≤ V_{IN} ≤ 18)			(9 ≤ V_{IN} ≤ 19)			(11.5 ≤ V_{IN} ≤ 21.5)			(13.5 ≤ V_{IN} ≤ 23.5)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)			(22 ≤ V_{IN} ≤ 32)			(28 ≤ V_{IN} ≤ 38)			V
	Dropout Voltage	T_j = 25°C, I_O = 1A		2.0			2.0			2.0			2.0			2.0			2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz		8			9			12			16			18			19			22			28		mΩ
R_O	Short-Circuit Current	T_j = 25°C		2.1			2.0			1.9			1.7			1.5			1.2			0.8			0.4		A
	Peak Output Current	T_j = 25°C		2.4			2.4			2.4			2.4			2.4			2.4			2.4			2.4		A
	Average TC of V_O	Min, T_j = 0°C, I_O = 5 mA		−0.6			−0.7			−1.0			−1.2			−1.5			−1.8			−2.3			−3.0		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	T_j = 25°C	7.3			8.3			10.4			12.4			14.5			17.5			20.6			26.7			V

Note 1: Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistance of the TO-220 package (T) is typically 4°C/W junction to case and 60°C/W case to ambient.

Note 2: All characteristics are measured with a capacitor across the input of 0.22 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \leq$ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Electrical Characteristics LM140 (Note 2)

$-55°C \leq T_j \leq +150°C$ unless otherwise noted.

OUTPUT VOLTAGE			5V			6V			8V			10V			12V			15V			18V			24V			
INPUT VOLTAGE (unless otherwise noted)			10V			11V			14V			17V			19V			23V			27V			33V			UNITS
PARAMETER		CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	$T_j = 25°C$, 5 mA $\leq I_O \leq$ 1A	4.8	5	5.2	5.75	6	6.25	7.7	8	8.3	9.6	10	10.4	11.5	12	12.5	14.4	15	15.6	17.3	18	18.7	23.0	24	25.0	V
		$P_D \leq$ 15W, 5 mA $\leq I_O \leq$ 1A	4.75		5.25	5.7		6.3	7.6		8.4	9.5		10.5	11.4		12.6	14.25		15.75	17.1		18.9	22.8		25.2	V
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$		(8 ≤ V_{IN} ≤ 20)			(9 ≤ V_{IN} ≤ 21)			(11.5 ≤ V_{IN} ≤ 23)			(13.5 ≤ V_{IN} ≤ 25)			(15.5 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)			(22 ≤ V_{IN} ≤ 33)			(28 ≤ V_{IN} ≤ 38)		V
ΔV_O	Line Regulation	I_O = 500 mA, $T_j = 25°C$	3		50	3		60	4		80	4		100	4		120	4		150	4		180	6		240	mV
		ΔV_{IN}	(7 ≤ V_{IN} ≤ 25)			(8 ≤ V_{IN} ≤ 25)			(10.5 ≤ V_{IN} ≤ 25)			(12.5 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			(21 ≤ V_{IN} ≤ 33)			(27 ≤ V_{IN} ≤ 38)		V
		I_O = 500 mA, $-55°C \leq T_j \leq +150°C$			50			60			80			100			120			150			180			240	mV
		ΔV_{IN}		(8 ≤ V_{IN} ≤ 20)			(9 ≤ V_{IN} ≤ 21)			(11 ≤ V_{IN} ≤ 23)			(13 ≤ V_{IN} ≤ 25)			(15 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)			(21.5 ≤ V_{IN} ≤ 33)			(28 ≤ V_{IN} ≤ 38)		V
		$I_O \leq$ 1A, $T_j = 25°C$			50			60			80			100			120			150			180			240	mV
		ΔV_{IN}	(7.3 ≤ V_{IN} ≤ 20)			(8.35 ≤ V_{IN} ≤ 21)			(10.5 ≤ V_{IN} ≤ 23)			(12.5 ≤ V_{IN} ≤ 25)			(14.6 ≤ V_{IN} ≤ 27)			(17.7 ≤ V_{IN} ≤ 30)			(21 ≤ V_{IN} ≤ 33)			(27.1 ≤ V_{IN} ≤ 38)		V
		$I_O \leq$ 1A, $-55°C \leq T_j \leq +150°C$			25			30			40			50			60			75			90			120	mV
		ΔV_{IN}		(8 ≤ V_{IN} ≤ 12)			(9 ≤ V_{IN} ≤ 13)			(11 ≤ V_{IN} ≤ 17)			(14 ≤ V_{IN} ≤ 20)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)			(24 ≤ V_{IN} ≤ 30)			(30 ≤ V_{IN} ≤ 36)		V
ΔV_O	Load Regulation	$T_j = 25°C$, 5 mA $\leq I_O \leq$ 1.5A	10		50	12		60	12		80	12		100	12		120	12		150	12		180	12		240	mV
		250 mA $\leq I_O \leq$ 750 mA			25			30			40			50			60			75			90			120	mV
		$-55°C \leq T_j \leq +150°C$, 5 mA $\leq I_O \leq$ 1A			50			60			80			100			120			150			180			240	mV
I_Q	Quiescent Current	$I_O \leq$ 1A, $T_j = 25°C$			6			6			6			6			6			6			6			6	mA
		$-55°C \leq T_j \leq +150°C$			7			7			7			7			7			7			7			7	mA
ΔI_Q	Quiescent Current Change	5 mA $\leq I_O \leq$ 1A			0.5			0.5			0.5			0.5			0.5			0.5			0.5			0.5	mA
		$T_j = 25°C$, $I_O \leq$ 1A			0.8			0.8			0.8			0.8			0.8			0.8			0.8			0.8	mA
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$		(8 ≤ V_{IN} ≤ 20)			(9 ≤ V_{IN} ≤ 21)			(11.5 ≤ V_{IN} ≤ 23)			(13.5 ≤ V_{IN} ≤ 25)			(15 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)			(22 ≤ V_{IN} ≤ 33)			(28 ≤ V_{IN} ≤ 38)		V
		$I_O \leq$ 500 mA, $-55°C \leq T_j \leq +150°C$			0.8			0.8			0.8			0.8			0.8			0.8			0.8			0.8	mA
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$		(8 ≤ V_{IN} ≤ 25)			(9 ≤ V_{IN} ≤ 25)			(11.5 ≤ V_{IN} ≤ 25)			(13.5 ≤ V_{IN} ≤ 25)			(15 ≤ V_{IN} ≤ 30)			(18.5 ≤ V_{IN} ≤ 30)			(22 ≤ V_{IN} ≤ 33)			(28 ≤ V_{IN} ≤ 38)		V
V_N	Output Noise Voltage	$T_A = 25°C$, 10 Hz ≤ f ≤ 100 kHz		40			45			52			70			75			90			110			170		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz, $I_O \leq$ 1A, $T_j = 25°C$ or	68	80		65	78		62	76		61	74		61	72		60	70		59	69		56	66		dB
		$I_O \leq$ 500 mA, $-55°C \leq T_j \leq +150°C$	68			65			62			61			61			60			59			56			dB
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$		(8 ≤ V_{IN} ≤ 18)			(9 ≤ V_{IN} ≤ 19)			(11.5 ≤ V_{IN} ≤ 21.5)			(13.5 ≤ V_{IN} ≤ 23.5)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)			(22 ≤ V_{IN} ≤ 32)			(28 ≤ V_{IN} ≤ 38)		V
	Dropout Voltage	$T_j = 25°C$, I_{OUT} = 1A		2.0			2.0			2.0			2.0			2.0			2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz		8			9			12			16			18			19			22			28		mΩ
R_O	Short-Circuit Current	$T_j = 25°C$		2.1			2.0			1.9			1.7			1.5			1.2			0.8			0.4		A
	Peak Output Current	$T_j = 25°C$		2.4			2.4			2.4			2.4			2.4			2.4			2.4			2.4		A
	Average TC of V_{OUT}	$0°C \leq T_j \leq +150°C$, I_O = 5 mA		−0.6			−0.7			−1.0			−1.2			−1.5			−1.8			−2.3			−3.0		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	$T_j = 25°C$, $I_O \leq$ 1A	7.3			8.35			10.5			12.5			14.6			17.7			21			27.1			V

Note 2: All characteristics are measured with a capacitor across the input of 0.22 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \leq$ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

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Electrical Characteristics LM340 (Note 2)

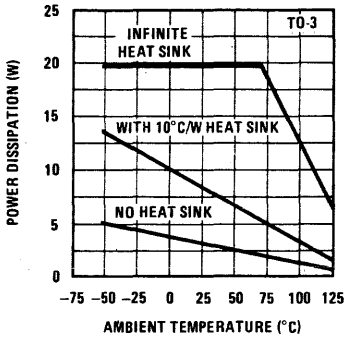
$0°C \leq T_j \leq +125°C$ unless otherwise noted.

OUTPUT VOLTAGE				5V			6V			8V			10V			12V			15V			18V			24V			
INPUT VOLTAGE (unless otherwise noted)				10V			11V			14V			17V			19V			23V			27V			33V			UNITS
PARAMETER		CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	$T_j = 25°C$, 5 mA $\leq I_O \leq$ 1A		4.8	5	5.2	5.75	6	6.25	7.7	8	8.3	9.6	10	10.4	11.5	12	12.5	14.4	15	15.6	17.3	18	18.7	23.0	24	25.0	V
		$P_D \leq$ 15W, 5 mA $\leq I_O \leq$ 1A		4.75		5.25	5.7		6.3	7.6		8.4	9.5		10.5	11.4		12.6	14.25		15.75	17.1		18.9	22.8		25.2	V
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$		(7 ≤ V_{IN} ≤ 20)			(8 ≤ V_{IN} ≤ 21)			(10.5 ≤ V_{IN} ≤ 23)			(12.5 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 27)			(17.5 < V_{IN} ≤ 30)			(21 ≤ V_{IN} ≤ 33)			(27 ≤ V_{IN} ≤ 38)			V
ΔV_O	Line Regulation	I_O = 500 mA	$T_j = 25°C$		3	50		3	60		4	80		4	100		4	120		4	150		4	180		6	240	mV
			ΔV_{IN}	(7 ≤ V_{IN} ≤ 25)			(8 ≤ V_{IN} ≤ 25)			(10.5 ≤ V_{IN} ≤ 25)			(12.5 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			(21 ≤ V_{IN} ≤ 33)			(27 ≤ V_{IN} ≤ 38)			V
			0°C ≤ T_j ≤ +125°C			50			60			80			100			120			150			180			240	mV
			ΔV_{IN}	(8 ≤ V_{IN} ≤ 20)			(9 ≤ V_{IN} ≤ 21)			(11 ≤ V_{IN} ≤ 23)			(13 ≤ V_{IN} ≤ 25)			(15 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)			(21.5 ≤ V_{IN} ≤ 33)			(28 ≤ V_{IN} ≤ 38)			V
		$I_O \leq$ 1A	$T_j = 25°C$			50			60			80			100			120			150			180			240	mV
			ΔV_{IN}	(7.3 ≤ V_{IN} ≤ 20)			(8.35 ≤ V_{IN} ≤ 21)			(10.5 ≤ V_{IN} ≤ 23)			(12.5 ≤ V_{IN} ≤ 25)			(14.6 ≤ V_{IN} ≤ 27)			(17.7 ≤ V_{IN} ≤ 30)			(21 ≤ V_{IN} ≤ 33)			(27.1 ≤ V_{IN} ≤ 38)			V
			0°C ≤ T_j ≤ +125°C			25			30			40			50			60			75			90			120	mV
			ΔV_{IN}	(8 ≤ V_{IN} ≤ 12)			(9 ≤ V_{IN} ≤ 13)			(11 ≤ V_{IN} ≤ 17)			(14 ≤ V_{IN} ≤ 20)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)			(24 ≤ V_{IN} ≤ 30)			(30 ≤ V_{IN} ≤ 36)			V
ΔV_O	Load Regulation	$T_j = 25°C$	5 mA ≤ I_O ≤ 1.5A		10	50		12	60		12	80		12	100		12	120		12	150		12	180		12	240	mV
			250 mA ≤ I_O ≤ 750 mA			25			30			40			50			60			75			90			120	mV
		5 mA ≤ I_O ≤ 1A, 0°C ≤ T_j ≤ +125°C				50			60			80			100			120			150			180			240	mV
I_Q	Quiescent Current	$I_O \leq$ 1A	$T_j = 25°C$			8			8			8			8			8			8			8			8	mA
			0°C ≤ T_j ≤ +125°C			8.5			8.5			8.5			8.5			8.5			8.5			8.5			8.5	mA
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A				0.5			0.5			0.5			0.5			0.5			0.5			0.5			0.5	mA
		$T_j = 25°C$, $I_O \leq$ 1A				1.0			1.0			1.0			1.0			1.0			1.0			1.0			1.0	mA
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$		(7.5 ≤ V_{IN} ≤ 20)			(8.6 ≤ V_{IN} ≤ 21)			(10.6 ≤ V_{IN} ≤ 23)			(12.7 ≤ V_{IN} ≤ 25)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)			(21 ≤ V_{IN} ≤ 33)			(27.3 ≤ V_{IN} ≤ 38)			V
		$I_O \leq$ 500 mA, 0°C ≤ T_j ≤ +125°C				1.0			1.0			1.0			1.0			1.0			1.0			1.0			1.0	mA
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$		(7 ≤ V_{IN} ≤ 25)			(8 ≤ V_{IN} ≤ 25)			(10.5 ≤ V_{IN} ≤ 25)			(12.5 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			(21 ≤ V_{IN} ≤ 33)			(27 ≤ V_{IN} ≤ 38)			V
V_N	Output Noise Voltage	$T_A = 25°C$, 10 Hz ≤ f ≤ 100 kHz			40			45			52			70			75			90			110			170		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz	$I_O \leq$ 1A, $T_j = 25°C$ or	62	80		59	78		56	76		55	74		55	72		54	70		53	69		50	66		dB
			$I_O \leq$ 500 mA, 0°C ≤ T_j ≤ +125°C	62			59			56			55			55			54			53			50			dB
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$		(8 ≤ V_{IN} ≤ 18)			(9 ≤ V_{IN} ≤ 19)			(11.5 ≤ V_{IN} ≤ 21.5)			(13.5 ≤ V_{IN} ≤ 23.5)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)			(22 ≤ V_{IN} ≤ 32)			(28 ≤ V_{IN} ≤ 38)			V
R_O	Dropout Voltage	$T_j = 25°C$, I_{OUT} = 1A			2.0			2.0			2.0			2.0			2.0			2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz			8			9			12			16			18			19			22			28		mΩ
	Short-Circuit Current	$T_j = 25°C$			2.1			2.0			1.9			1.7			1.5			1.2			0.8			0.4		A
	Peak Output Current	$T_j = 25°C$			2.4			2.4			2.4			2.4			2.4			2.4			2.4			2.4		A
	Average TC of V_{OUT}	0°C ≤ T_j ≤ +150°C, I_O = 5 mA			−0.6			−0.7			−1.0			−1.2			−1.5			−1.8			−2.3			−3.0		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	$T_j = 25°C$, $I_O \leq$ 1A		7.3			8.35			10.5			12.5			14.6			17.7			21			27.1			V

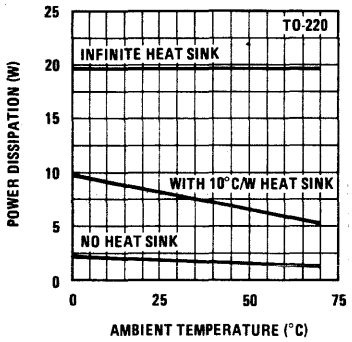
Note 2: All characteristics are measured with a capacitor across the input of 0.22 μF and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq$ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Characteristics

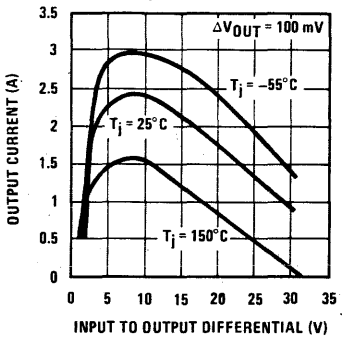
Maximum Average Power Dissipation



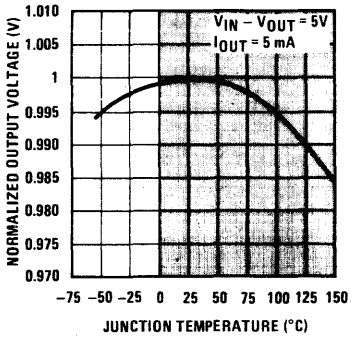
Maximum Average Power Dissipation



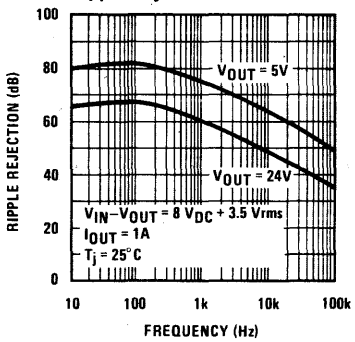
Peak Output Current



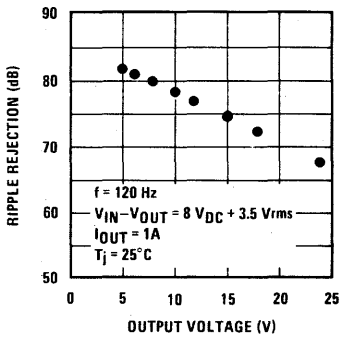
Output Voltage (Normalized to 1V at $T_j = 25°C$)



Ripple Rejection

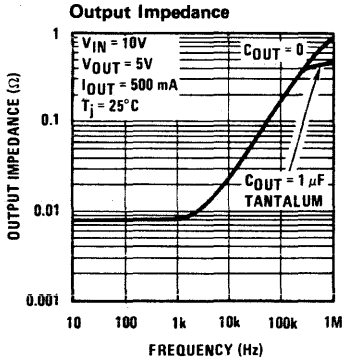


Ripple Rejection

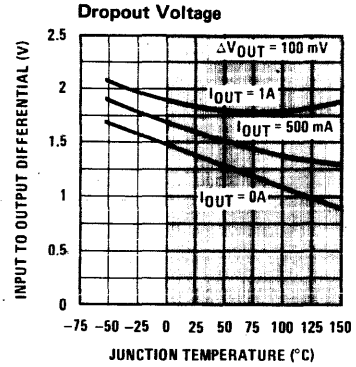


Note. Shaded area refers to LM340A/LM340

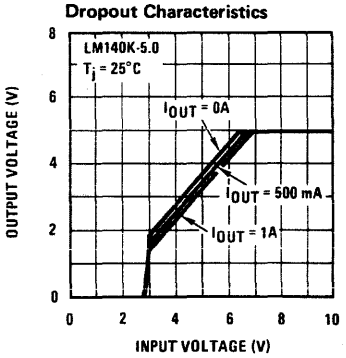
Output Impedance



Dropout Voltage

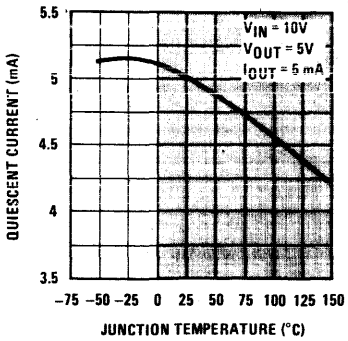


Dropout Characteristics

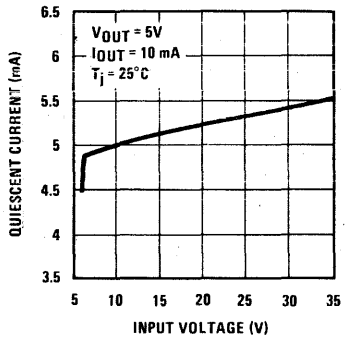


Note. Shaded area refers to LM340A/LM340

Quiescent Current



Quiescent Current

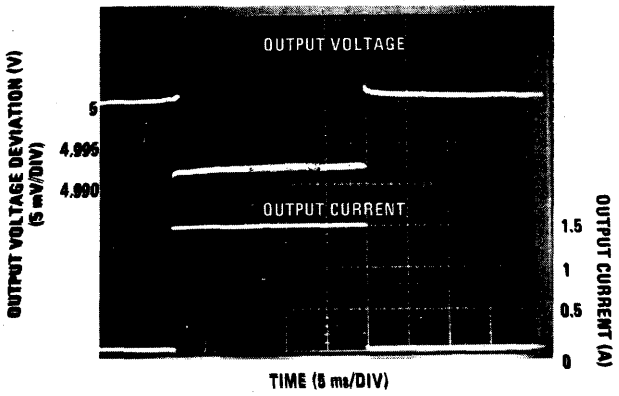


Note. Shaded area refers to LM340A/LM340

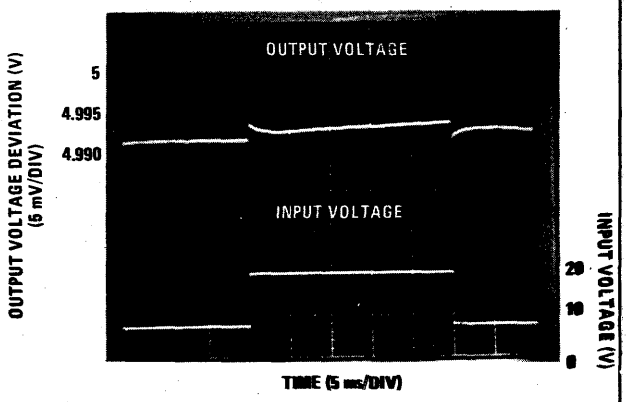
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Typical Performance Characteristics (Continued)

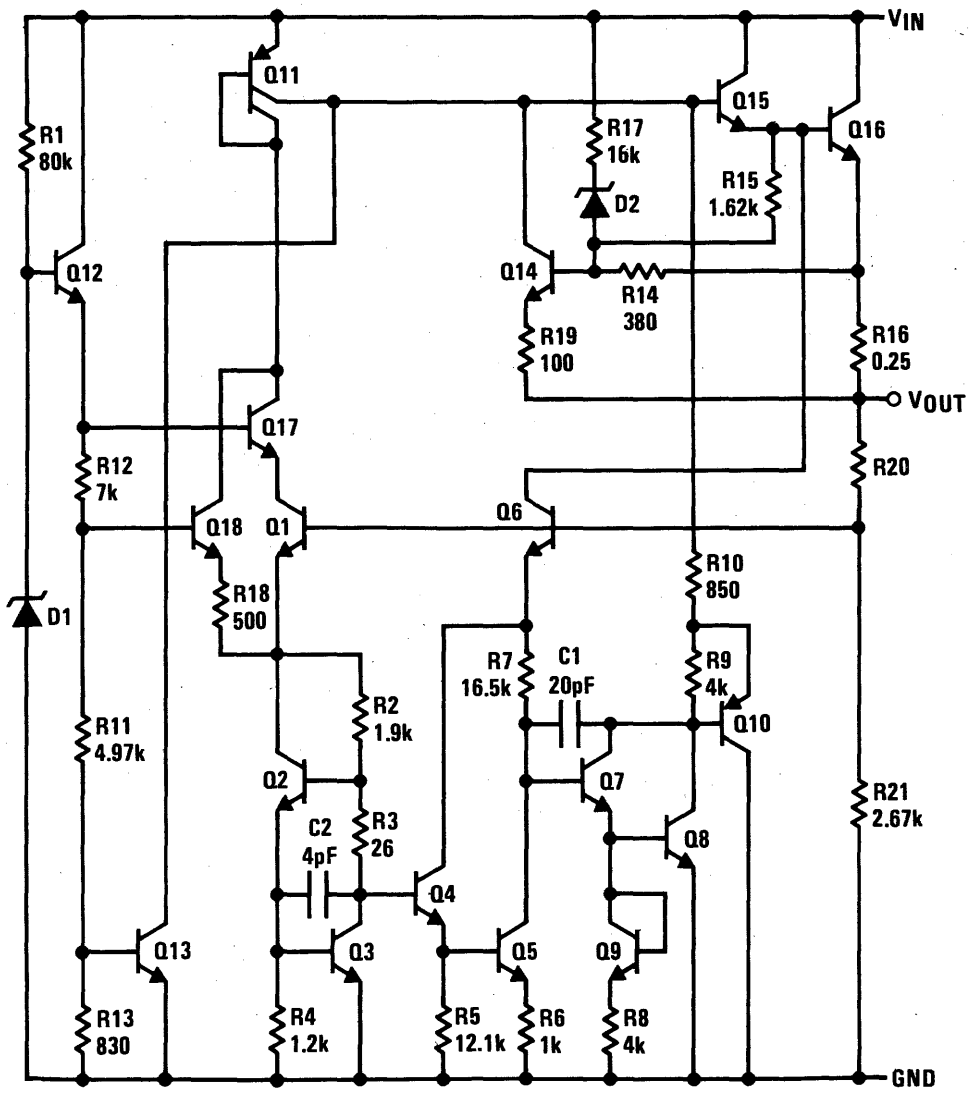
Load Regulation
140AK-5.0, V_{IN} = 10V, T_A = 25°C



Line Regulation
140AK-5.0, I_{OUT} = 1A, T_A = 25°C



Equivalent Schematic



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Application Hints

The LM340 is designed with thermal protection, output short-circuit protection and output transistor safe area protection. However, as with *any* IC regulator, it becomes necessary to take precautions to assure that the regulator is not inadvertently damaged. The following describes possible misapplications and methods to prevent damage to the regulator.

Shorting the Regulator Input: When using large capacitors at the output of these regulators that have V_{OUT} greater than 6V, a protection diode connected input to output *(Figure 1)* may be required if the input is shorted to ground. Without the protection diode, an input short will cause the input to rapidly approach ground potential, while the output remains near the initial V_{OUT} because of the stored charge in the large output capacitor. The capacitor will then discharge through reverse biased emitter-base junction of the pass device, Q16, which breaks down at 6.5V and forward biases the base-collector junction. If the energy released by the capacitor into the emitter-base junction is large enough, the junction and the regulator will be destroyed. The fast diode in *Figure 1* will shunt the capacitor's discharge current around the regulator.

Raising the Output Voltage above the Input Voltage: Since the output of the LM340 does not sink current, forcing the output high can cause damage to internal low current paths in a manner similar to that just described in the "Shorting the Regulator Input" section.

Regulator Floating Ground *(Figure 2)*: When the ground pin alone becomes disconnected, the output approaches the unregulated input, causing possible damage to other circuits connected to V_{OUT}. If ground is reconnected with power "ON", damage may also occur to the regulator. This fault is most likely to occur when plugging in regulators or modules with on card regulators into powered up sockets. Power should be turned off first, or ground should be connected first if power must be left on.

Transient Voltages: If transients exceed the maximum rated input voltage of the 340, or reach more than 0.8V below ground and have sufficient energy, they will damage the regulator. The solution is to use a large input capacitor, a series input breakdown diode, a choke, a transient suppressor or a combination of these.

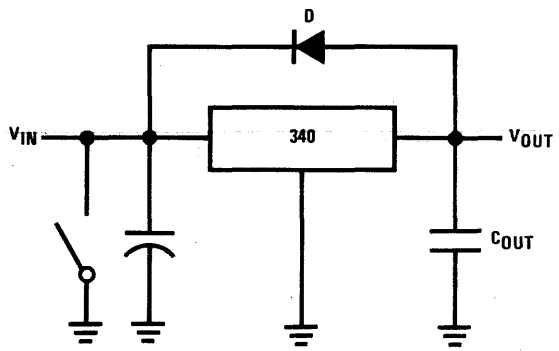


FIGURE 1. Input Short

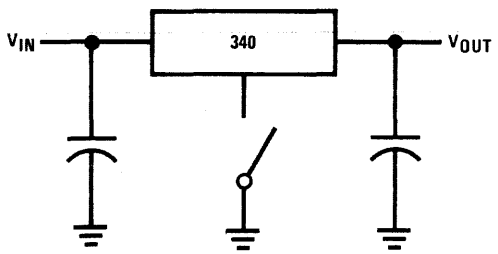


FIGURE 2. Regulator Floating Ground

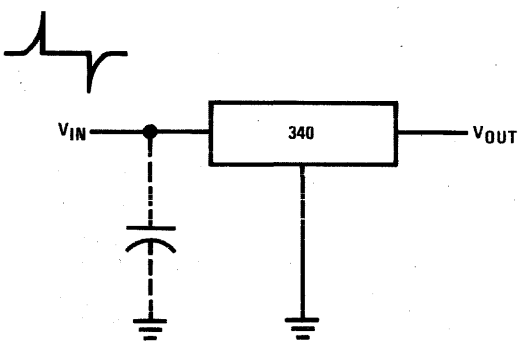
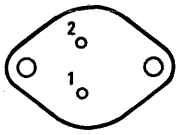


FIGURE 3. Transients

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Connection Diagrams

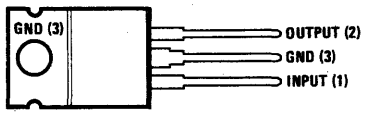
Metal Can Package



BOTTOM VIEW

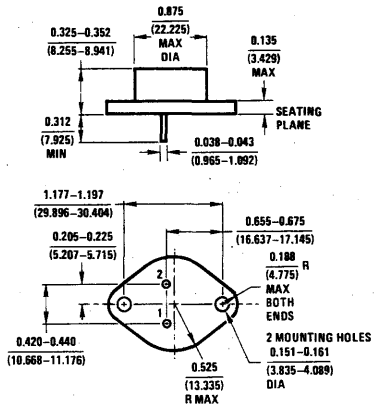
Pin 1 — input
Pin 2 — output
Case — ground

Power Package



TOP VIEW

Physical Dimensions inches (millimeters)



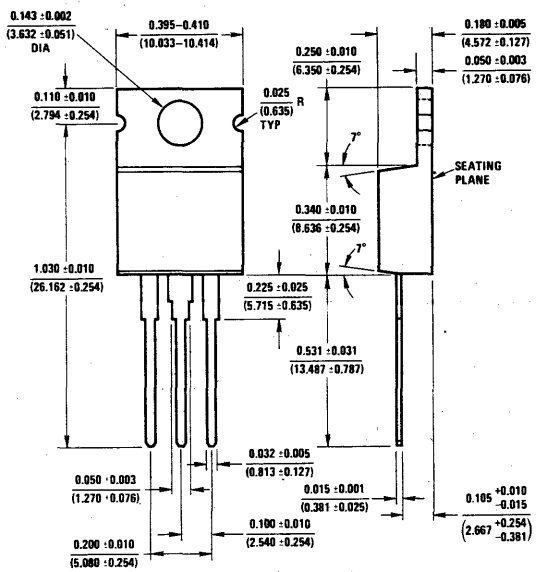
TO-3 Metal Can Power Package (K) and (KC)

Steel Package Order Numbers:

LM140AK-5.0	LM140K-5.0	LM340AK-5.0	LM340K-5.0
LM140AK-6.0	LM140K-6.0	LM340AK-6.0	LM340K-6.0
LM140AK-8.0	LM140K-8.0	LM340AK-8.0	LM340K-8.0
LM140AK-10	LM140K-10	LM340AK-10	LM340K-10
LM140AK-12	LM140K-12	LM340AK-12	LM340K-12
LM140AK-15	LM140K-15	LM340AK-15	LM340K-15
LM140AK-18	LM140K-18	LM340AK-18	LM340K-18
LM140AK-24	LM140K-24	LM340AK-24	LM340K-24

Aluminum Package Order Numbers:

LM340AKC-5.0	LM340KC-5.0
LM340AKC-6.0	LM340KC-6.0
LM340AKC-8.0	LM340KC-8.0
LM340AKC-10	LM340KC-10
LM340AKC-12	LM340KC-12
LM340AKC-15	LM340KC-15
LM340AKC-18	LM340KC-18
LM340AKC-24	LM340KC-24



TO-220 Plastic Power Package (T)

Plastic Package Order Numbers:

LM340AT-5.0	LM340T-5.0
LM340AT-6.0	LM340T-6.0
LM340AT-8.0	LM340T-8.0
LM340AT-10	LM340T-10
LM340AT-12	LM340T-12
LM340AT-15	LM340T-15
LM340AT-18	LM340T-18
LM340AT-24	LM340T-24

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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LM150/LM250/LM350
3 Amp Adjustable Power Regulators

General Description

The LM150/LM250/LM350 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 3A over a 1.2V to 33V output range. They are exceptionally easy to use and require only 2 external resistors to set the output voltage. Further, both line and load regulation are comparable to discrete designs. Also, the LM150 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM150 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is accidentally disconnected.

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejections ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators or discrete designs, the LM150 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM150 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

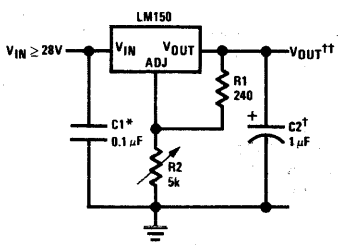
The LM150/LM250/LM350 are packaged in standard steel TO-3 transistor packages. The LM150 is rated for operation from −55°C to +150°C, the LM250 from −25°C to +150°C and the LM350 from 0°C to +125°C.

Features

- Adjustable output down to 1.2V
- Guaranteed 3A output current
- Line regulation typically 0.005%/V
- Load regulation typically 0.1%
- Guaranteed thermal regulation
- Current limit constant with temperature
- **100% electrical burn-in in thermal limit**
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 86 dB ripple rejection

Typical Applications

1.2V–25V Adjustable Regulator

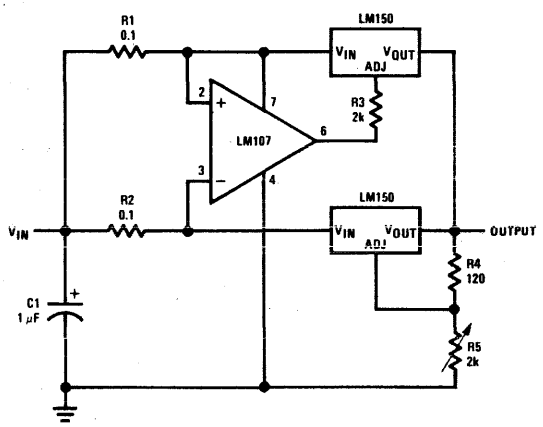


†Optional—improves transient response

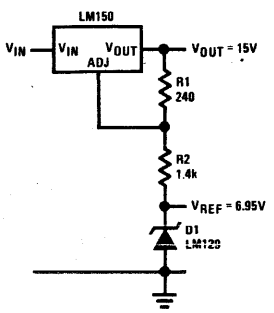
*Needed if device is far from filter capacitors

††$V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right)$

6A Regulator



Regulator and Voltage Reference



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IM-B20M107/Printed in U.S.A.

Absolute Maximum Ratings

Power Dissipation	Internally limited
Input–Output Voltage Differential	35V
LM150	−55°C to +150°C
LM250	−25°C to +150°C
LM350	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Preconditioning

Burn-In in Thermal Limit	**All Devices 100%**

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM150/LM250			LM350			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	$T_A = 25°C$, $3V \leq V_{IN} - V_{OUT} \leq 35V$, (Note 2)		0.005	0.01		0.005	0.03	%/V
Load Regulation	$T_A = 25°C$, $10\ mA \leq I_{OUT} \leq 3A$							
	$V_{OUT} \leq 5V$, (Note 2)		5	15		5	25	mV
	$V_{OUT} \geq 5V$, (Note 2)		0.1	0.3		0.1	0.5	%
Thermal Regulation	Pulse = 20 ms		0.002	0.01		0.002	0.03	%/W
Adjustment Pin Current			50	100		50	100	μA
Adjustment Pin Current Change	$10\ mA \leq I_L \leq 3A$		0.2	5		0.2	5	μA
	$3V \leq (V_{IN} - V_{OUT}) \leq 35V$							
Reference Voltage	$3 \leq (V_{IN} - V_{OUT}) \leq 35V$, (Note 3)	1.20	1.25	1.30	1.20	1.25	1.30	V
	$10\ mA \leq I_{OUT} \leq 3A$, $P \leq 30W$							
Line Regulation	$3V \leq V_{IN} - V_{OUT} \leq 35V$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	$10\ mA \leq I_{OUT} \leq 3A$, (Note 2)							
	$V_{OUT} \leq 5V$		20	50		20	70	mV
	$V_{OUT} \geq 5V$		0.3	1		0.3	1.5	%
Temperature Stability	$T_{MIN} \leq T_j \leq T_{MAX}$		1			1		%
Minimum Load Current	$V_{IN} - V_{OUT} = 35V$		3.5	5		3.5	10	mA
Current Limit	$V_{IN} - V_{OUT} \leq 10V$	3.0	4.5		3.0	4.5		A
	$V_{IN} - V_{OUT} = 30V$		1			1		A
RMS Output Noise, % of V_{OUT}	$T_A = 25°C$, $10\ Hz \leq f \leq 10\ kHz$		0.003			0.003		%
Ripple Rejection Ratio	$V_{OUT} = 10V$, f = 120 Hz		65			65		dB
	$C_{ADJ} = 10\ \mu F$	66	86		66	86		dB
Long Term Stability	$T_A = 125°C$		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	K Package		2	2.5		2	2.5	°C/W

Note 1: Unless otherwise specified, these specifications apply $-55°C \leq T_j \leq +150°C$ for the LM150, $-25°C \leq T_j \leq +150°C$ for the LM250 and $0°C \leq T_j \leq +125°C$ for the LM350, $V_{IN} - V_{OUT} = 5V$ and $I_{OUT} = 1.5A$. Although power dissipation is internally limited, these specifications are applicable for power dissipations up to 30W.

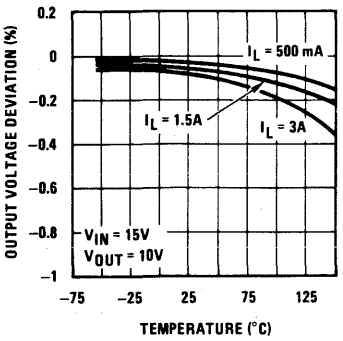
Note 2: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Note 3: Selected devices with tightened tolerance reference voltage available.

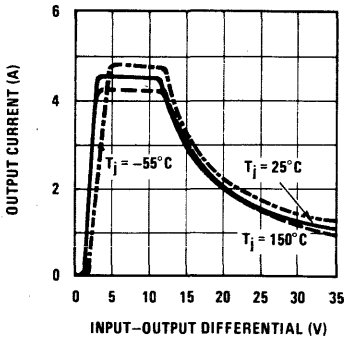
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Typical Performance Characteristics

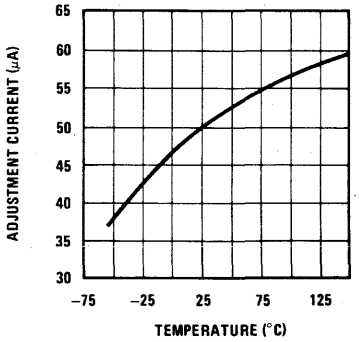
Load Regulation



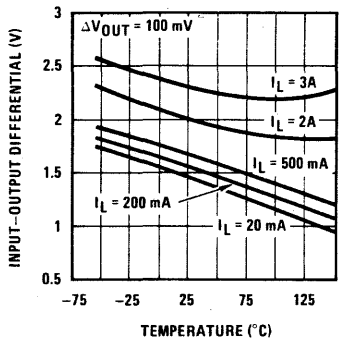
Current Limit



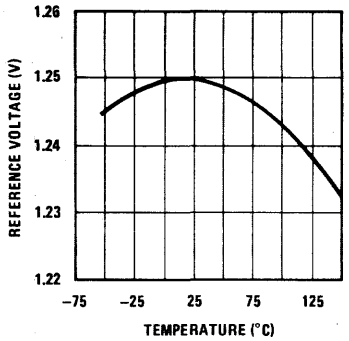
Adjustment Current



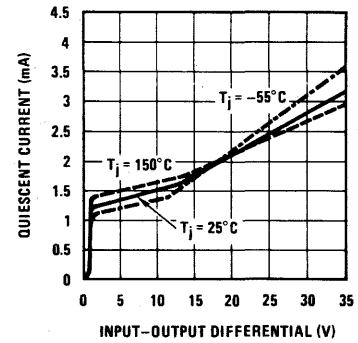
Dropout Voltage



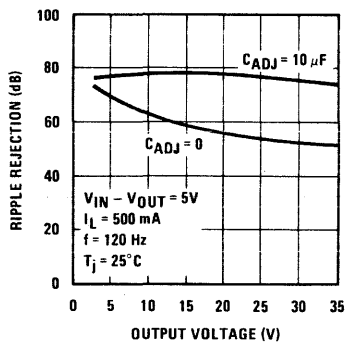
Temperature Stability



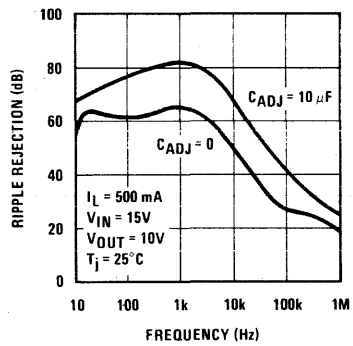
Minimum Operating Current



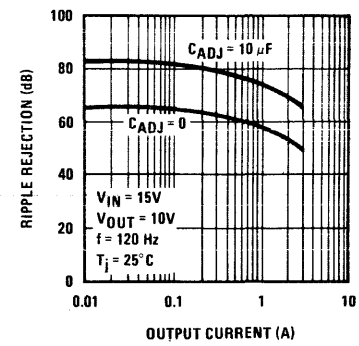
Ripple Rejection



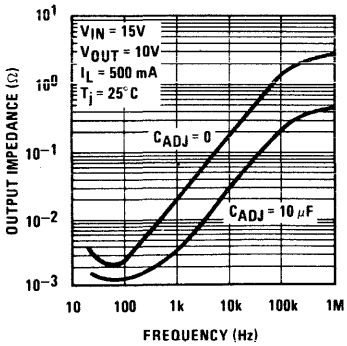
Ripple Rejection



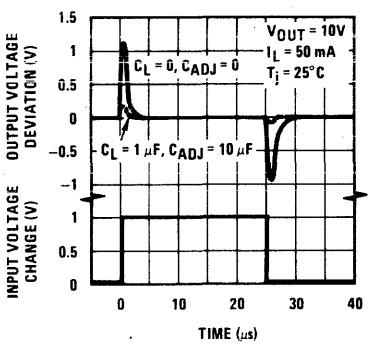
Ripple Rejection



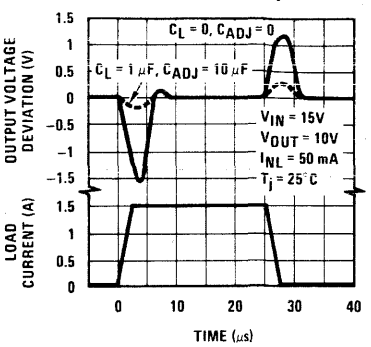
Output Impedance



Line Transient Response



Load Transient Response



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Application Hints

In operation, the LM150 develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2.$$

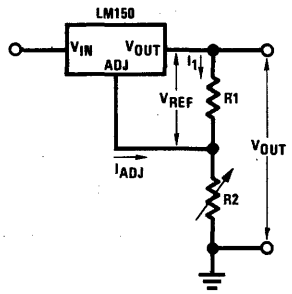


FIGURE 1

Since the 50 μA current from the adjustment terminal represents an error term, the LM150 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A 0.1 μF disc or 1 μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM150 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 μF bypass capacitor 86 dB ripple rejection is obtainable at any output level. Increases over 10 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1 μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies, but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01 μF disc may seem to work better than a 0.1 μF disc as a bypass.

Although the LM150 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability.

Load Regulation

The LM150 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω x I_L. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.

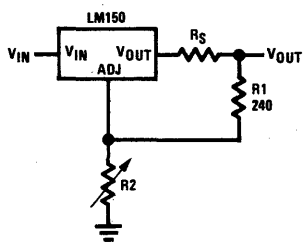


FIGURE 2. Regulator with Line Resistance in Output Lead

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using 2 separate leads to the case. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

Protection Diodes

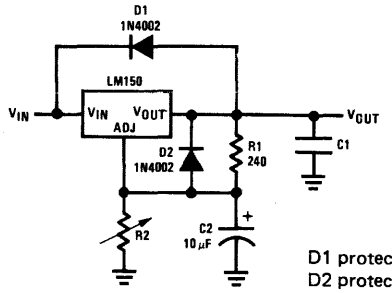
When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM150, this discharge path is through a large junction that is able to sustain 25A surge with no problem. This is not true of other types of positive

Application Hints (Continued)

regulators. For output capacitors of 25 μF or less, there is no need to use diodes.

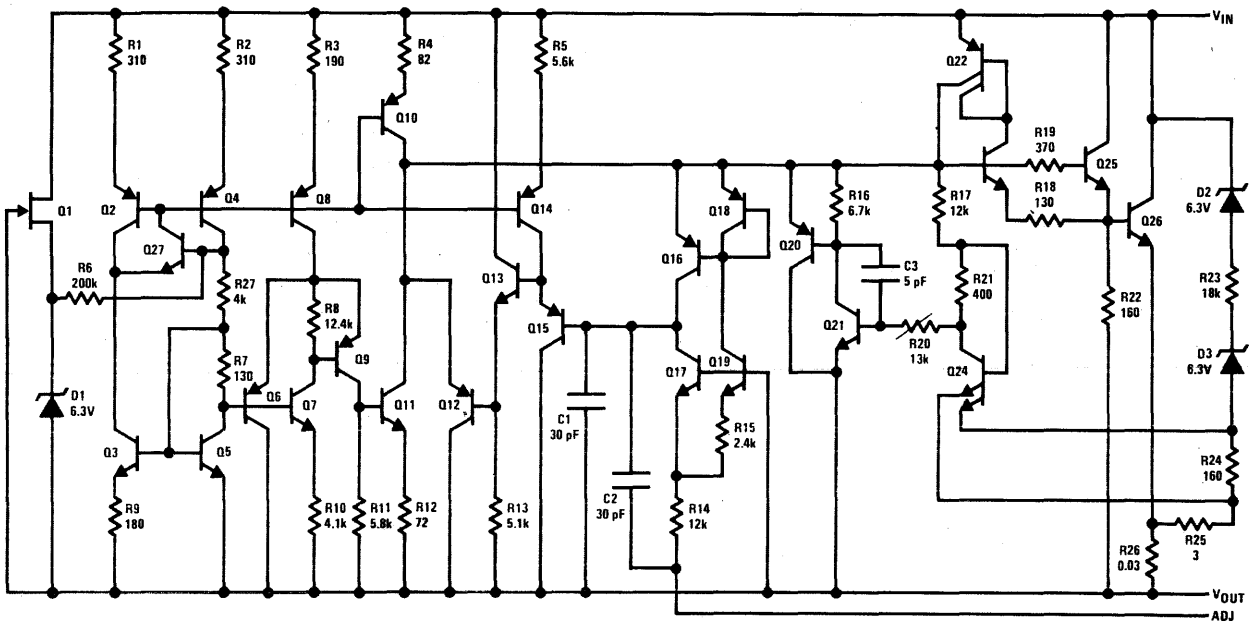
The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM150 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10 μF capacitance. *Figure 3* shows an LM150 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.



$$V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right) + R2I_{ADJ}$$

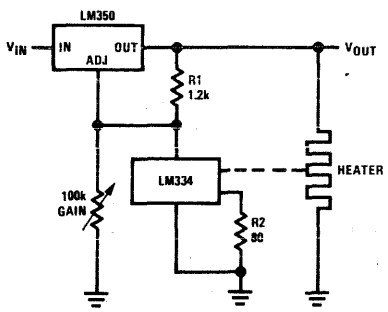
FIGURE 3. Regulator with Protection Diodes

Schematic Diagram

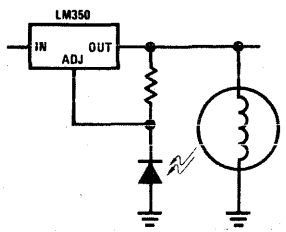


Typical Applications (Continued)

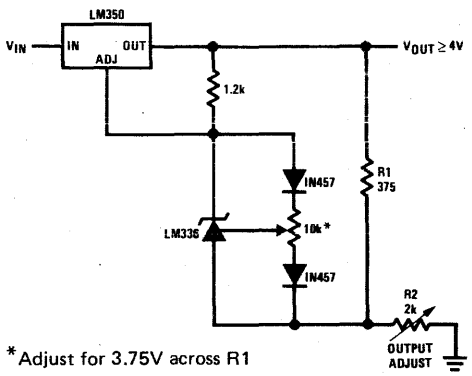
Temperature Controller



Light Controller



Precision Power Regulator with Low Temperature Coefficient

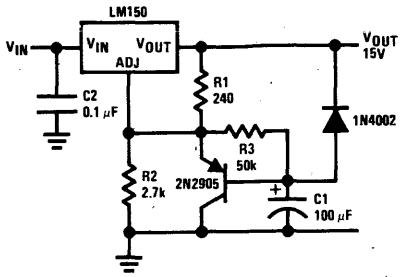


*Adjust for 3.75V across R1

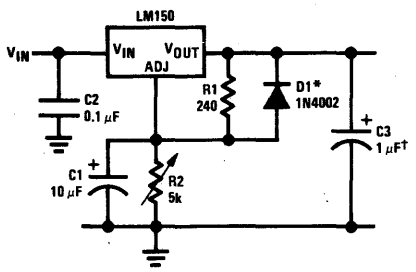
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Typical Applications (Continued)

Slow Turn-ON 15V Regulator



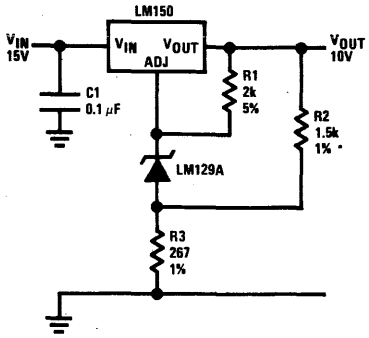
Adjustable Regulator with Improved Ripple Rejection



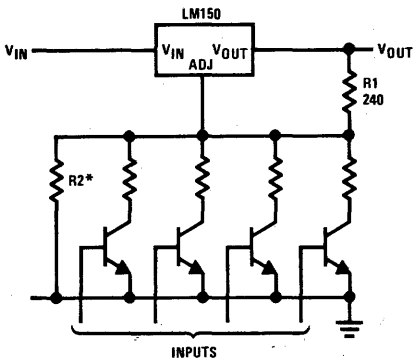
†Solid tantalum

*Discharges C1 if output is shorted to ground

High Stability 10V Regulator

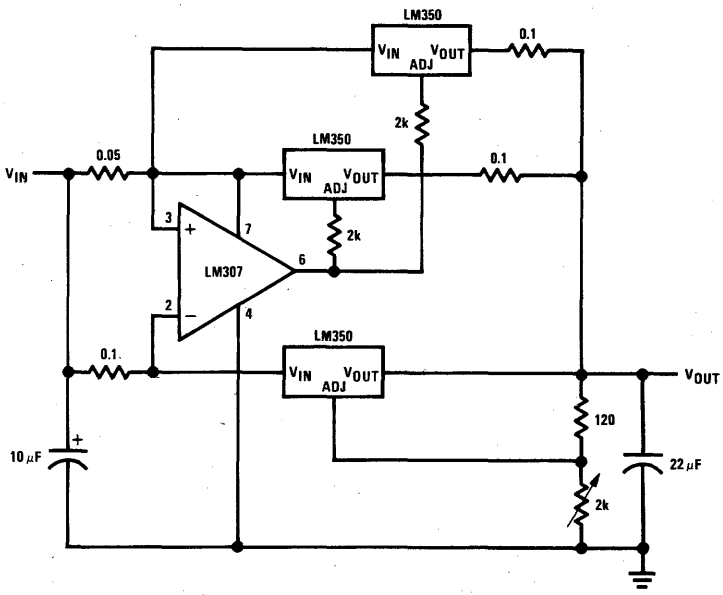


Digitally Selected Outputs

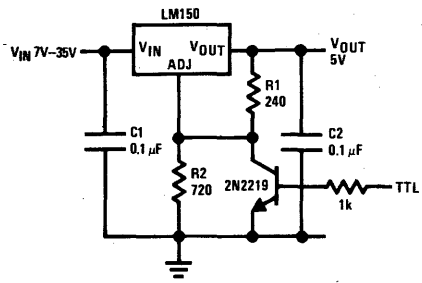


*Sets maximum V_{OUT}

10A Regulator

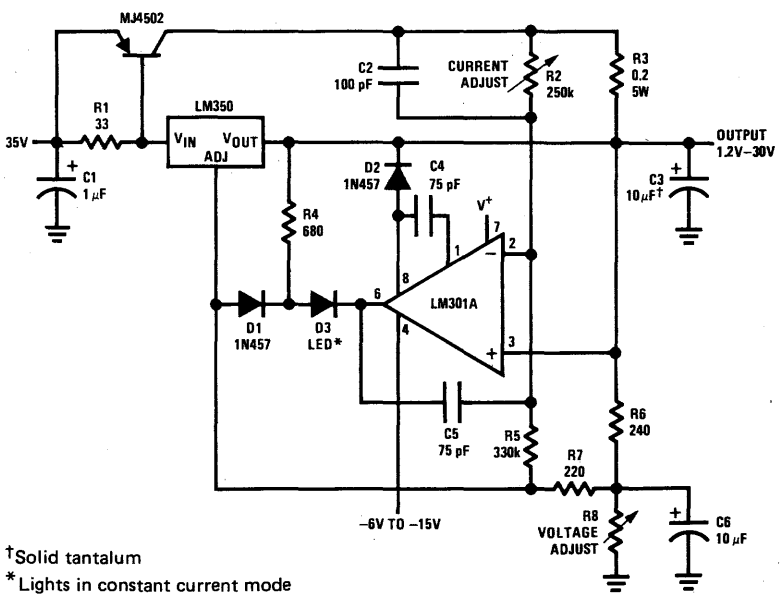


5V Logic Regulator with Electronic Shutdown*



*Min output ≈ 1.2V

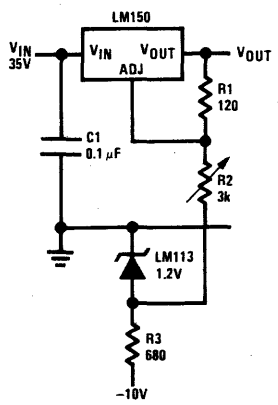
5A Constant Voltage/Constant Current Regulator



†Solid tantalum

*Lights in constant current mode

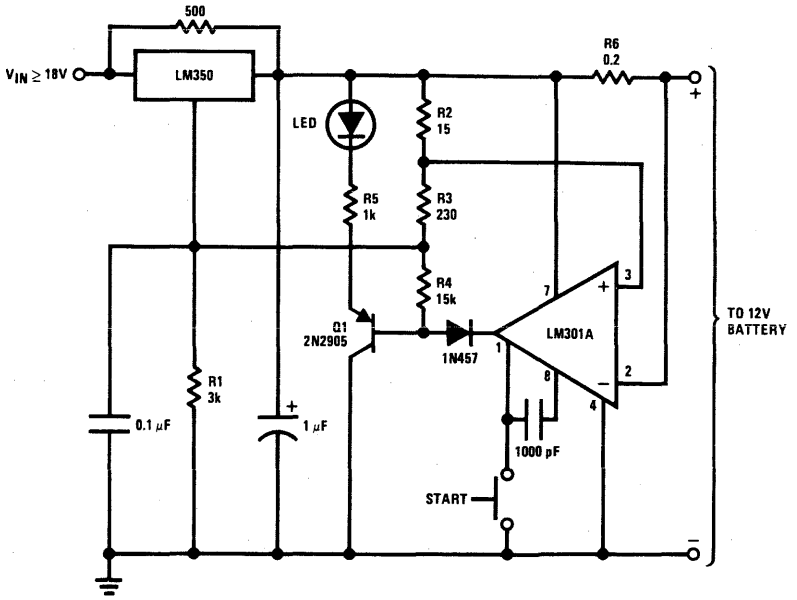
0 to 30V Regulator



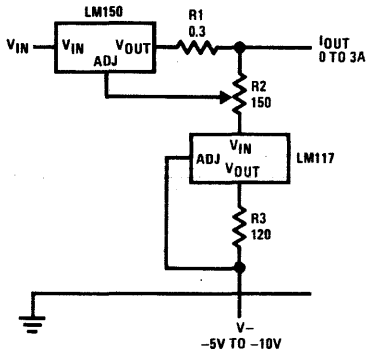
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Typical Applications (Continued)

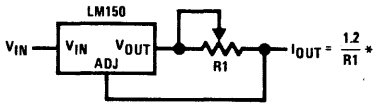
12V Battery Charger



Adjustable Current Regulator

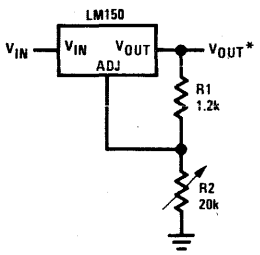


Precision Current Limiter



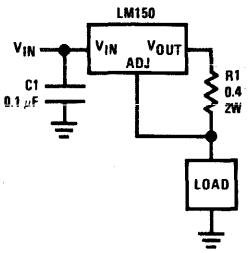
*0.4 ≤ R1 ≤ 120Ω

1.2V – 20V Regulator with Minimum Program Current

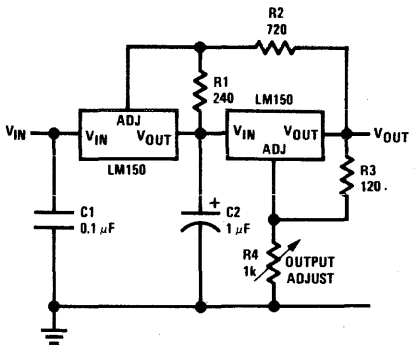


*Minimum load current ≈ 4 mA

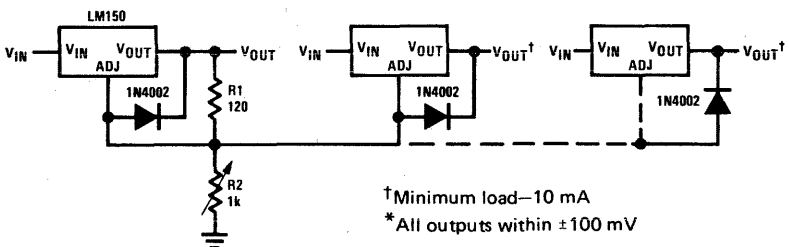
3A Current Regulator



Tracking Preregulator



Adjusting Multiple On-Card Regulators with Single Control*

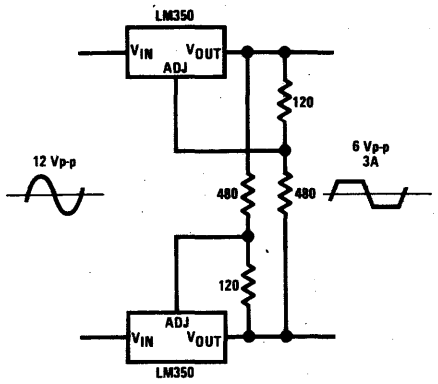


†Minimum load—10 mA
*All outputs within ±100 mV

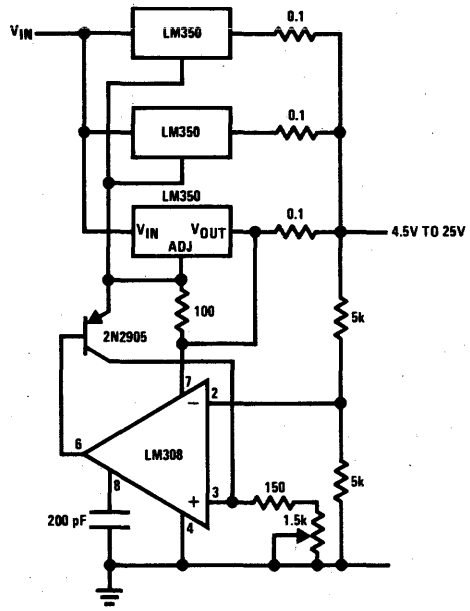
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Typical Applications (Continued)

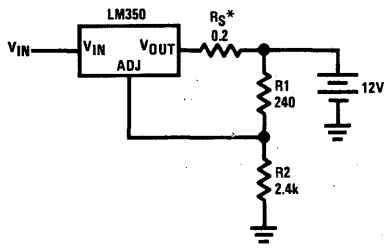
AC Voltage Regulator



Adjustable 10A Regulator

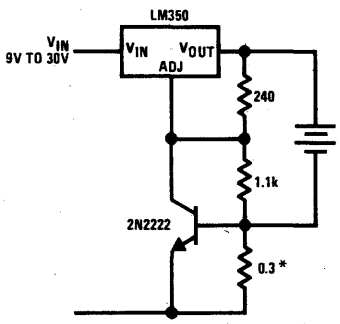


Simple 12V Battery Charger



*R_S—sets output impedance of charger $Z_{OUT} = R_S\left(1 + \frac{R2}{R1}\right)$
Use of R_S allows low charging rates with fully charged battery.

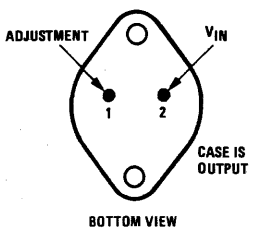
Current Limited 6V Charger



*Sets peak current (2A for 0.3Ω)

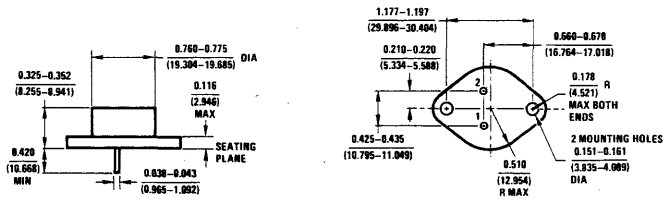
Connection Diagram

Metal Can Package



BOTTOM VIEW

Physical Dimensions inches (millimeters)



Steel TO-3 Metal Can Package (K Steel)
Order Number LM150K Steel,
LM250K Steel or LM350K Steel
NS Package Number K02A

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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LM137/LM237/LM337 3-Terminal Adjustable Negative Regulators

General Description

The LM137/LM237/LM337 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −1.5A over an output voltage range of −1.2V to −37V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM137 series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

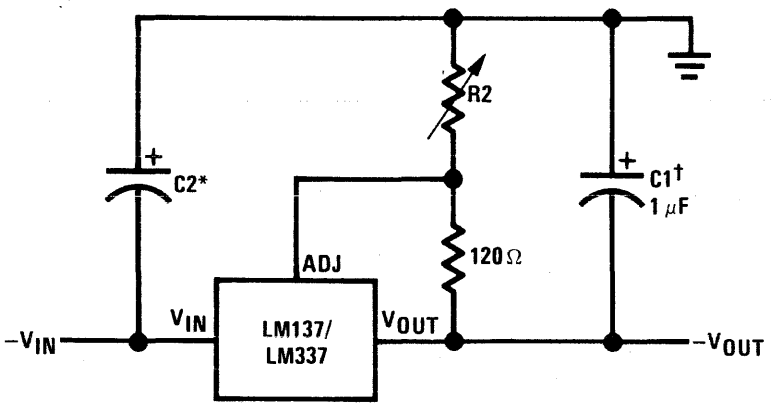
The LM137/LM237/LM337 serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM137/LM237/LM337 are ideal complements to the LM117/LM217/LM317 adjustable positive regulators.

Features

- Output voltage adjustable from −1.2V to −37V
- 1.5A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 77 dB ripple rejection
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- 100% electrical burn-in
- Standard 3-lead transistor package

Typical Applications

Adjustable Negative Voltage Regulator



$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{120\Omega}\right)$$

†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability
*C2 = 1 μF solid tantalum is required only if regulator is more than 4" from power-supply filter capacitor

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IM-B20M107/Printed in U.S.A.

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Absolute Maximum Ratings

Power Dissipation	Internally limited
Input–Output Voltage Differential	40V
Operating Junction Temperature Range	
LM137	−55°C to +150°C
LM237	−25°C to +150°C
LM337	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Preconditioning

Burn-In in Thermal Limit **100% All Devices**

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	LM137/LM237			LM337			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	$T_A = 25°C$, $3V \le \lvert V_{IN}-V_{OUT}\rvert \le 40V$ (Note 2)		0.01	0.02		0.01	0.04	%/V
Load Regulation	$T_A = 25°C$, $10\ mA \le I_{OUT} \le I_{MAX}$							
	$\lvert V_{OUT}\rvert \le 5V$, (Note 2)		15	25		15	50	mV
	$\lvert V_{OUT}\rvert \ge 5V$, (Note 2)		0.3	0.5		0.3	1.0	%
Thermal Regulation	$T_A = 25°C$, 10 ms Pulse		0.002	0.02		0.003	0.04	%/W
Adjustment Pin Current			65	100		65	100	μA
Adjustment Pin Current Change	$10\ mA \le I_L \le I_{MAX}$		2	5		2	5	μA
	$2.5V \le \lvert V_{IN}-V_{OUT}\rvert \le 40V$, $T_A = 25°C$							
Reference Voltage	$T_A = 25°C$ (Note 3)	−1.225	−1.250	−1.275	−1.213	−1.250	−1.287	V
	$3 \le \lvert V_{IN}-V_{OUT}\rvert \le 40V$, (Note 3)	−1.200	−1.250	−1.300	−1.200	−1.250	−1.300	V
	$10\ mA \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$							
Line Regulation	$3V \le \lvert V_{IN}-V_{OUT}\rvert \le 40V$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	$10\ mA \le I_{OUT} \le I_{MAX}$, (Note 2)							
	$\lvert V_{OUT}\rvert \le 5V$		20	50		20	70	mV
	$\lvert V_{OUT}\rvert \ge 5V$		0.3	1		0.3	1.5	%
Temperature Stability	$T_{MIN} \le T_j \le T_{MAX}$		0.6			0.6		%
Minimum Load Current	$\lvert V_{IN}-V_{OUT}\rvert \le 40V$		2.5	5		2.5	10	mA
	$\lvert V_{IN}-V_{OUT}\rvert \le 10V$		1.2	3		1.5	6	mA
Current Limit	$\lvert V_{IN}-V_{OUT}\rvert \le 15V$							
	K and T Package	1.5	2.2		1.5	2.2		A
	H and P Package	0.5	0.8		0.5	0.8		A
	$\lvert V_{IN}-V_{OUT}\rvert = 40V$							
	K and T Package		0.4			0.4		A
	H and P Package		0.17			0.17		A
RMS Output Noise, % of V_{OUT}	$T_A = 25°C$, $10\ Hz \le f \le 10\ kHz$		0.003			0.003		%
Ripple Rejection Ratio	$V_{OUT} = -10V$, f = 120 Hz		60			60		dB
	$C_{ADJ} = 10\ \mu F$	66	77		66	77		dB
Long-Term Stability	$T_A = 125°C$, 1000 Hours		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	H Package		12	15		12	15	°C/W
	K Package		2.3	3		2.3	3	°C/W
	T Package					5		°C/W
	P Package					12		°C/W

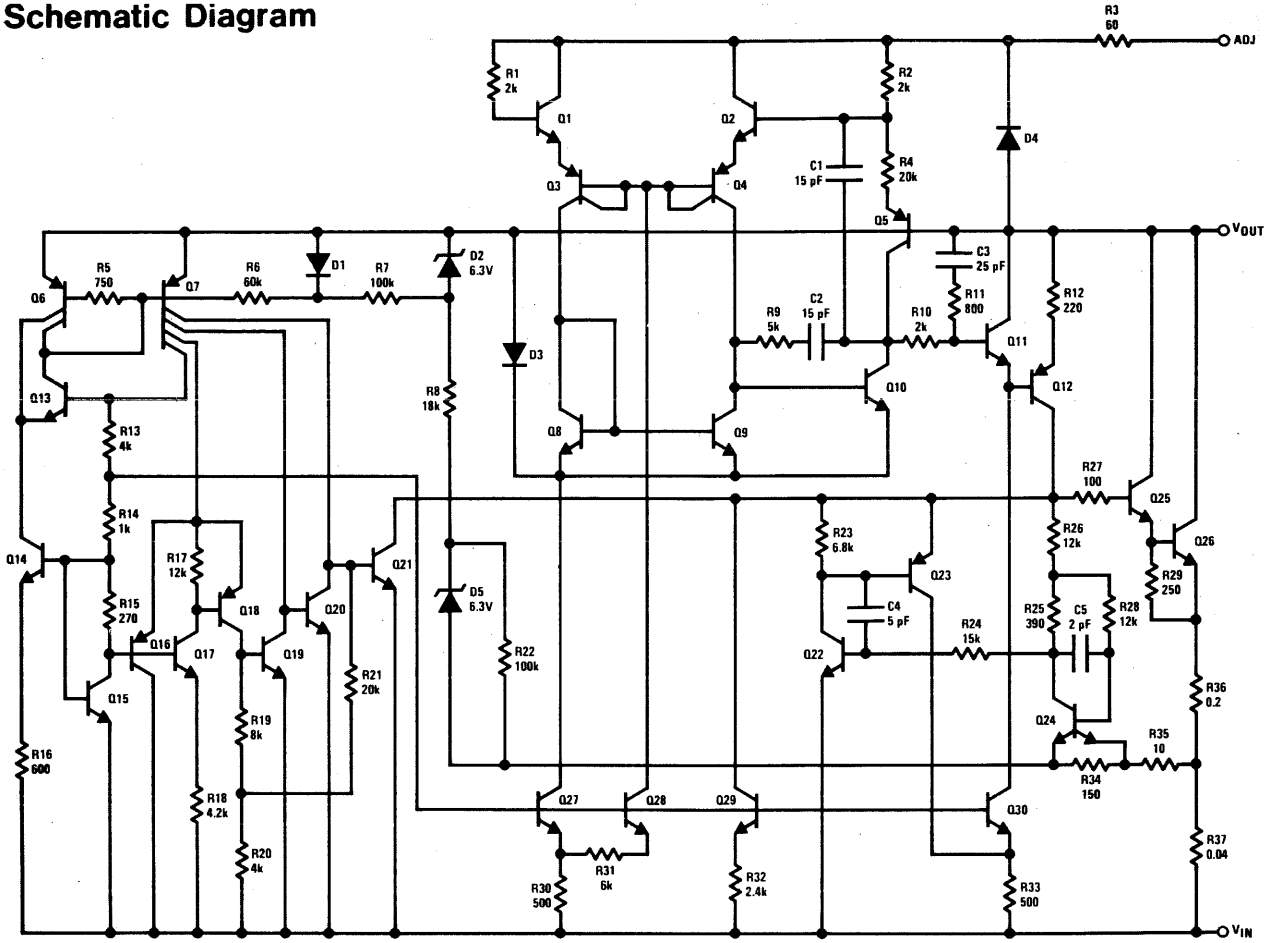
Note 1: Unless otherwise specified, these specifications apply $-55°C \le T_j \le +150°C$ for the LM137, $-25°C \le T_j \le +150°C$ for the LM237 and $0°C \le T_j \le +125°C$ for the LM337; $V_{IN} - V_{OUT} = 5V$; and $I_{OUT} = 0.1A$ for the TO-5 package and TO-202 package and $I_{OUT} = 0.5A$ for the TO-3 package and TO-220 package. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-5 and TO-202 and 20W for the TO-3 and TO-220. I_{MAX} is 1.5A for the TO-3 and TO-220 package and 0.5A for the TO-5 package and TO-202 package.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation. Load regulation is measured on the output pin at a point 1/8" below the base of the TO-3 and TO-5 packages.

Note 3: Selected devices with tightened tolerance reference voltage available.

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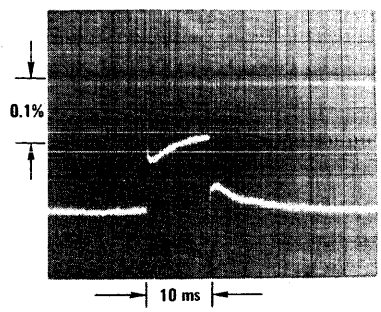
Schematic Diagram



Thermal Regulation

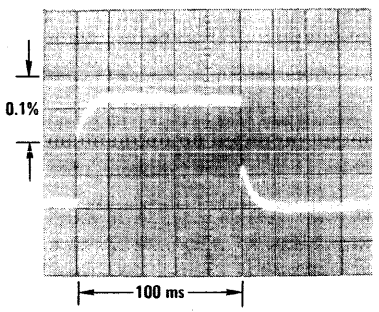
When power is dissipated in an IC, a temperature gradient occurs across the IC chip affecting the individual IC circuit components. With an IC regulator, this gradient can be especially severe since power dissipation is large. Thermal regulation is the effect of these temperature gradients on output voltage (in percentage output change) per Watt of power change in a specified time. Thermal regulation error is independent of electrical regulation or temperature coefficient, and occurs within 5 ms to 50 ms after a change in power dissipation. Thermal regulation depends on IC layout as well as electrical design. The thermal regulation of a voltage regulator is defined as the percentage change of V_{OUT}, per Watt, within the first 10 ms after a step of power is applied. The LM137's specification is 0.02%/W, max.

In *Figure 1*, a typical LM137's output drifts only 3 mV (or 0.03% of V_{OUT} = −10V) when a 10W pulse is applied for 10 ms. This performance is thus well inside the specification limit of 0.02%/W x 10W = 0.2% max. When the 10W pulse is ended, the thermal regulation again shows a 3 mV step as the LM137 chip cools off. Note that the load regulation error of about 8 mV (0.08%) is additional to the thermal regulation error. In *Figure 2*, when the 10W pulse is applied for 100 ms, the output drifts only slightly beyond the drift in the first 10 ms, and the thermal error stays well within 0.1% (10 mV).



LM137, V_{OUT} = −10V
$V_{IN}-V_{OUT}$ = −40V
I_L = 0A → 0.25A → 0A
Vertical sensitivity, 5 mV/div

FIGURE 1



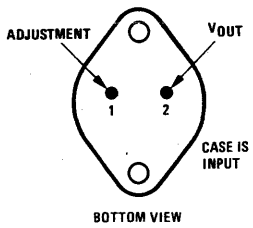
LM137, V_{OUT} = −10V
$V_{IN}-V_{OUT}$ = −40V
I_L = 0A → 0.25A → 0A
Horizontal sensitivity, 20 ms/div

FIGURE 2

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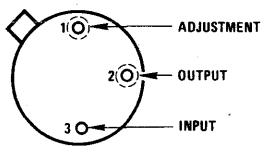
Connection Diagrams

TO-3
Metal Can Package



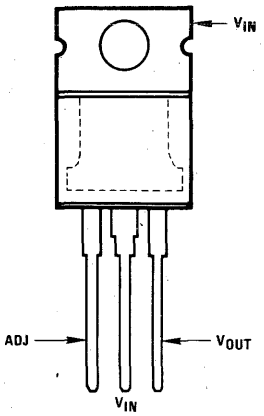
BOTTOM VIEW

TO-5
Metal Can Package



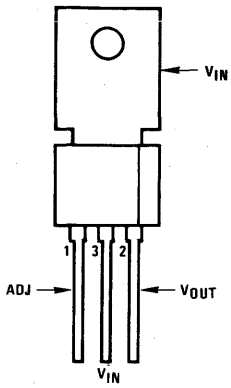
CASE IS INPUT
BOTTOM VIEW

TO-220
Plastic Package



FRONT VIEW

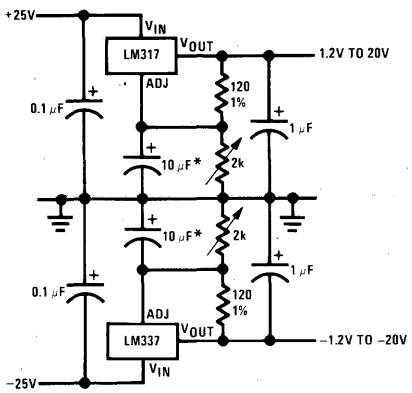
TO-202
Plastic Package



FRONT VIEW

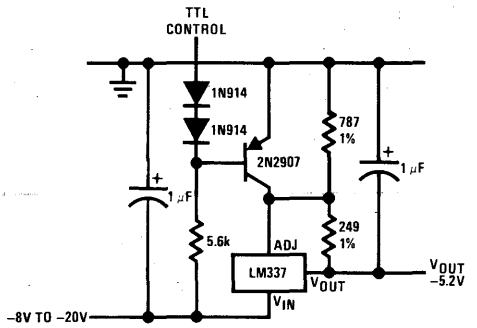
Typical Applications (Continued)

Adjustable Lab Voltage Regulator



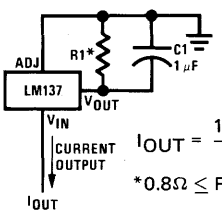
*The 10 μF capacitors are optional to improve ripple rejection

−5.2V Regulator with Electronic Shutdown*



*Minimum output ≅ −1.3V when control input is low

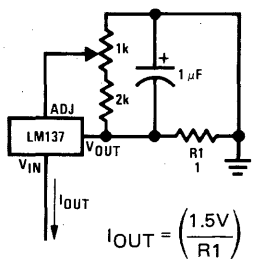
Current Regulator



$$I_{OUT} = \frac{1.250V}{R1}$$

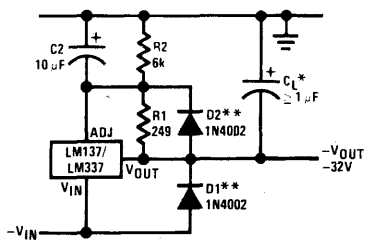
*0.8Ω ≤ R1 ≤ 120Ω

Adjustable Current Regulator



$$I_{OUT} = \left(\frac{1.5V}{R1}\right)$$ ±15% adjustable

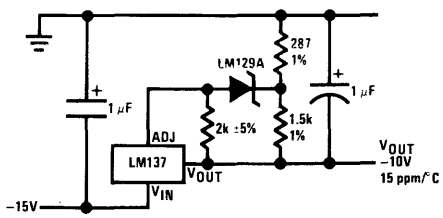
Negative Regulator with Protection Diodes



*When C_L is larger than 20 μF, D1 protects the LM137 in case the input supply is shorted

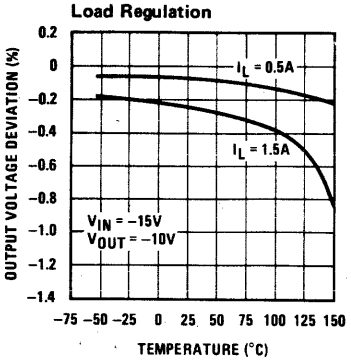
**When C2 is larger than 10 μF and $-V_{OUT}$ is larger than −25V, D2 protects the LM137 in case the output is shorted

High Stability −10V Regulator

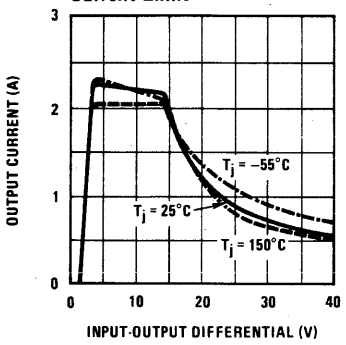


Typical Performance Characteristics (K Steel, KC and T Packages)

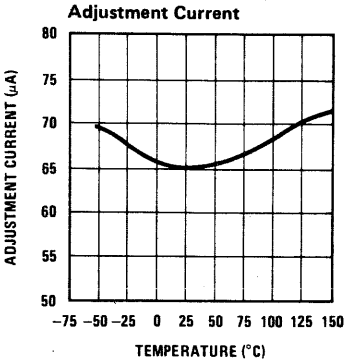
Load Regulation



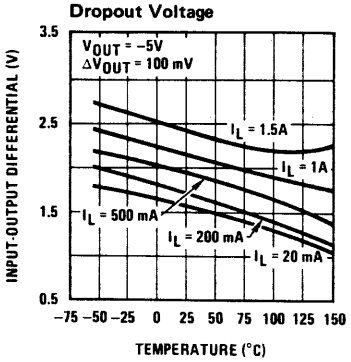
Current Limit



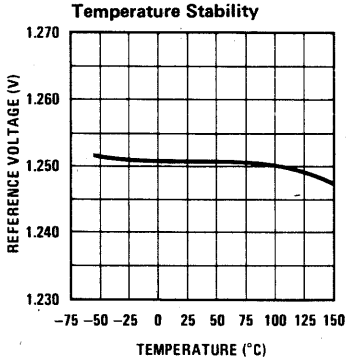
Adjustment Current



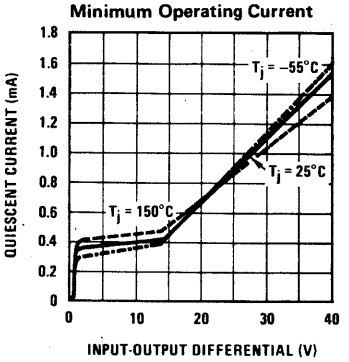
Dropout Voltage



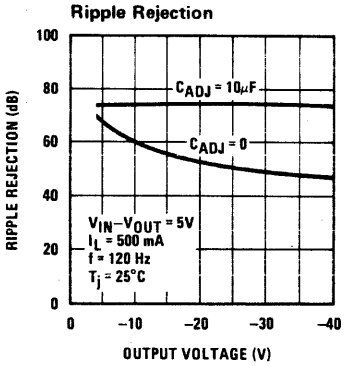
Temperature Stability



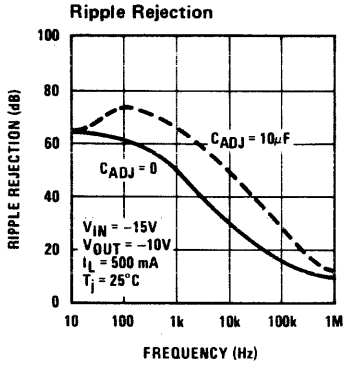
Minimum Operating Current



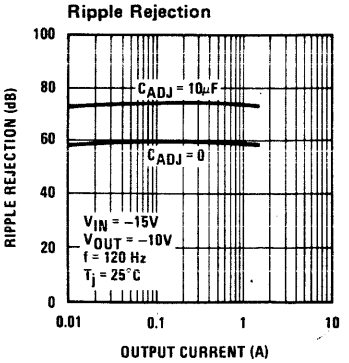
Ripple Rejection



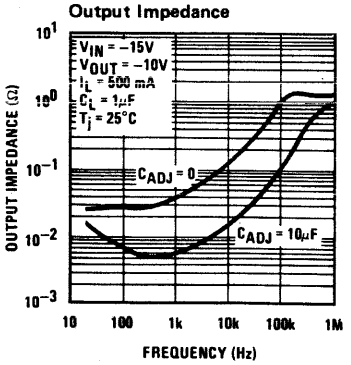
Ripple Rejection



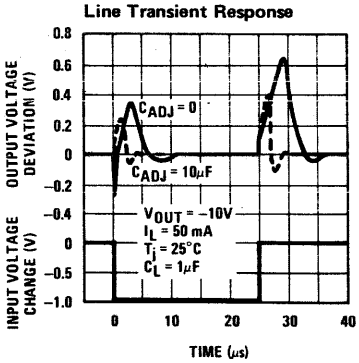
Ripple Rejection



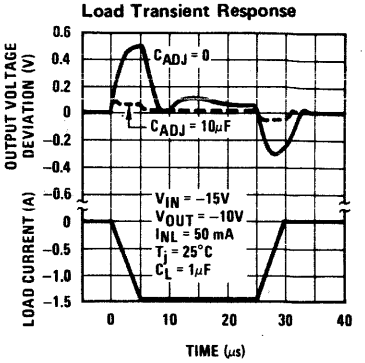
Output Impedance



Line Transient Response

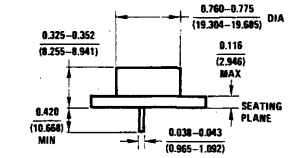


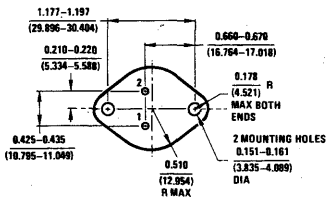
Load Transient Response



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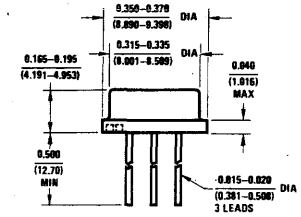
Physical Dimensions inches (millimeters)

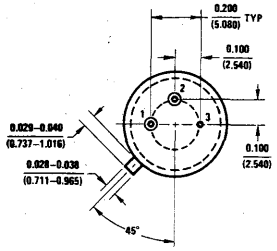




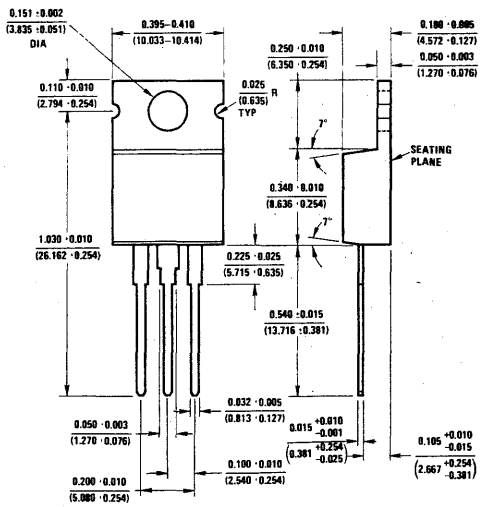
Steel TO-3 Metal Can Package (K)
Order Number LM137K Steel, LM237K Steel or LM337K Steel
NS Package Number K02A

AL TO-3 Metal Can Package (KC)
Order Number LM337KC

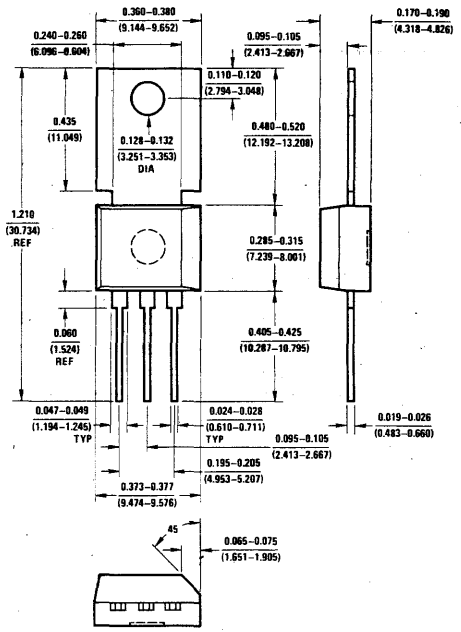




TO-5 Metal Can Package (H)
Order Number LM137H, LM237H or LM337H
NS Package Number H03A



TO-220 Plastic Package (T)
Order Number LM337T
NS Package Number TO3B



TO-202 Plastic Package (P)
Order Number LM337MP
NS Package Number P03A

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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LM117/LM217/LM317 3-terminal adjustable regulator

general description

The LM117/LM217/LM317 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5A over a 1.2V to 37V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM117 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM117 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

features

- Adjustable output down to 1.2V
- Guaranteed 1.5A output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- 100% electrical burn-in
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejections ratios which are difficult to achieve with standard 3-terminal regulators.

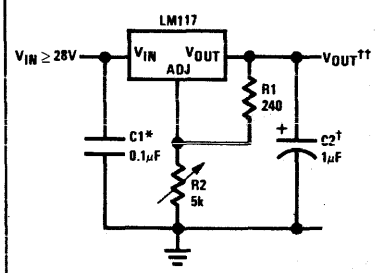
Besides replacing fixed regulators, the LM117 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

The LM117K, LM217K and LM317K are packaged in standard TO-3 transistor packages while the LM117H, LM217H and LM317H are packaged in a solid Kovar base TO-5 transistor package. The LM117 is rated for operation from −55°C to +150°C, the LM217 from −25°C to +150°C and the LM317 from 0°C to +125°C. The LM317T, rated for operation over a 0°C to +125°C range is available in a TO-220 plastic package.

typical applications

1.2V–25V Adjustable Regulator

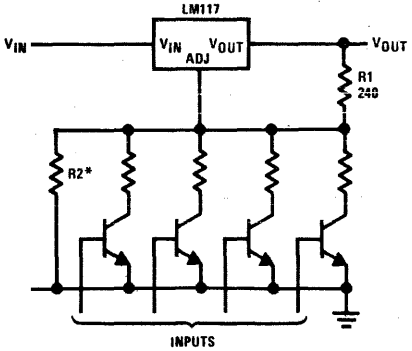


†Optional—improves transient response

*Needed if device is far from filter capacitors

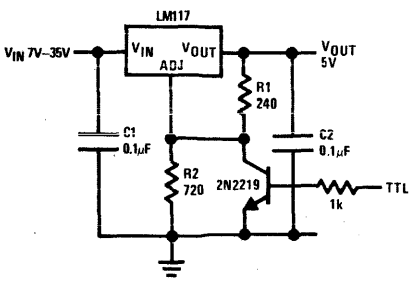
††$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right)$

Digitally Selected Outputs



*Sets maximum V_{OUT}

5V Logic Regulator with Electronic Shutdown*



* Min output ≈ 1.2V

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IM-B15M66/Printed in U.S.A.

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absolute maximum ratings

Power Dissipation	Internally limited
Input–Output Voltage Differential	40V
Operating Junction Temperature Range	
LM117	−55°C to +150°C
LM217	−25°C to +150°C
LM317	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	LM117/217			LM317			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	$T_A = 25°C$, $3V \le V_{IN} - V_{OUT} \le 40V$ (Note 2)		0.01	0.02		0.01	0.04	%/V
Load Regulation	$T_A = 25°C$, $10\ mA \le I_{OUT} \le I_{MAX}$							
	$V_{OUT} \le 5V$, (Note 2)		5	15		5	25	mV
	$V_{OUT} \ge 5V$, (Note 2)		0.1	0.3		0.1	0.5	%
Adjustment Pin Current			50	100		50	100	μA
Adjustment Pin Current Change	$10\ mA \le I_L \le I_{MAX}$ $2.5V \le (V_{IN}-V_{OUT}) \le 40V$		0.2	5		0.2	5	μA
Reference Voltage	$3 \le (V_{IN}-V_{OUT}) \le 40V$, (Note 3) $10\ mA \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$	1.20	1.25	1.30	1.20	1.25	1.30	V
Line Regulation	$3V \le V_{IN} - V_{OUT} \le 40V$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	$10\ mA \le I_{OUT} \le I_{MAX}$, (Note 2)							
	$V_{OUT} \le 5V$		20	50		20	70	mV
	$V_{OUT} \ge 5V$		0.3	1		0.3	1.5	%
Temperature Stability	$T_{MIN} \le T_j \le T_{MAX}$		1			1		%
Minimum Load Current	$V_{IN}-V_{OUT} = 40V$		3.5	5		3.5	10	mA
Current Limit	$V_{IN}-V_{OUT} \le 15V$							
	K and T Package	1.5	2.2		1.5	2.2		A
	H and P Package	0.5	0.8		0.5	0.8		A
	$V_{IN}-V_{OUT} = 40V$							
	K and T Package		0.4			0.4		A
	H and P Package		0.07			0.07		A
RMS Output Noise, % of V_{OUT}	$T_A = 25°C$, $10\ Hz \le f \le 10\ kHz$		0.003			0.003		%
Ripple Rejection Ratio	$V_{OUT} = 10V$, f = 120 Hz		65			65		dB
	$C_{ADJ} = 10\mu F$	66	80		66	80		dB
Long-Term Stability	$T_A = 125°C$		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	H Package		12	15		12	15	°C/W
	K Package		2.3	3		2.3	3	°C/W
	T Package					5		°C/W
	P Package					12		°C/W

Note 1: Unless other wise specified, these specifications apply $-55°C \le T_j \le +150°C$ for the LM117, $-25°C \le T_j \le +150°C$ for the LM217 and $0°C \le T_j \le +125°C$ for the LM317; $V_{IN}-V_{OUT} = 5V$ and $I_{OUT} = 0.1A$ for the TO-5 package and $I_{OUT} = 0.5A$ for the TO-3 package and TO-220 package. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-5 and 20W for the TO-3 and TO-220. I_{MAX} is 1.5A for the TO-3 and TO-220 package and 0.5A for the TO-5 package.

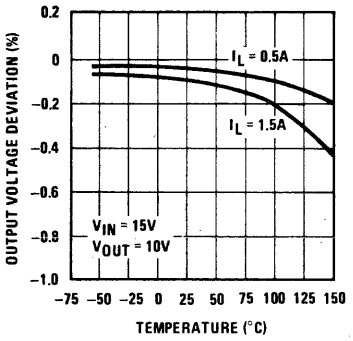
Note 2: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Note 3: Selected devices with tightend tolerance reference voltage available.

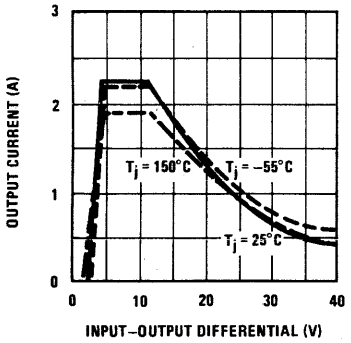
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typical performance characteristics (K and T Packages)

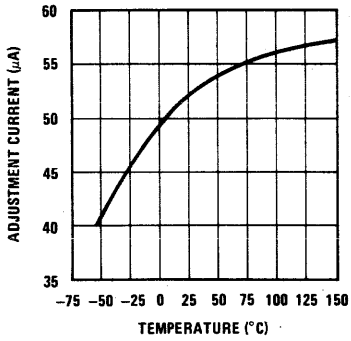
Load Regulation



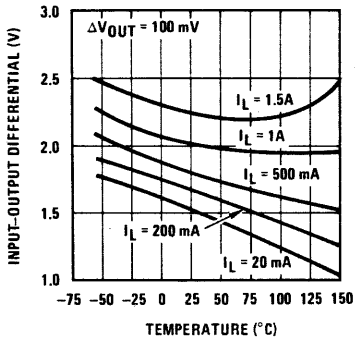
Current Limit



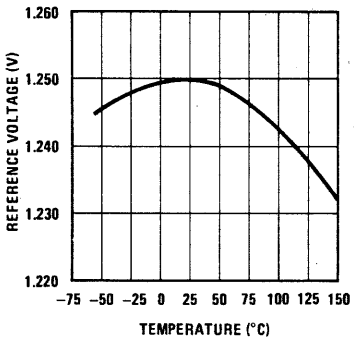
Adjustment Current



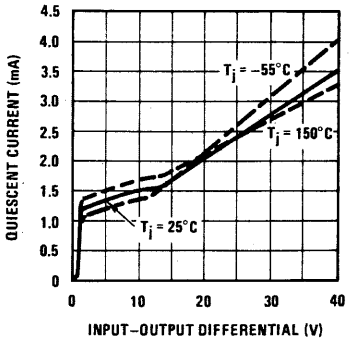
Dropout Voltage



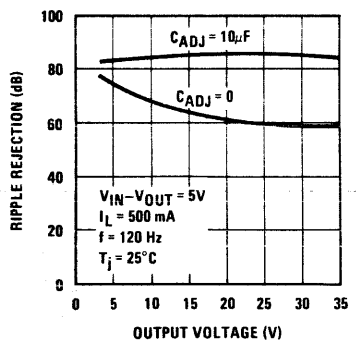
Temperature Stability



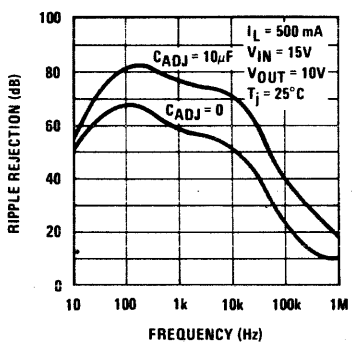
Minimum Operating Current



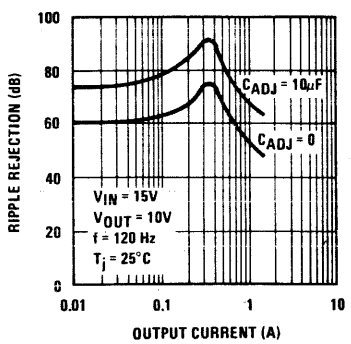
Ripple Rejection



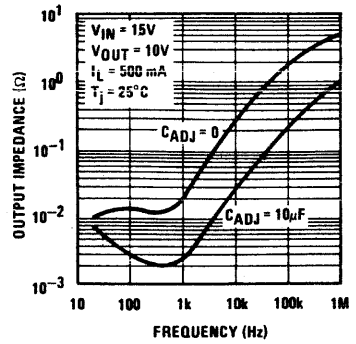
Ripple Rejection



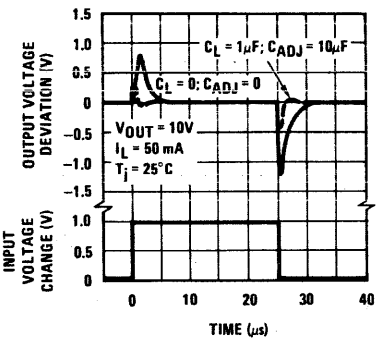
Ripple Rejection



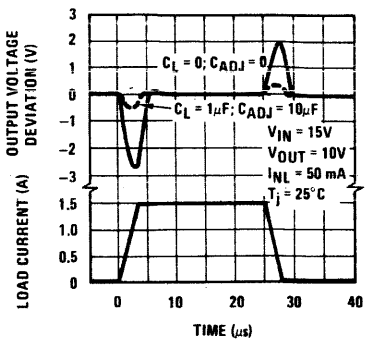
Output Impedance



Line Transient Response



Load Transient Response



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application hints

In operation, the LM117 develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

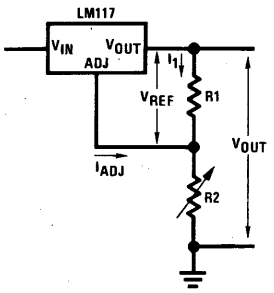


FIGURE 1.

Since the 100μA current from the adjustment terminal represents an error term, the LM117 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A 0.1μF disc or 1μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM117 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10μF bypass capacitor 80 dB ripple rejection is obtainable at any output level. Increases over 10μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

In general, the best type of capacitors to use are solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25μF in aluminum electrolytic to equal 1μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01μF disc may seem to work better than a 0.1μF disc as a bypass.

Although the LM117 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1μF solid tantalum (or 25μF aluminum electrolytic) on the output swamps this effect and insures stability.

Load Regulation

The LM117 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectvely in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω x I_L. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.

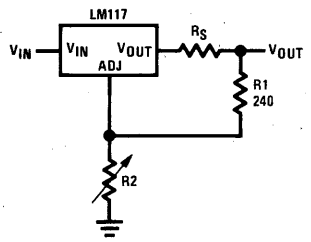


FIGURE 2. Regulator with Line Resistance in Output Lead

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the case. However, with the TO-5 package, care should be taken to minimize the wire length of the output lead. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

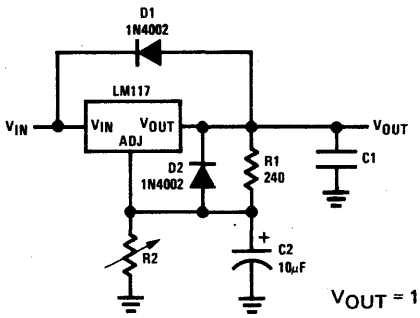
Protection Diodes

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10μF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge

current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM117, this discharge path is through a large junction that is able to sustain 15A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25μF or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM117 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and 10μF capacitance. *Figure 3* shows an LM117 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.

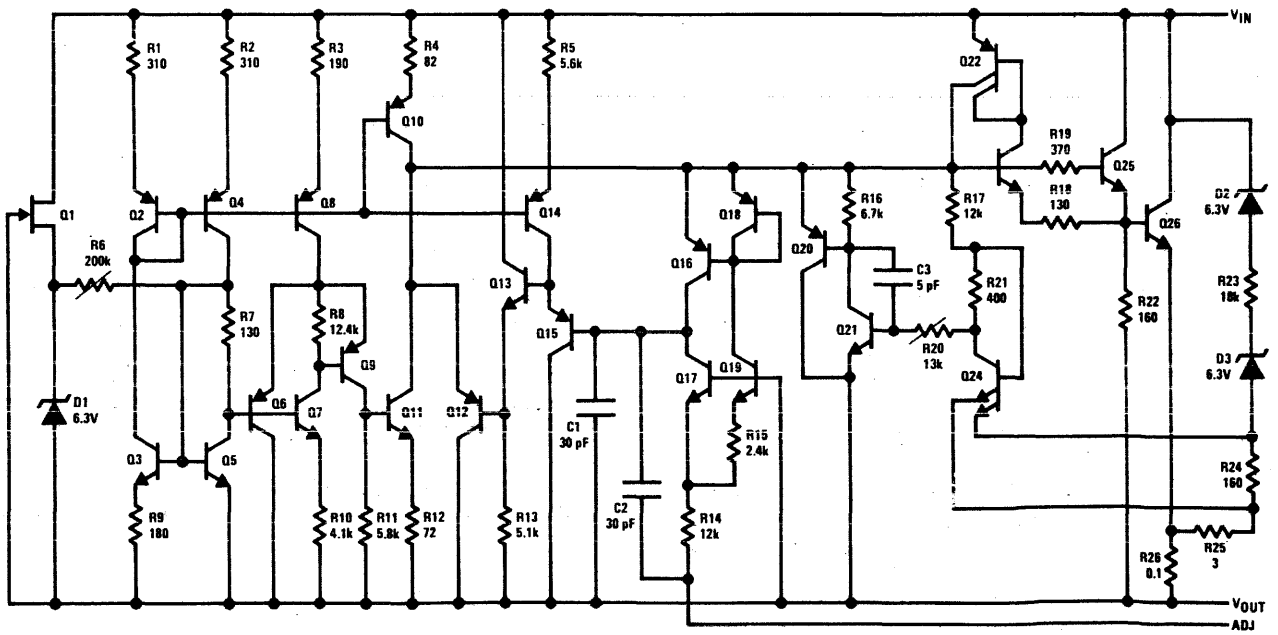


$$V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right) + R2 I_{ADJ}$$

D1 protects against C1
D2 protects against C2

FIGURE 3. Regulator with Protection Diodes

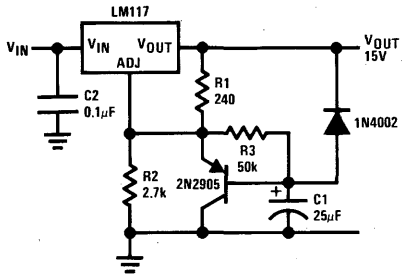
schematic diagram



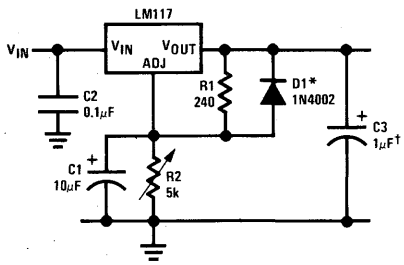
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typical applications (con't)

Slow Turn-On 15V Regulator



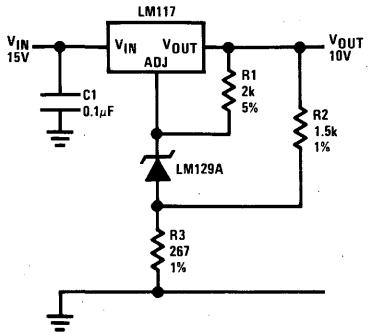
Adjustable Regulator with Improved Ripple Rejection



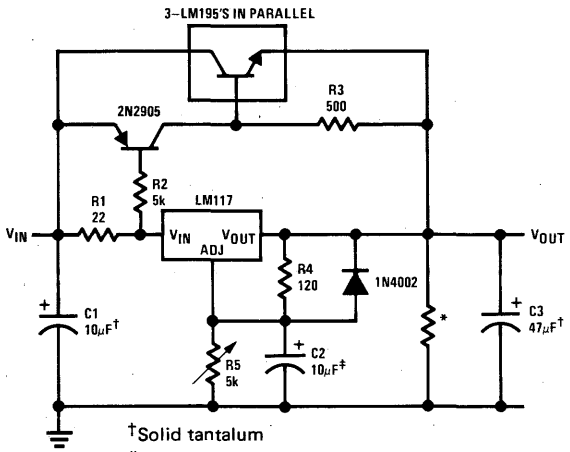
†Solid tantalum

*Discharges C1 if output is shorted to ground

High Stability 10V Regulator



High Current Adjustable Regulator

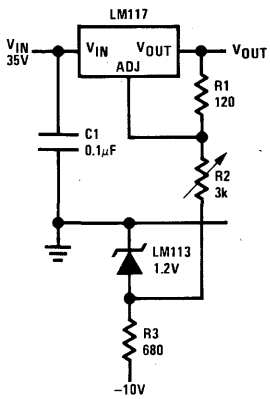


†Solid tantalum

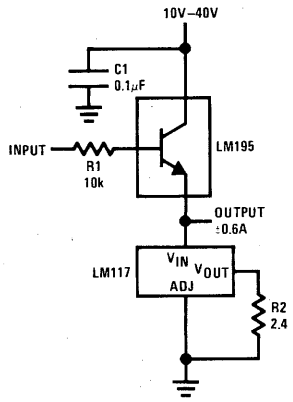
*Minimum load current = 30 mA

‡Optional—improves ripple rejection

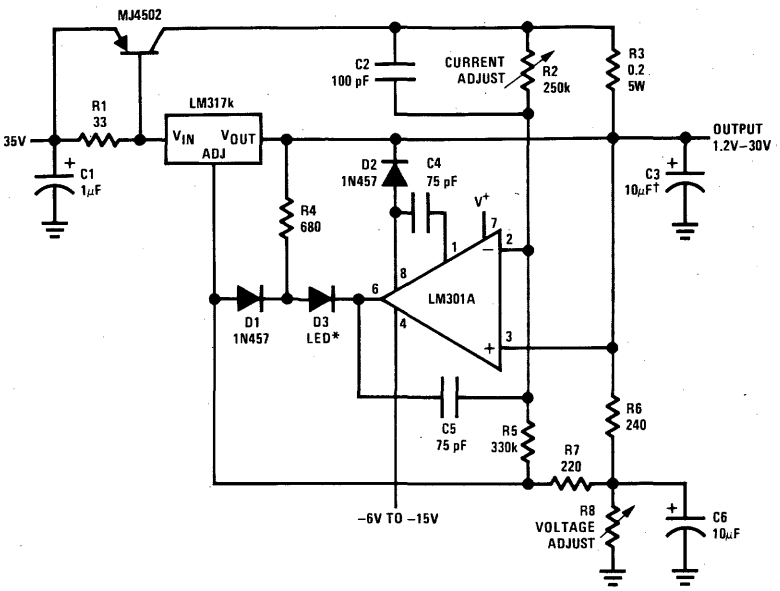
0 to 30V Regulator



Power Follower



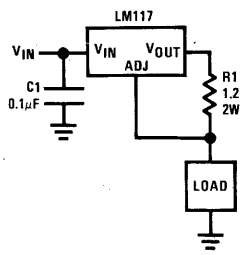
5A Constant Voltage/Constant Current Regulator



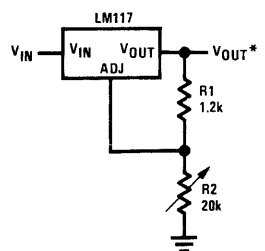
†Solid tantalum

*Lights in constant current mode

1A Current Regulator



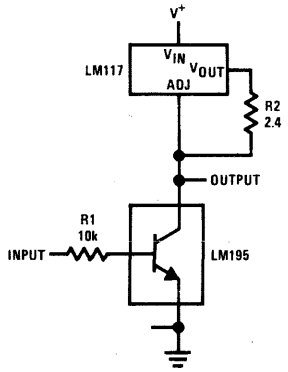
1.2V–20V Regulator with Minimum Program Current



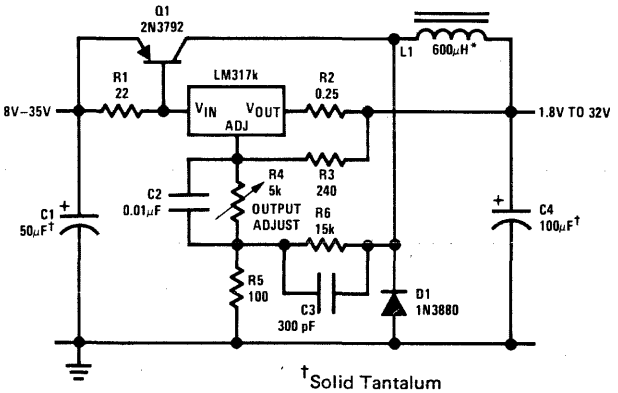
*Minimum load current ≈ 4 mA

typical applications (con't)

High Gain Amplifier



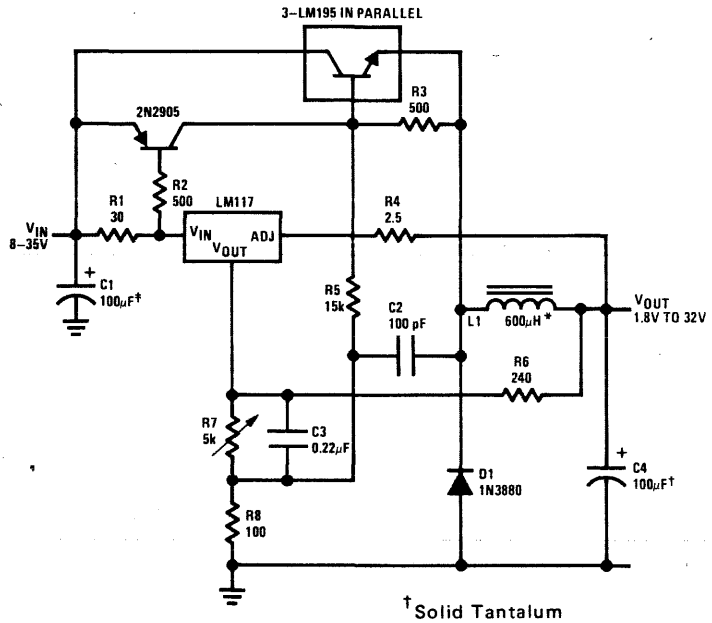
Low Cost 3A Switching Regulator



†Solid Tantalum

*Core–Arnold A-254168-2 60 turns

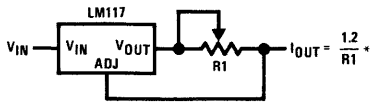
4A Switching Regulator with Overload Protection



†Solid Tantalum

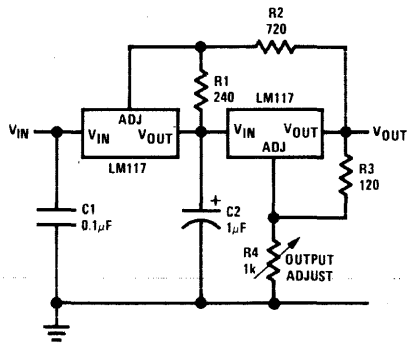
*Core Arnold A-254168-2 60 turns

Precision Current Limiter

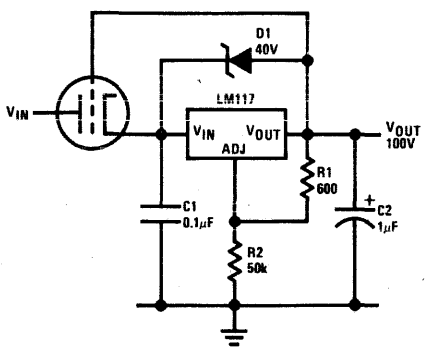


*0.8Ω ≤ R1 ≤ 120Ω

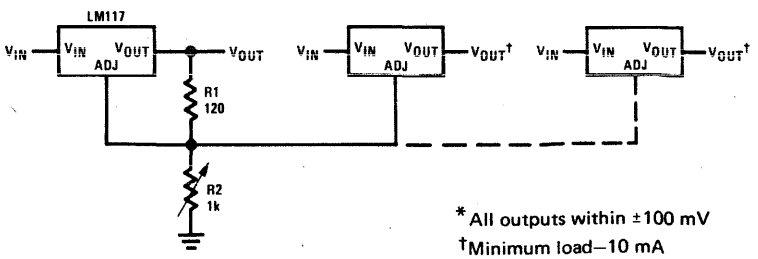
Tracking Preregulator



High Voltage Regulator



Adjusting Multiple On-Card Regulators with Single Control*



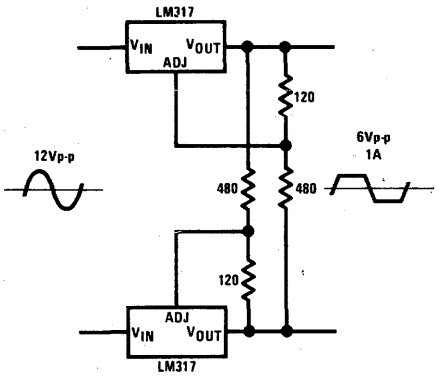
*All outputs within ±100 mV

†Minimum load–10 mA

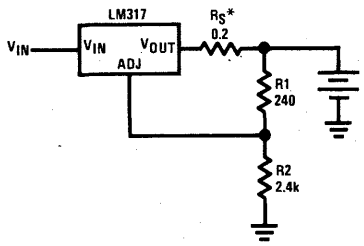
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typical applications (con't)

AC Voltage Regulator

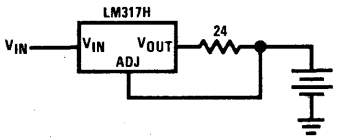


12V Battery Charger

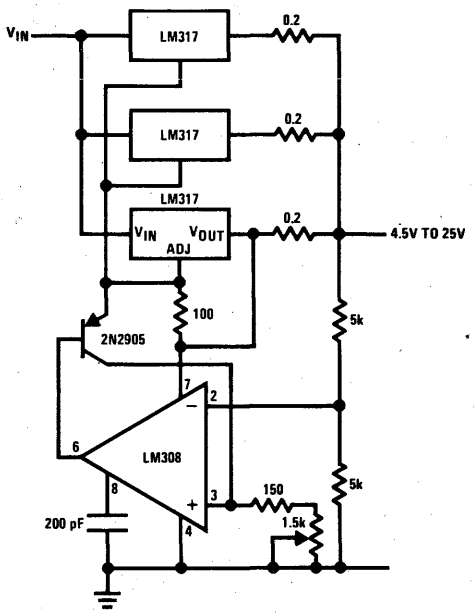


*R_S—sets output impedance of charger $Z_{OUT} = R_S\left(1 + \frac{R2}{R1}\right)$
Use of R_S allows low charging rates with fully charged battery.

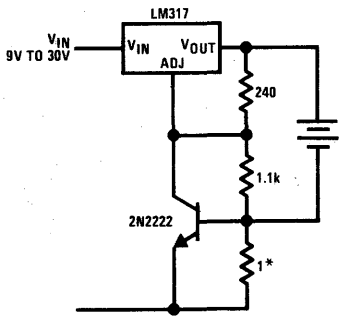
50 mA Constant Current Battery Charger



Adjustable 4A Regulator



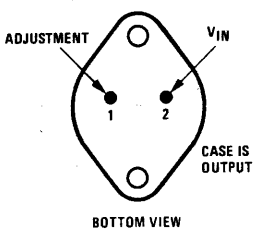
Current Limited 6V Charger



*Sets peak current (0.6A for 1Ω)

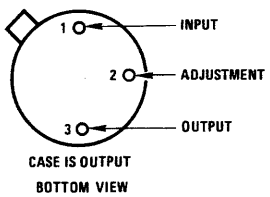
connection diagrams

Metal Can Package



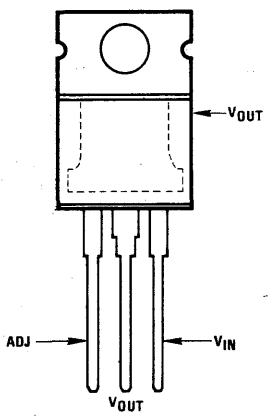
Order Number LM117K, LM217K or LM317K

Metal Can Package



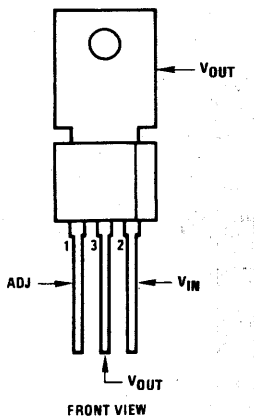
Order Number LM117H, LM217H or LM317H

Plastic Package



Order Number LM317T

Plastic Package



Order Number LM317P

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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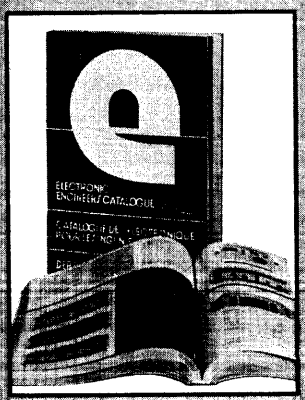
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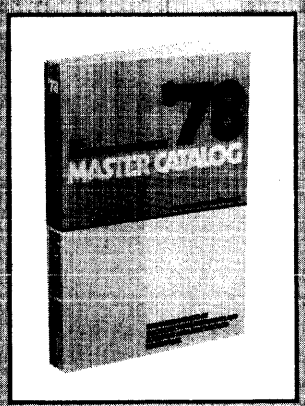


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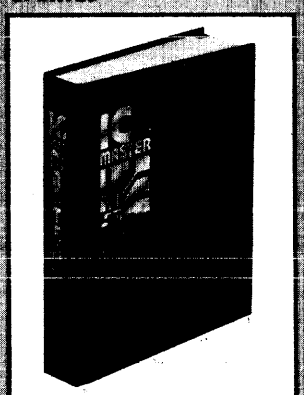
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OP-01

INVERTING HIGH SPEED OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The OP-01 Series of monolithic High Speed Operational Amplifiers combines high slew rate, fast settling time output performance with excellent D.C. input characteristics.

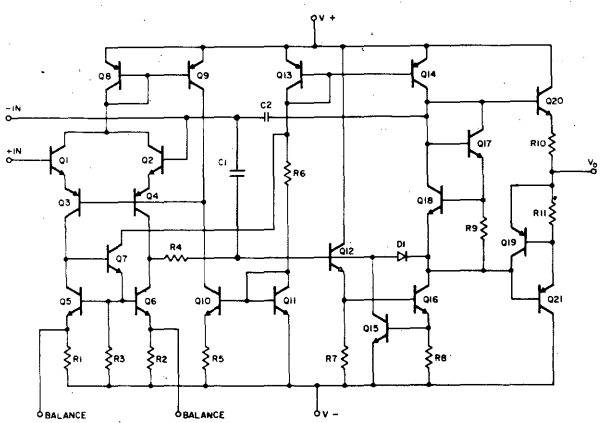
An internal feed-forward frequency compensation network provides simplicity of application—no external capacitors are required for stable, high-speed performance. The fast output response is achieved without sacrifice in input bias current or power consumption. 250kHz power bandwidth is attained with a small signal bandwidth of 2.5 MHz, allowing non-critical board layout. The OP-01 is completely protected at both input and output, fits standard 741 sockets, and is offset nulled with a 10kΩ potentiometer.

The low offset voltage, input bias current and offset voltage drift vs. temperature provide accurate D.C. performance in applications such as channel preamplifiers, fast integrators and precision summing amplifiers. The fast output response makes the OP-01 ideal in state-variable filters, servo drivers, waveform generators, analog computing amplifiers, and D/A converter output amplifiers.

FEATURES

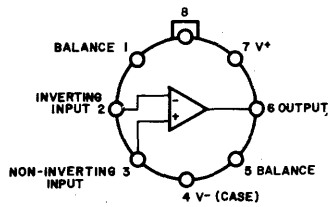
- Fast Settling Time . . . . . 1 μsec to 0.1%
- High Slew Rate . . . . . 18 V/μsec
- Power Bandwidth . . . . . 250 kHz
- Low Power Consumption . . . . . 90 mW Max
- Excellent D.C. Specifications
- Internally Compensated
- Ideal DAC Output Amplifier
- MIL-STD-883 Processing Available
- Fits Standard 741 Sockets
- Low Cost

SIMPLIFIED SCHEMATIC

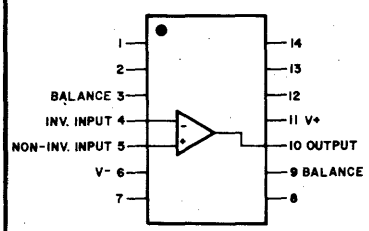


PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW

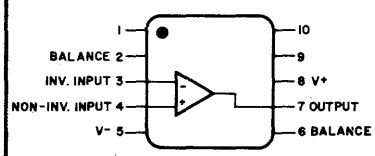


TO-99 (J-Suffix)
ORDER: OP-01J
OP-01FJ
OP-01GJ
OP-01HJ
OP-01EJ
OP-01CJ



14 PIN DIP (Y-Suffix)*
ORDER: OP-01Y
OP-01FY
OP-01GY
OP-01HY
OP-01EY
OP-01CY

*Formerly "P" Suffix



10 PIN FLATPACK (L-Suffix)
ORDER: OP-01L
OP-01FL
OP-01GL

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ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage		Short Circuit Duration	Indefinite
OP-01, OP-01F, OP-01E, OP-01H	±22V	Operating Temperature Range	
OP-01G, OP-01C	±20V	OP-01, OP-01F, OP-01G	-55°C to +125°C
Power Dissipation (see note)	500mW	OP-01H, OP-01E, OP-01C	0°C to +70°C
Differential Input Voltage	±30V	Storage Temperature Range	-65°C to +150°C
Input Voltage	±15V	Lead Temperature (Soldering, 60 Sec)	300°C

NOTE: Maximum Package Power Dissipation vs. ambient temperature

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
Dual-in-Line (P, Y)	100°C	10.0mW/°C
Flat Pack (L)	62°C	5.7mW/°C

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, T_A = 25°C unless otherwise noted.

Parameter	Symbol	Test Conditions	OP-01 OP-01H Min	OP-01 OP-01H Typ	OP-01 OP-01H Max	OP-01F OP-01E Min	OP-01F OP-01E Typ	OP-01F OP-01E Max	OP-01G OP-01C Min	OP-01G OP-01C Typ	OP-01G OP-01C Max	Units
Input Offset Voltage	V_{OS}	$R_S \leq 50k\Omega$	–	0.3	0.7	–	1.0	2.0	–	2.0	5.0	mV
Input Offset Current	I_{OS}		–	0.5	2.0	–	1.0	5.0	–	2.0	20	nA
Input Bias Current	I_B		–	18	30	–	20	50	–	25	100	nA
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_S \leq 50k\Omega$	90	110	–	80	100	–	80	100	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±20V $R_S \leq 50k\Omega$	90	110	–	80	100	–	80	100	–	dB
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	±12.5 ±12.0	±13.5 ±13.0	– –	±12.5 ±12.0	±13.5 ±13.0	– –	±12.5 ±12.0	±13.5 ±13.0	– –	V V
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega, V_O = \pm 10V$	50	100	–	50	100	–	25	75	–	V/mV
Power Consumption	P_D	V_{OUT} = 0	–	40	60	–	50	90	–	50	90	mW
Settling Time to 0.1% (Summing Node Error)		A_V = -1 (Note) V_{IN} = 5V	–	0.7	1.0	–	0.7	1.0	–	0.7	1.0	µsec
Slew Rate			–	18	–	–	18	–	–	18	–	V/µs
Large Signal Bandwidth			–	250	–	–	250	–	–	250	–	kHz
Small Signal Bandwidth			–	2.5	–	–	2.5	–	–	2.5	–	MHz
Risetime (Note)		A_V = -1 V_{IN}=50mV	–	150	–	–	150	–	–	150	–	nsec
Overshoot (Note)			–	2	–	–	2	–	–	2	–	%
The following specifications apply for V_S = ±15V, -55°C ≤ T_A ≤ +125°C for OP-01, OP-01F, OP-01G and 0°C ≤ T_A ≤ +70°C for OP-01H, OP-01E, OP-01C, unless otherwise specified.												
Input Offset Voltage	V_{OS}	$R_S \leq 50k\Omega$	–	0.4	1.0	–	1.5	3.0	–	3.0	6.0	mV
Input Offset Current	I_{OS}		–	1.0	4.0	–	2.0	10	–	4.0	40	nA
Input Bias Current	I_B		–	30	50	–	40	100	–	50	200	nA
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM}=±CMVR $R_S \leq 50k\Omega$	90	110	–	80	100	–	80	100	–	dB
Power Supply Rejection Ratio	PSRR	V_S=± 5V to ±20V $R_S \leq 50k\Omega$	90	110	–	80	100	–	80	100	–	dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega, V_O = \pm 10V$	30	60	–	25	60	–	15	50	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	±12.5 ±12.0	±13.5 ±13.0	– –	±12.5 ±12.0	±13.5 ±13.0	– –	±12.5 ±12.0	±13.5 ±13.0	– –	V V
Offset Voltage Drift	TCV_{OS}	$R_S \leq 5k\Omega$	–	2.0	8.0	–	3.0	10.0	–	5.0	20.0	µV/°C

NOTE: R_L = 2kΩ, C_L = 50pF. See Settling Time Test Circuit.

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IMPROVED PM741/SSS741

OP-02

HIGH PERFORMANCE GENERAL PURPOSE OPERATIONAL AMPLIFIER

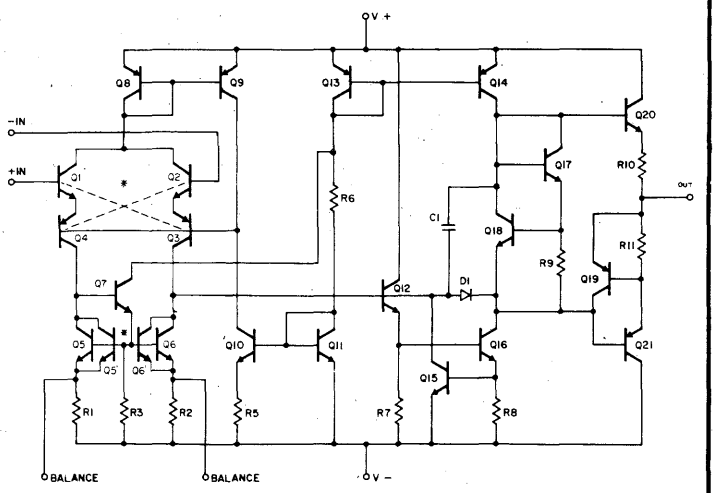
GENERAL DESCRIPTION

The OP-02 Series of High Performance General Purpose Operational Amplifiers provides significant improvements over industry-standard and "premium" 741 types while maintaining pin-for-pin compatibility, ease of application, and low cost. Key specifications, such as V_{OS}, I_{OS}, I_B, CMRR, PSRR and A_{VO}, are guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process eliminates "popcorn noise." A thermally-symmetrical input stage design provides low TCV_{OS}, TCI_{OS} and insensitivity to output load conditions. The OP-02 Series is ideal for upgrading existing designs where accuracy improvements are required and for eliminating special low drift or low noise selected types. OP-02's with MIL-STD-883 processing are available. For dual high performance matched general purpose operational amplifiers, refer to the OP-04 and OP-14 data sheets.

FEATURES

- Excellent D.C. Input Specifications
- Fits Standard 741 Socket
- Internally Compensated
- Low Noise ..... 0.65 μVp-p
- Low Drift (TCV_{OS}) ..... 8 $\mu V/^{\circ}C$
- "Premium" 741 Replacement
- 0°C/+70°C and –55°C/+125°C Models
- MIL-STD-883 Processing Available
- Silicon-Nitride Passivation
- Low Cost

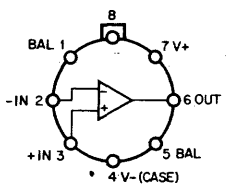
SIMPLIFIED SCHEMATIC



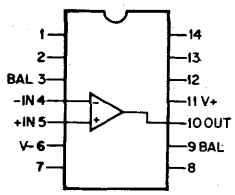
*Q1, Q2, Q3 & Q4 FORM A THERMALLY CROSS-COUPLED TRANSISTOR QUAD. Q5, Q5', Q6 & Q6' COMPRISE A SIMILAR THERMALLY CROSS-COUPLED QUAD.

PIN CONNECTIONS AND ORDERING INFORMATION

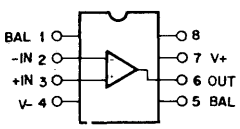
TOP VIEW



TO-99 (J-Suffix)
ORDER:
OP-02AJ
OP-02J
OP-02EJ
OP-02CJ



14 PIN HERMETIC DIP (Y-Suffix)
ORDER:
OP-02AY
OP-02Y
OP-02EY
OP-02CY



EPOXY B MINI-DIP (P-Suffix)
ORDER:
OP-02CP

Military Temperature Range Devices with MIL-STD-883A Class B Processing:

ORDER: OP02-883-AJ
OP02-883-AY
OP02-883-J
OP02-883-Y

Precision Monolithics

LINEAR

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ELECTRICAL CHARACTERISTICS			OP-02A			OP-02			
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.3	0.5	–	1.0	2.0	mV
Input Offset Current	I_{os}		–	0.5	2.0	–	1.0	5.0	nA
Input Bias Current	I_B		–	18	30	–	20	50	nA
Input Resistance-Differential Mode	R_{in}		3.8	7.5	–	2.3	7.0	–	MΩ
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_o = ±10V	100	250	–	50	200	–	V/mV
Power Consumption	P_d	V_o = 0V	–	40	60	–	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.65	–	–	0.65	–	μV p-p
Input Noise Voltage Density	e_n	f_o = 10Hz f_o = 100Hz f_o = 1000Hz	– – –	25 22 21	– – –	– – –	25 22 21	– – –	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	12.8	–	–	12.8	–	pA p-p
Input Noise Current Density	i_n	f_o = 10Hz f_o = 100Hz f_o = 1000Hz	– – –	1.4 0.7 0.4	– – –	– – –	1.4 0.7 0.4	– – –	pA/√Hz
Slew Rate (Note 1)	SR		0.25	0.5	–	0.25	0.5	–	V/μs
Large Signal Bandwidth (Note 1)		V_o = 20Vp-p	4.0	8.0	–	4.0	8.0	–	kHz
Closed Loop Bandwidth (Note 1)	BW	A_{VCL} = +1.0	0.8	1.3	–	0.8	1.3	–	MHz
Risetime (Note 1)		A_V = +1 V_{IN} = 50mV	–	200	300	–	200	300	nsec
Overshoot (Note 1)			–	5	10	–	5	10	%
The following specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted									
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.5	1.0	–	1.4	3.0	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{os}	$R_s \leq 5k\Omega$	–	2.0	8.0	–	4.0	10.0	μV/°C
Input Offset Current	I_{os}		–	1.0	5.0	–	2.0	10.0	nA
Average Input Offset Current Drift (Note 1)	TCI_{os}		–	7.5	75	–	15	150	pA/°C
Input Bias Current	I_B		–	30	55	–	40	100	nA
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_o = ±10V	50	100	–	25	60	–	V/mV
Maximum Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V
Note 1: Parameter is not 100% tested. 90% of all units meet these specifications.									

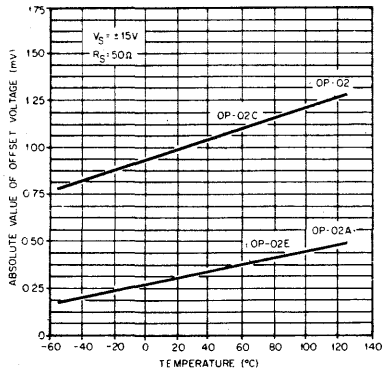
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ELECTRICAL CHARACTERISTICS			OP-02E			OP-02C			
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.3	0.5	–	1.0	2.0	mV
Input Offset Current	I_{os}		–	0.5	2.0	–	1.0	5.0	nA
Input Bias Current	I_B		–	18	30	–	20	50	nA
Input Resistance-Differential Mode	R_{in}		3.8	7.5	–	2.3	7.0	–	MΩ
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_o = ±10V	100	250	–	50	200	–	V/mV
Power Consumption	P_d	V_o = 0V	–	40	60	–	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.65	–	–	0.65	–	μV p-p
Input Noise Voltage Density	e_n	f_o = 10Hz f_o = 100Hz f_o = 1000Hz	– – –	25 22 21	– – –	– – –	25 22 21	– – –	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	12.8	–	–	12.8	–	pA p-p
Input Noise Current Density	i_n	f_o = 10Hz f_o = 100Hz f_o = 1000Hz	– – –	1.4 0.7 0.4	– – –	– – –	1.4 0.7 0.4	– – –	pA/√Hz
Slew Rate (Note 1)	SR		0.25	0.5	–	0.25	0.5	–	V/μs
Large Signal Bandwidth (Note 1)		V_o = 20Vp-p	4.0	8.0	–	4.0	8.0	–	kHz
Closed Loop Bandwidth (Note 1)	BW	A_{VCL} = +1.0	0.8	1.3	–	0.8	1.3	–	MHz
Risetime (Note 1)		A_V = +1 V_{IN} = 50mV	–	200	300	–	200	300	nsec
Overshoot (Note 1)			–	5	10	–	5	10	%
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.									
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.4	1.0	–	1.2	3.0	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{os}	$R_s \leq 5k\Omega$	–	2.0	8.0	–	4.0	10.0	μV/°C
Input Offset Current	I_{os}		–	0.7	4.0	–	1.4	10.0	nA
Average Input Offset Current Drift (Note 1)	TCI_{os}		–	7.5	120	–	15	250	pA/°C
Input Bias Current	I_B		–	22	50	–	25	100	nA
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_o = ±10V	50	200	–	25	150	–	V/mV
Maximum Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V
Note 1: Parameter is not 100% tested. 90% of all units meet these specifications.									

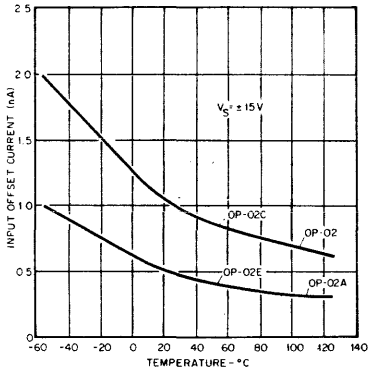
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TYPICAL PERFORMANCE CURVES

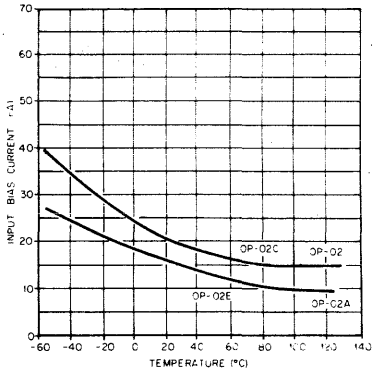
UNTRIMMED OFFSET VOLTAGE VS TEMPERATURE



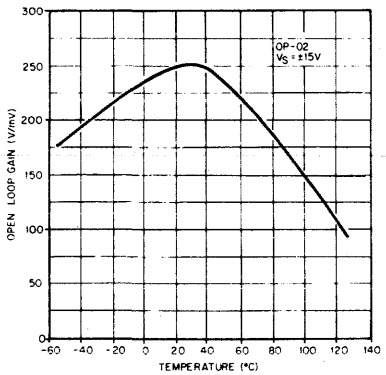
INPUT OFFSET CURRENT VS TEMPERATURE



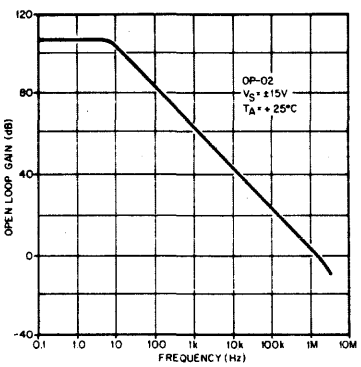
INPUT BIAS CURRENT VS TEMPERATURE



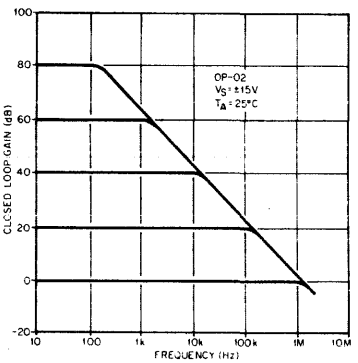
OPEN LOOP GAIN VS TEMPERATURE



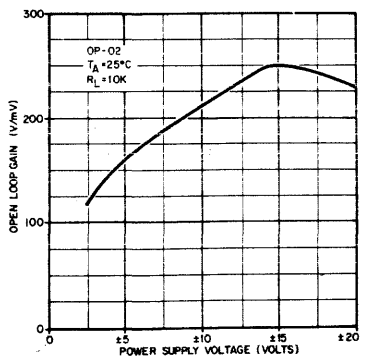
OPEN LOOP FREQUENCY RESPONSE



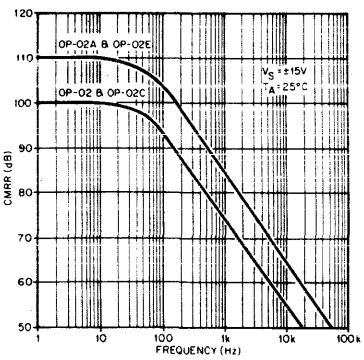
CLOSED LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



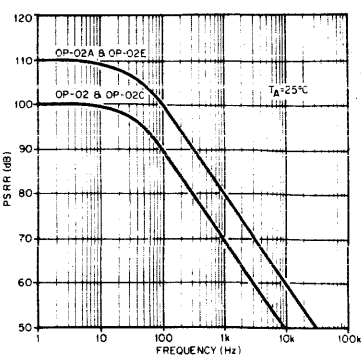
OPEN LOOP GAIN VS POWER SUPPLY VOLTAGE



CMRR VS FREQUENCY



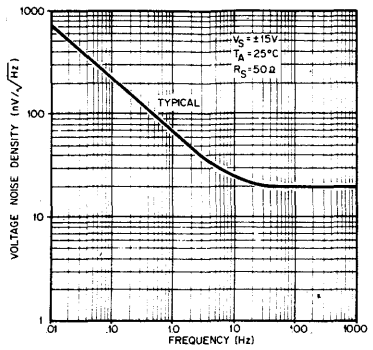
PSRR VS FREQUENCY



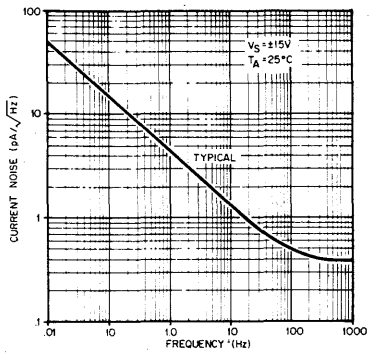
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TYPICAL PERFORMANCE CURVES

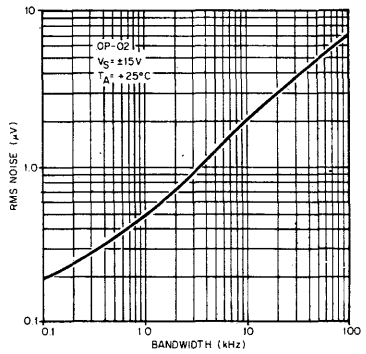
INPUT SPOT NOISE VOLTAGE VS FREQUENCY



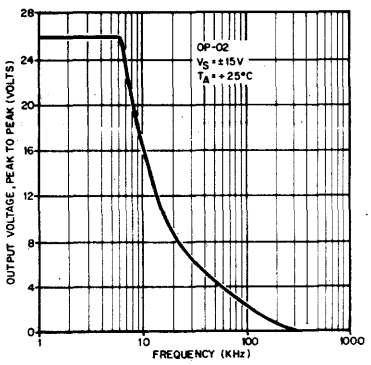
INPUT SPOT NOISE CURRENT VS FREQUENCY



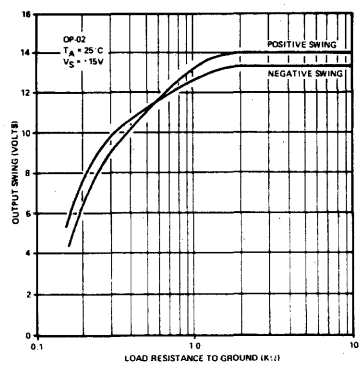
INPUT WIDEBAND NOISE VS BANDWIDTH (.1 Hz TO FREQUENCY INDICATED)



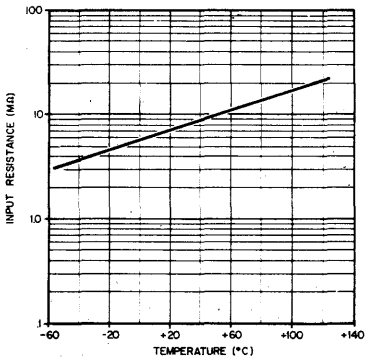
MAXIMUM UNDISTORTED OUTPUT VS FREQUENCY



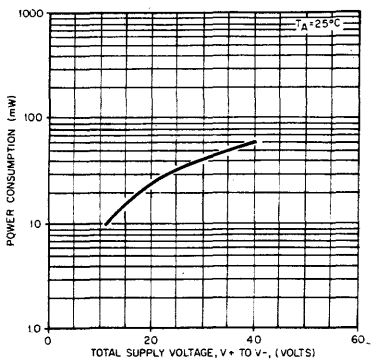
OUTPUT VOLTAGE VS LOAD RESISTANCE



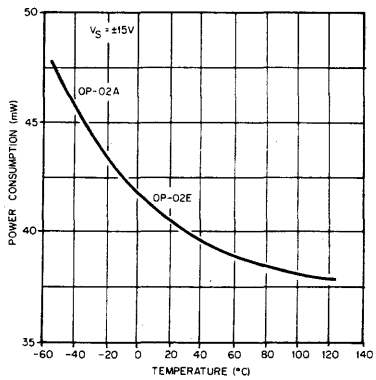
INPUT RESISTANCE VS TEMPERATURE



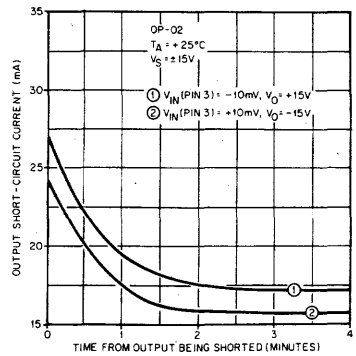
POWER CONSUMPTION VS POWER SUPPLY



POWER CONSUMPTION VS TEMPERATURE



OUTPUT SHORT-CIRCUIT CURRENT VS TIME



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IMPROVED PM747/SSS747

OP-04

DUAL MATCHED HIGH PERFORMANCE OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

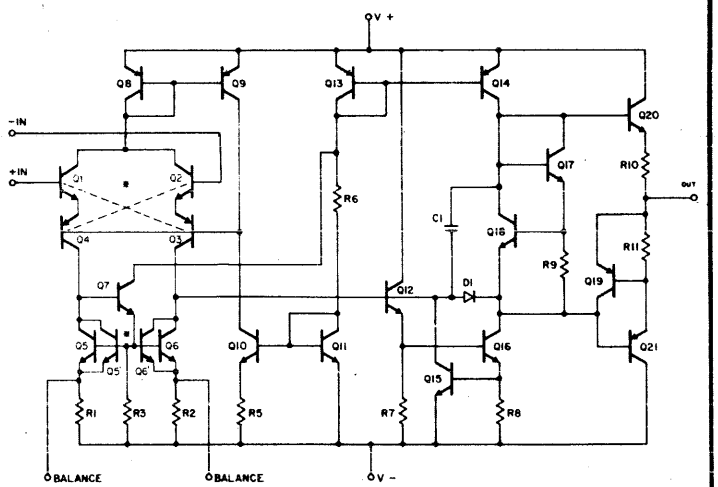
The OP-04 Series of Dual Matched High Performance General Purpose Operational Amplifiers provides significant improvements over industry-standard 747 types while maintaining pin-for-pin compatibility, ease of application, and low cost. Key specifications, such as V_{OS}, I_{OS}, I_B, CMRR, PSRR and A_{VO}, are guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process eliminates "popcorn noise." A thermally-symmetrical input stage design provides low TCV_{OS}, TCI_{OS} and insensitivity to output load conditions. The OP-04 Series is ideal for upgrading existing designs where accuracy improvements are required and for eliminating special low drift or low noise selected types. For more stringent requirements, refer to the OP-10 Dual Matched Instrumentation Operational Amplifier data sheet.

FEATURES

- Excellent D.C. Input Specifications
- Matched V_{OS} and CMRR
- Fits Standard 747 Socket
- Internally Compensated
- Low Noise
- Low Drift
- Low Cost
- 0°C/+70°C and −55°C/+125°C Models
- Silicon-Nitride Passivation
- Models With MIL-STD-883A Class B Processing Available From Stock

SIMPLIFIED SCHEMATIC

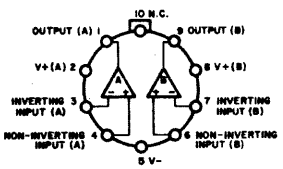
(1/2 OF CIRCUIT SHOWN)



*Q1, Q2, Q3 & Q4 FORM A THERMALLY CROSS-COUPLED TRANSISTOR QUAD. Q5, Q5', Q6 & Q6' COMPRISE A SIMILAR THERMALLY CROSS-COUPLED QUAD.

PIN CONNECTIONS AND ORDERING INFORMATION

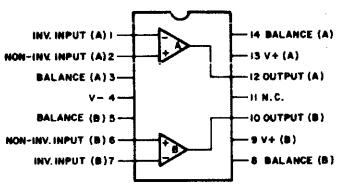
TOP VIEW



TO-100 (K-Suffix)

ORDER: OP-04AK
OP-04K
OP-04EK
OP-04CK

14 PIN HERMETIC DIP (Y-Suffix)



ORDER: OP-04AY
OP-04Y
OP-04EY
OP-04CY

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:

ORDER: OP04-883-AK
OP04-883-K
OP04-883-AY
OP04-883-Y

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IMPROVED PM1458/SSS1458

OP-14

DUAL MATCHED HIGH PERFORMANCE OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

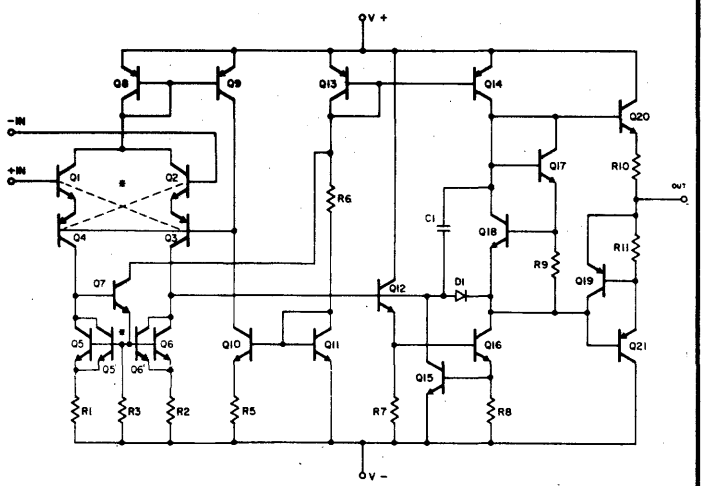
The OP-14 Series of Dual Matched High Performance General Purpose Operational Amplifiers provides significant improvements over industry-standard 1458/1558 types while maintaining pin-for-pin compatibility, ease of application, and low cost. Key specifications, such as V_{OS}, I_{OS}, I_B, CMRR, PSRR, and A_{VO}, are guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process eliminates "popcorn noise." A thermally-symmetrical input stage design provides low TCV_{OS}, TCI_{OS} and insensitivity to output load conditions. The OP-14 Series is ideal for upgrading existing designs where accuracy improvements are required and for eliminating special low drift or low noise selected types. For similar devices with nulling capability, refer to the OP-04 data sheet.

FEATURES

- Excellent D.C. Input Specifications
- Matched V_{OS} and CMRR
- Fits Standard 1458/1558 Socket
- Internally Compensated
- Low Noise
- Low Drift
- Low Cost
- 0°C/+70°C and –55°C/+125°C Models
- Silicon-Nitride Passivation
- Models With MIL-STD-883A Class B Processing Available From Stock

SIMPLIFIED SCHEMATIC

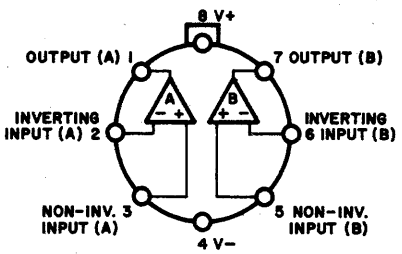
(1/2 OF CIRCUIT SHOWN)



*Q1, Q2, Q3 & Q4 FORM A THERMALLY CROSS-COUPLED TRANSISTOR QUAD. Q5, Q5', Q6 & Q6' COMPRISE A SIMILAR THERMALLY CROSS-COUPLED QUAD.

PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



TO-99 (J-Suffix)

ORDER: OP-14AJ
OP-14J
OP-14EJ
OP-14CJ

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:

ORDER: OP14-883-AJ
OP14-883-J

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Indefinite
Storage Temperature Range	− 5° to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Operating Temperature Range

OP-04A/14A, OP-04/14	−55°C to +125°C
OP-04E/14E. OP-04C/14C	0°C to +70°C

Note 1: Maximum package power dissipation vs. ambient temperature.

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
DUAL-IN-LINE (Y)	100°C	10.0mW/°C
TO-100 (K)	80°C	7.1mW/°C

MATCHING CHARACTERISTICS

OP-04A OP-04E OP-14A OP-14E | OP-04 OP-04C OP-14 OP-14C

These specifications apply for V_S = ±15V, T_A = 25°C, $R_S \leq 100\Omega$, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage Match	ΔV_{OS}			0.3	1.0	—	1.0	2.0	mV
Common Mode Rejection Ratio Match	ΔCMRR	V_{CM} = ± CMVR	94	106	—	94	106	—	dB
These specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C for OP-04A and OP-04, 0°C ≤ T_A ≤ 70°C for OP-04E and OP-04C $R_S \leq 100\Omega$, unless otherwise noted.									
Input Offset Voltage Match	ΔV_{OS}		—	0.5	1.5	—	1.5	3.0	mV
Common Mode Rejection Ratio Match	ΔCMRR	V_{CM} = ± CMVR	90	100	—	90	100	—	dB

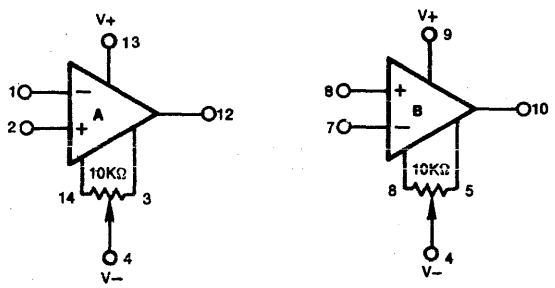
MATCHING PARAMETER DEFINITIONS

COMMON MODE REJECTION RATIO MATCH (ΔCMRR)
The difference between the common-mode rejection ratios (expressed in volt/volt) of side A and side B.
ΔCMRR in dB = 20 $\log_{10}$ (ΔCMRR in volt/volt).

INPUT OFFSET VOLTAGE MATCH (ΔV_{os}). The difference between the offset voltages of side A and side B; ($V_{OSA} - V_{OSB}$).

OFFSET NULLING CIRCUITS

DIP (Y) PACKAGE ONLY
OP-04 ONLY



OP-04/OP-14 DEFINITIONS

INPUT OFFSET VOLTAGE (V_{os})
The voltage which must be applied between the input terminals to obtain zero output voltage with no load.

INPUT OFFSET CURRENT (i_{os})
The difference between the currents into the two input terminals when the output is at zero volts with no load.

INPUT BIAS CURRENT (I_B)
The average of the currents into the two input terminals when the output is at zero volts with no load.

INPUT VOLTAGE RANGE (CMVR)
The range of common-mode voltage on the input terminals for which the common-mode rejection specifications apply.

COMMON-MODE REJECTION RATIO (CMRR)
The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

POWER SUPPLY REJECTION RATIO (PSRR)
The inverse ratio of the change in input offset voltage to the change in power supply voltage producing it.

MAXIMUM OUTPUT VOLTAGE SWING (V_{om})
The peak output voltage that can be obtained without clipping.

LARGE SIGNAL VOLTAGE GAIN (A_{vo})
The ratio of the change in output voltage (over a specified range) to the change in input voltage producing it.

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ELECTRICAL CHARACTERISTICS (Each Amplifier)			OP-04A OP-14A			OP-04 OP-14			
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.3	0.75	–	1.0	2.0	mV
Input Offset Current	I_{os}		–	0.5	2.0	–	1.0	5.0	nA
Input Bias Current	I_B		–	18	50	–	20	75	nA
Input Resistance-Differential Mode	R_{in}		3.8	7.5	–	2.3	7.0	–	MΩ
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_o = ±10V	100	250	–	50	200	–	V/mV
Power Consumption	P_d	V_o = 0V	–	40	60	–	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.65	–	–	0.65	–	µV p-p
Input Noise Voltage Density	e_n	f_o = 10Hz f_o = 100Hz f_o = 1000Hz	– – –	25 22 21	– – –	– – –	25 22 21	– – –	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	12.8	–	–	12.8	–	pA p-p
Channel Separation	CS		100	–	–	100	–	–	dB
Input Noise Current Density	i_n	f_o = 10Hz f_o = 100Hz f_o = 1000Hz	– – –	1.4 0.7 0.4	– – –	– – –	1.4 0.7 0.4	– – –	pA/√Hz
Slew Rate (Note 1)	SR		0.5	0.5	–	0.5	0.7	–	V/µs
Large Signal Bandwidth (Note 1)		V_o = 20Vp-p	4.0	8.0	–	4.0	8.0	–	kHz
Closed Loop Bandwidth (Note 1)	BW	A_{VCL} = +1.0	0.8	1.3	–	0.8	1.3	–	MHz
Risetime (Note 1)		A_V = +1 V_{IN} = 50mV	–	200	300	–	200	300	nsec
Overshoot (Note 1)			–	5	10	–	5	10	%
The following specifications apply for V_S = ±15V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted									
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.5	1.5	–	1.4	3.0	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{os}	$R_s \leq 5k\Omega$	–	2.0	8.0	–	4.0	10.0	µV/°C
Input Offset Current	I_{os}		–	1.0	5.0	–	2.0	10.0	nA
Average Input Offset Current Drift (Note 1)	TCI_{os}		–	7.5	75	–	15	150	pA/°C
Input Bias Current	I_B		–	30	100	–	40	125	nA
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_o = ±10V	50	100	–	25	60	–	V/mV
Maximum Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V
Note 1: Parameter is not 100% tested. 90% of all units meet these specifications.									

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ELECTRICAL CHARACTERISTICS (Each Amplifier)			OP-04E OP-14E			OP-04C OP-14C			
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.3	0.75	–	1.0	2.0	mV
Input Offset Current	I_{os}		–	0.5	2.0	–	1.0	5.0	nA
Input Bias Current	I_B		–	18	50	–	20	75	nA
Input Resistance-Differential Mode	R_{in}		3.8	7.5	–	2.3	7.0	–	MΩ
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	90	110	–	90	100	–	dB
Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_o = ±10V	100	250	–	50	200	–	V/mV
Power Consumption	P_d	V_o = 0V	–	40	60	–	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.65	–	–	0.65	–	μV p-p
Input Noise Voltage Density	e_n	f_o = 10Hz f_o = 100Hz f_o = 1000Hz	– – –	25 22 21	– – –	– – –	25 22 21	– – –	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	12.8	–	–	12.8	–	pA p-p
Channel Separation	CS		100	–	–	100	–	–	dB
Input Noise Current Density	i_n	f_o = 10Hz f_o = 100Hz f_o = 1000Hz	– – –	1.4 0.7 0.4	– – –	– – –	1.4 0.7 0.4	– – –	pA/√Hz
Slew Rate (Note 1)	SR		0.5	0.7	–	0.5	0.7	–	V/μs
Large Signal Bandwidth (Note 1)		V_o = 20Vp-p	4.0	8.0	–	4.0	8.0	–	kHz
Closed Loop Bandwidth (Note 1)	BW	A_{VCL} = +1.0	0.8	1.3	–	0.8	1.3	–	MHz
Risetime (Note 1)		A_V = +1 V_{IN} = 50mV	–	200	300	–	200	300	nsec
Overshoot (Note 1)			–	5	10	–	5	10	%
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.									
Input Offset Voltage	V_{os}	$R_s \leq 50k\Omega$	–	0.4	1.5	–	1.2	3.0	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{os}	$R_s \leq 5k\Omega$	–	2.0	8.0	–	4.0	10.0	μV/°C
Input Offset Current	I_{os}		–	0.7	4.0	–	1.4	10.0	nA
Average Input Offset Current Drift (Note 1)	TCI_{os}		–	7.5	120	–	15	250	pA/°C
Input Bias Current	I_B		–	22	50	–	25	125	nA
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±5 to ±20V $R_s \leq 50k\Omega$	84	110	–	84	100	–	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_o = ±10V	50	200	–	25	150	–	V/mV
Maximum Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	V
Note 1: Parameter is not 100% tested. 90% of all units meet these specifications.									

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IMPROVED PM725/SSS725

OP-05

INSTRUMENTATION OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The OP-05 Series of monolithic Instrumentation Operational Amplifiers combines superlative performance in low signal level applications with the flexibility and ease of application of a fully protected, internally compensated op amp. OP-05 characteristics include low offset voltage and bias current and high gain, input impedance, CMRR and PSRR.

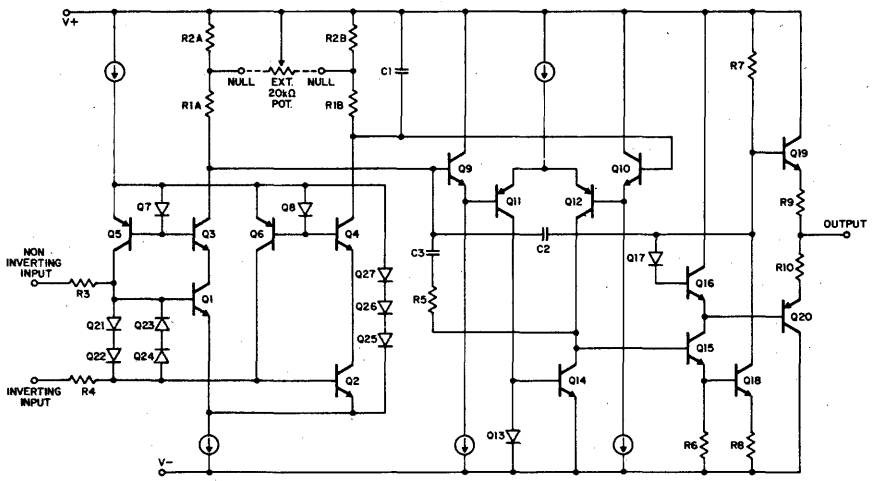
The OP-05 is a direct replacement in 725, 108A and unnulled 741 sockets allowing instant system performance improvement without redesign.

The OP-05 is an excellent choice for a wide variety of applications including strain gauge and thermocouple bridges, high gain active filters, buffers, integrators, and sample and hold amplifiers. For dual matched versions, refer to the OP-10 data sheet.

FEATURES

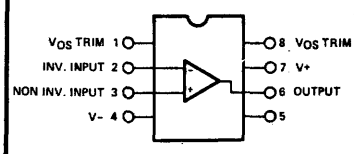
- Low Noise . . . . . 0.6μV p-p Max., 0.1 to 10Hz
- Low Drift vs. Temp . . . . . 0.5μV/°C Max
- Low Drift vs. Time . . . . . 0.3μV/Month Typ
- Low Bias Current . . . . . 2.0nA Max
- Low V_{OS} . . . . . 0.15mV Max
- High CMRR . . . . . 114dB Min
- High PSRR . . . . . 100dB Min
- High Gain . . . . . 300,000 Min
- High R_{in} Diff . . . . . 30MΩ Min
- High R_{in} CM . . . . . 200GΩ Typ
- High Slew Rate . . . . . 0.17 V/μsec Typ
- Internally Compensated . . . . . Stable to 500pF Load
- Easy to Use . . . . . Fully Protected
- Easy Offset Nulling . . . . . Single 20kΩ Pot
- Fits 725, 108A and 741 Sockets

SIMPLIFIED SCHEMATIC

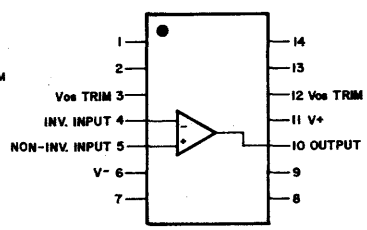


PIN CONNECTIONS AND ORDERING INFORMATION

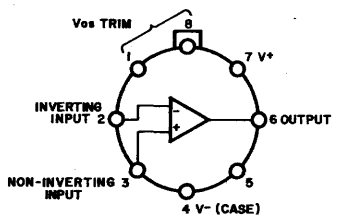
TOP VIEW



EPOXY B MINI-DIP (P-Suffix)
ORDER: OP-05CP



14 PIN DIP (Y-Suffix)
ORDER: OP-05AY OP-05EY
OP-05Y OP-05CY



TO-99 (J-Suffix)
ORDER: OP-05AJ OP-05EJ
OP-05J OP-05CJ

Military Temperature Range Devices With MIL-STD-883A Class B Processing:
ORDER: OP05-883-AJ
OP05-883-AY
OP05-883-J
OP05-883-Y

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V	Storage Temperature Range	-65°C to +150°C
Internal Power Dissipation (Note 1)	500mW	Operating Temperature Range	
Differential Input Voltage	±30V	OP-05A, OP-05	-55°C to +125°C
Input Voltage (Note 2)	±22V	OP-05E, OP-05C	0°C to +70°C
Output Short Circuit Duration	Indefinite	Lead Temperature Range (Soldering, 60 sec)	300°C

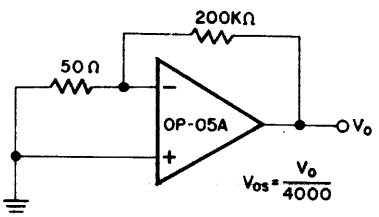
NOTES:

Note 1: Maximum package power dissipation vs. ambient temperature.

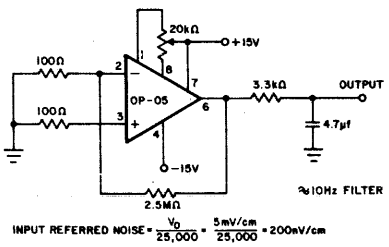
Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
Dual-in-Line (Y)	100°C	10.0mW/°C
Flat Pack (L)	62°C	5.7mW/°C

Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

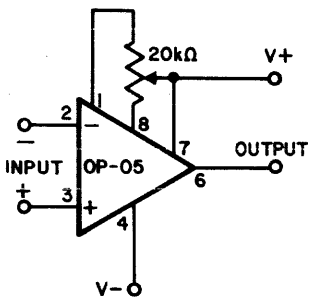
OFFSET VOLTAGE TEST CIRCUIT



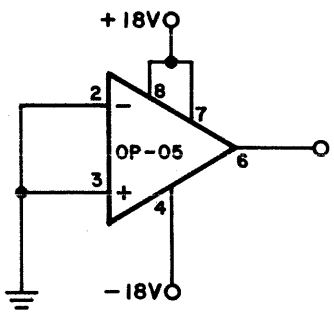
LOW FREQUENCY NOISE TEST CIRCUIT



OFFSET NULLING CIRCUIT



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

OP-05 Series devices may be fitted directly to 725 and 108/108A Series sockets with or without removal of external compensation components. Additionally, OP-05 may be fitted to unnulled 741 Series sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-05 operation. The OP-05 provides stable operation with load capacitances up to 500pF and ±10V swings; larger capacitances should be decoupled with a 50Ω decoupling resistor. The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

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ELECTRICAL CHARACTERISTICS			OP-05A			OP-05			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}		—	0.07	0.15	—	0.2	0.5	mV
Long Term Input Offset Voltage Stability	V_{os}/Time	(Note 1)	—	0.2	1.0	—	0.2	1.0	µV/Mo
Input Offset Current	I_{os}		—	.7	2.0	—	1.0	2.8	nA
Input Bias Current	I_B		—	±.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.35	0.6	µV p-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 2)	—	10.3	18.0	—	10.3	18.0	nV/√Hz
		f_o = 100Hz (Note 2)	—	10.0	13.0	—	10.0	13.0	
		f_o = 1000Hz (Note 2)	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 2)	—	14	30	—	14	30	pA p-p
Input Noise Current Density	i_n	fo = 10Hz (Note 2)	—	0.32	0.80	—	0.32	0.80	pA/√Hz
		fo = 100Hz (Note 2)	—	0.14	0.23	—	0.14	0.23	
		fo = 1000Hz (Note 2)	—	0.12	0.17	—	0.12	0.17	
Input Resistance - Differential Mode	R_{in}		30	80	—	20	60	—	MΩ
Input Resistance - Common Mode	R_{inCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	CMVR		±13.5	±14.0	—	±13.5	±14.0	—	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	114	126	—	114	126	—	dB
Power Supply Rejection Ratio	PSRR	V_s = ±3V to ±18V	100	110	—	100	110	—	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$, V_o = ±10V	300	500	—	200	500	—	V/mV
		$R_L \geq 500\Omega$, V_o = ±.5V, V_s = ±3V	150	500	—	150	500	—	
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	±10.5	±12.0	—	
Slewing Rate	SR	$R_L \geq 2k\Omega$	—	0.17	—	—	0.17	—	V/µsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0	—	0.6	—	—	0.6	—	MHz
Open Loop Output Resistance	R_o	V_o = O, I_o = O	—	60	—	—	60	—	Ω
Power Consumption	Pd		—	90	120	—	90	120	mW
		V_s = ±3V	—	4	6	—	4	6	
Offset Adjustment Range		R_p = 20kΩ	—	4	—	—	4	—	mV
The following specifications apply for V_S = ±15V, -55°C ≤ T_A ≤ +125°C, unless otherwise noted.									
Input Offset Voltage	V_{os}		—	0.10	0.24	—	0.3	0.7	mV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{os}		—	0.3	0.9	—	0.7	2.0	µV/°C
With External Trim	TCV_{osn}	R_p = 20kΩ	—	0.2	0.5	—	0.3	1.0	µV/°C
Input Offset Current	I_{os}		—	1.0	4.0	—	1.8	5.6	nA
Average Input Offset Current Drift	TCI_{os}		—	5	25	—	8	50	pA/°C
Input Bias Current	I_B		—	±1.0	±4.0	—	±2.0	±6.0	nA
Average Input Bias Current Drift	TCI_B		—	8	25	—	13	50	pA/°C
Input Voltage Range	CMVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	110	123	—	110	123	—	dB
Power Supply Rejection Ratio	PSRR	V_s = ±3V to ±18V	94	106	—	94	106	—	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$, V_o = ±10V	200	400	—	150	400	—	V/mV
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 2k\Omega$	±12.0	±12.6	—	±12.0	±12.6	—	V

NOTE 1: Long Term Input Offset Voltage Stability refers to the averaged trend line of Vos vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days are typically 2.5µV – refer to typical performance curve on Page 5. Parameter is not 100% tested; 90% of units meet this specification.

NOTE 2: Parameter is not 100% tested; 90% of units meet this specification.

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ELECTRICAL CHARACTERISTICS			OP-05E			OP-05C			

These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage	V_{os}		—	0.2	0.5	—	0.3	1.3	mV
Long Term Input Offset Voltage Stability	V_{os}/Time	(Note 1)	—	0.3	1.5	—	0.4	2.0	μV/Mo
Input Offset Current	I_{os}		—	1.2	3.8	—	1.8	6.0	nA
Input Bias Current	I_B		—	±1.2	±4.0	—	±1.8	±7.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.38	0.65	μV p-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 2) f_o = 100Hz (Note 2) f_o = 1000Hz (Note 2)	— — —	10.3 10.0 9.6	18.0 13.0 11.0	— — —	10.5 10.2 9.8	20.0 13.5 11.5	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 2)	—	14	30	—	15	35	pAp-p
Input Noise Current Density	i_n	f_o = 10Hz (Note 2) f_o = 100Hz (Note 2) f_o = 1000Hz (Note 2)	— — —	0.32 0.14 0.12	0.80 0.23 0.17	— — —	0.35 0.15 0.13	0.90 0.27 0.18	pA/√Hz
Input Resistance – Differential Mode	R_{in}		15	50	—	8	33	—	MΩ
Input Resistance – Common Mode	R_{inCM}		—	160	—	—	120	—	GΩ
Input Voltage Range	CMVR		±13.5	±14.0	—	±13.0	±14.0	—	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	110	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	94	107	—	90	104	—	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$, V_o = ±10V $R_L \geq 500\Omega$, V_o = ±.5V V_S = ±3V	200 150	500 500	— —	120 100	400 400	— —	V/mV
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	— — —	±12.0 ±11.5 —	±13.0 ±12.8 ±12.0	— — —	V
Slewing Rate	SR	$R_L \geq 2k\Omega$	–	0.17	—	—	0.17	—	V/μsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0	—	0.6	—	—	0.6	—	MHz
Open Loop Output Resistance	R_o	V_o = 0, I_o = 0	—	60	—	—	60	—	Ω
Power Consumption	P_d	 V_S = ±3V	— —	90 4	120 6	— —	95 4	150 8	mW
Offset Adjustment Range		R_p = 20kΩ	—	4	—	—	4	—	mV

The following specifications apply for $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

Input Offset Voltage	V_{os}		—	0.25	0.6	—	0.35	1.6	mV
Average Input Offset Voltage Drift Without External Trim With External Trim	 TCV_{os} TCV_{osn}	 (Note 2) R_p = 20kΩ (Note 3)	 — —	 0.7 0.2	 2.0 0.6	 — —	 1.2 0.4	 4.5 1.5 (Note 2)	μV/°C
Input Offset Current	I_{os}		—	1.4	5.3	—	2.0	8.0	nA
Average Input Offset Current Drift	TCI_{os}	(Note 2)	—	8	35	—	12	50	pA/°C
Input Bias Current	I_B		—	±1.5	±5.5	—	±2.2	±9.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	35	—	18	50	pA/°C
Input Voltage Range	CMVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	107	123	—	97	120	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	90	104	—	86	100	—	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$, V_o = ±10V	180	450	—	100	400	—	V/mV
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 2k\Omega$,	±12.0	±12.6	—	±11.0	±12.6	—	V

NOTE 1: Long Term Input Offset Voltage Stability refers to the averaged trend line of Vos vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days are typically 2.5μV – refer to typical performance curve on Page 5. Parameter is not 100% tested; 90% of units meet this specification.

NOTE 2: Parameter is not 100% tested; 90% of units meet this specification.

NOTE 3: Devices are tested in oil bath environment at 75°C. Adjustments are made for heat sink capabilities of oil.

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OP-07

ULTRA-LOW OFFSET VOLTAGE OP AMP

GENERAL DESCRIPTION

The OP-07 Series represents a breakthrough in monolithic operational amplifier performance—Vos of 10μV, TC Vos of 0.2μV/°C and long term stability of 0.2μV/month are achieved by a low noise, chopper-less bipolar input transistor amplifier circuit. Complete elimination of external components for offset nulling, frequency compensation and device protection permits extreme miniaturization and optimization of system Mean-Time-Between-Failure Rates in high performance aerospace/defense and industrial applications. Excellent device interchangeability provides reduced system assembly time and eliminates field recalibrations.

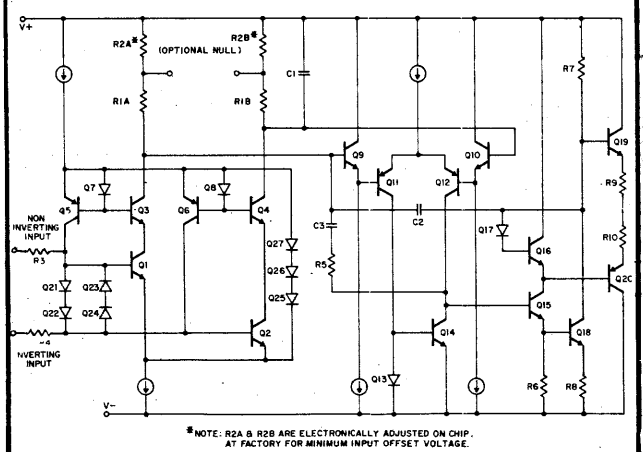
True differential inputs with wide input voltage range and outstanding common mode rejection provide maximum flexibility and performance in high noise environments and non-inverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range.

Low cost, high volume production of OP-07 is achieved by electronic adjustment of an on-chip offset trimming network during initial factory testing. The OP-07 provides unparalleled performance for low noise, high accuracy amplification of very low level signals in transducer applications. Other applications include use in stable integrators, precision summing amplifiers for analog computation and test equipment and in ultra-precise voltage threshold detectors and comparators. The OP-07 is recommended as a replacement for modular and monolithic chopper-stabilized amplifiers where reductions in cost, noise, size and power consumption are required. Devices are available in chip form for use in hybrid circuitry. The OP-07 is a direct replacement for 725, 108A/308A, and OP-05 amplifiers; 741-types may be directly replaced by removing the 741's nulling potentiometer.

FEATURES

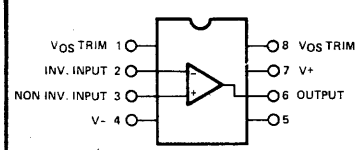
- Ultra-Low Vos . . . . . 10 μV
- Ultra-Low Vos Drift . . . . . 0.2 μV/°C
- Ultra-Stable vs Time . . . . . 0.2 μV/Month
- Ultra-Low Noise . . . . . 0.35 μVp-p
- No External Components Required
- Replaces Chopper amps at Lower Cost
- Single Chip Monolithic Construction
- High Common Mode Input Range . . . . . ±14.0V
- Wide Supply Voltage Range . . . . . ±3V to ±18V
- Fits 725, 108A/308A, 741,AD510 Sockets

SIMPLIFIED SCHEMATIC



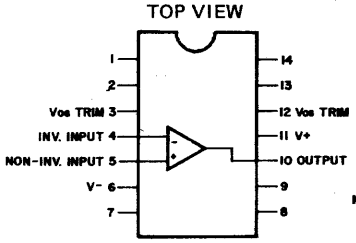
*NOTE: R2A & R2B ARE ELECTRONICALLY ADJUSTED ON CHIP AT FACTORY FOR MINIMUM INPUT OFFSET VOLTAGE.

PIN CONNECTIONS AND ORDERING INFORMATION

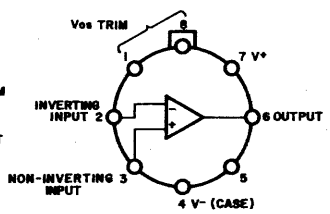


EPOXY B MINI-DIP (P-Suffix)
ORDER: OP-07CP

TOP VIEW



14 PIN DIP (Y-Suffix)
ORDER: OP-07AY OP-07CY
OP-07Y
OP-07EY



TO-99 (J-Suffix)
ORDER: OP-07AJ OP-07CJ
OP-07J OP-07DJ
OP-07EJ

Military Temperature Range Devices with MIL-STD-883A Class B Processing

ORDER: OP07-883-AJ
OP07-883-AY
OP07-883-J
OP07-883-Y

ELECTRICAL CHARACTERISTICS			OP-07A			OP-07			
These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	(Note 1)	—	10	25	—	30	75	μV
Long Term Input Offset Voltage Stability	V_{os}/Time	(Note 2)	—	0.2	1.0	—	0.2	1.0	μV/Mo
Input Offset Current	I_{os}		—	0.3	2.0	—	0.4	2.8	nA
Input Bias Current	I_B		—	±.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.35	0.6	μV p-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 3) f_o = 100Hz (Note 3) f_o = 1000Hz (Note 3)	— — —	10.3 10.0 9.6	18.0 13.0 11.0	— — —	10.3 10.0 9.6	18.0 13.0 11.0	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	14	30	pA p-p
Input Noise Current Density	i_n	fo = 10Hz (Note 3) fo = 100Hz (Note 3) fo = 1000Hz (Note 3)	— — —	0.32 0.14 0.12	0.80 0.23 0.17	— — —	0.32 0.14 0.12	0.80 0.23 0.17	pA/√Hz
Input Resistance – Differential Mode	R_{in}		30	80	—	20	60	—	MΩ
Input Resistance - Common Mode	R_{inCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	CMVR		±13.0	± 14.0	—	±13.0	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$V_{cM} = \pm$CMVR	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSRR	$V_s = \pm 3V$ to $\pm 18V$	100	110	—	100	110	—	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$, $V_o = \pm 10V$ $R_L \geq 500\Omega$, $V_o = \pm .5V$ $V_s = \pm 3V$	300 150	500 500	— —	200 150	500 500	— —	V/mV
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	± 12.5 ± 12.0 ± 10.5	± 13.0 ± 12.8 ± 12.0	— — —	± 12.5 ±12.0 ± 10.5	± 13.0 ±12.8 ± 12.0	— — —	V
Slewing Rate	SR	$R_L \geq 2k\Omega$	—	0.17	—	—	0.17	—	V/μsec
Closed Loop Bandwidth	BW	$A_{VCL} = +1.0$	—	0.6	—	—	0.6	—	MHz
Open Loop Output Resistance	R_o	$V_o = O$, $I_o = O$	—	60	—	—	60	—	Ω
Power Consumption	Pd	 $V_s = \pm 3V$	— —	75 4	120 6	— —	75 4	120 6	mW
Offset Adjustment Range		$R_p = 20k\Omega$	—	±4	—	—	±4	—	mV
The following specifications apply for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.									
Input Offset Voltage	V_{os}	(Note 1)	—	25	60	—	60	200	μV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{os}		—	0.2	0.6	—	0.3	1.3	μV/°C
With External Trim	TCV_{osn}	$R_p = 20k\Omega$	—	0.2	0.6	—	0.3	1.3	μV/°C
Input Offset Current	I_{os}		—	0.8	4.0	—	1.2	5.6	nA
Average Input Offset Current Drift	TCI_{os}		—	5	25	—	8	50	pA/°C
Input Bias Current	I_B		—	±1.0	±4.0	—	±2.0	±6.0	nA
Average Input Bias Current Drift	TCI_B		—	8	25	—	13	50	pA/°C
Input Voltage Range	CMVR		± 13.0	± 13.5	—	± 13.0	± 13.5	—	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm$ CMVR	106	123	—	106	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_s = \pm 3V$ to $\pm 18V$	94	106	—	94	106	—	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	200	400	—	150	400	—	V/mV
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 2k\Omega$	± 12.0	± 12.6	—	± 12.0	±12.6	—	V

NOTE 1: Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, OP-07A offset voltage is measured five minutes after power supply application at 25°C, -55°C and +125°C.

NOTE 2: Long Term Input Offset Voltage Stability refers to the averaged trend line of Vos vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days are typically 2.5μV – refer to typical performance curve on Page 5. Parameter is not 100% tested; 90% of units meet this specification.

NOTE 3: Parameter is not 100% tested; 90% of units meet this specification.

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ELECTRICAL CHARACTERISTICS			OP-07E			OP-07C			OP-07D			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.												
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	(Note 1)	–	30	75	–	60	150	–	60	150	µV
Long Term V_{os} Stability	V_{os}/Time	(Note 2)	–	0.3	1.5	–	0.4	2.0	–	0.5	3.0	µV/Mo
Input Offset Current	I_{os}		–	0.5	3.8	–	0.8	6.0	–	0.8	6.0	nA
Input Bias Current	I_B		–	±1.2	±4.0	–	±1.8	±7.0	–	±2.0	±12	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	–	0.35	0.6	–	0.38	0.65	–	0.38	0.65	µV p-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 3)	–	10.3	18.0	–	10.5	20.0	–	10.5	20.0	nV/√Hz
		f_o = 100Hz (Note 3)	–	10.0	13.0	–	10.2	13.5	–	10.2	13.5	
		f_o = 1000Hz (Note 3)	–	9.6	11.0	–	9.8	11.5	–	9.8	11.5	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)	–	14	30	–	15	35	–	15	35	pAp-p
Input Noise Current Density	i_n	f_o = 10Hz (Note 3)	–	0.32	0.80	–	0.35	0.90	–	0.35	0.90	pA/√Hz
		f_o = 100Hz (Note 3)	–	0.14	0.23	–	0.15	0.27	–	0.15	0.27	
		f_o = 1000Hz (Note 3)	–	0.12	0.17	–	0.13	0.18	–	0.13	0.18	
Input Resistance – Diff. Mode	R_{in}		15	50	–	8	33	–	7	31	–	MΩ
Input Resistance – Common Mode	R_{inCM}		–	160	–	–	120	–	–	120	–	GΩ
Input Voltage Range	CMVR		±13.0	±14.0	–	±13.0	±14.0	–	±13.0	±14.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	106	123	–	100	120	–	94	110	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±3V to ±18V	94	107	–	90	104	–	90	104	–	dB
Large Signal Voltage Gain	A_{vo}	R_L ≥ 2kΩ, V_o = ±10V	200	500	–	120	400	–	120	400	–	V/mV
		R_L ≥ 500Ω, V_o = ±.5V, V_s = ±3V	150	500	–	100	400	–	–	–	–	
Maximum Output Voltage Swing	V_{oM}	R_L ≥ 10kΩ	±12.5	±13.0	–	±12.0	±13.0	–	±12.0	±13.0	–	V
		R_L ≥ 2kΩ	±12.0	±12.8	–	±11.5	±12.8	–	±11.5	±12.8	–	
		R_L ≥ 1kΩ	±10.5	±12.0	–	–	±12.0	–	–	–	–	
Slewing Rate	SR	R_L ≥ 2kΩ	–	0.17	–	–	0.17	–	–	0.17	–	V/µsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0	–	0.6	–	–	0.6	–	–	0.6	–	MHz
Open Loop Output Resistance	R_o	V_o = 0, I_o = 0	–	60	–	–	60	–	–	60	–	Ω
Power Consumption	P_d	V_s = ±3V	–	75	120	–	80	150	–	80	150	mW
			–	4	6	–	4	8	–	4	8	
Offset Adjustment Range		R_p = 20kΩ	–	±4	–	–	±4	–	–	±4	–	mV
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.												
Input Offset Voltage	V_{os}	(Note 1)	–	45	130	–	85	250	–	85	250	µV
Average Input Offset Voltage Drift								(Note 3)			(Note 3)	µV/°C
Without External Trim	TCV_{os}		–	0.3	1.3	–	0.5	1.8	–	0.7	2.5	
With External Trim	TCV_{osn}	R_p = 20kΩ	–	0.3	1.3	–	0.4	1.6 (Note 3)	–	0.7	2.5 (Note 3)	
Input Offset Current	I_{os}		–	0.9	5.3	–	1.6	8.0	–	1.6	8.0	nA
Average Input Offset Current Drift	TCI_{os}	(Note 3)	–	8	35	–	12	50	–	12	50	pA/°C
Input Bias Current	I_B		–	±1.5	±5.5	–	±2.2	±9.0	–	±3.0	±14	nA
Average Input Bias Current Drift	TCI_B	(Note 3)	–	13	35	–	18	50	–	18	50	pA/°C
Input Voltage Range	CMVR		±13.0	±13.5	–	±13.0	±13.5	–	±13.0	±13.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	103	123	–	97	120	–	94	106	–	dB
Power Supply Rejection Ratio	PSRR	V_s = ±3V to ±18V	90	104	–	86	100	–	86	100	–	dB
Large Signal Voltage Gain	A_{vo}	R_L ≥ 2kΩ, V_o = ±10V	180	450	–	100	400	–	100	400	–	V/mV
Maximum Output Voltage Swing	V_{oM}	R_L ≥ 2kΩ	±12.0	±12.6	–	±11.0	±12.6	–	±11.0	±12.6	–	V

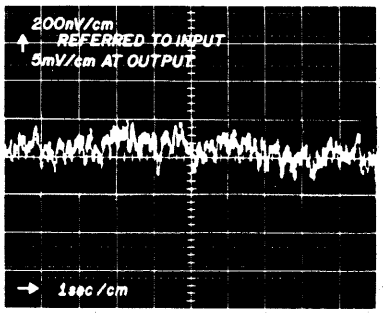
NOTE 1: Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

NOTE 2: Long Term Input Offset Voltage Stability refers to the averaged trend line of Vos vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days are typically 2.5µV – refer to typical performance curve on Page 5. Parameter is not 100% tested; 90% of units meet this specification.

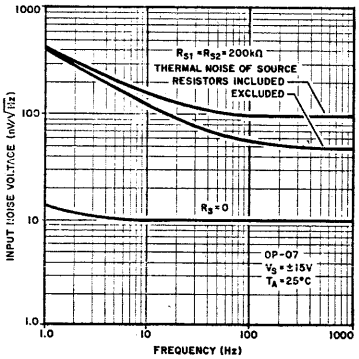
NOTE 3: Parameter is not 100% tested; 90% of units meet this specification.

TYPICAL PERFORMANCE CURVES

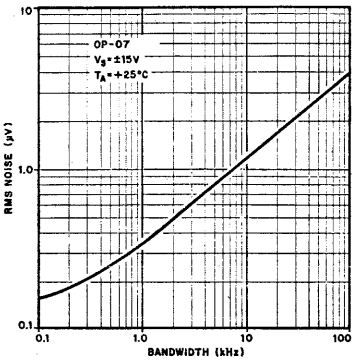
OP-07 LOW FREQUENCY NOISE



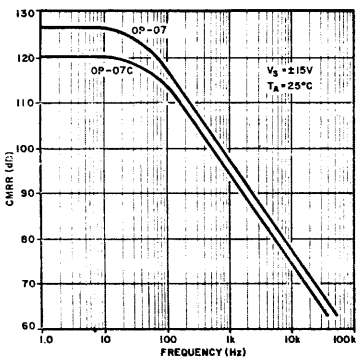
TOTAL INPUT NOISE VOLTAGE VS FREQUENCY



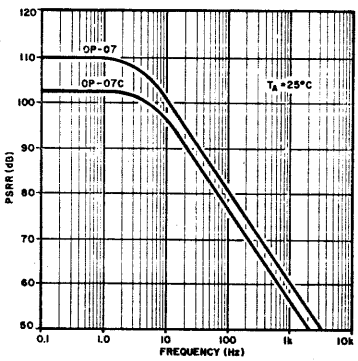
INPUT WIDEBAND NOISE VS BANDWIDTH (.1Hz TO FREQUENCY INDICATED)



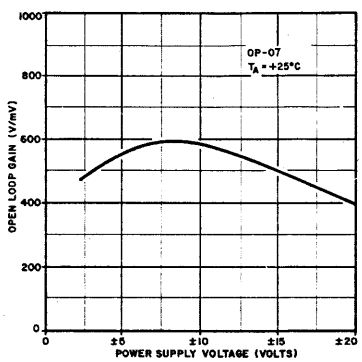
CMRR VS FREQUENCY



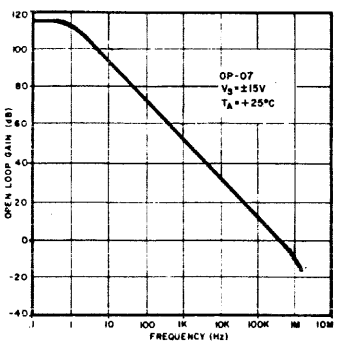
PSRR VS FREQUENCY



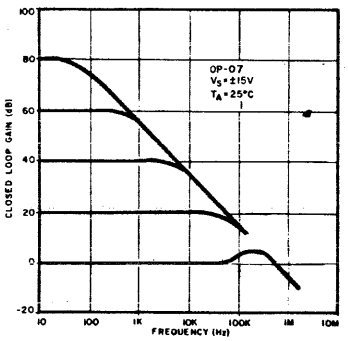
OPEN LOOP GAIN VS POWER SUPPLY VOLTAGE



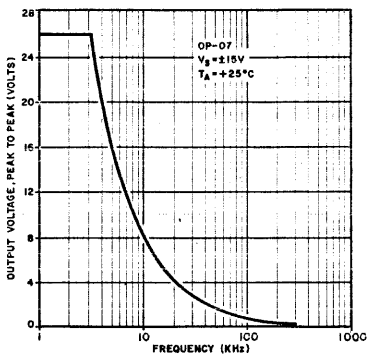
OPEN LOOP FREQUENCY RESPONSE



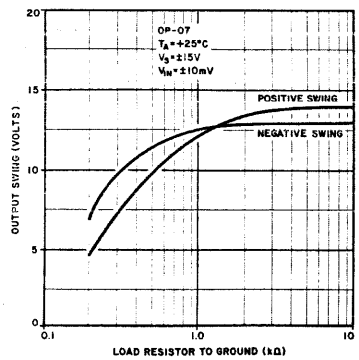
CLOSED LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



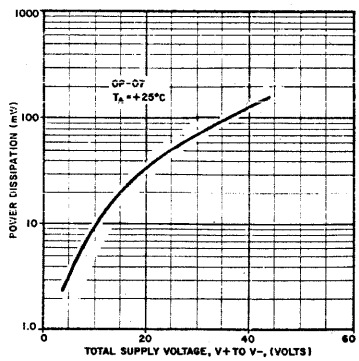
MAXIMUM UNDISTORTED OUTPUT VS FREQUENCY



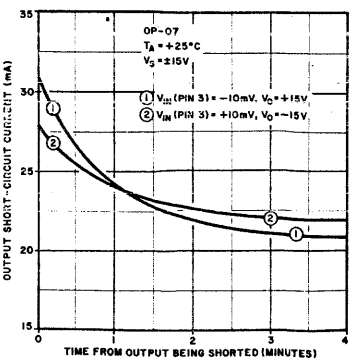
OUTPUT VOLTAGE VS. LOAD RESISTANCE



POWER CONSUMPTION VS POWER SUPPLY



OUTPUT SHORT-CIRCUIT CURRENT VS TIME



©IC MASTER 1978

OP-10

DUAL MATCHED INSTRUMENTATION OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The OP-10 Series of Dual Matched Instrumentation Operational Amplifiers consists of two independent monolithic high performance operational amplifiers in a single 14-pin Dual-in-Line package. For the first time, extremely tight matching of critical parameters is provided between channels of a dual operational amplifier, whereas previous dual op amp designs have made no attempt towards matching.

The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels enables realization of extremely high performance instrumentation amplifier designs without resorting to laborious and expensive selection and matching of discrete amplifiers. The designer is assured of achieving the full performance guaranteed by the specification as the common package eliminates the unavoidable temperature differentials incurred by all designs utilizing separately housed amplifiers.

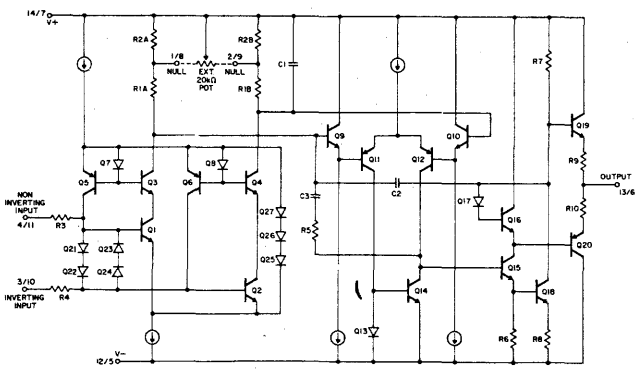
Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common mode and power supply rejection ratios. The individual amplifiers feature extremely low offset voltage, offset voltage drift, low noise voltage, low bias current and are completely compensated and protected.

FEATURES

- Extremely Tight Matching
- Excellent Individual Amplifier Parameters
- Tight Offset Voltage Match . . . . . 0.18mV Max
- Tight Offset Voltage Match vs. Temp. . 0.8 μV/°C Max
- Tight Common Mode Rejection Match . . 114 dB Min
- Tight Power Supply Rejection Match . . . 100 dB Min
- Tight Bias Current Match. . . . . 2.8 nA Max
- Low Noise . . . . . 0.6 μVp-p Max
- Low Bias Current . . . . . 3.0 nA Max
- High Common Mode Input Impedance . . 200GΩ Typ
- High Channel Separation . . . . . 126 dB Min
- Internally Compensated. . . . . Easy to Use
- Compact . . . . . 14 Pin Dip Package

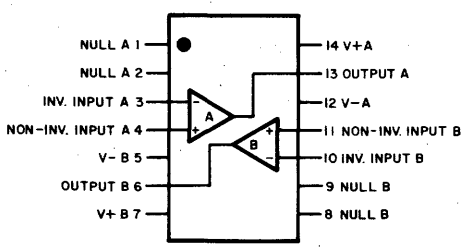
SIMPLIFIED SCHEMATIC

1/2 OP-10)



PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



14 PIN CERAMIC DIP (Y-Suffix)

ORDER: OP-10AY OP-10EY
OP-10Y OP-10CY

NOTE: Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B.

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IMPROVED PM108A

OP-08

PRECISION LOW INPUT CURRENT OP AMP

GENERAL DESCRIPTION

The PMI OP-08 is an improved version of the popular LM108A low power op amp. The OP-08 has a three times lower offset voltage and a two times lower offset voltage drift. The total worst case input offset voltage over −55°C to +125°C for the OP-08 is only 350μV, while the 108A has 900μV to 1000μV for these conditions. In addition the OP-08 drives a 2kΩ load. This is five times the output current capability of the 108A. This excellent performance is achieved by applying PMI's ion-implanted super beta process and on-chip-zener-zap trimming capabilities. For devices with identical specifications plus internal frequency compensation, see the OP-12 data sheet.

FEATURES

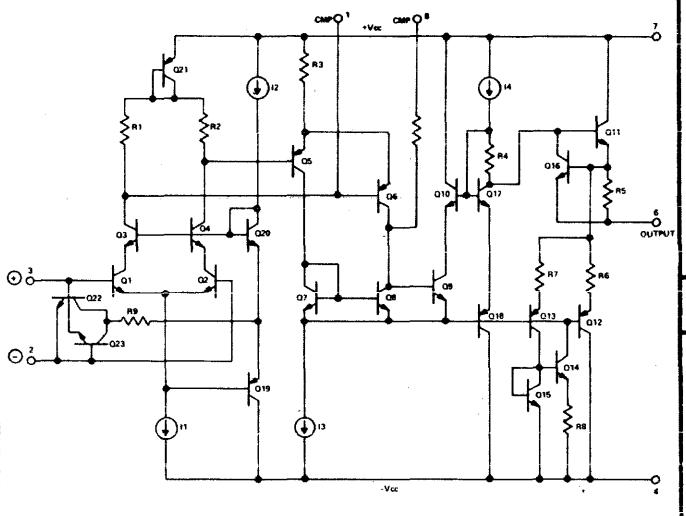
- Low Offset Voltage . . . . . 150μV Max.
- Low Offset Voltage Drift . . . . . 2.5μV/°C Max.
- Five Times PM108A Load Current . . . . . 5 mA Min.

Plus the Outstanding PM108A Features

- Low Offset Current . . . . . 200 pA Max.
- Low Bias Current . . . . . 2.0 nA Max.
- Low Power Consumption . . . . 18 mW max. @ ±15V
- High Common Mode Input Range . . . . ±13.5V Min.
- MIL-STD-883A Class B Processing Available
- Silicon-Nitride Passivation

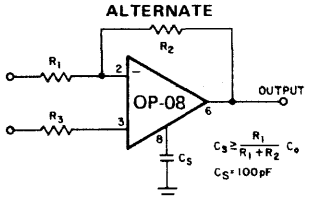
SIMPLIFIED SCHEMATIC

OP-08 SCHEMATIC DIAGRAM



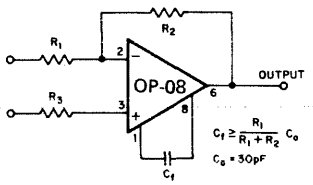
COMPENSATION CIRCUITS

ALTERNATE



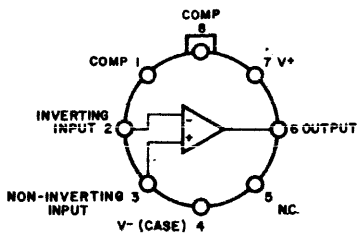
(Improves rejection of power supply noise by a factor of ten)

STANDARD



PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



TO-99 (J-Suffix)

ORDER: OP-08AJ
OP-08BJ
OP-08CJ
OP-08EJ
OP-08FJ
OP-08GJ

Military Temperature Range Devices With MIL-STD-883A Class B Processing

ORDER: OP08-883-AJ
OP08-883-BJ
OP08-883-CJ

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OP-12

PRECISION LOW INPUT CURRENT OP AMP

INTERNALLY COMPENSATED

GENERAL DESCRIPTION

The PMI OP-12 is an improved version of the popular LM108A low power op amp. The OP-12 is internally compensated and its chip dimensions are only 42 x 58 mils. Additionally, the OP-12 has a three times lower offset voltage and a two times lower offset voltage drift. The total worst case input offset voltage over -55°C to +125°C for the OP-12 is only 350μV while the 108A has 900μV to 1000μV for these conditions. In addition the OP-12 drives a 2kΩ load. This is five times the output current capability of the 108A. This excellent performance is achieved by applying PMI's ion-implanted super beta process and on-chip zener-zap trimming capabilities. The internal compensation makes this op amp ideal for hybrid assembly applications

FEATURES

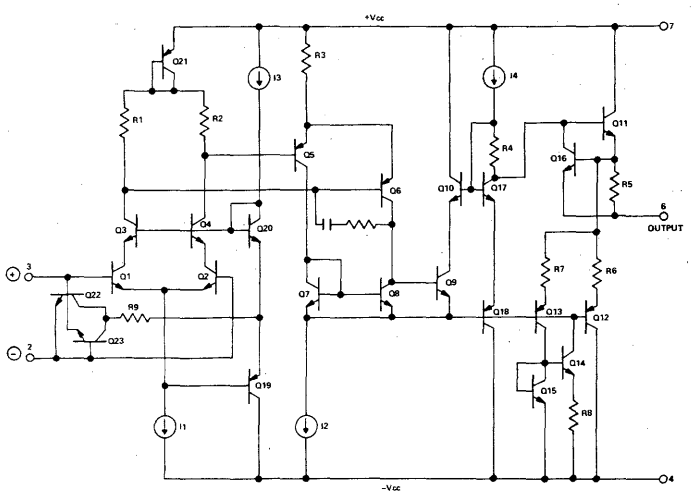
- Low Offset Voltage . . . . . 150μV Max.
- Low Offset Voltage Drift . . . . . 2.5μV/°C Max.
- Five Times PM108A Load Current . . . . . 5 mA Min.
- Internal Frequency Compensation

Plus the Outstanding PM108A Features

- Low Offset Current . . . . . 200 pA Max.
- Low Bias Current . . . . . 2.0 nA Max.
- Low Power Consumption . . . . 18 mW max. @ ±15V
- High Common Mode Input Range . . . . ±13.5V Min.
- MIL-STD-883A Class B Processing Available
- Silicon-Nitride Passivation

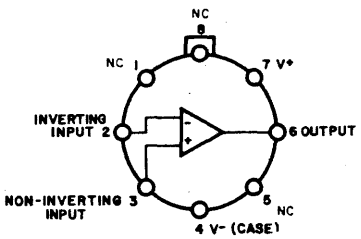
SIMPLIFIED SCHEMATIC

OP-12 SCHEMATIC DIAGRAM



PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



TO-99 (J-Suffix)

ORDER: OP-12AJ
OP-12BJ
OP-12CJ
OP-12EJ
OP-12FJ
OP-12GJ

Military Temperature Range Devices
With MIL-STD-883A Class B Processing

ORDER: OP12-883-AJ
OP12-883-BJ
OP12-883-CJ

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
OP-08A/12A, OP-08B/12B, OP-08C/12C	±20V
OP-08E/12E, OP-08F/12F, OP -08G/12G	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Current (Note 2)	±10mA
Input Voltage (Note 3)	±15V
Output Short Circuit Duration	Indefinite

Operating Temperature Range	
OP-08A/12A, OP-08B/12B, OP-08C/12C	-55°C to +125°C
OP-08E/12E, OP-08F/12F, OP-08G/12G	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range	
(Soldering, 60 sec)	300°C

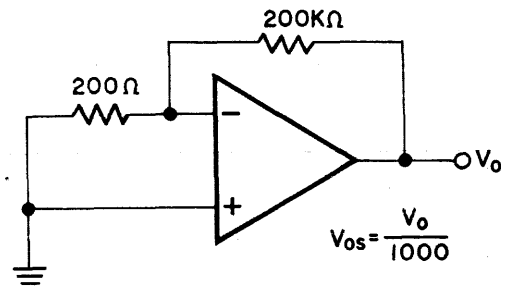
NOTE 1: Maximum package power dissipation vs. ambient temperature:

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1 mW/°C

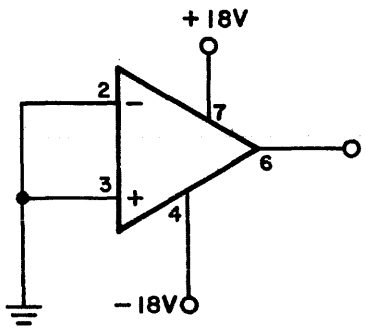
NOTE 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is provided.

NOTE 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

OFFSET VOLTAGE TEST CIRCUIT

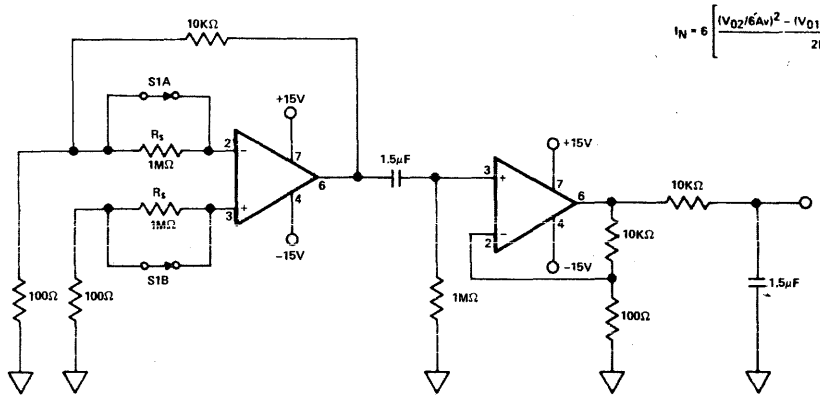


BURN-IN CIRCUIT



LOW FREQUENCY NOISE TEST CIRCUIT (0.1 TO 10 Hz)

$$I_N = 6\left[\frac{(V_{02}/6A_V)^2 - (V_{01}/6A_V)^2 - 2(4kT\Delta f R_s)}{2R_s^2}\right]^{1/2}$$



NOTES: 1. S1 CLOSED MEASURES e_n (V_{01}).
2. S1 OPEN MEASURES e_n AND 1_n (V_{02}). 1_n IS COMPUTED FROM THE TWO MEASUREMENTS
3. SEE NOISE PHOTO OF e_n IN TYPICAL PERFORMANCE CURVES.

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ELECTRICAL CHARACTERISTICS			OP-08A OP-12A			OP-08B OP-12B			OP-08C OP-12C			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.												
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}		–	0.07	0.15	–	0.18	0.30	–	0.25	1.0	mV
Input Offset Current	I_{os}		–	0.05	0.20	–	0.05	0.20	–	0.08	0.50	nA
Input Bias Current	I_B		–	0.80	2.0	–	0.80	2.0	–	1.0	5.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.9	–	–	0.9	–	–	0.9	–	μV p-p
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	22 21 20	– – –	– – –	22 21 20	– – –	– – –	22 21 20	– – –	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	3	–	–	3	–	–	3	–	pA p-p
Input Noise Current Density	i_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	0.15 0.14 0.13	– – –	– – –	0.15 0.14 0.13	– – –	– – –	0.15 0.14 0.13	– – –	pA/√Hz
Input Resistance — Differential Mode	R_{in}		26	70	–	26	70	–	10	50	–	MΩ
Input Voltage Range	CMVR		±13.5	±14.0	–	±13.5	±14.0	–	±13.5	±14.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	104	120	–	104	120	–	84	116	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±15V	104	120	–	104	120	–	84	116	–	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 10K\Omega$, V_O = ±10V $R_L \geq 2K\Omega$, V_O = ±10V	80 50	300 150	– –	80 50	300 150	– –	40 –	250 100	– –	V/mV
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 10K\Omega$ $R_L \geq 2K\Omega$	±13.0 ±10.0	±14.0 ±12.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	V
Slewing Rate	SR	$R_L \geq 2K\Omega$	–	0.12	–	–	0.12	–	–	0.12	–	V/μsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0	–	0.80	–	–	0.80	–	–	0.80	–	MHz
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0	–	200	–	–	200	–	–	200	–	Ω
Power Consumption	Pd	V_S = ± 15V V_S = ±5V	– –	9 3	18 6	– –	9 3	18 6	– –	12 4	24 8	mW
The following specifications apply for V_S = ±15V, –55°C ≤ T_A ≤ +125°C, unless otherwise noted.												
Input Offset Voltage	V_{os}		–	0.12	0.35	–	0.28	0.60	–	0.40	2.0	mV
Average Input Offset Voltage Drift	TCV_{os}		–	0.50	2.5	–	1.0	3.5	–	1.5	10	μV/°C
Input Offset Current	I_{os}		–	0.12	0.40	–	0.12	0.40	–	0.18	1.0	nA
Average Input Offset Current Drift	TCI_{os}		–	0.50	2.5	–	0.50	2.5	–	1.0	5.0	pA/°C
Input Bias Current	I_B		–	1.2	3.0	–	1.2	3.0	–	1.8	10	nA
Input Voltage Range	CMVR		±13.5	±14.0	–	±13.5	±14.0	–	±13.5	±14.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	100	110	–	100	110	–	80	106	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±15V	100	110	–	100	110	–	80	106	–	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 5K\Omega$, V_O = ±10V	40	120	–	40	120	–	15	80	–	V/mV
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 10K\Omega$ $R_L \geq 5K\Omega$	±13.0 ±10.0	±14.0 ±13.0	– –	±13.0 ±10.0	±14.0 ±13.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	V
Power Consumption	Pd		–	9	18	–	9	18	–	15	24	mW

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ELECTRICAL CHARACTERISTICS			OP-08E OP-12E			OP-08F OP-12F			OP-08G OP-12G			

These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage	V_{os}		–	0.07	0.15	–	0.18	0.30	–	0.25	1.0	mV
Input Offset Current	I_{os}		–	0.05	0.20	–	0.07	0.40	–	0.08	0.50	nA
Input Bias Current	I_B		–	0.80	2.0	–	0.90	4.0	–	1.0	5.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.9	–	–	0.9	–	–	0.9	–	μV p-p
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	22 21 20	– – –	– – –	22 21 20	– – –	– – –	22 21 20	– – –	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	3	–	–	3	–	–	3	–	pA p-p
Input Noise Current Density	i_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	0.15 0.14 0.13	– – –	– – –	0.15 0.14 0.13	– – –	– – –	0.15 0.14 0.13	– – –	pA/√Hz
Input Resistance – Differential Mode	R_{in}		26	70	–	13	60	–	10	50	–	MΩ
Input Voltage Range	CMVR		±13.5	±14.0	–	±13.5	±14.0	–	±13.5	±14.0	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	104	120	–	102	120	–	84	116	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±15V	104	120	–	102	120	–	84	116	–	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 10K\Omega$, V_O = ±10V $R_L \geq 2K\Omega$, V_O = ±10V	80 50	300 150	– –	80 30	300 120	– –	40 –	250 100	– –	V/mV
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 10K\Omega$ $R_L \geq 2K\Omega$	±13.0 ±10.0	±14.0 ±12.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	V
Slewing Rate	SR	$R_L \geq 2K\Omega$	–	0.12	–	–	0.12	–	–	0.12	–	V/μsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0	–	0.80	–	–	0.80	–	–	0.80	–	MHz
Open Loop Output Resistance	R_O	V_O = O, I_O = O	–	200	–	–	200	–	–	200	–	Ω
Power Consumption	Pd	V_S = ±15V V_S = ±5V	– –	9 3	18 6	– –	9 3	18 6	– –	12 4	24 8	mW

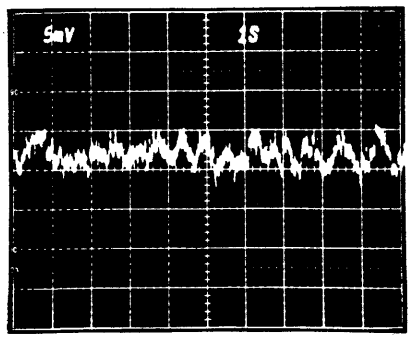
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤+70°C, unless otherwise noted.

Input Offset Voltage	V_{os}		–	0.10	0.26	–	0.23	0.45	–	0.32	1.4	mV
Average Input Offset Voltage Drift	TCV_{os}		–	0.50	2.5	–	1.0	3.5	–	1.5	10	μV/°C
Input Offset Current	I_{os}		–	0.08	0.30	–	0.11	0.60	–	0.12	0.70	nA
Average Input Offset Current Drift	TCI_{os}		–	0.50	2.5	–	1.0	5.0	–	1.0	5.0	pA/°C
Input Bias Current	I_B		–	1.0	2.6	–	1.2	5.2	–	1.4	6.5	nA
Input Voltage Range	CMVR		±13.5	±14.0	–	±13.5	±14.0	–	±13.5	–	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	100	116	–	100	116	–	80	112	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±15V	100	116	–	100	116	–	80	112	–	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2K\Omega$, V_O = ±10V $R_L \geq 10K\Omega$, V_O = ±10V	25 60	100 200	– –	15 60	100 200	– –	– 25	80 150	– –	V/mV
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 10K\Omega$ $R_L \geq 2K\Omega$	±13.0 ±10.0	±14.0 ±12.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	±13.0 ±10.0	±14.0 ±12.0	– –	V
Power Consumption	P_D		–	9	18	–	9	18	–	15	24	mW

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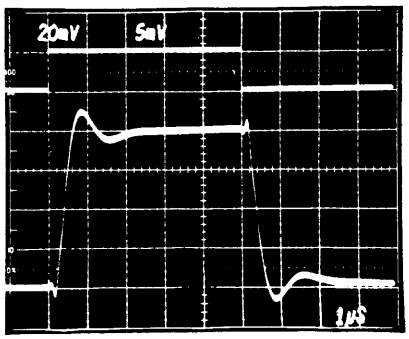
TYPICAL PERFORMANCE CURVES

LOW FREQUENCY NOISE

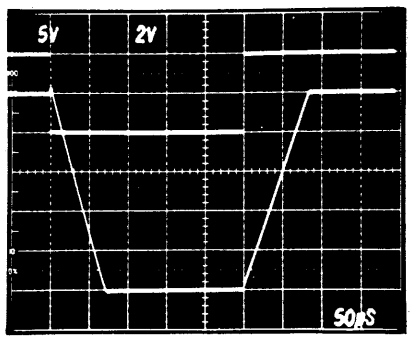


R_S = 0, BW = 0.1Hz to 10Hz
5 mV/div AT OUTPUT
0.5 μV/div REFERRED TO INPUT

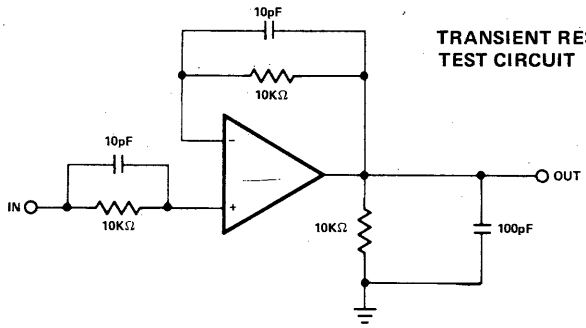
SMALL SIGNAL TRANSIENT RESPONSE



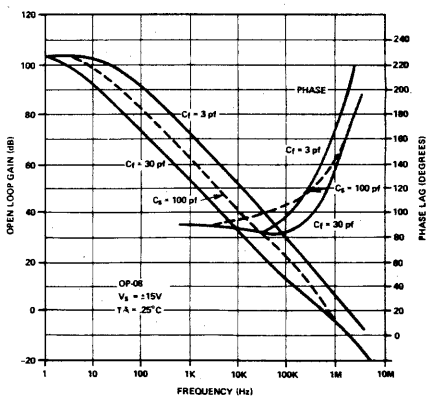
LARGE SIGNAL TRANSIENT RESPONSE



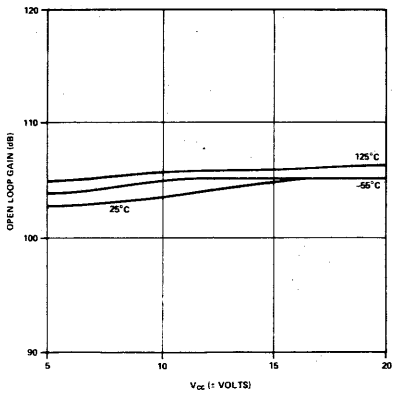
TRANSIENT RESPONSE TEST CIRCUIT



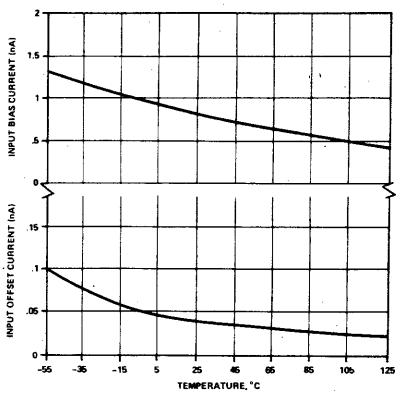
OPEN LOOP GAIN (A_{VO}) AND PHASE VS. FREQUENCY



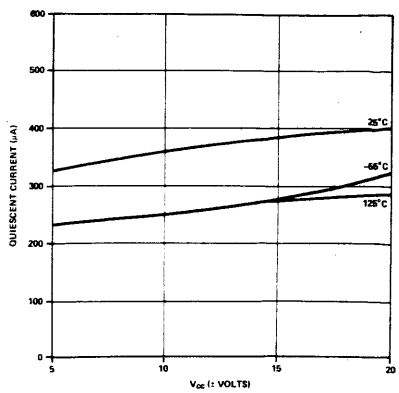
OPEN LOOP GAIN (Avo) VS. SUPPLY VOLTAGE (Vcc) WITH TEMPERATURE AS A PARAMETER



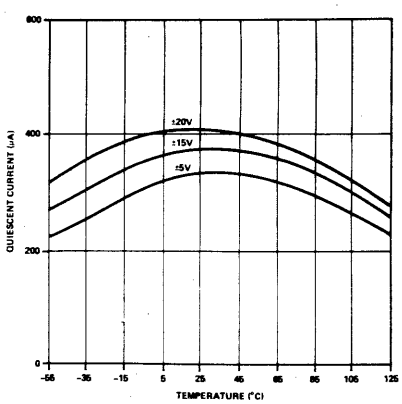
INPUT BIAS CURRENT AND INPUT OFFSET CURRENT VS. TEMPERATURE



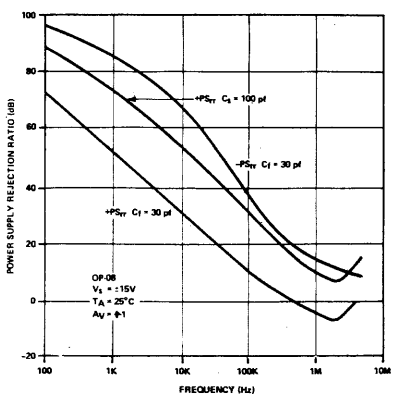
QUIESCENT CURRENT (ISY) VS. SUPPLY VOLTAGE WITH TEMPERATURE AS A PARAMETER



QUIESCENT CURRENT (ISY) VS. TEMPERATURE WITH SUPPLY VOLTAGE AS A PARAMETER



POWER SUPPLY REJECTION RATIO (PSRR) VS. FREQUENCY



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IMPROVED PM4136

OP-09

QUAD MATCHED 741-TYPE OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The OP-09 provides four matched 741-type operational amplifiers in a single 14-pin DIP package. The OP-09 is pin compatible with the RM4136 and RC4136 amplifiers. The amplifiers are matched for common mode rejection ratio and offset voltage. These parameters are very important in the design of instrumentation amplifiers. In addition the amplifier is designed to have equal positive-going and negative-going slew rates. This is a very important consideration for good audio system performance.

Each of the four amplifiers has the proven OP-02 advantages of low noise, low drift and excellent long term stability. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process eliminates "popcorn noise" and provides maximum reliability and long term stability of parameters for lowest overall system operating cost.

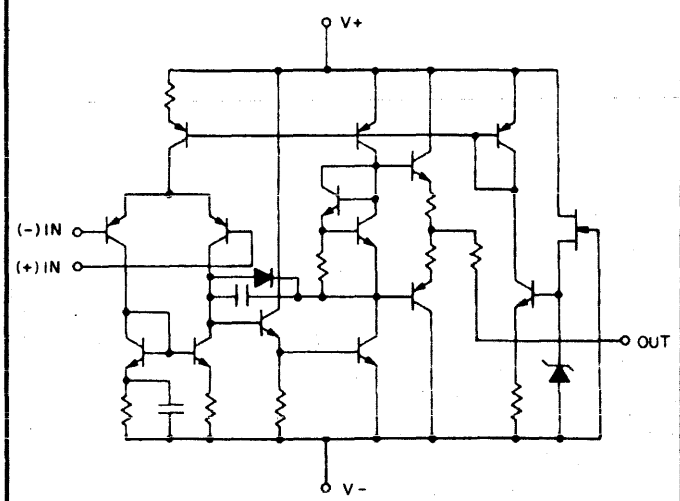
FEATURES

- Guaranteed V_{OS} . . . . . 500μ V MAX.
- Guaranteed Matched CMRR . . . . . 94 dB MIN.
- Guaranteed Matched V_{OS} . . . . . 750 μV MAX.
- RM4136/RC4136 Direct Replacements
- Low Noise
- Silicon-Nitride Passivation
- Internal Frequency Compensation
- Low Crossover Distortion
- Continuous Short Circuit Protection
- Low Input Bias Current

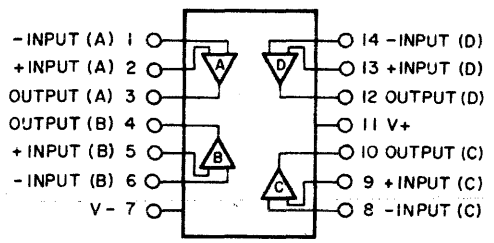
The OP-09 is ideal for use in designs requiring minimum space and cost while maintaining OP-02-type performance. OP-09's with processing per the requirements of MIL-STD-883A are available. For dual-741-type versions, see the OP-04 and OP-14 data sheets.

EQUIVALENT SCHEMATIC

(1/4 CIRCUIT SHOWN)



PIN CONNECTIONS



TOP VIEW

ORDERING INFORMATION

ORDER: OP-09AY, OP-09BY	-55°C TO +125°C
OP-09EY, OP-09FY	0°C TO +70°C

Military Temperature Range Devices
With MIL-STD-883A Class B Processing

ORDER: OP09-883-AY
OP09-883-BY

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IMPROVED LM148

OP-11

QUAD MATCHED 741-TYPE OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The OP-11 provides four matched 741-type operational amplifiers in a single 14-pin DIP package. The OP-11 is pin compatible with the LM148 and LM348 amplifiers. The amplifiers are matched for common mode rejection ratio and offset voltage. These parameters are very important in the design of instrumentation amplifiers. In addition the amplifier is designed to have equal positive-going and negative-going slew rates. This is a very important consideration for good audio system performance.

Each of the four amplifiers has the proven OP-02 advantages of low noise, low drift and excellent long term stability. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process eliminates "popcorn noise" and provides maximum reliability and long term stability of parameters for lowest overall system operating cost.

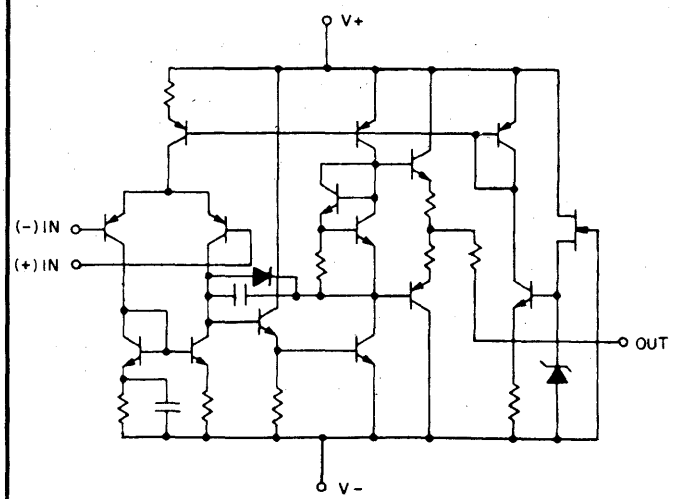
FEATURES

- Guaranteed V_{os} . . . . . 500μ V MAX.
- Guaranteed Matched CMRR . . . . . 94 dB MIN.
- Guaranteed Matched V_{os} . . . . . 750 μV MAX.
- LM148/LM348 Direct Replacements
- Low Noise
- Silicon-Nitride Passivation
- Internal Frequency Compensation
- Low Crossover Distortion
- Continuous Short Circuit Protection
- Low Input Bias Current

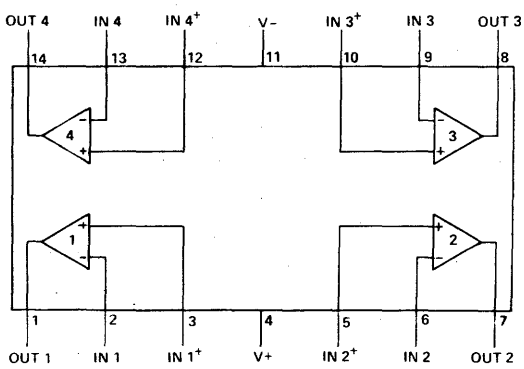
The OP-11 is ideal for use in designs requiring minimum space and cost while maintaining OP-02-type performance. OP-11's with processing per the requirements of MIL-STD-883A are available. For dual-741-type versions, see the OP-04 and OP-14 data sheets.

EQUIVALENT SCHEMATIC

(1/4 CIRCUIT SHOWN)



PIN CONNECTIONS



TOP VIEW

ORDERING INFORMATION

ORDER: OP-11AY, OP-11BY	-55°C TO +125°C
OP-11EY, OP-11FY	0°C TO +70°C

Military Temperature Range Devices
With MIL-STD-883A Class B Processing

ORDER: OP11-883-AY
OP11-883-BY

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	800 mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short Circuit Duration	Continuous (One Amplifier Only)
Storage Temperature Range	-65° to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Operating Temperature Range

OP-09A, OP-09B, OP-11A, OP-11B	-55°C to +125°C
OP-09E, OP-09F, OP-11E, OP -11F	0°C to +70°C

Note 1: Maximum package power dissipation vs. ambient temperature.

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14 Pin DIP (Y)	80°C	10 mW/°C

MATCHING CHARACTERISTICS

OP-09A OP-09E OP-11A OP-11E | OP-09B OP-09F OP-11B OP-11F

These specifications apply for V_S = ±15V, T_A = 25°C, $R_S \leq 100\Omega$, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage Match	ΔV_{OS}		–	0.5	0.75	–	0.8	2.0	mV
Common Mode Rejection Ratio Match	ΔCMRR	V_{CM} = ±CMVR	–	1.0	20	–	1.0	20	μV/V
			94	120	–	94	120	–	dB
These specifications apply for V_S = ±15V, -55°C ≤ T_A ≤ +125°C for OP-09A and OP-09B, 0°C ≤ T_A ≤ +70°C for OP-09E and OP-09F $R_S \leq 100\Omega$ unless otherwise noted.									
Input Offset Voltage Match	ΔV_{OS}		–	0.6	1.0	–	1.0	2.5	mV
Common Mode Rejection Ratio Match	ΔCMRR	V_CM = ±CMVR	–	3.2	20	–	3.2	20	μV/V
			94	110	–	94	110	–	dB

MATCHING PARAMETER DEFINITIONS

COMMON MODE REJECTION RATIO MATCH (ΔCMRR). The difference between the common-mode rejection ratios (expressed in volt/volt) of side A and side B. ΔCMRR in dB = $-20 \log_{10}$ (ΔCMRR in volt/volt). Match exists between any two amplifiers.

INPUT OFFSET VOLTAGE MATCH (ΔV_{OS}). The difference between the offset voltages of side A and side B; ($V_{OSA} - V_{OSB}$). Using amplifier A as reference then $\Delta V_{OS} = V_{OSN} - V_{OSA}$.

OP-09/OP-11 DEFINITIONS

INPUT OFFSET VOLTAGE (V_{os})
The voltage which must be applied between the input terminals to obtain zero output voltage with no load.

INPUT OFFSET CURRENT (I_{os})
The difference between the currents into the two input terminals when the output is at zero volts with no load.

INPUT BIAS CURRENT (I_B)
The average of the currents into the two input terminals when the output is at zero volts with no load.

INPUT VOLTAGE RANGE (CMVR)
The range of common-mode voltage on the input terminals for which the common-mode rejection specifications apply.

COMMON-MODE REJECTION RATIO (CMRR)
The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

POWER SUPPLY REJECTION RATIO (PSRR)
The inverse ratio of the change in input offset voltage to the change in power supply voltage producing it.

MAXIMUM OUTPUT VOLTAGE SWING (V_{om})
The peak output voltage that can be obtained without clipping.

LARGE SIGNAL VOLTAGE GAIN (A_{vo})
The ratio of the change in output voltage (over a specified range) to the change in input voltage producing it.

AVERAGE OFFSET VOLTAGE DRIFT (TCV_{os})
The ratio of the change in the offset voltage to the change in temperature producing it.

AVERAGE OFFSET CURRENT DRIFT (TCI_{os})
The ratio of the change in the offset current to the change in temperature producing it.

POWER DISSIPATION (P_d)
The total power dissipated in the amplifier with the output at zero volts and no load.

UNITY GAIN CLOSED LOOP BANDWIDTH (BW)
The frequency at which the magnitude of the small signal voltage gain of the amplifier, operated closed-loop as a unity-gain follower, is 3dB below unity.

INPUT NOISE VOLTAGE (e_{np-p})
The peak to peak noise voltage in a specified frequency band.

INPUT NOISE VOLTAGE DENSITY (e_n)
The rms noise voltage in a 1 Hz band surrounding a specified value of frequency.

INPUT NOISE CURRENT (i_{np-p})
The peak to peak noise current in a specified frequency band.

INPUT NOISE CURRENT DENSITY (i_n)
The rms noise current in a 1 Hz band surrounding a specified value of frequency.

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ELECTRICAL CHARACTERISTICS (Each Amplifier)			OP-09A OP-11A			OP-09B OP-11B			
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	$R_S \leq 10k\Omega$	–	0.30	0.50	–	0.60	2.5	mV
Input Offset Current	I_{os}		–	5.5	20	–	25	50	nA
Input Bias Current	I_B		–	180	300	–	300	500	nA
Input Resistance Differential Mode	R_{in}		0.20	0.40	–	0.20	0.40	–	MΩ
Input Voltage Range	CMVR		±12	±13	–	±12	±13	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_S \leq 10k\Omega$	100	120	–	100	120	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±15V $R_S \leq 10k\Omega$	90	110	–	90	110	–	dB
Output Voltage Swing	V_{oM}	$R_L \geq 2k\Omega$	±11	±13	–	±11	±13	–	V
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_O = ±10V	100	650	–	100	650	–	V/mV
Power Consumption (Note 1)	P_d	V_O = 0V	–	123	180	–	123	180	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.7	–	–	0.7	–	μV p-p
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	18 14 12	– – –	– – –	18 14 12	– – –	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	17	–	–	17	–	pA p-p
Channel Separation	CS		100	130	–	100	130	–	dB
Input Noise Current Density	i_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	1.8 1.5 1.2	– – –	– – –	1.8 1.5 1.2	– – –	pA/√Hz
Slew Rate (Note 2)	SR		0.70	1.0	–	0.70	1.0	–	V/μs
Large Signal Bandwidth (Note 2)		V_O = 20Vp-p	11	16	–	11	16	–	kHz
Closed Loop Bandwidth (Note 2)	BW	A_{VCL} = +1.0	1.5	2.0	–	1.5	2.0	–	MHz
Risetime (Note 2)		A_V = +1 V_{IN} = 50mV	–	80	120	–	80	120	nsec
Overshoot (Note 2)			–	15	25	–	15	25	%
The following specifications apply for V_S = ±15V, –55°C ≤ T_A ≤ +125°C, unless otherwise noted.									
Input Offset Voltage	V_{os}	$R_S \leq 10k\Omega$	–	0.40	1.0	–	1.0	3.5	mV
Average Input Offset Voltage Drift (Note 2)	TCV_{os}	$R_S \leq 10k\Omega$	–	2.0	10	–	4.0	15	μV/°C
Input Offset Current	I_{os}		–	20	40	–	40	80	nA
Average Input Offset Current Drift	TCI_{os}		–	0.10	0.30	–	0.30	0.60	nA/°C
Input Bias Current	I_B		–	200	375	–	400	650	nA
Input Voltage Range	CMVR		±12	±13	–	±12	±13	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_S \geq 10k\Omega$	100	120	–	100	120	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±15V $R_S \leq 10k\Omega$	90	110	–	90	110	–	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_O = ±10V	50	250	–	50	250	–	V/mV
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 2k\Omega$	±11	±13	–	±11	±13	–	V
Power Consumption (Note 1)	P_d	V_O = 0V	–	115	200	–	115	200	mW

NOTE 1: Total dissipation for all 4 amplifiers in package.

NOTE 2: Parameter is not 100% tested. 90% of all units meet these specifications.

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ELECTRICAL CHARACTERISTICS (Each Amplifier)			OP-09E OP-11E			OP-09F OP-11F			
These specifications for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	Symbol	Test Conditions	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage	V_{os}	$R_S \leq 10k\Omega$	–	0.30	0.50	–	0.60	2.5	mV
Input Offset Current	I_{os}		–	5.5	20	–	25	50	nA
Input Bias Current	I_B		–	180	300	–	300	500	nA
Input Resistance Differential Mode	R_{in}		0.20	0.40	–	0.20	0.40	–	MΩ
Input Voltage Range	CMVR		±12	±13	–	±12	±13	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_S \leq 10k\Omega$	100	120	–	100	120	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±15V $R_S \leq 10k\Omega$	90	110	–	90	110	–	dB
Output Voltage Swing	V_{oM}	$R_L \geq 2k\Omega$	±11	±13	–	±11	±13	–	V
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_O = ±10V	100	650	–	100	650	–	V/mV
Power Consumption (Note 1)	P_d	V_O = 0V	–	123	180	–	123	180	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	–	0.7	–	–	0.7	–	μV p-p
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	18 14 12	– – –	– – –	18 14 12	– – –	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	–	17	–	–	17	–	pA p-p
Channel Separation	CS		100	130	–	100	130	–	dB
Input Noise Current Density	i_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	– – –	1.8 1.5 1.2	– – –	– – –	1.8 1.5 1.2	– – –	pA/√Hz
Slew Rate (Note 2)	SR		0.70	1.0	–	0.70	1.0	–	V/μs
Large Signal Bandwidth (Note 2)		V_O = 20Vp-p	11	16	–	11	16	–	kHz
Closed Loop Bandwidth (Note 2)	BW	A_{VCL} = +1.0	1.5	2.0	–	1.5	2.0	–	MHz
Risetime (Note 2)		A_V = +1 V_{IN} = 50mV	–	80	120	–	80	120	nsec
Overshoot (Note 2)			–	15	25	–	15	25	%
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤+70°C, unless otherwise noted.									
Input Offset Voltage	V_{os}	$R_S \leq 10k\Omega$	–	0.40	0.80	–	0.80	3.0	mV
Average Input Offset Voltage Drift (Note 2)	TCV_{os}	$R_S \leq 10k\Omega$	–	2.0	10	–	4.0	15	μV/°C
Input Offset Current	I_{os}		–	20	30	–	40	60	nA
Average Input Offset Current Drift	TCI_{os}		–	0.10	0.30	–	0.30	0.60	nA/°C
Input Bias Current	I_B		–	200	350	–	400	550	nA
Input Voltage Range	CMVR		±12	±13	–	±12	±13	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR $R_S \geq 10k\Omega$	100	120	–	100	120	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±15V $R_S \leq 10k\Omega$	90	110	–	90	110	–	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_O = ±10V	50	250	–	50	250	–	V/mV
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 2k\Omega$	±11	±13	–	±11	±13	–	V
Power Consumption (Note 1)	P_d	V_O = 0V	–	115	200	–	115	200	mW

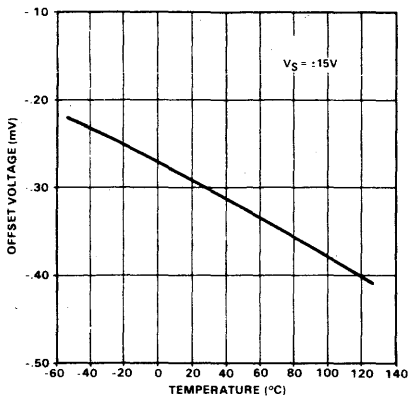
NOTE 1: Total dissipation for all 4 amplifiers in package.

NOTE 2: Parameter is not 100% tested. 90% of all units meet these specifications.

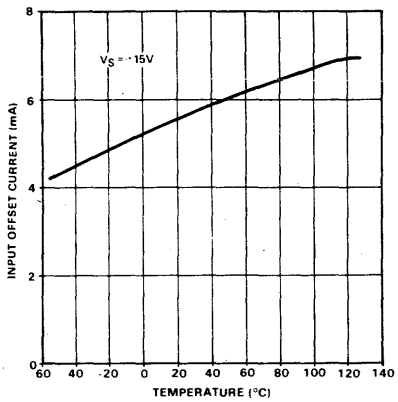
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TYPICAL PERFORMANCE CURVES

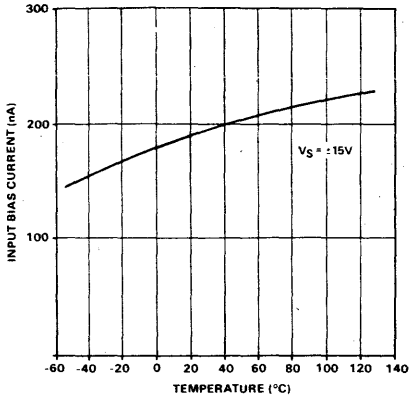
OFFSET VOLTAGE VS TEMPERATURE



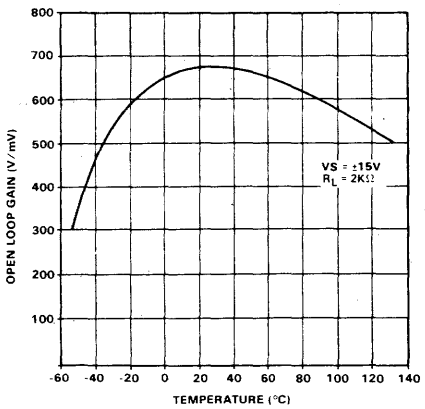
OFFSET CURRENT VS TEMPERATURE



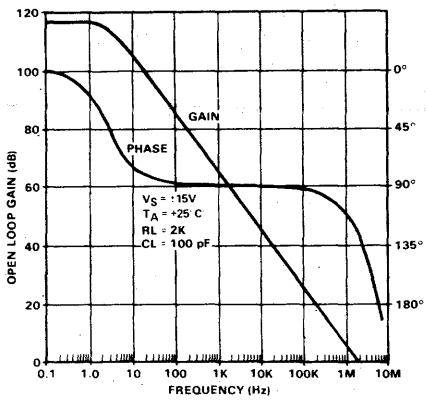
BIAS CURRENT VS TEMPERATURE



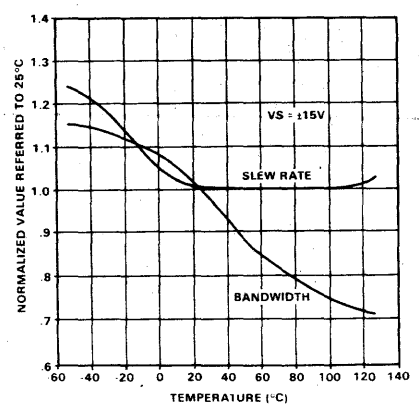
OPEN LOOP GAIN VS TEMPERATURE



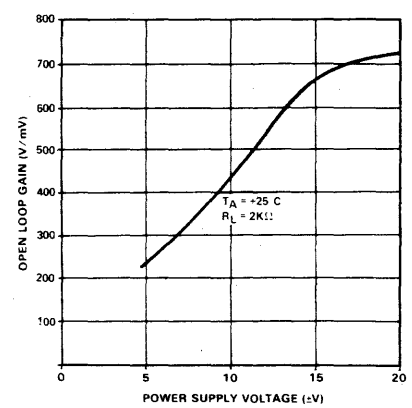
OPEN LOOP FREQUENCY & PHASE RESPONSE



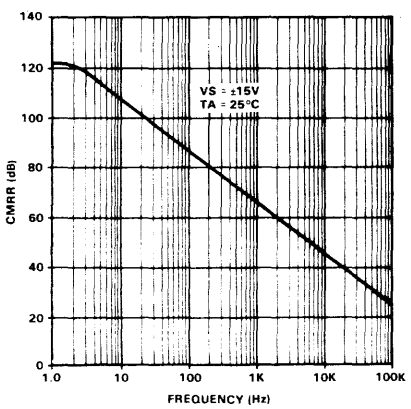
NORMALIZED A/C PARAMETERS VS TEMPERATURE



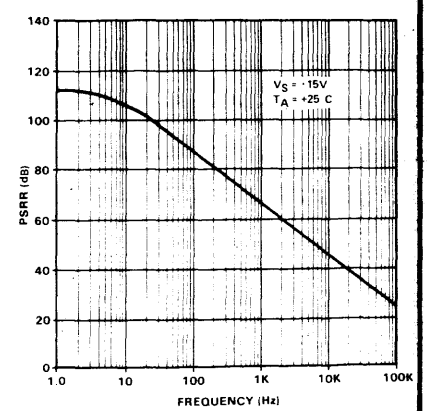
OPEN LOOP GAIN VS SUPPLY VOLTAGE



CMRR VS FREQUENCY



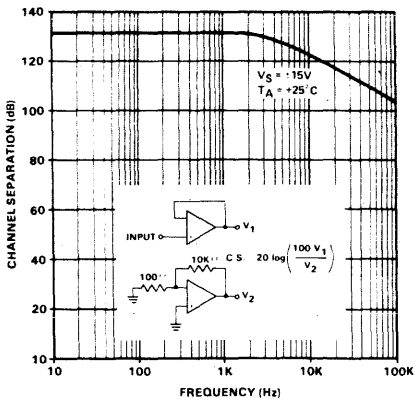
PSRR VS FREQUENCY



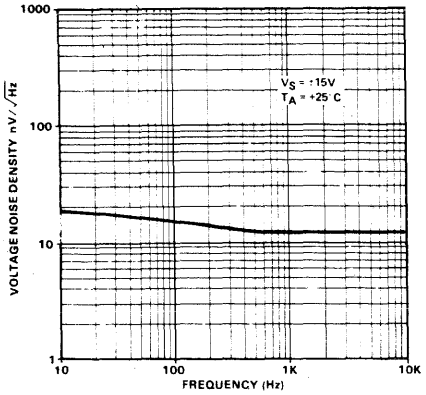
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TYPICAL PERFORMANCE CURVES

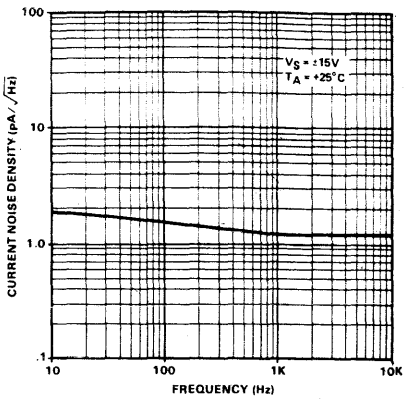
CHANNEL SEPARATION VS FREQUENCY



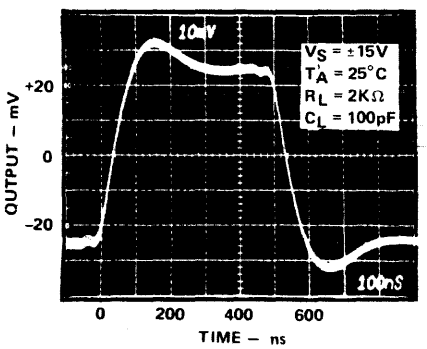
SPOT NOISE VOLTAGE VS FREQUENCY



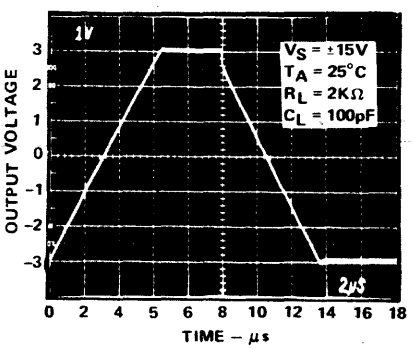
SPOT NOISE CURRENT VS FREQUENCY



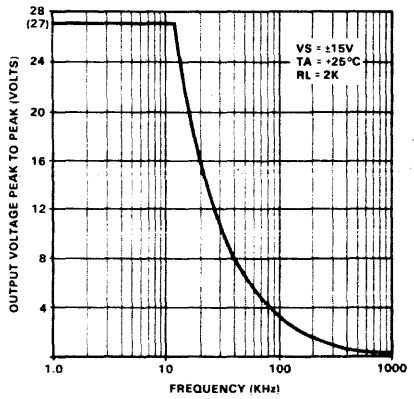
TRANSIENT RESPONSE



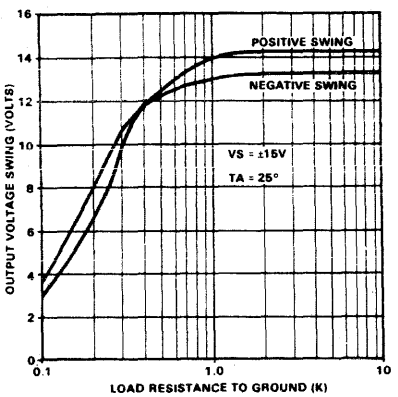
VOLTAGE FOLLOWER PULSE RESPONSE



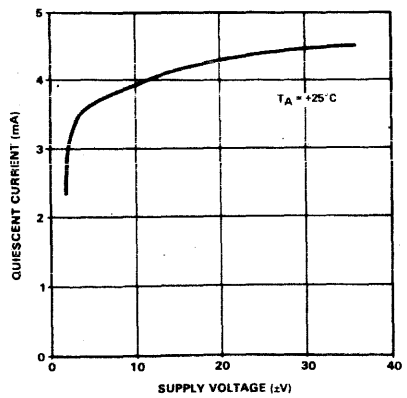
MAX UNDISTORTED OUTPUT VS FREQUENCY



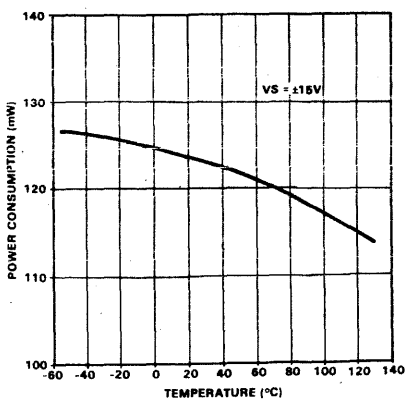
OUTPUT VOLTAGE VS LOAD RESISTANCE



QUIESCENT CURRENT VS SUPPLY VOLTAGE



POWER CONSUMPTION VS TEMPERATURE



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IMPROVED PM155A

OP-15

PRECISION JFET INPUT OPERATIONAL AMPLIFIER

LOW SUPPLY CURRENT

GENERAL DESCRIPTION

The OP-15 provides an excellent combination of high speed and low input offset voltage. In addition the OP-15 offers the speed of the 156A op amp with 155A dissipation. To further enhance the excellent input parameters, the OP-15 uses bias current compensation to maintain low input bias current at elevated temperatures.

The OP-15 was designed to provide real precision performance along with its high speed. For example the 500μV offset voltage yields less than 1/2 LSB error in a 12 bit, 5V DAC. Although the OP-15 can be nulled, the design objective was to provide low offset voltage and drift WITHOUT NULLING. Systems become MORE COST-EFFECTIVE as the number of error correcting "knobs" decrease. PMI achieves this performance by use of an improved BI-FET process coupled with on-chip zener-zap offset trimming.

Most high speed monolithic op amps give settling time specifications to 0.01% error band, and so does PMI. Since 0.01% of 10V is 1mV, it is surprising that these same op amps have offset voltage errors in the 0.02% to 0.3% range. A large number of applications are in the 0.05% to 0.1% range, and PMI also gives specs for these error bands in its settling times. The fact that 500μV is only 0.005% of 10V is why PMI specifies settling time to a true 0.01% error band.

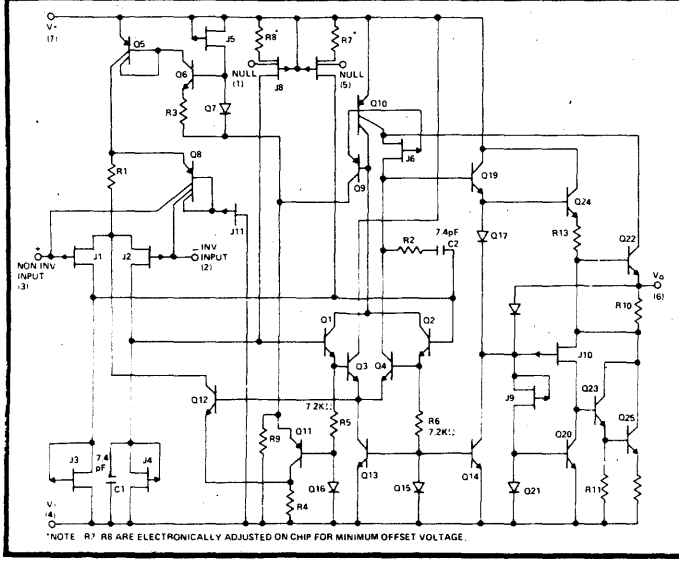
The combination of low input offset voltage of 500μV MAX., slew rate of 17V/μsec, and settling time of 900nsec—to 0.1%—makes the OP-15 a true precision, high speed op amp. The additional features of low supply current coupled with an input bias current of 9nA at 125°C ambient (not junction) temperature makes the OP-15 useful in a wide range of applications.

Applications include high speed amplifiers for current output DAC's, active filters, sample-and-hold buffers, and photocell amplifiers. For additional precision JFET op amps, see the OP-16 and OP-17 data sheets.

FEATURES

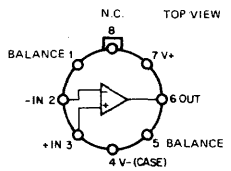
- High Slew Rate 17V/μs
- Fast Settling to ±0.1% . . . . . 900 nsec
- Low Input Offset Voltage . . . . . 500 μV MAX
- Low Input Offset Voltage Drift . . . . . 2.0 μV/°C
- 156 Speed with 155 Dissipation
- Wide Bandwidth . . . . . 6 MHz
- Minimum Slew Rate Guaranteed on All Models
- Temperature Compensated Input Bias Currents*
- Guaranteed Input Bias Current @ 125°C. . 9nA MAX
- Bias Current Specified WARMED UP Over Temp.
- Internal Compensation
- Low Input Noise Current . . . . . 0.01 pA $\sqrt{Hz}$
- High Common Mode Rejection Ratio 100dB
- Models With MIL-STD-883A Class B Processing Available From Stock

SIMPLIFIED SCHEMATIC DIAGRAM



*NOTE R7 R8 ARE ELECTRONICALLY ADJUSTED ON CHIP FOR MINIMUM OFFSET VOLTAGE.

PIN CONNECTIONS



TO-99 (J Suffix)

ORDERING INFORMATION

ORDER: OP-15AJ, OP-15BJ, OP-15CJ	−55°C TO +125°C
OP-15EJ, OP-15FJ, OP-15GJ	0°C TO +70°C

Military Temperature Range Devices
With MIL-STD-883A Class B Processing

ORDER: OP15-883-AJ
ORDER OP15-883-BJ
OP15-883-CJ

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- OP-15A, OP-15B, OP-15E, OP-15F: ±22V
- OP-15C, OP-15G: ±18V

Internal Power Dissipation
- All Devices: 500mW
  (The TO-99(J) package must be derated based on a thermal resistance of 150° C/W junction to ambient or 45° C/W junction to case.)

Operating Temperature Range
- OP-15A, OP-15B, OP-15C: –55°C to +125°C
- OP-15E, OP-15F, OP-15G: 0°C to +70°C

Maximum Junction Temperature (T_J)
- All Devices: +150°C

Differential Input Voltage
- OP-15A, OP-15B, OP-15E, OP-15F: ±40V
- OP-15C, OP-15G: ±30V

Input Voltage
- OP-15A, OP-15B, OP-15E, OP-15F: ±20V
- OP-15C, OP-15G: ±16V

  (Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.)

Output Short Circuit Duration: Indefinite

Storage Temperature Range: –65°C to +150°C

Lead Temperature Range (Soldering, 60 sec): +300°C

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	OP-15A Min	OP-15A Typ	OP-15A Max	OP-15B Min	OP-15B Typ	OP-15B Max	OP-15C Min	OP-15C Typ	OP-15C Max	Units
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.2	0.5	–	0.4	1.0	–	0.5	3.0	mV
Input Offset Current	I_{OS}	T_J - 25°C (Note 1)	–	3.0	10	–	3.0	20	–	3.0	50	pA
		Device Operating	–	5.0	22	–	5.0	40	–	5.0	100	
Input Bias Current	I_B	T_J = 25°C (Note 1)	–	15	50	–	15	100	–	15	200	pA
		Device Operating	–	18	110	–	18	200	–	18	400	
Input Resistance	R_{in}		–	10^{12}	–	–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K\Omega$, V_O = ±10V	100	240	–	75	220	–	50	200	–	V/mV
Output Voltage Swing	V_{OM}	R_L = 10K	±12	±13	–	±12	±13	–	±12	±13	–	V
		R_L = 2K	±11	±12.7	–	±11	±12.7	–	±11	±12.7	–	
Supply Current	I_{SY}		–	2.7	4.0	–	2.7	4.0	–	2.8	5.0	mA
Slew Rate	SR	A_{VCL} = +1.0	10	17	–	7.5	16	–	5.0	15	–	V/μsec
Gain-Bandwidth Product	GBW		4.0	6.0	–	3.5	5.7	–	3.0	5.4	–	MHz
Closed Loop Bandwidth	CLBW	A_{VCL} = +1.0	–	14	–	–	13	–	–	12	–	MHz
Settling Time	t_S	to 0.01%	–	2.2	–	–	2.3	–	–	2.4	–	μs
		to 0.05% (Note 2)	–	1.1	–	–	1.1	–	–	1.2	–	
		to 0.10%	–	0.9	–	–	0.9	–	–	1.0	–	
Input Voltage Range	CMVR		±10.5	+14.8 −11.5	–	±10.5	+14.8 −11.5	–	±10.3	+14.8 −11.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	86	100	–	86	100	–	82	96	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	86	100	–	86	100	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	82	100	–	
Input Noise Voltage Density	e_n	f_O = 100Hz	–	20	–	–	20	–	–	20	–	nV/√Hz
		f_O = 1000Hz	–	15	–	–	15	–	–	15	–	
Input Noise Current Density	i_n	f_O = 100Hz	–	0.01	–	–	0.01	–	–	0.01	–	pA/√Hz
		f_O = 1000Hz	–	0.01	–	–	0.01	–	–	0.01	–	
Input Capacitance	C_{IN}		–	3.0	–	–	3.0	–	–	3.0	–	pF
The following specifications apply for V_S = ±15V, –55°C ≤ T_A ≤ +125°C, unless otherwise noted.												
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.4	0.9	–	0.7	2.0	–	0.9	4.5	mV
Average Input Offset Voltage Drift											(Note 3)	
Without External Trim	TCV_{OS}		–	2.0	5.0	–	3.0	10	–	4.0	15	μV/°C
With External Trim	TCV_{OSn}	R_P = 100KΩ	–	2.0	–	–	3.0	–	–	4.0	–	
Input Offset Current (Note 1)	I_{OS}	T_J = 125°C	–	0.6	4.0	–	0.8	6.0	–	1.0	9.0	nA
		T_A = 125°C Device Operating	–	0.8	7.0	–	1.2	11	–	1.5	17	
Input Bias Current (Note 1)	I_B	T_J = 125°C	–	1.2	5.0	–	1.5	7.5	–	1.8	10	nA
		T_A = 125°C Device Operating	–	1.7	9.0	–	2.2	14	–	2.7	19	
Input Voltage Range	CMVR		±10.4	+14.6 −11.3	–	±10.4	+14.6 −11.3	–	±10.25	+14.6 −11.3	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	97	–	85	97	–	80	93	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	85	97	–	85	97	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	80	93	–	
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K$, V_S = ±10V	35	120	–	30	110	–	25	100	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10K\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V

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ELECTRICAL CHARACTERISTICS			OP-15E			OP-15F			OP-15G			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.												
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.2	0.5	–	0.4	1.0	–	0.5	3.0	mV
Input Offset Current	I_{OS}	T_J = 25°C (Note 1)	–	3.0	10	–	3.0	20	–	3.0	50	pA
		Device Operating	–	5.0	22	–	5.0	40	–	5.0	100	
Input Bias Current	I_B	T_J = 25°C (Note 1)	–	15	50	–	15	100	–	15	200	pA
		Device Operating	–	18	110	–	18	200	–	18	400	
Input Resistance	R_{in}		–	10^{12}	–	–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K\Omega$, V_S = ±10V	100	240	–	75	220	–	50	200	–	V/mV
Output Voltage Swing	V_{OM}	R_L = 10K	±12	±13	–	±12	±13	–	±12	±13	–	V
		R_L = 2K	±11	±12.7	–	±11	±12.7	–	±11	±12.7	–	
Supply Current	I_{SY}		–	2.7	4.0	–	2.7	4.0	–	2.8	5.0	mA
Slew Rate	SR	A_{VCL} = +1.0	10	17	–	7.5	16	–	5.0	15	–	V/μsec
Gain Bandwidth Product	GBW		4.0	6.0	–	3.5	5.7	–	5.0	5.4	–	MHz
Closed Loop Bandwidth	CLBW	A_{VCL} = +1.0	–	14	–	–	13	–	–	12	–	MHz
Settling Time	t_S	to 0.01%	–	2.2	–	–	2.3	–	–	2.4	–	μs
		to 0.05% (Note 2)	–	1.1	–	–	1.1	–	–	1.2	–	
		to 0.10%	–	0.9	–	–	0.9	–	–	1.0	–	
Input Voltage Range	CMVR		±10.5	+14.8 −11.5	–	±10.5	+14.8 −11.5	–	±10.3	+14.8 −11.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	86	100	–	86	100	–	82	96	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	86	100	–	86	100	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	82	100	–	
Input Noise Voltage Density	e_n	f_O = 100Hz	–	20	–	–	20	–	–	20	–	nV/√Hz
		f_O = 1000Hz	–	15	–	–	15	–	–	15	–	
Input Noise Current Density	i_n	f_O = 100Hz	–	0.01	–	–	0.01	–	–	0.01	–	pA/√Hz
		f_O = 1000Hz	–	0.01	–	–	0.01	–	–	0.01	–	
Input Capacitance	C_{IN}		–	3.0	–	–	3.0	–	–	3.0	–	pF
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.												
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.3	0.75	–	0.55	1.5	–	0.7	3.8	mV
Average Input Offset Voltage Drift											(Note 3)	
Without External Trim	TCV_{OS}		–	2.0	5.0	–	3.0	10	–	4.0	15	μV/°C
With External Trim	TCV_{OSn}	R_P = 100KΩ	–	2.0	–	–	3.0	–	–	4.0	–	
Input Offset Current	I_{OS}	T_J = +70°C (Note 1)	–	0.04	0.30	–	0.06	0.45	–	0.08	0.65	nA
		T_A = +70°C Device Operating	–	0.06	0.55	–	0.08	0.80	–	0.10	1.2	
Input Bias Current	I_B	T_J = +70°C (Note 1)	–	0.10	0.40	–	0.12	0.60	–	0.14	0.80	nA
		T_A = +70°C Device Operating	–	0.13	0.75	–	0.16	1.1	–	0.19	1.5	
Input Voltage Range	CMVR		±10.4	+14.7 −11.4	–	±10.4	+14.7 −11.4	–	±10.25	+14.7 −11.4	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	98	–	85	98	–	80	94	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	85	98	–	85	98	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	80	94	–	
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K$, V_S = ±10V	65	200	–	50	180	–	35	130	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10K\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V

NOTE 1: Due to limited production test times the bias currents correspond to junction temperatures. The bias current vs. time (after power-on) curve clarifies this point. Since most amplifiers (in use) are on for more than 1 second, PMI also specifies the bias current for the warmed-up condition. The warmed-up bias current value is correlated to the junction temp. value via the curves of I_B vs. T_J and I_B vs. T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at V_{CM} = 0.

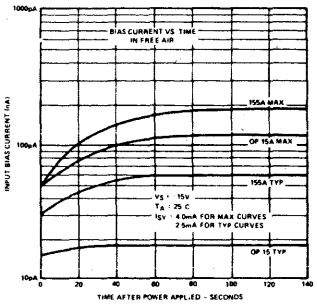
NOTE 2: Settling time is defined here for a unity gain inverter connection using 2KΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.

NOTE 3: Parameter is not 100% tested. 90% of all units meet these specifications.

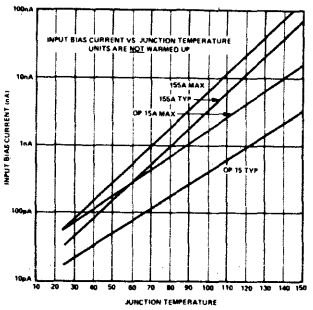
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TYPICAL PERFORMANCE CURVES

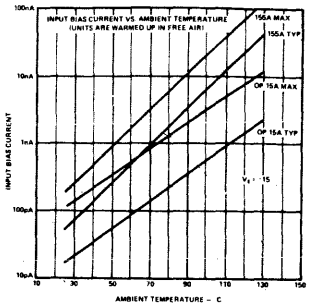
BIAS CURRENT VS. TIME IN FREE AIR



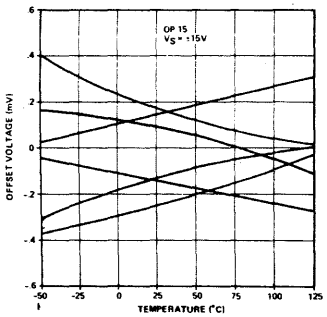
INPUT BIAS CURRENT VS. JUNCTION TEMPERATURE UNITS ARE NOT WARMED-UP



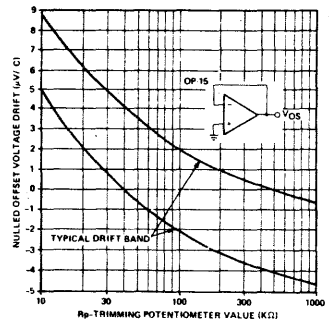
INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE (UNITS ARE WARMED-UP IN FREE AIR)



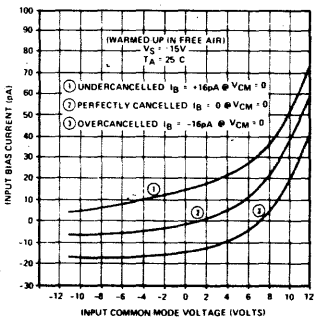
OFFSET VOLTAGE VS TEMPERATURE DRIFT OF REPRESENTATIVE UNITS



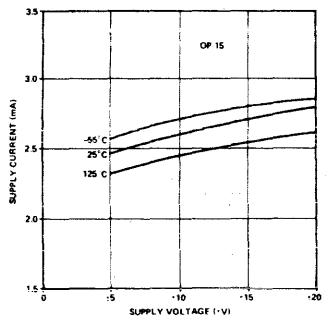
NULLED OFFSET VOLTAGE DRIFT VS POTENTIOMETER SIZE



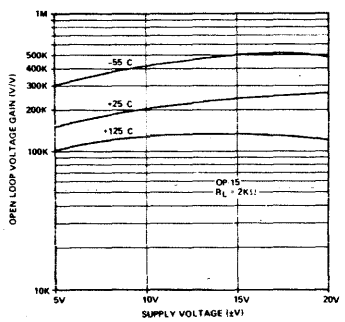
INPUT BIAS CURRENT VS COMMON MODE VOLTAGE



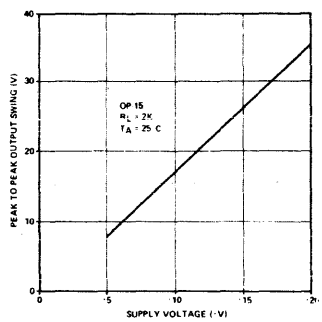
SUPPLY CURRENT VS SUPPLY VOLTAGE



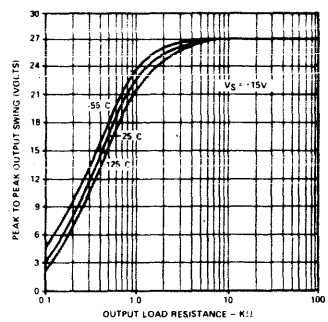
OPEN LOOP VOLTAGE GAIN



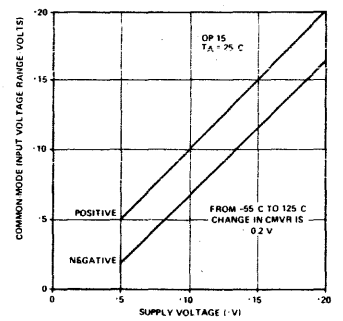
VOLTAGE SWING VS SUPPLY VOLTAGE



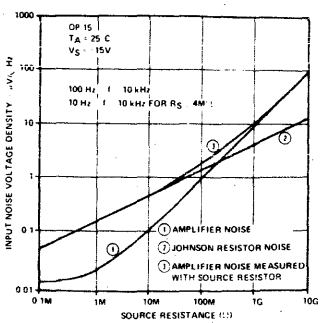
OUTPUT VOLTAGE VS LOAD RESISTANCE



COMMON MODE INPUT VOLTAGE RANGE



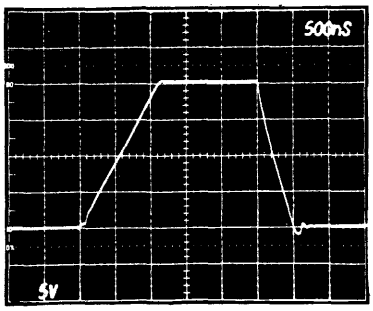
VOLTAGE NOISE VS SOURCE RESISTANCE



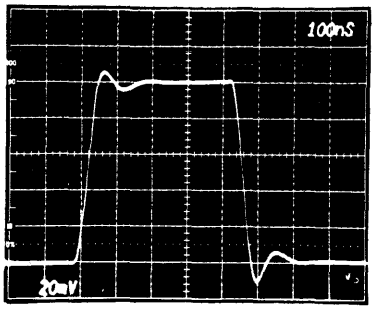
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TYPICAL PERFORMANCE CURVES

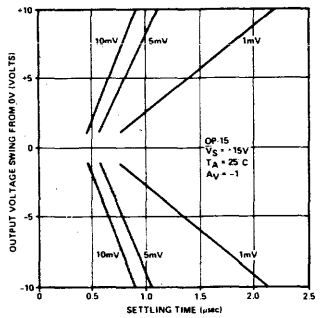
LARGE SIGNAL TRANSIENT RESPONSE



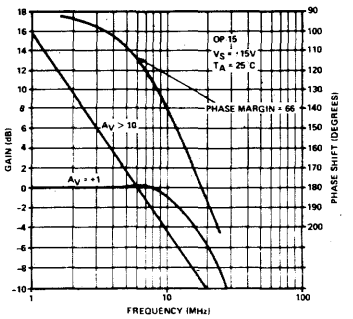
SMALL SIGNAL TRANSIENT RESPONSE



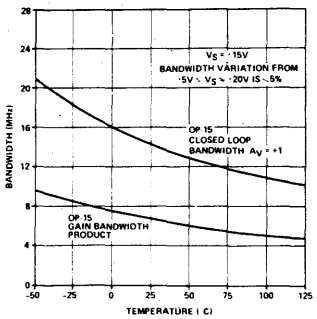
SETTLING TIME



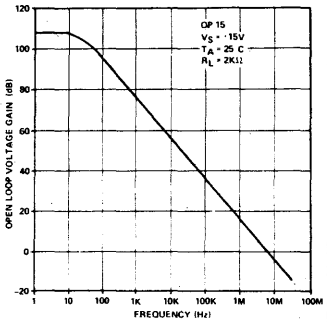
CLOSED LOOP BANDWIDTH AND PHASE SHIFT VS FREQUENCY



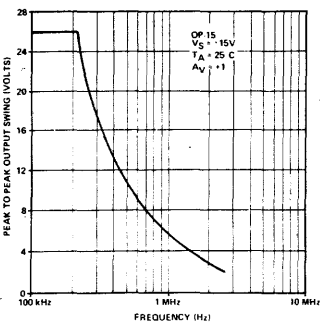
BANDWIDTH VS TEMPERATURE



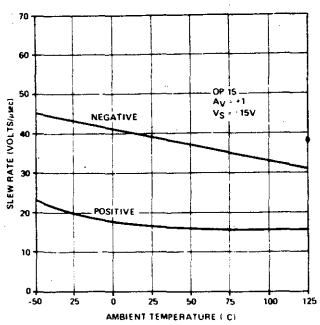
OPEN LOOP FREQUENCY RESPONSE



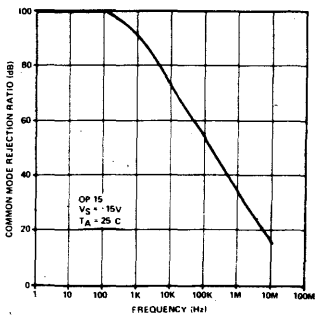
UNDISTORTED OUTPUT SWING



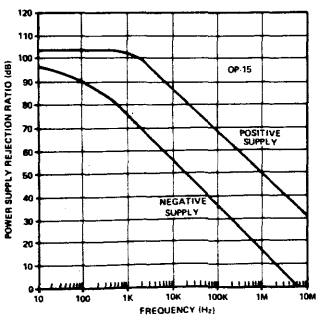
SLEW RATE VS TEMPERATURE



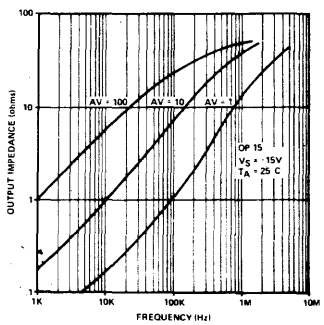
COMMON MODE REJECTION RATIO VS FREQUENCY



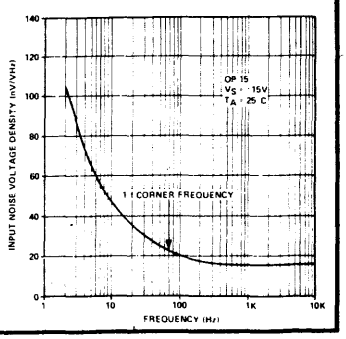
POWER SUPPLY REJECTION VS FREQUENCY



OUTPUT IMPEDANCE VS FREQUENCY



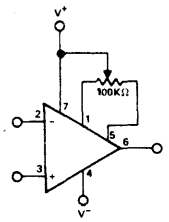
VOLTAGE NOISE VS FREQUENCY



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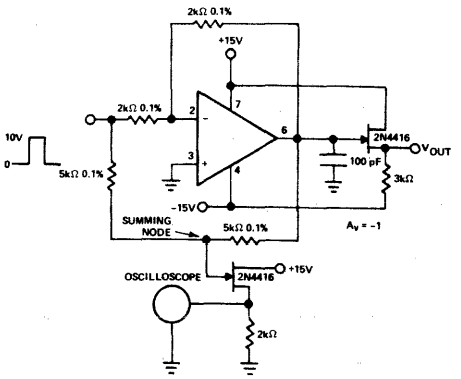
BASIC CONNECTIONS

INPUT OFFSET VOLTAGE NULLING



NOTE: V_{OS} CAN BE TRIMMED WITH POTENTIOMETERS RANGING FROM 10KΩ TO 1MΩ. FOR MOST UNITS TCV_{OS} WILL BE MINIMUM WHEN V_{OS} IS ADJUSTED WITH A 100KΩ POTENTIOMETER.

SETTLING TIME TEST CIRCUIT



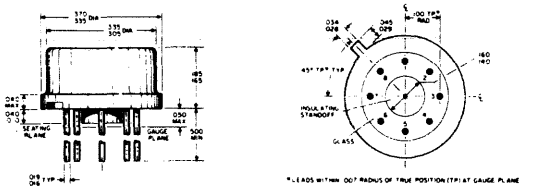
APPLICATION INFORMATION

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

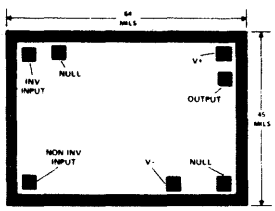
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

PACKAGE DIMENSIONS



TO-99 (J)

CHIP DIMENSIONS



SPECIFICATION COMPARISON TABLE (OP-15 VS. LF155)

		-55°C/+125°C MODELS					0°C/+70°C MODELS				
SPECIFICATION	CONDITION	OP-15A	LF155A	OP-15B	OP-15C	LF155	OP-15E	LF355A	OP-15F	OP-15G	LF355
MAX Input Offset Voltage	T_A=25°C	0.5mV	2.0mV	1.0mV	3.0mV	5.0mV	0.5mV	2.0mV	1.0mV	3.0mV	10mV
MAX Input Offset Voltage	T_A=Full	0.9mV	2.5mV	2.0mV	4.5mV	7.0mV	0.75mV	2.3mV	1.5mV	3.8mV	13mV
MAX Input Offset Voltage Drift	T_A=Full	5μV/°C	5μV/°C	10μV/°C	15μV/°C	NO SPEC	5μV/°C	5μV/°C	10μV/°C	15μV/°C	NO SPEC
MAX Input Bias Current	T_j=25°C	50pA	50pA	100pA	200pA	100pA	50pA	50pA	100pA	200pA	200pA
MAX Input Bias Current	T_A=25°C (Note)	110pA	NO SPEC	200pA	400pA	NO SPEC	110pA	NO SPEC	200pA	400pA	NO SPEC
MAX Input Bias Current	T_j=Full	5.0nA	25nA	7.5nA	10nA	50nA	0.4nA	5nA	0.6nA	0.8nA	8nA
MAX Input Bias Current	T_A=Full (Note)	9.0nA	NO SPEC	14nA	19nA	NO SPEC	0.75nA	NO SPEC	1.1nA	1.5nA	NO SPEC
MIN Slew Rate	T_A=25°C A_V=+1	10V/μsec	3V/μsec	7.5V/μsec	5.0V/μsec	NO SPEC	10V/μsec	3V/μsec	7.5V/μsec	5.0V/μsec	NO SPEC
MAX Supply Current	T_A=25°C	4.0mA	4.0mA	4.0mA	5.0mA	4.0mA	4.0mA	4.0mA	4.0mA	5.0mA	4.0mA

NOTE: Warmed up bias current.

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IMPROVED PM156A

OP-16

PRECISION JFET INPUT OPERATIONAL AMPLIFIER

WIDE BANDWIDTH

GENERAL DESCRIPTION

The OP-16 offers a performance combination not usually found in the same op amp—high speed and low input offset voltage. Not only does the OP-16 out-perform the 156A in speed and error band, but it is clearly superior to several more costly hybrid and dielectrically-isolated op amps. In addition, the OP-16 uses bias current compensation to maintain low input bias current at elevated temperatures.

The OP-16 was designed to provide real precision performance along with its high speed. For example the 500μV offset voltage yields less than 1/2 LSB error in a 12 bit, 5V DAC. Although the OP-16 can be nulled, the design objective was to provide low offset voltage and drift WITHOUT NULLING. Systems become MORE COST-EFFECTIVE as the number of error correcting "knobs" decrease. PMI achieves this performance by use of an improved BI-FET process coupled with on-chip zener-zap offset trimming.

Most high speed monolithic op amps give settling time specifications to 0.01% error band, and so does PMI. Since 0.01% of 10V is 1mV, it is surprising that these same op amps have offset voltage errors in the 0.02% to 0.3% range. A large number of applications are in the 0.05% to 0.1% range, and PMI also gives specs for these error bands in its settling times. The fact that 500μV is only 0.005% of 10V is why PMI specifies settling time to a true 0.01% error band.

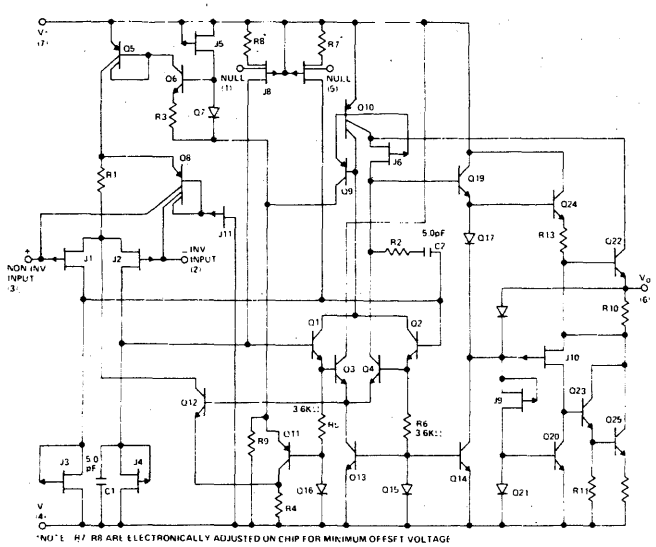
The combination of low input offset voltage of 500μV MAX., slew rate of 25V/μsec, and settling time of 700nsec—to 0.1%—makes the OP-16 a true precision, high speed op amp. Because of the input bias current compensation, the maximum input bias current at 125°C ambient (not junction) temperature is only 11nA. This kind of performance makes the OP-16 useful in a wide range of applications.

Applications include high speed amplifiers for current output DAC's, active filters, sample-and-hold buffers, and photocell amplifiers. For additional precision JFET op amps, see the OP-15 and OP-17 data sheets.

FEATURES

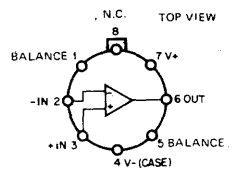
- **High Slew Rate** **25V/μs**
- **Fast Settling to ±0.1%** ..... **700 nsec**
- **Low Input Offset Voltage** ..... **500 μV MAX**
- **Low Input Offset Voltage Drift** ..... **2.0 μV/°C**
- **Wide Bandwidth** ..... **8 MHz**
- **Minimum Slew Rate Guaranteed on All Models**
- **Temperature Compensated Input Bias Currents***
- **Guaranteed Input Bias Current @ 125°C. .11nA MAX**
- **Bias Current Specified WARMED UP Over Temp.**
- **Internal Compensation**
- **Low Input Noise Current** ..... **0.01 pA $\sqrt{Hz}$**
- **High Common Mode Rejection Ratio** **100dB**
- **Models With MIL-STD-883A Class B Processing Available From Stock**

SIMPLIFIED SCHEMATIC DIAGRAM



*NOTE: R7, R8 ARE ELECTRONICALLY ADJUSTED ON CHIP FOR MINIMUM OFFSET VOLTAGE

PIN CONNECTIONS



TO 99 (J Suffix)

ORDERING INFORMATION

ORDER:	OP-16AJ OP-16BJ OP-16CJ	-55°C TO +125°C
	OP-16EJ OP-16FJ OP-16GJ	0°C TO +70°C

Military Temperature Range Devices
With MIL-STD-883A Class B Processing

ORDER: OP16-883-AJ
OP16-883-BJ
OP16-883-CJ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- OP-16A, OP-16B, OP-16E, OP-16F: ±22V
- OP-16C, OP-16G: ±18V

Internal Power Dissipation
- All Devices: 500mW
  - (The TO-99(J) package must be derated based on a thermal resistance of 150° C/W junction to ambient or 45° C/W junction to case.)

Operating Temperature Range
- OP-16A, OP-16B, OP-16C: –55°C to +125°C
- OP-16E, OP-16F, OP-16G: 0°C to +70°C

Maximum Junction Temperature (T_J)
- All Devices: +150°C

Differential Input Voltage
- OP-16A, OP-16B, OP-16E, OP-16F: ±40V
- OP-16C, OP-16G: ±30V

Input Voltage
- OP-16A, OP-16B, OP-16E, OP-16F: ±20V
- OP-16C, OP-16G: ±16V
  - (Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.)

Output Short Circuit Duration: Indefinite

Storage Temperature Range: –65°C to +150°C

Lead Temperature Range (Soldering, 60 sec): +300°C

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	OP-16A Min	OP-16A Typ	OP-16A Max	OP-16B Min	OP-16B Typ	OP-16B Max	OP-16C Min	OP-16C Typ	OP-16C Max	Units
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.2	0.5	–	0.4	1.0	–	0.5	3.0	mV
Input Offset Current	I_{OS}	T_J = 25°C (Note 1)	–	3.0	10	–	3.0	20	–	3.0	50	pA
		Device Operating	–	5.0	25	–	5.0	50	–	5.0	125	
Input Bias Current	I_B	T_J = 25°C (Note 1)	–	15	50	–	15	100	–	15	200	pA
		Device Operating	–	20	130	–	20	250	–	20	500	
Input Resistance	R_{in}		–	10^{12}	–	–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K\Omega$, V_S = ±10V	100	240	–	75	220	–	50	200	–	V/mV
Output Voltage Swing	V_{OM}	R_L = 10K	±12	±13	–	±12	±13	–	±12	±13	–	V
		R_L = 2K	±11	±12.7	–	±11	±12.7	–	±11	±12.7	–	
Supply Current	I_{SY}		–	4.6	7.0	–	4.6	7.0	–	4.8	8.0	mA
Slew Rate	SR	A_{VCL} = +1.0	18	25	–	12	24	–	9.0	23	–	V/μsec
Gain Bandwidth Product	GBW		6.0	8.0	–	5.5	7.6	–	5.0	7.2	–	MHz
Closed Loop Bandwidth	CLBW	A_{VCL} = +1.0	–	19	–	–	18	–	–	17	–	MHz
Settling Time	t_s	to 0.01%	–	1.7	–	–	1.7	–	–	1.8	–	μs
		to 0.05% (Note 2)	–	0.9	–	–	0.9	–	–	1.0	–	
		to 0.10%	–	0.7	–	–	0.7	–	–	0.8	–	
Input Voltage Range	CMVR		±10.5	+14.8 –11.5	–	±10.5	+14.8 –11.5	–	±10.3	+14.8 –11.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	86	100	–	86	100	–	82	96	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	86	100	–	86	100	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	82	100	–	
Input Noise Voltage Density	e_n	f_O = 100Hz	–	20	–	–	20	–	–	20	–	nV/√Hz
		f_O = 1000Hz	–	15	–	–	15	–	–	15	–	
Input Noise Current Density	i_n	f_O = 100Hz	–	0.01	–	–	0.01	–	–	0.01	–	pA/√Hz
		f_O = 1000Hz	–	0.01	–	–	0.01	–	–	0.01	–	
Input Capacitance	C_{IN}		–	3.0	–	–	3.0	–	–	3.0	–	pF
The following specifications apply for V_S = ±15V, –55°C ≤ T_A ≤ +125°C, unless otherwise noted.												
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.4	0.9	–	0.7	2.0	–	0.9	4.5	mV
Average Input Offset Voltage Drift											(Note 3)	
Without External Trim	TCV_{OS}		–	2.0	5.0	–	3.0	10	–	4.0	15	μV/°C
With External Trim	TCV_{OSn}	R_P = 100KΩ	–	2.0	–	–	3.0	–	–	4.0	–	
Input Offset Current	I_{OS}	T_J = 125°C (Note 1)	–	0.6	4.0	–	0.80	6.0	–	1.0	9.0	nA
		T_A = 125°C	–	1.0	8.5	–	1.3	14.5	–	1.7	22	
		Device Operating										
Input Bias Current	I_B	T_J = 125°C (Note 1)	–	1.2	5.0	–	1.5	7.5	–	1.8	10	nA
		T_A = 125°C	–	2.0	11	–	2.5	18	–	3.0	25	
		Device Operating										
Input Voltage Range	CMVR		±10.4	+14.6 –11.3	–	±10.4	+14.6 –11.3	–	±10.25	+14.6 –11.3	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	97	–	85	97	–	80	93	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	85	97	–	85	97	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	80	93	–	
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K$, V_S = ±10V	35	120	–	30	110	–	25	100	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10K\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V

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ELECTRICAL CHARACTERISTICS			OP-16E			OP-16F			OP-16G			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.												
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.2	0.5	–	0.4	1.0	–	0.5	3.0	mV
Input Offset Current	I_{OS}	T_J = 25°C (Note 1)	–	3.0	10	–	3.0	20	–	3.0	50	pA
		Device Operating	–	5.0	25	–	5.0	50	–	5.0	125	
Input Bias Current	I_B	T_J = 25°C (Note 1)	–	15	50	–	15	100	–	15	200	pA
		Device Operating	–	20	130	–	20	250	–	20	500	
Input Resistance	R_{in}		–	10^{12}	–	–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K\Omega$, V_O = ±10V	100	240	–	75	220	–	50	200	–	V/mV
Output Voltage Swing	V_{OM}	R_L = 10K	±12	±13	–	±12	±13	–	±12	±13	–	V
			±11	±12.7	–	±11	±12.7	–	±11	±12.7	–	
Supply Current	I_{SY}		–	4.6	7.0	–	4.6	7.0	–	4.8	8.0	mA
Slew Rate	SR	A_{VCL} = +1.0	18	25	–	12	24	–	9.0	23	–	V/μsec
Gain Bandwidth Product	GBW		6.0	8.0	–	5.5	7.6	–	5.0	7.2	–	MHz
Closed Loop Bandwidth	CLBW	A_{VCL} = +1.0	–	19	–	–	18	–	–	17	–	MHz
Settling Time	t_S	to 0.01%	–	1.7	–	–	1.7	–	–	1.8	–	μs
		to 0.05% (Note 2)	–	0.9	–	–	0.9	–	–	1.0	–	
		to 0.10%	–	0.7	–	–	0.7	–	–	0.8	–	
Input Voltage Range	CMVR		±10.5	+14.8 −11.5	–	±10.5	+14.8 −11.5	–	±10.3	+14.8 −11.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	86	100	–	86	100	–	82	96	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	86	100	–	86	100	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	82	100	–	
Input Noise Voltage Density	e_n	f_O = 100Hz	–	20	–	–	20	–	–	20	–	nV/√Hz
		f_O = 1000Hz	–	15	–	–	15	–	–	15	–	
Input Noise Current Density	i_n	f_O = 100Hz	–	0.01	–	–	0.01	–	–	0.01	–	pA/√Hz
		f_O = 1000Hz	–	0.01	–	–	0.01	–	–	0.01	–	
Input Capacitance	C_{IN}		–	3.0	–	–	3.0	–	–	3.0	–	pF
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.												
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.3	0.75	–	0.55	1.5	–	0.7	3.8	mV
Average Input Offset Voltage Drift											(Note 3)	
Without External Trim	TCV_{OS}		–	2.0	5.0	–	3.0	10	–	4.0	15	μV/°C
With External Trim	TCV_{OSn}	R_P = 100KΩ	–	2.0	–	–	3.0	–	–	4.0	–	
Input Offset Current	I_{OS}	T_J = +70°C (Note 1)	–	0.04	0.30	–	0.06	0.45	–	0.08	0.65	nA
		T_A = +70°C Device Operating	–	0.07	0.70	–	0.10	1.1	–	0.15	1.7	
Input Bias Current	I_B	T_J = +70°C (Note 1)	–	0.10	0.40	–	0.12	0.60	–	0.14	0.80	nA
		T_A = +70°C Device Operating	–	0.15	0.90	–	0.20	1.4	–	0.25	2.0	
Input Voltage Range	CMVR		±10.4	+14.7 −11.4	–	±10.4	+14.7 −11.4	–	±10.25	+14.7 −11.4	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	98	–	85	98	–	80	94	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	85	98	–	85	98	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	80	94	–	
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K$, V_S = ±10V	65	200	–	50	180	–	35	160	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10K\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V

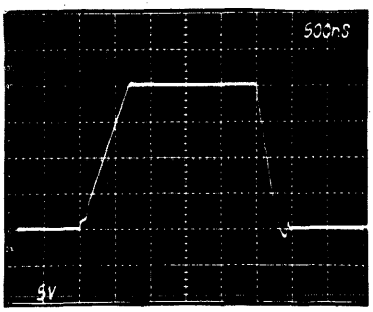
NOTE 1: Due to limited production test times the bias currents correspond to junction temperatures. The bias current vs. time (after power-on) curve clarifies this point. Since most amplifiers (in use) are on for more than 1 second, PMI also specifies the bias current for the warmed-up condition. The warmed-up bias current value is correlated to the junction temp. value via the curves of I_B vs. T_J and I_B vs. T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at V_{CM} = 0.

NOTE 2: Settling time is defined here for a unity gain inverter connection using 2KΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.

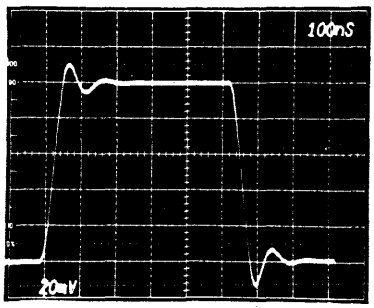
NOTE 3: Parameter is not 100% tested. 90% of all units meet these specifications.

TYPICAL PERFORMANCE CURVES

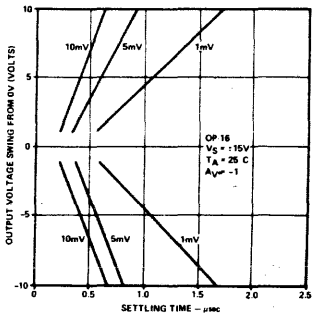
LARGE SIGNAL TRANSIENT RESPONSE



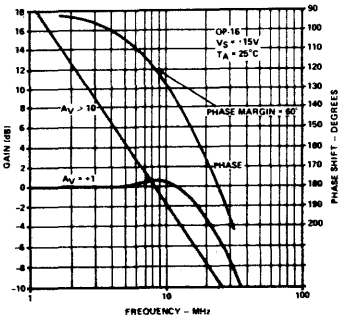
SMALL SIGNAL TRANSIENT RESPONSE



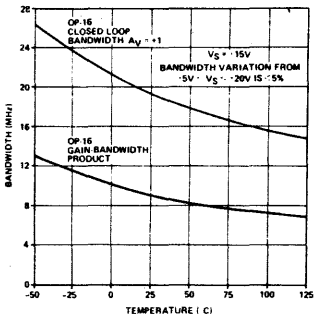
SETTLING TIME



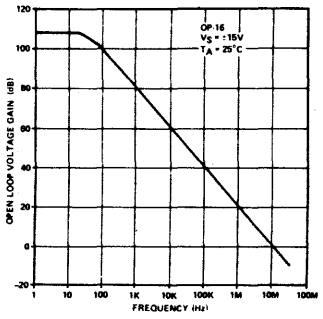
CLOSED LOOP BANDWIDTH AND PHASE SHIFT VS FREQUENCY



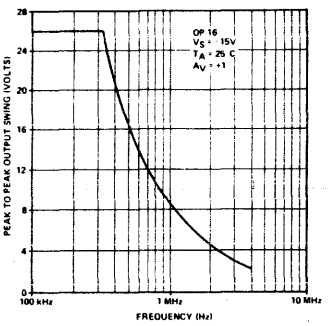
BANDWIDTH VS TEMPERATURE



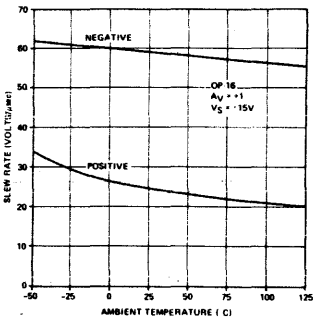
OPEN LOOP FREQUENCY RESPONSE



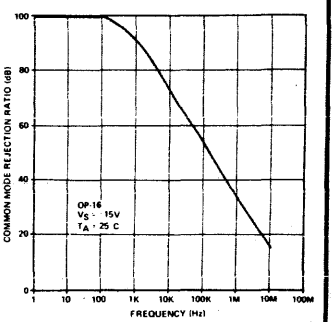
UNDISTORTED OUTPUT SWING



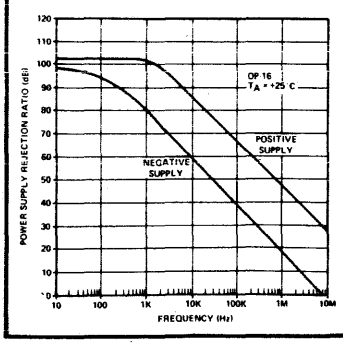
SLEW RATE VS TEMPERATURE



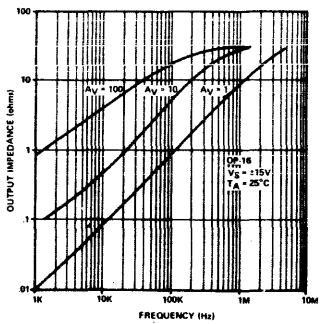
COMMON MODE REJECTION RATIO VS FREQUENCY



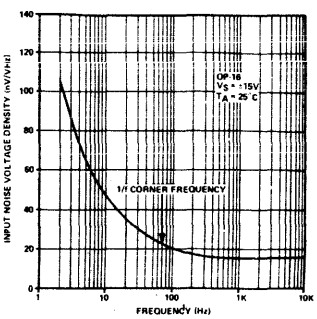
POWER SUPPLY REJECTION VS FREQUENCY



OUTPUT IMPEDANCE VS FREQUENCY



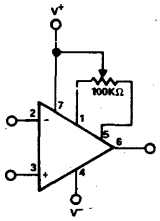
VOLTAGE NOISE VS FREQUENCY



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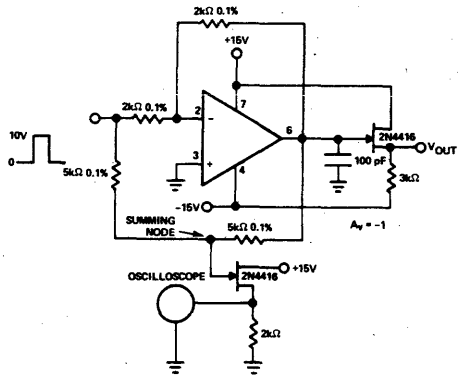
BASIC CONNECTIONS

INPUT OFFSET VOLTAGE NULLING



NOTE: V_{OS} CAN BE TRIMMED WITH POTENTIOMETERS RANGING FROM 10KΩ TO 1MΩ. FOR MOST UNITS TCV_{OS} WILL BE MINIMUM WHEN V_{OS} IS ADJUSTED WITH A 100KΩ POTENTIOMETER.

SETTLING TIME TEST CIRCUIT



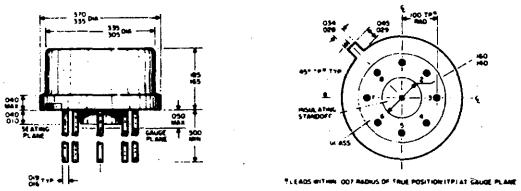
APPLICATION INFORMATION

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

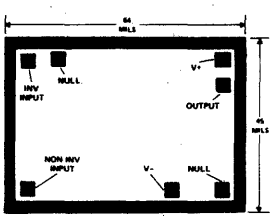
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

PACKAGE DIMENSIONS



TO-99 (J)

CHIP DIMENSIONS



SPECIFICATION COMPARISON TABLE (OP-16 VS. LF156)

		-55°C/+125°C MODELS					0°C/+70°C MODELS				
SPECIFICATION	CONDITION	OP-16A	LF156A	OP-16B	OP-16C	LF156	OP-16E	LF356A	OP-16F	OP-16G	LF356
MAX Input Offset Voltage	T_A=25°C	0.5mV	2.0mV	1.0mV	3.0mV	5.0mV	0.5mV	2.0mV	1.0mV	3.0mV	10mV
MAX Input Offset Voltage	T_A=Full	0.9mV	2.5mV	2.0mV	4.5mV	7.0mV	0.75mV	2.3mV	1.5mV	3.8mV	13mV
MAX Input Offset Voltage Drift	T_A=Full	5μV/°C	5μV/°C	10μV/°C	15μV/°C	NO SPEC	5μV/°C	5μV/°C	10μV/°C	15μV/°C	NO SPEC
MAX Input Bias Current	T_j=25°C	50pA	50pA	100pA	200pA	100pA	50pA	50pA	100pA	200pA	200pA
MAX Input Bias Current	T_A=25°C (Note)	130pA	NO SPEC	250pA	500pA	NO SPEC	130pA	NO SPEC	250pA	500pA	NO SPEC
MAX Input Bias Current	T_j=Full	5.0nA	25nA	7.5nA	10nA	50nA	0.4nA	5nA	0.6nA	0.8nA	8nA
MAX Input Bias Current	T_A=Full (Note)	11nA	NO SPEC	18nA	25nA	NO SPEC	0.9nA	NO SPEC	1.4nA	2.0nA	NO SPEC
MIN Slew Rate	T_A=25°C A_V=+1	18V/μsec	10V/μsec	12V/μsec	9V/μsec	7.5V/μsec	18V/μsec	10V/μsec	12V/μsec	9V/μsec	NO SPEC
MAX Supply Current	T_A=25°C	7.0mA	7.0mA	7.0mA	8.0mA	7.0mA	7.0mA	10mA	7.0mA	8.0mA	10mA

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IMPROVED PM157A

OP-17

PRECISION JFET INPUT OPERATIONAL AMPLIFIER

WIDE BANDWIDTH DECOMPENSATED (AV_{MIN} = 5)

GENERAL DESCRIPTION

With an unusual performance combination of 400nsec settling time and an input offset voltage of 500μV MAX., the OP-17 clearly outperforms the 157A op amp. In addition, the OP-17 is superior in both cost and performance to several dielectrically-isolated and hybrid op amps. Bias current compensation provides low input bias current at elevated temperatures.

The OP-17 was designed to provide real precision performance along with its high speed. For example the 500μV offset voltage yields less than 1/2 LSB error in a 12 bit, 5V DAC. Although the OP-17 can be nulled, the design objective was to provide low offset voltage and drift WITHOUT NULLING. Systems become MORE COST-EFFECTIVE as the number of error correcting "knobs" decrease. PMI achieves this performance by use of an improved BI-FET process coupled with on-chip zener-zap offset trimming.

Most high speed monolithic op amps give settling time specifications to 0.01% error band, and so does PMI. Since 0.01% of 10V is 1mV, it is surprising that these same op amps have offset voltage errors in the 0.02% to 0.3% range. A large number of applications are in the 0.05% to 0.1% range, and PMI also gives specs for these error bands in its settling times. The fact that 500μV is only 0.005% of 10V is why PMI specifies settling time to a true 0.01% error band.

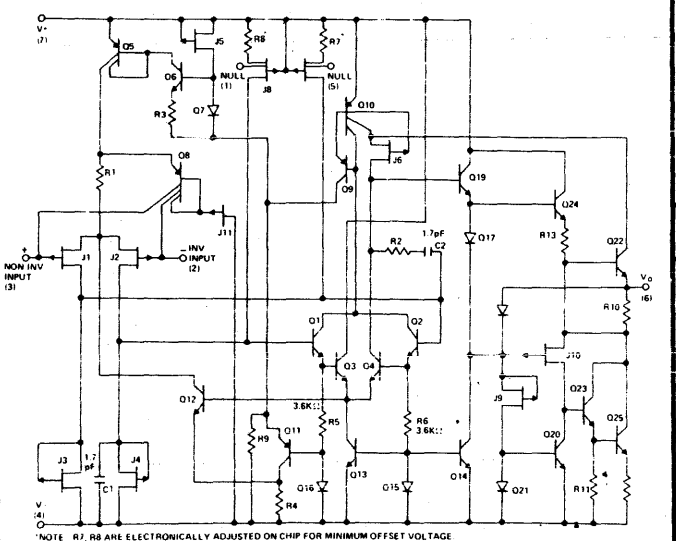
The combination of low input offset voltage of 500μV MAX., slew rate of 70V/μsec, and settling time of 400nsec—to 0.1%—makes the OP-17 a true precision, high speed op amp. Because of the input bias current compensation, the maximum input bias current at 125°C ambient (not junction) temperature is only 11nA. This kind of performance makes the OP-17 useful in a wide range of applications.

Applications include high speed amplifiers for current output DAC's, active filters, and photocell amplifiers. For unity gain fast follower applications see the OP-15 and OP-16 precision JFET op amp data sheets.

FEATURES

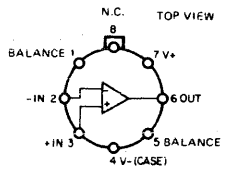
- High Slew Rate 70V/μs
- Fast Settling to ±0.1% . . . . . 400 nsec
- Low Input Offset Voltage . . . . . 500 μV MAX
- Low Input Offset Voltage Drift . . . . . 2.0 μV/°C
- Big Gain Bandwidth Product . . . . . 30 MHz
- Minimum Slew Rate Guaranteed on All Models
- Temperature Compensated Input Bias Currents*
- Guaranteed Input Bias Current @ 125°C. .11nA MAX
- Bias Current Specified WARMED UP Over Temp.
- Internal Compensation
- Low Input Noise Current . . . . . 0.01 pA $\sqrt{Hz}$
- High Common Mode Rejection Ratio 100dB
- Models with MIL-STD-883A Class B Processing Available From Stock

SIMPLIFIED SCHEMATIC DIAGRAM



NOTE: R7, R8 ARE ELECTRONICALLY ADJUSTED ON CHIP FOR MINIMUM OFFSET VOLTAGE

PIN CONNECTIONS



TO-99 (J Suffix)

ORDERING INFORMATION

ORDER: OP-17AJ, OP-17BJ, OP-17CJ	−55°C TO +125°C
OP-17EJ, OP-17FJ, OP-17GJ	0°C TO +70°C

Military Temperature Range Devices With MIL-STD-883A Class B Processing:

ORDER: OP17-883-AJ
OP17-883-BJ
OP17-883-CJ

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- OP-17A, OP-17B, OP-17E, OP-17F: ±22V
- OP-17C, OP-17G: ±18V

Internal Power Dissipation
- All Devices: 500mW
  - (The TO-99(J) package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.)

Operating Temperature Range
- OP-17A, OP-17B, OP-17C: –55°C to +125°C
- OP-17E, OP-17F, OP-17G: 0°C to +70°C

Maximum Junction Temperature (T_J)
- All Devices: +150°C

Differential Input Voltage
- OP-17A, OP-17B, OP-17E, OP-17F: ±40V
- OP-17C, OP-17G: ±30V

Input Voltage
- OP-17A, OP-17B, OP-17E, OP-17F: ±20V
- OP-17C, OP-17G: ±16V
  - (Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.)

Output Short Circuit Duration: Indefinite

Storage Temperature Range: –65°C to +150°C

Lead Temperature Range (Soldering, 60 sec): +300°C

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	OP-17A Min	OP-17A Typ	OP-17A Max	OP-17B Min	OP-17B Typ	OP-17B Max	OP-17C Min	OP-17C Typ	OP-17C Max	Units
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.2	0.5	–	0.4	1.0	–	0.5	3.0	mV
Input Offset Current	I_{OS}	T_J = 25°C (Note 1)	–	3.0	10	–	3.0	20	–	3.0	50	pA
		Device Operating	–	5.0	25	–	5.0	50	–	5.0	125	
Input Bias Current	I_B	T_J = 25°C (Note 1)	–	15	50	–	15	100	–	15	200	pA
		Device Operating	–	20	130	–	20	250	–	20	500	
Input Resistance	R_{in}		–	10^{12}	–	–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K\Omega$, V_S = ±10V	100	240	–	75	220	–	50	200	–	V/mV
Output Voltage Swing	V_{OM}	R_L = 10K	±12	±13	–	±12	±13	–	±12	±13	–	V
		R_L = 2K	±11	±12.7	–	±11	±12.7	–	±11	±12.7	–	
Supply Current	I_{SY}		–	4.6	7.0	–	4.6	7.0	–	4.8	8.0	mA
Slew Rate	SR	A_{VCL} = +5.0	45	70	–	35	66	–	25	62	–	V/μsec
Gain Bandwidth Product	GBW		20	30	–	15	28	–	11	26	–	MHz
Closed Loop Bandwidth	CLBW	A_{VCL} = +5.0	–	11	–	–	10	–	–	9	–	MHz
Settling Time	t_s	to 0.01%	–	1.5	–	–	1.5	–	–	1.6	–	μs
		to 0.05% (Note 2)	–	0.5	–	–	0.5	–	–	0.6	–	
		to 0.10%	–	0.4	–	–	0.4	–	–	0.5	–	
Input Voltage Range	CMVR		±10.5	+14.8 –11.5	–	±10.5	+14.8 –11.5	–	±10.3	+14.8 –11.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	86	100	–	86	100	–	82	96	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	86	100	–	86	100	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	82	100	–	
Input Noise Voltage Density	e_n	f_O = 100Hz	–	20	–	–	20	–	–	20	–	nV/√Hz
		f_O = 1000Hz	–	15	–	–	15	–	–	15	–	
Input Noise Current Density	i_n	f_O = 100Hz	–	0.01	–	–	0.01	–	–	0.01	–	pA/√Hz
		f_O = 1000Hz	–	0.01	–	–	0.01	–	–	0.01	–	
Input Capacitance	C_{IN}		–	3.0	–	–	3.0	–	–	3.0	–	pF
The following specifications apply for V_S = ±15V, –55°C ≤ T_A ≤ +125°C, unless otherwise noted.												
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.4	0.9	–	0.7	2.0	–	0.9	4.5	mV
Average Input Offset Voltage Drift											(Note 3)	
Without External Trim	TCV_{OS}		–	2.0	5.0	–	3.0	10	–	4.0	15	μV/°C
With External Trim	TCV_{OSn}	R_P = 100KΩ	–	2.0	–	–	3.0	–	–	4.0	–	
Input Offset Current	I_{OS}	T_J = 125°C (Note 1)	–	0.6	4.0	–	0.8	6.0	–	1.0	9.0	nA
		T_A = 125°C	–	1.0	8.5	–	1.3	14.5	–	1.7	22	
		Device Operating										
Input Bias Current	I_B	T_J = 125°C (Note 1)	–	1.2	5.0	–	1.5	7.5	–	1.8	10	nA
		T_A = 125°C	–	2.0	11	–	2.5	18	–	3.0	25	
		Device Operating										
Input Voltage Range	CMVR		±10.4	+14.6 –11.3	–	±10.4	+14.6 –11.3	–	±10.25	+14.6 –11.3	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	97	–	85	97	–	80	93	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	85	97	–	85	97	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	80	93	–	
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K$, V_S = ±10V	35	120	–	30	110	–	25	100	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10K\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V

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ELECTRICAL CHARACTERISTICS			OP-17E			OP-17F			OP-17G			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.												
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.2	0.5	–	0.4	1.0	–	0.5	3.0	mV
Input Offset Current	I_{OS}	T_J = 25°C (Note 1)	–	3.0	10	–	3.0	20	–	3.0	50	pA
		Device Operating	–	5.0	25	–	5.0	50	–	5.0	125	
Input Bias Current	I_B	T_J = 25°C (Note 1)	–	15	50	–	15	100	–	15	200	pA
		Device Operating	–	20	130	–	20	250	–	20	500	
Input Resistance	R_{in}		–	10^{12}	–	–	10^{12}	–	–	10^{12}	–	Ω
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K\Omega$, V_O = ±10V	100	240	–	75	220	–	50	200	–	V/mV
Output Voltage Swing	V_{OM}	R_L = 10K	±12	±13	–	±12	±13	–	±12	±13	–	V
		R_L = 2K	±11	±12.7	–	±11	±12.7	–	±11	±12.7	–	
Supply Current	I_{SY}		–	4.6	7.0	–	4.6	7.0	–	4.8	8.0	mA
Slew Rate	SR	A_{VCL} = +5.0	45	70	–	35	66	–	25	62	–	V/μsec
Gain Bandwidth Product	GBW		20	30	–	15	28	–	11	26	–	MHz
Closed Loop Bandwidth	CLBW	A_{VCL} = +5.0	–	11	–	–	10	–	–	9	–	MHz
Settling Time	t_s	TO 0.01%	–	1.5	–	–	1.5	–	–	1.6	–	μs
		TO 0.05% (Note 2)	–	0.5	–	–	0.5	–	–	0.6	–	
		TO 0.10%	–	0.4	–	–	0.4	–	–	0.5	–	
Input Voltage Range	CMVR		±10.5	+14.8 −11.5	–	±10.5	+14.8 −11.5	–	±10.3	+14.8 −11.5	–	V
Common Mode Rejection Ratio	CMRR	V_{CM}= ±CMVR	86	100	–	86	100	–	82	96	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	86	100	–	86	100	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	82	100	–	
Input Noise Voltage Density	e_n	f_O = 100Hz	–	20	–	–	20	–	–	20	–	nV/√Hz
		f_O = 1000Hz	–	15	–	–	15	–	–	15	–	
Input Noise Current Density	i_n	f_O = 100Hz	–	0.01	–	–	0.01	–	–	0.01	–	pA/√Hz
		f_O = 1000Hz	–	0.01	–	–	0.01	–	–	0.01	–	
Input Capacitance	C_{IN}		–	3.0	–	–	3.0	–	–	3.0	–	pF
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.												
Input Offset Voltage	V_{OS}	R_S = 50Ω	–	0.3	0.75	–	0.55	1.5	–	0.7	3.8	mV
Average Input Offset Voltage Drift											(Note 3)	
Without External Trim	TCV_{OS}		–	2.0	5.0	–	3.0	10	–	4.0	15	μV/°C
With External Trim	TCV_{OSn}	R_P = 100KΩ	–	2.0	–	–	3.0	–	–	4.0	–	
Input Offset Current	I_{OS}	T_J = +70°C (Note 1)	–	0.04	0.30	–	0.06	0.45	–	0.08	0.65	nA
		T_A = +70°C Device Operating	–	0.07	0.70	–	0.10	1.1	–	0.15	1.7	
Input Bias Current	I_B	T_J = +70°C (Note 1)	–	0.10	0.40	–	0.12	0.60	–	0.14	0.80	nA
		T_A = +70°C Device Operating	–	0.15	0.90	–	0.20	1.4	–	0.25	2.0	
Input Voltage Range	CMVR		±10.4	+14.7 −11.4	–	±10.4	+14.7 −11.4	–	±10.25	+14.7 −11.4	–	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	85	98	–	85	98	–	80	94	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	85	98	–	85	98	–	–	–	–	dB
		V_S = ±10V to ±15V	–	–	–	–	–	–	80	94	–	
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2K$, V_S = ±10V	65	200	–	50	180	–	35	160	–	V/mV
Maximum Output Voltage Swing	V_{OM}	$R_L \geq 10K\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V

NOTE 1: Due to limited production test times the bias currents correspond to junction temperatures. The bias current vs. time (after power-on) curve clarifies this point. Since most amplifiers (in use) are on for more than 1 second, PMI also specifies the bias current for the warmed-up condition. The warmed-up bias current value is correlated to the junction temp. value via the curves of I_B vs. T_J and I_B vs. T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at V_{CM} = 0.

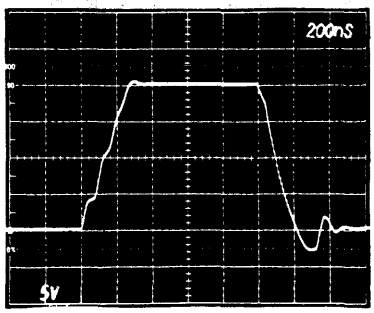
NOTE 2: Settling time is defined here for a gain of five inverter connection using 2KΩ and 400Ω resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.

NOTE 3: Parameter is not 100% tested. 90% of all units meet these specifications.

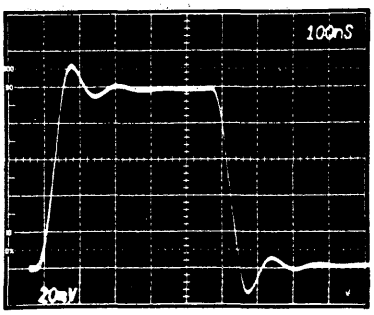
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TYPICAL PERFORMANCE CURVES

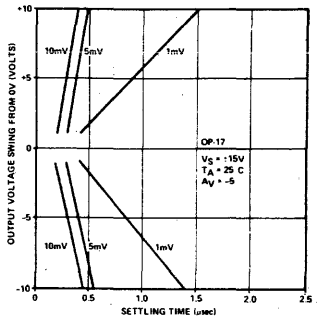
LARGE SIGNAL TRANSIENT RESPONSE



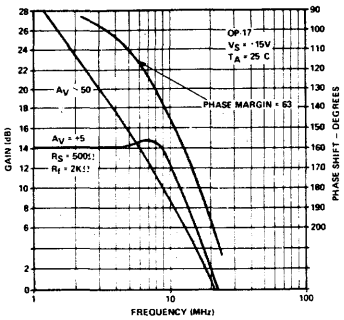
SMALL SIGNAL TRANSIENT RESPONSE



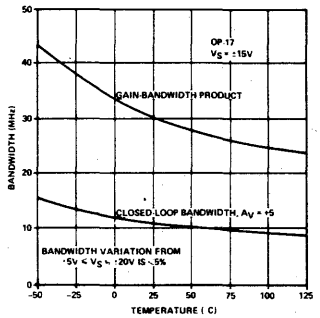
SETTLING TIME



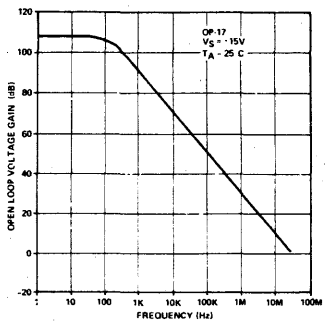
CLOSED LOOP BANDWIDTH AND PHASE SHIFT VS FREQUENCY



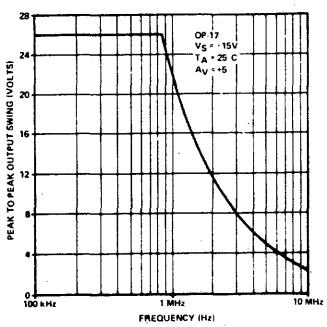
BANDWIDTH VS TEMPERATURE



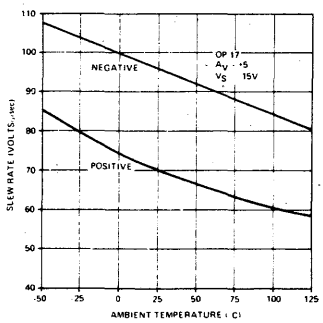
OPEN LOOP FREQUENCY RESPONSE



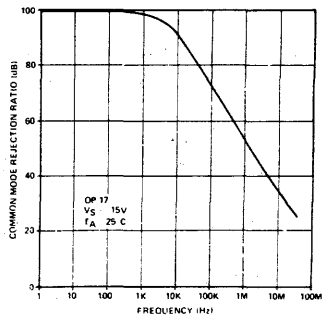
UNDISTORTED OUTPUT SWING



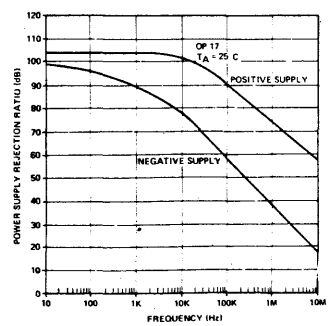
SLEW RATE VS TEMPERATURE



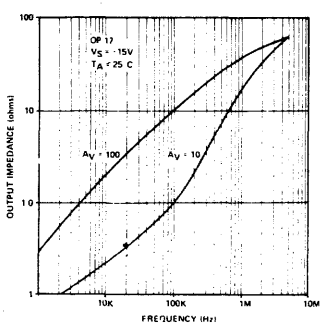
COMMON MODE REJECTION RATIO VS FREQUENCY



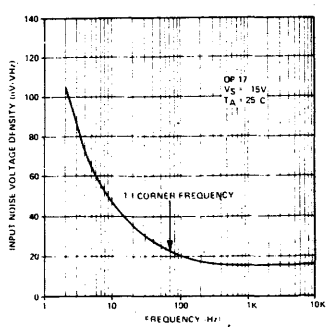
POWER SUPPLY REJECTION VS FREQUENCY



OUTPUT IMPEDANCE VS FREQUENCY

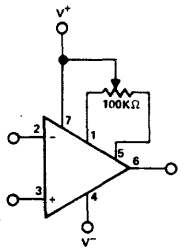


VOLTAGE NOISE VS FREQUENCY



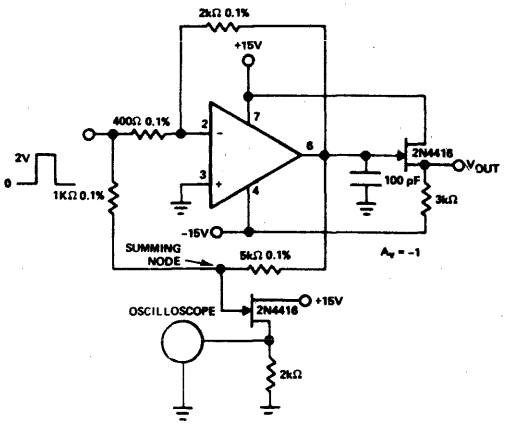
BASIC CONNECTIONS

INPUT OFFSET VOLTAGE NULLING



NOTE: V_{OS} CAN BE TRIMMED WITH POTENTIOMETERS RANGING FROM 10KΩ TO 1MΩ. FOR MOST UNITS TCV_{OS} WILL BE MINIMUM WHEN V_{OS} IS ADJUSTED WITH A 100KΩ POTENTIOMETER.

SETTLING TIME TEST CIRCUIT



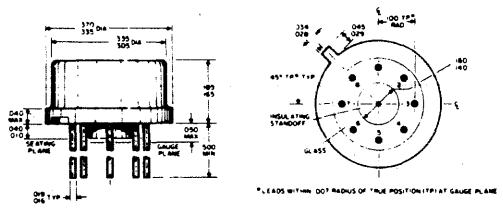
APPLICATION INFORMATION

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

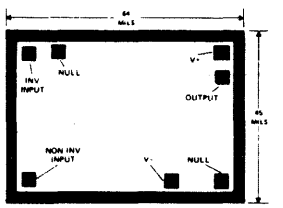
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

PACKAGE DIMENSIONS



TO-99 (J)

CHIP DIMENSIONS



SPECIFICATION COMPARISON TABLE (OP-17 VS. LF157)

		-55°C/+125°C MODELS					0°C/+70°C MODELS				
SPECIFICATION	CONDITION	OP-17A	LF157A	OP-17B	OP-17C	LF157	OP-17E	LF357A	OP-17F	OP-17G	LF357
MAX Input Offset Voltage	T_A=25°C	0.5mV	2.0mV	1.0mV	3.0mV	5.0mV	0.5mV	2.0mV	1.0mV	3.0mV	10mV
MAX Input Offset Voltage	T_A=Full	0.9mV	2.5mV	2.0mV	4.5mV	7.0mV	0.75mV	2.3mV	1.5mV	3.8mV	13mV
MAX Input Offset Voltage Drift	T_A=Full	5μV/°C	5μV/°C	10μV/°C	15μV/°C	NO SPEC	5μV/°C	5μV/°C	10μV/°C	15μV/°C	NO SPEC
MAX Input Bias Current	T_j=25°C	50pA	50pA	100pA	200pA	100pA	50pA	50pA	100pA	200pA	200pA
MAX Input Bias Current	T_A=25°C (Note)	130pA	NO SPEC	250pA	500pA	NO SPEC	130pA	NO SPEC	250pA	500pA	NO SPEC
MAX Input Bias Current	T_j=Full	5.0nA	25nA	7.5nA	10nA	50nA	0.4nA	5nA	0.6nA	0.8nA	8nA
MAX Input Bias Current	T_A=Full (Note)	11nA	NO SPEC	18nA	25nA	NO SPEC	0.9nA	NO SPEC	1.4nA	2.0nA	NO SPEC
MIN Slew Rate	T_A=25°C A_V=+5	45V/μsec	40V/μsec	35V/μsec	25V/μsec	30V/μsec	45V/μsec	40V/μsec	35V/μsec	25V/μsec	NO SPEC
MAX Supply Current	T_A=25°C	7.0mA	7.0mA	7.0mA	8.0mA	7.0mA	7.0mA	10mA	7.0mA	8.0mA	10mA

NOTE: Warmed up bias current.

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MAT-01

ULTRA-MATCHED MONOLITHIC DUAL TRANSISTOR

EXCELLENT LOG CONFORMANCE

GENERAL DESCRIPTION

The MAT-01 series are monolithic ultra-tightly matched dual NPN transistors, fabricated using an exclusive Silicon Nitride "Triple-Passivation" process which provides extreme stability of critical parameters versus both temperature and time. Outstanding matching characteristics include offset voltages of 40μV, temperature drift of V_{OS} of 0.15μV/°C and h_{FE} matching of 0.7%. Very high h_{FE} is provided over a six decade range of collector current, including an exceptional h_{FE} of 590 @ I_C = 10**nano** amperes! Excellent logarithmic conformance over a seven decade collector current span suggests application in log/antilog and multiplier/divider circuitry. The very low values of noise voltage and current make the MAT-01 ideal for usage in critical low-level input stages while the 6 pin TO-99 package allows direct replacement of most previous dual transistors for immediate performance improvements. The very high h_{FE} at low collector currents also makes the MAT-01 attractive in all high impedance and micropower circuit designs.

FEATURES

- **Tight V_{OS} (V_{BE} Match) . . . . 40μV Typ, 100μV Max**
- **Low TC V_{OS} . . . . . 0.15μV/°C Typ, 0.5μV/°C Max**
- **Tight h_{FE} Match . . . . . 0.7% Typ, 3.0% Max**
- **High h_{FE} . . . . . 770 Typ, 500 Min**
- **Excellent h_{FE} Linearity from 10nA to 10mA**
- **High h_{FE} at Low I_C . . . . . 590 Typ @ I_C = 10nA**
- **Low Noise Voltage . . . . 0.23μVp-p — 0.1Hz to 10Hz**
- **Excellent Long Term Stability . . 0.2μV/Month, Typ**
- **High Breakdowns . . . . . 45V and 60V Min**
- **Precision Logarithmic Conformance**
- **Direct Replacement for Most Dual Transistors**

ABSOLUTE MAXIMUM RATINGS

	MAT-01 AH, GH	MAT-01 H, FH
Collector-Base Voltage (BV_{CBO})	45V	60V
Collector-Emitter Voltage (BV_{CEO})	45V	60V
Collector-Collector Voltage (BV_{CC})	45V	60V
Emitter-Emitter Voltage (BV_{EE})	45V	60V
Emitter-Base Voltage (BV_{EBO}) (Note 1)	5V	5V
Collector Current (I_C)	25mA	25mA
Emitter Current (I_E)	25mA	25mA

	MAT-01 AH, GH	MAT-01 H, FH
Total Power Dissipation		
Case Temperature ≤ 40°C (Note 2)	1.8W	1.8W
Ambient Temperature ≤ 70°C (Note 3)	500mW	500mW
Operating Ambient Temperature	−55°C to +125°C	
Operating Junction Temperature	−55°C to +150°C	
Storage Temperature	−65°C to +150°C	
Lead Temperature (Soldering, 60 sec.)	300°C	

NOTES

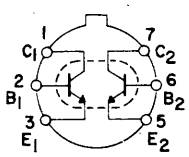
Note 1: Application of reverse bias voltages in excess of rating shown can result in degradation of h_{FE} and h_{FE} matching characteristics. Do not attempt to measure BV_{EBO} greater than the 5V rating shown.

Note 2: Rating applies to applications using heat sinking to control case temperature. Derate linearly at 16.4mW/°C for case temperatures above 40°C.

Note 3: Rating applies to applications not using heat sinking; device in free air only. Derate linearly at 6.3mW/°C for ambient temperatures above 70°C.

PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



Note: Substrate is connected to case.

ORDER: MAT-01AH
MAT-01H
MAT-01FH
MAT-01GH

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:

ORDER: MAT01-883-AH
MAT01-883-H
MAT01-883-FH
MAT01-883-GH

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ELECTRICAL CHARACTERISTICS

These specifications apply for V_{CB} = 15V, I_C = 10μA, T_A = 25°C, unless otherwise noted.

			MAT-01H			MAT-01FH			
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Breakdown Voltage	BV_{CEO}		60	–	–	60	–	–	V
Offset Voltage	V_{os}		–	0.04	0.1	–	0.10	0.50	mV
Offset Voltage Stability									
First Month	V_{os}/Time	(Note 1)	–	2.0	–	–	2.0	–	μV/Month
Long Term	V_{os}/Time	(Note 2)	–	0.2	–	–	0.2	–	μV/Month
Offset Current	I_{os}		–	0.1	0.8	–	0.2	3.2	nA
Bias Current	I_B	–	–	15	30	–	18	40	nA
Current Gain	h_{FE}	I_C = 10nA	–	520	–	–	430	–	
	h_{FE}	I_C = 10μA	330	680	–	250	560	–	
	h_{FE}	I_C = 10mA	–	740	–	–	610	–	
Current Gain Match	Δh_{FE}		–	0.7	2.7	–	1.0	8.0	%
	Δh_{FE}	100nA ≤ I_C ≤ 10mA	–	0.8	–	–	1.2	–	%
Low Frequency Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	–	0.23	0.4	–	0.23	0.4	μVp-p
Broadband Noise Voltage	e_{nRMS}	1Hz to 10kHz	–	0.60	–	–	0.60	–	μV_{RMS}
Narrowband Noise Voltage Density	e_n	f_o = 10Hz (Note 3)	–	7.0	9.0	–	7.0	9.0	nV/√Hz
		f_o = 100Hz (Note 3)	–	6.1	7.6	–	6.1	7.6	nV/√Hz
		f_o = 1000Hz (Note 3)	–	6.0	7.5	–	6.0	7.5	nV/√Hz
Offset Voltage Change	$\Delta V_{os}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 45V	–	0.5	3.0	–	0.8	8.0	μV/V
Offset Current Change	$\Delta I_{os}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 45V	–	2.0	15.0	–	3.0	70	pA/V
Collector-Base Leakage Current	I_{CBO}	V_{CB} = 45V, I_E = 0 (Note 4)	–	15	50	–	25	200	pA
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = 45V, V_{BE} = 0 (Note 4)	–	50	200	–	90	400	pA
Collector-Collector Leakage Current	I_{CC}	V_{CC} = 45	–	20	200	–	30	400	pA
Collector Saturation Voltage	$V_{CE(SAT)}$	I_B = 0.1mA, I_C = 1mA	–	0.12	0.20	–	0.12	0.25	V
	$V_{CE(SAT)}$	I_B = 1mA, I_C = 10mA	–	0.8	–	–	0.8	–	V
Gain-Bandwidth Product	f_T	V_{CE} = 10V, I_C = 10mA	–	450	–	–	450	–	MHz
Output Capacitance	C_{ob}	V_{CE} = 15V, I_E = 0	–	2.8	–	–	2.8	–	pF
Collector-Collector Capacitance	C_{CC}	V_{CC} = 0	–	8.5	–	–	8.5	–	pF
The following specifications apply for V_{CB} = 15V, I_C = 10μA, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.									
Offset Voltage	V_{os}		–	0.06	0.15	–	0.14	0.70	mV
Average Offset Voltage Drift	TCV_{os}	(Note 3)	–	0.15	0.50	–	0.35	1.8	μV/°C
Offset Current	I_{os}		–	0.9	9.0	–	1.5	15.0	nA
Average Offset Current Drift	TCI_{os}	(Note 3)	–	11	110	–	15	150	pA/°C
Bias Current	I_B		–	30	95	–	36	130	nA
Current Gain	h_{FE}		105	350	–	77	300	–	
Collector-Base Leakage Current	I_{CBO}	T_A = 125°C, V_{CB} = 45V, I_E = 0 (Note 4)	–	15	80	–	25	200	nA
Collector-Emitter Leakage Current	I_{CES}	T_A = 125°C, V_{CE} = 45V, V_{BE} = 0 (Note 4)	–	50	300	–	90	400	nA
Collector-Collector Leakage Current	I_{CC}	T_A = 125°C, V_{CC} = 45V	–	30	200	–	50	400	nA

NOTES:

Note 1: Exclude first hour of operation to allow for stabilization of external circuitry.

Note 2: Parameter describes long term average drift trend after first month of operation.

Note 3: Parameter is not 100% tested; 90% of all units meet this specification.

Note 4: The collector-base (I_{CBO}) and collector-emitter (I_{CEO}) leakage currents may be reduced by a factor of two to ten times by connecting the substrate (package) to a potential which is lower than either collector voltage.

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CROSS REFERENCE – MAT-01 TO MONOLITHIC DUAL TRANSISTORS (I_C = 10μA)

DEVICE	BV_{CEO} MIN (V)	V_{os} MAX (mV)	TCV_{os} MAX (μV/°C)	h_{FE} MIN	I_{os} MAX (nA)	TCI_{os} MAX (pA/°C)
MAT-01AH	**45**	**0.1**	**0.5**	**500**	**0.6**	**90**
MAT-01H	**60**	**0.1**	**0.5**	**330**	**0.8**	**110**
MAT-01FH	**60**	**0.5**	**1.8**	**250**	**3.2**	**150**
MAT 01GH	**45**	**0.5**	**1.8**	**250**	**3.2**	**150**
LM114A	45	0.5	2.0	500	2.0	---
LM114	45	2.0	10	250	10	---
LM115A	60	0.5	2.0	250	2.0	---
LM115	60	2.0	10	250	10	---
AD810	35	3.0	15	100	2.0	600
AD811	45	1.5	7.5	200	10	300
AD812	35	1.0	5.0	400	2.5	300
AD813	45	0.5	2.5	200	5	300
AD818	20	1.0	5.0	200	10	300

CROSS REFERENCE – MAT-01 TO 2N TYPES (I_C = 10μA)

DEVICE	BV_{CEO} MIN (V)	V_{os} MAX (mV)	TCV_{os} MAX (μV/°C)	h_{FE} MIN	%h_{FE} MATCH MAX	I_{os} MAX (nA)	TCI_{os} MAX (pA/°C)
MAT-01GH	**45**	**0.5**	**1.8**	**250**	**8**	**3.2**	**150**
2N2639	45	5.0	10	50	10	20	1000
2N2640	45	10	20	50	20	40	2000
2N2642	45	5.0	10	100	10	10	500
2N2643	45	10	20	100	20	20	375
2N2915	45	3.0	10	60	10	17	600
2N2915A	45	2.0	5.0	60	15	26	900
2N2916	45	5.0	10	150	10	7	N.C.
2N2916A	45	2.0	5.0	150	15	10	300
2N2917	45	10	20	60	20	17	1450
2N2918	45	5.0	20	150	20	7	750
MAT-01FH	**60**	**0.5**	**1.8**	**250**	**8**	**3.2**	**150**
2N2919	60	3.0	10	60	10	17	600
2N2919A	60	1.5	5.0	60	10	17	600
2N2920	60	3.0	10	150	10	7	N.C.
2N2920A	60	1.5	5.0	150	10	7	300
2N2060	60	5.0	10	25	10	40	N.C.
2N2060A	60	3.0	5.0	25	10	40	N.C.
2N2060B	60	1.5	5.0	25	10	40	N.C.

Notes: 1. TCI_{os} Max and I_{os} Max calculated from published data.
2. N.C. = Insufficient published data to calculate.
3. All of the above are physically interchangeable pin-for-pin with MAT-01 series.

REF-01

+10V PRECISION VOLTAGE REFERENCE

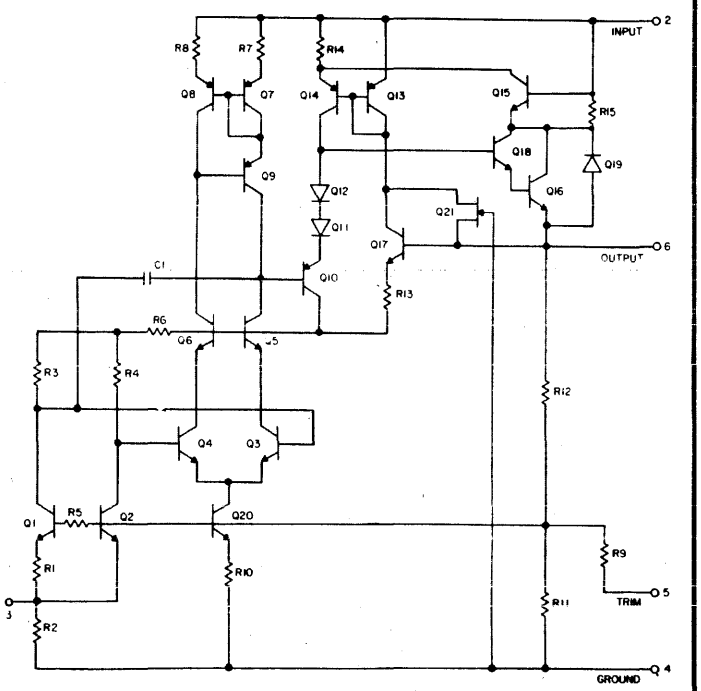
GENERAL DESCRIPTION

The REF-01 Precision Voltage Reference provides a stable +10V output which can be adjusted over a ±3% range with minimal effect on temperature stability. Single supply operation over an input voltage range of 12 to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise and low power make the REF-01 an excellent choice whenever a stable voltage reference is required, such as in D/A and A/D converters, in portable instruments, and in digital voltmeters. Full military temperature range devices with screening to MIL-STD-883A are available.

FEATURES

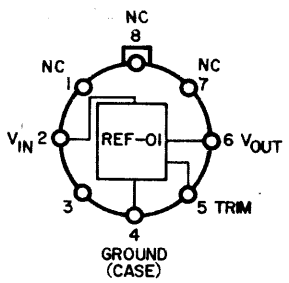
- **Adjustable 10 Volt Output** . . . . . ±3%
- **Excellent Temperature Stability** . . . . . 3 ppm/°C
- **Low Noise** 20μVp-p
- **Low Power** 15mW
- **Wide Input Voltage Range** . . . . . 12 to 40V
- **High Load Driving Capability** 20mA
- **No External Components**
- **Short Circuit Proof**
- **MIL-STD-883A Screening Available**

SIMPLIFIED SCHEMATIC



PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



TO-99 (J-Suffix)

ORDER: REF-01AJ
REF-01J
REF-01EJ
REF-01HJ
REF-01CJ
REF-01DJ

Military Temperature Range Devices
with MIL-STD-883A Class B Processing:

ORDER: REF01-883-AJ
REF01-883-J

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ABSOLUTE MAXIMUM RATINGS

Input Voltage REF-01, A, E, H	40 V
REF-01C, D	30 V
Power Dissipation (see note)	500mW
Output Short Circuit Duration (to ground or V_{IN})	Indefinite
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Operating Temperature Range

REF-01A, REF-01	−55°C to +125°C
REF-01E, REF-01H, REF-01D REF-01C,	0°C to +70°C

Note: Derate at 7.1mW/°C above 80°C ambient temperature.

ELECTRICAL CHARACTERISTICS

			REF-01A			REF-01			
These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Output Voltage	V_O	I_L = 0mA	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	±3.3	–	±3.0	±3.3	–	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	–	20	30	–	20	30	μVp-p
Input Voltage Range	V_{IN}		12	–	40	12	–	40	V
Line Regulation (Note 4)		V_{IN} = 13 to 33V	–	0.006	0.010	–	0.006	0.010	%/V
Load Regulation (Note 4)		I_L = 0 to 10mA	–	0.005	0.008	–	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	–	5.0	–	–	5.0	–	μsec
Quiescent Current	I_{SY}	No Load	–	1.0	1.4	–	1.0	1.4	mA
Load Current	I_L		10	21	–	10	21	–	mA
Sink Current	I_S		−0.3	−0.5	–	−0.3	−0.5	–	mA
Short Circuit Current	I_{SC}	V_O = 0	–	30	–	–	30	–	mA
The following specifications apply for V_{IN} = +15V, −55°C ≤ T_A ≤ +125°C **and I_L = 0mA**, unless otherwise noted.									
Output Voltage Change with Temperature (Notes 1 and 2)	ΔV_{OT}	0°≤T_A≤+70°C	–	0.02	0.06	–	0.07	0.17	%
		−55°≤T_A≤+125°C	–	0.06	0.15	–	0.18	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	–	3	8.5	–	10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	–	0.7	–	–	0.7	–	ppm/%
Line Regulation (V_{IN} = 13 to 33V) (Note 4)		0°≤T_A≤+70°C	–	0.007	0.012	–	0.007	0.012	%/V
		−55°≤T_A≤+125°C	–	0.009	0.015	–	0.009	0.015	%/V
Load Regulation (I_L = 0 to 8mA) (Note 4)		0°≤T_A≤+70°C	–	0.006	0.010	–	0.007	0.012	%/mA
		−55°≤T_A≤+125°C	–	0.007	0.012	–	0.009	0.015	%/mA

NOTE 1: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{10V} \times 100$$

NOTE 2: ΔV_{OT} specification applies trimmed to 10.000V or untrimmed.

NOTE 3: TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e., $TCV_O(0°\text{to}+70°C) = \frac{\Delta V_{OT}\ 0°\text{to}+70°C}{70°C}$

and $TCV_O(-55°\text{to}+125°C) = \frac{\Delta V_{OT}\ -55\ \text{to}+125°C}{180°C}$

NOTE 4: Line and Load Regulation specifications include the effects of self heating.

NOTE 5: Parameter is not 100% tested; 90% of units meet this specification.

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REF-01 DEFINITIONS

LINE REGULATION
The ratio of the change in output voltage to the change in line voltage producing it.

LOAD REGULATION
The ratio of the change in output voltage to the change in load current producing it.

QUIESCENT CURRENT (I_{SY})
The current required from the supply to operate the device with no load.

OUTPUT TURN-ON SETTLING TIME (t_{on})
The time required for the output voltage to reach its final value within a specified error band after application of V_{IN}.

OUTPUT VOLTAGE NOISE (e_{np-p})
The peak to peak output noise voltage in a specified frequency band.

OUTPUT CHANGE WITH TEMPERATURE (ΔV_{OT})
The absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{10V} \times 100$$

OUTPUT TEMPERATURE COEFFICIENT (TCV_O)
The ratio of the output change with temperature to the specified temperature range expressed in ppm/°C.

ELECTRICAL CHARACTERISTICS

			REF-01E			REF-01H			
These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Output Voltage	V_O	I_L = 0mA	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	±3.3	–	±3.0	±3.3	–	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	–	20	30	–	20	30	µVp-p
Input Voltage Range	V_{IN}		12	–	40	12	–	40	V
Line Regulation (Note 4)		V_{IN} = 13 to 33V	–	0.006	0.010	–	0.006	0.010	%/V
Load Regulation (Note 4)		I_L = 0 to 10 mA	–	0.005	0.008	–	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	–	5.0	–	–	5.0	–	µsec
Quiescent Current	I_{SY}	No Load	–	1.0	1.4	–	1.0	1.4	mA
Load Current	I_L		10	21	–	10	21	–	mA
Sink Current	I_S		–0.3	–0.5	–	–0.3	–0.5	–	mA
Short Circuit Current	I_{SC}	V_O = 0	–	30	–	–	30	–	mA
The following specifications apply for V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C and I_L = 0mA, unless otherwise noted.									
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 1 and 2)	–	0.02	0.06	–	0.07	0.17	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	–	3	8.5	–	10	25	ppm/°C
Change in V_O Temperature Coefficient With Output Adjustment		R_p = 10kΩ	–	0.7	–	–	0.7	–	ppm/%
Line Regulation (Note 4)		V_{IN} = 13 to 33V	–	0.007	0.012	–	0.007	0.012	%/V
Load Regulation (Note 4)		I_L = 0 to 8 mA	–	0.006	0.010	–	0.007	0.012	%/mA

NOTE 1: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{10V} \times 100$$

NOTE 2: ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.

NOTE 3: TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e., $TCV_O = \frac{\Delta V_{OT}}{70°C}$

NOTE 4: Line and Load Regulation specifications include the effects of self heating.

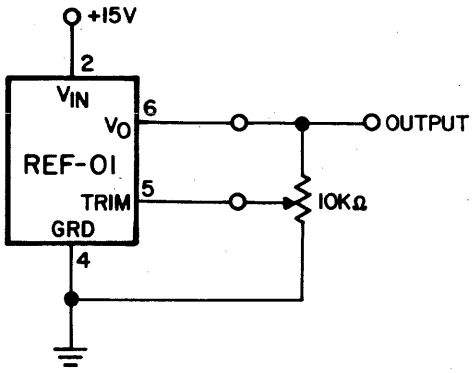
NOTE 5: Parameter is not 100% tested; 90% of units meet this specification.

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OUTPUT ADJUSTMENT

The REF-01 trim terminal can be used to adjust the output voltage over a 10V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V. Of course, the output can also be set to exactly 10.000V, or to 10.240V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. Typically the temperature coefficient change is 0.7 ppm/°C for 100mV of output adjustment.



ELECTRICAL CHARACTERISTICS

			REF-01C			REF-01D			
These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Output Voltage	V_O	I_L = 0mA	9.90	10.00	10.10	9.850	10.00	10.150	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±2.7	±3.3	–	±2.0	±3.3	–	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	–	25	35	–	25	–	μVp-p
Input Voltage Range	V_{IN}		12	–	30	12	–	30	V
Line Regulation (Note 4)		V_{IN} = 13 to 30V	–	0.009	0.015	–	0.012	0.04	%/V
Load Regulation (Note 4)		I_L = 0 to 8 mA	–	0.006	0.015	–	–	–	%/mA
Load Regulation (Note 4)		I_L = 0 to 4 mA	–	0.006	0.015	–	0.009	0.04	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	–	5.0	–	–	5.0	–	μsec
Quiescent Current	I_{SY}	No Load	–	1.0	1.6	–	1.0	2.0	mA
Load Current	I_L		8	21	–	8	21	–	mA
Sink Current	I_S		–0.2	–0.5	–	–0.2	–0.5	–	mA
Short Circuit Current	I_{SC}	V_O = 0	–	30	–	–	30	–	mA
The following specifications apply for V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.									
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 1 and 2)	–	0.14	0.45	–	0.49	–	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	–	20	65	–	70	–	ppm/°C
Change in V_O Temperature Coefficient With Output Adjustment		R_p = 10kΩ	–	0.7	–	–	0.7	–	ppm/%
Line Regulation (Note 4)		V_{IN} = 13 to 30V	–	0.011	0.018	–	0.020	–	%/V
Load Regulation (Note 4)		I_L = 0 to 5 mA	–	0.008	0.018	–	0.020	–	%/mA

NOTE 1: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{10V} \times 100$$

NOTE 2: ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.

NOTE 3: TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e., $TCV_O = \frac{\Delta V_{OT}}{70°C}$

NOTE 4: Line and Load Regulation specifications include the effects of self heating.

NOTE 5: Parameter is not 100% tested; 90% of units meet this specification.

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REF-02

+5V PRECISION VOLTAGE REFERENCE/THERMOMETER

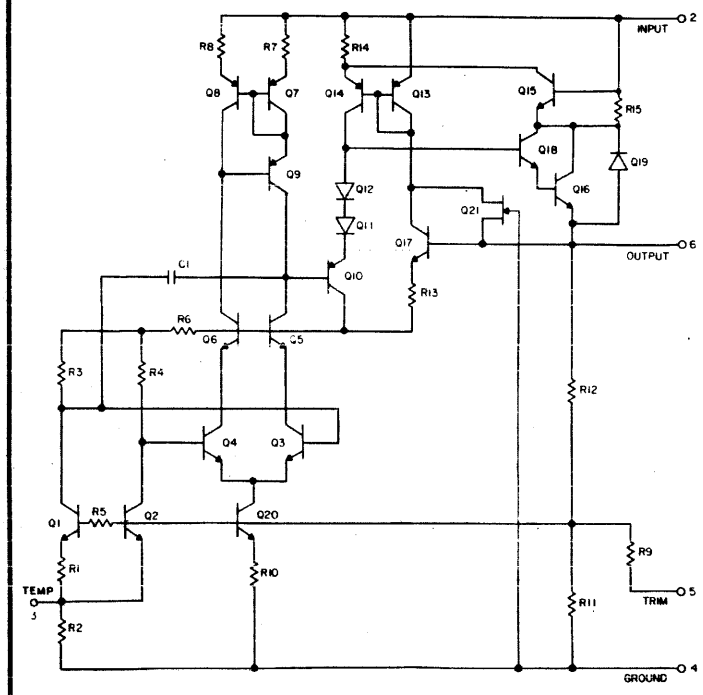
GENERAL DESCRIPTION

The REF-02 Precision Voltage Reference provides a stable +5V output which can be adjusted over a ±6% range with minimal effect on temperature stability. Single supply operation over an input voltage range of 7V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise and low power make the REF-02 an excellent choice whenever a stable voltage reference is required, such as in D/A and A/D converters, in portable instruments, and in digital voltmeters. The versatility of the REF-02 is illustrated by its use as a monolithic thermometer. (See AN-18, "Thermometer Applications of the REF-02.") For +10V Precision Voltage References see the REF-01 data sheet.

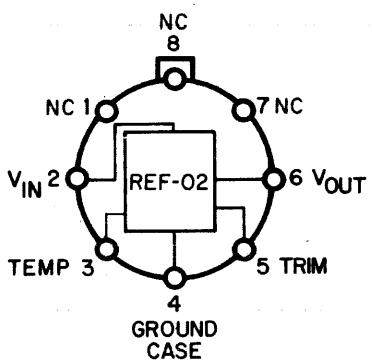
FEATURES

- Temperature Voltage Output . . . . . 2.1 mV/°C
- Adjustable 5 Volt Output . . . . . ±6%
- Excellent Temperature Stability . . . . . 3 ppm/°C
- Low Noise 10μVp-p
- Low Power 15mW
- Wide Input Voltage Range . . . . . 7V to 40V
- High Load Driving Capability 20mA
- No External Components
- Short Circuit Proof
- MIL-STD-883A Screening Available

SIMPLIFIED SCHEMATIC



PIN CONNECTIONS AND ORDERING INFORMATION



TO-99 (J-Suffix)

ORDER: REF-02AJ
REF-02J
REF-02EJ
REF-02HJ
REF-02CJ
REF-02DJ

Military Temperature Range Devices with MIL-STD-883A Class B Processing:

ORDER: REF02-883-AJ
REF02-883-J

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ABSOLUTE MAXIMUM RATINGS

Input Voltage REF-02, A, E, H	40 V	Operating Temperature Range	
REF-02C, D	30 V	REF-02A, REF-02	−55°C to +125°C
Power Dissipation (see note)	500mW	REF-02E, REF-02H	0°C to +70°C
Output Short Circuit Duration (to ground or V_{IN})	Indefinite	REF-02C, REF-02D	
Storage Temperature Range	−65°C to +150°C	Note: Derate at 7.1mW/°C above 80°C ambient temperature.	
Lead Temperature (Soldering, 60 sec)	300°C		

ELECTRICAL CHARACTERISTICS

These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	REF-02A Min	REF-02A Typ	REF-02A Max	REF-02 Min	REF-02 Typ	REF-02 Max	Units
Output Voltage	V_O	I_L = 0mA	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	±6.0	–	±3.0	±6.0	–	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 1)	–	10	15	–	10	15	μVp-p
Input Voltage Range	V_{IN}		7	–	40	7	–	40	V
Line Regulation (Note 2)		V_{IN} = 8 to 33V	–	0.006	0.010	–	0.006	0.010	%/V
Load Regulation (Note 2)		I_L = 0 to 10mA	–	0.005	0.010	–	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	–	5.0	–	–	5.0	–	μsec
Quiescent Current	I_{SY}	No Load	–	1.0	1.4	–	1.0	1.4	mA
Load Current	I_L		10	21	–	10	21	–	mA
Sink Current	I_S		−0.3	−0.5	–	−0.3	−0.5	–	mA
Short Circuit Current	I_{SC}	V_O = 0	–	30	–	–	30	–	mA
Temp Voltage Output	V_T	(Note 3)	–	630	–	–	630	–	mV
The following specifications apply for V_{IN} = +15V, −55°C ≤ T_A ≤ +125°C and I_L = 0mA, unless otherwise noted.									
Output Voltage Change with Temperature (Notes 4 and 5)	ΔV_{OT}	0° ≤ T_A ≤ +70°C	–	0.02	0.06	–	0.07	0.17	%
		−55° ≤ T_A ≤ +125°C	–	0.06	0.15	–	0.18	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	–	3	8.5	–	10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	–	0.7	–	–	0.7	–	ppm/%
Line Regulation (V_{IN} = 8 to 33V) (Note 2)		0° ≤ T_A ≤ +70°C	–	0.007	0.012	–	0.007	0.012	%/V
		−55° ≤ T_A ≤ +125°C	–	0.009	0.015	–	0.009	0.015	%/V
Load Regulation (I_L = 0 to 8mA) (Note 2)		0° ≤ T_A ≤ +70°C	–	0.006	0.010	–	0.007	0.012	%/mA
		−55° ≤ T_A ≤ +125°C	–	0.007	0.012	–	0.009	0.015	%/mA
Temp Voltage Output Temperature Coefficient	TCV_T	(Note 3)	–	2.1	–	–	2.1	–	mV/°C

NOTE 1: Parameter is not 100% tested; 90% of units meet this specification.

NOTE 2: Line and Load Regulation specifications include the effects of self heating.

NOTE 3: Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.

NOTE 4: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and minimum output voltage over the specified temperature range expressed as a percentage of 5V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{5V} \times 100$$

NOTE 5: ΔV_{OT} specification applies trimmed to 5.000V or untrimmed.

NOTE 6: TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e., TCV_O (0° to +70°C) = $\frac{\Delta V_{OT}\ 0° \text{ to } +70°C}{70°C}$

and TCV_O (−55° to +125°C) = $\frac{\Delta V_{OT}\ -55° \text{ to } +125°C}{180°C}$

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REF-02 DEFINITIONS

LINE REGULATION
The ratio of the change in output voltage to the change in line voltage producing it.

LOAD REGULATION
The ratio of the change in output voltage to the change in load current producing it.

QUIESCENT CURRENT (I_{SY})
The current required from the supply to operate the device with no load.

OUTPUT TURN-ON SETTLING TIME (t_{on})
The time required for the output voltage to reach its final value within a specified error band after application of V_{IN}

OUTPUT VOLTAGE NOISE (e_{np-p})
The peak to peak output noise voltage in a specified frequency band.

OUTPUT CHANGE WITH TEMPERATURE (ΔV_{OT})
The absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V:

$$\Delta V_{OT} = \frac{V_{MAX}-V_{MIN}}{5V} \times 100$$

OUTPUT TEMPERATURE COEFFICIENT (TCV_O)
The ratio of the output change with temperature to the specified temperature range expressed in ppm/°C.

ELECTRICAL CHARACTERISTICS

			REF-02E			REF-02H			
These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Output Voltage	V_O	I_L = 0 mA	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	±6.0	–	±3.0	±6.0	–	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 1)	–	10	15	–	10	15	µVp-p
Input Voltage Range	V_{IN}		7	–	40	7	–	40	V
Line Regulation (Note 2)		V_{IN} = 8 to 33V	–	0.006	0.010	–	0.006	0.010	%/V
Load Regulation (Note 2)		I_L = 0 to 10 mA	–	0.005	0.010	–	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	–	5.0	–	–	5.0	–	µsec
Quiescent Current	I_{SY}	No Load	–	1.0	1.4	–	1.0	1.4	mA
Load Current	I_L		10	21	–	10	21	–	mA
Sink Current	I_S		–0.3	–0.5	–	–0.3	–0.5	–	mA
Short Circuit Current	I_{SC}	V_O = 0	–	30	–	–	30	–	mA
Temp Voltage Output	V_T	(Note 3)	–	630	–	–	630	–	mV
The following specifications apply for V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C and I_L = 0mA, unless otherwise noted.									
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 4 and 5)	–	0.02	0.06	–	0.07	0.17	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	–	3	8.5	–	10	25	ppm/°C
Change in V_O Temperature Coefficient With Output Adjustment		R_p = 10kΩ	–	0.7	–	–	0.7	–	ppm/%
Line Regulation (Note 2)		V_{IN} = 8 to 33V	–	0.007	0.012	–	0.007	0.012	%/V
Load Regulation (Note 2)		I_L = 0 to 8 mA	–	0.006	0.010	–	0.007	0.012	%/mA
Temp Voltage Output Temperature Coefficient	TCV_T	(Note 3)	–	2.1	–	–	2.1	–	mV/°C

NOTE 1: Parameter is not 100% tested; 90% of units meet this specification.

NOTE 2: Line and Load Regulation specifications include the effects of self heating.

NOTE 3: Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.

NOTE 4: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{5V} \times 100$$

NOTE 5: ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.

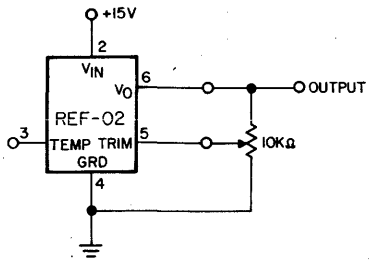
NOTE 6: TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e., $TCV_O = \frac{\Delta V_{OT}}{70°C}$

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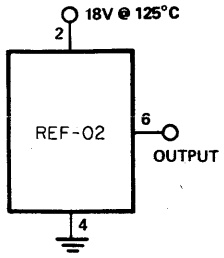
OUTPUT ADJUSTMENT

The REF-02 trim terminal can be used to adjust the output voltage over a 5V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V. Of course, the output can also be set to exactly 5.000V, or to 5.12V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. Typically the temperature coefficient change is 0.7 ppm/°C for 100mV of output adjustment.



BURN-IN CIRCUIT



ELECTRICAL CHARACTERISTICS

			REF-02C			REF-02D			
These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Output Voltage	V_O	I_L = 0 mA	4.950	5.000	5.050	4.900	5.000	5.100	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±2.7	±6.0	–	±2.0	±6.0	–	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 1)	–	12	18	–	12	–	μVp-p
Input Voltage Range	V_{IN}		7	–	30	7	–	30	V
Line Regulation (Note 2)		V_{IN} = 8 to 30V	–	0.009	0.015	–	0.010	0.04	%/V
Load Regulation (Note 2)		I_L = 0 to 8 mA	–	0.006	0.015	–	–	–	%/mA
Load Regulation (Note 2)		I_L = 0 to 4 mA	–	0.006	0.015	–	0.015	0.04	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value	–	5.0	–	–	5.0	–	μsec
Quiescent Current	I_{SY}	No Load	–	1.0	1.6	–	1.0	2.0	mA
Load Current	I_L		8	21	–	8	21	–	mA
Sink Current	I_S		-0.2	-0.5	–	-0.2	-0.5	–	mA
Short Circuit Current	I_{SC}	V_O = 0	–	30	–	–	30	–	mA
Temp Voltage Output	V_T	(Note 3)	–	630	–	–	630	–	mV
The following specifications apply for V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C and I_L = 0mA, unless otherwise noted.									
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 4 and 5)	–	0.14	0.45	–	0.49	–	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	–	20	65	–	70	–	ppm/°C
Change in V_O Temperature Coefficient With Output Adjustment		R_p = 10kΩ	–	0.7	–	–	0.7	–	ppm/%
Line Regulation (Note 2)		V_{IN} = 8 to 30V	–	0.011	0.018	–	0.012	–	%/V
Load Regulation (Note 2)		I_L = 0 to 5 mA	–	0.008	0.018	–	0.016	–	%/mA
Temp Voltage Output Temperature Coefficient	TCV_T	(Note 3)	–	2.1	–	–	2.1	–	mV/°C

NOTE 1: Parameter is not 100% tested; 90% of units meet this specification.

NOTE 2: Line and Load Regulation specifications include the effects of self heating.

NOTE 3: Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.

NOTE 4: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{5V} \times 100$$

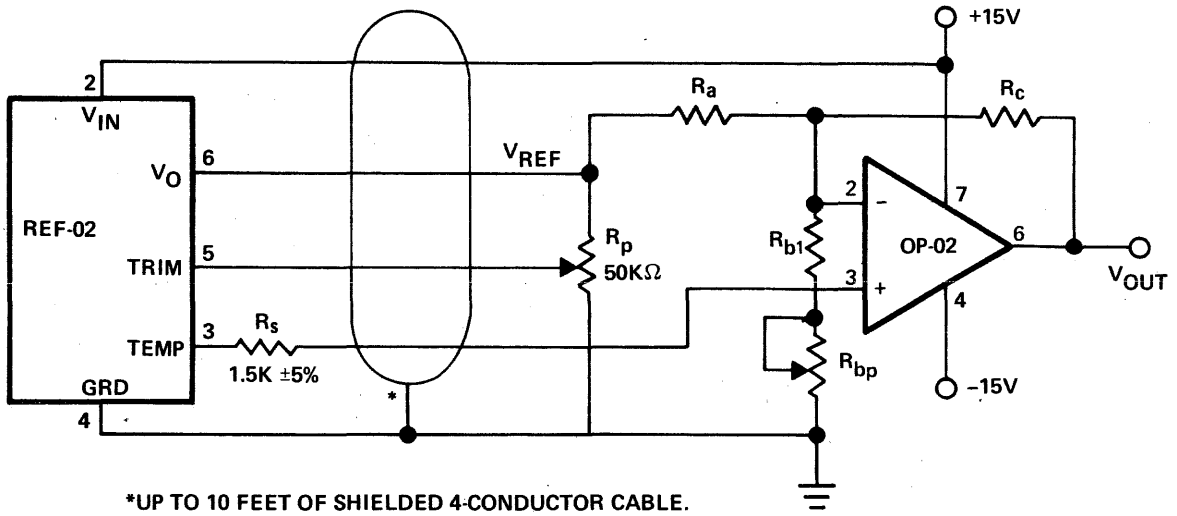
NOTE 5: ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.

NOTE 6: TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e., $TCV_O = \frac{\Delta V_{OT}}{70°C}$

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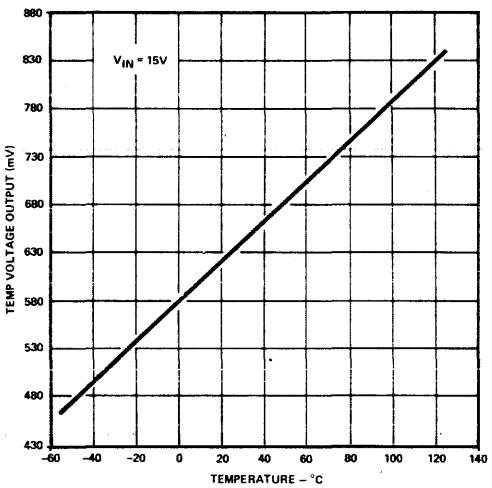
TYPICAL APPLICATIONS

PRECISION TEMPERATURE TRANSDUCER WITH REMOTE SENSOR



*UP TO 10 FEET OF SHIELDED 4-CONDUCTOR CABLE.

TYPICAL TEMPERATURE VOLTAGE OUTPUT VS TEMPERATURE (REF-02A)



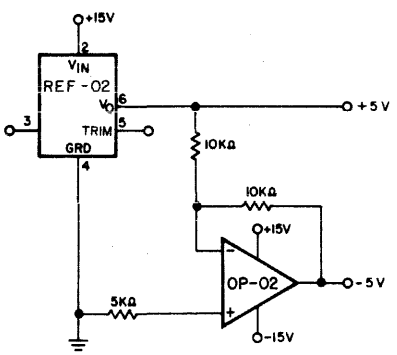
RESISTOR VALUES

TCV_{OUT} SLOPE (S)	10mV/°C	100mV/°C	10mV/°F
TEMPERATURE RANGE	–55° to +125°C	–55° to +125°C	–67°F to +257°C
OUTPUT VOLTAGE RANGE	–0.55V to +1.25V	–5.5V to +12.5V*	–0.67V to +2.57V
ZERO SCALE	0V @ 0°C	0V @ 0°C	0V @ 0°F
R_a (±1% resistor)	9.09KΩ	15KΩ	7.5KΩ
R_{b1} (±1% resistor)	1.5KΩ	1.82KΩ	1.21KΩ
R_{bp} (Potentiometer)	200Ω	500Ω	200Ω
R_c (±1% resistor)	5.11KΩ	84.5KΩ	8.25KΩ

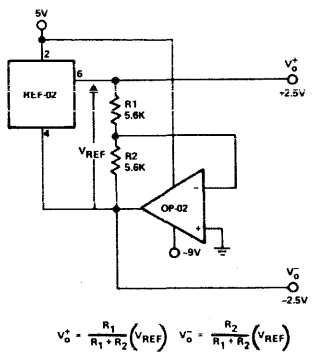
*For 125°C operation, the op amp output must be able to swing to +12.5V; increase V_{IN} to +18V from +15V if this is a problem.

FOR THEORY OF OPERATION AND CALIBRATION PROCEDURE CONSULT APPLICATION NOTE AN-18, "THERMOMETER APPLICATIONS OF THE REF-02."

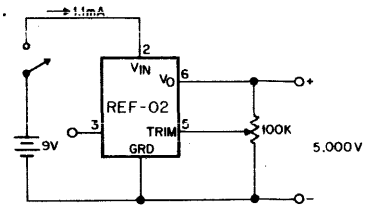
±5V REFERENCE



±2.5V REFERENCE



PRECISION CALIBRATION STANDARD



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PRELIMINARY

SMP-81

TELECOMMUNICATIONS SAMPLE AND HOLD AMPLIFIER

GENERAL DESCRIPTION

The SMP-81 precision sample and hold amplifier provides the high accuracy, low droop rate and fast acquisition ideally required for PCM telecommunication applications. The SMP-81 is a non-inverting unity gain circuit consisting of two buffer amplifiers of very high input impedance connected by a diode bridge switch.

High Accuracy and Low Droop Rate

The high input impedance and low droop rate of the SMP-81 is achieved by PMI ion implant super beta process. The high input impedance permits high impedance sources applications without degrading accuracy, and low droop rate. Other features of the SMP-81 include a 0.01% accuracy, 0.3mV of combined offset voltage and step transfer error, and very low feed-through. A diode bridge switch design allows minimum charge transfer step. On-chip PMI Zener-Zap trimming, around zero, eliminates nulling for most applications.

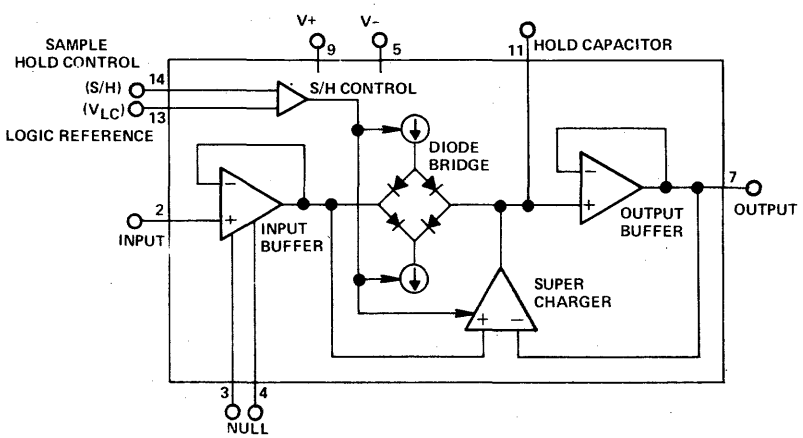
Fast Acquisition

A unique super charger or transconductance amplifier provides up to 50mA charging current to the hold capacitor. As a result, smooth charging of the hold capacitor is achieved with minimum noise. The super charger, in conjunction with the high slewing rate input and output buffer amplifiers, permits fast acquisition operation. The adjustable logic input threshold makes the SMP-81 compatible to all logic families.

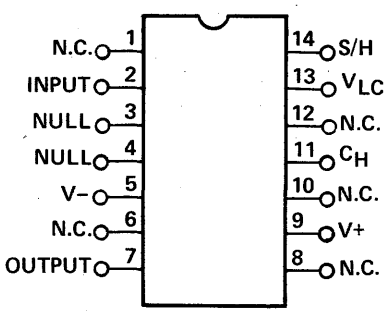
FEATURES

- Internally trimmed for a minimum offset voltage and charge transfer step 0.3mV
- Low Droop Rate Over Temperature. . . . 0.5μV/μsec
- Low Aperture Time 50ns
- Fast Acquisition Time 10V Step to 0.1% 3.5μs
- High Slew Rate 10V/μs
- High Sample Current/Hold Current Ratio . . . . . 1.7×10^8
- DTL, TTL & CMOS Compatible Logic Input
- HA-2425, DATEL SHM-IC-1, and AD-583 Socket Compatible
- Low Dissipation
- Low Cost

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



14 PIN DIP
(Y-Suffix)

ORDERING INFORMATION

ORDER:		
	SMP-81EY	0°C TO 70°C
	SMP-81FY	

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V	Hold Capacitor Short Circuit Duration	60 sec
Power Dissipation	500mW	Operating Temperature Range	0°C to +70°C
Input Voltage	Equal to Supply Voltage	Storage Temperature Range	−65°C to +150°C
Logic and Logic Reference Voltage	Equal to Supply Voltage	Lead Temperature (Soldering 60 sec)	300°C
Output Short Circuit Duration	Indefinite		

ELECTRICAL CHARACTERISTICS

SMP-81E | SMP-81F

These specifications apply for V_S ±15V, C_H = 0.005 µF, V_{LC} connected to ground, T_A = 25°C, device fully warmed up, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Min	Typ	Max	Units
Zero Scale Error	V_{ZS}	V_{IN} = 0 V_{LOG} = 3.5V Hold Mode	–	0.3	1.0	–	0.5	2.5	mV
Input Bias Current	I_B	V_{IN} = 0	–	25	50	–	30	90	nA
Leakage (Droop) Current	I_{DR}	Device Warmed Up	–	0.30	1.00	–	0.35	1.50	nA
Droop Rate			–	60	200	–	100	500	µV/msec
Input Resistance	R_{IN}		$3x10^{10}$	$6x10^{10}$	–	$15x10^{10}$	$5x10^{10}$	–	Ω
Voltage Gain	A_V	Sample Mode V_{IN} = ±10V R_L = 5KΩ or V_{IN} = ±5V R_L = 2KΩ	0.99977	0.99985	1.00000	0.99965	0.99982	1.00000	V/V
Acquisition Time		10V step to 0.1% of final value	–	3.5	–	–	3.5	–	µs
Aperture Time	t_a		–	50	–	–	50	–	nsec
Charge Transfer		V_{IN} = 0 V_{LOG} = 3.5V	–	5	–	–	5	–	pC
Slew Rate	SR	V_{IN} = ±10V R_L = 2KΩ	–	10	–	–	10	–	V/µs
Hold Capacitor Charging Current		V_{IN}-V_{OUT} ≥ ±3 volts	30	50	–	20	50	–	mA
Sample/Hold Current Ratio			–	$1.7x10^8$	–	–	$1.5x10^8$	–	mA/mA
Feedthrough Attenuation Ratio		Input = 20V pk-pk 1 kHz	86	96	–	80	90	–	dB
Full Power Bandwidth		±10V p-p	–	160	–	–	160	–	kHz
Input Voltage Range and/or Output Voltage Swing		R_L = 2KΩ	±11	±11.5	–	±10.5	±11.5	–	V
Output Resistance			–	0.15	–	–	0.15	–	Ω
Power Supply Rejection Ratio	PSRR	Sample Mode V_S = ±9V to ±18V	82	92	–	77	92	–	dB
Power Consumption	P_D	Sample Mode V_{IN} = 0	–	160	180	–	170	210	mW

The following specifications apply for V_S = ±15V, C_H = 0.005 µF, V_{LC} connected to ground, 0°C ≤ T_A ≤ +70°C, device fully warmed up, unless otherwise noted.

Zero Scale Error	V_{ZS}	V_{IN} = 0 V_{LOG} = 3.5V	–	0.6	1.6	–	0.9	3.5	mV
Input Bias Current	I_B	V_{IN} = 0	–	35	75	–	40	140	nA
Leakage (Droop) Current	I_{DR}	Device Warmed Up	–	0.5	1.8	–	0.6	2.8	nA
Voltage Gain	A_V	Sample Mode V_{IN} = ±10V R_L = 5KΩ or V_{IN} = ±5V R_L = 2.5KΩ	0.99972	0.99982	1.00000	0.99960	0.99978	1.00000	V/V
Power Supply Rejection Ratio	PSRR	Sample Mode V_S = ±9V to ±18V	80	90	–	75	90	–	dB
Logic Reference Input Current			−2	−1	–	−3	−1	–	µA
Logic Input Current		Sample Mode	−15	−5	–	−15	−5	–	µA
		Hold Mode	0	0.2	–	0	0.2	–	nA
Differential Logic Threshold			0.8	1.3	2.4	0.8	1.3	2.4	V

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DEFINITIONS OF TERMS

Zero Scale Error: The magnitude of the output voltage when switched to the hold mode with zero input voltage. This error consists of the sum of the offset voltage and charge transfer step voltage, and is adjustable to zero.

Acquisition Time: The minimum time required for the output to follow the input signal, within a specified percent error, after the sample command.

Voltage Gain: The ratio of the output voltage signal to the input voltage signal, in the sample mode.

HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor (C_H) acts as a memory element and also as a compensating capacitor for the sample and hold amplifier. For stable operation, a minimum value of 0.002μF is recommended, with no limit set for the maximum value. The SMP-81 is internally trimmed for a C_H = 0.005μF. Other values of C_H will cause a zero scale shift, which can be calculated from the following equation:

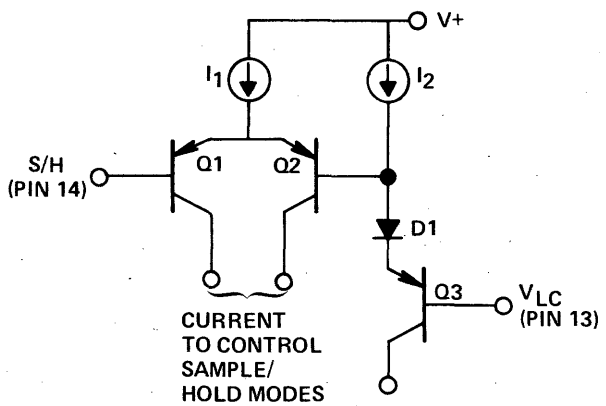
$$\Delta V_{ZS} = \frac{5pC}{C_H} - 1mV$$

The hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85°C, polystyrene capacitors are recommended, while teflon capacitors are recommended for higher temperature applications.

SMP-81 LOGIC CONTROL

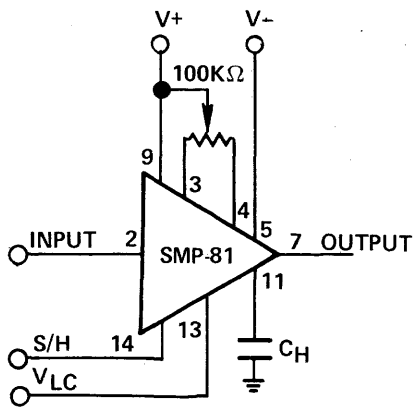
The sample/hold mode control of the SMP-81 incorporates a unique logic input circuit, which enables direct interface to all popular logic families and provides maximum noise immunity. As shown in the figure, the mode control is accomplished by steering the current (I_1) through Q1 or Q2, thus providing high speed switching and a predictable logic threshold. For TTL and DTL interface, simply ground V_{LC} (pin 13). For CMOS, HTL and HNIL interface, the appropriate threshold voltage should be applied to V_{LC}.

For proper operation, the V_{LC} (logic reference) must be always at least 3.5V below the positive supply and 2.0V above the negative supply. Also, sample and hold control (S/H) must always be 2.8V above the negative supply.



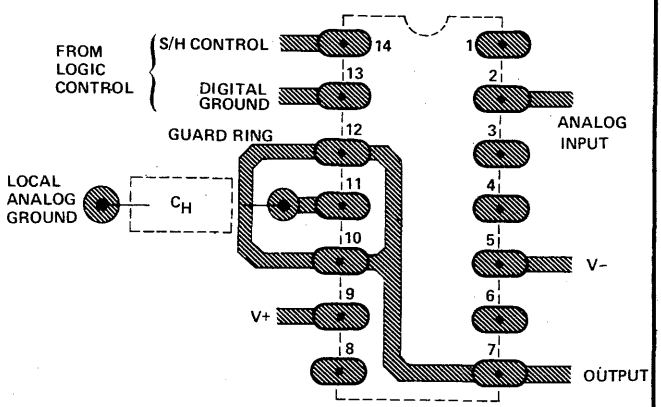
ZERO SCALE ERROR NULL ADJUSTMENT

During the null adjustment, the amplifier should be switched continuously between the "sample" and "hold" mode. The error should then be adjusted to zero when the unit is in the "hold" mode. In this way, both offset voltage errors and charge transfer errors are adjusted to zero.



GUARDING AND GROUNDING LAYOUT

The use of a ground plane is strongly recommended to minimize ground path resistances. Separate analog and digital grounds should be used, and it is advisable to keep these two ground systems isolated until they are tied back to the common system ground. Digital currents should not flow back to the system ground through the analog ground path.



CMP-01

FAST PRECISION COMPARATOR

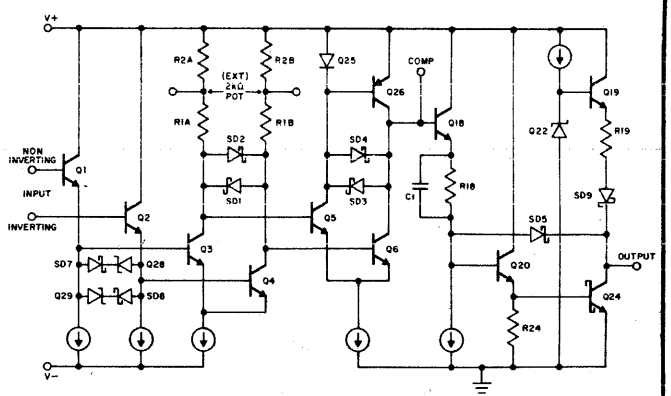
GENERAL DESCRIPTION

The CMP-01 is a monolithic Fast Precision Voltage Comparator using an advanced compatible NPN-Schottky Barrier Diode process. It features fast response time to both large and small input signals, while maintaining excellent input characteristics. The CMP-01 is capable of operating over a wide range of supply voltages, including single 5 volt supply operation. The large output current sinking and high output voltage capability assure good application flexibility, while the combination of fast response, high accuracy, and freedom from oscillation assure performance in precision level detectors and 12 and 13 bit A/D converters. The CMP-01 is pin compatible to earlier 111, 106, and 710 types. For applications requiring lower input offset and bias currents, refer to the CMP-02 data sheet.

FEATURES

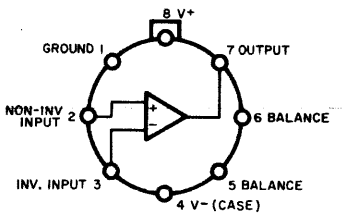
- Fast Response Time . . . . . 110 ns typ., 180 ns Max
- High Input Slew Rate . . . . . .92 V/μS
- Low Offset Voltage . . . . . 0.3 mV typ., 0.8 mV Max
- Low Offset Current . . . . . 4 nA typ., 25 nA Max
- Low Offset Drift . . . . . 1.0 μV/°C, 30 pA/°C
- Standard Power Supplies . . . . . ±5V to ±18V
- Guaranteed Operation from Single +5V Supply
- No Pull-up Resistor Required for TTL Drive
- Wired OR Capability
- Fits 111, 106, 710 Sockets
- Easy Offset Nulling. . . . . Single 2kΩ Potentiometer
- Easy to Use. . . . . Free from Oscillations

SIMPLIFIED SCHEMATIC

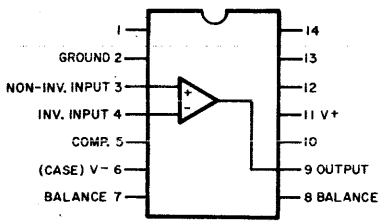


PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



TO-99 (J-Suffix)
ORDER: CMP-01J
CMP-01EJ
CMP-01CJ



14 PIN HERMETIC DIP (Y-Suffix)
ORDER: CMP-01Y
CMP-01EY
CMP-01CY

Military Temperature Range Devices
With MIL-STD-883A Class B Processing

CMP01-883-J
CMP01-883-Y

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ABSOLUTE MAXIMUM RATINGS

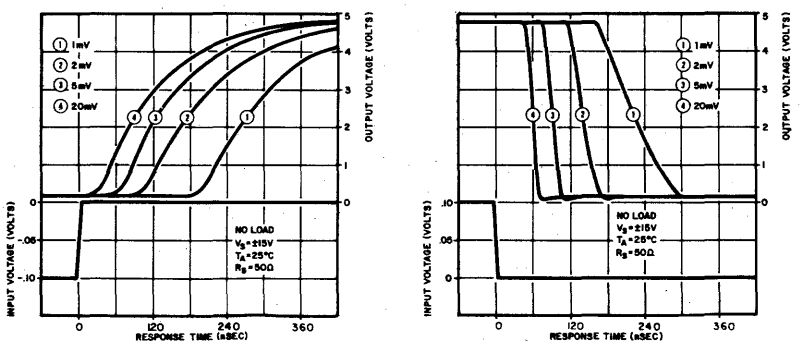
Total Supply Voltage, V+ to V-	36V	Output Sink Current (Continuous Operation)	75 mA
Output to Ground	-5V to +32V	Operating Temperature Range –	
Output to Negative Supply Voltage	50V	CMP-01	-55°C to +125°C
Ground to Negative Supply Voltage	30V	CMP-01E, -01C	0°C to +70°C
Positive Supply Voltage to Ground	30V	Storage Temperature Range	-65°C to +150°C
Positive Supply Voltage to Offset Null	0 to 2V	Lead Temperature (Soldering, 60 Sec)	300°C
Power Dissipation (See Note)	500 mW	Output Short Circuit Duration – to ground	Indefinite
Differential Input Voltage	±11V	to V+	1 min.
Input Voltage (V_s = ±15V)	±15V		

Note: Maximum package power dissipation vs. ambient temperature

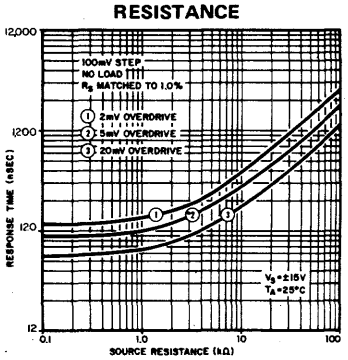
Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1 mW/°C
Dual-in-Line (Y)	100°C	10.0 mW/°C

TYPICAL PERFORMANCE CURVES

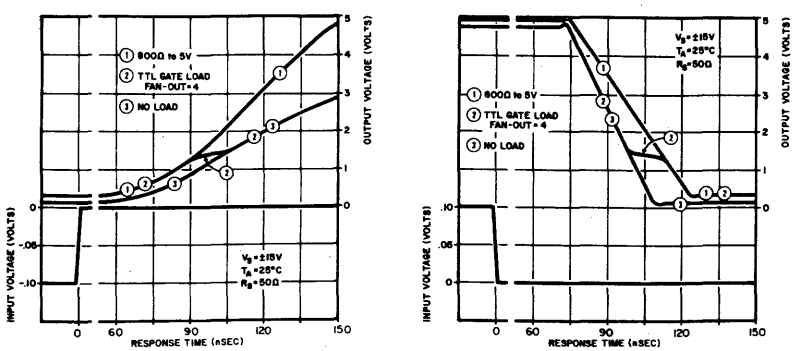
RESPONSE TIME FOR 100mV STEP AND VARIOUS INPUT OVERDRIVES



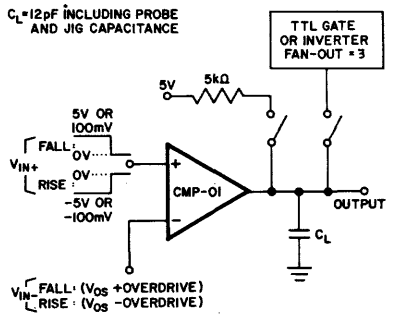
RESPONSE TIME VS SOURCE RESISTANCE



RESPONSE TIME, 100mV STEP, 5mV OVERDRIVE, VARIOUS LOADS



RESPONSE TIME TEST CIRCUIT



ELECTRICAL CHARACTERISTICS			CMP-01			
These specifications apply for V_s = ±15V, T_A = 25°C unless otherwise noted.						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ.**	**Max.**	**Units**
Input Offset Voltage	V_{os}	$R_s \leq 5k\Omega$ (Note 1)	–	0.3	0.8	mV
Input Offset Current	I_{os}	(Note 1)	–	4	25	nA
Input Bias Current	I_B		–	350	600	nA
Differential Input Resistance	R_{in}		3.0	14	–	MΩ
Voltage Gain	A_v	V_O = 0.4V to 2.4V	200	500	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive				
		no load (no pull-up)	–	110	180	nsec
		5kΩ to 5V	–	110	–	nsec
		TTL fan-out = 4, no pull-up	–	110	–	nsec
		5V step 5mV overdrive				
		no load (no pull-up)	–	160	–	nsec
		5kΩ to 5V	–	160	–	nsec
		TTL fan-out = 4, no pull-up	–	160	–	nsec
Input Slew Rate			–	92	–	V/μsec
Input Voltage Range	CMVR		±12.5	±13.0	–	V
Common Mode Rejection Ratio	CMRR		94	110	–	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{s+} \leq 18V$, $-18V \leq V_{s-} \leq 0V$	80	100	–	dB
Positive Output Voltage	V_{OH}	$V_{in} \geq 3mV$, $I_O = 320\mu A$	2.4	3.2	–	V
		$V_{in} \geq 3mV$, $I_O = 0$	2.4	4.8	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -10mV$, I_{sink} = 6.4 mA	–	0.3	0.45	V
		$V_{in} \leq -10mV$, $I_{sink} \leq 12$ mA	–	0.36	0.5	V
Output Leakage Current	I_{LEAK}	$V_{in} \geq 10mV$, V_O = 30V	–	0.03	2.0	μA
Positive Supply Current	I+	$V_{in} \leq -10mV$	–	5.6	8.0	mA
Negative Supply Current	I–	$V_{in} \leq -10mV$	–	1.3	2.2	mA
Power Dissipation	P_d	$V_{in} \leq -10mV$	–	103	153	mW
Offset Voltage Adjustment Range		Nulling Pot ≥ 2kΩ	–	±5	–	mV
These specifications apply for V_{s+} = 5V, V_{s-} = 0V, T_A = 25°C, unless otherwise noted.						
Input Offset Voltage	V_{os}	$R_s \leq 5k\Omega$ (Note 1)	–	0.4	1.5	mV
Input Offset Current	I_{is}	(Note 1)	–	3	21	nA
Input Bias Current	I_B		–	250	500	nA
Voltage Gain	A_v	V_O = 0.4V to 2.4V (Note 1)	–	50	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive				
		5kΩ to 5V	–	150	–	nsec
		TTL fan-out = 4, 5kΩ to 5V	–	150	–	nsec
Input Voltage Range	CMVR		1.8/3.5	1.7/3.8	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -3.5mV$, $I_{sink} \leq 6.4$ mA	–	0.3	0.45	V
Positive Supply Current	I+	$V_{in} \leq -10mV$	–	2.3	3.2	mA
Power Dissipation	P_d	$V_{in} \leq -10mV$	–	11.5	16.0	mW
The following specifications apply for V_s = ±15V, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.						
Input Offset Voltage	V_{os}	$R_s \leq 5k\Omega$ (Note 1)	–	0.5	1.6	mV
		V_{s+} = 5V, V_{s-} = 0V (Note 1)	–	0.6	2.8	mV
Average Input Offset Voltage Drift						
Without External Trim	TCV_{os}	$R_s = 50\Omega$	–	1.5	–	μV/°C
With External Trim	TCV_{osn}	$R_s = 50\Omega$	–	1.0	–	μV/°C
Input Offset Current	I_{os}	T_A = +125°C (Note 1)	–	4	25	nA
		T_A = –55°C (Note 1)	–	8	80	nA
Average Input Offset Current Drift	TCI_{os}	$25°C \leq T_A \leq +125°C$	–	12	–	pA/°C
		$-55°C \leq T_A \leq 25°C$	–	35	–	pA/°C
Input Bias Current	I_B	T_A = +125°C	–	300	600	nA
		T_A = –55°C	–	550	1400	nA
Voltage Gain	A_v	V_O = 0.4V to 2.4V	100	500	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive				
		T_A = +125°C, no load	–	160	–	nsec
		T_A = –55°C, no load	–	90	–	nsec
Input Voltage Range	CMVR		±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR		88	106	–	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{s+} \leq 15V$, $-15V, \leq V_{s-} \leq 0V$	75	96	–	dB
Positive Output Voltage	V_{OH}	$V_{in} \geq 4mV$, $I_O = 200\mu A$	2.4	3.0	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -10mV$, I_{sink} = 0	–	0.20	0.4	V
		$V_{in} \leq -10mV$, I_{sink} = 6.4 mA	–	0.32	0.5	V

NOTE 1: These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.

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ELECTRICAL CHARACTERISTICS			CMP-01E			CMP-01C			
These specifications apply for V_S = ±15V, T_A = 25°C unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	–	0.3	0.8	–	0.4	2.8	mV
Input Offset Current	I_{OS}	(Note 1)	–	4	25	–	5	80	nA
Input Bias Current	I_B		–	350	600	–	400	900	nA
Differential Input Resistance	R_{in}		3.0	14	–	1.0	10	–	MΩ
Voltage Gain	A_V	V_O = 0.4V to 2.4V	200	500	–	100	500	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive							
		no load (no pull-up)	–	110	180	–	110	180	nsec
		5kΩ to 5V	–	110	–	–	110	–	nsec
		TTL fan-out = 4, no pull-up	–	110	–	–	110	–	nsec
		5V step 5mV overdrive							
		no load (no pull-up)	–	160	–	–	160	–	nsec
		5kΩ to 5V	–	160	–	–	160	–	nsec
		TTL fan-out = 4, no pull-up	–	160	–	–	160	–	nsec
Input Slew Rate			–	92	–	–	92	–	V/μsec
Input Voltage Range	CMVR		±12.5	±13.0	–	±12.5	±13.0	–	V
Common Mode Rejection Ratio	CMRR		94	110	–	90	110	–	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 18V$, $-18V \leq V_{S-} \leq 0V$	80	100	–	74	98	–	dB
Positive Output Voltage	V_{OH}	$V_{in} \geq 3mV$, $I_O = 320\mu A$	2.4	3.2	–	–	–	–	V
		$V_{in} \geq 3mV$, $I_O = 240\mu A$	–	–	–	2.4	3.4	–	V
		$V_{in} \geq 3mV$, $I_O = 0$	2.4	4.8	–	2.4	4.8	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -10mV$, $I_{sink} = 0$	–	0.16	0.4	–	0.16	0.4	V
		$V_{in} \leq -10mV$, $I_{sink} \leq 6.4$ mA	–	0.31	0.45	–	0.31	0.45	V
Output Leakage Current I	I_{LEAK}	$V_{in} \geq 10mV$, V_O = 30V	–	0.03	4.0	–	0.05	8.0	μA
Positive Supply Current	I+	$V_{in} \leq -10mV$	–	5.6	8.0	–	5.6	8.5	mA
Negative Supply Current	I–	$V_{in} \leq -10mV$	–	1.3	2.2	–	1.3	2.2	mA
Power Dissipation	P_d	$V_{in} \leq -10mV$	–	103	153	–	103	161	mW
Offset Voltage Adjustment Range		Nulling Pot ≥ 2kΩ	–	±5	–	–	±5	–	mV
These specifications apply for V_S+ = 5V, V_S– = 0V, T_A = 25°C unless otherwise noted.									
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	–	0.4	1.5	–	0.5	3.5	mV
Input Offset Current	I_{OS}	(Note 1)	–	3	21	–	4	65	nA
Input Bias Current	I_B		–	250	500	–	300	720	nA
Voltage Gain	A_V	V_O = 0.4V to 2.4V (Note 1)	–	50	–	–	50	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive							
		5kΩ to 5V	–	150	–	–	150	–	nsec
		TTL fan-out = 4, 5kΩ to 5V	–	150	–	–	150	–	nsec
Input Voltage Range	CMVR		1.8/3.5	1.7/3.8	–	1.8/3.5	1.7/3.8	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -3.5mV$, $I_{sink} \leq 6.4mA$	–	0.3	0.45	–	0.3	0.45	V
Positive Supply Current	I+	$V_{in} \leq -10mV$	–	2.3	3.2	–	2.4	3.8	mA
Power Dissipation	P_d	$V_{in} \leq -10mV$	–	11.5	16.0	–	12.0	19.0	mW
The following specifications apply for V_S = ±15V, $0° \leq T_A \leq +70°C$ unless otherwise noted.									
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	–	0.4	1.4	–	0.5	3.5	mV
		V_{S+} = 5V, V_{S-} = 0V (Note 1)	–	0.5	2.4	–	0.6	4.3	mV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	$R_S = 50\Omega$	–	1.5	–	–	1.8	–	μV/°C
With External Trim	TCV_{OSn}	$R_S = 50\Omega$	–	1.0	–	–	1.2	–	μV/°C
Input Offset Current	I_{OS}	$T_A = +70°C$ (Note 1)	–	4	25	–	5	80	nA
		$T_A = 0°C$ (Note 1)	–	5	45	–	6	120	nA
Average Input Offset Current Drift	TCI_{OS}	$25°C \leq T_A \leq +70°C$	–	12	–	–	12	–	pA/°C
		$0°C \leq T_A \leq 25°C$	–	35	–	–	40	–	pA/°C
Input Bias Current	I_B	$T_A = +70°C$	–	330	600	–	340	900	nA
		$T_A = 0°C$	–	400	950	–	450	1200	nA
Voltage Gain	A_V	V_O = 0.4V to 2.4V	100	500	–	70	500	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive							
		$T_A = +70°C$, no load	–	130	–	–	130	–	nsec
		$T_A = 0°C$, no load	–	100	–	–	100	–	nsec
Input Voltage Range	CMVR		±12.0	±13.3	–	±12.0	±13.3	–	V
Common Mode Rejection Ratio	CMRR		90	108	–	86	108	–	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	77	98	–	70	88	–	dB
Positive Output Voltage	V_{OH}	$V_{in} \geq 4mV$, $I_O = 200\mu A$	2.4	3.2	–	2.4	3.2	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -10mV$, $I_{sink} = 0$	–	0.17	0.4	–	0.17	0.4	V
		$V_{in} \leq -10mV$, I_{sink} = 6.4 mA	–	0.3	0.5	–	0.31	0.5	V

NOTE 1: These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.

CMP-02

LOW INPUT CURRENT PRECISION COMPARATOR

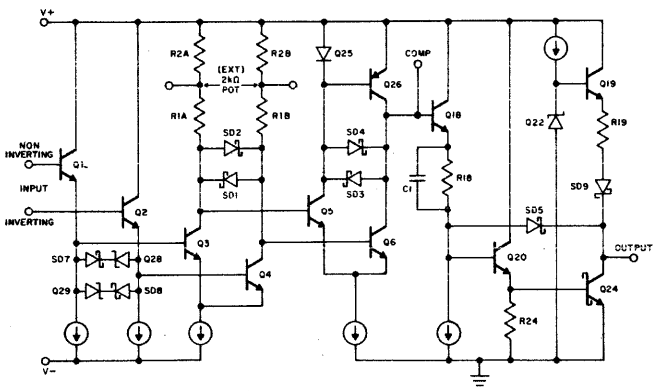
GENERAL DESCRIPTION

The CMP-02 is a monolithic low input current comparator using an advanced compatible NPN-Schottky Barrier Diode process. It features superior input characteristics with extremely low offset voltage, offset current, bias current and temperature drift. High common mode and power supply rejection plus good response time contribute to excellent performance in the most demanding applications. The balanced offset nulling, large output drive, and wired-or capability combined with internal pull-up maximize application convenience. The CMP-02 is capable of operating over a wide range of supply voltages, including single plus 5 volt supply operation, and is pin-compatible to earlier 111, 106, and 710 types. For applications requiring faster response time, please refer to the CMP-01 Fast Precision Comparator data sheet.

FEATURES

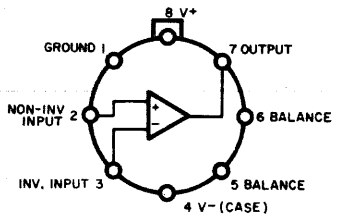
- Low Offset Voltage . . . . . 0.3 mV typ., 0.8 mV Max
- Low Offset Current . . . . . 0.3 nA typ., 3.0 nA Max
- Low Bias Current . . . . . 28 nA typ., 50 nA Max
- Low Offset Drift . . . . . 1.0 μV/°C, 4 pA/°C
- High Gain . . . . . 200,000 Min
- High CMRR . . . . . 110 dB typ., 94 dB Min
- High Input Impedance . . . . . 16 MΩ
- Fast Response Time . . . . . 190 ns typ., 270 ns Max
- Standard Power Supplies . . . . . ±5V to ±18V
- Guaranteed Operation from Single +5V Supply
- No Pull-up Resistor Required for TTL Drive
- Wired-OR Capability
- Fits 111, 106, 710 Sockets
- Easy Offset Nulling . . . . . Single 2KΩ Potentiometer
- Easy to Use . . . . . Free from Oscillations

SIMPLIFIED SCHEMATIC

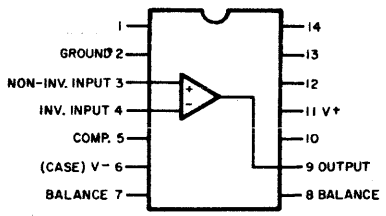


PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW



TO-99 (J-Suffix)
ORDER: CMP-02J
CMP-02EJ
CMP-02CJ



14 PIN HERMETIC DIP (Y-Suffix)
ORDER: CMP-02Y
CMP-02EY
CMP-02CY

Military Temperature Range Devices
With MIL-STD-883A Class B Processing
CMP02-883-J
CMP02-883-Y

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ELECTRICAL CHARACTERISTICS			CMP-02			
These specifications apply for V_S = ±15V, T_A = 25°C unless otherwise noted.						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	–	0.3	0.8	mV
Input Offset Voltage	V_{OS}	$R_S \leq 50K\Omega$ (Note 1)	–	0.3	0.9	mV
Input Offset Current	I_{OS}	(Note 1)	–	0.3	3.0	nA
Input Bias Current	I_B		–	28	50	nA
Differential Input Resistance	R_{in}		5.0	16	–	MΩ
Voltage Gain	A_V	V_O = 0.4V to 2.4V	200	500	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive				
		no load (no pull-up)	–	190	270	nsec
		5kΩ to 5V	–	190	–	nsec
		TTL fan-out = 4, no pull-up	–	190	–	nsec
Input Slew Rate			–	12.5	–	V/μsec
Input Voltage Range	CMVR		±12.5	±13.0	–	V
Common Mode Rejection Ratio	CMRR		94	110	–	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 18V$, $-18V \leq V_{S-} \leq 0V$	80	100	–	dB
Positive Output Voltage	V_{OH}	$V_{in} \geq 3mV$, $I_O = 320\mu A$	2.4	3.2	–	V
		$V_{in} \geq 3mV$, $I_O = 0$	2.4	4.8	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -10mV$, I_{sink} = 6.4 mA	–	0.3	0.45	V
		$V_{in} \leq -10mV$, I_{sink} = 12 mA	–	0.36	0.5	V
Output Leakage Current	I_{LEAK}	$V_{in} \geq 10mV$, V_O = 30V	–	0.03	2.0	μA
Positive Supply Current	I+	$V_{in} \leq -10mV$	–	5.5	8.0	mA
Negative Supply Current	I–	$V_{in} \leq -10mV$	–	1.1	2.2	mA
Power Dissipation	P_d	$V_{in} \leq -10mV$	–	99	153	mW
Offset Voltage Adjustment Range		Nulling Pot ≥ 2kΩ	–	±5.0	–	mV
These specifications apply for V_S+ = 5V, V_S– = 0V, T_A = 25°C, unless otherwise noted.						
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	–	0.4	1.5	mV
Input Offset Current	I_{OS}	(Note 1)	–	0.25	3.0	nA
Input Bias Current	I_B		–	24	45	nA
Voltage Gain	A_V	V_O = 0.4V to 2.4V (Note 1)	–	50	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive				
		5kΩ to 5V	–	250	–	nsec
		TTL fan-out = 4, 5kΩ to 5V	–	250	–	nsec
Input Voltage Range	CMVR		1.8/3.5	1.7/3.9	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -3.5mV$, $I_{sink} \leq 6.4$ mA	–	0.30	0.45	V
Positive Supply Current	I+	$V_{in} \leq -10mV$	–	2.2	3.0	mA
Power Dissipation	P_d	$V_{in} \leq -10mV$	–	11.0	15.0	mW
The following specifications apply for V_S = ±15V, –55°C ≤ T_A ≤ +125°C, unless otherwise noted.						
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ (Note 1)	–	0.5	1.6	mV
		V_{S+} = 5V, V_{S-} = 0V (Note 1)	–	0.6	2.8	mV
Average Input Offset Voltage Drift						
Without External Trim	TCV_{OS}	$R_S = 50\Omega$	–	1.5	–	μV/°C
With External Trim	TCV_{OSn}	$R_S = 50\Omega$	–	1.0	–	μV/°C
Input Offset Current	I_{OS}	T_A = +125°C (Note 1)	–	0.3	4.0	nA
		T_A = –55°C (Note 1)	–	0.6	12.0	nA
Average Input Offset Current Drift	TCI_{OS}	25°C ≤ T_A ≤ +125°C	–	2.0	–	pA/°C
		–55°C ≤ T_A ≤ 25°C	–	4.0	–	pA/°C
Input Bias Current	I_B	T_A = +125°C	–	25	50	nA
		T_A = –55°C	–	45	120	nA
Voltage Gain	A_V	V_O = 0.4V to 2.4V	100	500	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive				
		T_A = +125°C, no load	–	310	–	nsec
		T_A = –55°C, no load	–	155	–	nsec
Input Voltage Range	CMVR		±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR		88	106	–	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	75	96	–	dB
Positive Output Voltage	V_{OH}	$V_{in} \geq 4mV$, $I_O = 200\mu A$	2.4	3.0	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -10mV$, I_{sink} = 0	–	0.20	0.4	V
		$V_{in} \leq -10mV$, I_{sink} = 6.4 mA	–	0.32	0.5	V

NOTE 1: These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.

ELECTRICAL CHARACTERISTICS

These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted.

Parameter	Symbol	Test Conditions	CMP-02E Min.	CMP-02E Typ.	CMP-02E Max.	CMP-02C Min.	CMP-02C Typ.	CMP-02C Max.	Units
Input Offset Voltage	V_{os}	$R_S \leq 5k\Omega$ (Note 1)	–	0.3	0.8	–	0.4	2.8	mV
Input Offset Voltage	V_{os}	$R_S \leq 50K\Omega$ (Note 1)	–	0.3	0.9	–	0.4	3.0	mV
Input Offset Current	I_{os}	(Note 1)	–	0.3	3.0	–	0.4	15	nA
Input Bias Current	I_B		–	28	50	–	35	100	nA
Differential Input Resistance	R_{in}		5.0	16	–	1.5	12	–	MΩ
Voltage Gain	A_v	$V_O = 0.4V$ to $2.4V$	200	500	–	100	500	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive							
		no load (no pull-up)	–	190	270	–	190	270	nsec
		5kΩ to 5V	–	190	–	–	190	–	nsec
		TTL fan-out = 4, no pull-up	–	190	–	–	190	–	nsec
Input Slew Rate			–	15	–	–	15	–	V/μsec
Input Voltage Range	CMVR		±12.5	±13.0	–	±12.5	±13.0	–	V
Common Mode Rejection Ratio	CMRR		94	110	–	90	110	–	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{s+} \leq 18V$, $-18V \leq V_{s-} \leq 0V$	80	100	–	74	98	–	dB
Positive Output Voltage	V_{OH}	$V_{in} \geq 3mV$, $I_O = 320\mu A$	2.4	3.2	–	–	–	–	V
		$V_{in} \geq 3mV$, $I_O = 240\mu A$	–	–	–	2.4	3.4	–	V
		$V_{in} \geq 3mV$, $I_O = 0$	2.4	4.8	–	2.4	4.8	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -10mV$, $I_{sink} = 0$	–	0.16	0.4	–	0.16	0.4	V
		$V_{in} \leq -10mV$, $I_{sink} \leq 6.4$ mA	–	0.31	0.45	–	0.31	0.45	V
Output Leakage Current	I_{LEAK}	$V_{in} \geq 10mV$, $V_O = 30V$	–	0.03	4.0	–	0.05	8.0	μA
Positive Supply Current	I+	$V_{in} \leq -10mV$	–	5.5	8.0	–	5.6	8.5	mA
Negative Supply Current	I–	$V_{in} \leq -10mV$	–	1.1	2.2	–	1.2	2.2	mA
Power Dissipation	P_d	$V_{in} \leq -10mV$	–	99	153	–	102	161	mW
Offset Voltage Adjustment Range		Nulling Pot ≥ 2kΩ	–	±5.0	–	–	±5.0	–	mV
These specifications apply for $V_{s+} = 5V$, $V_{s-} = 0V$, $T_A = 25°C$ unless otherwise noted.									
Input Offset Voltage	V_{os}	$R_S \leq 5k\Omega$ (Note 1)	–	0.4	1.5	–	0.5	3.5	mV
Input Offset Current	I_{os}	(Note 1)	–	0.25	3.0	–	0.35	14	nA
Input Bias Current	I_B		–	24	45	–	30	90	nA
Voltage Gain	A_v	$V_O = 0.4V$ to $2.4V$ (Note 1)	–	50	–	–	50	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive							
		5kΩ to 5V	–	250	–	–	250	–	nsec
		TTL fan-out = 4, 5kΩ to 5V	–	250	–	–	250	–	nsec
Input Voltage Range	CMVR		1.8/3.5	1.7/3.8	–	1.8/3.5	1.7/3.8	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -3.5mV$, $I_{sink} \leq 6.4$ mA	–	0.3	0.45	–	0.3	0.45	V
Positive Supply Current	I+	$V_{in} \leq -10mV$	–	2.2	3.0	–	2.3	3.6	mA
Power Dissipation	P_d	$V_{in} \leq -10mV$	–	11.0	15.0	–	11.5	18.0	mW
The following specifications apply for $V_S = \pm 15V$, $0° \leq T_A \leq +70°C$ unless otherwise noted.									
Input Offset Voltage	V_{os}	$R_S \leq 5k\Omega$ (Note 1)	–	0.4	1.4	–	0.5	3.5	mV
		$V_{s+} = 5V$, $V_{s-} = 0V$ (Note 1)	–	0.5	2.4	–	0.6	4.3	mV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{os}	$R_S = 50\Omega$	–	1.5	–	–	1.8	–	μV/°C
With External Trim	TCV_{osn}	$R_S = 50\Omega$	–	1.0	–	–	1.2	–	μV/°C
Input Offset Current	I_{os}	$T_A = +70°C$ (Note 1)	–	0.3	3.0	–	0.4	15	nA
		$T_A = 0°C$ (Note 1)	–	0.4	6.0	–	0.5	25	nA
Average Input Offset Current Drift	TCI_{os}	$25°C \leq T_A \leq +70°C$	–	2.0	–	–	3.0	–	pA/°C
		$0°C \leq T_A \leq 25°C$	–	4.0	–	–	5.0	–	pA/°C
Input Bias Current	I_B	$T_A = +70°C$	–	26	50	–	33	100	nA
		$T_A = 0°C$	–	34	80	–	42	160	nA
Voltage Gain	A_v	$V_O = 0.4V$ to $2.4V$	100	500	–	70	500	–	V/mV
Response Time	t_r	100mV step, 5mV overdrive							
		$T_A = +70°C$, no load	–	225	–	–	225	–	nsec
		$T_A = 0°C$, no load	–	180	–	–	180	–	nsec
Input Voltage Range	CMVR		±12.0	±13.0	–	±12.0	±13.0	–	V
Common Mode Rejection Ratio	CMRR		90	108	–	86	108	–	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{s+} \leq 15V$, $-15V \leq V_{s-} \leq 0V$	77	98	–	70	88	–	dB
Positive Output Voltage	V_{OH}	$V_{in} \geq 4mV$, $I_O = 200\mu A$	2.4	3.2	–	2.4	3.2	–	V
Saturation Voltage	V_{SAT}	$V_{in} \leq -10mV$, $I_{sink} = 0$	–	0.17	0.4	–	0.17	0.4	V
		$V_{in} \leq -10mV$, $I_{sink} = 6.4$ mA	–	0.30	0.5	–	0.31	0.5	V

NOTE 1: These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.

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DAC-01

6 BIT MONOLITHIC D/A CONVERTER

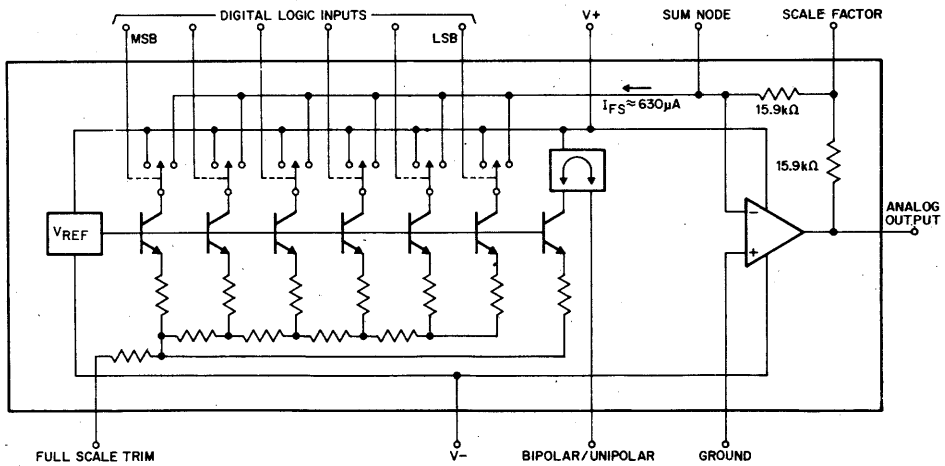
GENERAL DESCRIPTION

The DAC-01 is a complete monolithic 6-bit digital-to-analog converter, incorporating current steering logic, current sources, diffused resistor ladder network, precision voltage reference and fast summing op amp on one chip. Monolithic construction provides small size, light weight, low power consumption and very high reliability. Wide power supply range, three output voltage options, and three input code options assure flexibility for a wide variety of applications. A seventh bit may also be added for greater resolution. The DAC-01 is ideal for CRT deflection circuits, servo positioning controls, digitally programmed power supplies and pulse generators, modem and telephone system digitizing and demodulation circuits, digital filters, and 6-bit A/D converters. Introduced in 1970, the DAC-01 is still the fastest, lowest power, most accurate 6-bit complete monolithic DAC ever made.

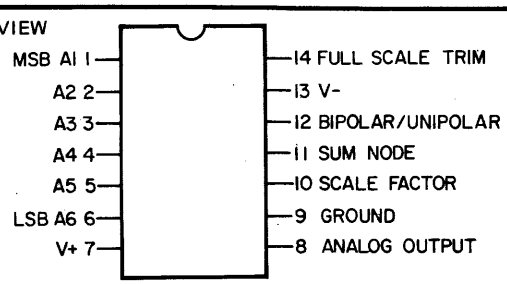
FEATURES

- Fast . . . . . 3μsec Settling Time (Max)
- Complete . . . . Includes Reference, Ladder, Op Amp
- Low Power Consumption . . . . . 250 mW (Max)
- 6-Bit Resolution . . . . . 7 Bit Accuracy
- 3 Output Options . . . . . +10V, ±5V, ±10V
- Standard Power Supplies . . . . . ±12V to ±18V
- −55°/+125°C or 0°/70°C Ranges Available
- TTL, DTL Compatible Logic Levels
- Models With MIL-STD-883A Class B Processing Available From Stock
- Low Cost

SIMPLIFIED SCHEMATIC



PIN CONNECTIONS AND ORDERING INFORMATION



14 PIN HERMTIC DIP (Y-Suffix)

ORDER: DAC-01Y DAC-01CY
DAC-01BY DAC-01HY
DAC-01FY DAC-01DY

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:

ORDER: DAC01-883-Y
DAC01-883-BY
DAC01-883-FY

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ABSOLUTE MAXIMUM RATINGS

Operating Temperature	
DAC-01, DAC-01B, DAC-01F	−55°C to +125°C
DAC-01C, DAC-01H, DAC-01D	0°C to +70°C
V+ Supply Voltage to Ground	0 to +18V
V− Supply Voltage to Ground	0 to −18V
Logic Input to Ground	−0.7 to +6V
Internal Power Dissipation (Note 1)	500 mW
Storage Temperature	−65°C to +150°C
Lead Soldering Temperature	300°C (60 sec)
Output Short Circuit Duration (Note 2)	Indefinite

NOTE 1: Rating applies up to ambient temperatures of 100°C. For temperatures above 100°C, derate linearly at 10mW/°C.

NOTE 2: Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V and over the rated operating temperature range unless otherwise noted.

Parameter	DAC-01	DAC-01B	DAC-01F	DAC-01C	DAC-01H	DAC-01D	Units
Output Options	Unipolar Bipolar	Unipolar Bipolar	Unipolar	Unipolar Bipolar	Unipolar	Unipolar Bipolar	
Temperature Range	−55/+125	−55/+125	−55/+125	0/+70	0/+70	0/+70	°C
Nonlinearity 25°C — Max	±0.40	±0.40	±0.40	±0.40	±0.40	±0.78	%FS
Nonlinearity Over Temperature — Max	±0.45	±0.45	±0.45	±0.45	±0.45	±0.78	%FS
Full Scale Tempco — Max	±80	±120	±80	±160	±160	±160	ppm/°C
Unipolar Zero Scale Output Voltage — Max (Note 1, 2)	25	25	40	25	40	50	mV

These specifications apply for all DAC-01 grades, V_S = ±15V and over the rated operating temperature range unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Unipolar Full Scale Output Voltage (Note 3)	2KΩ load, logic ≤ 0.5V, short pin 13 to pin 14. Short pin 12 to Ground and pin 10 to pin 11.	+10.00	—	+11.75	Volts
Bipolar Output Voltage (Note 3)	2KΩ Load, Short pin 11 to pin 12.				
±5 Volt Range	Short pin 13 to pin 14, Short pin 10 to pin 11.				
V_{FS+}	Logic Inputs ≤ 0.5V	+4.93	—	+5.94	Volts
V_{FS-}	Logic Inputs ≥ 2.1V	−5.94	—	−4.93	Volts
±10 Volt Range	Open pin 10				
V_{FS+}	Logic Inputs ≤ 0.5V	+9.86	—	+11.89	Volts
V_{FS-}	Logic Inputs ≥ 2.1V	−11.89	—	−9.86	Volts
Bipolar Offset Voltage (Note 1) ±1/2 (I V_{FS+} I−I V_{FS-}I)	±5 Volt Range ±10 Volt Range	— —	±40 ±80	±70 ±140	mV mV
Resolution		—	—	6	bits
Logic Input "0"		—	—	0.5	Volts
Logic Input "1"		2.1	—	—	Volts
Logic Input Current, Each Input		—	2.2	8	μA
Power Supply Sensitivity	±12V ≤ V_S ≤ ±18V V_{FS} ≅ 10.0 V	—	±0.01	±0.15	%V_{FS}/V
Power Consumption		—	200	250	mW
Settling Time to ±1/2 LSB	2.1V ≤ logic level ≤ 0.5V T_A = 25°C.	—	1.5	3	μsec

NOTES:

1. Zero scale or bipolar offset voltage can be trimmed to zero volts or to the exact one's or two's complement condition with an external resistor network to pin 11.
2. Logic input voltage ≥ 2.1 volts.
3. Full scale is adjustable to precisely 10 volts for unipolar operation and 10 volt or 20 volt p-p bipolar operation with an external 500 ohm potentiometer from pin 14 to V−.

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DAC-03

8 & 10 BIT LOW COST MONOLITHIC D/A CONVERTER

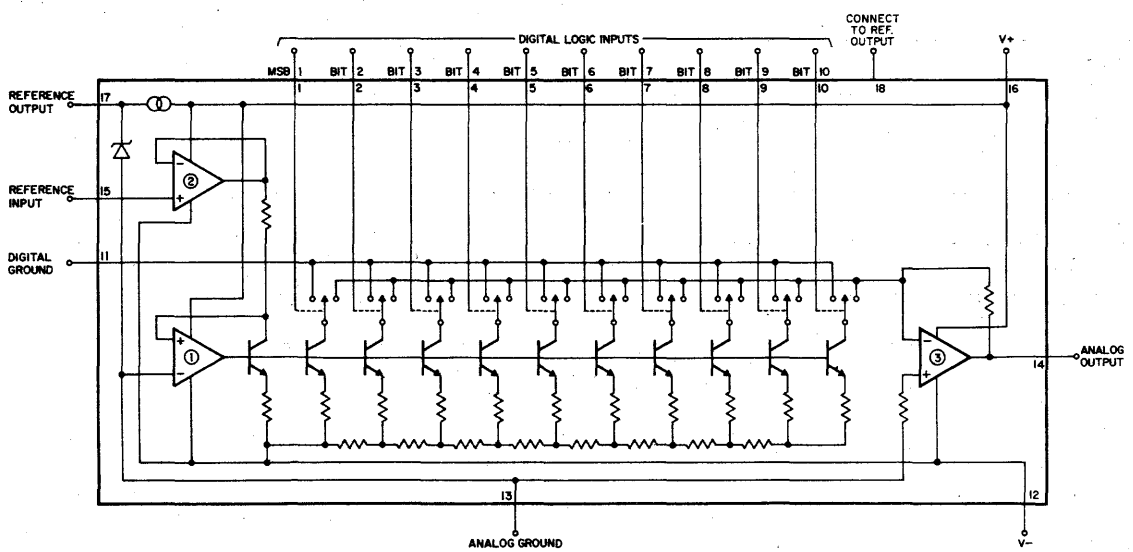
GENERAL DESCRIPTION

The DAC-03 is a complete 10 bit low cost D/A converter on a single 82 x 148 mil monolithic chip. All elements of a complete DAC are included—precision voltage reference, current steering logic, current sources, R-2R resistor network and high speed internally compensated output op amp. The untrimmed diffused R-2R resistor ladder network achieves monotonic operation over a wide temperature range. The buffered reference input is capable of tracking over a wide range of voltages, increasing application flexibility. The wide power supply range, low power consumption and choice of full scale output voltages assure utility in a wide range of applications including CRT displays, data acquisition systems, A/D converters, and servo positioning controls. For bipolar DAC's refer to the DAC-02 and DAC-04 data sheets.

FEATURES

- Monotonicity Guaranteed
- Low Cost
- Complete . . . . . Includes Reference and Op Amp
- Compact . . . . . Single 18 Pin DIP Package
- Fast . . . . . 1.5 μsec Settling Time
- Stable . . . . . Full Scale Tempco 60 ppm/°C
- Standard Power Supplies . . . . . ±12V to ±18V
- Low Power Consumption . . . . . 350 mW Max
- TTL, DTL, CMOS Compatible Inputs
- 5V and 10V Models Available

SIMPLIFIED SCHEMATIC AND PIN CONNECTION DIAGRAM



ORDERING INFORMATION

MODEL	MONOTONICITY	TEMP RANGE	FS TEMPCO	PACKAGE
DAC-03 ADX1 (or X2)*	10 BITS	0°/+70°C	60 ppm/°C TYP	18 PIN DIP
DAC-03 BDX1 (or X2)*	9 BITS	0°/+70°C	60 ppm/°C TYP	18 PIN DIP
DAC-03 CDX1 (or X2)*	8 BITS	0°/+70°C	60 ppm/°C TYP	18 PIN DIP
DAC-03 DDX1 (or X2)*	7 BITS	0°/+70°C	60 ppm/°C TYP	18 PIN DIP

*Suffix X1 indicates +10V output; suffix X2 indicates +5V output.

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ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0° to +70°C	Internal Reference Output Current	300μA
Storage Temperature Range	−65°C to +150°C	Reference Input Voltage	0 to +10V
V+ Supply to Analog Ground	0 to +18V	Internal Power Dissipation	500 mW
V− Supply to Analog Ground	0 to −18V	Lead Soldering Temperature	300°C (60 sec)
Analog Ground to Digital Ground	0 to ±0.5V	Output Short Circuit Duration	Indefinite
Logic Inputs to Digital Ground	−5V to (V_+ −.7V)	(Short circuit may be to ground or either supply.)	

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V and T_A = 25°C unless otherwise specified.

Parameter	Condition	Min	Typ	Max	Units
Resolution		10	10	10	bits
Monotonicity	Grade AD	10	–	–	bits
	Grade BD	9	–	–	bits
	Grade CD	8	–	–	bits
	Grade DD	7	–	–	bits
Nonlinearity	Grade AD	–	–	±0.1	%
	Grade BD	–	–	±0.1	%
	Grade CD	–	–	±0.2	%
	Grade DD	–	–	±0.4	%
Settling Time	To ±1/2 LSB, 10 Volt Step	–	1.5	–	μsec
Full Scale Tempco	Total, Internal Reference Connected	–	60	–	ppm/°C
Full Scale Tempco	External Reference	–	±40	–	ppm/°C
Reference Input Bias Current		–	100	–	nA
Reference Input Impedance		–	200	–	MΩ
Reference Input Slew Rate		–	1.5	–	V/μsec
Reference Output Voltage		–	6.7	–	V
Zero Scale Offset		–	±1.0	±10	mV
Power Supply Sensitivity	V_S = ±12V to ±18V	–	±.015	±0.1	% V_{FS}/V
Power Dissipation	I_{OUT} = 0	–	225	350	mW
Logic Input Current	(Each Input, −5V to (V_+ −.7V)	–	1	–	μA
Logic Input "0"		–	–	0.8	V
Logic Input "1"		2.0	–	–	V
Full Scale Output Voltage					
10 Volt Models (X1)	(See Note)	+10.0	–	+11.5	V
5 Volt Models (X2)		+5.00	–	+5.75	V

NOTE: Reference Output terminal connected directly to Reference Input terminal and pin 18; R_L = 2KΩ, all logic inputs ≥ 2.0 V.

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IMPROVED DAC-02

DAC-05

11 BIT DIGITAL TO ANALOG CONVERTER
(10 BITS PLUS SIGN)

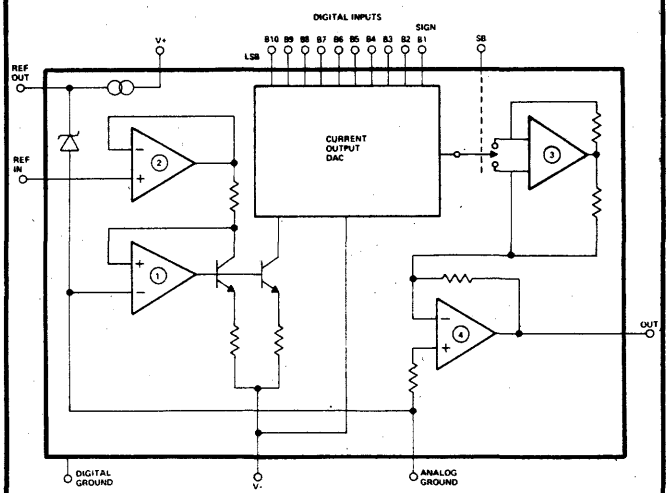
GENERAL DESCRIPTION

The DAC-05 is a complete, monolithic, Sign Plus 10 Bit DAC with a voltage output. A precision voltage reference, a logic-controlled polarity switch, and a high speed (1.5 μsec settling time) output op amp are included. Monotonicity, non-linearity, power consumption, and full scale temperature coefficient are guaranteed over the full operating temperature range. Reliability is enhanced by a monolithic design, 100% burn-in, and a hermetic DIP package. Six low cost 0°/70°C and six -55°/+125°C models are available plus six models with MIL-STD-883A Class B processing.

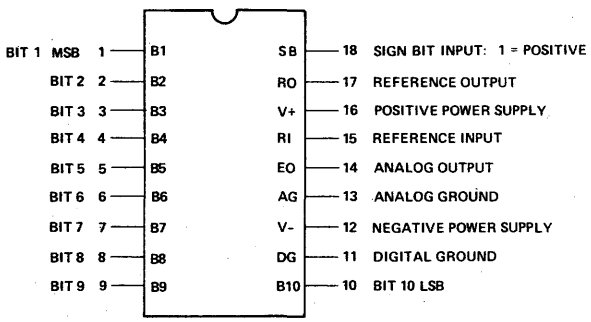
FEATURES

- **Complete** ..... Includes Reference and Op Amp
- **Bipolar Output** ..... Sign/Magnitude Coding
- **Fast** ..... 1.5 μsec Settling Time
- **Monotonicity and Nonlinearity Guaranteed**
- **Reliable** ..... 100% Burned-in 72 Hrs @+125°C
- **Low Power Consumption** ..... 350 mW Max
- **Compact** ..... Single 18 Pin Hermetic DIP Package
- **Choice of Output Ranges** ..... ±5V or ±10V
- **Models with MIL-STD-883A Class B Processing Available From Stock**

SIMPLIFIED SCHEMATIC



PIN CONNECTIONS



TOP VIEW
18 PIN HERMETIC DUAL-IN-LINE
(X-Suffix)

ORDERING INFORMATION

MODEL	MONOTONICITY	TEMP RANGE
DAC-05AX1 (or 2)	10 BITS	-55°/+125°C
DAC-05BX1 (or 2)	9 BITS	-55°/+125°C
DAC-05CX1 (or 2)	8 BITS	-55°/+125°C
DAC-05EX1 (or 2)	10 BITS	0°/+70°C
DAC-05FX1 (or 2)	9 BITS	0°/+70°C
DAC-05GX1 (or 2)	8 BITS	0°/+70°C

NOTE: Use suffix X1 for ±10V output or suffix X2 for ±5V output.

Military Temperature Range Devices with MIL-STD-883A Class B Processing:

MODEL	MONOTONICITY
DAC 05-883-AX1 (or 2)	10 BITS
DAC 05-883-BX1 (or 2)	9 BITS
DAC 05-883-CX1 (or 2)	8 BITS

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ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range		Analog Ground to Digital Ground	0 to ±0.5V
DAC-05A,B,C	-55°C to +125°C	Logic Inputs to Digital Ground	-5V to (V_+ – .7V)
DAC-05E,F,G	0°C to +70°C	Internal Reference Output Current	300μA
Storage Temperature Range	-65°C to +150°C	Reference Input Voltage	0 to +10V
V+ Supply to Analog Ground	0 to +18V	Internal Power Dissipation	500 mW
V-Supply to Analog Ground	0 to -18V	Lead Soldering Temperature	300°C (60 sec)
		Output Short Circuit Duration	Indefinite
		(Short circuit may be to ground or either supply.	

ELECTRICAL CHARACTERISTICS — MILITARY GRADES

These specifications apply for V_S = ±15V and T_A = -55°C to +125°C unless otherwise specified.

			DAC-05A			DAC-05B			DAC-05C			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Resolution		Including Sign	11	11	11	11	11	11	11	11	11	bits
Monotonicity			10	–	–	9	–	–	8	–	–	bits
Nonlinearity	NL	T_A = 0°C to +70°C	–	–	±0.1	–	–	±0.2	–	–	±0.4	%FS
		T_A = -55°C to +125°C	–	–	±0.2	–	–	±0.3	–	–	±0.5	%FS
Full Scale Tempco	TCV_{FS}	Internal Reference Connected	–	30	60	–	45	90	–	60	120	ppm/°C
		External Reference Connected	–	30	–	–	30	–	–	30	–	ppm/°C
Full Scale Output Voltage (X1 Suffix)	V_{FS+}	Sign Bit High (Note 1)	+10.0	–	+11.5	+10.0	–	+11.5	+10.0	–	+11.5	V
	V_{FS-}	Sign Bit Low (Note 1)	-11.5	–	-10.0	-11.5	–	-10.0	-11.5	–	-10.0	V
Full Scale Output Voltage (X2 Suffix)	V_{FS+}	Sign Bit High (Note 1)	+5.00	–	+5.75	+5.00	–	+5.75	+5.00	–	+5.75	V
	V_{FS-}	Sign Bit Low (Note 1)	-5.75	–	-5.00	-5.75	–	-5.00	-5.75	–	-5.00	V
Zero Scale Offset (Sign Bit High, All Others Low)	V_{FS+}	T_A = +25°C	–	1.0	5.0	–	1.0	5.0	–	1.0	5.0	mV
		T_A = -55°C to +125°C	–	2.0	10	–	2.0	10	–	2.0	10	mV
Zero Scale Symmetry (X1 Suffix)		(Note 2)	–	±4.0	±10	–	±4.0	±10	–	±4.0	±10	mV
Zero Scale Symmetry (X2 Suffix)		(Note 2)	–	±2.0	±5.0	–	±2.0	±5.0	–	±2.0	±5.0	mV
Full Scale Bipolar Symmetry (X1 Suffix)		T_A = +25°C (Note 3)	–	±10	±50	–	±10	±50	–	±10	±50	mV
		T_A = -55°C to +125°C	–	±20	±70	–	±20	±70	–	±20	±70	mV
Full Scale Bipolar Symmetry (X2 Suffix)		T_A = +25°C (Note 3)	–	±5.0	±25	–	±5.0	±25	–	±5.0	±25	mV
		T_A = -55°C to +125°C	–	±10	±35	–	±10	±35	–	±10	±35	mV
Settling Time	t_s	To ± ½ LSB, 10V Change	–	1.5	–	–	1.5	–	–	1.5	–	μsec
Reference Input Slew Rate			–	1.5	–	–	1.5	–	–	1.5	–	V/μsec
Reference Input Bias Current			–	100	–	–	100	–	–	100	–	nA
Reference Input Impedance			–	200	–	–	200	–	–	200	–	MΩ
Reference Output Voltage			–	6.7	–	–	6.7	–	–	6.7	–	V
Logic Input Current	I_{IN}	Each Input, -5V to (V+ – .7V)	–	±1.0	±10	–	±1.0	±10	–	±1.0	±10	μA
Logic Input "0"	V_{IL}		–	–	0.8	–	–	0.8	–	–	0.8	V
Logic Input "1"	V_{IH}		2.0	–	–	2.0	–	–	2.0	–	–	V
Power Supply Sensitivity (V_S = ±12V to ±18V)		T_A = +25°C	–	0.02	0.05	–	0.02	0.05	–	0.02	0.05	$\%V_{FS}/V$
		T_A = -55°C to +125°C	–	0.05	0.1	–	0.05	0.1	–	0.05	0.1	$\%V_{FS}/V$
Power Dissipation (I_{OUT} = 0)		T_A = +25°C	–	200	300	–	200	300	–	200	300	mW
		T_A = -55°C to +125°C	–	250	350	–	250	350	–	250	350	mW

NOTE 1: Reference Output terminal connected directly to Reference Input terminal, R_L = 2KΩ, all logic inputs ≥ 2.0 V.

NOTE 2: Zero Scale Symmetry is the change in the output voltage produced by switching the Sign Bit with all logic bits low (V_{ZS+} -V_{ZS-}).

NOTE 3: Full Scale Bipolar Symmetry is the magnitude of the difference between $|V_{FS+}|$ and $|V_{FS-}|$.

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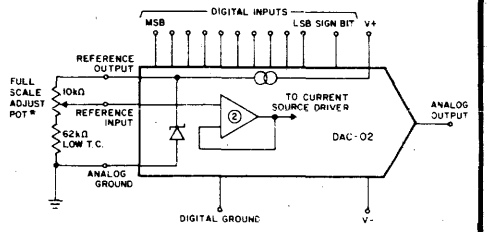
CONNECTION INFORMATION

FULL SCALE ADJUSTMENT - Full Scale output voltage may be trimmed by use of a potentiometer and series resistor as shown; however, best results will be obtained if a low tempco resistor is used or if pot and resistor tempcos match. Alternatively, a single pot of ⩾ 75KΩ may be used.

REFERENCE INPUT BYPASS - Lowest noise and fastest settling operation will be obtained by bypassing the Reference Input to Analog Ground with a 0.01μF disk capacitor

GROUNDING - For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably near the DAC-05 package, so that the large digital currents do not flow through the analog ground path.

FULL SCALE ADJUSTMENT CIRCUIT



ELECTRICAL CHARACTERISTICS— COMMERCIAL GRADES

These specifications apply for V_S = ±15V and T_A = 0°C to +70°C unless otherwise specified.

			DAC-05E			DAC-05F			DAC-05G			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Resolution		Including Sign	11	11	11	11	11	11	11	11	11	bits
Monotonicity			10	–	–	9	–	–	8	–	–	bits
Nonlinearity	NL	T_A = +25°C	–	–	±0.1	–	–	±0.2	–	–	±0.4	%FS
		T_A = 0°C to 70°C	–	–	±0.2	–	–	±0.3	–	–	±0.5	%FS
Full Scale Tempco (Note 4)	TCV_{FS}	Internal Reference Connected	–	45	100	–	45	100	–	45	100	ppm/°C
		External Reference Connected	–	30	–	–	30	–	–	30	–	ppm/°C
Full Scale Output Voltage (X1 Suffix)	V_{FS+}	Sign Bit High (Note 1)	+10.0	–	+11.5	+10.0	–	+11.5	+10.0	–	+11.5	V
	V_{FS-}	Sign Bit Low (Note 1)	-11.5	–	-10.0	-11.5	–	-10.0	-11.5	–	-10.0	V
Full Scale Output Voltage (X2 Suffix)	V_{FS+}	Sign Bit High (Note 1)	+5.00	–	+5.75	+5.00	–	+5.75	+5.00	–	+5.75	V
	V_{FS-}	Sign Bit Low (Note 1)	-5.75	–	-5.00	-5.75	–	-5.00	-5.75	–	-5.00	V
Zero Scale Offset (Sign Bit High, All Others Low)	V_{ZS+}	T_A = 25°C	–	1.0	5.0	–	1.0	5.0	–	1.0	5.0	mV
		T_A = 0°C to +70°C	–	2.0	10	–	2.0	10	–	2.0	10	mV
Zero Scale Symmetry (X1 Suffix)		(Note 2)	–	±4.0	±10	–	±4.0	±10	–	±4.0	±10	mV
Zero Scale Symmetry (X2 Suffix)		(Note 2)	–	±2.0	±5.0	–	±2.0	±5.0	–	±2.0	±5.0	mV
Full Scale Bipolar Symmetry (X1 Suffix)		T_A = +25°C (Note 3)	–	±10	±50	–	±10	±50	–	±10	±50	mV
		T_A = 0°C to +70°C	–	±20	±70	–	±20	±70	–	±20	±70	mV
Full Scale Bipolar Symmetry (X2 Suffix)		T_A = +25°C (Note 3)	–	±5.0	±25	–	±5.0	±25	–	±5.0	±25	mV
		T_A = 0°C to +70°C	–	±10	±35	–	±10	±35	–	±10	±35	mV
Settling Time		To ± ½ LSB, 10V Change	–	1.5	–	–	1.5	–	–	1.5	–	μsec
Reference Input Slew Rate			–	1.5	–	–	1.5	–	–	1.5	–	V/μsec
Reference Input Bias Current			–	100	–	–	100	–	–	100	–	nA
Reference Input Impedance			–	200	–	–	200	–	–	200	–	MΩ
Reference Output Voltage			–	6.7	–	–	6.7	–	–	6.7	–	V
Logic Input Current	I_{IN}	Each Input, -5V to (V+ – .7V)	–	±1.0	±10	–	±1.0	±10	–	±1.0	±10	μA
Logic Input "0"	V_{IL}		–	–	0.8	–	–	0.8	–	–	0.8	V
Logic Input "1"	V_{IH}		2.0	–	–	2.0	–	–	2.0	–	–	V
Power Supply Sensitivity (V_S = ±12V to ±18V)		T_A = +25°C	–	0.02	0.05	–	0.02	0.05	–	0.02	0.05	$\%V_{FS}/V$
		T_A = 0°C to +70°C	–	0.05	0.1	–	0.05	0.1	–	0.05	0.1	$\%V_{FS}/V$
Power Dissipation (I_{OUT} = 0)		T_A = +25°C	–	200	300	–	200	300	–	200	300	mW
		T_A = 0°C to +70°C	–	250	350	–	250	350	–	250	350	mW

NOTE 1: Reference Output terminal connected directly to Reference Input terminal, R_L = 2KΩ, all logic inputs ⩾ 2.0 V.

NOTE 2: Zero Scale Symmetry is the change in the output voltage produced by switching the Sign Bit with all logic bits low (V_{ZS+} -V_{ZS-}).

NOTE 3: Full Scale Bipolar Symmetry is the magnitude of the difference between $|V_{FS+}|$ and $|V_{FS-}|$.

NOTE 4: Parameter is not 100% tested; 90% of units meet this specification.

IMPROVED DAC-04

DAC-06

TWO'S COMPLEMENT 10 BIT D/A CONVERTER

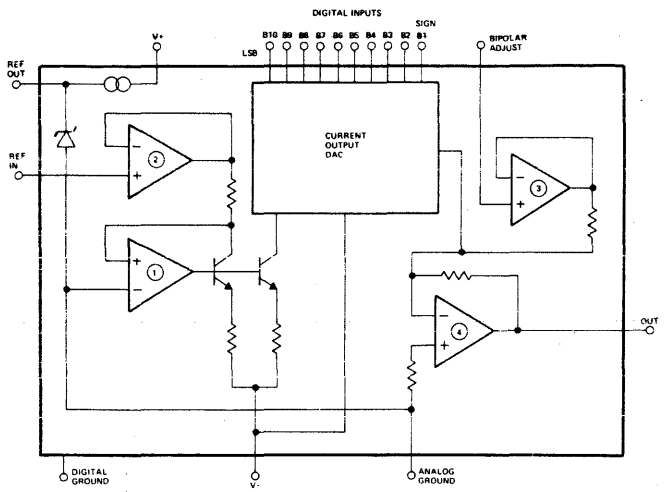
GENERAL DESCRIPTION

The DAC-06 is a complete, monolithic, Two's Complement 10 Bit DAC with a voltage output. A precision voltage reference, R-2R resistor network, bipolar offset circuit, and a high speed (1.5 μsec settling time) output op amp are included. Monotonicity, nonlinearity, power consumption, and full scale temperature coefficient are guaranteed over the full operating temperature range. Reliability is enhanced by a monolithic design, 100% burn-in, and a hermetic DIP package. Three low cost 0°/70°C and three -55°/+125°C models are available plus three models with MIL-STD-883A Class B processing.

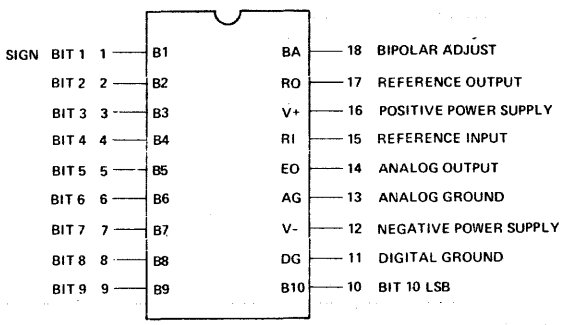
FEATURES

- Complete . . . . . Includes Reference and Op Amp
- Bipolar Output . . . . . Two's Complement Coding
- Fast . . . . . 1.5 μsec Settling Time
- Monotonicity and Nonlinearity Guaranteed
- Reliable . . . . . 100% Burned-in 72 Hrs @ +125°C
- Low Power Consumption . . . . . 350 mW Max
- Compact . . . . Single 18 Pin Hermetic DIP Package
- Models with MIL-STD-883A Class B Processing Available From Stock

SIMPLIFIED SCHEMATIC



PIN CONNECTIONS



TOP VIEW

18 PIN HERMETIC DUAL-IN-LINE
(X-Suffix)

ORDERING INFORMATION

MODEL	MONOTONICITY	TEMP RANGE
DAC-06AX	10 BITS	-55°/+125°C
DAC-06BX	9 BITS	-55°/+125°C
DAC-06CX	8 BITS	-55°/+125°C
DAC-06EX	10 BITS	0°/+70°C
DAC-06FX	9 BITS	0°/+70°C
DAC-06GX	8 BITS	0°/+70°C

Military Temperature Range Devices with MIL-STD-883A Class B Processing:

MODEL	MONOTONICITY
DAC06-883-AX	10 BITS
DAC06-883-BX	9 BITS
DAC06-883-CX	8 BITS

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ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range		Internal Reference Output Current	300μA
DAC-06A, B, C	-55°C to +125°C	Reference Input Voltage	0 to +10V
DAC-06E, F, G	0°C to +70°C	Bipolar Offset Input Voltage	0 to +10V
Storage Temperature Range	-65°C to +150°C	Internal Power Dissipation	500 mW
V+ Supply to Analog Ground	0 to +18V	Lead Soldering Temperature	300°C (60 sec)
V- Supply to Analog Ground	0 to -18V	Output Short Circuit Duration	Indefinite
Analog Ground to Digital Ground	0 to ±0.5V	(Short circuit may be to ground or either supply.)	
Logic Inputs to Digital Ground	-5V to (V_+ - .7V)		

DAC-06 DEFINITIONS

FULL SCALE OUTPUT RANGE—The peak-to-peak voltage swing of the converter's output, i.e. $|V_{FS+}|+|V_{FS-}|$ for bipolar operation, and (V_{FS}-V_{ZS}) for unipolar operation.

POSITIVE BIPOLAR FULL SCALE OUTPUT VOLTAGE (V_{FS+})—The output for 0111111111 input code.

NEGATIVE BIPOLAR FULL SCALE OUTPUT VOLTAGE(V_{FS-})—The output voltage for 1000000001 input code for Two's Complement coding, or the output voltage for 1000000000 input code for One's Complement coding.

UNIPOLAR FULL SCALE OUTPUT VOLTAGE (V_{FS})—The (positive) output voltage for 0111111111 input code.

UNIPOLAR ZERO SCALE OUTPUT VOLTAGE (V_{ZS})—The output voltage for 1000000000 input code.

BIPOLAR OFFSET VOLTAGE 1/2($|V_{FS+}|-|V_{FS-}|$)—The maximum error due to asymmetry around zero output expressed as a percentage of Full Scale Output Range. (This is adjustable to zero—see Adjustment Procedures on the last page.)

LEAST SIGNIFICANT BIT (LSB)—The smallest incremental output change obtainable, which is ideally equal to the full scale output range divided by 2^{n-1}, where n = number of bits of resolution.

MOST SIGNIFICANT BIT (MSB)—The largest incremental output change obtainable by switching a single logic input, ideally equal to the ideal LSB multiplied by 2^{n-1}, where n = number of bits of resolution. In Two's and One's Complement Converters this MSB is inverted with respect to the other (binary) bits and is used as a sign bit; this feature is incorporated into the DAC-06 design.

MONOTONICITY—Having each successive output state greater than or equal to the preceding one when the DAC is sequenced through all successive states from V_{FS-} to V_{FS+}.

FULL SCALE TEMPERATURE COEFFICIENT—Change in absolute full scale output range in ppm between 25°C and either temperature extreme divided by the corresponding change in temperature.

POWER SUPPLY SENSITIVITY—The ratio of the percentage change in full scale output range to the change in the supply voltage producing it.

ELECTRICAL CHARACTERISTICS – MILITARY GRADES

These specifications apply for V_S = ±15V and T_A = -55°C to +125°C unless otherwise specified.

			DAC-06A			DAC-06B			DAC-06C			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Resolution			10	10	10	10	10	10	10	10	10	bits
Monotonicity			10	–	–	9	–	–	8	–	–	bits
Nonlinearity	NL	T_A = 0°C to 70°C	0.1	–	–	0.2	–	–	0.4	–	–	%FSR
		T_A = -55°C to +125°C	0.2	–	–	0.3	–	–	0.5	–	–	%FSR
Full Scale Tempco	TCV_{FS}	Internal Reference Connected	–	30	60	–	45	90	–	60	120	ppm/°C
		External Reference Connected	–	30	–	–	30	–	–	30	–	ppm/°C
Full Scale Output Range	FSR	$\|V_{FS-}\| + \|V_{FS+}\|$ (Note 1)	10	–	11.5	10	–	11.5	10	–	11.5	V
Unipolar Zero Scale Output Voltage (Pin 18 to Pin 11)	V_{ZS}	T_A = +25°C	–	1.0	5.0	–	1.0	5.0	–	1.0	5.0	mV
		T_A = -55°C to +125°C	–	2.0	10	–	2.0	10	–	2.0	10	mV
Bipolar Offset Voltage (Pin 15 to 18 and 17)		$½(\|V_{FS+}\|-\|V_{FS-}\|)$	-5.0	–	-0.1	-5.0	–	-0.1	-5.0	–	-0.1	%FSR
Settling Time	t_s	To ±½ LSB, 10 Volt Step	–	1.5	–	–	1.5	–	–	1.5	–	μsec
Reference Input Slew Rate			–	1.5	–	–	1.5	–	–	1.5	–	V/μsec
Reference Input Bias Current			–	100	–	–	100	–	–	100	–	nA
Reference Input Impedance			–	200	–	–	200	–	–	200	–	MΩ
Reference Output Voltage			–	6.7	–	–	6.7	–	–	6.7	–	V
Logic Input Current	I_{IN}	Each Input, -5V to (V+ – .7V)	–	±1.0	±10	–	±1.0	±10	–	±1.0	±10	μA
Logic Input "0"	V_{IL}		–	–	0.8	–	–	0.8	–	–	0.8	V
Logic Input "1"	V_{IH}		2.0	–	–	2.0	–	–	2.0	–	–	V
Power Supply Sensitivity (V_S = ±12V to ±18V)		T_A = +25°C	–	0.02	0.05	–	0.02	0.05	–	0.02	0.05	%FS/V
		T_A = -55°C to +125°C	–	0.05	0.1	–	0.05	0.1	–	0.05	0.1	%FS/V
Power Dissipation (I_{OUT} = 0)		T_A = +25°C	–	200	300	–	200	300	–	200	300	mW
		T_A = -55°C to +125°C	–	250	350	–	250	350	–	250	350	mW

NOTE 1: Reference output terminal connected to Reference Input terminal and to Bipolar Adjust terminal with R_L = 2KΩ.

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CONNECTION INFORMATION

EXTERNAL ADJUSTMENTS - Full Scale Range and Bipolar Symmetry may be adjusted using the connections shown with the procedures on the next page.

REFERENCE INPUT BYPASS - Lowest noise and fastest settling operation will be obtained by bypassing the Reference Input and the Bipolar Offset Adjust inputs with 0.01μF disc capacitors connected to Analog Ground.

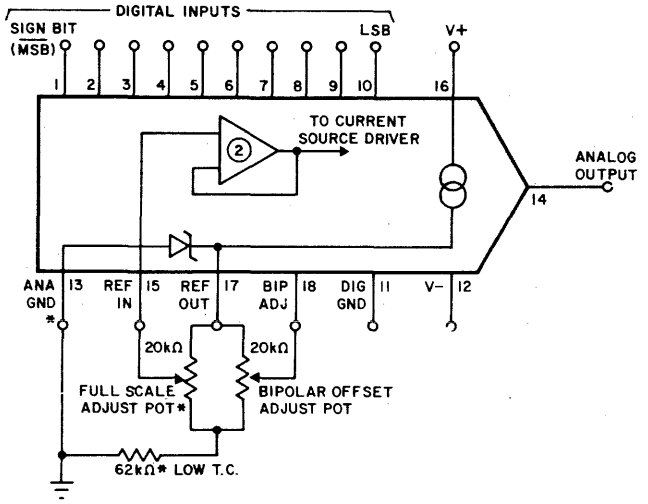
GROUNDING - For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably at the DAC-06 package, so that large digital currents do not flow through the analog ground path.

REFERENCE OUTPUT - For best results, Reference Output current should not exceed 100μA.

USE WITH EXTERNAL REFERENCES - Positive-polarity external reference voltages referred to Analog Ground may be applied to the Reference Input terminal to improve full scale tempco, to provide tracking to other system elements, or to slave a number of DAC-06's to the Reference Output of any one of them.

UNIPOLAR OPERATION - Operation as a 10V positive output 10 bit converter may be implemented by permanently tying pin 18 to ground.

LOWER RESOLUTION APPLICATIONS - For applications not requiring full 10 bit resolution, unused logic inputs should be tied to ground.



NOTE: For unipolar operation, omit the Bipolar offset adjustment potentiometer.

ELECTRICAL CHARACTERISTICS — COMMERCIAL GRADES

These specifications apply for V_S = ±15V and T_A = 0°C to 70°C unless otherwise specified.

			DAC-06E			DAC-06F			DAC-06G			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Resolution			10	10	10	10	10	10	10	10	10	bits
Monotonicity			10	–	–	9	–	–	8	–	–	bits
Nonlinearity	NL	T_A = +25°C	0.1	–	–	0.2	–	–	0.4	–	–	%FSR
		T_A = 0°C to +70°C	0.2	–	–	0.3	–	–	0.5	–	–	%FSR
Full Scale Tempco (Note 2)	TCV_{FS}	Internal Reference Connected	–	45	100	–	45	100	–	45	100	ppm/°C
		External Reference Connected	–	30	–	–	30	–	–	30	–	ppm/°C
Full Scale Output Range	FSR	$\|V_{FS-}\| + \|V_{FS+}\|$ (Note 1)	10	–	11.5	10	–	11.5	10	–	11.5	V
Unipolar Zero Scale Output Voltage (Pin 18 to Pin 11)	V_{ZS}	T_A = +25°C	–	1.0	5.0	–	1.0	5.0	–	1.0	5.0	mV
		T_A = 0°C to +70°C	–	2.0	10	–	2.0	10	–	2.0	10	mV
Bipolar Offset Voltage (Pin 15 to 18 and 17)		$½(\|V_{FS+}\|-\|V_{FS-}\|)$	-5.0	–	-0.1	-5.0	–	-0.1	-5.0	–	-0.1	%FSR
Settling Time	t_s	To ±½ LSB, 10 Volt Step	–	1.5	–	–	1.5	–	–	1.5	–	μsec
Reference Input Slew Rate			–	1.5	–	–	1.5	–	–	1.5	–	V/μsec
Reference Input Bias Current			–	100	–	–	100	–	–	100	–	nA
Reference Input Impedance			–	200	–	–	200	–	–	200	–	MΩ
Reference Output Voltage			–	6.7	–	–	6.7	–	–	6.7	–	V
Logic Input Current	I_{IN}	Each Input, -5V to (V+ – .7V)	–	±1.0	± 10	–	±1.0	±10	–	±1.0	± 10	μA
Logic Input "0"	V_{IL}		–	–	0.8	–	–	0.8	–	–	0.8	V
Logic Input "1"	V_{IH}		2.0	–	–	2.0	–	–	2.0	–	–	V
Power Supply Sensitivity (V_S = ±12V to ±18V)		T_A = +25°C	–	0.02	0.05	–	0.02	0.05	–	0.02	0.05	%FS/V
		T_A = 0°C to +70°C	–	0.05	0.1	–	0.05	0.1	–	0.05	0.1	%FS/V
Power Dissipation (I_{OUT} = 0)		T_A = +25°C	–	200	300	–	200	300	–	200	300	mW
		T_A = 0°C to +70°C	–	250	350	–	250	350	–	250	350	mW

NOTE 1: Reference Output terminal connected to Reference Input terminal and to Bipolar Adjust terminal with R_L = 2KΩ.

NOTE 2: Parameter is not 100% tested; 90% of units meet this specification.

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IMPROVED 1408A/1508A

DAC-08

8 BIT HIGH SPEED MULTIPLYING D/A CONVERTER

UNIVERSAL DIGITAL LOGIC INTERFACE

GENERAL DESCRIPTION

The DAC-08 series of 8 bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design*achieves 85 nsec settling times with very low "glitch" and at low power consumption. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

High voltage compliance dual complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8 bit monotonicity, and nonlinearities as tight as ±0.1%over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 33 mW power consumption attainable at ±5V supplies.

FEATURES

- Fast Settling Output Current . . . . . 85 nsec
- Full Scale Current Prematched to ±1 LSB
- Direct Interface to TTL, CMOS, ECL, HTL, PMOS
- Nonlinearity to ±0.1% Max Over Temp Range
- High Output Impedance and Compliance . . −10V to +18V
- Differential Current Outputs
- Wide Range Multiplying Capability . . . . 1 MHz Bandwidth
- Low FS Current Drift . . . . . ±10ppm/°C
- Wide Power Supply Range . . . . . ±4.5V to ±18V
- Low Power Consumption . . . . . 33 mW @ ±5V
- Low Cost

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications; devices processed to MIL-STD-883A, Level B are available.

DAC-08 applications include 8 bit, 1 μsec A/D converters, servo-motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high speed modems and other applications where low cost, high speed and complete input/output versatility are required.

EQUIVALENT CIRCUIT

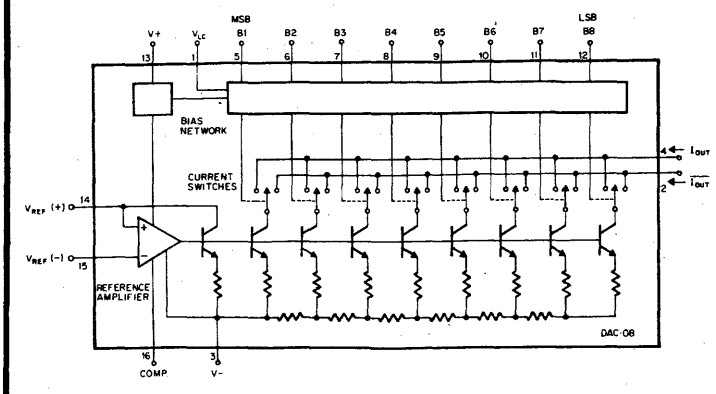
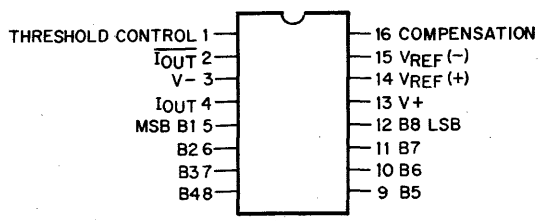


FIGURE 1

ORDERING INFORMATION AND PIN CONNECTION



TOP VIEW

16 PIN HERMETIC DUAL-IN-LINE
(Q-Suffix)

MODEL	TEMP RANGE	NONLINEARITY
DAC-08AQ	-55°/+125°C	±0.1%
DAC-08Q	-55°/+125°C	±0.19%
DAC-08HQ	0°/70°C	±0.1%
DAC-08EQ	0°/70°C	±0.19%
DAC-08CQ	0°/70°C	±0.39%

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:

ORDER: DAC-08-883-AQ
DAC-08-883-Q

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Operating Temperature		V+ Supply to V− Supply	36V
DAC-08AQ, Q	−55°C to +125°C	Logic Inputs	V− to V− plus 36V
DAC-08EQ, CQ	0°C to +70°C	V_{LC}	V− to V+
Storage Temperature	−65°C to +150°C	Analog Current Outputs	See Fig. 12
Power Dissipation	500mW	Reference Inputs (V_{14}, V_{15})	V− to V+
Derate above 100°C	10mW/°C	Reference Input Differential Voltage (V_{14} to V_{15})	±18V
Lead Soldering Temperature	300°C (60 sec)	Reference Input Current (I_{14})	5.0mA

TYPICAL PERFORMANCE PHOTOGRAPHS

FIGURE 2
TRUE AND COMPLEMENTARY OUTPUT OPERATION

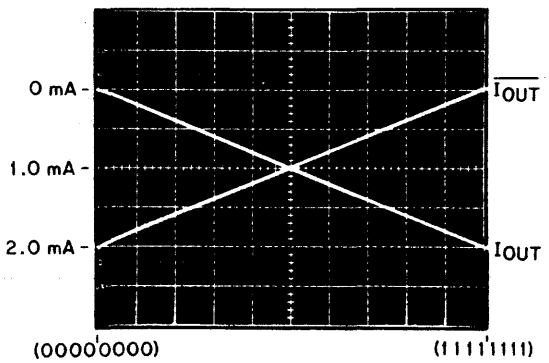
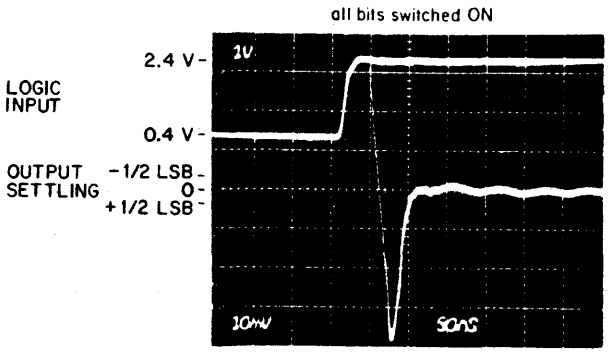


FIGURE 3
FULL SCALE SETTLING TIME



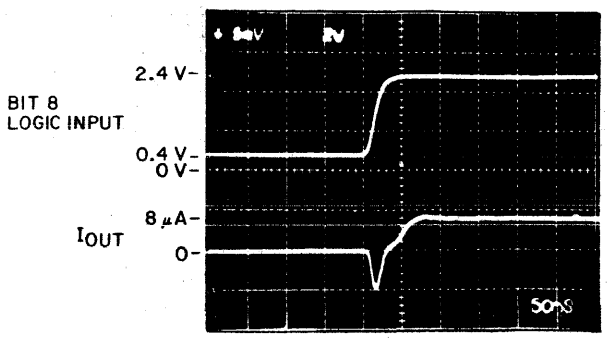
50 nsec/division

SETTLING TIME FIXTURE OF FIGURE 29

I_{FS} = 2mA R_L = 1K Ω

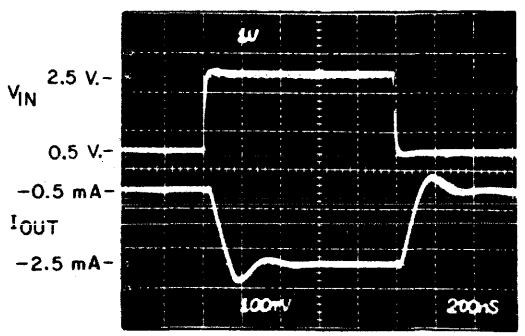
1/2 LSB = 4μA

FIGURE 4
LSB SWITCHING



50 nsec/division

FIGURE 5
FAST PULSED REFERENCE OPERATION



200 nsec/division

SEE FIGURE 27

$R_{EQ} \approx 200\Omega$

$R_L = 100\Omega$

$C_C = 0$

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ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, I_{REF} = 2.0 mA, T_A = −55°C to +125°C unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

			DAC-08A			DAC-08			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Resolution			8	8	8	8	8	8	bits
Monotonicity			8	8	8	8	8	8	bits
Nonlinearity		T_A = −55°C to +125°C	–	–	±0.1	–	–	±0.19	% FS
Settling Time	t_s	To ±½ LSB, all bits switched ON or OFF T_A = 25°C	–	85	135	–	85	135	nsec
Propagation Delay Each bit All bits switched	t_{PLH}, t_{PHL}	T_A = 25°C	 – –	 35 35	 60 60	 – –	 35 35	 60 60	 nsec nsec
Full Scale Tempco	TCI_{FS}		–	±10	±50	–	±10	±50	ppm/°C
Output Voltage Compliance	V_{OC}	Full scale current change <½ LSB R_{OUT} > 20 Megohm typ.	−10	–	+18	−10	–	+18	Volts
Full Scale Current	I_{FS4}	V_{REF} = 10.000V R_{14}, R_{15} = 5.000kΩ T_A = 25°C	1.984	1.992	2.000	1.94	1.99	2.04	mA
Full Scale Symmetry	I_{FSS}	$I_{FS4} - I_{FS2}$	–	±0.5	±4.0	–	±1.0	±8.0	μA
Zero Scale Current	I_{ZS}		–	0.1	1.0	–	0.2	2.0	μA
Output Current Range	I_{FSR}	V− = −5.0V V− = −7.0V to −18V	0 0	2.0 2.0	2.1 4.2	0 0	2.0 2.0	2.1 4.2	mA mA
Logic Input Levels Logic "0" Logic "1"	 V_{IL} V_{IH}	V_{LC} = 0V	 – 2.0	 – –	 0.8 –	 – 2.0	 – –	 0.8 –	 Volts Volts
Logic Input Current Logic "0" Logic "1"	 I_{IL} I_{IH}	V_{LC} = 0V V_{IN} = −10V to +0.8V V_{IN} = 2.0V to 18V	 – –	 −2.0 0.002	 −10 10	 – –	 −2.0 0.002	 −10 10	 μA μA
Logic Input Swing	V_{IS}	V− = −15V	−10	–	+18	−10	–	+18	Volts
Logic Threshold Range	V_{THR}	V_S = ±15V	−10	–	+13.5	−10	–	+13.5	Volts
Reference Bias Current	I_{15}		–	−1.0	−3.0	–	−1.0	−3.0	μA
Reference Input Slew Rate	dI/dt	See Figs. 5, 27	4.0	8.0	–	4.0	8.0	–	mA/μsec
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = 4.5V to 18V V− = −4.5V to −18V I_{REF} = 1.0 mA	– –	±0.0003 ±0.002	±0.01 ±0.01	– –	±0.0003 ±0.002	±0.01 ±0.01	%/% %/%
Power Supply Current	 I+ I−	V_S = ±5V, I_{REF} = 1.0 mA	 – –	 2.3 −4.3	 3.8 −5.8	 – –	 2.3 −4.3	 3.8 −5.8	 mA mA
	 I+ I−	V_S = +5V, −15V, I_{REF} = 2.0 mA	 – –	 2.4 −6.4	 3.8 −7.8	 – –	 2.4 −6.4	 3.8 −7.8	 mA mA
	 I+ I−	V_S = ±15V, I_{REF} = 2.0 mA	 – –	 2.5 −6.5	 3.8 −7.8	 – –	 2.5 −6.5	 3.8 −7.8	 mA mA
Power Dissipation	P_D	±5V, I_{REF} = 1.0 mA +5V, −15V, I_{REF} = 2.0 mA ±15V, I_{REF} = 2.0 mA	– – –	33 108 135	48 136 174	– – –	33 108 135	48 136 174	mW mW mW

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ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, I_{REF} = 2.0 mA, T_A = 0°C to 70°C unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

			DAC-08H			DAC-08E			DAC-08C			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Resolution			8	8	8	8	8	8	8	8	8	bits
Monotonicity			8	8	8	8	8	8	8	8	8	bits
Nonlinearity		T_A = 0°C to 70°C	–	–	±0.1	–	–	±0.19	–	–	±0.39	% FS
Settling Time	t_s	To ±½ LSB, all bits switched ON or OFF T_A = 25°C	–	85	135	–	85	150	–	85	150	nsec
Propagation Delay												
Each bit	t_{PLH}	T_A = 25°C	–	35	60	–	35	60	–	35	60	nsec
All bits switched	t_{PHL}		–	35	60	–	35	60	–	35	60	nsec
Full Scale Tempco	TCI_{FS}		–	±10	±50	–	±10	±50	–	±10	±80	ppm/°C
Output Voltage Compliance	V_{OC}	Full scale current change < ½ LSB R_{OUT} > 20 Megohm typ.	-10	–	+18	-10	–	+18	-10	–	+18	Volts
Full Scale Current	I_{FS4}	V_{REF} = 10.000V R_{14}, R_{15} = 5.000k Ω T_A = 25°C	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Scale Symmetry	I_{FSS}	$I_{FS4} - I_{FS2}$	–	±0.5	±4.0	–	±1.0	±8.0	–	±2.0	±16	μA
Zero Scale Current	I_{ZS}		–	0.1	1.0	–	0.2	2.0	–	0.2	4.0	μA
Output Current Range	I_{FSR}	V- = -5.0V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
		V- = -7.0V to -18V	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	mA
Logic Input Levels												
Logic "0"	V_{IL}	V_{LC} = 0V	–	–	0.8	–	–	0.8	–	–	0.8	Volts
Logic "1"	V_{IH}		2.0	–	–	2.0	–	–	2.0	–	–	Volts
Logic Input Current		V_{LC} = 0V										
Logic "0"	I_{IL}	V_{IN} = -10V to +0.8V	–	-2.0	-10	–	-2.0	-10	–	-2.0	-10	μA
Logic "1"	I_{IH}	V_{IN} = 2.0V to 18V	–	0.002	10	–	0.002	10	–	0.002	10	μA
Logic Input Swing	V_{IS}	V- = -15V	-10	–	+18	-10	–	+18	-10	–	+18	Volts
Logic Threshold Range	V_{THR}	V_S = ±15V	-10	–	+13.5	-10	–	+13.5	-10	–	+13.5	Volts
Reference Bias Current	I_{15}		–	-1.0	-3.0	–	-1.0	-3.0	–	-1.0	-3.0	μA
Reference Input Slew Rate	dI/dt	See Figs. 5, 27	4.0	8.0	–	4.0	8.0	–	4.0	8.0	–	mA/μsec
Power Supply Sensitivity	$PSSI_{FS+}$	V+ = 4.5V to 18V	–	±0.0003	±0.01	–	±0.0003	±0.01	–	±0.0003	±0.01	%/%
	$PSSI_{FS-}$	V- = -4.5V to -18V	–	±0.002	±0.01	–	±0.002	±0.01	–	±0.002	±0.01	%/%
		I_{REF} = 1.0 mA										
Power Supply Current		V_S = ±5V,										
	I+	I_{REF} = 1.0 mA	–	2.3	3.8	–	2.3	3.8	–	2.3	3.8	mA
	I-		–	-4.3	-5.8	–	-4.3	-5.8	–	-4.3	-5.8	mA
		V_S = +5V, -15V										
	I+	I_{REF} = 2.0 mA	–	2.4	3.8	–	2.4	3.8	–	2.4	3.8	mA
	I-		–	-6.4	-7.8	–	-6.4	-7.8	–	-6.4	-7.8	mA
		V_S = ±15V										
	I+	I_{REF} = 2.0 mA	–	2.5	3.8	–	2.5	3.8	–	2.5	3.8	mA
	I-		–	-6.5	-7.8	–	-6.5	-7.8	–	-6.5	-7.8	mA
Power Dissipation	P_D	±5V, I_{REF} = 1.0 mA	–	33	48	–	33	48	–	33	48	mW
		+5V, -15V, I_{REF} = 2.0 mA	–	108	136	–	103	136	–	108	136	mW
		±15V, I_{REF} = 2.0 mA	–	135	174	–	135	174	–	135	174	mW

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TYPICAL PERFORMANCE CURVES

FIGURE 6
FULL SCALE CURRENT VS. REFERENCE CURRENT

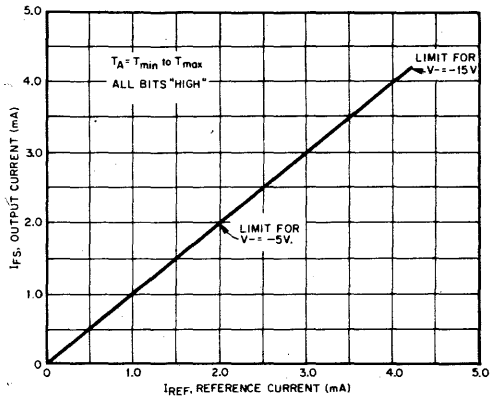


FIGURE 7
LSB PROPAGATION DELAY VS. I_{FS}

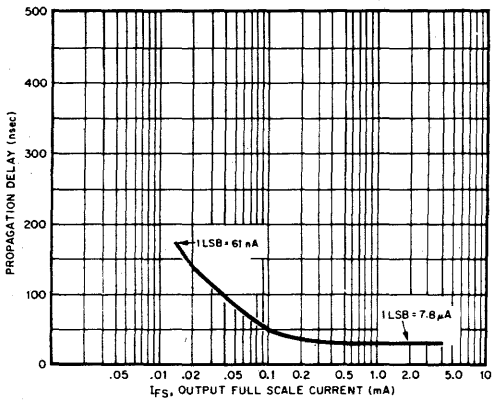
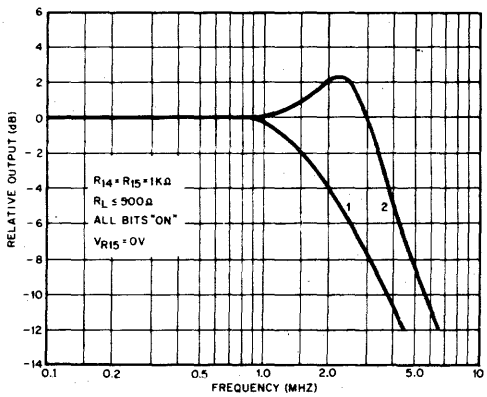
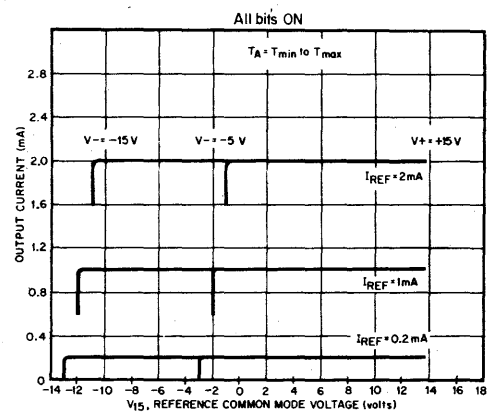


FIGURE 8
REFERENCE INPUT FREQUENCY RESPONSE



CURVE 1: C_C=15pF, V_{IN} = 2.0 Vp-p CENTERED AT +1.0 V. LARGE SIGNAL
CURVE 2: C_C=15pF, V_{IN} = 50mVp-p CENTERED AT +200mV. SMALL SIGNAL

FIGURE 9
REFERENCE AMP COMMON MODE RANGE



NOTE: POSITIVE COMMON MODE RANGE IS ALWAYS (V+) − 1.5 V

FIGURE 10
LOGIC INPUT CURRENT VS. INPUT VOLTAGE

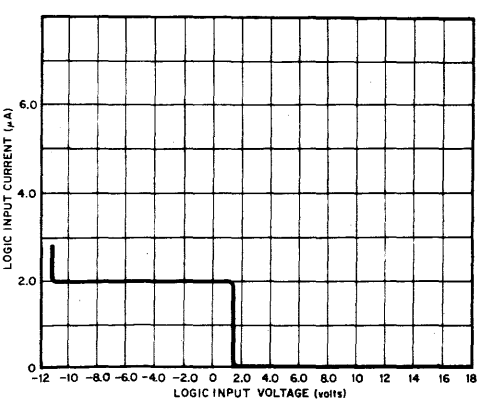
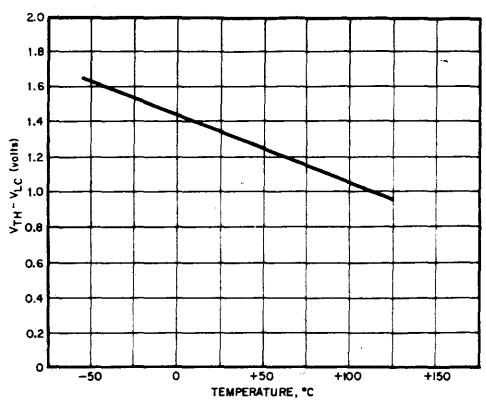


FIGURE 11
$V_{TH} - V_{LC}$ VS. TEMPERATURE



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TYPICAL PERFORMANCE CURVES

FIGURE 12
OUTPUT CURRENT VS. OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)

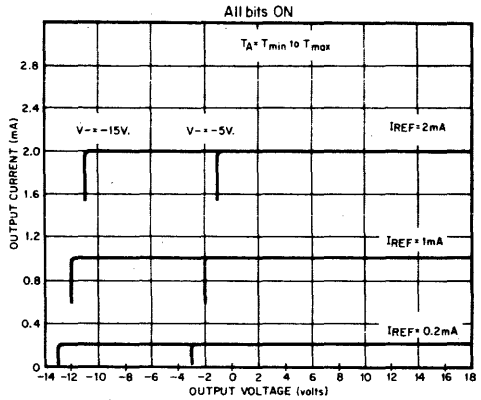


FIGURE 13
OUTPUT VOLTAGE COMPLIANCE VS. TEMPERATURE

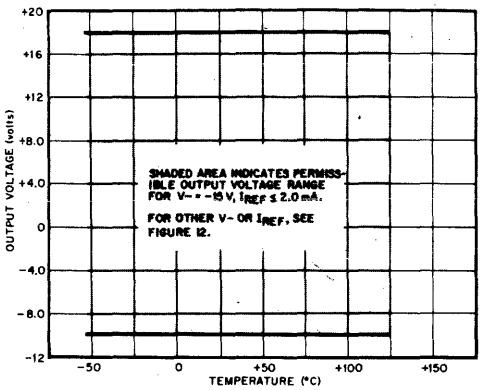
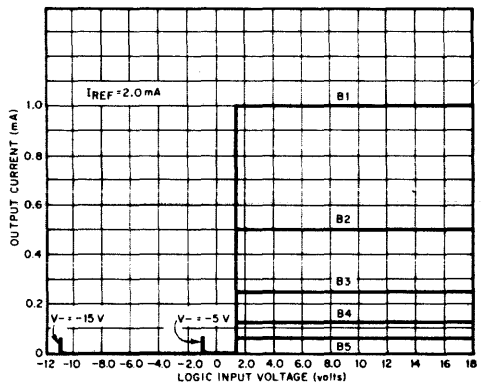


FIGURE 14
BIT TRANSFER CHARACTERISTICS



NOTE: B1 THROUGH B8 HAVE IDENTICAL TRANSFER CHARACTERISTICS. BITS ARE FULLY SWITCHED, WITH LESS THAN 1/2 LSB ERROR, AT LESS THAN ±100mV FROM ACTUAL THRESHOLD. THESE SWITCHING POINTS ARE GUARANTEED TO LIE BETWEEN 0.8 AND 2.0 VOLTS OVER THE OPERATING TEMPERATURE RANGE (V_{LC} = 0.0V).

FIGURE 15
POWER SUPPLY CURRENT VS. V+

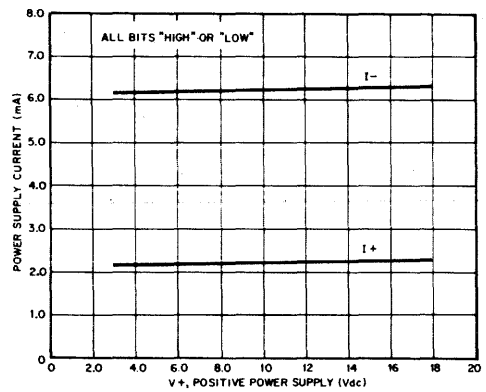


FIGURE 16
POWER SUPPLY CURRENT VS. V–

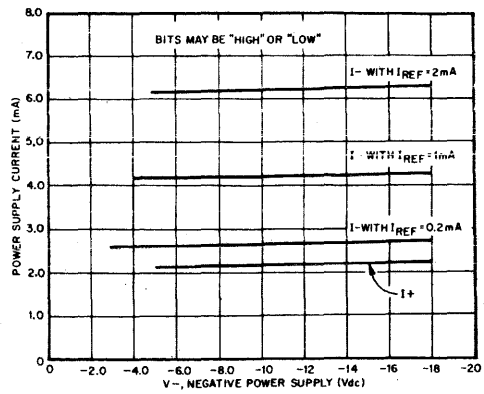
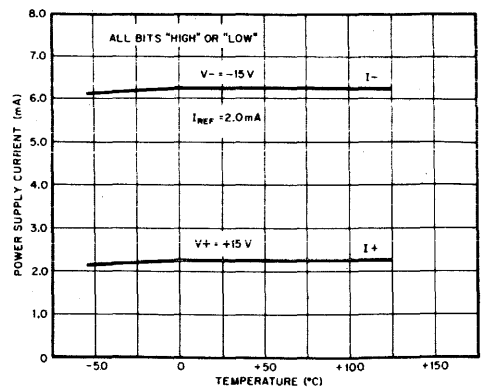
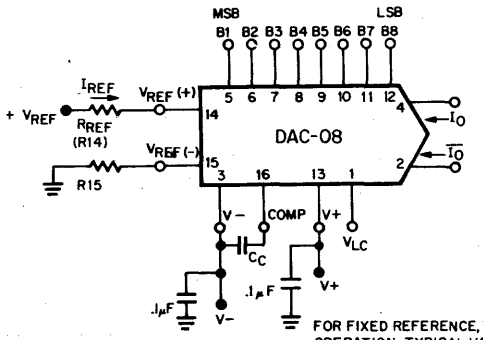


FIGURE 17
POWER SUPPLY CURRENT VS. TEMPERATURE



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FIGURE 18
BASIC POSITIVE REFERENCE OPERATION



$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \overline{I_O} = I_{FS}$ FOR ALL LOGIC STATES

FOR FIXED REFERENCE, TTL OPERATION, TYPICAL VALUES ARE:

$V_{REF} = +10.000V$

$R_{REF} = 5.000K$

$R_{15} \approx R_{REF}$

$C_C = 0.01\mu F$

$V_{LC} = 0$ V (GROUND)

FIGURE 19
RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT

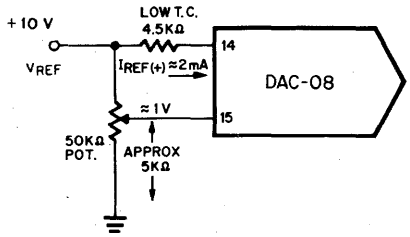
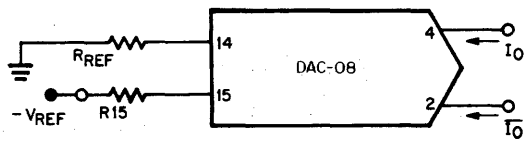


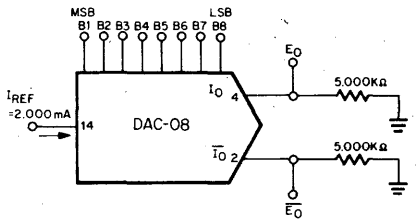
FIGURE 20
BASIC NEGATIVE REFERENCE OPERATION



$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

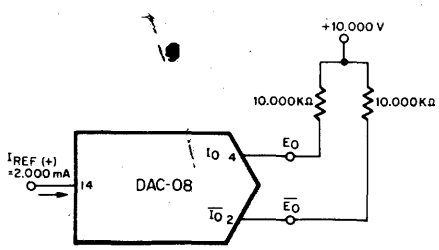
NOTE 1. R_{REF} SETS I_{FS}; R15 IS FOR BIAS CURRENT CANCELLATION.

FIGURE 21
BASIC UNIPOLAR NEGATIVE OPERATION



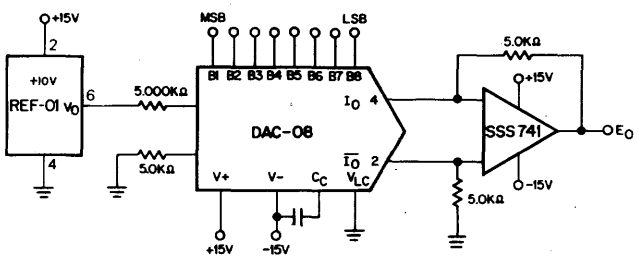
	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
FULL SCALE	1	1	1	1	1	1	1	1	1.992	.000	-9.960	.000
FULL SCALE-LSB	1	1	1	1	1	1	1	0	1.984	.008	-9.920	-.040
HALF SCALE+LSB	1	0	0	0	0	0	0	1	1.008	.984	-5.040	-4.920
HALF SCALE	1	0	0	0	0	0	0	0	1.000	.992	-5.000	-4.960
HALF SCALE -LSB	0	1	1	1	1	1	1	1	.992	1.000	-4.960	-5.000
ZERO SCALE +LSB	0	0	0	0	0	0	0	1	.008	1.984	-.040	-9.920
ZERO SCALE	0	0	0	0	0	0	0	0	.000	1.992	.000	-9.960

FIGURE 22
BASIC BIPOLAR OUTPUT OPERATION



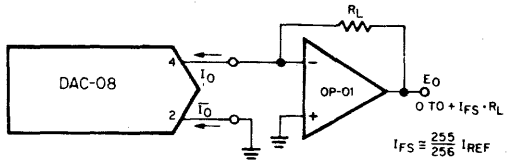
	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
POS FULL SCALE	1	1	1	1	1	1	1	1	-9.920	+10.000
POS FULL SCALE-LSB	1	1	1	1	1	1	1	0	-9.840	+ 9.920
ZERO SCALE+LSB	1	0	0	0	0	0	0	1	-0.080	+ 0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	+ 0.080
ZERO SCALE-LSB	0	1	1	1	1	1	1	1	+0.080	0.000
NEG FULL SCALE+LSB	0	0	0	0	0	0	0	1	+9.920	- 9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	+10.000	- 9.920

FIGURE 23
SYMMETRICAL OFFSET BINARY OPERATION



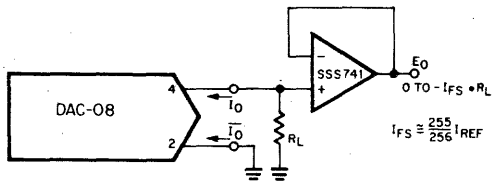
	B1	B2	B3	B4	B5	B6	B7	B8	E_O
POS FULL SCALE	1	1	1	1	1	1	1	1	+9.920
POS FULL SCALE-LSB	1	1	1	1	1	1	1	0	+9.840
(+) ZERO SCALE	1	0	0	0	0	0	0	0	+0.040
(-) ZERO SCALE	0	1	1	1	1	1	1	1	-0.040
NEG FULL SCALE+LSB	0	0	0	0	0	0	0	1	-9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	-9.920

FIGURE 24
POSITIVE LOW IMPEDANCE OUTPUT OPERATION



FOR COMPLEMENTARY OUTPUT (OPERATION AS NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

FIGURE 25
NEGATIVE LOW IMPEDANCE OUTPUT OPERATION



FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC) CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

FIGURE 26
INTERFACING WITH VARIOUS LOGIC FAMILIES

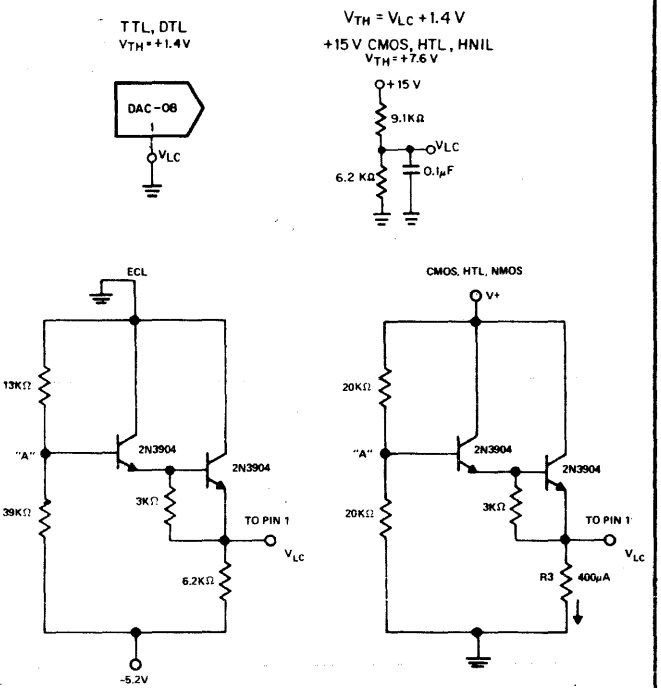


FIGURE 27
PULSED REFERENCE OPERATION

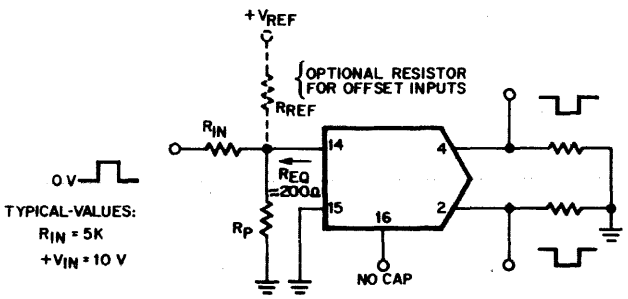
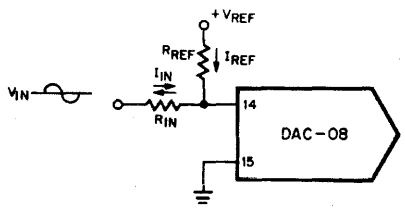
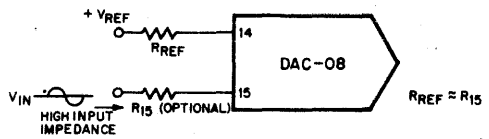


FIGURE 28
ACCOMODATING BIPOLAR REFERENCES



$I_{REF} \geq$ PEAK NEGATIVE SWING OF I_{IN}

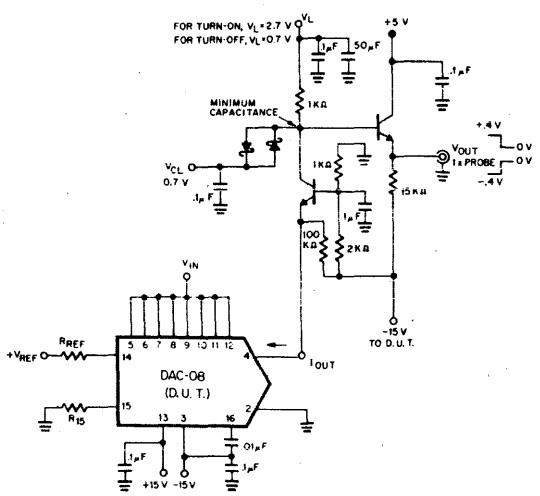
FIGURE A



+V_{REF} MUST BE ABOVE PEAK POSITIVE SWING OF V_{IN}

FIGURE B

FIGURE 29
SETTLING TIME MEASUREMENT



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APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The DAC-08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full scale output current is a linear function of the reference current and is given by:

$$I_{FS} = \frac{255}{256} \times I_{REF} \text{ where } I_{REF} = I_{14}.$$

In positive reference applications (Fig. 18), an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15 (Fig. 20); reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors; R_{15} may be eliminated with only a minor increase in error.

Bipolar references may be accomodated by offsetting V_{REF} or pin 15 as shown in Fig. 28. The negative common mode range of the reference amplifier is given by: V_{CM-} = V− plus ($I_{REF} \times 1\,K\Omega$) plus 2.5V. The positive common mode range is V+ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1 μF capacitor.

For most applications, a +10.0V reference is recommended for optimum full scale temperature coefficient performance. This will minimize the contributions of reference amplifier V_{OS} and TCV_{OS}. For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}. An improved method of full scale trimming which eliminates potentiometer T.C. effects in shown in Fig. 19.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 16 to V−. For fixed reference operation, a 0.01 μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

MULTIPLYING OPERATION

The DAC-08 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4 mA to 4 μA. Monotonic operation is maintained over a typical range of I_{REF} from 100 μA to 4.0 mA; consult factory for devices selected for monotonic operation over wider I_{REF} ranges.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the impedance presented to pin 14: for R_{14} values of 1.0, 2.5 and 5.0 KΩ, minimum values of C_c are 15, 37, and 75 pF. Larger values of R_{14} require proportionately increased values of C_c for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_c values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14} = 1 KΩ and C_c = 15 pF, the reference amplifier slews at 4 mA/μsec enabling a transition from I_{REF} = 0 to I_{REF} = 2 mA in 500 nsec.

Operation with pulse inputs to the reference amplifier may be accomodated by an alternate compensation scheme shown in Fig. 27. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full scale transition (0 to 2 mA) occurs in 120 nsec when the equivalent impedance at pin 14 is 200 Ω and C_c = 0. This yields a reference slew rate of 16 mA/μsec which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V− = −15V, the logic inputs may swing between −10V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V− plus ($I_{REF} \times 1\,K\Omega$) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). Fig. 11 shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an I_{REF} = 1 mA is recommended. For interfacing other logic families, see Fig. 26. For general setup of the logic control circuit, it should be noted that pin 1 will source 100 μA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1 KΩ divider, for example, it should be bypassed to ground by a 0.01 μF capacitor.

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ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided, where $I_O + \overline{I_O} = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V− and is independent of the positive supply. Negative compliance is given by V− plus (I_{REF} X1 KΩ) plus 2.5V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq 1$ mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at −4.5V with I_{REF} = 2 mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be useful to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows:

$P_d = (I+)\ (V+) + (I+)\ (V-) + (2\ I_{REF})\ (V-)$. A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-08 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is tight, typically ±10 ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

Full scale output drift performance will be best with +10.0V references as V_{OS} and TCV_{OS} of the reference amplifier will be very small compared to 10.0V. The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full scale drift. Settling times of the DAC-08 decrease approximately 10% at −55°C; at +125°C an increase of about 15% is typical.

SETTLING TIME

The DAC-08 is capable of extremely fast settling times, typically 85 nsec at I_{REF} = 2.0 mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35 nsec for each of the 8 bits. Settling time to within 1/2 LSB of the LSB is therefore 35 nsec, with each progressively larger bit taking successively longer. The MSB settles in 85 nsec, thus determining the overall settling time of 85 nsec. Settling to 6-bit accuracy requires about 65 to 70 nsec. The output capacitance of the DAC-08 including the package is approximately 15 pF, therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0 mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4 μA, therefore a 1 KΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of Fig. 29 uses a cascode design to permit driving a 1 KΩ load with less than 5pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1.0 mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}.

DAC-08 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1 μF capacitors at the supply pins provide full transient protection.

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PRELIMINARY

DAC-10

10 BIT HIGH SPEED MULTIPLYING D/A CONVERTER
UNIVERSAL DIGITAL LOGIC INTERFACE

GENERAL DESCRIPTION

The DAC-10 series of 10 bit monolithic multiplying Digital-to-Analog Converters provide high speed performance and full scale accuracy.

Advanced circuit design achieves 250nsec settling times with very low 'glitch' and at low power consumption. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

High voltage compliance dual complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-10 series models guarantee full 10 bit monotonicity, and nonlinearities as tight as ±.05% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 75mW power consumption attainable at lower supplies.

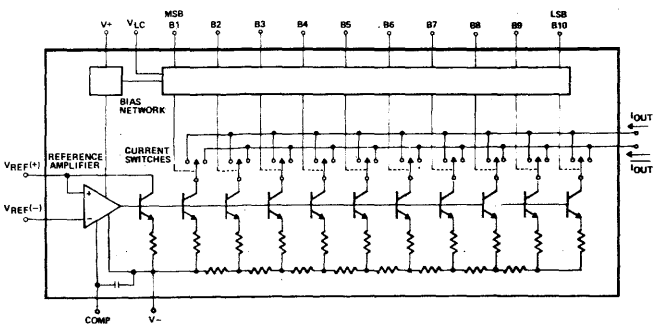
A 'Field Proven' unique trim method is used, which selectively shorts zener diodes, to provide 1/4 LSB full scale accuracy without the need for laser trimming.

FEATURES

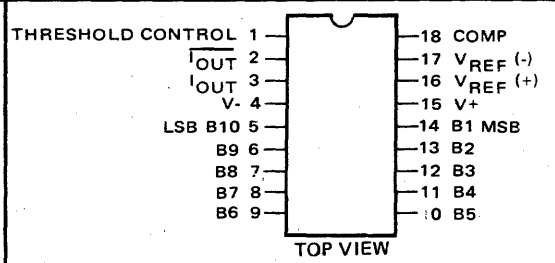
- **Fast Settling Output Current 250nsec**
- **Full Scale Current Prematched to ±1 LSB**
- **Direct Interface to TTL, CMOS, ECL, HTL, PMOS**
- **Nonlinearity to ±0.025% Full Scale**
- **High Output Impedance and True Compliance ±10V**
- **Differential Current Outputs**
- **Wide Range Multiplying Capability . . . . 1 MHz Bandwidth**
- **Low FS Current Drift . . . . . ± 6 ppm/°C**
- **Wide Power Supply Range . . . . . ±4.5V to ±18V**
- **Low Power Consumption 75mW**
- **Low Cost**

Single chip reliability coupled with low cost and outstanding flexibility make the DAC-10 devices ideal building blocks in A/D converters, Data Acquisition systems, CRT display, programmable test equipment, and other applications where low power consumption and complete input/output versatility are required.

EQUIVALENT CIRCUIT



ORDERING INFORMATION AND PIN CONNECTION



TOP VIEW
18 PIN HERMETIC DUAL-IN-LINE
(X Suffix)

MODEL	TEMP RANGE	NONLINEARITY
DAC-10AX	-55°/+125°C	±0.025%
DAC-10BX	-55°/+125°C	±0.05%
DAC-10EX	0°/70°C	±0.05%
DAC-10FX	0°/70°C	±0.1%

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:
ORDER: DAC 10-883-AX
DAC 10-883-BX

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PRELIMINARY

DAC-12/30

12 BIT HIGH SPEED MULTIPLYING D/A CONVERTER
UNIVERSAL DIGITAL LOGIC INTERFACE

GENERAL DESCRIPTION

The DAC-12/30 series of 12 bit monolithic multiplying Digital-to-Analog converters offers the DAC-12 for straight binary or offset binary applications, and the DAC-30 for BCD code requirements.

Advanced circuit design achieves 750nsec settling times with very low 'glitch' and at low power consumption. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

High voltage compliance dual complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-12 series models guarantee full 12 bit monotonicity, and nonlinearities as tight as ±.02% over the entire operating temperature range are available. Device performance is essentially unchanged over the +4.5V/-10V to ±18V power supply range, with 150mW power consumption attainable at lower supplies.

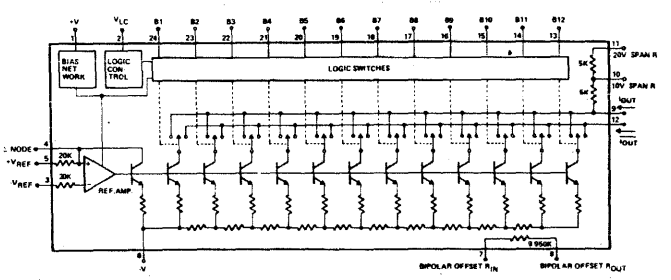
FEATURES

- True Monolithic Construction
- Fast Settling Output Current 750nsec
- Full Scale Current Prematched to ±1 LSB
- Direct Interface to TTL, CMOS, ECL, HTL, PMOS
- True 12-Bit Linearity . . . . . ±0.25LSB
- High Output Impedance and True Compliance . . . . . ±5V
- Differential Current Outputs
- High Speed Multiplying Capability
- Low FS Current Drift . . . . . ± 6 ppm/°C
- Wide Power Supply Range . . . . . +4.5V/-10V to ±18V
- Low Power Consumption 150mW
- Trimmed for Linearity after Package is Sealed

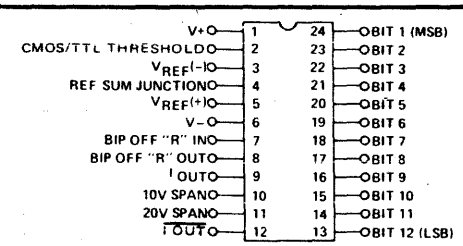
A field proven unique trim method is used, which selectively shorts zener diodes, to provide 1/4 LSB full scale accuracy on DAC-12 models without the need for laser trimming.

High speed and precision accuracy coupled with single chip reliability, low cost and outstanding flexibility make the DAC-12/30 devices ideal building blocks in A/D converters, Data Acquisition systems, CRT displays, programmable test equipment, and other applications where low power consumption and complete input/output versatility are required.

EQUIVALENT CIRCUIT



ORDERING INFORMATION AND PIN CONNECTION



TOP VIEW
24-PIN HERMETIC DUAL IN-LINE
(V-Suffix)

MODEL	TEMP RANGE	NONLINEARITY
DAC-12AV	-55°/+125°C	±0.006%
DAC-12BV	-55°/+125°C	±0.012%
DAC-12EV	0°/70°C	±0.012%
DAC-12EF	0°/70°C	±0.024%
DAC-30AV	-55°/+125°C	±0.02%
DAC-30BV	-55°/+125°C	±0.05%
DAC-30EV	0°/70°C	±0.05%
DAC-30FV	0°/70°C	±0.10%

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:

ORDER: DAC12-883-AV DAC30-883-AV
DAC12-883-BV DAC30-883-BV

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DAC-20

2 DIGIT BCD HIGH SPEED MULTIPLYING DAC
UNIVERSAL DIGITAL LOGIC INTERFACE

GENERAL DESCRIPTION

The DAC-20 series of 2 digit BCD monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design* achieves 85 nsec settling times with very low "glitch" and at low power consumption. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary current outputs with -10V to +18V voltage compliance enable resistive termination, a voltage output without an external op amp.

All DAC-20 series models guarantee full 2 digit monotonicity, and nonlinearities as tight as ±¼ LSB over the entire operating temperature range are available. Nonlinearity is unchanged over the ±4.5V to ±18V power supply range, with 37mW power consumption attainable at ±5V supplies.

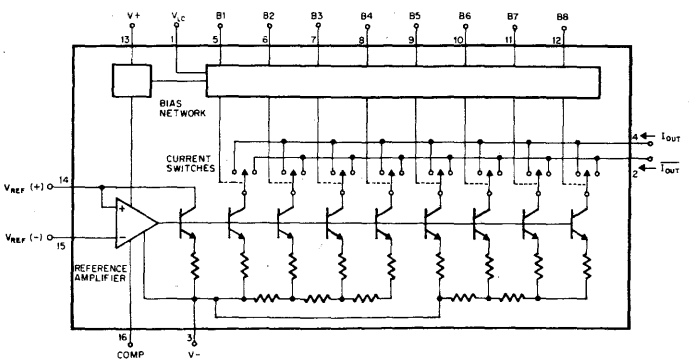
FEATURES

- Fast Settling Output Current . . . . . 85 nsec
- Full Scale Current Prematched to ±1 LSB
- Direct Interface to TTL, CMOS, ECL, HTL, PMOS
- Nonlinearity to ±¼ LSB Max Over Temp Range
- High Output Impedance and Compliance . . -10V to +18V
- Complementary Current Outputs
- Wide Range Multiplying Capability . . . . 1 MHz Bandwidth
- Low FS Current Drift . . . . . ±10ppm/°C
- Wide Power Supply Range . . . . . ±4.5V to ±18V
- Low Power Consumption . . . . . 37mW @ ±5V
- Low Cost

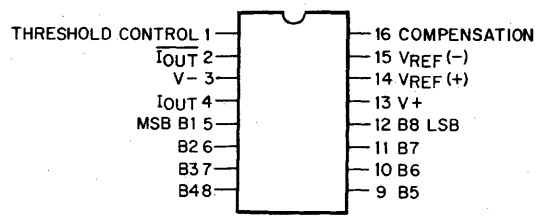
The compact size and low power consumption make the DAC-20 attractive for portable and military/aerospace applications; devices processed to MIL-STD-883A, Level B, are available.

DAC-20 applications include A/D converters, audio attenuators, analog meter drivers, programmable power supplies, high speed modems and other applications where low cost, high speed and complete input/output versatility are required.

EQUIVALENT CIRCUIT



ORDERING INFORMATION AND PIN CONNECTION



TOP VIEW
16 PIN HERMETIC DUAL-IN-LINE
(Q-Suffix)

MODEL	TEMP RANGE	NONLINEARITY
DAC-20AQ	-55°/+125°C	±¼ LSB
DAC-20Q	-55°/+125°C	±½ LSB
DAC-20EQ	0°/70°C	±¼ LSB
DAC-20CQ	0°/70°C	±½ LSB

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:
ORDER: DAC20-883-AQ
DAC20-883-Q

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Operating Temperature Range		V+ Supply to V- Supply	36V
DAC-20AQ, Q	-55°C to +125°C	Logic Inputs	V- to V- plus 36V
DAC-20EQ, CQ	0°C to +70°C	V_{LC}	V- to V+
Storage Temperature Range	-65°C to +150°C		
Power Dissipation	500mW	Reference Inputs (V_{14}, V_{15})	V- to V+
Derate above 100°C	10mW/°C	Reference Input Differential Voltage (V_{14} to V_{15})	±18V
Lead Soldering Temperature	300°C (60 sec)	Reference Input Current (I_{14})	5.0mA

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, I_{REF} = 2.0 mA, T_A = -55°C to +125°C for DAC-20A and DAC-20, T_A = 0°C to +70°C for DAC-20E and DAC-20C, unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

			DAC-20A, DAC-20E			DAC-20, DAC-20C			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Resolution		BCD 0 to 99 steps	2	2	2	2	2	2	digits
Monotonicity		BCD 99 steps	2	2	2	2	2	2	digits
Nonlinearity	NL	FS = 1001 1001	–	–	±1/4	–	–	±1/2	LSB
Settling Time	t_S	To ±½LSB (±0.5% FS) all bits switched ON or OFF. T_A = 25°C	–	85	135	–	85	150	nsec
Propagation Delay	t_{PLH}, t_{PHL}	T_A = 25°C							
Each bit			–	35	60	–	35	60	nsec
All bits switched			–	35	60	–	35	60	nsec
Full Scale Tempco	TCI_{FS}		–	±10	±50	–	±10	±80	ppm/°C
Output Voltage Compliance	V_{OC}	Full scale current change <½LSB (<0.5% FS) R_{OUT} > 20 Megohm typ. I_{REF} = 1.0mA	-10	–	+18	-10	–	+18	Volts
Full Scale Current (Digital Input 1001 1001)	I_{FS4}	V_{REF} = 10.000V R_{14}, R_{15} = 5.000kΩ T_A = 25°C	1.96	1.98	2.00	1.92	1.98	2.04	mA
Zero Scale Current	I_{ZS}		–	0.1	2.5	–	0.2	5.0	µA
Output Current Range	I_{FSR}	V- = -5.0V	0	2.0	2.2	0	2.0	2.2	mA
		V- = -7.0V to -18V	0	2.0	4.2	0	2.0	4.2	mA
Logic Input Levels									
Logic "0"	V_{IL}	V_{LC} = 0V	–	–	0.8	–	–	0.8	Volts
Logic "1"	V_{IH}		2.0	–	–	2.0	–	–	Volts
Logic Input Current		V_{LC} = 0V							
Logic "0"	I_{IL}	V_{IN} = -10V to +0.8V	–	-2.0	±10	–	-2.0	±10	µA
Logic "1"	I_{IH}	V_{IN} = 2.0V to 18V	–	0.002	±10	–	0.002	±10	µA
Logic Input Swing	V_{IS}	V- = -15V	-10	–	+18	-10	–	+18	Volts
Logic Threshold Range	V_{THR}	V_S = ±15V	-10	–	+13.5	-10	–	+13.5	Volts
Reference Bias Current	I_{15}		–	-1.0	-3.0	–	-1.0	-3.0	µA
Reference Input Slew Rate	dI/dt		4.0	8.0	–	4.0	8.0	–	mA/µsec
Power Supply Sensitivity	$PSSI_{FS+}$	V+ = 4.5V to 18V	–	±0.0003	±0.03	–	±0.0003	±0.03	%/%
	$PSSI_{FS-}$	V- = -4.5V to -18V I_{REF} = 1.0mA	–	±0.002	±0.03	–	±0.002	±0.03	%/%
Power Supply Current		V_S = ±5V, I_{REF} = 1.0 mA							
	I+		–	2.3	3.8	–	2.3	3.8	mA
	I-		–	-5.0	-6.5	–	-5.0	-6.5	mA
		V_S = ±15V, I_{REF} = 2.0 mA							
	I+		–	2.5	3.8	–	2.5	3.8	mA
	I-		–	-7.8	-9.1	–	-7.8	-9.1	mA
Power Dissipation	P_D	V_S = ±5V, I_{REF} = 1.0 mA	–	37	52	–	37	52	mW
		V_S = ±15V, I_{REF} = 2.0 mA	–	152	194	–	152	194	mW

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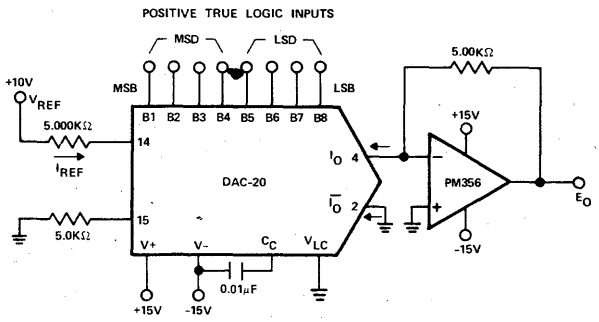
BASIC OUTPUT CONNECTIONS

With complementary current outputs, the DAC-20 may be used with either positive true or negative true (complementary) logic. Current appears at the "true" output (I_O) when a "1" is applied to a logic input. As the BCD-coded input increases, the sink current at pin 4 increases proportionately, in the fashion of a "positive logic" D/A converter. When a "0" is applied to a logic input, that current is turned off at pin 4 and on at pin 2 ($\overline{I_O}$) which is used for negative true or "negative logic" D/A converters.

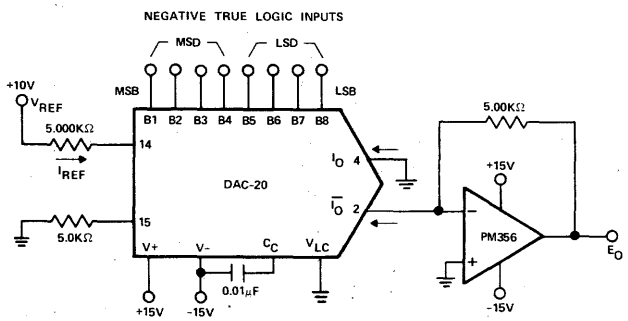
The unused output must be connected to ground or some voltage source capable of sourcing 1.65 times I_{REF}. A detailed discussion of reference input operation begins on the next page.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V- and is independent of the positive supply. Negative compliance is given by V- plus (I_{REF} X800Ω) plus 2.5V.

POSITIVE VOLTAGE OUTPUT

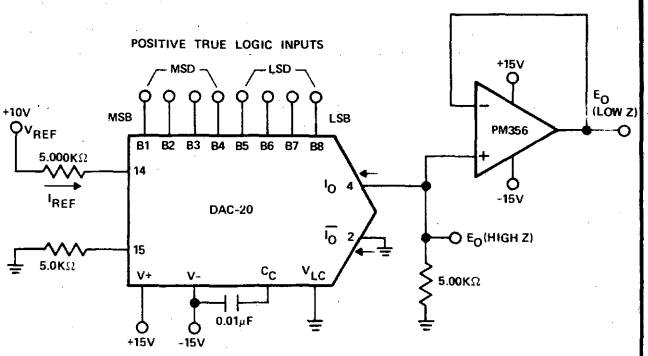


NORMALIZED INPUT	DIGITAL INPUT MSD	DIGITAL INPUT LSD	I_O	E_O
0	0000	0000	0	0
10	0001	0000	0.20mA	+1.0V
20	0010	0000	0.40mA	+2.0V
30	0011	0000	0.60mA	+3.0V
40	0100	0000	0.80mA	+4.0V
80	1000	0000	1.60mA	+8.0V
99 (FS)	1001	1001	1.98mA	+9.9V

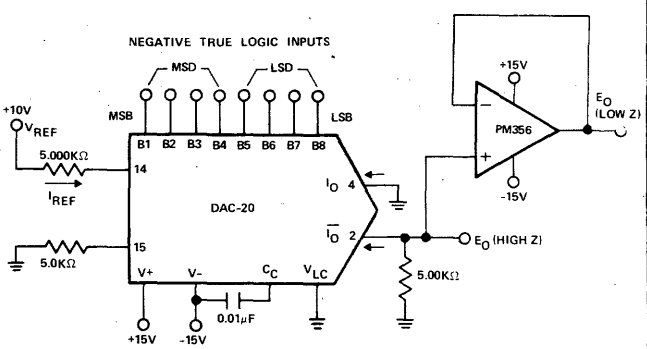


NORMALIZED INPUT	DIGITAL INPUT MSD	DIGITAL INPUT LSD	$\overline{I_o}$	E_O
0	1111	1111	0	0
10	1110	1111	0.20mA	+1.0V
20	1101	1111	0.40mA	+2.0V
30	1100	1111	0.60mA	+3.0V
40	1011	1111	0.80mA	+4.0V
80	0111	1111	1.60mA	+8.0V
99 (FS)	0110	0110	1.98mA	+9.9V

NEGATIVE VOLTAGE OUTPUT



NORMALIZED INPUT	DIGITAL INPUT MSD	DIGITAL INPUT LSD	I_O	E_O
0	0000	0000	0	0
10	0001	0000	0.20mA	-1.0V
20	0010	0000	0.40mA	-2.0V
30	0011	0000	0.60mA	-3.0V
40	0100	0000	0.80mA	-4.0V
80	1000	0000	1.60mA	-8.0V
99 (FS)	1001	1001	1.98mA	-9.9V

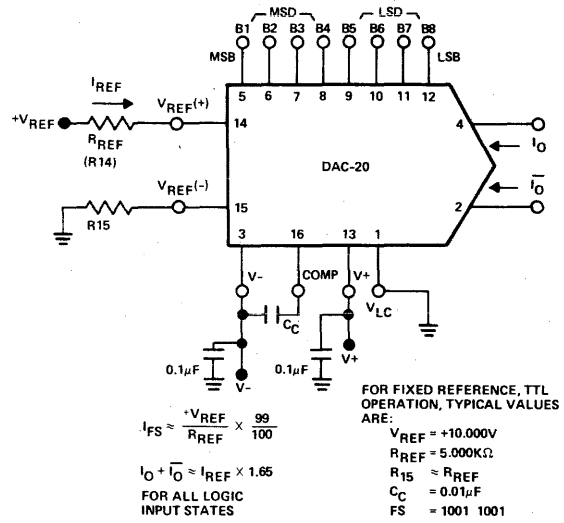


NORMALIZED INPUT	DIGITAL INPUT MSD	DIGITAL INPUT LSD	$\overline{I_O}$	E_O
0	1111	1111	0	0
10	1110	1111	0.20mA	-1.0V
20	1101	1111	0.40mA	-2.0V
30	1100	1111	0.60mA	-3.0V
40	1011	1111	0.80mA	-4.0V
80	0111	1111	1.60mA	-8.0V
99 (FS)	0110	0110	1.98mA	-9.9V

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REFERENCE OPERATION

POSITIVE



$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{99}{100}$$

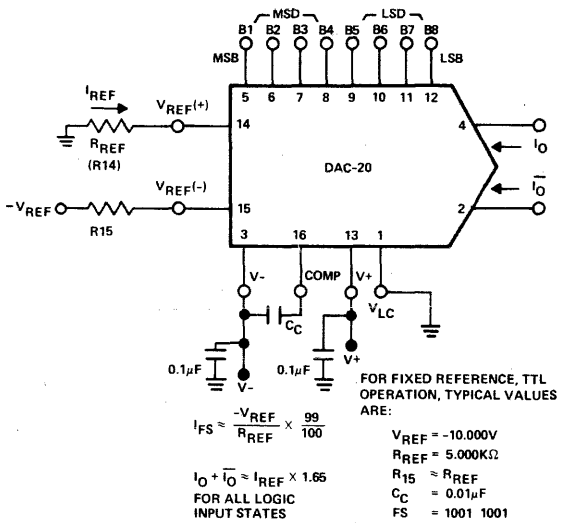
$I_O + \overline{I_O} \approx I_{REF} \times 1.65$

FOR ALL LOGIC INPUT STATES

FOR FIXED REFERENCE, TTL OPERATION, TYPICAL VALUES ARE:

$V_{REF} = +10.000V$
$R_{REF} = 5.000K\Omega$
$R_{15} \approx R_{REF}$
$C_C = 0.01\mu F$
FS = 1001 1001

NEGATIVE



$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{99}{100}$$

$I_O + \overline{I_O} \approx I_{REF} \times 1.65$

FOR ALL LOGIC INPUT STATES

FOR FIXED REFERENCE, TTL OPERATION, TYPICAL VALUES ARE:

$V_{REF} = -10.000V$
$R_{REF} = 5.000K\Omega$
$R_{15} \approx R_{REF}$
$C_C = 0.01\mu F$
FS = 1001 1001

REFERENCE AMPLIFIER SETUP

The DAC-20 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full scale output current is a linear function of the reference current and is given by:

$$I_{FS} = 99/100 \times I_{REF} \text{ where } I_{REF} = I_{14}.$$

In positive reference applications an external positive reference voltage forces current through R_{14} into the $V_{REF}(+)$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF}(-)$ at pin 15; reference current flows from ground through R_{14} into $V_{REF}(+)$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors and may be eliminated with only a minor increase in error.

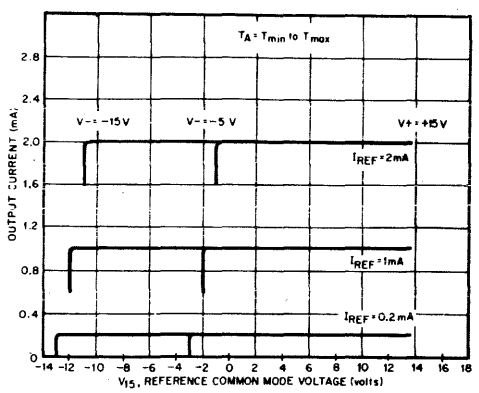
When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications, a +10.0V reference such as the PMI REF-01 is recommended for optimum full scale temperature coefficient performance. This will minimize the contributions of reference amplifier V_{OS} and TCV_{OS}. For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R14.

The reference amplifier must be compensated by using a capacitor from pin 16 to V-. For fixed reference operation, a 0.01 μF capacitor is recommended. For variable reference applications, see section entitled "Multiplying Operation."

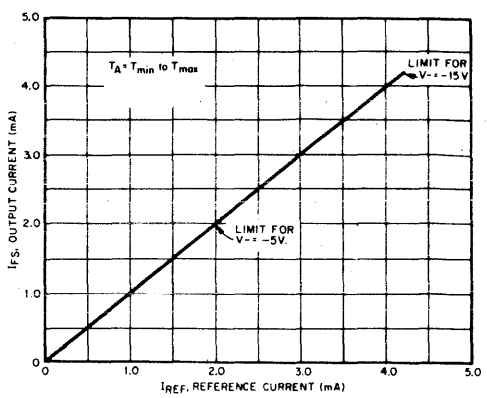
TYPICAL REFERENCE PERFORMANCE CURVES

REFERENCE AMP COMMON MODE RANGE (DIGITAL INPUT 1001 1001)



NOTE: Positive common mode range is always (V+)−1.5V; negative common mode range is V- plus(I_{REF} X 800Ω) plus 2.5V.

FULL SCALE CURRENT VS. REFERENCE CURRENT (DIGITAL INPUT 1001 1001)



NOTE: The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

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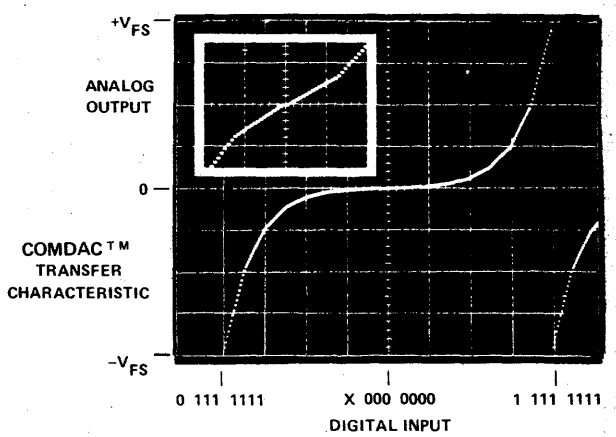
DAC-76

COMDAC™ COMPANDING D/A CONVERTER

MONOLITHIC LOGARITHMIC DAC

FEATURES

- Sign Plus 12 Bit Range With Sign Plus 7 Bit Coding
- 12 Bit Accuracy and Resolution Around Zero
- Sign Plus 72dB Dynamic Range
- True Current Outputs: –5V to +18V Compliance
- Tight Full Scale Tolerance Eliminates Calibration
- Low Full Scale Drift Over Temperature
- Conforms With Bell System μ-255 Companding Law
- Multiplying Reference Inputs
- Low Power Consumption and Low Cost
- Ideal for PCM, Audio, and 8 Bit μP Applications
- Outputs Multiplexed for Time Shared Applications

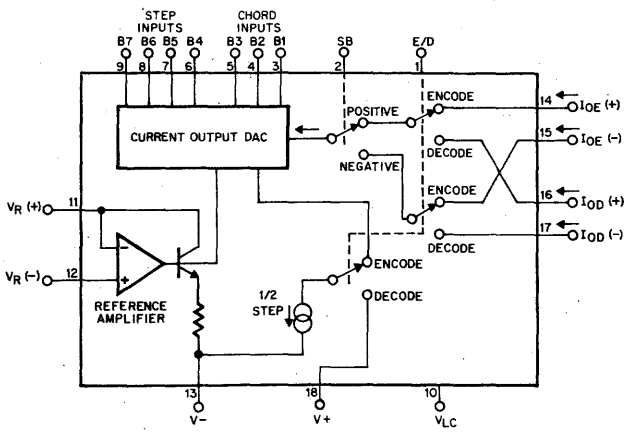


GENERAL DESCRIPTION

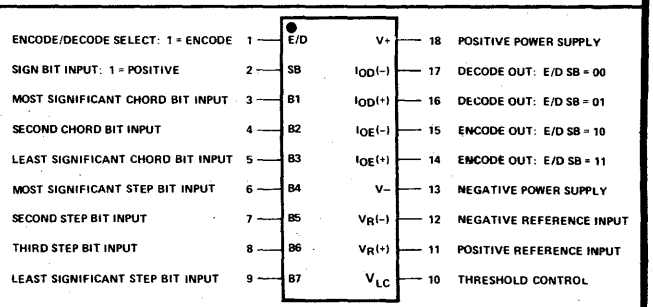
The DAC-76 monolithic COMDAC™ D/A Converter provides the dynamic range of a sign + 12-bit DAC in a sign + 7-bit format. A companding (compression/expansion) transfer function is implemented by using three bits to select one of eight binarily-related chords (or segments) and four bits to select one of sixteen linearly-related steps within each chord. Accuracy is assured by specifying chord end point values, chord nonlinearity, and monotonicity over the full operating temperature range.

The 8-bit format with a sign + 72dB dynamic range is especially useful in control systems using 8-bit microprocessors, RAM's and ROM's. Low distortion multiplying capability and conformance with the Bell System μ-255 logarithmic law for PCM transmission make the DAC-76 ideal for use in audio applications. Other applications include servo controls, stress and vibration analysis, digital recording and speech synthesis. Additional applications are listed on the last page.

EQUIVALENT CIRCUIT



ORDERING INFORMATION AND PIN CONNECTIONS



18 PIN HERMETIC DUAL-IN-LINE (X-Suffix)

MODEL	TEMP RANGE	ACCURACY
DAC-76BX	–55°/+125°C	±1/2 STEP
DAC-76X	–55°/+125°C	±1 STEP
DAC-76EX	0°/+70°C	±1/2 STEP
DAC-76CX	0°/+70°C	±1 STEP
DAC-76DX	0°/+70°C	±1 1/2 STEP

Military Temperature Range Devices
With MIL-STD-883A Class B Processing
DAC76-883-BX
DAC76-883-X

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COMPANDING PRINCIPLES

BACKGROUND

Companding or signal compression and signal expansion is widely used. In FM broadcasting companding is performed by de-emphasis and pre-emphasis. In analog systems companding is performed by log and antilog amplifiers. But in data conversion and transmission, companding has been limited to the telecommunications industry. They recognized the need to efficiently represent analog signals with the fewest possible number of digital bits. With just 8 bits, the standard format of microprocessors, RAM's, ROM's and registers, telecommunications companding systems achieve very low signal-to-quantizing distortion over a 40dB range of speech amplitudes by using the Bell System μ-255 logarithmic companding law.

BELL μ-255 LOGARITHMIC CHARACTERISTIC

The output of the DAC-76 is an approximation to the μ-255 law which can be expressed as:

$Y = 0.18 \ln (1 + \mu x)$ where:

X = Normalized input signal level of the compressor (encoder), V_{IN}/V_{FS} with values from −1 to +1.

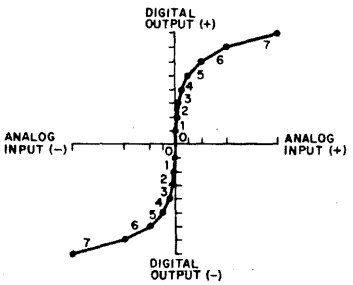
Y = Output signal level of the encoder

μ = 255

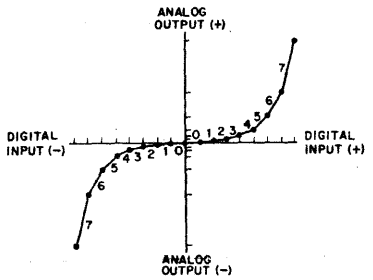
This law is implemented by the DAC-76 with an eight chord (or segment) piecewise linear approximation for each polarity with sixteen linear steps in each chord. A dynamic range of 72dB in both polarities is achieved with 8 bit coding.

TRANSFER CHARACTERISTICS

ENCODE TRANSFER CHARACTERISTIC (A/D CONVERSION)



DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)



The system transfer characteristics above result when the DAC-76 is used for signal compression (A/D conversion) and for signal expansion (D/A conversion). As one would expect, when the curves are superimposed their average is a straight line because compression and expansion must be equal and opposite.

Both transfer characteristics show outputs divided into 8 chords in both polarities with 16 equal steps in each chord. Note that each chord endpoint is approximately 6dB down from the next higher chord's endpoint and that the chord slopes are binarily-related.

The table below relates step size in each chord to other commonly-encountered measurements and to the equivalent, conventional, binary-coded DAC. Step size (except in Chord 0) is about 0.3dB and is an almost constant percentage of reading. In addition, there is a 1 1/2 step change between the maximum code in each chord and the minimum code in the next chord to smooth the chord transitions and to conform with existing telecommunication specifications.

The following three pages contain electrical specifications, the DC test circuit, tables of ideal chord endpoint currents for both encode and decode modes, and parameter definitions.

STEP SIZE SUMMARY TABLE DECODE OUTPUT (SIGN BIT EXCLUDED)

CHORD	STEP SIZE NORMALIZED TO FULL SCALE	STEP SIZE IN μA WITH 2007.75 μA F.S.	STEP SIZE AS A % OF FULL SCALE	STEP SIZE IN dB AT CHORD ENDPOINTS	STEP SIZE AS A % OF READING AT CHORD ENDPOINTS	RESOLUTION & ACCURACY OF EQUIVALENT BINARY DAC
0	2	0.5	0.025%	0.60	6.67%	SIGN + 12 BITS
1	4	1.0	0.05%	0.38	4.30%	SIGN + 11 BITS
2	8	2.0	0.1%	0.32	3.65%	SIGN + 10 BITS
3	16	4.0	0.2%	0.31	3.40%	SIGN + 9 BITS
4	32	8.0	0.4%	0.29	3.28%	SIGN + 8 BITS
5	64	16	0.8%	0.28	3.23%	SIGN + 7 BITS
6	128	32	1.6%	0.28	3.20%	SIGN + 6 BITS
7	256	64	3.2%	0.28	3.19%	SIGN + 5 BITS

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ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, I_{REF} = 528 μA, −55°C ≤ T_A ≤ +125°C, and for all 4 outputs unless otherwise specified.

Note: In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is 0.5 μA, while in the last chord near full scale (C_7) step size is 64 μA.

			DAC-76B			DAC-76			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Resolution		8 chords with 16 steps each	±128	±128	±128	±128	±128	±128	Steps
Dynamic Range		20 log ($I_{7,15}/I_{0,1}$)	72	72	72	72	72	72	dB
Monotonicity		Sign Bit + or −	128	—	—	128	—	—	Steps
Chord Endpoint Accuracy		Error relative to ideal values at I_{FS} = 2007.75μA	—	—	±1/2	—	—	±1	Step
Step Nonlinearity		Step error within chord	—	—	±1/2	—	—	±1	Step
Encode Current		Additional Output Encode/Decode = 1	3/8	1/2	5/8	1/4	1/2	3/4	Step
Settling Time	t_s	To within ±1/2 step	—	500	—	—	500	—	nsec
Full Scale Drift	ΔI_{FS}	Full Temperature Range	—	±1/20	±1/4	—	±1/10	±1/2	Step
Output Voltage Compliance	V_{OC}	Full scale current change ≤ 1/2 step	−5	—	+18	−5	—	+18	Volts
Full Scale Current Deviation from Ideal (See Tables)	$I_{FS}(D)$ $I_{FS}(E)$	V_{REF} = 10.000V T_A=25°C R11 = 18.94 kΩ R12 = 20 kΩ	— —	— —	±1/2 ±1/2	— —	— —	±1 ±1	Step Step
Full Scale Symmetry Error	$I_O(+)-I_O(-)$	Decode or Encode Pair	—	±1/40	±1/8	—	±1/20	±1/4	Step
Zero Scale Current	I_{ZS}	Measured at Selected Output with 000 0000 Input	—	1/40	1/4	—	1/20	1/2	Step
Disable Current	I_{DIS}	Leakage of output disabled by E/Dand SB	—	5.0	50	—	5.0	50	nA
Output Current Range	I_{FSR}		0	2.0	4.2	0	2.0	4.2	mA
Logic Input Levels Logic "0" Logic "1"	 V_{IL} V_{IH}	V_{LC} = OV	 — 2.0	 — —	 0.8 —	 — 2.0	 — —	 0.8 —	 Volts Volts
Logic Input Current	I_{IN}	V_{IN} = −5V to +18V	—	—	40	—	—	40	μA
Logic Input Swing	V_{IS}	V− = −15V	−5	—	+18	−5	—	+18	Volts
Reference Bias Current	I_{12}		—	−1.0	−4.0	—	−1.0	−4.0	μA
Reference Input Slew Rate	dI/dt		—	0.25	—	—	0.25	—	mA/μsec
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS+}$ $PSSI_{FS-}$	V+=4.5 to 18V,V−=−15V V−=−10.8Vto−18V,V+=15V	— —	±1/20 ±1/10	±1/2 ±1/2	— —	±1/20 ±1/10	±1/2 ±1/2	Step Step
Power Supply Current	I+ I−	V_S=+5V,−15V, I_{FS}=2.0 mA	— —	2.7 −6.7	4.0 −8.8	— —	2.7 −6.7	4.0 −8.8	mA mA
Power Supply Current	I+ I−	V_S = ±15V, I_{FS} = 2.0 mA	— —	2.7 −6.7	4.0 −8.8	— —	2.7 −6.7	4.0 −8.8	mA mA
Power Dissipation	P_D	V_S=+5V,−15V,I_{FS}=2.0mA V_S=±15V,I_{FS}=2.0mA	— —	114 141	152 192	— —	114 141	152 192	mW mW

ELECTRICAL CHARACTERISTICS

These specifications apply for $V_S = \pm 15V$, $I_{REF} = 528\ \mu A$, $0°C \leq T_A \leq +70°C$, and for all 4 outputs unless otherwise specified.

Note: In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is 0.5 μA, while in the last chord near full scale (C_7) step size is 64 μA.

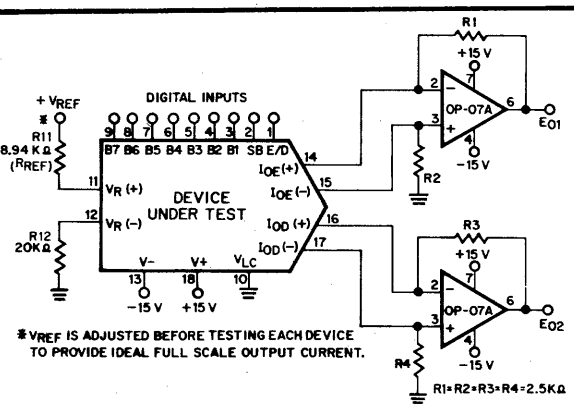
			DAC-76E			DAC-76C			DAC-76D			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Resolution		8 chords with 16 steps each	±128	±128	±128	±128	±128	±128	±128	±128	±128	Steps
Dynamic Range		20 log ($I_{7,15}/I_{0,1}$)	72	72	72	72	72	72	72	72	72	dB
Monotonicity		Sign Bit + or –	128	–	–	128	–	–	128	–	–	Steps
Chord Endpoint Accuracy		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	–	–	±1/2	–	–	±1	–	–	±1½	Step
Step Nonlinearity		Step error within chord	–	–	±1/2	–	–	±1	–	–	±1½	Step
Encode Current		Additional Output Encode/Decode = 1	3/8	1/2	5/8	1/4	1/2	3/4	1/4	1/2	3/4	Step
Settling Time	t_s	To within ±1/2 step	–	500	–	–	500	–	–	500	–	nsec
Full Scale Drift	ΔI_{FS}	Full Temperature Range	–	±1/20	±1/4	–	±1/10	±1/2	–	±1/10	±1/2	Step
Output Voltage Compliance	V_{OC}	Full scale current change ≤ 1/2 step	–5	–	+18	–5	–	+18	–5	–	+18	Volts
Full Scale Current Deviation from Ideal (See Tables)	$I_{FS}(D)$ $I_{FS}(E)$	$V_{REF} = 10.000V$ $T_A=25°C$ R11 = 18.94 kΩ R12 = 20 kΩ	– –	– –	±1/2 ±1/2	– –	– –	±1 ±1	– –	– –	±1 ±1	Step Step
Full Scale Symmetry Error	$I_O(+)-I_O(-)$	Decode or Encode Pair	–	±1/40	±1/8	–	±1/20	±1/4	–	±1/20	±1/2	Step
Zero Scale Current	I_{ZS}	Measured at Selected Output with 000 0000 Input	–	1/40	1/4	–	1/20	1/2	–	1/20	1/2	Step
Disable Current	I_{DIS}	Leakage of output disabled by E/D and SB	–	5.0	50	–	5.0	50	–	5.0	100	nA
Output Current Range	I_{FSR}		0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	mA
Logic Input Levels Logic "0" Logic "1"	 V_{IL} V_{IH}	$V_{LC} = 0V$	 – 2.0	 – –	 0.8 –	 – 2.0	 – –	 0.8 –	 – 2.0	 – –	 0.8 –	 Volts Volts
Logic Input Current	I_{IN}	V_{IN} = –5V to +18V	–	–	40	–	–	40	–	–	40	µA
Logic Input Swing	V_{IS}	V– = –15V	–5	–	+18	–5	–	+18	–5	–	+18	Volts
Reference Bias Current	I_{12}		–	–1.0	–4.0	–	–1.0	–4.0	–	–1.0	–6.0	µA
Reference Input Slew Rate	dI/dt		–	0.25	–	–	0.25	–	–	0.25	–	mA/µsec
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS+}$ $PSSI_{FS-}$	V+=4.5 to 18V, V–=–15V V–=–10.8V to –18V, V+=15V	– –	±1/20 ±1/10	±1/2 ±1/2	– –	±1/20 ±1/10	±1/2 ±1/2	– –	±1/20 ±1/10	±3/4 ±3/4	Step Step
Power Supply Current	I+ I–	V_S = +5V, –15V, I_{FS}=2.0mA	– –	2.7 –6.7	4.0 –8.8	– –	2.7 –6.7	4.0 –8.8	– –	2.7 –6.7	4.5 –9.3	mA mA
Power Supply Current	I+ I–	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	– –	2.7 –6.7	4.0 –8.8	– –	2.7 –6.7	4.0 –8.8	– –	2.7 –6.7	4.5 –9.3	mA mA
Power Dissipation	P_D	V_S=+5V, –15V, I_{FS}=2.0mA $V_S = \pm 15V$, I_{FS}=2.0mA	– –	114 141	152 192	– –	114 141	152 192	– –	114 141	167 207	mW mW

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ABSOLUTE MAXIMUM RATINGS

V+ Supply to V– Supply	36V	Operating Temperature	
V_{LC} Swing	V– plus 8V to V+	DAC-76B, DAC-76	–55°C to +125°C
Analog Current Outputs	V– plus 8V to V– plus 36V	DAC-76E, DAC-76C, DAC-76D	0°C to +70°C
Reference Inputs	V– to V+	Storage Temperature	–65°C to +150°C
Reference Input Differential Voltage	±18V	Power Dissipation	500mW
Reference Input Current	1.25 mA	Derate above 100°C	10mW/°C
Logic Inputs	V– plus 8V to V– plus 36V	Lead Soldering Temperature	300°C (60 sec)

OUTPUT CURRENT DC TEST CIRCUIT



LINE SELECTION TABLE

TEST GROUP	ENCODE/ DECODE	SIGN BIT	OUTPUT MEASUREMENT	
1	1	1	I_{OE} (+)	(E_{01}/R1)
2	1	0	I_{OE} (–)	(E_{01}/R2)
3	0	1	I_{OD} (+)	(E_{02}/R3)
4	0	0	I_{OD} (–)	(E_{02}/R4)

NOTE:—Accuracy is specified in the test circuit using the tables below to be within the specified proportion of a step at the maximum value in each chord. Monotonic operation is guaranteed for all input codes.

CONDENSED CURRENT OUTPUT TABLES

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		0.50	1	2	4	8	16	32	64

IDEAL ENCODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0.25	8.75	25.75	59.75	127.75	263.75	535.75	1079.75
15	1111	7.75	23.75	55.75	119.75	247.75	503.75	1015.75	2039.75
STEP SIZE		0.50	1	2	4	8	16	32	64

SPECIFICATION PARAMETER DEFINITIONS

STEP NONLINEARITY: Step size deviation from ideal within a chord.

ENCODE CURRENT: The difference between I_{OE}(+) and I_{OD}(+) or the difference between I_{OE}(–) and I_{OD}(–) at any code.

FULL SCALE DRIFT: The change in output current over the full operating temperature with V_{REF} = 10.000V, R11 = 18.94KΩ, and R12 = 20KΩ.

FULL SCALE SYMMETRY ERROR: The difference between I_{OD}(–) and I_{OD}(+) or the difference between I_{OE}(–) and I_{OE}(+) at full scale output.

OUTPUT VOLTAGE COMPLIANCE: The maximum output voltage swing at any current level which causes <1/2 step change in output current.

CHORDS: Groups of linearly-related steps in the transfer function. Also known as segments.

CHORD ENDPOINTS: The maximum code in each chord. Used to specify accuracy.

STEPS: Increments in each chord which divide it into 16 equal levels.

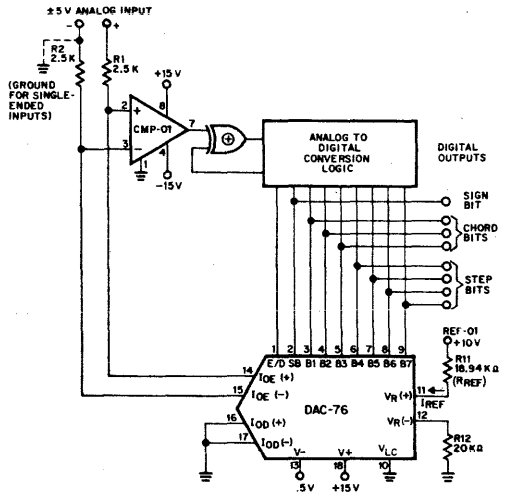
OUTPUT LEVEL NOTATION: Each output current level may be designated by the code $I_{C,S}$ where C = chord number and S = step number. For example, $I_{0,0}$ = zero scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of first chord (C_0); $I_{7,15}$ = full scale current.

DYNAMIC RANGE: Ratio of the largest output ($I_{7,15}$) to the smallest output excluding zero ($I_{0,1}$) expressed in dB. This can be measured peak or peak-to-peak with the same result.

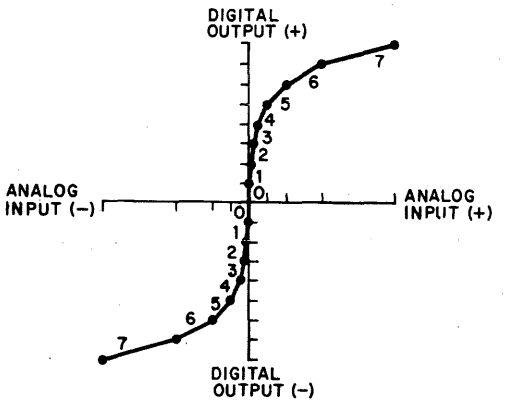
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BASIC ENCODE OPERATION (COMPRESSING A/D CONVERSION)

BASIC ENCODE CONNECTIONS



ENCODE TRANSFER CHARACTERISTIC (A/D CONVERSION)



ENCODE DECISION LEVELS

Compressing A/D conversion with the DAC-76 requires a comparator, an exclusive-or gate, and a successive approximation register—the usual elements in any sign-plus-magnitude A/D converter. However, a compressing ADC has one significant difference from regular A/D converters.

In a conventional (linear) converter, the step size is a constant percentage of full scale, but in a compressing A/D converter, the step size increases as the output changes from zero scale to full scale. The standard 1/2 step bias used in conventional ADC's to keep quantizing error below ±1/2 step cannot be easily furnished by the user of a compressing ADC. For this reason, the DAC has a 1/2 step greater output in the encode mode than it has in the decode mode. This may be seen clearly by comparing the normalized encode and decode output tables at any code point.

ENCODING SEQUENCE

An encoding sequence begins with the Sign Bit comparison and decision. During this time the comparator is a polarity detector only. The Encode/Decode (E/D) input is held at a logic "0". Therefore, no current flows into the encode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input is changed to a logic "1" allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$ depending upon the Sign Bit Answer.

For positive inputs, current flows into $I_{OE}(+)$ through R1, and the comparator's output will be entered as the answer for each successive decision. For negative inputs, current flows into $I_{OE}(-)$ through R2 developing a negative voltage which is compared with the analog input. An exclusive-or gate inverts the comparator's output during negative trials to maintain the proper logic coding, all ones for full scale and all zeros for zero scale. (A more complete schematic is shown in the applications section.)

The bits are converted with a successive removal technique, starting with a decision at the code 011 1111 and turning off bits sequentially until all decisions have been made. Successive removal is necessary because the 1/2 step encode decision level current is drawn from the sum node, rather than sourced into it.

NORMALIZED ENCODE LEVEL (SIGN BIT EXCLUDED)

$I_{C,S} = 2[2^C (S+17) - 16.5]$

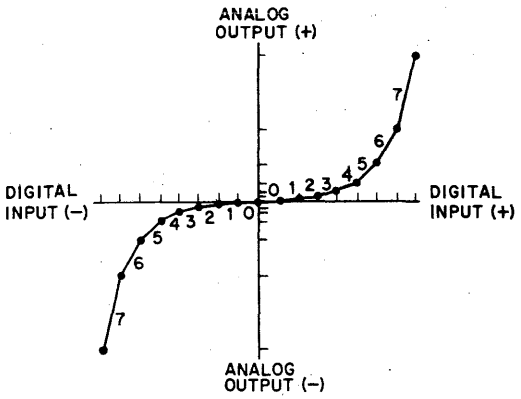
C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
STEP SIZE		2	4	8	16	32	64	128	256

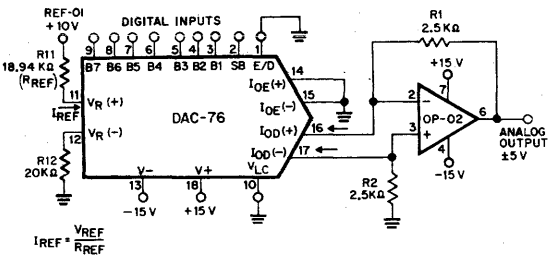
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BASIC DECODE OPERATION (EXPANDING D/A CONVERSION)

DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)



BASIC DECODE CONNECTIONS



$I_{REF} = \frac{V_{REF}}{R_{REF}}$

IDEAL VALUES:
$I_{REF} = 528\mu A$
$I_{FS} = 2007.75\mu A$

	E/D	SB	B1	B2	B3	B4	B5	B6	B7	E_O
POS FULL SCALE	0	1	1	1	1	1	1	1	1	5.019V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0V
(−) ZERO SCALE	0	0	0	0	0	0	0	0	0	0V
(−) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	−0.0012
NEG FULL SCALE	0	0	1	1	1	1	1	1	1	−5.019V

DECODE OPERATION

D/A conversion with the DAC-76 may be illustrated by using an operational amplifier connected to the decode outputs as a balanced load. The decode mode of operation is selected by applying a logic "0" to the Encode/Decode input. This enables the I_{OD} outputs, disables the I_{OE} outputs, and allows $I_{OD}(+)$ or $I_{OD}(-)$ to be selected by the Sign Bit input. When the Sign Bit input is high, a logic "1", all of the output current flows into $I_{OD}(+)$ forcing a positive voltage at the operational amplifier's output. When the Sign Bit input is low, a logic "0", all of the output current flows into $I_{OD}(-)$ through R2 forcing a negative voltage output. Since the Sign Bit only steers current into $I_{OD}(+)$ or $I_{OD}(-)$, the output will always be symmetrical, limited only by the matching of R1 and R2.

NORMALIZED TABLES

The encode and decode tables may be used to calculate ideal output current at any code point. For example, in decode mode at $I_{3,7}$ (011 0111) find 343. 343/8031 times I_{FS} of 2007.75μA equals 85.75μA. Alternatively, use the condensed current tables and add up the number of steps.

BASIC REFERENCE CONSIDERATIONS

Full scale output current is ideally 2007.75μA when the reference current is 528μA in the decode mode. In the encode mode it is 2039.75μA because the additional 1/2 step adds 32μA to the output. A percentage change in I_{REF} caused by changes in V_{REF} or R_{REF} will produce the same percentage change in output current.

The large step size at full scale allows the use of inexpensive references in many applications. In some situations V_{REF} may even be the positive power supply. For example, with V+ = 15V, R_{REF} = 15V/528μA or 28.4KΩ. When using a power supply as a reference, R11 should be two resistors, R11A and R11B, and the junction should be bypassed to ground to provide decoupling.

NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED)

$I_{C,S} = 2[2^C (S+16.5) - 16.5]$

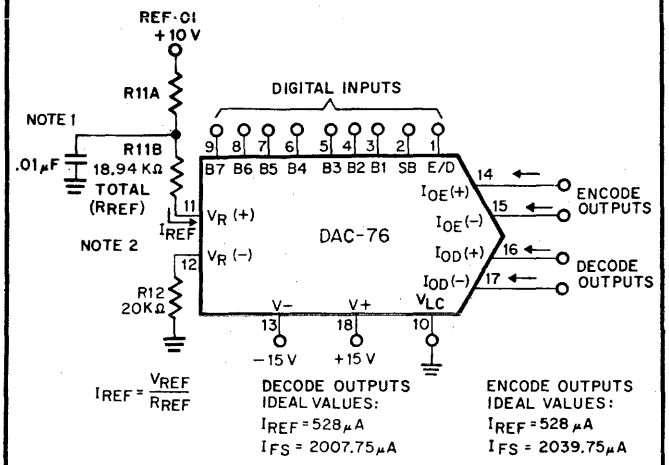
C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
STEP SIZE		2	4	8	16	32	64	128	256

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REFERENCE AMPLIFIER OPERATION

POSITIVE REFERENCE OPERATION



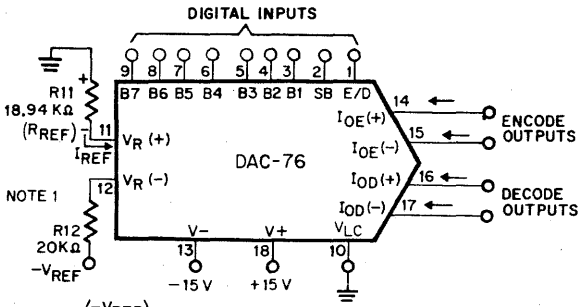
$I_{REF} = \frac{V_{REF}}{R_{REF}}$

DECODE OUTPUTS IDEAL VALUES:
$I_{REF} = 528\mu A$
$I_{FS} = 2007.75\mu A$

ENCODE OUTPUTS IDEAL VALUES:
$I_{REF} = 528\mu A$
$I_{FS} = 2039.75\mu A$

NOTE 1: RECOMMENDED WHEN V_{REF} IS V+ OR THE LOGIC POWER SUPPLY.
NOTE 2: PINS 11 AND 12 ARE EQUAL IN VOLTAGE. V_{REF} IS IMPRESSED ACROSS R11 (R_{REF})

NEGATIVE REFERENCE OPERATION



$I_{REF} = -\left(\frac{-V_{REF}}{R_{REF}}\right)$

DECODE OUTPUTS IDEAL VALUES:
$I_{REF} = 528\mu A$
$I_{FS} = 2007.75\mu A$

ENCODE OUTPUTS IDEAL VALUES:
$I_{REF} = 528\mu A$
$I_{FS} = 2039.75\mu A$

NOTE 1: PINS 11 AND 12 ARE EQUAL IN VOLTAGE. V_{REF} IS IMPRESSED ACROSS R11 (R_{REF}).

REFERENCE AMPLIFIER SETUP

The DAC-76 is a multiplying D/A converter in which the output current is the product of the normalized digital input and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full scale output current is a linear function of the reference current and is given for all four outputs in the figures above.

In positive reference applications an external positive reference voltage forces current through R11 into the $V_R(+)$ terminal (pin 11) of the reference amplifier. Alternatively, a negative reference may be applied to $V_R(-)$ at pin 12; reference current flows from ground through R11 into $V_R(+)$, as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 12. The voltage at pin 11 is equal to and tracks the voltage at pin 12 due to the high gain of the internal reference amplifier. R12 (nominally equal to R11) is used to cancel bias current errors and may be eliminated with only a minor increase in error.

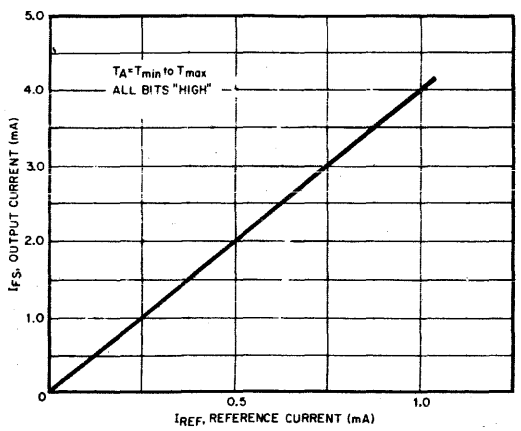
REFERENCE RECOMMENDATIONS

For most applications a +10.0V reference, such as the PMI REF-01, is recommended for optimum full scale temperature coefficient performance. (This also minimizes the contributions of reference amplifier V_{OS} and TCV_{OS}.) For most applications the tight relationship between I_{REF} and I_{FS} eliminates the need for trimming I_{REF}; but if desired, full scale trimming may be accomplished by selecting R11 or by using a potentiometer for R11.

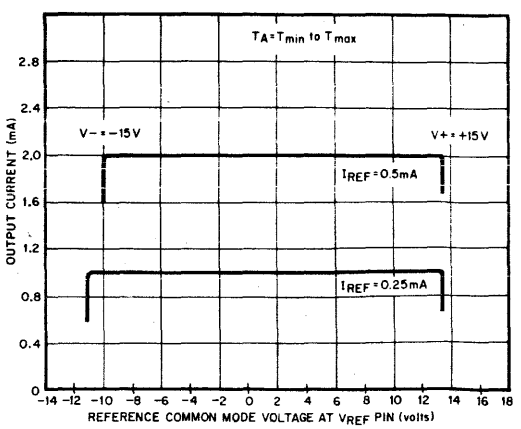
Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. While the recommended operating range of DC reference currents is 0.1mA to 1.0mA, monotonic operation is maintained over an even wider range allowing the DAC-76 to be used in many multiplying applications. For variable reference applications, see section entitled "Multiplying Operation."

TYPICAL PERFORMANCE CURVES

OUTPUT FULL SCALE CURRENT VS. REFERENCE INPUT CURRENT



REFERENCE AMPLIFIER INPUT COMMON MODE RANGE

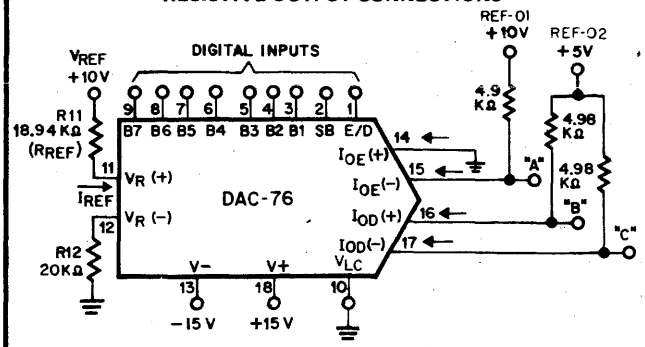


NOTE: POSITIVE COMMON MODE RANGE IS ALWAYS (V+)−1.5 V

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TRUE CURRENT OUTPUT OPERATION

RESISTIVE OUTPUT CONNECTIONS



	OUTPUT VOLTAGE (V)			
INPUT CODE	"A"	"B"	"C"	DIFF
11 111 1111	0			
11 110 1111	+5.02	N/A	N/A	N/A
11 000 0000	+10.00			
01 111 1111		−5.00	+5.00	−10
01 110 1111		+0.02	+5.00	−4.98
01 000 0000	N/A	+5.00	+5.00	0
00 000 0000		+5.00	+5.00	0
00 110 1111		+5.00	+0.02	+4.98
00 111 1111		+5.00	−5.00	+10

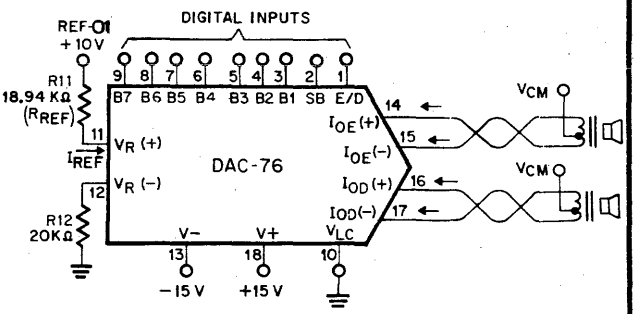
NEGATIVE OUTPUT VOLTAGE COMPLIANCE $V_{OC}(-)$

V− \ I_{FS}	1.0mA	2.0mA	4.0mA
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

MINIMUM NEGATIVE COMPLIANCE

$V_{OC}(-)$ MIN = $(V-)+(2I_{REF} \cdot 1.6K\Omega) + 8.4V$

BALANCED LOAD CONNECTIONS



TYPICAL BALANCED LOADS

- TRANSFORMER
- TRANSDUCER
- EARPHONE
- SAMPLE-AND-HOLD
- CURRENT INPUT FILTER
- TRANSMISSION LINE
- DAC REFERENCE INPUT
- BRIDGE
- OP AMP
- CRT
- SERVO

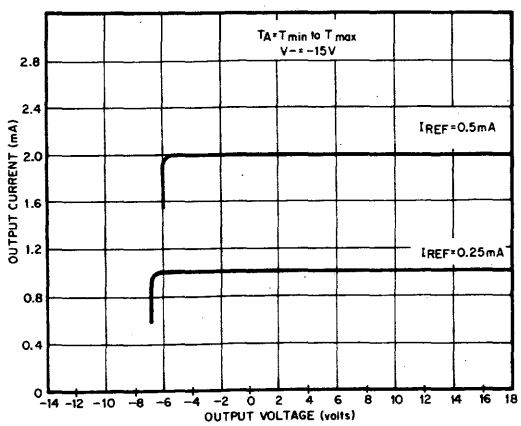
NOTE: THE SUM OF THE COMMON MODE VOLTAGE AND THE DIFFERENTIAL VOLTAGE ACROSS THE LOAD SHOULD BE WITHIN THE −5V TO +18V OUTPUT VOLTAGE COMPLIANCE SPECIFICATION.

The DAC-76 has true current outputs with wide voltage compliance enabling fast drive of a variety of single-ended and balanced loads. Positive voltage compliance is +18V, and negative voltage compliance is −5.0V with I_{REF} = 528μA and V− = −15V. Negative voltage compliance for other values of I_{REF} and V− may be calculated using the table above. Typical connections, both single-ended and differential, are shown in the figure above with output voltage tables. Note the differential sign-plus-magnitude relationship between "B" and "C". The differential output voltage is independent of the +5.00 nominal voltage source as long as the $V_{OC}(-)$ minimum values are observed.

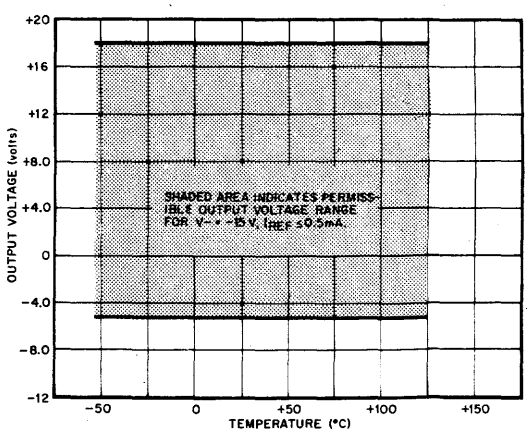
High common mode output range is possible due to the wide output voltage compliance and allows use with transformers or other balanced loads. The terminating impedances may be located a distance away from the DAC-76 allowing transmission of analog quantities as currents rather than voltages and elimination of ground loop errors. Capacitive termination is also possible, performing an "integrate-and-hold" process which is a function of V_{REF}, R_{REF}, the digital input code, and the selection time for a given current output. Resetting of the integrating capacitor may be accomplished with a CMOS switch in parallel with the capacitor. Thus, many applications traditionally requiring op amps may be performed with a high voltage compliance, current output DAC.

TYPICAL PERFORMANCE CURVES

OUTPUT CURRENT VS. OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)

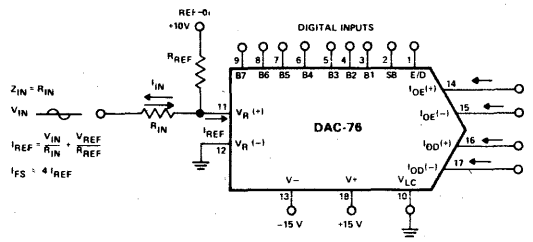


OUTPUT VOLTAGE COMPLIANCE VS. TEMPERATURE

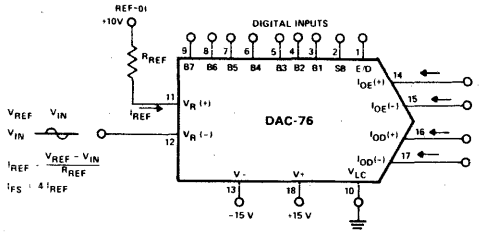


MULTIPLYING OPERATION

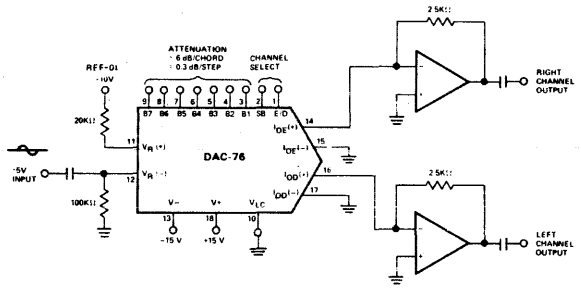
LOW INPUT IMPEDANCE CONNECTION



HIGH INPUT IMPEDANCE CONNECTION

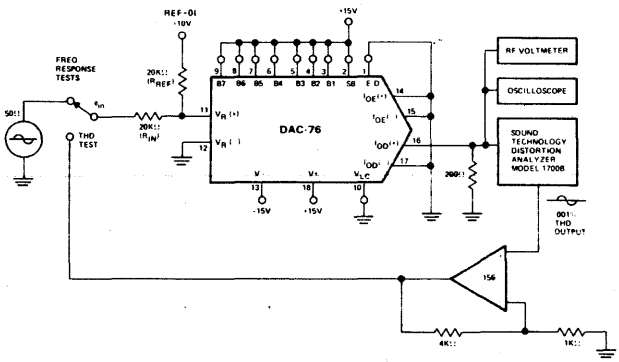


LOGARITHMIC DIGITAL GAIN CONTROL



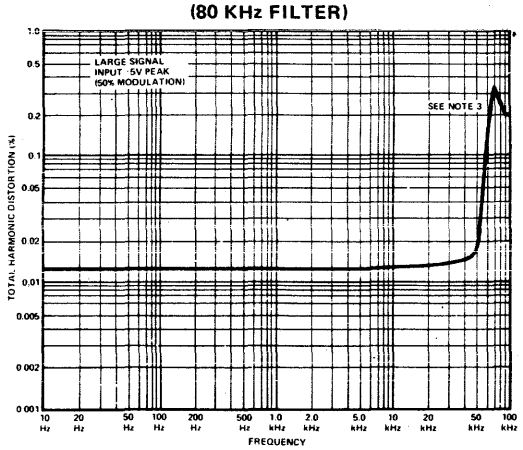
NOTE 1: LOW DISTORTION OUTPUTS ARE PROVIDED OVER A 72dB RANGE.
NOTE 2: UP TO 4 CHANNELS OF OUTPUT MAY BE SELECTED BY E/D AND SB LOGIC INPUTS.

REFERENCE AMPLIFIER DYNAMIC TEST CIRCUIT



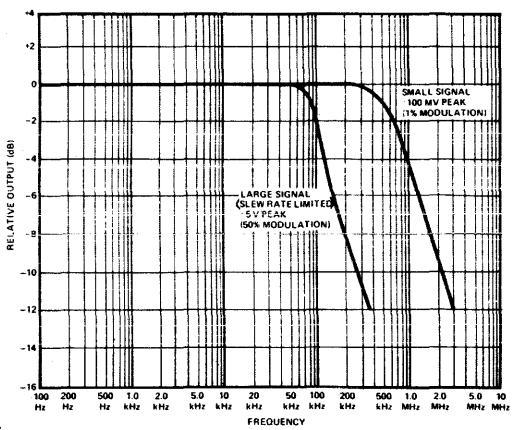
TYPICAL PERFORMANCE CURVES

REFERENCE AMPLIFIER TOTAL HARMONIC DISTORTION VS. FREQUENCY (80 KHz FILTER)



NOTE 1: THD IS NEARLY INDEPENDENT OF LOGIC INPUT CODE
NOTE 2: SIMILAR RESULTS ARE OBTAINED FOR A HIGH INPUT IMPEDANCE CONNECTION USING PIN 12 AS AN INPUT
NOTE 3: INCREASED DISTORTION ABOVE 50kHz IS DUE TO SLEW RATE LIMITING WHICH DETERMINES LARGE SIGNAL BANDWIDTH. FOR AN INPUT OF 2.5V PEAK (25% MODULATION), BANDWIDTH IS 100kHz.

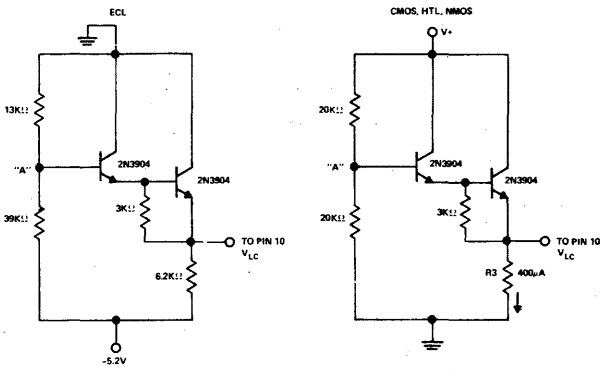
REFERENCE AMPLIFIER INPUT FREQUENCY RESPONSE



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LOGIC INPUT AND POWER SUPPLY CONSIDERATIONS

INTERFACING CIRCUIT FOR ECL, CMOS, HTL, & NMOS LOGIC INPUTS



NOTE 1: SET THE VOLTAGE "A" TO BE AT THE DESIRED LOGIC INPUT SWITCHING THRESHOLD.
NOTE 2: ALLOWABLE RANGE OF LOGIC THRESHOLD IS TYPICALLY -5V TO +13.5V WHEN OPERATING THE DAC-76 ON ±15V SUPPLIES.

LOGIC INPUTS

The DAC-76 may be interfaced with other-than-TTL logic by placing V_{LC} (pin 10) at a potential which is 1.4V below the desired logic input switching threshold. However, this voltage source must be capable of sourcing and sinking a changing current at pin 10.

The negative voltage at the logic inputs must be limited to +10V with respect to V– (pin 13).

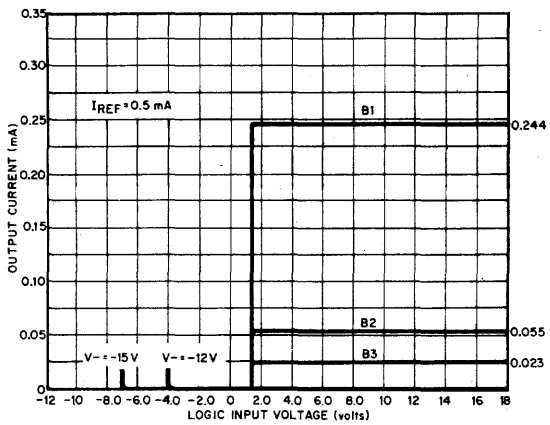
POWER SUPPLIES

As shown in the curves below, power supply current drain is relatively independent of voltage and temperature and completely independent of the logic input states.

When operating with V– between –15V and –11V, output negative voltage compliance, $V_{OC}(-)$, reference input amplifier common mode voltage range, and logic input negative voltage range are reduced by an amount equivalent to the difference between –15V and the V– supply in use. Operation with V+ between +5V and +15V affects V_{LC} and the reference amplifier common mode positive voltage range in the same manner.

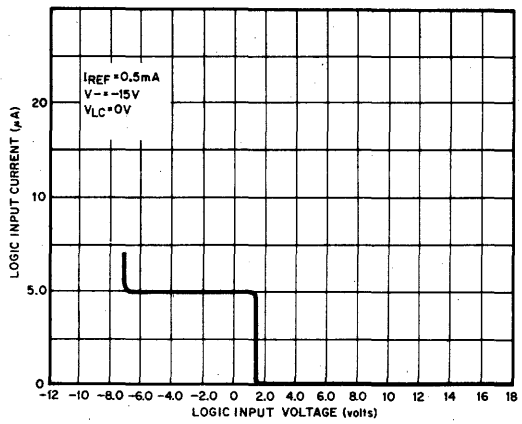
TYPICAL PERFORMANCE CURVES

BIT TRANSFER CHARACTERISTICS



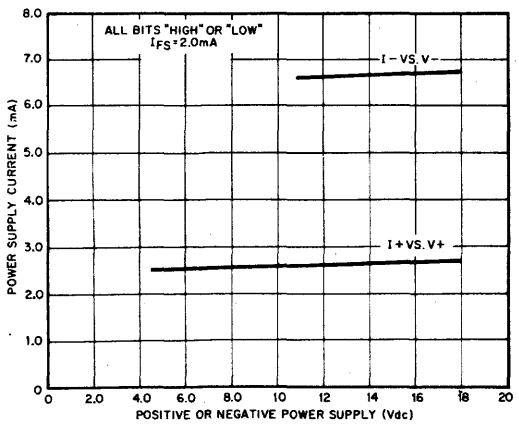
NOTE: ALL BITS ARE FULLY SWITCHED WITH LESS THAN 1/2 STEP ERROR AT SWITCHING POINTS WHICH ARE GUARANTEED TO LIE BETWEEN 0.8V AND 2.0V OVER THE OPERATING TEMPERATURE RANGE.

LOGIC INPUT CURRENT VS. INPUT VOLTAGE AND LOGIC INPUT RANGE

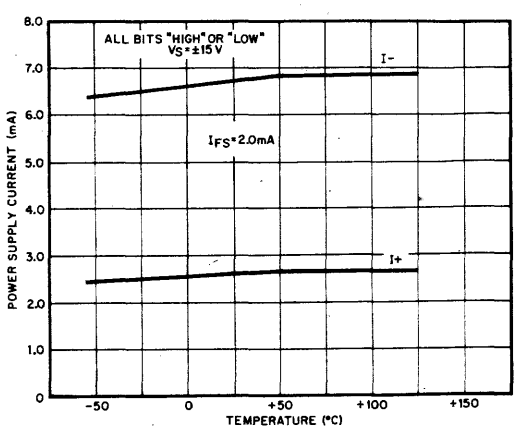


NOTE: LOGIC INPUT VOLTAGE RANGE IS INDEPENDENT OF THE POSITIVE POWER SUPPLY, AND LOGIC INPUTS MAY SWING ABOVE THE SUPPLY.

POWER SUPPLY CURRENTS VS. POWER SUPPLY VOLTAGES

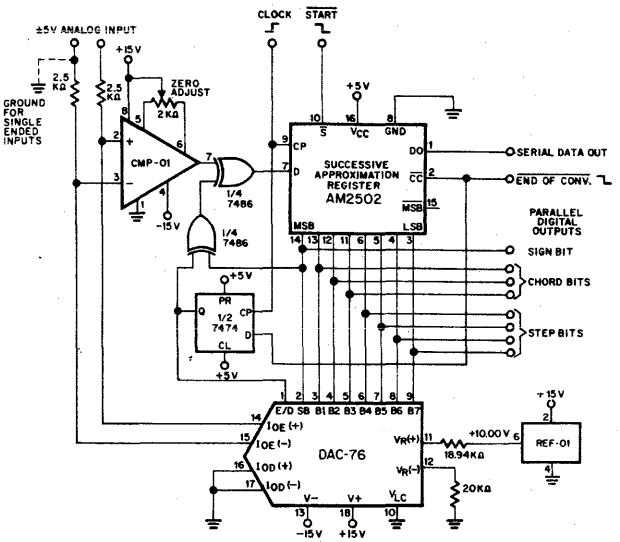


POWER SUPPLY CURRENTS VS. TEMPERATURE



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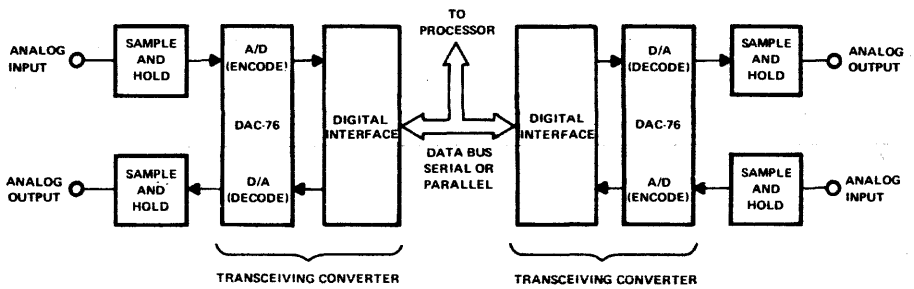
DETAILED ENCODE CONNECTIONS



NOTES:

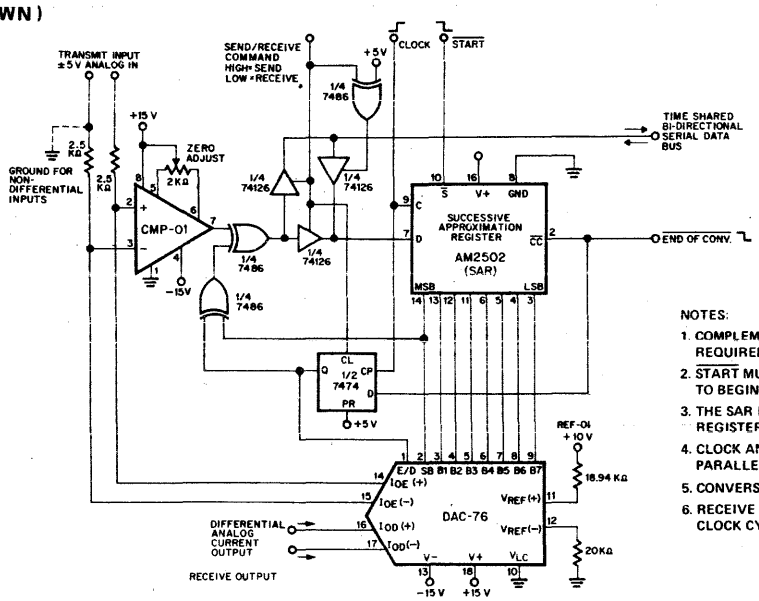
1. CONNECT $\overline{\text{END OF CONV.}}$ TO $\overline{\text{START}}$ FOR CONTINUOUS OPERATION.
2. FOR NON-CONTINUOUS OPERATION, HOLD $\overline{\text{START}}$ LOW FOR ONE CLOCK CYCLE. CONVERSIONS BEGIN ON THE NEXT LOW TO HIGH TRANSITION OF THE CLOCK AFTER $\overline{\text{START}}$ GOES HIGH.
3. CONVERSION IS COMPLETED IN 9 CLOCK CYCLES.

TRANSCEIVING CONVERTER – TWO WAY DATA TRANSMISSION



SERIAL DATA TRANSCEIVING CONVERTER

(1/2 OF SYSTEM SHOWN)



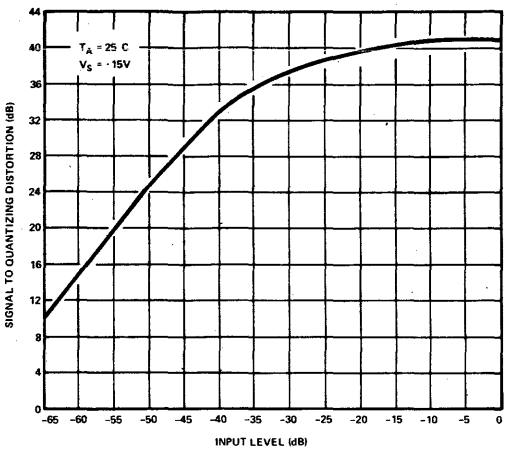
NOTES:

1. COMPLEMENTARY SEND/RECEIVE COMMANDS ARE REQUIRED FOR THE TWO ENDS.
2. $\overline{\text{START}}$ MUST BE HELD LOW FOR ONE CLOCK CYCLE TO BEGIN A SEND OR RECEIVE CYCLE.
3. THE SAR IS USED AS A SERIAL-IN/PARALLEL OUT REGISTER IN THE RECEIVE MODE.
4. CLOCK AND $\overline{\text{START}}$ MAY BE CONNECTED IN PARALLEL AT BOTH ENDS.
5. CONVERSION IS COMPLETED IN 9 CLOCK CYCLES.
6. RECEIVE OUTPUT IS AVAILABLE FOR ONE FULL CLOCK CYCLE

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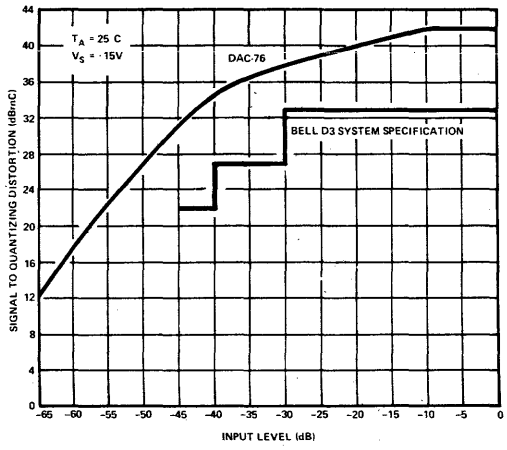
TYPICAL SIGNAL TO QUANTIZING DISTORTION CURVES

SIGNAL TO QUANTIZING DISTORTION VS. INPUT LEVEL (3 kHz FLAT FILTER)



NOTE: 0dB IS ±3.5V. +3dB IS ±5.0V OR FULL SCALE CODE (111 1111).

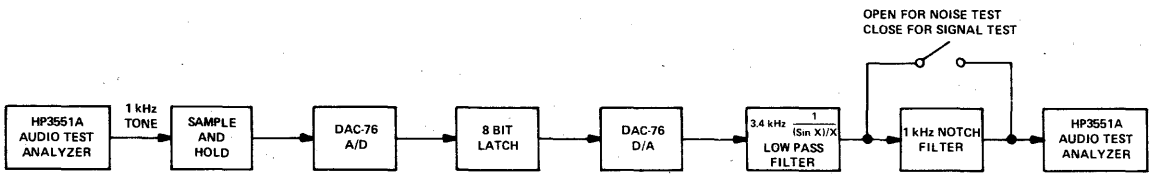
SIGNAL TO QUANTIZING DISTORTION VS. INPUT LEVEL (C-MESSAGE WEIGHTING FILTER & BELL SPEC)



NOTES:
1. 0dB IS ±3.5V. +3dB IS ±5.0V OR FULL SCALE CODE (111 1111).
2. C-MESSAGE WEIGHTING FILTER PROVIDES A FREQUENCY RESPONSE CHARACTERISTIC WHICH SIMULATES THE PERCEIVED RESPONSE OF THE HUMAN EAR TO TELEPHONE NOISE.

Note: Quantizing distortion is the difference between the original signal and the processed signal (i.e., after encoding and decoding).

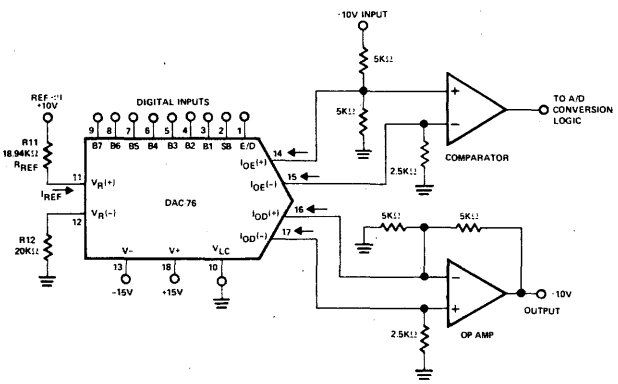
SIGNAL TO QUANTIZING DISTORTION TEST CIRCUIT BLOCK DIAGRAM



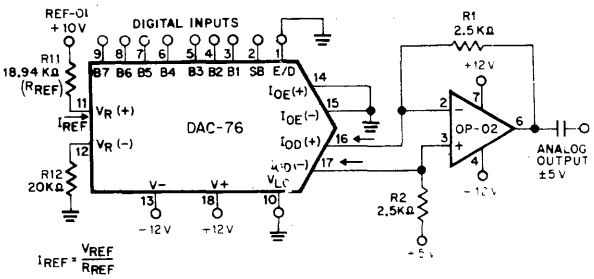
1. 8 kHz SAMPLING CONDITIONS: 62.5μsec SAMPLE PERIOD, 62.5μsec A/D CONVERSION TIME.
2. AUDIO TEST ANALYZER CONTAINS A C-MESSAGE FILTER AND A 3 kHz FLAT FILTER.

OUTPUT COMPLIANCE EXTENSION CONNECTIONS

±10V RANGE ENCODE/DECODE CONNECTIONS



COMPLIANCE EXTENSION USING AC COUPLED OUTPUT

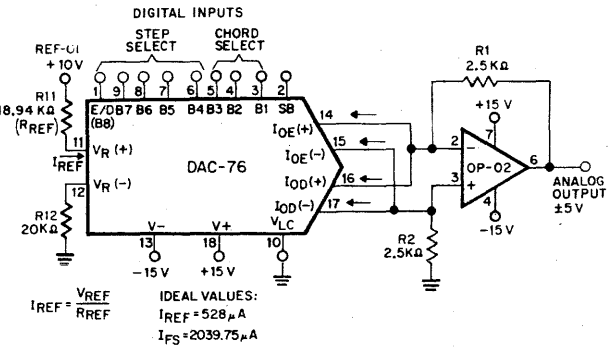


$I_{REF} = \frac{V_{REF}}{R_{REF}}$

IDEAL VALUES:
$I_{REF} = 528\mu A$
$I_{FS} = 2007.75\mu A$

EXTENSION TO SIGN PLUS 78dB DYNAMIC RANGE

EXTENDED RANGE CONNECTIONS



EXTENDED RANGE OPERATION

When used as a D/A converter only, the DAC-76 range may be extended from sign + 72dB to sign + 78dB by using the encode output current to insert additional levels halfway between each step. By connecting $I_{OD}(+)$ to $I_{OE}(+)$ and $I_{OD}(-)$ to $I_{OE}(-)$, the E/D logic input functions as a fifth step bit input. Full scale positive now becomes 1 111 11111; full scale negative is 0 111 11111. Each chord is divided into 32 steps instead of the former 16 steps, effectively increasing dynamic range by 6dB.

The accompanying table summarizes the new chord and step characteristics obtained in the extended connection shown above.

SUMMARY TABLE FOR 3 CHORD BITS AND 5 STEP BITS

CHORD	STEP (μA)	RANGE (μA)	STEP (mV)	RANGE (V)
0	0.25	0 to 7.75	0.625	0 to 0.019
1	0.5	8.25 to 23.75	1.25	0.021 to 0.059
2	1.0	24.75 to 55.75	2.5	0.062 to 0.139
3	2.0	57.75 to 119.75	5.0	0.144 to 0.299
4	4.0	123.75 to 247.75	10	0.309 to 0.619
5	8.0	255.75 to 503.75	20	0.639 to 1.259
6	16	519.75 to 1015.75	40	1.299 to 2.539
7	32	1047.75 to 2039.75	80	2.619 to 5.099

ADDITIONAL DECODE OUTPUT TABLES

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS (SIGN BIT EXCLUDED)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
1	0001	0.5	9.25	26.75	61.75	131.75	271.75	551.75	1111.75
2	0010	1	10.25	28.75	65.75	139.75	287.75	583.75	1175.75
3	0011	1.5	11.25	30.75	69.75	147.75	303.75	615.75	1239.75
4	0100	2	12.25	32.75	73.75	155.75	319.75	647.75	1303.75
5	0101	2.5	13.25	34.75	77.75	163.75	335.75	679.75	1367.75
6	0110	3	14.25	36.75	81.75	171.75	351.75	711.75	1431.75
7	0111	3.5	15.25	38.75	85.75	179.75	367.75	743.75	1495.75
8	1000	4	16.25	40.75	89.75	187.75	383.75	775.75	1559.75
9	1001	4.5	17.25	42.75	93.75	195.75	399.75	807.75	1623.75
10	1010	5	18.25	44.75	97.75	203.75	415.75	839.75	1687.75
11	1011	5.5	19.25	46.75	101.75	211.75	431.75	871.75	1751.75
12	1100	6	20.25	48.75	105.75	219.75	447.75	903.75	1815.75
13	1101	6.5	21.25	50.75	109.75	227.75	463.75	935.75	1879.75
14	1110	7	22.25	52.75	113.75	235.75	479.75	967.75	1943.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		.50	1	2	4	8	16	32	64

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CHORD SIZE SUMMARY TABLE DECODE OUTPUT (SIGN BIT EXCLUDED)

CHORD	CHORD ENDPOINTS NORMALIZED TO FULL SCALE	CHORD ENDPOINTS IN μA WITH 2007.75μA F.S.	CHORD ENDPOINTS AS A PERCENT OF FULL SCALE	CHORD ENDPOINTS IN dB DOWN FROM FULL SCALE
0	30	7.5	0.37%	-48.55
1	93	23.25	1.16%	-38.73
2	219	54.75	2.73%	-31.29
3	471	117.75	5.86%	-24.63
4	975	243.75	12.1%	-18.32
5	1983	495.75	24.7%	-12.15
6	3999	999.75	49.8%	-6.06
7	8031	2007.75	100%	0

DECODE OUTPUT EXPRESSED IN DB DOWN FROM FULL SCALE (SIGN BIT EXCLUDED)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	–	-47.73	-38.18	-30.82	-24.20	-17.90	-11.74	-5.65
1	0001	-72.07	-46.73	-37.51	-30.24	-23.66	-17.37	-11.22	-5.13
2	0010	-66.05	-45.84	-36.88	-29.70	-23.15	-16.87	-10.73	-4.65
3	0011	-62.53	-45.03	-36.30	-29.18	-22.66	-16.40	-10.27	-4.19
4	0100	-60.03	-44.29	-35.75	-28.70	-22.21	-15.96	-9.83	-3.75
5	0101	-58.10	-43.61	-35.24	-28.24	-21.77	-15.53	-9.41	-3.33
6	0110	-56.51	-42.98	-34.75	-27.80	-21.36	-15.13	-9.01	-2.94
7	0111	-55.17	-42.39	-34.29	-27.39	-20.96	-14.74	-8.63	-2.56
8	1000	-54.01	-41.84	-33.85	-26.99	-20.58	-14.37	-8.26	-2.19
9	1001	-52.99	-41.32	-33.44	-26.61	-20.22	-14.02	-7.91	-1.84
10	1010	-52.07	-40.83	-33.04	-26.25	-19.87	-13.68	-7.57	-1.51
11	1011	-51.25	-40.37	-32.66	-25.90	-19.54	-13.35	-7.25	-1.18
12	1100	-50.49	-39.93	-32.29	-25.57	-19.22	-13.03	-6.93	-0.87
13	1101	-49.80	-39.51	-31.95	-25.25	-18.91	-12.73	-6.63	-0.57
14	1110	-49.15	-39.11	-31.61	-24.94	-18.61	-12.43	-6.34	-0.28
15	1111	-48.55	-38.73	-31.29	-24.63	-18.32	-12.15	-6.06	0

DECODE OUTPUT EXPRESSED IN PERCENT OF FULL SCALE (SIGN BIT EXCLUDED)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	0.411	1.23	2.88	6.16	12.7	25.9	52.2
1	0001	0.025	0.461	1.33	3.08	6.56	13.5	27.5	55.4
2	0010	0.050	0.511	1.43	3.27	6.96	14.3	29.1	58.6
3	0011	0.075	0.560	1.53	3.47	7.36	15.1	30.7	61.7
4	0100	0.100	0.610	1.63	3.67	7.76	15.9	32.3	64.9
5	0101	0.125	0.660	1.73	3.87	8.16	16.7	33.9	68.1
6	0110	0.149	0.710	1.83	4.07	8.55	17.5	35.5	71.3
7	0111	0.174	0.760	1.93	4.27	8.95	18.3	37.0	74.5
8	1000	0.199	0.809	2.03	4.47	9.35	19.1	38.6	77.7
9	1001	0.224	0.859	2.13	4.67	9.75	19.9	40.2	80.9
10	1010	0.249	0.909	2.23	4.87	10.1	20.7	41.8	84.1
11	1011	0.274	0.959	2.33	5.07	10.5	21.5	43.4	87.2
12	1100	0.299	1.01	2.43	5.27	10.9	22.3	45.0	90.4
13	1101	0.324	1.06	2.53	5.47	11.3	23.1	46.6	93.6
14	1110	0.349	1.11	2.63	5.67	11.7	23.9	48.2	96.8
15	1111	0.374	1.16	2.73	5.86	12.1	24.7	49.8	100
STEP SIZE		0.025	0.050	0.100	0.199	0.398	0.797	1.59	3.19

DAC-100

8 & 10 BIT DIGITAL-TO-ANALOG CONVERTER

GENERAL DESCRIPTION

The DAC-100 is a complete 10 bit resolution Digital-to-Analog converter constructed on two monolithic chips in a single 16-pin DIP or 24-pin flatpack. Featuring excellent non-linearity vs. temperature performance, the DAC-100 includes a low tempco voltage reference, 10 current source/switches and a high stability thin-film R-2R ladder network. Maximum application flexibility is provided by the fast current output and by matched bipolar offset and feedback resistors which are included for use with an external op amp for voltage output applications. Although all units have 10-bit resolution, a wide choice of nonlinearity and tempco options is provided to allow price/performance optimization.

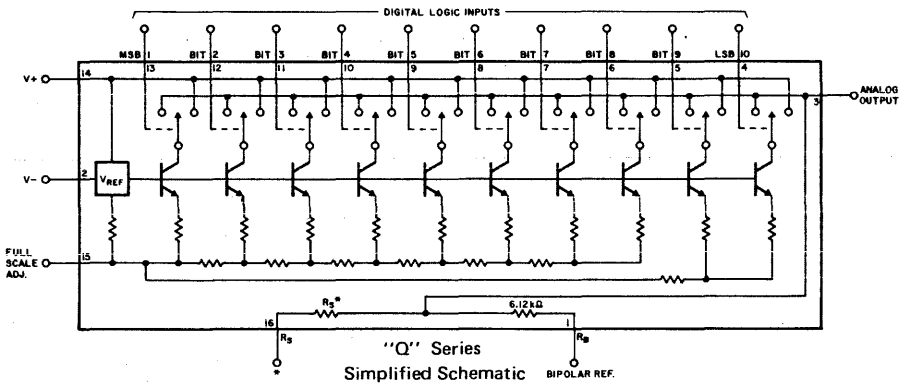
The small size, wide operating temperature range, low power consumption and high reliability construction make the DAC-100 ideal for aerospace applications. Other applications include use in servo-positioning systems, X-Y plotters, CRT displays, programmable power supplies, analog meter movement drivers, waveform generators and high speed Analog-to-Digital converters.

FEATURES

- **Complete . . . . . Internal Reference**
- **Flexible . . . . . 0 to 2mA Output**
- **Fast Settling . . . . 225nsec (8 Bits), 375nsec (10 Bits)**
- **Stable . . . . . Tempcos to ±15ppm/°C Max**
- **0°C/+70°C, −25°C/+85°C, −55°C/+125°C Models Available**
- **TTL and DTL Compatible Logic Inputs**
- **Wide Supply Range . . . . . ±6V to ±18V**
- **8 and 10 Bit Versions Available**
- **MIL-STD-883A Class B Processing Models Available**
- **Low Cost Q3, Q4 Series**

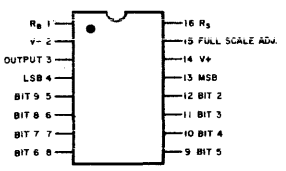
SIMPLIFIED SCHEMATIC AND PIN CONNECTIONS — 16 LEAD HERMETIC DIP

*For 10V or ±5V Operation
R_S = 4.88kΩ (Package Q1, Q3, Q5)
For 5V or ±2.5V Operation,
R_S = 2.44kΩ (Package Q2, Q4 or Q6)

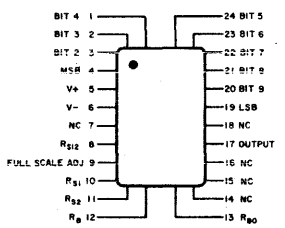


"Q" Series
Simplified Schematic

TOP VIEW



16 PIN HERMETIC
DUAL-IN-LINE
(Q-Suffix)



24 PIN HERMETIC
FLATPACK
(N-Suffix)

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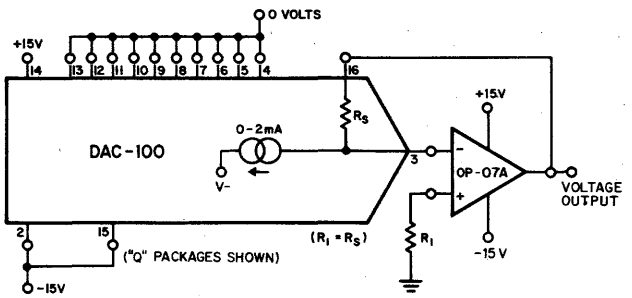
GENERAL INFORMATION

1. The DAC-100 series are digital-to-analog current converters; voltage outputs are implemented by using an external operational amplifier with the internally-provided feedback resistor. For clarity and convenience, most specifications will reference full scale output voltage rather than full scale output current, assuming an "ideal" op amp has been utilized for conversion (See test circuit at right).

2. The logic coding used for driving the DAC-100 should be complementary binary or offset complementary binary to obtain unipolar and bipolar analog outputs, respectively.

3. As shown in the ordering information below, the DAC-100 series provides a wide variety of worst-case nonlinearity and full-scale tempco combination options. All devices have 10 bits of resolution; the nonlinearity options of ±0.05%, ±0.1%, ±0.2% and ±0.3% guarantee monotonic operation for resolutions of 10, 9, 8, and 7 bits respectively. When less than the full 10 bits are utilized, the unused logic inputs must be connected to a "high" logic level (>2.1 V).

FULL SCALE TEST CIRCUIT



DEFINITION: Full Scale Tempco is defined as the change in output voltage measured in the circuit above and is expressed in ppm between 25°C and either temperature extreme divided by the corresponding temperature change.

NOTE: Since R_S precisely tracks the internal R-2R ladder network over temperature, the absolute I_{FS} Tempco of ±120ppm/°C is cancelled by R_S when the output voltage is used as in the above circuit

ORDERING INFORMATION

ORDER NUMBER: DAC-100 X X X X

NONLINEARITY		F.S. TEMPCO		PACKAGE		TEMP RANGE AND OUTPUT VOLTAGE
A	±0.05% MAX	A	15 ppm/°C MAX	Q	16 Pin HERMETIC DUAL-IN-LINE	as shown below
B	±0.1% MAX*	B	30 ppm/°C MAX*	N	24 Pin HERMETIC FLATPACK	
C	±0.2% MAX	C	60 ppm/°C MAX			
D	±0.3% MAX	D	120 ppm/°C MAX			

*NOTE: For DAC-100 BBQ5 and DAC-100 BBQ6 only; nonlinearity is ±0.1% over -25°C to +85°C and ±0.12% over -55°C to +125°C. Full Scale Tempco is 30 ppm/°C over -25°C to +85°C and 40 ppm/°C over -55°C to +125°C.

COMBINATION AVAILABILITY CHART (Temperature Range/Package Option Suffix)

Model	-55°/+125°C 883A Class B		-25°/+85°C 883A Class B		-25°/+85°C		0°/+70°C	
	10V ±5V	5V ±2.5V	10V ±5V	5V ±2.5V	10V ±5V	5V ±2.5V	10V ±5V	5V ±2.5V
DAC-100AA	–	–	N9		Q1	Q2	–	–
DAC-100AB	–	–	N9		Q1	Q2	–	–
DAC-100AC	Q5	Q6	N9		Q1	Q2	Q3	Q4
DAC-100BB	Q5	Q6	N9		Q1	Q2	–	–
DAC-100BC	Q5	Q6	N9		Q1	Q2	Q3	Q4
DAC-100CC	Q5	Q6	N9		Q1	Q2	Q3	Q4
DAC-100DD	–	–	N9		Q1	Q2	Q3	Q4

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ABSOLUTE MAXIMUM RATINGS

V+ Supply to V– Supply	0 to +36V	Operating Temperature Range	
V+ Supply to Output	0 to +18V	Q3, Q4	0°C to +70°C
V– Supply to Output	0 to –18V	All others	–55°C to +125°C
Logic Inputs to Output	–1V to +6V		
Power Dissipation (Note 1)	500mW	Storage Temperature Range	
		Q and N Packages	–65°C to +150°C
NOTES:			
1. Rating applies to ambient temperature of 100°C. Above 100°C, derate at 10mW/°C.		Lead Temperature (Soldering)	
		Q and N Packages	+300°C (60 sec)

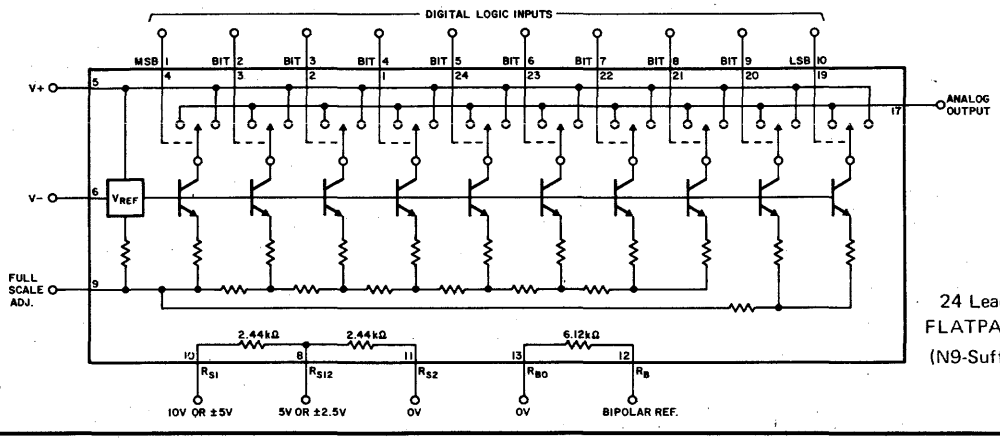
ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, -25°C ≤ T_A ≤ +85°C for Q1, Q2, and N9 devices; 0°C ≤ T_A ≤ +70°C; for Q3 and Q4, -55°C ≤ T_A ≤ +125°C for Q5 and Q6 devices, unless otherwise specified. (See BBQ5, Q6 note on previous page under Ordering Information.)

Parameter	Conditions	Min	Typ	Max	Units
Resolution		10	10	10	bits
Nonlinearity (For nonlinearity/tempco combinations, see Availability chart.)	"A" option (±½ LSB –10 bits)	–	–	± 0.05	% I_{FS}
	"B" option (±½ LSB –9 bits)	–	–	± 0.1	% I_{FS}
	"C" option (±½ LSB –8 bits)	–	–	± 0.2	% I_{FS}
	"D" option (±¾ LSB –8 bits)	–	–	± 0.3	% I_{FS}
Full Scale Tempco (See Full Scale Test Circuit.)	"A" option	–	–	± 15	ppm/°C
	"B" option	–	–	± 30	ppm/°C
	"C" option	–	–	± 60	ppm/°C
	"D" option	–	–	±120	ppm/°C
Settling Time T_A = 25°C	to ±0.05% FS	–	–	375	ns
	to ±0.1% FS	–	–	300	ns
	to ±0.2% FS	–	–	225	ns
	to ±0.4% FS	–	–	150	ns
	to ±0.8% FS	–	–	100	ns
Full Scale Output Voltage (Limits guarantee adjustability to exact 10.0 (5.0) V with a 200Ω Trimpot® between FS Adjust and V–.)	Connect FS Adjust to V–				
	10V Models (Q1, Q3, Q5, N9)	10	–	11.1	V
	5V Models (Q2, Q4, Q6)	5	–	5.55	V
	V_{IN} = 0.0V				
Zero Scale Output Voltage	V_{IN} = 2.1V	–	–	0.013	% FS
Logic Inputs	Measured with respect to output pin				
High		2.1	–	–	V
Low		–	–	0.7	V
Logic Input Current, Each Input	V_{IN} = 0 to +6V	–	–	5	µA
Logic Input Resistance	V_{IN} = 0 to +6V	–	3	–	MΩ
Logic Input Capacitance		–	2	–	pF
Output Resistance		–	500	–	kΩ
Output Capacitance		–	13	–	pF
Applied Power Supplies:					
V+	Linearity within specification	+6	–	+18	V
V–	Linearity within specification	–6	–	–18	V
Power Supply Sensitivity	V_S = ±6V to ±18V	–	–	±0.10	% per volt
Power Consumption					
Q3, Q4 models	V_S = ±15V	–	200	300	mW
All other models	V_S = ±6V	–	80	100	mW
	V_S = ±15V	–	200	250	mW

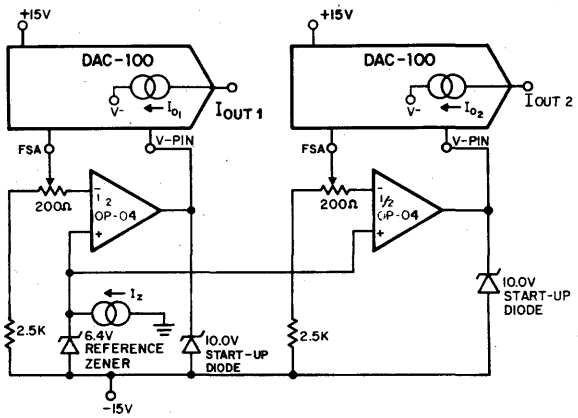
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SIMPLIFIED SCHEMATIC AND PIN CONNECTIONS – 24 LEAD FLATPACK

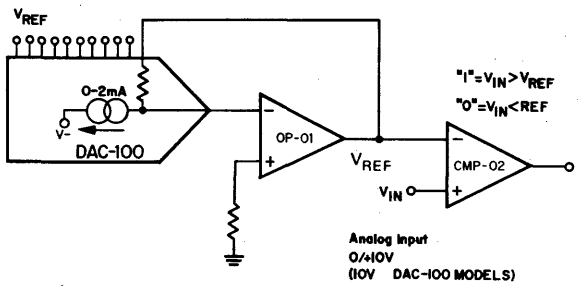


24 Lead
FLATPACK
(N9-Suffix)

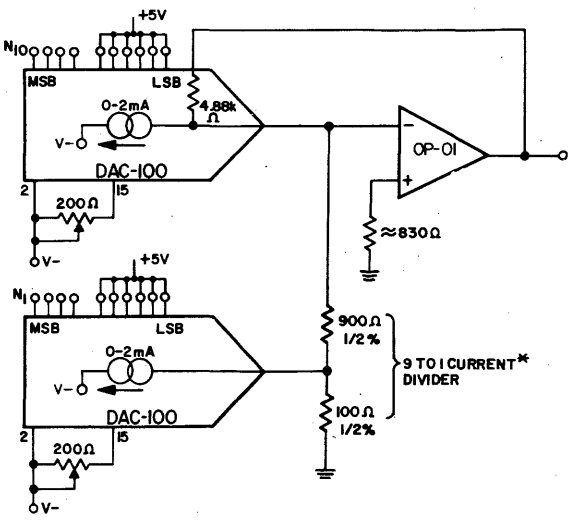
TYPICAL APPLICATIONS



EXTERNAL REFERENCE CONNECTION

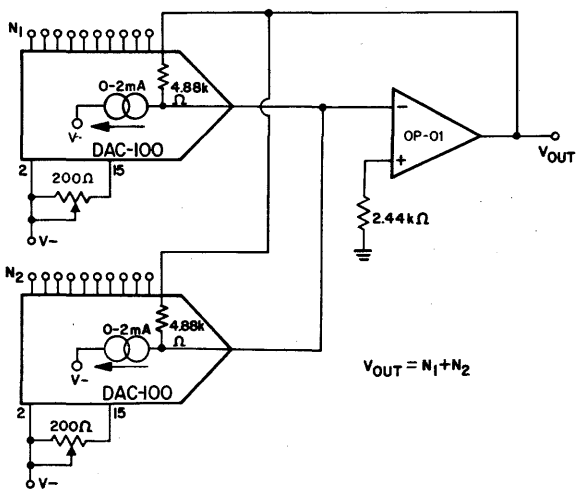


DIGITALLY PROGRAMMED LEVEL DETECTOR



BINARY-CODED-DECIMAL D/A CONVERSION

*(CAN BE EXPANDED TO 3 DIGITS BY ADDITION OF A THIRD DAC-100 AND 99 TO CURRENT DIVIDER)



ANALOG SUM OF TWO DIGITAL NUMBERS

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INTERFACING WITH CMOS LOGIC

The DAC-100 requires only about 1μA of input current into each logic stage. This enables use with CMOS inputs as long as one rule is observed: logic input voltages should not exceed 6.5 volts or V+, whichever is smaller. To provide an understanding of this rule, it is necessary to discuss the logic input stage design.

LOGIC INPUT STAGE DESIGN

For simplicity, only one of the ten identical input circuits is shown below. The DAC-100 uses a fast current-steering technique that switches a bit-weighted current between the positive supply (V+) and the analog output, which is usually constrained to be at zero volts (virtual ground) by an external summing amplifier.

Switching is accomplished by forward biasing Q4, a diode-connected transistor, for the bit "on" condition and back biasing Q4 in the "off" condition. For the "on" condition ($V_{IN} \leqslant .7$ volts), Q3 is "off"—all of the bit-weighted current, I_1, flows from the analog output through Q4 and ultimately to V-. In the "off" condition ($V_{IN} \geqslant 2.1$ volts), Q3 is "on", Q4 is back biased, and the bit-weighted current is sourced from the positive power supply instead of the analog output.

If V_{IN} is too high, Q4's emitter-base junction will experience reverse breakdown and a fault condition will occur. Equation 1 describes this condition:

$$1)\ BV_{IH} = V_{BE1} + V_{BE2} + V_{BE3} + BV_{EB4} \cong 7.7 \text{ volts}$$

Using this relationship, it can be seen that a conservative input voltage limit would be around 6.5 volts. When the 6.5V input limit is observed, DAC-100 operation with CMOS inputs is easily achieved.

±6 VOLT POWER SUPPLY OPERATION

This is the most convenient method of interfacing the DAC-100 with CMOS logic. At ±6 volts, DAC-100 power dissipation is only 80mW, which is very small considering the inclusion of a complete internal reference. No interfacing components are required with ±5% power supplies, and the CMOS logic and DAC-100 can use the same +6 volt power supply. In this application the device is directly CMOS compatible.

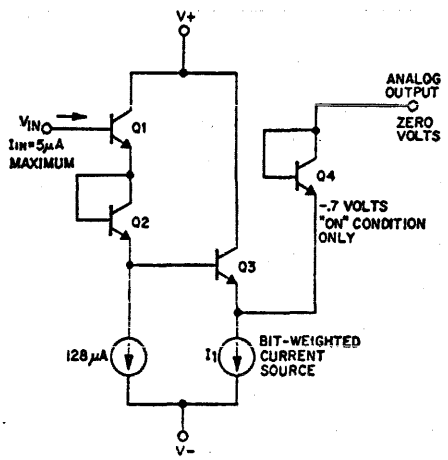
HIGH LEVEL CMOS INTERFACING

The block diagram below illustrates a convenient method for interfacing CMOS input levels between 6.5 volts and 15 volts with DAC-100. Inexpensive and readily available CMOS hex buffer/converters step down the high-level inputs to TTL levels that cannot exceed 5 volts—clearly satisfying the input stage voltage rule.

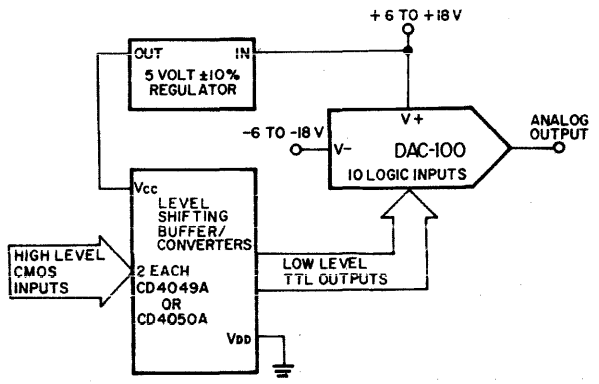
In addition to level shifting, buffer/converters provide input coding flexibility since they are available as inverting (CD4049A) or noninverting (CD4050A) devices. This gives the user a choice between negative-true and positive-true binary coding and allows the same basic DAC-100-to-CMOS interfacing method to be used in either type of application.

Since buffer/converter power consumption is very low, the required +5 volts can be provided by a simple regulator or even a resistive divider in some applications. In a multi-DAC system, one central, inexpensive 3-terminal IC regulator can supply several level shifting devices.

NOTE: For a more complete explanation and detailed circuit connections, refer to AN-14, "Interfacing PMI D/A's with CMOS Logic."



DAC-100 LOGIC INPUT STAGE



BLOCK DIAGRAM – CMOS TO DAC-100 INTERFACE

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IMPROVED AD562

SSS562

12 BIT MULTIPLYING D/A CONVERTER

GENERAL DESCRIPTION

The SSS562 is a 12-bit monolithic multiplying Digital-to-Analog converter consisting of a reference current amplifier, an R-2R ladder network, range and offset scaling resistors, and 12 high speed current switches. Improvements over the AD562 include faster settling time, lower power dissipation, greater negative power supply range, and wider voltage compliance. The SSS562 is directly interchangeable with the AD562.

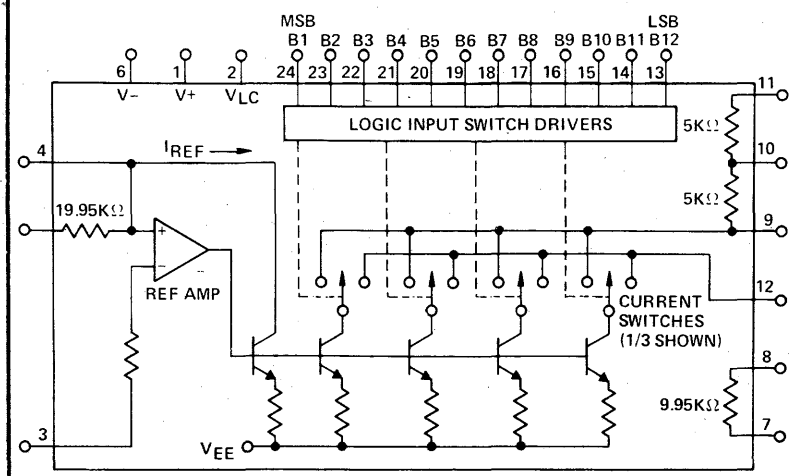
The SSS562 uses a unique trimming method, selective shorting of zener diodes by avalanche migration, to achieve 13 bit accuracy rather than laser trimming. Reliability of this trimming method has been proven in several other PMI products with over 3 years of reliability history. The SSS562 is recommended for 12 bit accuracy D/A applications where single chip reliability, small size and low cost are primary considerations.

FEATURES

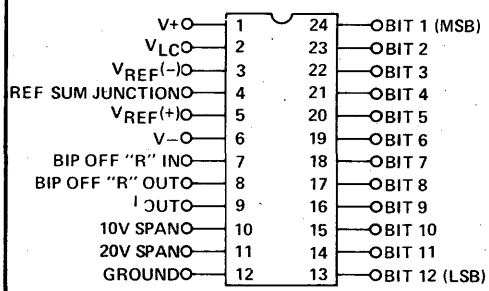
- Single Chip Monolithic Construction*
- Binary and BCD Models
- Nonlinearity to ±1/4 LSB (Max)
- Improved Settling Time . . . . . 1.5 μsec (Max)
- Fits AD562 Socket Directly
- Guaranteed Monotonicity
- High Speed Multiplying Capability
- TTL and CMOS Logic Input Compatibility
- Low Power Consumption
- Low Cost
- MIL-STD-883A Level B Models Available

For improved specifications and greater applications flexibility, see the DAC-12 High Speed Multiplying D/A Converter data sheet.

EQUIVALENT CIRCUIT



PIN CONNECTIONS



TOP VIEW
24-PIN HERMETIC DUAL IN-LINE
(V-Suffix)

ORDERING INFORMATION

MODEL NUMBER	ADI MODEL NO.	TEMP RANGE
SSS562-SD-BIN	AD562SD/BIN	-55°/+125°C
SSS562-883-BIN	AD562SD/BIN/883	-55°/+125°C
SSS562-SD-BCD	AD562SD/BCD	-55°/+125°C
SSS562-883-BCD	AD562SD/BCD/883	-55°/+125°C
SSS562-AD-BIN	AD562AD/BIN	-25°/+85°C
SSS562-AD-BCD	AD562AD/BCD	-25°/+85°C
SSS562-KD-BIN	AD562KD/BIN	0°/+70°C
SSS562-KD-BCD	AD562KD/BCD	0°/+70°C

Military Temperature Range Devices
With MIL-STD-883A Class B Processing:

ORDER: SSS562-883-BIN
SSS562-883-BCD

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ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range		Positive Power Supply (V_{CC})	36V– V_{EE}
SSS562-SD	–55°C to +125°C	Negative Power Supply (V_{EE})	36V– V_{CC}
SSS562-AD	–25°C to +85°C	V_{CC} to V_{EE}	36V
SSS562-KD	0°C to +70°C	Logic Inputs	V_{EE} to V_{EE} + 36V
Storage Temperature Range	–65°C to +150°C	Summing Junction (Pin 4)	V_{EE} to V_{CC}
Power Dissipation	500mW	CMOS/TTL Threshold (Pin 2)	V_{EE} to V_{CC}
Derate above 100°C	10mW/°C	I_{OUT} (Pin 9)	+18 to –12V
Lead Soldering Temperature	300°C (60 sec)	Span Resistors	36V

ELECTRICAL CHARACTERISTICS

These specifications apply for V_S = ±15V, V_{REF} = +10.0000V, T_A = +25°C, unless otherwise specified.

			SSS562SD			SSS562AD			SSS562KD			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Resolution (Binary Models)		T_A = Full	12	12	12	12	12	12	12	12	12	Bits
Monotonicity (Binary Models)		T_A = Full	12	–	–	12	–	–	12	–	–	Bits
Nonlinearity (Binary Models)	NL		–	–	±1/4	–	–	±1/2	–	–	±1/2	LSB
Resolution (BCD Models)		T_A = Full	3	3	3	3	3	3	3	3	3	Digits
Monotonicity (BCD Models)		T_A = Full (999 Steps)	3	–	–	3	–	–	3	–	–	Digits
Nonlinearity (BCD Models)	NL		–	–	±1/10	–	–	±1/2	–	–	±1/2	LSB
Settling Time	t_s	To ±1/2 LSB, All bits ON or OFF, current into short circuit.	–	–	1.5	–	–	1.5	–	–	1.5	µsec
Major Carry Switching Transient		To 90% compiete	–	200	–	–	200	–	–	200	–	nsec
Voltage Noise (All bits ON)	E_n	0.1Hz to 10Hz	–	30	–	–	30	–	–	30	–	µVp-p
Output Voltage Compliance	V_{OC}		–2.5	–	+10	–2.5	–	+10	–2.5	–	+10	V
Output Current Range		Unipolar (0 to –2mA)	–	±10	–	–	±10	–	–	±10	–	%
		Bipolar (–1mA to +1mA)	–	±10	–	–	±10	–	–	±10	–	%
Output Resistance			–	2.0	–	–	2.0	–	–	2.0	–	MΩ
Output Capacitance			–	30	–	–	30	–	–	30	–	pF
Zero Scale Current	I_{ZS}	All bits OFF	–	–	0.01	–	–	0.01	–	–	0.01	%FS
Logic Inputs –TTL, V_{CC} = +5V, Pin 2 Open Circuit	V_{IH}	I_{IN} = 100nA (Max)	2.0	–	–	2.0	–	–	2.0	–	–	V
	V_{IL}	I_{IN} = –100µA (Max)	–	–	0.8	–	–	0.8	–	–	0.8	V
Logic Inputs –CMOS, 4.75V ⩽ V_{CC} ⩽ 15.8V, Pin 2 to Pin 1	V_{IH}	I_{IN} = 100nA (Max)	70	–	–	70	–	–	70	–	–	% V_{CC}
	V_{IL}	I_{IN} = –100µA (Max)	–	–	30	–	–	30	–	–	30	% V_{CC}
Reference Voltage Input	Z_{IN}	20KΩ (Nominal)	–	±10	–	–	±10	–	–	±10	–	%
	V_{RR}	Range (Nominal)	0	–	±10	0	–	±10	0	–	±10	V
External Adjustment Range		(See following page)	–	±0.25	–	–	±0.25	–	–	±0.25	–	%
Power Supply Range	V+	I+ = 10mA (Typ)	4.75	–	15.8	4.75	–	15.8	4.75	–	15.8	V
	V–	I– = –15mA (Typ)	–16.5	–	–13.5	–16.5	–	–13.5	–16.5	–	–13.5	V
Power Supply Sensitivity of Gain		V+ = +5V	–	1.0	–	–	1.0	–	–	1.0	–	ppmFS/%
		V+ = +15V	–	1.0	–	–	1.0	–	–	1.0	–	ppmFS/%
		V– = –15V	–	2.0	–	–	2.0	–	–	2.0	–	ppmFS/%
The following specifications apply for V_S = ±15V, V_{REF} = +10.0000V, –55°C ⩽ T_A ⩽ +125°C for SSS562SD, –25°C ⩽ T_A ⩽ +85°C for SSS562AD, 0°C ⩽ T_A ⩽ +70°C for SSS562KD, unless otherwise specified.												
Zero Scale Temperature Coefficient	TC_{ZS}	Leakage Current	–	–	2.0	–	–	1.0	–	–	1.0	ppmFS /°C
Bipolar Offset Temperature Coefficient			–	–	4.0	–	–	4.0	–	–	4.0	ppmFS /°C
Gain Temperature Coefficient		Excludes V_{REF}	–	–	3.0	–	–	3.0	–	–	3.0	ppmFS /°C
Differential Nonlinearity Temperature Coefficient			–	2.0	–	–	2.0	–	–	2.0	–	ppmFS /°C

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MULTIPLYING ELECTRICAL CHARACTERISTICS AT T_A = +25°C (ALL MODELS)

Parameter	Description	Typ	Units
Quadrants	Two-quadrant: bipolar operation is achieved using the digital inputs only.	–	–
Reference Voltage	Unipolar. Digital input multiplies reference voltage.	0 to +10	V
Accuracy	10 bits for reduced reference voltage of +1V.	±0.05	%FS
Reference Feedthrough (Unipolar Mode)	All bits OFF, 0 to +10V (p-p) sinewave frequency for 1/2 LSB (p-p) feedthrough.	2.0	KHz
Output Slew Rate	All bits ON, 10V step change in reference voltage.	1.0	mA/μsec
Output Settling Time	All bits ON, 10V step change in reference voltage, to ±0.01% FS.	5.0	μsec
Reference Amplifier Bandwidth	Closed loop, small signal.	1.0	MHz

ADJUSTMENT PROCEDURES AND TABLE

BIPOLAR OFFSET

With all bits OFF, adjust R1 until op amp output is –2.5V on ±2.5V range, –5.0V on ±5.0V range, or –10.0V on ±10.0V range.

UNIPOLAR OFFSET

With all bits OFF, adjust R4 until op amp output is 0V. R1 and the connection from pin 8 to pin 9 are not required.

BIPOLAR BCD GAIN

Turn bits 2 and 4 ON, Turn bits 1, 3, 5 through 12 OFF. Adjust R2 until op amp output is 0V.

BIPOLAR BINARY GAIN

Turn bit 1 (MSB) ON. Turn bits 2 through 12 OFF. Adjust R2 until output is 0V.

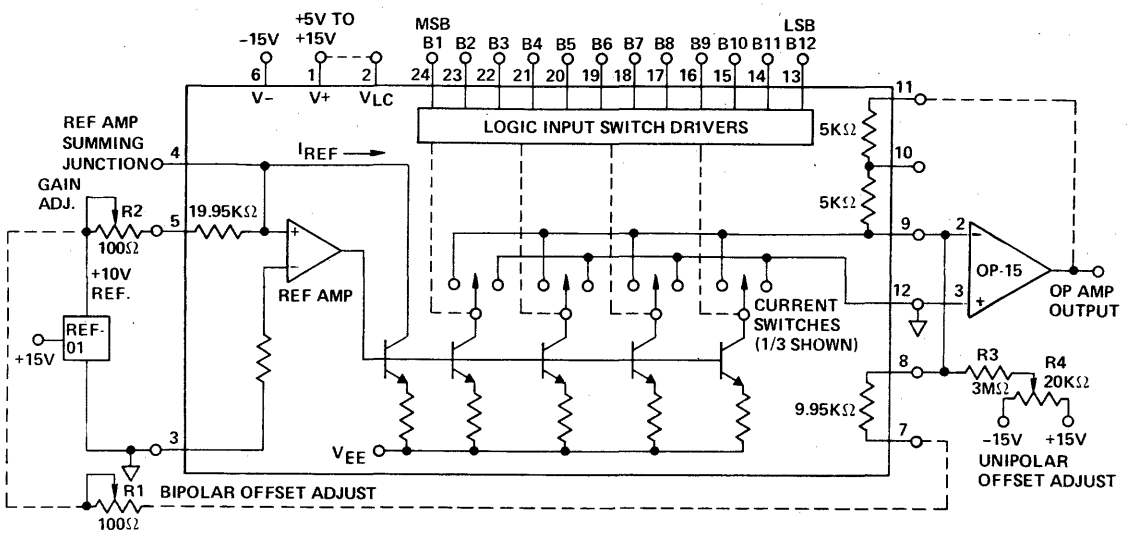
UNIPOLAR BCD GAIN

Turn bits 1, 4, 5, 8, 9, 12 ON (Code 1001 1001 1001, BCD 999). Adjust R2 until op amp output is +4.995V for 0 to +5.0V range, or +9.990V for 0 to +10.0V range.

UNIPOLAR BINARY GAIN

Turn all bits ON. Adjust R2 until op amp output is +4.9988V for 0 to +5.0V range, or +9.9976V for 0 to +10.0V range.

RANGE	OP AMP	CONNECTIONS	OFFSET ADJUST
–2.5V to +2.5V	Out to Pin 10	Pin 11 to Pin 9	R1 as below
–5.0V to +5.0V	Out to Pin 10	N.C. to Pin 11	R1 as below
–10.0V to +10.0V	Out to Pin 11	N.C. to Pin 10	R1 as below
0 to +5.0V	Out to Pin 10	Pin 11 to Pin 9	R4 as below
0 to +10.0V	Out to Pin 10	N.C. to Pin 11	R4 as below



NOTES: 1. FOR TTL AND DTL INPUTS, CONNECT +5V TO PIN 1; PIN 2 MAY BE GROUNDED OR LEFT OPEN.
2. FOR LOW VOLTAGE CMOS, CONNECT +5V TO PIN 1; SHORT PIN 2 TO PIN 1.
3. FOR HIGH VOLTAGE CMOS, CONNECT +15V TO PIN 1; SHORT PIN 2 TO PIN 1.

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PRELIMINARY

MUX-08

PROTECTED 8 CHANNEL BI-FET ANALOG MULTIPLEXER

GENERAL DESCRIPTION

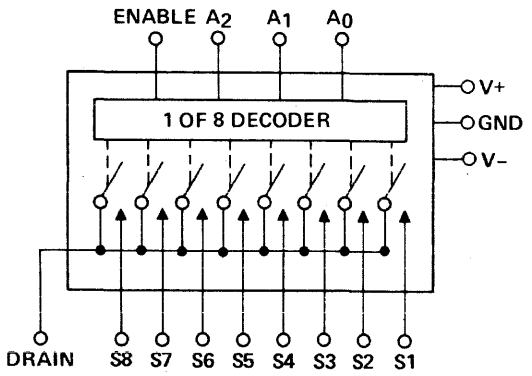
The MUX-08 is a monolithic 8 channel analog multiplexer which connects a single output to 1 of the 8 analog inputs depending upon the state of a 3-bit binary address. Disconnection of the output is provided by a logical "0" at the ENABLE input, thereby providing a package select function.

Fabricated with Precision Monolithics' high performance BI-FET technology, this device features overvoltage protection that is fail safe with power loss, while offering low, constant "ON" resistance. Performance advantages include low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. This multiplexer does not suffer from latch-up or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pullup resistors.

FEATURES

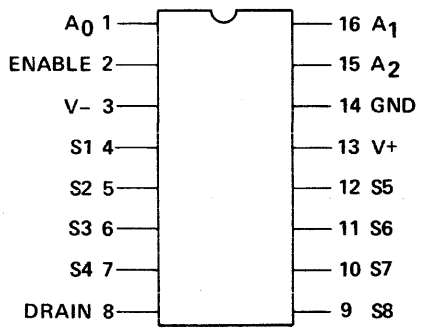
- Pin Compatible With DG508, HI-508A, LF11508
- JFET Switches Rather Than CMOS
- No Static Discharge Blow-out Problem
- No SCR Latch-up Problems
- Analog Inputs Overvoltage Protected ±20V Beyond Normal Ratings
- Fail Safe With Power Loss
- Low "ON" Resistance . . . . . 220Ω TYP
- Low Output Leakage Current . . . . . 100nA MAX
- Digital Inputs Compatible With TTL and CMOS
- No Pullup Resistors Required To Insure Break-Before-Make Action With TTL Inputs

FUNCTIONAL DIAGRAM AND TRUTH TABLE



A_2	A_1	A_0	E_N	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

PIN CONNECTIONS AND ORDERING INFORMATION



TOP VIEW

16 PIN HERMETIC DUAL-IN-LINE
(Q-Suffix)

MODEL	25°C "ON" RESISTANCE	TEMP RANGE
MUX-08AQ	220Ω	-55°C TO +125°C
MUX-08BQ	300Ω	-55°C TO +125°C
MUX-08EQ	220Ω	-25°C TO +85°C
MUX-08FQ	300Ω	-25°C TO +85°C

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PRELIMINARY

MUX-16

PROTECTED 16 CHANNEL BI-FET ANALOG MULTIPLEXER

GENERAL DESCRIPTION

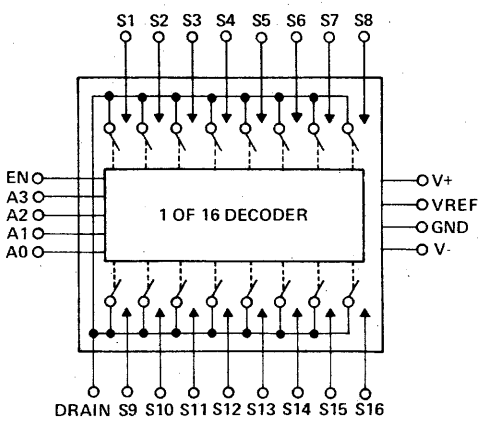
The MUX-16 is a monolithic 16 channel analog multiplexer which connects a single output to 1 of the 16 analog inputs depending upon the state of a 4-bit binary address. Disconnection of the output is provided by a logical "0" at the ENABLE input, thereby providing a package select function.

Fabricated with Precision Monolithics' high performance BI-FET technology, this device features overvoltage protection that is fail safe with power loss, while offering low, constant "ON" resistance. Performance advantages include low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. This multiplexer does not suffer from latch-up or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pullup resistors.

FEATURES

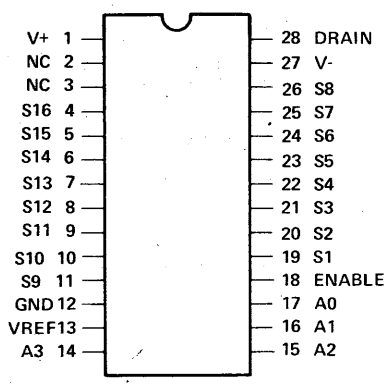
- Pin Compatible With DG506, HI-506A
- JFET Switches Rather Than CMOS
- No Static Discharge Blow-out Problem
- No SCR Latch-up Problems
- Analog Inputs Overvoltage Protected ±20V Beyond Normal Ratings
- Fail Safe With Power Loss
- Low "ON" Resistance . . . . . 250 Ω TYP
- Digital Inputs Compatible With TTL and CMOS
- No Pullup Resistors Required To Insure Break-Before-Make Action With TTL Inputs

FUNCTIONAL DIAGRAM AND TRUTH TABLE



A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

PIN CONNECTIONS AND ORDERING INFORMATION



TOP VIEW

28 PIN HERMETIC DUAL-IN-LINE
(T Suffix)

MODEL	25°C "ON" RESISTANCE	TEMP RANGE
MUX-16AT	250 Ω	-55°C TO +125°C
MUX-16BT	350 Ω	-55°C TO +125°C
MUX-16ET	250 Ω	-25°C TO +85°C
MUX 16FT	350 Ω	-25°C TO +85°C

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PRELIMINARY

MUX-24

PROTECTED DUAL 4 CHANNEL ANALOG MULTIPLEXER

GENERAL DESCRIPTION

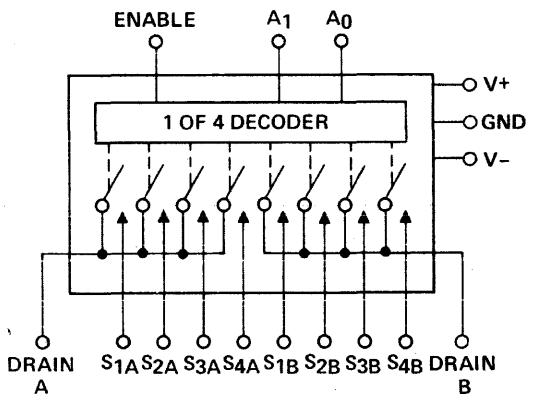
The MUX-24 is a monolithic 4-channel differential analog multiplexer configured in a double pole, 4-position (plus OFF) electronic switch array. A 2-bit binary input address connects a pair of independant analog inputs from each 4-channel input section to the corresponding pairof independant analog output "poles". Disconnection of both outputs is provided by a logical '0' at the ENABLE input, thereby offering a package select function.

Fabricated with Precision Monolithics' high performance BI-FET technology, this device features overvoltage protection that is fail safe with power loss, while offering low, constant "ON" resistance. Performance advantages include low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. This multiplexer does not suffer from latch-up or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pullup resistors.

FEATURES

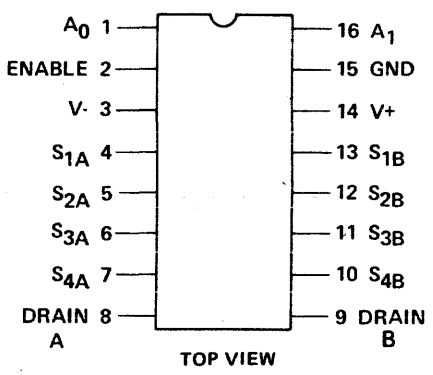
- Pin Compatible With DG509, HI-509A, LF11509
- JFET Switches Rather Than CMOS
- No Static Discharge Blow-out Problem
- No SCR Latch-up Problems
- Analog Inputs Overvoltage Protected ±20V Beyond Normal Ratings
- Fail Safe With Power Loss
- Low "ON" Resistance . . . . . 220Ω TYP
- Digital Inputs Compatible With TTL and CMOS
- No Pullup Resistors Required To Insure Break-Before-Make Action With TTL Inputs

FUNCTIONAL DIAGRAM AND TRUTH TABLE



A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

PIN CONNECTIONS AND ORDERING INFORMATION



16 PIN HERMETIC DUAL-IN-LINE
(Q-Suffix)

MODEL	25°C "ON" RESISTANCE	TEMP RANGE
MUX-24AQ	220 Ω	-55°C TO +125°C
MUX-24BQ	300 Ω	-55°C TO +125°C
MUX-24EQ	220 Ω	-25°C TO +85°C
MUX-24FQ	300 Ω	-25°C TO +85°C

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PRELIMINARY

MUX-28

PROTECTED DUAL 8 CHANNEL ANALOG MULTIPLEXER

GENERAL DESCRIPTION

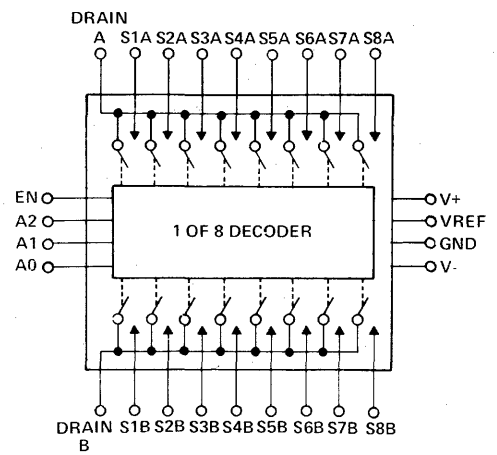
The MUX-28 is a monolithic 8-channel differential analog multiplexer configured in a double pole, 8-position (plus OFF) electronic switch array. A 3-bit binary input address connects a pair of independant analog inputs from each 8-channel input section to the corresponding pair of independant analog output "poles". Disconnection of both outputs is provided by a logical '0' at the ENABLE input, thereby offering a package select function.

Fabricated with Precision Monolithics' high performance BI-FET technology, this device features overvoltage protection that is fail safe with power loss, while offering low, constant "ON" resistance. Performance advantages include low leakag currents and fast settling time with low crosstalk to satisfy a wide variety of applications. This multiplexer does not sufier from latch-up or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pullup resistors.

FEATURES

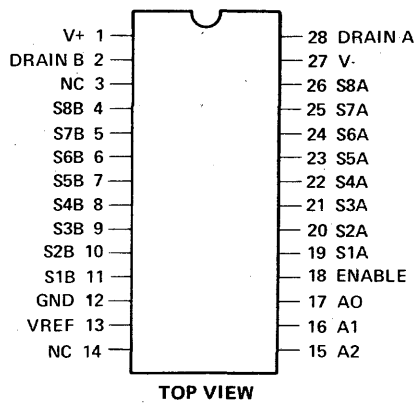
- Pin Compatible With DG507, HI-507A
- JFET Switches Rather Than CMOS
- No Static Discharge Blow-out Problem
- No SCR Latch-up Problems
- Analog Inputs Overvoltage Protected ±20V Beyond Normal Ratings
- Fail Safe With Power Loss
- Low "ON" Resistance . . . . . 250Ω TYP
- Digital Inputs Compatible With TTL and CMOS
- No Pullup Resistors Required To Insure Break-Before-Make Action With TTL Inputs

FUNCTIONAL DIAGRAM AND TRUTH TABLE



A1	A0	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
L	L	H	5
L	H	H	6
H	L	H	7
H	H	H	8

PIN CONNECTIONS AND ORDERING INFORMATION



TOP VIEW

28PIN HERMETIC DUAL-IN-LINE
(T-Suffix)

MODEL	25°C "ON" RESISTANCE	TEMP RANGE
MUX-28AT	250Ω	-55°C TO +125°C
MUX-28BT	350Ω	-55°C TO +125°C
MUX-28ET	250Ω	-25°C TO +85°C
MUX-28FT	350Ω	-25°C TO +85°C

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PRELIMINARY

MUX-88

PROTECTED 8 CHANNEL BI-FET ANALOG MULTIPLEXER

GENERAL DESCRIPTION

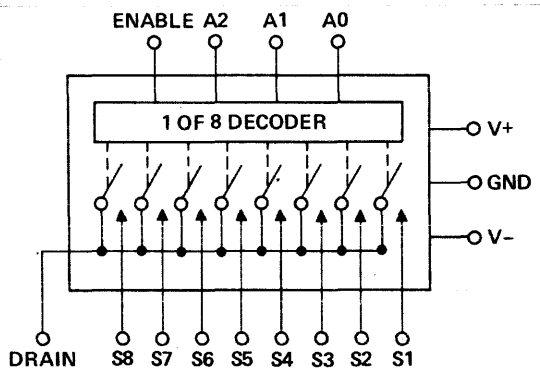
The MUX-88 is a monolithic 8 channel analog multiplexer which connects a single output to 1 of the 8 analog inputs depending upon the state of a 3-bit binary address. Disconnection of the output is provided by a logical "0" at the enable input, thereby providing a package select function.

Fabricated with Precision Monolithics' high performance BI-FET technology, this device features overvoltage protection that is fail safe with power loss, while offering low, constant "ON" resistance. Performance advantages include low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. This multiplexer does not suffer from latch-up or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pullup resistors.

FEATURES

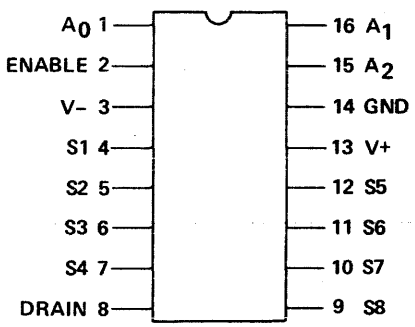
- Pin Compatible With DG508, HI-508A, LF11508
- JFET Switches Rather Than CMOS
- No Static Discharge Blow-out Problem
- No SCR Latch-up Problems
- Analog Inputs Overvoltage Protected ±20V Beyond Normal Ratings
- Fail Safe With Power Loss
- Low "ON" Resistance . . . . . 220Ω TYP
- Low Output Leakage Current . . . . . 100nA MAX
- Digital Inputs Compatible With TTL and CMOS
- No Pullup Resistors Required To Insure Break-Before-Make Action With TTL Inputs

FUNCTIONAL DIAGRAM AND TRUTH TABLE



A_2	A_1	A_0	E_N	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

PIN CONNECTIONS AND ORDERING INFORMATION



TOP VIEW

16 PIN HERMETIC DUAL-IN-LINE
(Q-Suffix)

MODEL	TEMP RANGE
MUX-88AQ	-55°C TO +125°C
MUX-88BQ	-55°C TO +125°C
MUX-88EQ	-25°C TO +85°C
MUX-88FQ	-25°C TO +85°C

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Operating Temperature Range, MUX-88AQ, BQ	–55°C to +125°C	Max Junction Temperature	150°C
Operating Temperature Range, MUX-88EQ, FQ	–25°C to +85°C	V+ Supply to V– Supply	36V
Storage Temperature Range	–65°C to +150°C	V+ Supply to Ground	18V
Power Dissipation	500mW	Logic Input Voltage	–4V to V+ Supply
Derate above 100°C	10mW/°C	Analog Input Voltage	V– Supply –20V to V+ Supply +15V
Lead Soldering Temperature	300°C (60 sec)	Max Current Through Any Pin	25mA

ELECTRICAL CHARACTERISTICS

These specifications apply for V+ = 15V, V– = –15V and T_A = 25°C unless otherwise specified.

			MUX-88A			MUX-88B			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
"ON" Resistance	R_{ON}	V_D = 0V, I_S = 100μA	–	220	260	–	300	370	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	–10V ≤ V_D ≤ 10V, I_S = 100μA	–	–	1.6	–	–	4.0	%
R_{ON} Match Between Switches	R_{ON} Match	V_D = 0V, I_S = 100μA	–	8.0	20	–	15	30	Ω
Source Current (Switch "OFF")	$I_{S(OFF)}$	V_S = 11V, V_D = –11V (Note 1)	–	0.01	0.1	–	0.01	0.1	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	V_S = 11V, V_D = –11V (Note 1)	–	0.1	1.0	–	0.1	1.0	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$	V_D = 11V (Note 1)	–	0.1	1.0	–	0.1	1.0	nA
Digital "1" Input Voltage	V_{INH}		2.0	–	–	2.0	–	–	Volts
Digital "0" Input Voltage	V_{INL}		–	–	0.8	–	–	0.8	Volts
Digital "0" Input Current	I_{INL}	V_{IN} = 0.7V	–	1.0	10	–	1.0	10	μA
Digital "0" Enable Current	$I_{INL(EN)}$	V_{EN} = 0.7V	–	4.0	10	–	4.0	10	μA
Digital Input Capacitance	C_{DIG}		–	3.0	–	–	3.0	–	pF
Switching Time	t_{TRAN}	Figure 1 (Note 2)	–	1.0	1.3	–	1.5	2.1	μsec
Output Settling Time	t_s	10V step to .025%	–	2.9	–	–	2.9	–	μsec
Break-Before-Make Delay	t_{DLY}	Figure 3	–	0.8	–	–	1.0	–	μsec
Enable Delay "ON"	$t_{ON(EN)}$	Figure 2	–	1.0	–	–	1.2	–	μsec
Enable Delay "OFF"	$t_{OFF(EN)}$	Figure 2	–	0.2	–	–	0.2	–	μsec
"OFF" Isolation	ISO_{OFF}	(Note 3)	–	–80	–	–	–80	–	dB
Crosstalk	CT	(Note 3)	–	–80	–	–	–80	–	dB
Source Capacitance	$C_{S(OFF)}$	Switch "OFF", V_S = 0V, V_D = 0V	–	2.5	–	–	2.5	–	pF
Drain Capacitance	$C_{D(OFF)}$	Switch "OFF", V_S = 0V, V_D = 0V	–	12	–	–	12	–	pF
Input to Output Capacitance	$C_{DS(OFF)}$	Switch "OFF", V_S = 0V, V_D = 0V	–	0.2	–	–	0.2	–	pF
Positive Supply Current (All Digital Inputs Grounded)	I+	V+ = 15V	–	10	12	–	6.0	8.0	mA
		V+ = 5V	–	8.0	–	–	5.0	–	mA
Negative Supply Current (All Digital Inputs Grounded)	I–	V– = –15V	–	3.0	3.8	–	2.0	3.0	mA
		V– = –5V	–	2.5	–	–	1.8	–	mA
These specifications apply for V+ = 15V, V– = –15V and –55°C ≤ T_A ≤ +125°C unless otherwise specified.									
"ON" Resistance	R_{ON}	V_D = 0V, I_S = 100μA	–	–	370	–	–	480	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	–10V ≤ V_D ≤ 10V, I_S = 100μA	–	–	2.4	–	–	6.0	%
R_{ON} Match Between Switches	R_{ON} Match	V_D = 0V, I_S = 100μA	–	10	30	–	15	45	Ω
Source Current (Switch "OFF")	$I_{S(OFF)}$	V_S = 11V, V_D = –11V (Note 2)	–	–	10	–	–	10	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	V_S = 11V, V_D = –11V (Note 2)	–	–	100	–	–	100	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$	V_D = 11V (Note 2)	–	–	100	–	–	100	nA
Digital "1" Input Voltage	V_{INH}		2.0	–	–	2.0	–	–	Volts
Digital "0" Input Voltage	V_{INL}		–	–	0.8	–	–	0.8	Volts
Digital "0" Input Current	I_{INL}	V_{IN} = 0.7V	–	–	20	–	–	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	V_{EN} = 0.7V	–	–	20	–	–	20	μA
Positive Supply Current	I+	All Digital Inputs Grounded	–	–	15	–	–	11	mA
Negative Supply Current	I–	All Digital Inputs Grounded	–	–	5.0	–	–	4.0	mA

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ELECTRICAL CHARACTERISTICS NOTES

NOTE 1: Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".

NOTE 2: Lots are sample tested to this parameter. The measurement conditions of FIGURE 1 insure worst case transition time.

NOTE 3: "OFF" isolation is measured with all switches "OFF" and driving a source. Crosstalk is measured with R_L = 1K, C_L = 7pF, V_s = 3V RMS, F = 100 kHz.

ELECTRICAL CHARACTERISTICS

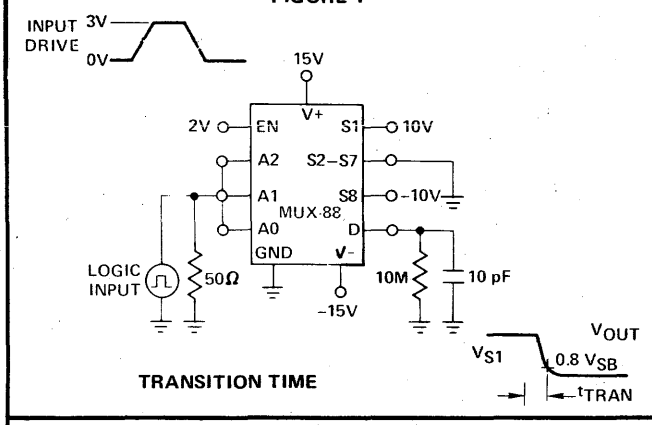
These specifications apply for V+ = 15V, V– = –15V and T_A = 25°C unless otherwise specified.

			MUX-88E			MUX-88F			
Parameter	Symbol	Conditions	Min	Typ	Max	Min	Typ	Max	Units
"ON" Resistance	R_{ON}	V_D = 0V, I_S = 100μA	–	220	260	–	300	370	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	–10V ≤ V_D ≤ 10V, I_S = 100μA	–	–	1.6	–	–	4.0	%
R_{ON} Match Between Switches	R_{ON} Match	V_D = 0V, I_S = 100μA	–	8.0	20	–	15	30	Ω
Source Current (Switch "OFF")	$I_{S(OFF)}$	V_S = 11V, V_D = –11V (Note 1)	–	0.01	0.1	–	0.01	0.1	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	V_S = 11V, V_D = –11V (Note 1)	–	0.1	1.0	–	0.1	1.0	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$	V_D = 11V (Note 1)	–	0.1	1.0	–	0.1	1.0	nA
Digital "1" Input Voltage	V_{INH}		2.0	–	–	2.0	–	–	Volts
Digital "0" Input Voltage	V_{INL}		–	–	0.8	–	–	0.8	Volts
Digital "0" Input Current	I_{INL}	V_{IN} = 0.7V	–	1.0	10	–	1.0	10	μA
Digital "0" Enable Current	$I_{INL(EN)}$	V_{EN} = 0.7V	–	4.0	10	–	4.0	10	μA
Digital Input Capacitance	C_{DIG}		–	3.0	–	–	3.0	–	pF
Switching Time	t_{TRAN}	Figure 1 (Note 2)	–	1.0	1.3	–	1.5	2.1	μsec
Output Settling Time	t_s	10V step to .025%	–	2.9	–	–	2.9	–	μsec
Break-Before-Make Delay	t_{DLY}	Figure 3	–	0.8	–	–	1.0	–	μsec
Enable Delay "ON"	$t_{ON(EN)}$	Figure 2	–	1.0	–	–	1.2	–	μsec
Enable Delay "OFF"	$t_{OFF(EN)}$	Figure 2	–	0.2	–	–	0.2	–	μsec
"OFF" Isolation	ISO_{OFF}	(Note 3)	–	–80	–	–	–80	–	dB
Crosstalk	CT	(Note 3)	–	–80	–	–	–80	–	dB
Source Capacitance	$C_{S(OFF)}$	Switch "OFF", V_S = 0V, V_D = 0V	–	2.5	–	–	2.5	–	pF
Drain Capacitance	$C_{D(OFF)}$	Switch "OFF", V_S = 0V, V_D = 0V	–	12	–	–	12	–	pF
Input to Output Capacitance	$C_{DS(OFF)}$	Switch "OFF", V_S = 0V, V_D = 0V	–	0.2	–	–	0.2	–	pF
Positive Supply Current (All Digital Inputs Grounded)	I+	V+ = 15V	–	10	12	–	6.0	8.0	mA
		V+ = 5V	–	8.0	–	–	5.0	–	mA
Negative Supply Current (All Digital Inputs Grounded)	I–	V– = –15V	–	3.0	3.8	–	2.0	3.0	mA
		V– = –5V	–	2.5	–	–	1.8	–	mA
These specifications apply for V+ = 15V, V– = –15V and –25°C ≤ T_A ≤ 85°C unless otherwise specified.									
"ON" Resistance	R_{ON}	V_D = 0V, I_S = 100μA	–	–	370	–	–	480	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	–10V ≤ V_D ≤ 10V, I_S = 100μA	–	–	2.4	–	–	6.0	%
R_{ON} Match Between Switches	R_{ON} Match	V_D = 0V, I_S = 100μA	–	10	30	–	15	45	Ω
Source Current (Switch "OFF")	$I_{S(OFF)}$	V_S = 11V, V_D = –11V (Note 2)	–	–	10	–	–	10	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	V_S = 11V, V_D = –11V (Note 2)	–	–	100	–	–	100	nA
Leakage Current (Switch "ON")	$I_{D(ON)}$	V_D = 11V (Note 2)	–	–	100	–	–	100	nA
Digital "1" Input Voltage	V_{INH}		2.0	–	–	2.0	–	–	Volts
Digital "0" Input Voltage	V_{INL}		–	–	0.8	–	–	0.8	Volts
Digital "0" Input Current	I_{INL}	V_{IN} = 0.7V	–	–	20	–	–	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	V_{EN} = 0.7V	–	–	20	–	–	20	μA
Positive Supply Current	I+	All Digital Inputs Grounded	–	–	15	–	–	11	mA
Negative Supply Current	I–	All Digital Inputs Grounded	–	–	5.0	–	–	4.0	mA

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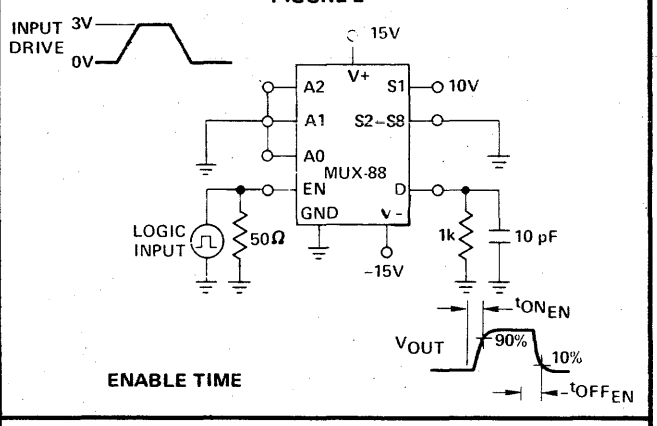
A.C. TEST CIRCUITS AND PERFORMANCE CHARACTERISTICS

FIGURE 1



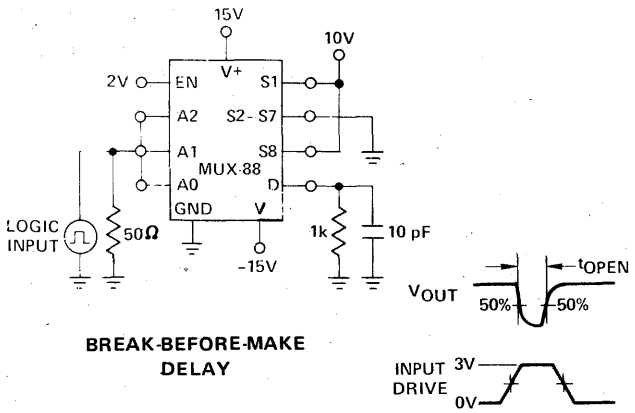
TRANSITION TIME

FIGURE 2



ENABLE TIME

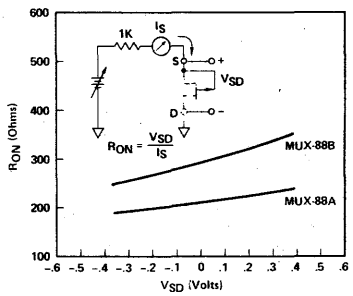
FIGURE 3



BREAK-BEFORE-MAKE DELAY

FIGURE 4

"ON" RESISTANCE CHARACTERISTICS
$T_A = 25°C$

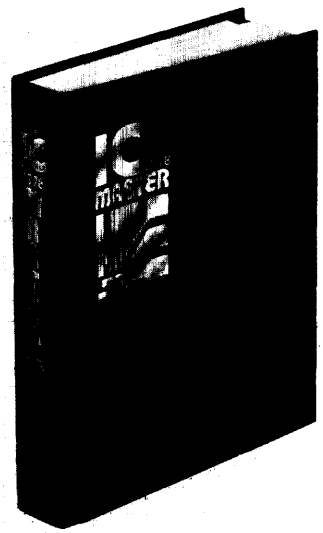


APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFET's in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with BI-FET processing rather than CMOS, special handling is not necessary to prevent damage to this multiplexer. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about .1 μA) as the input voltage is raised above $\approx$1.4V.

The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of -15V to +11V with $V_{SUPPLY} = \pm 15V$. Input voltages up to $\pm$20V beyond this normal input range are permissible with device power on. Input voltages of up to +11V and lower than -15V are allowable with device power off. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply) otherwise leakage currents will increase and a normally "OFF" switch may be falsely turned "ON". Although the output voltage will be erroneous, damage to the multiplexer will not result because the switch "ON" resistance greatly increases and the I_{DSS} of the JFET protects the switch (Figure 4). When operating with negative input voltages, current through an "ON" switch must be externally limited to prevent the voltage drop across the switch from exceeding -0.4V source to drain. This is not a problem generally, for in most applications the multiplexer output will be connected to a high impedance load.

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DESCRIPTION

The Raytheon 4152 consists of a comparator, a one-shot, a precise gated current-source output, an internal voltage reference, and an open-collector output . . . all on a single monolithic IC chip. These elements can be combined via external pin connections to perform a wide variety of circuit functions.

The versatility of this unique IC makes it easy to tailor the circuit operation to your needs. Pulse width, scale factor, and output drive are set by external resistors as shown in Figure 1. Combine the versatile 4152 with an op amp or two, some digital circuits, and the range of cost-effective applications becomes even greater.

The Raytheon 4152 provides a versatile, low-cost means of accurately converting an analog signal to a pulse train of proportional frequency, and vice versa. It can be imaginatively applied to a broad range of signal conditioning applications once the various functional blocks within the IC are understood.

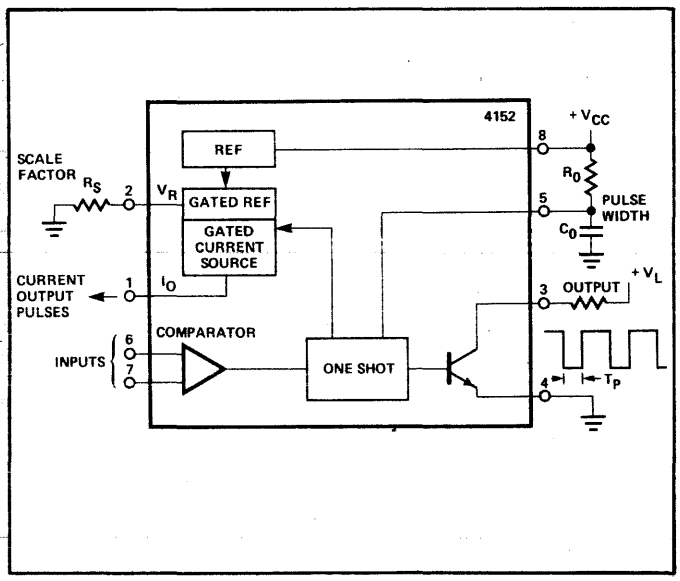


Figure 1. Functional Diagram of Raytheon 4152.

FEATURES

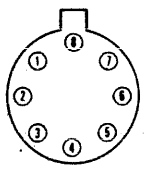
- Single supply operation (+7 V to +22 V)
- Pulse output compatible with all logic forms (DTL/TTL/ CMOS)
- Programmable scale factor (K)
- High linearity ±0.05% max
- Temperature stability ±150 ppm/°C max
- High noise rejection
- Inherent monotonicity
- Easily transmittable output
- Simple full scale trim
- Single-ended input, referenced to ground
- V/F or F/V conversion
- Voltage or current input
- Wide dynamic range

APPLICATIONS

- Precision voltage-to-frequency-converters
- Pulse-width modulators
- Programmable pulse generators
- Frequency-to-voltage converters
- Integrating analog-to-digital converter
- Long-term analog integrator
- Signal conversion —
  - Current-to-frequency
  - Temperature-to-frequency
  - Pressure-to-frequency
  - Capacitance-to-frequency
  - Frequency-to-current
- Signal isolation
  - VFC → opto-isolation → FVC
  - ADC with opto-isolation
- Signal encoding
  - FSK modulation/demodulation
  - Pulse-width modulation
- Frequency scaling
- DC motor speed control

CONNECTION INFORMATION

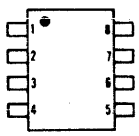
TE (TO-99) METAL CAN
(Top View)



Order Part Nos.: RC4151T, RM4151T

NOTE: PIN 4 CONNECTED TO CASE

NB MINIATURE DUAL-IN-LINE
(Top View)



Order Part Nos.: RC4151NB, RV4151NB

PIN	FUNCTION
1	CURRENT SOURCE
2	SCALE FACTOR
3	LOGIC OUTPUT
4	GROUND
5	ONE-SHOT R, C
6	THRESHOLD
7	INPUT VOLTAGE
8	V_{CC}

RAYTHEON
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Input Comparator

The input comparator section consists of transistors Q1 through Q7 (see Figure 2). A PNP ground-sensing input stage provides capability of operating down to low input voltages, thus the input range on either input is from zero up to $+V_S$-3V (power supply voltage less three volts). This is particularly important for single-supply operation. Input comparator gain is approximately 10,000. The output of the comparator, transistor Q7, switches from OFF to ON when the input voltage applied to pin 7 becomes more positive than the input voltage on pin 6. The output transistor Q7 going into saturation is used to trigger the one-shot.

One important precaution: The voltage applied to the input comparator (pins 6 and 7) must not be more negative than 0.3 V relative to the ground terminal (pin 4) unless there is protective current limiting. Negative input voltages will saturate the input PNP transistors and cause excessive input base current. This input-base current must not be allowed to exceed 25 mA over an extended period of time or the IC could be damaged. If there is a possibility of continuous excessive negative voltage on the input, then a resistor in series with the input should be added to limit the input current.

One-Shot Circuit

Pulse-width of the one-shot is determined by the external components R_o, C_o that are connected to pin 5. The capacitor C_o is normally discharged through the saturated transistor Q16. When the one-shot timing cycle is initiated, capacitor C_o is released by Q16 turning OFF and allowed to charge towards $+V_{CC}$ through R_o. At 2/3 of $+V_{CC}$, transistor Q16 is switched ON and the capacitor C_o is discharged. The pulse width will therefore be determined by the following equation:

$$1 - \epsilon^{\frac{-T_p}{R_o C_o}} = 0.667$$

$$T_p = 1.1\, R_o C_o$$

Pulse width T_p is independent of supply voltage $+V_{CC}$. For best linearity and stability, R_o and C_o should be selected within a range of 5 KΩ to 500 KΩ and 0.001 μF to 1.0 μF.

A latching action by the RS flip-flop comprised of Q9 and Q11 assures that the timing cycle will be completed regardless of input voltage. The flip-flop is set by Q7 going into the ON state. Q9 is normally OFF and Q11 normally ON; so Q7 going low will cause Q11 to switch OFF and Q9 to switch ON. Since Q9 and Q7 collectors are tied together, Q9 will keep the collectors low regardless of Q7 state. At the end of the timing cycle, Q10 is switched ON and this will make Q9 go OFF. If Q7 is OFF, then the flip-flop can reset to the normal state where Q9 is OFF and Q11 ON. The input state overides this reset action. In FVC applications, it is very important to make the input pulses narrower than the output pulse width T_p to assure proper resetting of the Q9-Q11 flip-flop.

The output pulse of the one-shot performs three functions during the timing interval:

1. The open-collector output transistor Q32 is switched into saturation. The output pulse at pin 3 is in the low state during the T_p timing interval.
2. A reference voltage V_R is switched ON at pin 2.
3. The output current source is gated ON. A current pulse of width T_p and amplitude V_R/R_S will come out of pin 1.

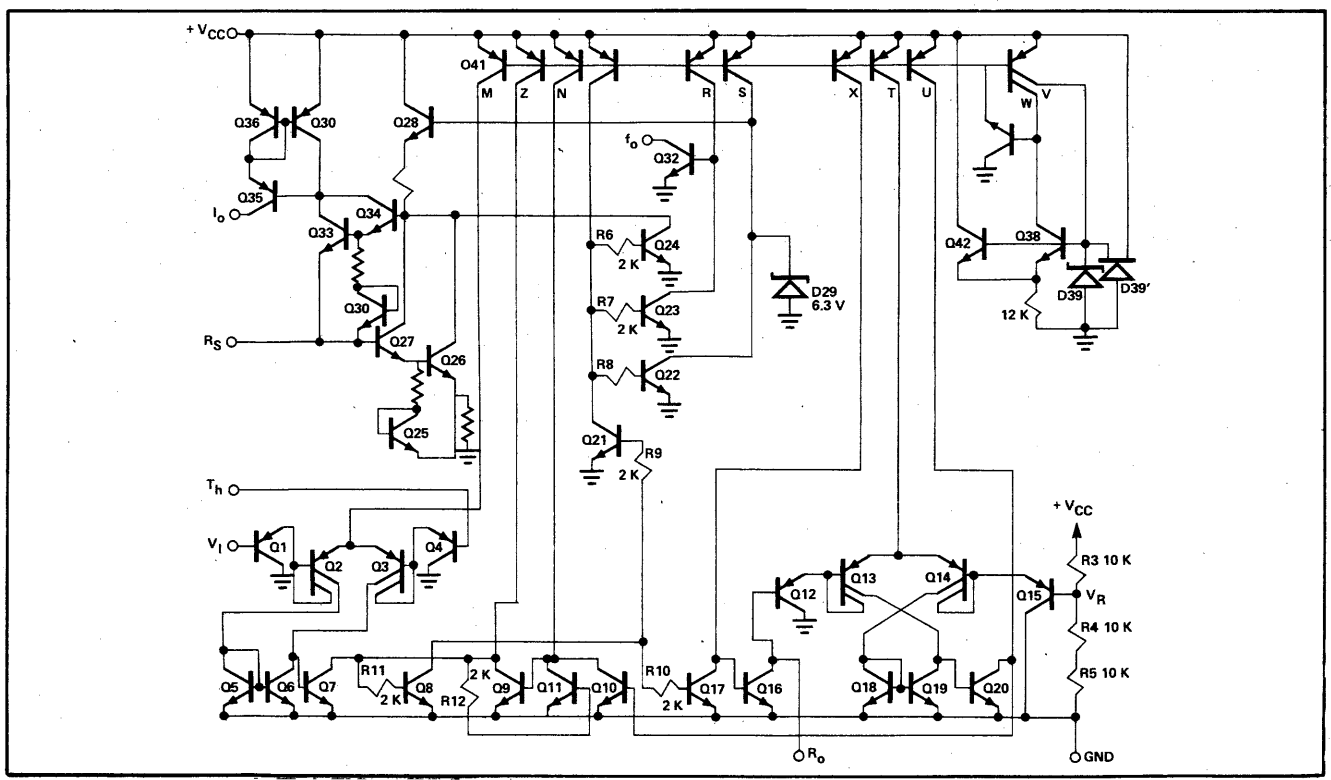


Figure 2. Raytheon 4152 Schematic Diagram

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ABSOLUTE MAXIMUM RATINGS

Supply Voltages	+7.0 to +22V
Output Sink Current	20mA
Internal Power Dissipation	500mW
Input Voltage	−0.2V to $+V_{CC}$
Output Short Circuit to Ground	Continuous

Storage Temperature Range	
RM4152	−65°C to +150°C
RV4152	−55°C to +125°C
RC4152	−55°C to +125°C
Operating Temperature Range	
RM4152	−55°C to +125°C
RV4152	−40°C to +85°C
RC4152	0°C to +70°C

ELECTRICAL SPECIFICATIONS

Typical performance at rated supply voltage and T_A = +25°C unless otherwise noted.

CIRCUIT CHARACTERISTICS

Input Comparator	
Input Offset Voltage @ 25°C	±10 mV max
vs. Temperature	±20 µV/°C
Input Offset Current	±100 nA max
Bias Current (Either Input)	-300 nA max
Input Voltage Range (Either Input)	0 to $+V_S$ - 3.0 Volts
Comparator Gain	10,000
One-Shot Pulse Circuit	
Pulse Width (See Fig. 4)	1.1 R_oC_o ± 5%
Threshold Voltage (Pin 5)	2/3 V_S (+10 V at V_S = 15 V)
Input Bias Current (Pin 5)	-500 nA
V_{sat} at Pin 5, I = 2.2 mA	0.15 V (0.5 V max)
Pulse Width Stability (T_p = 75 µs)	
vs. Temperature	±50 ppm/°C
vs. Supply	±100 ppm/V
Gated Current Source	
Output of Gated Current Source	$\frac{V_R}{R_S}$ ± 1%
vs. Temperature	±200 ppm/°C max
vs. Supply	±0.25%/V
Compliance (Change with Voltage)	0.25 µA/V max
Leakage in OFF State	10 nA (50 nA max)
Rise Time	100 nsec
Fall Time	100 nsec
Reference Voltage	
Voltage V_R (Pin 2)	2.2 ± 10%
Temperature Coefficient	±100 ppm/°C max
Logic Output (Pin 3)	
Output Sink Current, ON State	3.0 mA @ V_{sat} = 0.15 V
Output Leakage, OFF State	1 µA max
Power Supply	
Voltage, Rated Performance	+15 V
Quiescent Current Drain	+3.5 mA (6.0 mA max)

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DESCRIPTION

The RM4156/RC4156 is a monolithic integrated circuit, consisting of four independent high performance operational amplifiers constructed with the planar epitaxial process.

These amplifiers feature guaranteed A.C. performance which far exceeds that of the 741 type amplifiers. Also featured are excellent input characteristics and guaranteed low noise making this device the optimum choice for audio, active filter and instrumentation applications.

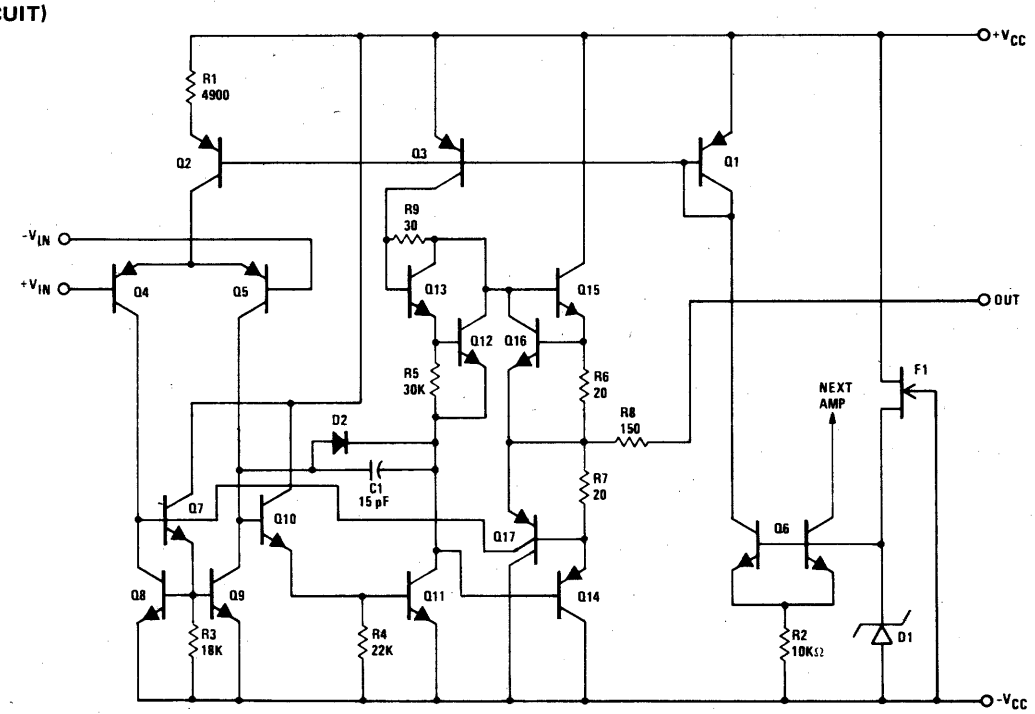
FEATURES

	Typical	Guaranteed
• Unity Gain Bandwidth	3.5 MHz	2.8 MHz
• High Slew Rate	1.6V/μS	1.3V/μS
• Low Noise Voltage	0.8μV	2.0μV

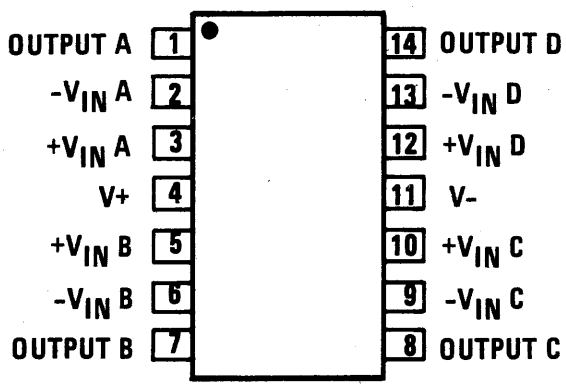
- Indefinite Short Circuit Protection
- No Crossover Distortion
- Low Input Offset and Bias Parameters
- Internal Compensation
- Pin-for-pin equivalent to LM324, LM348, HA4741

SCHEMATIC DIAGRAM

(1/4 CIRCUIT)



CONNECTION INFORMATION



Order Part Nos.
RM4156DC, RV4156DB, RV4156DC, RC4156DC, RC4156DB

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±20V
Internal Power Dissipation (Note 1) . . . . 880 mW
Differential Input Voltage . . . . . ±30V
Input Voltage (Note 2) . . . . . ±15V
Output Short Circuit Duration (Note 3) . . . Indefinite

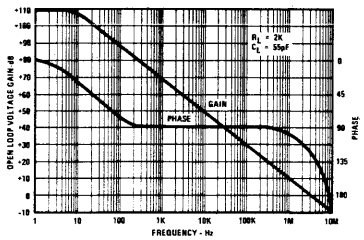
Storage Temperature Range . . . . . -65 to +150°C
Operating Temperature Range RM4156 -55 to +125°C
RV4156 -40 to +85°C
RC4156 0 to +70°C
Lead Soldering Temperature (60 sec) . . . . . 300°C

ELECTRICAL CHARACTERISTICS V_{CC} ±15V T_A +25°C unless otherwise specified

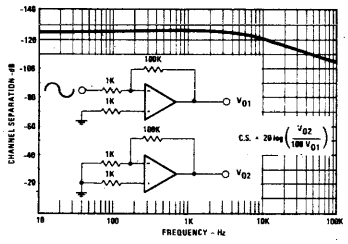
PARAMETER	CONDITIONS	RM4156			RV4156/RC4156			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10$ KΩ		0.5	3.0		1.0	5.0	mV
Input Offset Current			15	30		30	50	nA
Input Bias Current			60	200		60	300	nA
Input Resistance			0.5			0.5		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ KΩ V_{OUT} ±10V	50,000	100,000		25,000	100,000		V/V
Output Voltage Swing	$R_L \geq 10$ KΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ KΩ	±10	±13		±10	±13		V
Input Voltage Range		±12	±14		±12	±14		V
Output Resistance			230			230		Ω
Output Short Circuit Current			25			25		mA
Common Mode Rejection Ratio	$R_S \leq 10$ KΩ	80			80			dB
Power Supply Rejection Ratio	$R_S \leq 10$ KΩ	80			80			dB
Supply Current (all amplifiers)	$R_L = \infty$		4.5	5.0		5.0	7.0	mA
Transient Response								
Rise Time			50			75		ns
Overshoot			25%			25%		%
Slew Rate		1.3	1.6		1.3	1.6		V/μs
Unity Gain Bandwidth		2.8	3.5		2.8	3.5		MHz
Phase Margin	R_L = 2 KΩ R_C = 50 pF		50			50		degrees
Full Power Bandwidth	V_O = 20V p-p	20	25		20	25		kHz
Input Noise Voltage	f = 20 Hz to 20 kHz		0.8	2.0		0.8	2.0	μV RMS
Input Noise Current	f = 20 Hz to 20 kHz		15			15		pA RMS
Channel Separation			108			108		dB
The following specifications apply for -55°C ≤ T_A ≤ +125°C for RM4156, -40°C ≤ T_A ≤ +85°C for RV4156, 0°C ≤ T_A ≤ +70°C for RC4156.								
Input Offset Voltage	$R_S \leq 10$ KΩ			5.0			6.5	mV
Input Offset Current				75			100	nA
Input Bias Current				325			400	nA
Large Signal Voltage Gain	$R_L \geq 2$ KΩ V_{OUT} ±10V	25,000			15,000			V/V
Output Voltage Swing	$R_L \geq 2$ KΩ	±10			±10			V
Supply Current			10			10		mA
Average Offset Voltage Drift			5			5		μV/°C

Notes: 1. Rating applies for case temperature of +25°C maximum; derate linearity at 6.4 mW/°C for temperatures above +25°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit to ground on one amplifier only.

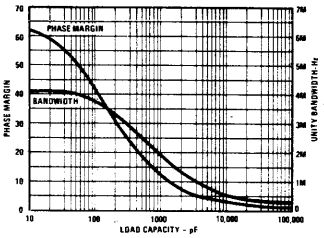
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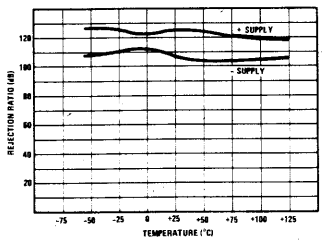
Open Loop Frequency Response



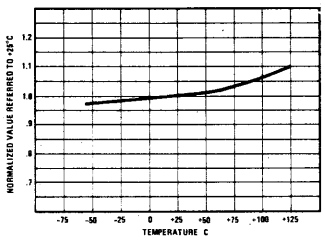
Channel Separation vs. Frequency



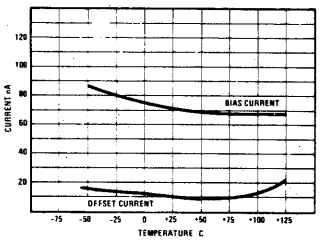
Small Signal Bandwidth and Phase Margin vs. Load Capacitance



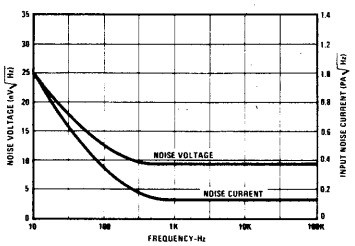
Power Supply Rejection Ratio vs. Temperature



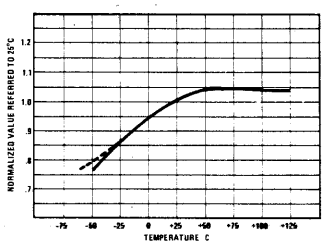
Transient Response vs. Temperature



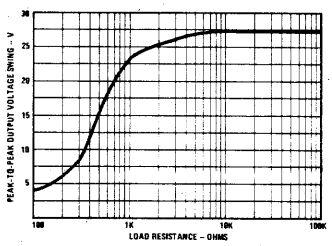
Input Currents vs. Temperature



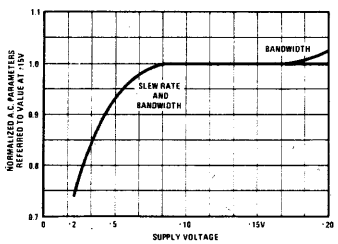
Input Noise vs. Frequency



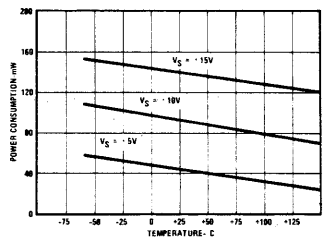
Normalized AC Parameters vs. Temperature



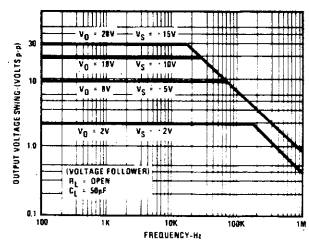
Output Voltage Swing vs. Load Resistance



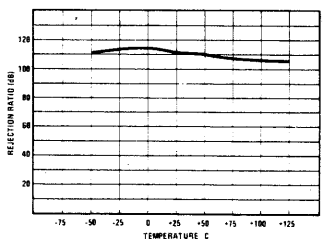
Slew Rate vs. Supply Voltage



Power Consumption vs. Temperature



Output Voltage Swing vs. Frequency



Common Mode Rejection Ratio vs. Temperature

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GENERAL DESCRIPTION

The 4559 integrated circuit is a high performance operational amplifier internally compensated and constructed on a single silicon chip using the planar epitaxial process.

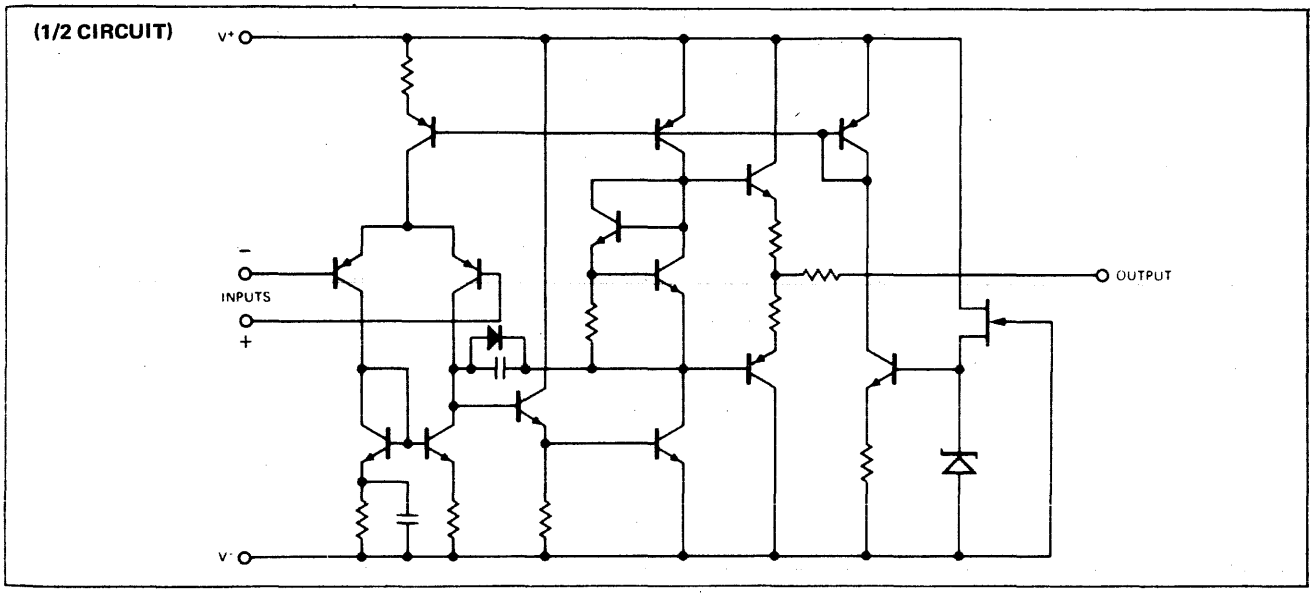
These amplifiers feature guaranteed AC performance which far exceeds that of the 741 type amplifiers. The specially designed low noise input transistors allow the 4559 to be used in low noise signal processing applications such as audio pre amplifiers and signal conditioners.

FEATURES

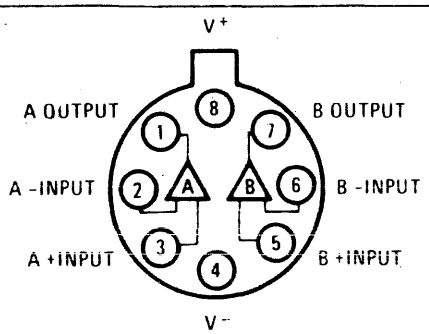
	Typical	Guaranteed
• Unity Gain Bandwidth	4.0 MHz	3.0 MHz
• Slew Rate	2.0 V/μsec	1.5 V/μsec

- Supply Voltage ±22V for RM4559 and ±18V for RC4559
- Low Input Noise Voltage 1.4 μV_{RMS} Typical
- No Frequency Compensation Required
- No Latch Up
- Large Common Mode and Differential Voltage Ranges
- Low Power Consumption
- Parametric Tracking Over Temperature Range
- Gain and Phase Match Between Amplifiers
- Pin-for-pin equivalent to 1458 and 4558

SCHEMATIC DIAGRAM

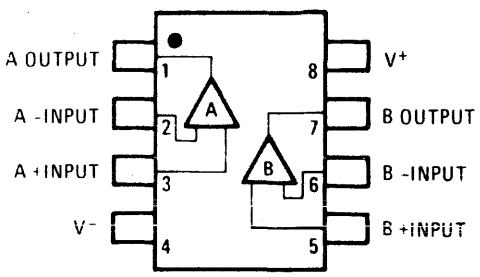


CONNECTION INFORMATION



TE Metal Can Package
(Top View)

Order Part Nos.:
RC4559T, RM4559T



NB Dual In-line Plastic Package
(Top View)

Order Part Nos.:
RC4559NB, RV4559NB
RC4559DE, RV4559DE
RM4559DE

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . RM4559: ±22V
RC4559: ±18V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage . . . . . ±30V
Input Voltage (Note 2) . . . . . ±15V
Storage Temperature Range . . . . . −65°C to +150°C

Operating Temperature Range
RM4559 . . . . . −55°C to +125°C
RV4559 . . . . . −40°C to +85°C
RC4559 . . . . . 0°C to +70°C
Lead Temperature (Soldering, 60 sec) . . . . . 300°C
Output Short-Circuit Duration (Note 3) . . . . . Indefinite

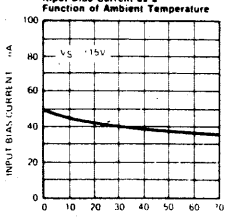
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = ±15 V unless otherwise specified.)

		RM4559			RV/RC4559			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			5	200		5	200	nA
Input Bias Current			40	500		40	500	nA
Input Resistance		0.3	1.0		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$ $V_{out} = \pm 10V$	50,000	300,000		20,000	300,000		V/V
Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	100		70	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		10	150		10	150	μV/V
Power Consumption			100	170		100	170	mW
Transient Response (unity gain) Rise Time Overshoot	V_{IN} = 20mV R_L = 2kΩ $C_L \leq$ 100pf		 80 18			 80 18		 nsec %
Slew Rate (unity gain)		1.5	2.0		1.5	2.0		V/μs
Unity Gain Bandwidth		3.0	4.0		3.0	4.0		MHz
Full Power Bandwidth	$V_O = 20\ V_{p-p}$	24	32		24	32		kHz
Input Noise Voltage	f = 20 Hz to 20 kHz		1.4			1.4		μV_{RMS}
Input Noise Current	f = 20 Hz to 20 kHz		25			25		pA RMS
Channel Separation	Gain = 100		90			90		dB
	f = 10 kHz R_S = 1kΩ							
The following specifications apply for −55°C ≤ T_A ≤ +125°C for RM4558; 0°C ≤ T_A ≤ +70°C for RC4558								
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1500			800/1500*	nA
Large-Signal Voltage Gain	$R_L \geq 2k\Omega$ $V_{out} = \pm 10V$	25,000			15,000			
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			±10			V
Power Consumption	V_S = ±15V T_A = +125°C T_A = −55°C		90 120	150 200		90 120	150 200	mW

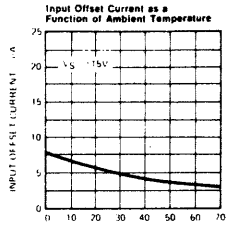
*RV4559

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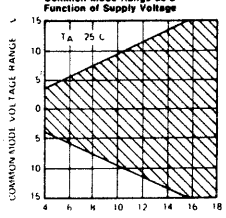
Input Bias Current as a Function of Ambient Temperature



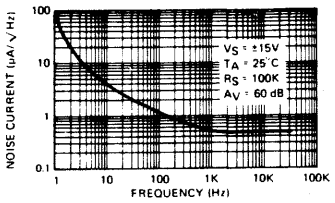
Input Offset Current as a Function of Ambient Temperature



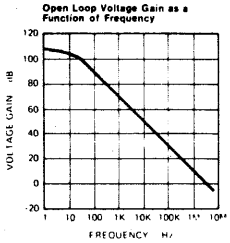
Common Mode Range as a Function of Supply Voltage



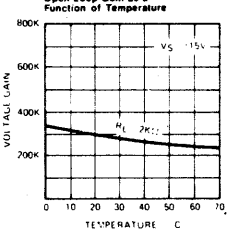
Input Noise Current as a Function of Frequency



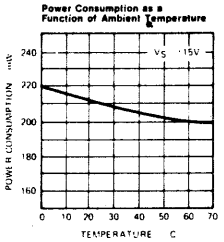
Open Loop Voltage Gain as a Function of Frequency



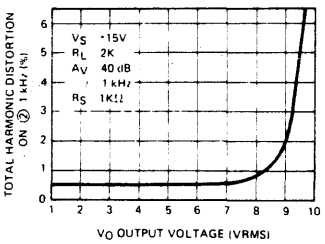
Open Loop Gain as a Function of Temperature



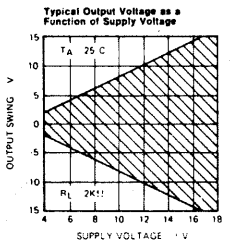
Power Consumption as a Function of Ambient Temperature



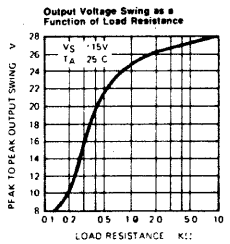
Total Harmonic Distortion vs Output Voltage



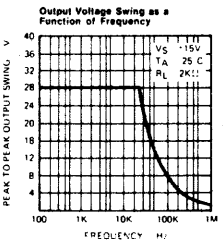
Typical Output Voltage as a Function of Supply Voltage



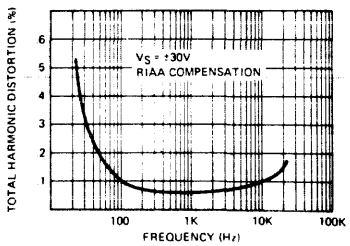
Output Voltage Swing as a Function of Load Resistance



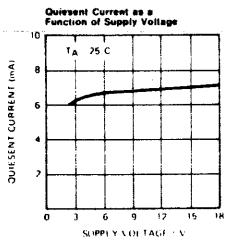
Output Voltage Swing as a Function of Frequency



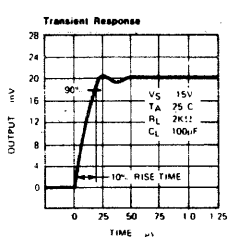
Distortion vs Frequency
VO = 1vrms



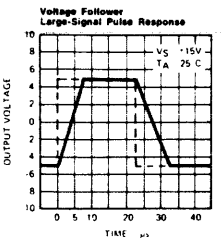
Quiescent Current as a Function of Supply Voltage



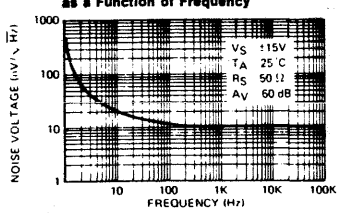
Transient Response



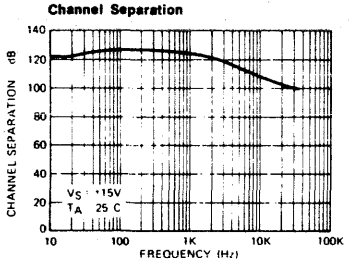
Voltage Follower Large-Signal Pulse Response



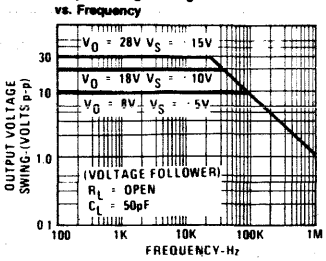
Input Noise Voltage as a Function of Frequency



Channel Separation



Output Voltage Swing vs. Frequency



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DF320
DF321
DF322

CMOS LOOP DISCONNECT DIALER CIRCUITS

D SUFFIX: –40 to +85°C
OPERATING TEMPERATURE RANGE

Description

The DF320 series of monolithic CMOS Loop Disconnect Diallers each contain all the logic necessary to interface a standard double contact keyboard to a telephone system requiring loop disconnect signalling.

A dial pulsing output and two masking output options are provided to control the impulsing (loop disconnect) and muting functions. The circuit is capable of storing a number string of up to 20 digits and re-dialling this stored number automatically at a later time, initiated by a RE-DIAL input code. Impulsing mark/space ratio (M/S), impulsing rate and interdigital pause (IDP) are all pin programmable to meet most telephone authority specifications.

The use of Siliconix low voltage CMOS technology allows operation with an unregulated supply voltage down to a guaranteed minimum of 2.5 V. This feature, together with low operating current, negligible standby current and high noise immunity make the DF320 series easy to interface from long telephone lines.

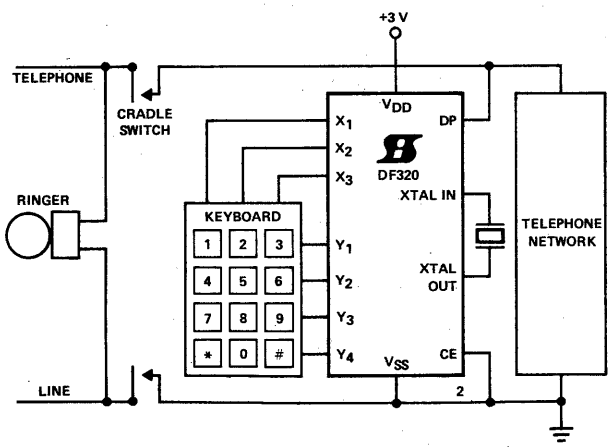
External component count is minimized by the inclusion of an on-chip clock oscillator, high impedance pull-down terminations to programming inputs as well as pull-up terminations to the keyboard giving direct interfacing.

The Loop Disconnect Dialler is available in three pinout options. The DF320 provides the functions most commonly required in the push button telephone application. M1 is the masking option which remains at logic "1" throughout the dialling sequence. The DF322 is identical to the DF320 except that M2 is offered instead of M1. The M2 masking option is at logic "1" only during impulsing, allowing the telephone line to be monitored during the IDP. The DF321 is a multioption version which offers both M1 and M2 together with FD, IDP and SYS CK. All versions are based on the same integrated circuit.

Features

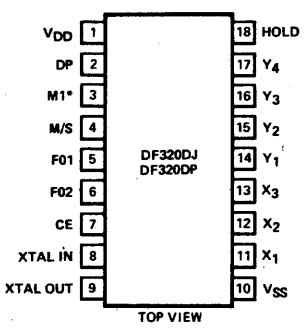
- **Operation from 2.5 V to 5.5 V V_{DD} Supply (May Be Unregulated)**
- **Low Standby Dissipation–3 μW Typ @ 3 V Supply**
- **Low Dynamic Dissipation–540 μW Typ @ 3 V Supply**
- **On-Chip Oscillator Uses Low Cost 3.579545 MHz Crystal**
- **Power ON Reset**
- **On-Chip Pull-Up and Pull-Down Terminations to Inputs**
- **High Input Noise Immunity: Typ 45% of Supply Voltage**
- **Key Input Debounce Circuitry**
- **Fully Static Storage Up to 20 Decimal Digits**
- **Repeat of Last Number**
- **Selectable Impulsing Mark/Space Ratios of 2:1 or 3:2**
- **Selectable Impulsing Speeds of 10, 16, 20 and 932 Hz**
- **Selectable Interdigital Pause: 8 or 4 Times Impulsing Period**

APPLICATION



PIN CONFIGURATIONS

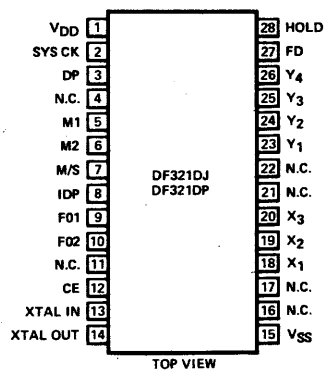
Dual In-Line Package



*M2 ON DF322DJ, DF322DP

ORDER NUMBERS:
DF320DJ, DF320DP, DF322DJ, DF322DP

Dual In-Line Package



ORDER NUMBERS:
DF321DJ, DF321DP

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OPERATING TEMPERATURE RANGE:
C SUFFIX 0 to +70°C

CMOS TELECOMMUNICATIONS A-LAW COMPANDER SET

Description

The DF341 (coder) is an analog-to-digital converter which has a transfer characteristic conforming to the telecommunication industry CCITT A-law. Its counterpart, the DF342 (decoder) is a digital-to-analog converter which also conforms to the A-law.

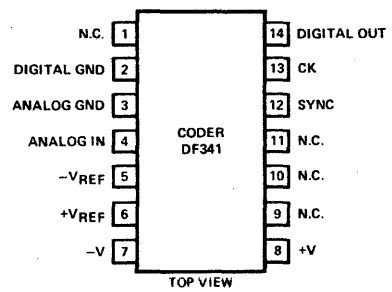
Together these parts form a codec (coder-decoder set) which is designed to meet the needs of the telecommunications industry for per channel voice frequency codecs used in PCM Channel Bank and PBX systems. Digital output and input of the coder and decoder is in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 2.048 megabit/sec rate with analog signal sampling occurring at an 8 kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line.

Features

- **Low Power Dissipation**
- **Follows the CCITT A-Law for Companding**
- **Serial Data Output of 2.048 MHz at 8 kHz Sampling Rate**
- **Open Drain Digital Output Allows Easy Interface to TTL and CMOS Multiplexers**
- **Decoder Contains On-Board Sample and Hold Output**
- **Separate Analog and Digital Grounding Pins Reduce System Noise Problems**

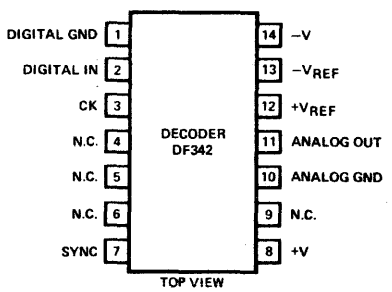
PIN CONFIGURATIONS

Dual In-Line Package



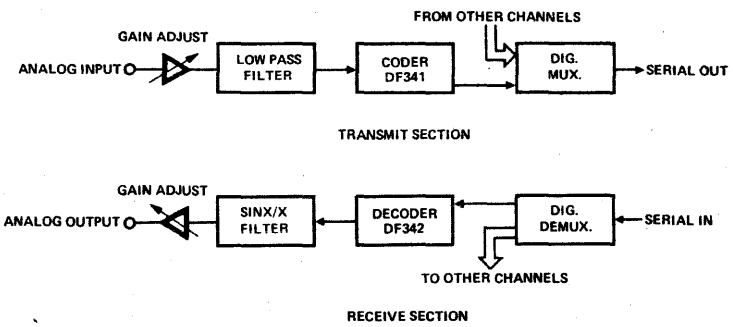
ORDER NUMBER: DF341CJ

Dual In-Line Package



ORDER NUMBER: DF342CJ

FUNCTIONAL BLOCK DIAGRAM



©IC MASTER 1978

OPERATING TEMPERATURE RANGE:
C SUFFIX 0 to +70°C

CMOS TELECOMMUNICATIONS μ-LAW COMPANDER SET

Description

The DF331 (coder) is an analog-to-digital converter which has a transfer characteristic conforming to the telecommunication industry μ-255 law. Its counterpart, the DF332 (decoder) is a digital-to-analog converter which also conforms to the μ-255 law.

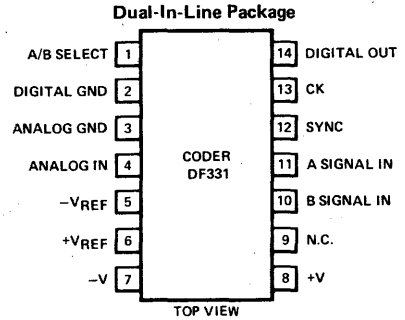
Together these parts form a codec (coder-decoder set) which is designed to meet the needs of the telecommunications industry for per channel voice frequency codecs used in PCM Channel Bank and PBX systems. Digital output and input of the coder and decoder is in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 1.544 megabit/sec rate with analog signal sampling occurring at an 8 kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line.

Features

- **Low Power Dissipation**
- **Follows the μ-255 Law for Companding**
- **Serial Data Output of 1.544 MHz at 8 kHz Sampling Rate**
- **Active Low Open Drain Digital Output Allows Easy Interface to TTL and CMOS Multiplexers**
- **Decoder Contains On-Board Sample and Hold Output**
- **Separate Analog and Digital Grounding Pins Reduce System Noise Problems**
- **Dual Channel Signalling**
- **Zero Code Suppression**

PIN CONFIGURATIONS

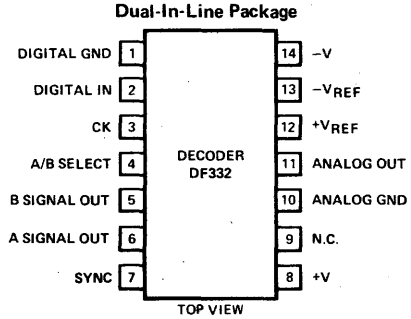
Dual-In-Line Package



TOP VIEW

ORDER NUMBER: DF331CJ

Dual-In-Line Package

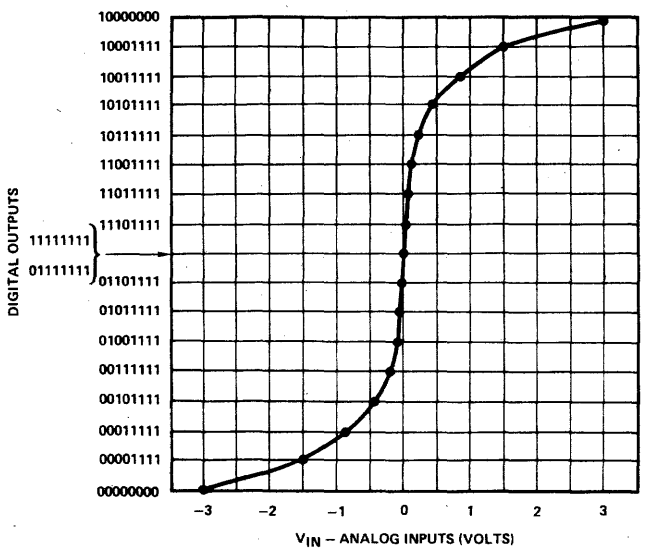


TOP VIEW

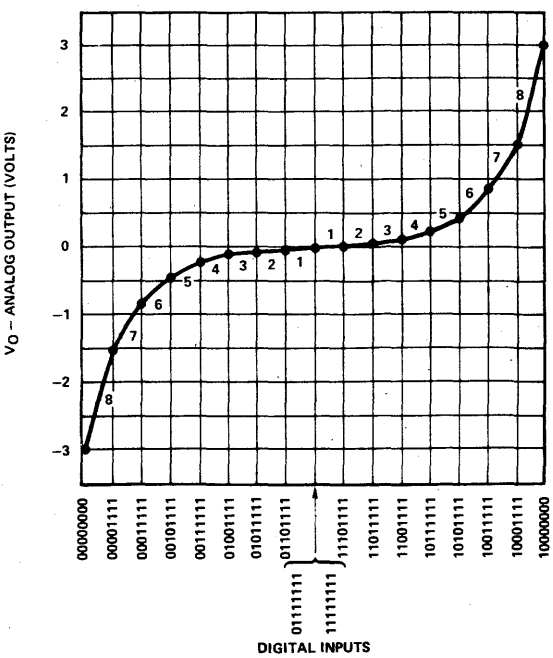
ORDER NUMBER: DF332CJ

TYPICAL CHARACTERISTICS

DF331 μ-Law Coder Transfer Characteristic



DF332 μ-Law Decoder Transfer Characteristic



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FUNCTIONAL DESCRIPTION

Positive and Negative Reference Voltages: Analog input voltages must be between the positive and negative reference voltages for accurate coding.

Analog Input: Voice frequency analog signals which are bandwidth limited to below 4 kHz are inputted at this pin. These analog signals are then sampled at an 8 kHz rate for approximately 31 μsec.

Fast Clock: A fast clock input is provided on the DF331 and DF332. This clock is used for the high speed data transmission needed in PCM Channel Bank and PBX systems, and is internally divided to provide timing and control. The on-chip 8 bit output shift register of the coder is unloaded at this fast clock rate while the input register of the decoder is loaded at this rate. A 1.544 MHz rate is standard for use in 24 channel PCM systems. A 32-channel system would require a 2.048 MHz clock. Both parts will operate at this higher clock rate.

Sync: In order to synchronize many channels into one data stream, a method of controlling the dumping and loading of the output and input shift registers of the individual coders and decoders is necessary. This is accomplished through the use of an externally generated sync pulse presented to the sync input pin. This pulse occurs at an 8 kHz rate and is synchronized to the fast clock. Its duration is 8 fast clock cycles.

Upon receiving a sync pulse the coder will dump the contents of the output shift register at the fast clock rate. The decoder upon reception of the sync will load its input register at the fast clock rate.

Digital Output: The coder output register stores the 8 bit encoded sample of the analog input. This 8 bit word is shifted out of the coder via an open drain output device in serial format. Open drain output allows easy interfacing to CMOS and TTL multiplexers.

Digital Input: The digital input of the decoder accepts an 8 bit word into the input shift register upon the decoder's reception of a sync pulse.

Analog Output: The analog output of the decoder is in the form of voltage pulses having a duration of 8 fast clock cycles and amplitude equal to the analog sample which was encoded. These pulses are then filtered with an active low pass filter to recreate the actual sampled voice signal.

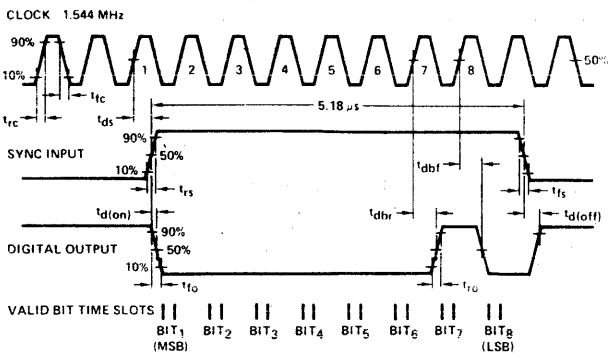
Signal Bit Inputs A and B: Two signaling bit inputs A and B are provided on the DF331 allowing insertion of signaling information into the transmitted data stream. This information occurs as the 8th bit in the transmitted word. A positive transition occuring on the A/B select input selects the A signaling input while a negative transition selects the B signaling input. Information presented to these inputs is inverted upon transmission. See Figure 4.

Signaling Bit Outputs A and B: Two outputs on the DF332 are provided to output received signaling information. A transition occuring on the A/B select determines whether the received signaling information is routed to the A or B output. The signaling information is present at the outputs immediately after reception.

A/B Select Input: The A/B Select Input is provided on both the DF331 and DF332 in order to select the A or B paths for the signaling information. It is a transition sensitive input. A positive transition will select path A and a negative transition will select path B. See Figure 4.

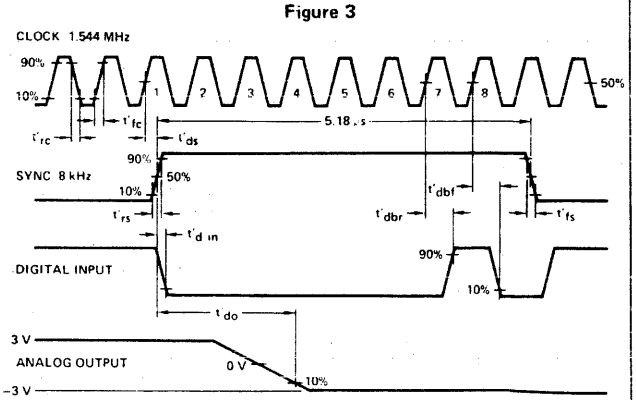
Zero Code Suppression: Should an all zeroes code result from the A to D Conversion of the sampled input (and the insertion of the signalling bit, if appropriate) bit 7 is forced to a one.

DF331 Coder Waveforms
Figure 2



Parameter		Test Condition	Min	Max	Unit
t_{rc}	Clock Rise Time	50		100	ns
t_{fc}	Clock Fall Time	50		80	
t_{rs}	Sync Rise Time	50		100	
t_{fs}	Sync Fall Time	50		100	
t_{ws}	Sync Pulse Width	5.18	8/F_{CLOCK}		μs
t_{ps}	Sync Pulse Period	125			

DF332 Decoder Waveforms
Figure 3



Parameter		Test Condition	Min	Max	Unit
t'_{rc}	Clock Rise Time	50		100	ns
t'_{fc}	Clock Fall Time	50		80	
t'_{rs}	Sync Rise Time	50		100	
t'_{fs}	Sync Fall Time	50		100	
t'_{ws}	Sync Pulse Width	5.18	8/F_{CLOCK}		μs
t'_{ps}	Sync Pulse Period	125			

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DF213 DF214

OPERATING TEMPERATURE RANGE:
C SUFFIX 0 to +70°C

DIGITAL STOPWATCH

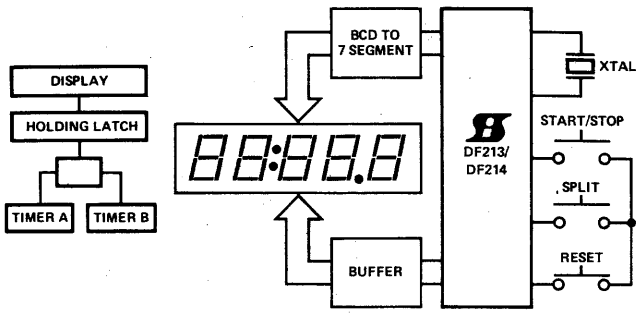
Description

The DF213 and DF214 are P-Channel MOS devices containing all the necessary logic to implement several configurations of a digital stopwatch. A 3.2768 MHz crystal oscillator provides an extremely accurate time reference. Each device contains two timers that operate independently.

The holding latch is updated continuously from timer A or timer B or it can "freeze" the display time at a touch of a button. This configuration allows versatile event timing with "split" capability normally requiring skilled manipulation of two stopwatches. The DF213 times in minutes, seconds, and hundredths of a second providing up to six digits of display. The DF214 times in minutes and thousandths of a minute providing five digits of display.

Applications

- **Sports Timing – Auto Racing, Track, Swimming, Rodeo, Sailing, Football, Soccer**
- **Industrial Timing – Testing, Time-Motion Studies, Process Timing**
- **Scientific Timing – Chemical Reaction Timing, Mechanical Stress Timing, Animal Behavior Studies**



DF215

OPERATING TEMPERATURE RANGE:
C SUFFIX 0 to +70°C

DUAL SET POINT TIMER/COUNTER

Description

The DF215 is a P-channel, depletion load MOS device containing all the necessary logic to implement a single or dual set point timer or counter. The device typically uses one or two thumbwheel switch banks to provide two sequential, fully selectable, accurate intervals for equipment control. Figure 1 shows the control output response. The DF215 either counts events or time intervals using a 50 Hz or 60 Hz power line time base. Multiplexed outputs provide the total elapsed time (or number of events) from start for display.

Applications

- **Industrial Process Control**
- **Commercial Food Preparation Control**
- **Automatic Feed, Fluid, or Material Dispensing**
- **Step and Repeat Control**
- **Test Timing**
- **Sporting Event Timing**

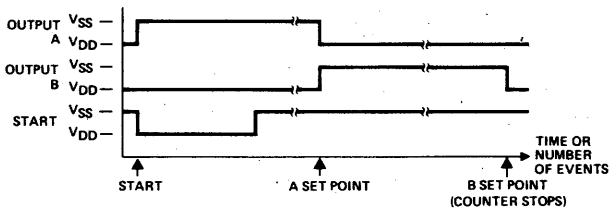
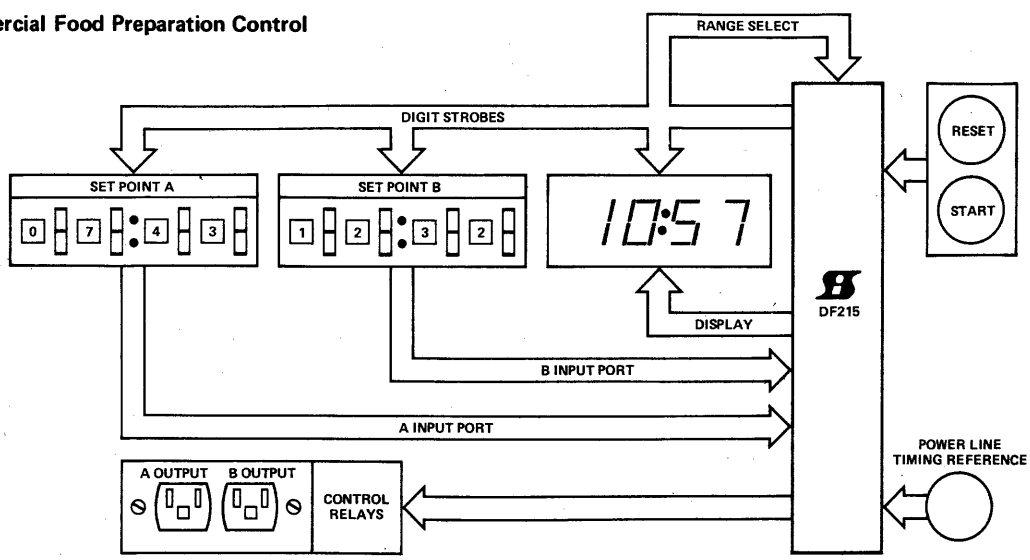


Figure 1



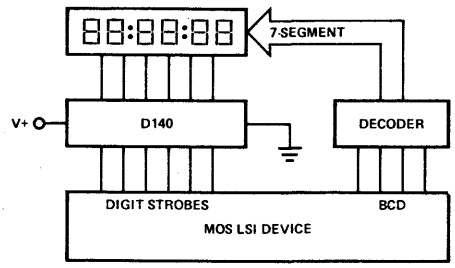
D140

OPERATING TEMPERATURE RANGE:
C SUFFIX 0 to +70°C

HEX DIGIT DRIVER

Description

The D140 is a Hex Driver intended as a digit driver for common cathode LED displays. The D140 has the advantage over other driver types of very low voltage operation and high current gain. The D140 is well suited to driving loads on the order of 100 mA from low current CMOS devices. Fast switching speeds (250 ns) and low input bias currents (80 μA) make the D140 well suited to applications such as clock drivers and hand-held instruments.

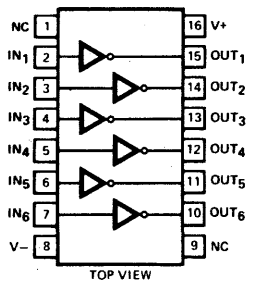


Applications

- Relay Drivers
- Common Cathode Digit Drivers
- Common Anode Segment Drivers
- CMOS to TTL Level Translators

PIN CONFIGURATION

Dual-In-Line Package



ORDER NUMBER: D140CJ

OPERATING TEMPERATURE RANGE:
A SUFFIX –55 to +125°C
B SUFFIX –20 to +85°C
C SUFFIX 0 to +70°C

L144

MICROPOWER TRIPLE OPERATIONAL AMPLIFIER

Description

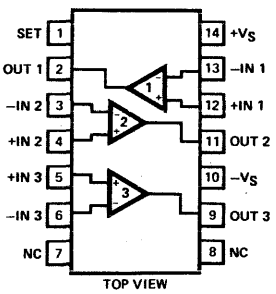
The L144 is a monolithic low-power triple operational amplifier stabilized for all feedback configurations and capacitive loads by internal gain compensation. Low power requirements permit high voltage operation across the rated temperature range, as well as battery operation from ±1.5 V.

Features

- External Control of Supply Current and Output Drive
- Operation With ±1.5 V to ±15 V Power Supplies
- 80 dB Gain With 20K Ω Load
- ±30 V Differential Input Voltage Range
- Drives Large Capacitive Loads (> 1000 pF)
- Internally-Compensated
- Continuous Short-Circuit Protection
- Monolithic Construction
- Slew Rate 0.4 V/μs Typical

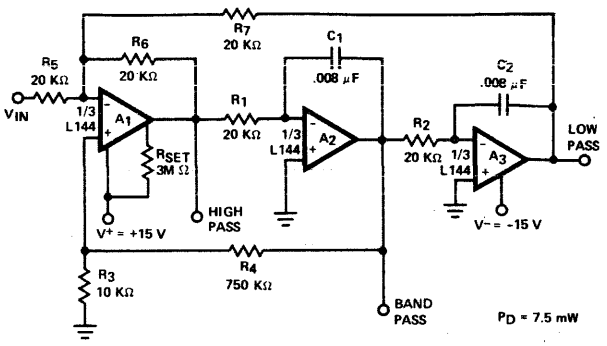
PIN CONFIGURATION

Dual-In-Line Package



ORDER NUMBERS:
L144AP, L144BP
or L144CJ

Active Filter



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Siliconix incorporated

OPERATING TEMPERATURE RANGE:
C SUFFIX 0 to +70°C

MICROPOWER COMPARATOR, DETECTOR ALARM CIRCUIT

MONOLITHIC INTEGRATED CIRCUIT FOR DETECTOR AND ALARM SYSTEMS

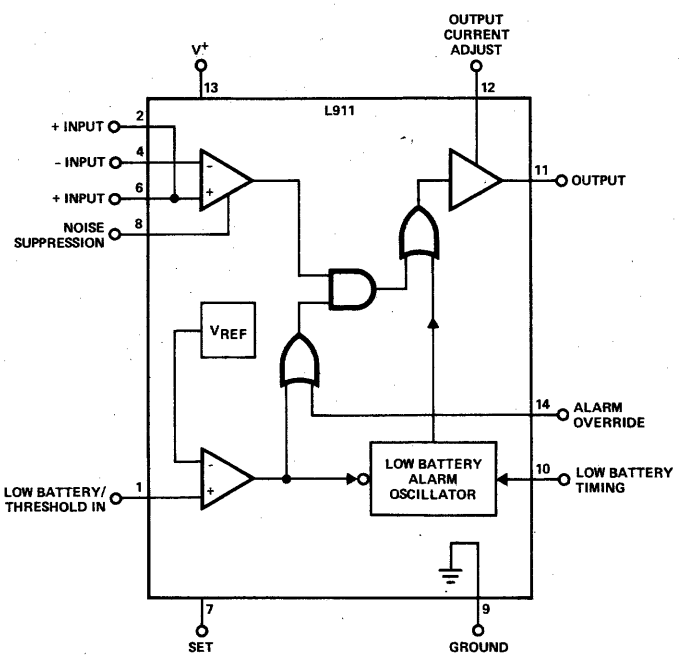
Description

The L911 is a monolithic bipolar-PMOS integrated circuit intended to meet the system requirements of a micropower detector alarm or ON/OFF control system. The circuit will operate from a supply as low as 6V and is tested for 15V conditions. The alarm output can source sufficient current to activate an NPN or SCR buzzer alarm driver and can also interface to TTL or CMOS logic. The L911 can easily operate with a standby supply current of less than 10 μA from a 9 V battery, and less than 17 μA at 15 V. The high input impedance MOSFET comparator easily interfaces to high impedance sensor devices.

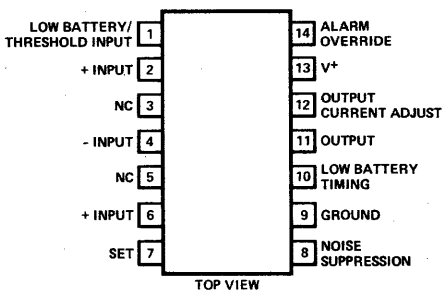
Features

- **High Input Impedance MOS FET Comparator**
- **Low Standby Current Drain (< 10 μA) Allows Greater than 1 Year Battery Life**
- **Operation from a 6 V to 15 V Power Source**
- **Includes Low Battery/Threshold Voltage Detection Circuitry**
- **Built-In Reverse Battery Protection**
- **Outputs to SCR or NPN for Driving Buzzer Alarm**
- **TTL or CMOS Logic Compatible Output**
- **Low Input Bias Current (I_{IN} < 10 nA)**
- **Wide Common Mode Input Range**
- **Output Sourcing Current Adjustable Up to 30 mA**
- **Adjustable Timing of "Trouble Signal" Pulses**
- **Allowance for Input Noise Suppression**
- **Can be Used in a Latching or Non-Latching System**

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



ORDER NUMBER: L911CJ

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OPERATING TEMPERATURE RANGE:
A SUFFIX –55 to +125°C
B SUFFIX –20 to +85°C
C SUFFIX 0 to +70°C

MICROPOWER QUAD COMPARATOR

Description

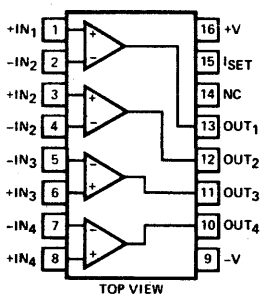
The L161 is a monolithic quad micropower comparator circuit, with an external control for varying supply current, input bias current and output current drive. This is accomplished by a single resistor connected to V+ which controls the bias current to Q_{10} which via a series of current mirrors supplies bias to the differential amplifier. The L161 finds applications in areas where low powered battery operation and CMOS compatibility are required. The ability to control comparator characteristics makes this a very versatile device.

Features

- **Power Dissipation as Low as 15 μW**
- **External Control of Supply Current and Output Drive**
- **Operation with ±1.5 V to ±18 V Power Supplies**
- **Single Supply Operation**
- **Gain Greater than 20K**
- **Sensing Near Ground**
- **±36V Differential Input Voltage Range**
- **Slew Rate 3 V/μs Typical**
- **CMOS Logic Compatible**
- **Operation in Low and High Power Modes**

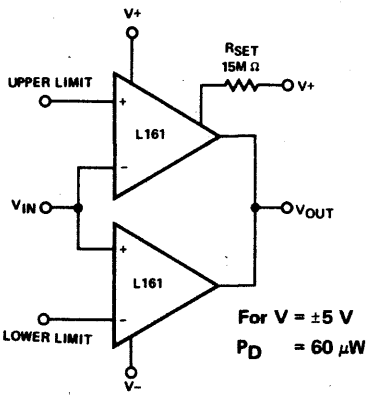
PIN CONFIGURATION

Dual-In-Line Package



L161AP, L161BP OR L161CJ

Zero Crossing Detector



For V = ±5 V
P_D = 60 μW

LM3909

MICROPOWER LED FLASHER

OPERATING TEMPERATURE RANGE:
–25° to +70°C

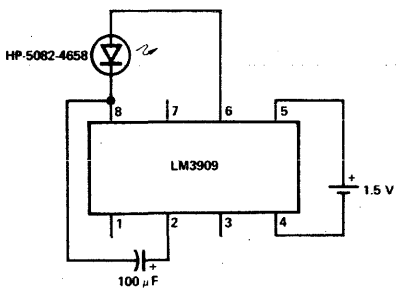
Description

The LM3909 is a monolithic oscillator specifically designed to flash Light Emitting Diodes. By using the timing capacitor for voltage boost, it delivers pulses of 2 or more volts to the LED while operating on a supply of 1.5 V or less. The circuit is inherently self-starting, and requires the addition of only a battery and capacitor to function as an LED flasher.

Features

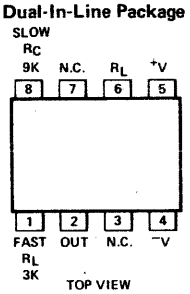
- **Operation Over One Year From One C Size Flashlight Cell**
- **Bright, High Current LED Pulse**
- **Minimum External Parts**
- **Low Cost**
- **Low Voltage Operation, From 1.15 V to 6 V**

Minimum Power at 1.5V



PIN CONFIGURATION

Dual-In-Line Package



ORDER NUMBER LM3909N

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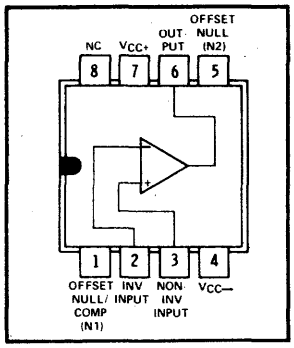
TYPES TL061, TL061A, TL061B, TL062, TL062A, TL062B, TL064, TL064A, TL064B, TL066, TL066A, TL066B LOW-POWER JFET-INPUT OPERATIONAL AMPLIFIERS

SEPTEMBER 1977

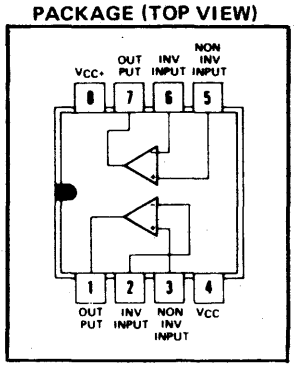
24 DEVICES COVER COMMERCIAL, INDUSTRIAL, AND MILITARY TEMPERATURE RANGES

- Very Low Power Consumption
- Typical Supply Current . . . 150 μA
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate . . . 3.5 V/μs Typ

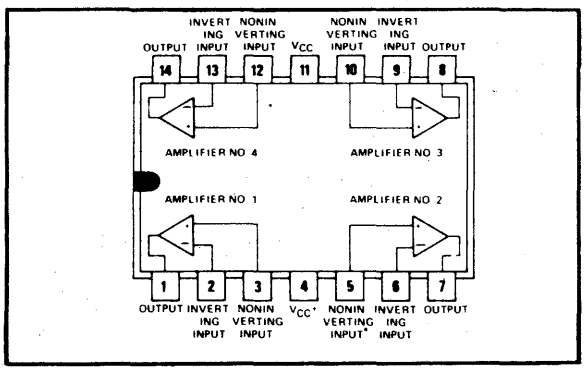
TL061, TL061A, TL061B JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)



TL062, TL062A, TL062B JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)



TL064, TL064A, TL064B J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

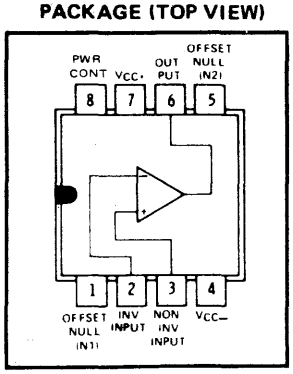


description

The JFET-input operational amplifiers of the TL061 series are designed as low-power versions of the TL081 series amplifiers. They feature high input impedance, wide bandwidth, high slew rate, and low input offset and bias currents. The TL061 series feature the same terminal assignments as the TL071 and TL081 series, except the TL066 has an additional power control function (pin 8) that allows the user to control the power dissipation of the circuit. This is achieved by connecting a resistor between the power-control terminal and V_{CC-}. For normal operation, the power-control terminal is connected directly to V_{CC-}.

Device types with an "M" suffix are characterized for operation over the full military temperature range of –55°C to 125°C, those with an "I" suffix are characterized for operation from –25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

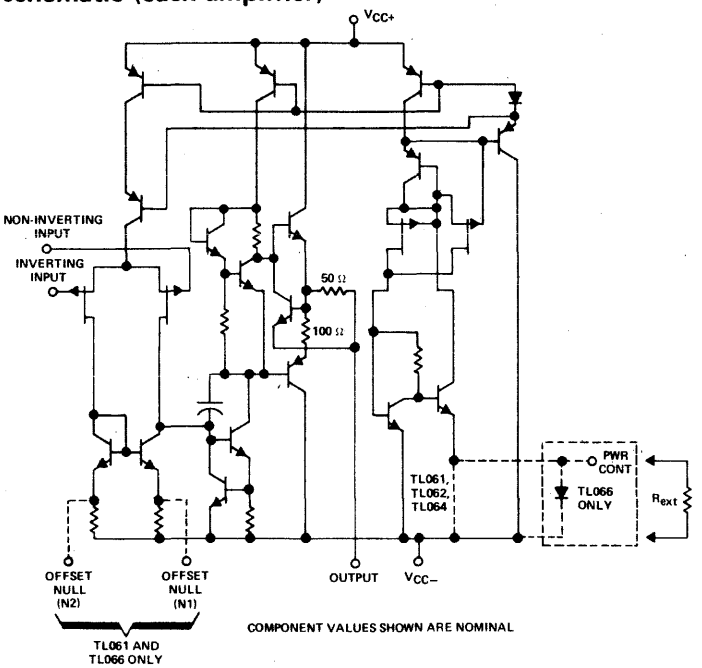
TL066, TL066A, TL066B JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

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schematic (each amplifier)



DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J	680 mW	8.2 mW/°C	67°C
JG	680 mW	6.6 mW/°C	47°C
N	680 mW	9.2 mW/°C	76°C
P	680 mW	8.0 mW/°C	65°C

For TL066 only

$$I_{CC} \approx \frac{2.85}{2.85 + R_{ext}} \cdot I_{CC(0)}$$

where R_{ext} is in kΩ
and $I_{CC(0)} = I_{CC}$ with $R_{ext} = 0$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL06_M TL06_AM	TL06_I	TL06_C TL06_AC TL06_BC	UNIT
Supply voltage, V_{CC} + (see Note 1)		18	18	18	V
Supply voltage, V_{CC} – (see Note 1)		–18	–18	–18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Voltage at power-control terminal of TL066 with respect to V_{CC-}		0.5	0.5	0.5	V
Duration of output short circuit (see Note 4)		Unlimited	Unlimited	Unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)		680	680	680	mW
Operating free-air temperature range		–55 to 125	–25 to 85	0 to 70	°C
Storage temperature range		–65 to 150	–65 to 150	–65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J or JG Package	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C, free-air temperature, refer to Dissipation Derating Table.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 10 kΩ, A_{VD} = 1		3.5		V/μs
t_r	Rise time	V_I = 20 mV, C_L = 100 pF,	R_L = 10 kΩ, A_{VD} = 1		0.15		μs
	Overshoot factor				10%		

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electrical characteristics, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS†		TL06_M TL06_AM			TL06_ I			TL06_C TL06_AC TL06_BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω, T_A = 25°C	'61, '62, '64, '66		3	6		3	6		3	15	mV
			'61A, '62A, '64A, '66A		2	3					3	6	
			'61B, '62B, '64B, '66B								2	3	
		R_S = 50 Ω, T_A = full range	'61, '62, '64, '66			9			9			20	
			'61A, '62A, '64A, '66A			5						7.5	
			'61B, '62B, '64B, '66B									5	
α_{VIO}	Temperature coefficient of input offset voltage	R_S = 50 Ω,	T_A = full range		10			10			10		μV/°C
I_{IO}	Input offset current‡	T_A = 25°C	'61, '62, '64, '66		5	100		5	100		5	200	pA
			'61A, '62A, '64A, '66A		5	100					5	100	
			'61B, '62B, '64B, '66B								5	100	
		T_A = full range	'61, '62, '64, '66			20			10			5	nA
			'61A, '62A, '64A, '66A			20						3	
			'61B, '62B, '64B, '66B									3	
I_{IB}	Input bias current‡	T_A = 25°C	'61, '62, '64, '66		30	200		30	200		30	400	pA
			'61A, '62A, '64A, '66A		30	200					30	200	
			'61B, '62B, '64B, '66B								30	200	
		T_A = full range	'61, '62, '64, '66			50			20			10	nA
			'61A, '62A, '64A, '66A			50						7	
			'61B, '62B, '64B, '66B									7	
V_{ICR}	Common-mode input voltage range	T_A = 25°C	'61, '62, '64, '66	±12			±12			±10			V
			'61A, '62A, '64A, '66A	±12						±12			
			'61B, '62B, '64B, '66B							±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	T_A = 25°C,	R_L = 10 kΩ	20	26		20	26		20	26		V
		T_A = full range,	R_L ≥ 10 kΩ	20			20			20			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 10 kΩ, V_O = ±10 V, T_A = 25°C	'61, '62, '64, '66	4	10		4	10		3	10		V/mV
			'61A, '62A, '64A, '66A	4	10					4	10		
			'61B, '62B, '64B, '66B							4	10		
		R_L ≥ 10 kΩ, V_O = ±10 V, T_A = full range	'61, '62, '64, '66	4			4			3			
			'61A, '62A, '64A, '66A	4						4			
			'61B, '62B, '64B, '66B							4			
B_1	Unity-gain bandwidth	T_A = 25°C			1			1			1		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	R_S ≤ 10 kΩ, T_A = 25°C	'61, '62, '64, '66	80	86		80	86		70	76		dB
			'61A, '62A, '64A, '66A	80	86					80	86		
			'61B, '62B, '64B, '66B							80	86		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	R_S ≤ 10 kΩ, T_A = 25°C	'61, '62, '64, '66	80	95		80	95		70	95		dB
			'61A, '62A, '64A, '66A	80	95					80	95		
			'61B, '62B, '64B, '66B							80	95		
P_D	Total power dissipation (each amplifier)	No load, T_A = 25°C,	No signal, See Note 6		4.5	6		4.5	6		4.5	7.5	mW
I_{CC}	Supply current (per amplifier)	No load, T_A = 25°C	No signal, See Note 6		150	200		150	200		150	250	μA
V_{o1}/V_{o2}	Channel separation	A_{VD} = 100,	T_A = 25°C		120			120			120		dB

† All characteristics are specified under open-loop conditions unless otherwise noted. Full range for T_A is −55°C to 125°C for TL06_M and TL06_AM; −25°C to 85°C for TL06_I; and 0°C to 70°C for TL06_C, TL06_AC, and TL06_BC.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

NOTE 6: For the TL066 supply current is measured with the power-control terminal (pin 8) connected to V_{CC-}.

TYPES TL071, TL071A, TL071B, TL072, TL072A, TL072B, TL074, TL074A, TL074B, TL075, TL075A, TL075B
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

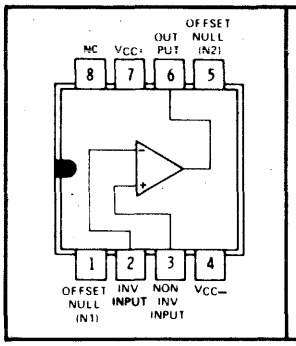
JULY 1977

24 DEVICES COVER COMMERCIAL, INDUSTRIAL, AND MILITARY TEMPERATURE RANGES

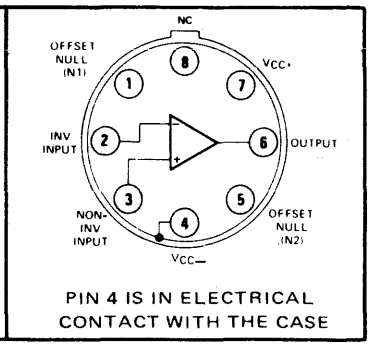
- Low Noise . . . V_n = 18 nV/$\sqrt{Hz}$ Typ
- Low Harmonic Distortion . . . 0.01% Typ
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation
- Low Power Consumption
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/μs Typ

TL071, TL071A, TL071B

JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)

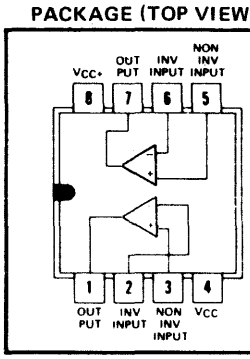


L PLUG-IN PACKAGE (TOP VIEW)

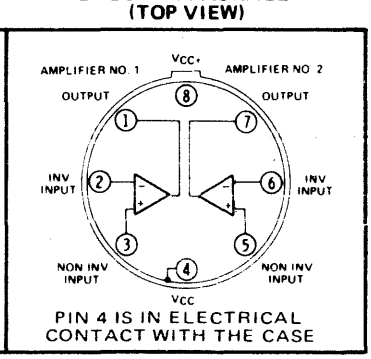


TL072, TL072A, TL072B

JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)



L PLUG-IN PACKAGE (TOP VIEW)

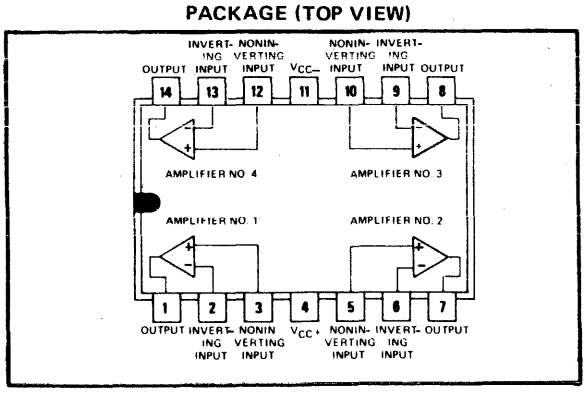


description

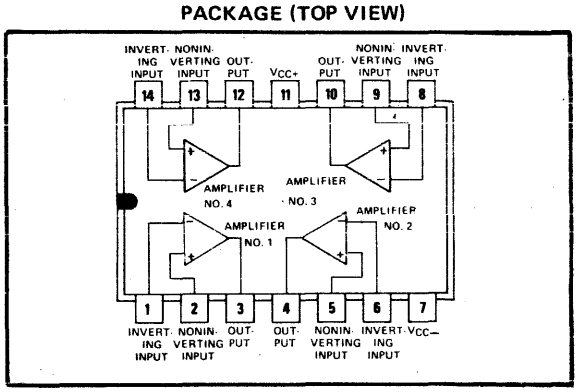
The JFET-input operational amplifiers of the TL071 series are designed as low-noise versions of the TL081 series amplifiers with lower input bias current, offset current, and offset voltage. The low harmonic distortion and low noise make the TL071 series ideally suited as amplifiers for high-fidelity and audio preamplifier applications. Each amplifier features JFET-inputs (for high input impedance) coupled with bipolar output stages all integrated on a single monolithic chip.

Device types with an "M" suffix are characterized for operation over the full military temperature range of −55°C to 125°C, those with an "I" suffix are characterized for operation from −25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

TL074, TL074A, TL074B
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

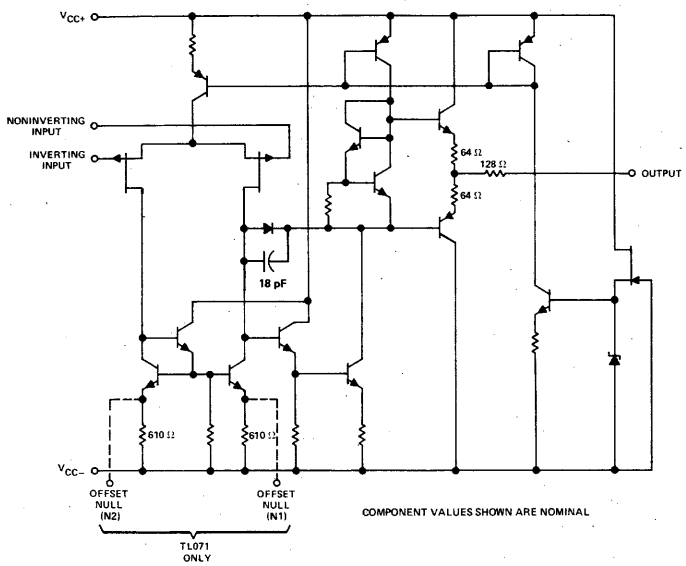


TL075, TL075A, TL075B
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



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schematic (each amplifier)



DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J	680 mW	8.2 mW/°C	67°C
JG	680 mW	6.6 mW/°C	47°C
L	625 mW	5.0 mW/°C	25°C
N	680 mW	9.2 mW/°C	76°C
P	680 mW	8.0 mW/°C	65°C

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL07_M TL07_AM	TL07_I	TL07_C TL07_AC TL07_BC	UNIT
Supply voltage, V_{CC} + (see Note 1)		18	18	18	V
Supply voltage, V_{CC} − (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		Unlimited	Unlimited	Unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	J, JG, N, or P Package	680	680	680	mW
	L Package	625	625	625	
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, JG, or L Package	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Table.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, A_{VD} = 1		13		V/μs
t_r	Rise time	V_I = 20 mV, C_L = 100 pF,	R_L = 2 kΩ, A_{VD} = 1		0.1		μs
	Overshoot factor				10%		
V_n	Equivalent input noise voltage	R_S = 100 Ω	f = 1 kHz		18		nV/√Hz
			f = 10 Hz to 10 kHz		4		μV
I_n	Equivalent input noise current	R_S = 100 Ω,	f = 1 kHz		0.01		pA/√Hz
THD	Total harmonic distortion	$V_{O(rms)}$ = 10 V, $R_L \geq$ 2 kΩ,	$R_S \leq$ 1 kΩ, f = 10 kHz		0.01%		

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electrical characteristics, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS†		TL07_M TL07_AM			TL07_I			TL07_C TL07_AC TL07_BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω, T_A = 25°C	'71, '72, '74, '75		3	6		3	6		3	10	mV
			'71A, '72A, '74A, '75A		2	3					3	6	
			'71B, '72B, '74B, '75B								2	3	
		R_S = 50 Ω, T_A = full range	'71, '72, '74, '75			9			9			13	
			'71A, '72A, '74A, '75A			5						7.5	
			'71B, '72B, '74B, '75B									5	
α_{VIO}	Temperature coefficient of input offset voltage	R_S = 50 Ω,	T_A = full range		10			10			10		μV/°C
I_{IO}	Input offset current‡	T_A = 25°C	'71, '72, '74, '75		5	50		5	50		5	50	pA
			'71A, '72A, '74A, '75A		5	50					5	50	
			'71B, '72B, '74B, '75B								5	50	
		T_A = full range	'71, '72, '74, '75			20			10			2	nA
			'71A, '72A, '74A, '75A			20						2	
			'71B, '72B, '74B, '75B									2	
I_{IB}	Input bias current‡	T_A = 25°C	'71, '72, '74, '75		30	200		30	200		30	200	pA
			'71A, '72A, '74A, '75A		30	200					30	200	
			'71B, '72B, '74B, '75B								30	200	
		T_A = full range	'71, '72, '74, '75			50			20			7	nA
			'71A, '72A, '74A, '75A			50						7	
			'71B, '72B, '74B, '75B									7	
V_{ICR}	Common-mode input voltage range	T_A = 25°C	'71, '72, '74, '75	±12			±12			±10			V
			'71A, '72A, '74A, '75A	±12						±12			
			'71B, '72B, '74B, '75B							±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	T_A = 25°C	R_L = 10 kΩ	24	27		24	27		24	27		V
		T_A = full range	$R_L \geq$ 10 kΩ	24			24			24			
			$R_L \geq$ 2 kΩ	20	24		20	24		20	24		
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, V_O = ± 10 V, T_A = 25°C	'71, '72, '74, '75	50	200		50	200		25	200		V/mV
			'71A, '72A, '74A, '75A	50	200					50	200		
			'71B, '72B, '74B, '75B							50	200		
		$R_L \geq$ 2 kΩ, V_O = ± 10 V, T_A = full range	'71, '72, '74, '75	25			25			15			
			'71A, '72A, '74A, '75A	25						25			
			'71B, '72B, '74B, '75B							25			
B_1	Unity-gain bandwidth	T_A = 25°C			3			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S \leq$ 10 kΩ, T_A = 25°C	'71, '72, '74, '75	80	86		80	86		70	76		dB
			'71A, '72A, '74A, '75A	80	86					80	86		
			'71B, '72B, '74B, '75B							80	86		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$R_S \leq$ 10 kΩ, T_A = 25°C	'71, '72, '74, '75	80	86		80	86		70	76		dB
			'71A, '72A, '74A, '75A	80	86					80	86		
			'71B, '72B, '74B, '75B							80	86		
I_{CC}	Supply current (per amplifier)	No load, T_A = 25°C	No signal,		1.4	2.5		1.4	2.5		1.4	2.5	mA
V_{o1}/V_{o2}	Channel separation	A_{VD} = 100,	T_A = 25°C		120			120			120		dB

†All characteristics are specified under open-loop conditions unless otherwise noted. Full range for T_A is −55°C to 125°C for TL07_M and TL07_AM; −25°C to 85°C for TL07_I; and 0°C to 70°C for TL07_C, TL07_AC, and TL07_BC.

‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

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TYPES TL080 THRU TL084, TL080A THRU TL084A, TL081B, TL082B, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS

JULY 1977

26 DEVICES COVER COMMERCIAL, INDUSTRIAL, AND MILITARY TEMPERATURE RANGES

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation (Except TL080, TL080A)
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/μs Typ

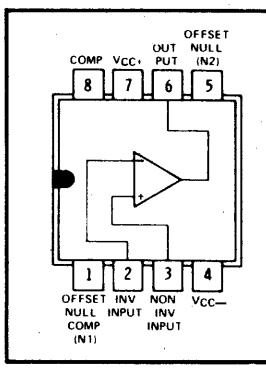
description

The TL081 JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL081 Family.

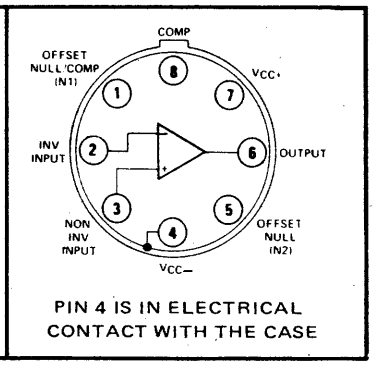
Device types with an "M" suffix are characterized for operation over the full military temperature range of −55°C to 125°C, those with an "I" suffix are characterized for operation from −25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

TL080, TL080A

JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)

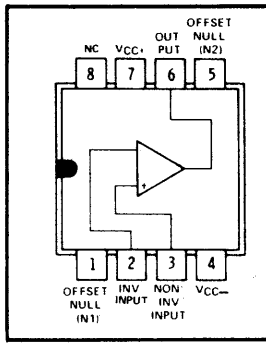


L PLUG-IN PACKAGE (TOP VIEW)

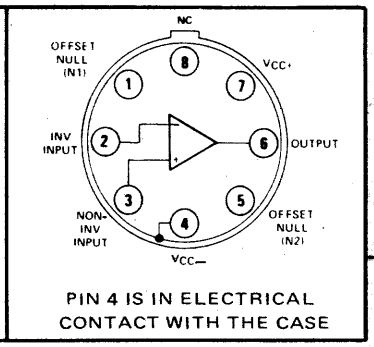


TL081, TL081A, TL081B

JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)

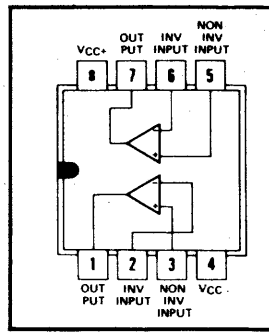


L PLUG-IN PACKAGE (TOP VIEW)

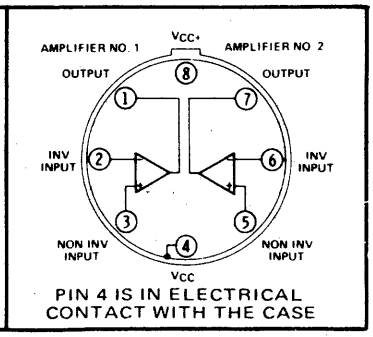


TL082, TL082A, TL082B

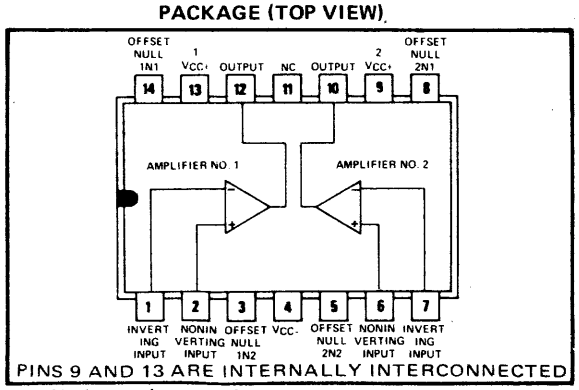
JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)



L PLUG-IN PACKAGE (TOP VIEW)

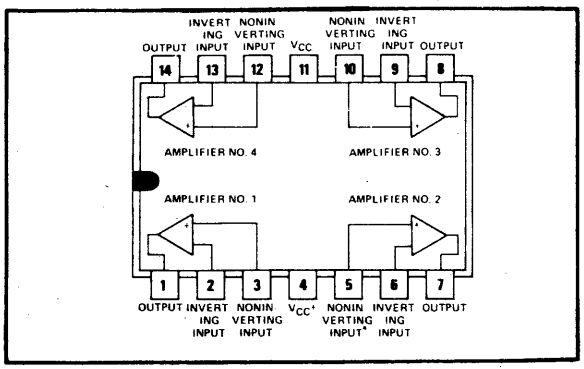


TL083, TL083A
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



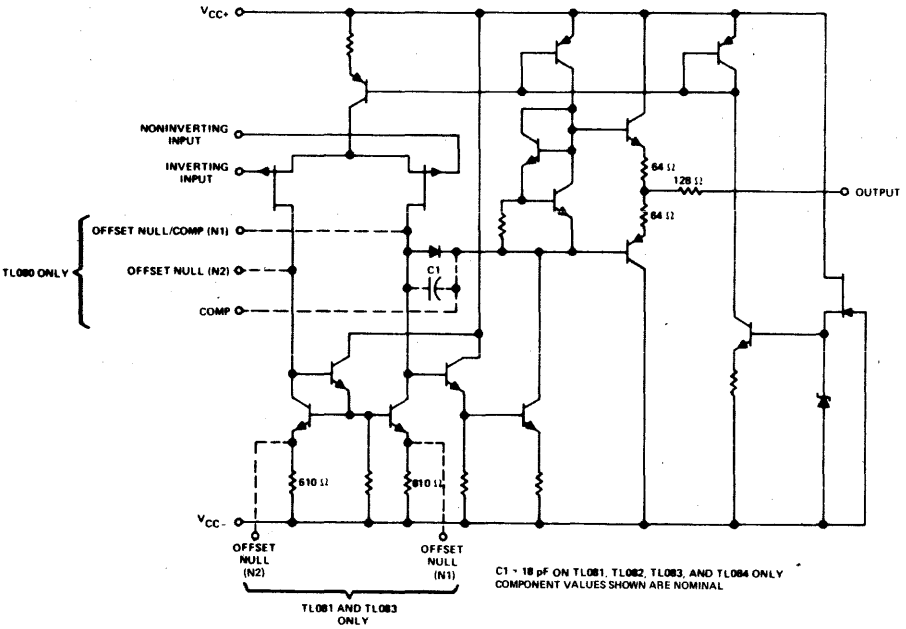
NC—No internal connection

TL084, TL084A, TL084B
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



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schematic (each amplifier)



DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J	680 mW	8.2 mW/°C	67°C
JG	680 mW	6.6 mW/°C	47°C
L	625 mW	5.0 mW/°C	25°C
N	680 mW	9.2 mW/°C	76°C
P	680 mW	8.0 mW/°C	65°C

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL08_M TL08_AM	TL08_I	TL08_C TL08_AC TL08_BC	UNIT
Supply voltage, V_{CC} + (see Note 1)		18	18	18	V
Supply voltage, V_{CC} − (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		Unlimited	Unlimited	Unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	J, JG, N, or P Package	680	680	680	mW
	L Package	625	625	625	
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J, JG, or L Package	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P Package	260	260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Table.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, A_{VD}=1		13		V/μs
t_r	Rise time	V_I = 20 mV, C_L = 100 pF,	R_L = 2 kΩ, A_{VD}=1		0.1		μs
	Overshoot factor				10%		
V_n	Equivalent input noise voltage	R_S = 100 Ω,	f = 1 kHz		47		nV/√Hz

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electrical characteristics, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS†		TL08_M TL08_AM			TL08_I			TL08_C TL08_AC TL08_BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω, T_A = 25°C	TL08_		3	6		3	6		5	15	mV
			TL08_A‡		2	3					3	6	
			'81B,'82B,'84B								2	3	
		R_S = 50 Ω, T_A = full range	TL08_		9			9			20		
			TL08_A‡		5						7.5		
			'81B,'82B,'84B								5		
α_{VIO}	Temperature coefficient of input offset voltage	R_S = 50 Ω,	T_A = full range		10			10			10		μV/°C
I_{IO}	Input offset current§	T_A = 25°C	TL08_		5	100		5	100		5	200	pA
			TL08_A‡		5	100					5	100	
			'81B,'82B,'84B								5	100	
		T_A = full range	TL08_		20			10			5		nA
			TL08_A‡		20						3		
			'81B,'82B,'84B								3		
I_{IB}	Input bias current§	T_A = 25°C	TL08_		30	200		30	200		30	400	pA
			TL08_A‡		30	200					30	200	
			'81B,'82B,'84B								30	200	
		T_A = full range	TL08_		50			20			10		nA
			TL08_A‡		50						7		
			'81B,'82B,'84B								7		
V_{ICR}	Common-mode input voltage range	T_A = 25°C	TL08_	±12			±12			±10			V
			TL08_A‡	±12						±12			
			'81B,'82B,'84B							±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	T_A = 25°C	R_L = 10 kΩ	24	27		24	27		24	27		V
		T_A = full range	$R_L \geq$ 10 kΩ	24			24			24			
			$R_L \geq$ 2 kΩ	20	24		20	24		20	24		
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, V_O = ± 10 V, T_A = 25°C	TL08_	50	200		50	200		25	200		V/mV
			TL08_A‡	50	200					50	200		
			'81B,'82B,'84B							50	200		
		$R_L \geq$ 2 kΩ, V_O = ± 10 V, T_A = full range	TL08_	25			25			15			
			TL08_A‡	25						25			
			'81B,'82B,'84B							25			
B_1	Unity-gain bandwidth	T_A = 25°C			3			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S \leq$ 10 kΩ, T_A = 25°C	TL08_	80	86		80	86		70	76		dB
			TL08_A‡	80	86					80	86		
			'81B,'82B,'84B							80	86		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$R_S \leq$ 10 kΩ, T_A = 25°C	TL08_	80	86		80	86		70	76		dB
			TL08_A‡	80	86					80	86		
			'81B,'82B,'84B							80	86		
I_{CC}	Supply current (per amplifier)	No load, T_A = 25°C	No signal,		1.4	2.8		1.4	2.8		1.4	2.8	mA
V_{o1}/V_{o2}	Channel separation	A_{VD} = 100,	T_A = 25°C		120			120			120		dB

† All characteristics are specified under open-loop conditions unless otherwise noted. Full range for T_A is −55°C to 125°C for TL08_M and TL08_AM; −25°C to 85°C for TL08_I; and 0°C to 70°C for TL08_C, TL08_AC, and TL08_BC.

‡ Types TL080AM and TL083AM are not defined by this data sheet.

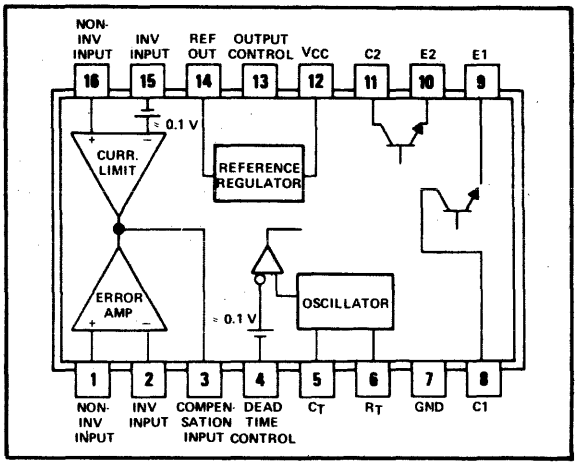
§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

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- Complete PWM Power Control Circuitry
- Uncommitted Outputs for Single-Ended or Push-Pull Operation
- Internal Circuitry Prohibits Double Pulse at Either Output
- Variable Dead-Time Control . . . 45% to 0% at Each Output
- Oscillator Capable of Stand-Alone or Driven Operation

TL494M . . . J
TL494I, TL494C . . . J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)

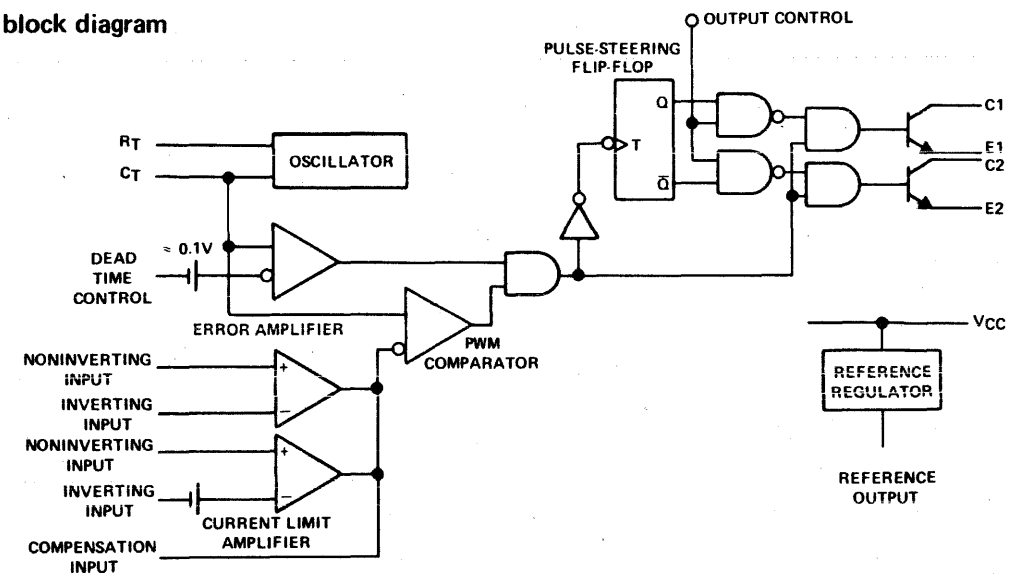


description

The TL494 incorporates on a monolithic chip all the functions required for pulse-width-modulation control circuits. Designed primarily for power supply control, the TL494 has an on-chip 5-volt regulator, error amplifier, current-limit amplifier, adjustable oscillator, dead time control comparator, pulse-steering flip-flop, and output control circuitry. The uncommitted output transistors may be operated common-collector or common-emitter. Internal circuitry provides output control for either complementary or tandem operation. The trigger for the pulse-steering flip-flop is derived from the pulse-width-modulation circuit to prevent double-pulsing of either output. Both the error amplifier and the current-limit amplifier have a common-mode input voltage range from −0.2 volt to V_{CC} − 1.5 volts. Fixed internal offsets provide a current-limit sense threshold of 0.1 volt for the current-limit amplifier and a 45% maximum duty cycle for the dead time control comparator. The oscillator can be programmed by passive components or driven by a master oscillator. The versatility of the TL494 makes it suitable for a variety of PWM applications including switching regulators (of either polarity) and dc-to-dc converters (with or without transformer-coupled outputs).

The TL494M will be characterized for operation over the full military temperature range of −55°C to 125°C. The TL494I will be characterized for operation from −25°C to 85°C, and the TL494C will be characterized for operation from 0°C to 70°C.

functional block diagram



DESIGN GOAL

This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

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recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	7	40	V
Collector output voltage		40	V
Collector output current (each transistor)		200	mA

electrical characteristics

	MIN	TYP	MAX	UNIT
Amplifier common-mode input voltage range	−0.2 to V_{CC} − 2			V
Input bias current (each amplifier)			500	nA
Current-limit sense threshold		0.1		V
Collector-emitter saturation voltage (at I_C = 200 mA)		1.2		V
Range of adjustment of maximum duty cycle (each output)	0 to 45			%
Frequency range	0.001 to 200			kHz
Standard deviation of frequency		2		%
Reference output voltage	4.75		5.25	V

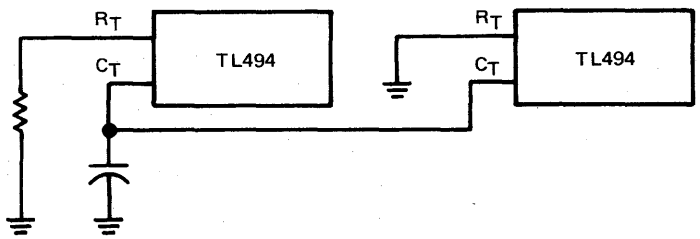
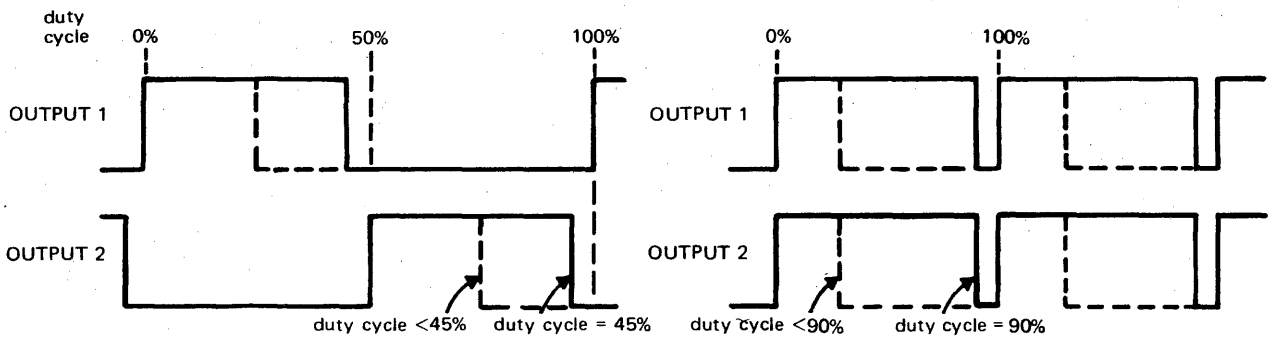


FIGURE 1–MASTER-SLAVE OSCILLATOR CONNECTION



Output control input to V_{CC}.
Each output $f_{out} = \frac{1}{2} f_{osc}$

COMPLEMENTARY (PUSH-PULL) OPERATION

Output control input to ground.
Each output $f_{out} = f_{osc}$

TANDEM (SINGLE-ENDED) OPERATION

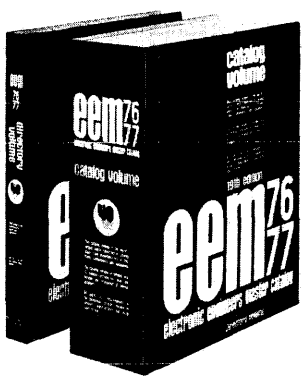
FIGURE 2–OUTPUT DUTY CYCLE AND PHASE RELATIONSHIPS

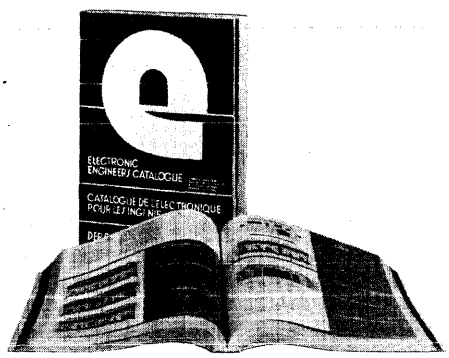
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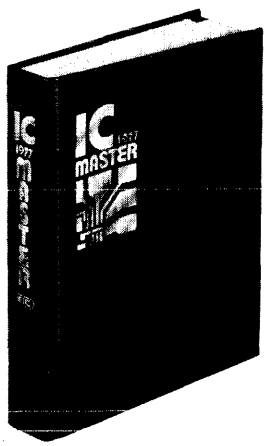
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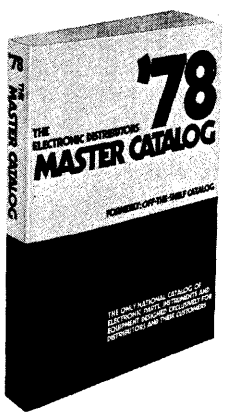
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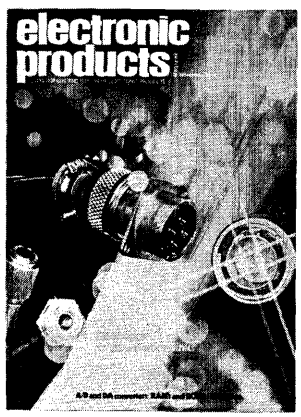
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INTRODUCTION TO MEMORY

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MEMORY.....

The Master Selection Guide provides sufficient information to make initial product selections, to lead you to a group of device numbers and manufacturers' names. It enables you to find the products which are most appropriate to fulfill your major requirements and then provides data for many of the more important products.

All devices that appear in this section, both in the initial selection guide and in the data pages, are included in the Part Number and Product Indexes. These index listings lead to the page and the line on that page where each device appears.

The Memory Section provides initial selection information and data on PROMs, RAMs, and ROMs as well as other memory devices. In these particular sections, the devices are characterized by organization (words and bits/word) and by access times. In order to assure that the access times are comparable, whenever possible the values have been shown in nanoseconds over the full rated temperature range for the devices (i.e., 0° to 70°C for commercial units and −55°C to 125°C for military units). The full temperature nanosecond value is marked "nsF." When this value isn't specified, the guaranteed nanosecond value at room temperature is listed followed by "nsR." In some cases a guaranteed value has not yet been established; then the typical value is shown followed by "ns," "* ". "Typical" values are invariably much faster than the guaranteed ones so that such listings place these memories higher on the list than they otherwise would appear.

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MEMORY–Character Generators

Character Generators

Format	Number of Output Lines	Input Logic levels	Supply Voltage	Device	Source	Line
4 x 5	25	MOS	-12,14	4881	Nortec	
5 x 5	25	MOS	-12,14	4881	Nortec	
6 x 8	8	TTL	-12,5	MM4241	†National	
				MM5241	National	
5 x 7	1	TTL	5	**DM8678**	**National (1274)**	
	5	MOS	±12	4481	Nortec	
		TTL	5	RO3-2513	EMM/Semi	
				RO3-2513	GI	
				5051	†MMI	
				6051	MMI	10
				5052	†MMI	
				6052	MMI	
				5055	†MMI	
				6055	MMI	
				5061	†MMI	
				6061	MMI	
				MCM6670	Motorola	
			-12,±5	2513	Signetics	
			-12,5	3258	Fairchild	
				35581	Fairchild	20
				35582	Fairchild	
	7	MOS	±12	MCS1004	MOS	
				MCS1005	MOS	
			-12(5-12)	MCS2027	MOS	
			±14	CG4100	SMC	
				CG4103	SMC	
			-12,5	CG4103	SMC	
		TTL	5	5056	†MMI	
				6056	MMI	
				5062	†MMI	30
				6062	MMI	
			±12	EA40105	EA	
			-12,5	3257	Fairchild	
				RO5-2240S	GI	
				MK2302	Mostek	
	8	TTL	-12,±5	2516	Signetics	
			±5,12	TMS4710	TI	
	10	TTL	-12,5	MK2408	Mostek	
5 x 8	5	MOS	±12	MM4240	†National	
7 x 8	4	TTL	5	N8228CB	Signetics	40
	10	MOS	±12	EA4004	EA	
	35	MOS	-12,14	4881	Nortec	
7 x 9	1	TTL	5	DM7678	†National	
				DM7679	†National	
				DM8678	**National (1274)**	
				DM8679	National	
			-12,5	MM4220	†National	
				MM5220	National	
	7	MOS	±5	MCS2017	MOS	
		TTL	-12,5	S8564	AMI	50
				3260	Fairchild	
			5	5071	†MMI	
				6071	MMI	
				5072	†MMI	
				6072	MMI	
				5297	†MMI	
				6297	MMI	
				MCM66700	Motorola	

(Continued)

Character Generators (Cont'd)

Format	Number of Output Lines	Input Logic levels	Supply Voltage	Device	Source	Line
7 x 9	7	TTL	5	(Cont'd.)		
				MCM66710	Motorola	60
				MCM6671A0	Motorola	
				MCM66720	Motorola	
				MCM66730	Motorola	
				MCM6673A0	Motorola	
				MCM66740	Motorola	
				MCM66750	Motorola	
				MCM66760	Motorola	
				MCM66770	Motorola	
				MCM66780	Motorola	
				MCM66790	Motorola	70
				2609	Signetics	
			±5	MCS2022	MOS	
			-3,5,12	MCM6570	Motorola	
				MCM6571A	Motorola	
				MCM6572	Motorola	
				MCM6573	Motorola	
				MCM6573A	Motorola	
				MCM6574	Motorola	
				MCM6575	Motorola	
				MCM6576	Motorola	80
				MCM6577	Motorola	
				MCM6578	Motorola	
				MCM6579	Motorola	
				NC6570	Nitron	
				NC6571	Nitron	
				NC6571A	Nitron	
				NC6572	Nitron	
				NC6573	Nitron	
				NC6574	Nitron	
				NC6575	Nitron	90
				NC6576	Nitron	
				NC6580	Nitron	
				NC6581	Nitron	
				NC6533	Nitron	
			±5,12	NC6570A	Nitron	
	9	MOS	-12,-24	EA3815	EA	
			±12	EA4001	EA	
		MOS/TTL	±5	MCS2024	MOS	
		TTL	5	5073	†MMI	
				6073	MMI	00
				5074	†MMI	
				6074	MMI	
			-3,5,12	MCM6580	Motorola	
				MCM6581	Motorola	
				MCM6583	Motorola	
				NC6580	Nitron	
				NC6581	Nitron	
				NC6583	Nitron	
	7 x 10	7	MOS/TTL	±5	MCS2020	MOS
			TTL	±12	EA4016	EA 10
	7 x 11	1	TTL	5	CG5004L	SMC
					CG8002	SMC
	9 x 9	9	TTL	-12,5	RO5-5184	GI
				5	5292	†MMI
					6292	MMI
					5299	†MMI
					6299	MMI
	10 x 12	10	MOS/TTL	±5	MCS2018	MOS
					MCS2025	MOS

† Military Temperature Range (−55° to 125°C)

* Typical Values

MEMORY–Code Converters

Code Converters

Code Conversion From	To	Bits In	Bits Out	Process	Supply Voltage	Device	Source	Line
ASCII-BCDIC		6	6	PMOS	±12	MM4220LR MM5220LR	†National National	
ASCII-EBCDIC		6	7	PMOS	±12	MM4220EK MM5220EK	†National National	
		7	8	PMOS	±12	MM4220AE MM5220AE	†National National	
					-12,5	MM4221RR MM5221RR	†National National	
		8	8	PMOS	-12,5	MK2503 MK2601	Mostek Mostek	10
					±12	MM4230QY MM5230QY	†National National	
			10	PMOS	±12	EA4015	EA	
ASCII HOLLERITH		8	8	PMOS	±12	MM4231BUS MM5231BUS	National National	
		9	10	PMOS	-24	EA4035	EA	
ASCII RS244A and Vice Versa		6	8	PMOS	-12,5	MM4221RQ MM5221RQ	†National National	20
ASCII SELECTRIC		7	7	PMOS	-12,5	3512A	Fairchild	
					±12	MM4230KP MM5230KP	†National National	
BCD-BINARY		6	6	Bipolar	5	SN54184 SN74184	†TI TI	
BCDIC-ASCII		6	7	PMOS	±12	MM4220AP MM5220AP MM4220LR MM5220LR	†National National †National National	30
BCDIC-EBCDIC		6	7	PMOS	±12	MM4220EK MM4230JT MM5220EK MM5230JT	†National †National National National	
Baudot-ASCII		5	8	PMOS	±12	MM4220BL MM5220BL	†National National	
BINARY-BCD		6	6	Bipolar	5	SN54185A SN74185A	†TI TI	
EBCDIC-ASCII		8	8	Bipolar	5	N8204	Signetics	
				PMOS	-12,5	MK2503 MK2601	Mostek Mostek	40
					±12	MM4230QX MM4231RP MM5230QX MM5231RP	†National †National National National	
					-12,5	N2461	Signetics	
			10	PMOS	±12	EA4015	EA	
		9	8	PMOS	±12	N2430	Signetics	
		12	8	Bipolar	5	DM8576AAA	National	
EBCDIC-DCDIC		7	6	PMOS	±12	MM4230JT MM5230JT	†National National	50
EBCDIC HOLLERITH		9	10	MOS	-24	EA4034	EA	
				PMOS	-24	EA4035	EA	
EBCDIC SELECTRIC		8	8	PMOS	±12	MM4230FE MM5230FE	†National National	

Code Converters (Cont'd)

Code Conversion From	To	Bits In	Bits Out	Process	Supply Voltage	Device	Source	Line
HOLLERITH ASCII		8	8	PMOS	±12	MM4230BO MM5230BO MM4231BUS MM5231BUS	†National National †National †National	60
HOLLERITH EBCDIC		8	8	PMOS	±12	MM4230QW MM5230QW	†National National	
		9	10	PMOS	-24	EA4034	EA	
Multiple SELECTRIC, HOLLERITH EBCDIC ASCII and Vice Versa				NMOS	-3,5,12	MCM6561 MCM6562 NC6561	Motorola Motorola Nitron	70
Multiple ASCII SELECTRIC, EBCDIC, HOLLERITH				NMOS	-3,5,12	MCM6591 NC6591	Motorola Nitron	
					±5	MCM68316	Motorola	
SELECTRIC EBCDIC		8	8	PMOS	±12	MM4230FE MM5230FE	†National National	80

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

MEMORY–EAROMs, FIFOs, LIFOs

Electrically Alterable ROMs

Words	Bits Per Word	Access Time (Max)	Output	Supply Voltage	Device	Source	Line
1	1			±20	NOM201	Plessey	
	2			±20	NOM202	Plessey	
	4			±20	NOM204	Plessey	
8	8			±20	NOM401	Plessey	
16	18	1 msF		-30,-18	NC7035	Nitron	
21	16	10 µsF		-20,10	NC7033	Nitron	
32	16	3 µsF	TS	-28	**ER2051**	**GI** (1162)	
		4 nsF	TS	-29,5	NCR2051	NCR	
		10 nsF	TS	-28,5	**ER2050**	**GI** (1162)	
64	4	2 µsF		±15,5	NC7040	Nitron	10
	8	4 nsF	TS	-29,5	NCR2055	NCR	
100	14	3.4 msF	Serial	-35	**ER1400**	**GI** (1159)	
128	8	850 nsF	TS	15, 12,5,25	NCR1721	NCR	
		1.2 µsF	TS	-25,±5	NC7053	Nitron	
256	4	850 nsF	TS	15, 12,5,25	ER1711 NCR1711	GI NCR	20
		1 µsF	TS	±15,5	NC7050	Nitron	
		1.5 µsF		28, 15,5,28	TMM142	Toshiba	
		2 µsF		24,±12,30	ER1105 NCR1105	GI NCR	
		1.2 usF	TS	-25,±5	NC7054	Nitron	
	8	800 nsF	TS	40, 5, 12,5,12,26,36	**µPD454**	**NEC Micro** (1448)	30
		950 nsF	TS	15, 12,5,25	ER1731 NCR1731	GI NCR	
	9	1 µsF	TS	-30,-12	MN1102	Panasonic	
512	2	25 µsR	TS	-30	NC7010	Nitron	
1024	1	5 µsF	TS	-30,-8.7	NC7051	Nitron	
		25 µsR	TS	-30	NC7010	Nitron	40
	4	650 nsF	TS	-30,-12,5	**ER3400**	**GI** (1170)	
		900 nsF	TS	-30,-12,5	NCR2450	NCR	
		950 nsF	TS	-30,-12,5	**ER3401**	**GI** (1170)	
		2 µsF	TS	-23,-14,±5	ER2401 ER2401A NCR2401	GI GI NCR	
	8	450 nsF	TS	40, 5, 12,5,12,26,36	**µPD458**	**NEC Micro** (1454)	
2048	4	1.4 µsF	TS	-23,-14,±5	NCR2810	NCR	50
		1.65µsF	TS	-23,-14,±5	**ER2805** NCR2805	**GI** (1164) NCR	
		2.6 µsF	TS	-23,-14,±5	**ER2800**	**GI** (1164)	

First-In First-Out

Words	Bits/ Word	Data Rate MHz(max)	Supply Voltage	Device	Source	Line
16	2	10.0*	5	8X04	Signetics	
			13	8X03	Signetics	
	4	8.0*	3-15	CD40105B CD40105BE	†RCA RCA	
		10.0	5	**9403C** **9403M**	**Fairchild** (1613) **†Fairchild** (1613)	
	5	10.0	5	SN74S225	TI	60
24	4	2.5	5-16	MS618	†RTC	
32	8	0.5	-12,5	AM2812C AM2812M	AMD †AMD	
		1.0	-12,5	AM2812AC AM2812AM	AMD †AMD	
	9	0.5	-12,5	AM2813C AM2813M	AMD †AMD	
		1.0	-12,5	AM2813AC AM2813AM	AMD †AMD	
40	9	0.25	-12,5	FR1502E-02	Western	70
		0.5	-12,5	FR1502E-01	Western	
		1.0	-12,5	33512 FR1502E	Fairchild Western	
		2.0	-12,5	33511	Fairchild	
64	4	0.7	-12,5	3341C 3341	AMD Fairchild	
		1.0	-12,5	AM2841C AM2841M 3341A	AMD †AMD Fairchild	
		7.0	5	**57401**	**†MMI** (1654)	80
		8.0	5	9423	Fairchild	
		10.0	5	**67401**	**MMI** (1654)	

Last-In First-Out

Words	Bits/ Word	Data Rate MHz(max)	Supply Voltage	Device	Source	Line
16	4	10.5	5	9406C 9406M	Fairchild Fairchild	
81	4	1.0	5	SR5018	SMC	
133	4	1.0	5	SR5017	SMC	

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–PLAs

Organization	Propagation Time	Output	Supply Voltage	Device	Source	Line
PLAs						
48 Product Terms, 16 Inputs, Field Programmable						
	50 nsF	OC	5	93458	Fairchild	
				82S101	MMI	
				N82S101	Signetics	
		TS	5	93459	Fairchild	
				82S100	MMI	
				N82S100	Signetics	
	80 nsF	OC	5	S82S101	† Signetics	
		TS	5	S82S100	† Signetics	
48 Product Terms, 16 Inputs, Factory Programmable						10
	50 nsF	OC	5	N82S201	Signetics	
		TS	5	N82S200	Signetics	
	80 nsF	OC	5	S82S201	† Signetics	
		TS	5	S82S200	† Signetics	
48 Product Terms, 14 Inputs, Field Programmable						
	60 nsF	OC	5	HM7660-5	Harris	
		—	5	HM7661-5	Harris	
	85 nsF	OC	5	HM7660-2	† Harris	
		—	5	HM7661-2	† Harris	
	100 nsF	—	5	IM5200	Intersil	20
50 Product Terms, 12 Inputs, 6 Outputs, Field Programmable						
	35 ns*	TS	5	SN54S330	† TI	
				SN74S330	TI	
		—	5	SN54S331	† TI	
				SN74S331	TI	
96 Product Terms, 14 Inputs, Factory Programmable						
	150 nsF	—	5	**DM7575**	**† National (1285)**	
				DM7576	**† National (1285)**	
				DM8575	**National (1285)**	30
				DM8576	**National (1285)**	
Field Programmable Gate Array, 16 Inputs, 9 AND/NAND Gates, 9 Outputs, Field Programmable						
	30 nsF	OC	5	N82S102	Signetics	
		TS	5	N82S103	Signetics	
	50 nsF	OC	5	S82S102	† Signetics	
		TS	5	S82S103	† Signetics	
Field Programmable Multiplexer, (10 inputs, four 10x8 programmable arrays, four 8:1 addressable multiplexers, four outputs)						40
	55 nsF	TS	5	**29693C**	**Raytheon (1494)**	
	75 nsF	TS	5	**29693M**	**† Raytheon (1494)**	
Field Programmable ROM Patch, for correcting or changing the programs in large ROMs						
	—	OC	5	N82S106	Signetics	
		TS	5	N82S107	Signetics	
Field Programmable Sequential Machine (for building state machines), 48 Transition Terms, 16 Inputs, 8 Outputs						
	—	OC	5	N82S204	Signetics	50
		TS	5	N82S205	Signetics	

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY–PROMs

PROMs

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
32x8	10 ns*	ECL	OE	16	-5.2	MC10139A	Motorola	
	20 nsR	ECL	OE	16	-5.2	SN10139	TI	
	22 nsF	ECL	OE	16	-5.2	10139	Signetics	
	30 nsF	TTL	OC	16	5	**DM74S188**	**National (1262)**	
			TS	16	5	**DM74S288**	**National (1262)**	
	40 nsF	TTL	OC	16	5	AM29750C	AMD	
						HM7602-5	**Harris (1192)**	
						DM54S188	**† National (1262)**	
						SN74S188	TI	
			TS	16	5	AM29751C	AMD	10
						HM7603-5	**Harris (1192)**	
						DM54S288	**† National (1262)**	
						SN74S288	TI	
	50 nsF	TTL	OC	16	5	**HM7602-2**	**† Harris (1192)**	
						M54730	Mitsubishi	
						6330-1	**MMI (1248)**	
						N82S23	Signetics	
						SN54S188	† TI	
			TS	16	5	**HM7603-2**	**† Harris (1192)**	
						6331-1	**MMI (1248)**	20
						N82S123	Signetics	
						SN54S288	† TI	
	50 nsR	TTL	OC	16	5	HPROM8256-2	† Harris	
						HPROM8256-5	Harris	
						IM5600C	Intersil	
						IM5600M	† Intersil	
						DM8577	National	
						SN54188A	† TI	
						SN74188A	TI	
			TS	16	5	IM5610C	Intersil	30
						IM5610M	† Intersil	
						DM8578	National	
	55 nsF	TTL	OC	16	5	AM27S08C	AMD	
			TS	16	5	AM27S09C	AMD	
	60 nsF	TTL	OC	16	5	**5330-1**	**† MMI (1248)**	
			TS	16	5	**5331-1**	**† MMI (1248)**	
	65 nsF	TTL	OC	16	5	AM29750M	† AMD	
						S82S23	† Signetics	
			TS	16	5	AM29751M	† AMD	
						S82S123	† Signetics	40
	70 nsF	TTL	OC	16	5	DM7577	† National	
			TS	16	5	DM7578	† National	
	70 nsR	TTL	OC	16	5	IM5600CF	Intersil	
			TS	16	5	IM5610CF	Intersil	
	75 nsF	TTL	OC	16	5	AM27S08M	† AMD	
						MB7056	Fujitsu	
			TS	16	5	AM27S09M	† AMD	
						MB7051	Fujitsu	
64x8	75 nsR	TTL	OC	24	5	JAN38510/201	† Harris	
						HPROM0512-2	† Harris	50
						HPROM0512-5	Harris	
						MCM5003A	Motorola	
						MCM5303A	† Motorola	
			—	24	5	MCM5004A	Motorola	
						MCM5304A	† Motorola	
256x4	12 ns*	ECL	OE	16	-5,2	GXB1049	Siemens	
	15 ns*	ECL	OE	16	-5.2	F10416C	Fairchild	
	20 nsR	ECL	OE	16	-5.2	10149	Signetics	

(Continued)

PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
256x4	(Cont'd.)							
	25 nsR	ECL	OE	16	-5.2	MCM10149	Motorola	60
						HM7610A-5	**Harris (1200)**	
						N82S27	Signetics	
						HM7611A-5	**Harris (1200)**	
	45 nsF	TTL	OC	16	5	**93417C**	**Fairchild (1151)**	
			TS	16	5	**93427C**	**Fairchild (1151)**	
	50 nsF	TTL	OC	16	5	3601-1	Intel	
						DM74S387	**National (1264)**	
						N82S126	Signetics	
			TS	16	5	3621-1	Intel	
						DM74S287	**National (1264)**	70
						N82S129	Signetics	
	55 nsF	TTL	OC	16	5	**6300-1**	**MMI (1248)**	
			TS	16	5	**6301-1**	**MMI (1248)**	
	60 nsF	TTL	OC	16	5	**93417M**	**† Fairchild (1151)**	
						HM7610-5	**Harris (1192)**	
						M54700	Mitsubishi	
						DM54S387	**† National (1264)**	
						29662C	**Raytheon (1494)**	
			TS	16	5	**93427M**	**† Fairchild (1151)**	
						HM7611-5	**Harris (1192)**	80
						DM54S287	**† National (1264)**	
						29663C	**Raytheon (1494)**	
	60 nsR	TTL	OC	16	5	IM5603AC	Intersil	
						IM5603AM	† Intersil	
						μPB403	**NEC Micro (1462)**	
			TS	16	5	IM5623C	Intersil	
						IM5623M	† Intersil	
	65 nsF	TTL	OC	16	5	SN74S387	TI	
			TS	16	5	SN74S287	TI	
	70 nsF	TTL	OC	16	5	AM27LS10C	AMD	90
						AM27S10C	AMD	
						AM29760C	AMD	
						MB7057	Fujitsu	
						3601	Intel	
						29660C	**Raytheon (1494)**	
						S82S126	† Signetics	
			TS	16	5	AM27LS11C	AMD	
						AM27S11C	AMD	
						AM29761C	AMD	
						MB7052	Fujitsu	100
						3621	Intel	
						29661C	**Raytheon (1494)**	
						S82S129	† Signetics	
	70 nsR	TTL	OC	16	5	HPROM1024A-2	† Harris	
						HPROM1024A-5	Harris	
			TS	16	5	HPROM1024-2	† Harris	
						HPROM1024-5	Harris	
	75 nsF	TTL	OC	16	5	**HM7610-2**	**Harris (1192)**	
						5300-1	**† MMI (1248)**	
						29662M	**† Raytheon (1494)**	110
						SN54S387	† TI	
			TS	16	5	**HM7611-2**	**† Harris (1192)**	
						5301-1	**† MMI (1248)**	
						29663M	**† Raytheon (1494)**	
						SN54S287	† TI	
	80 nsF	TTL	OC	16	5	AM27LS10M	† AMD	
						AM27S10M	† AMD	
						29660M	**† Raytheon (1494)**	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–PROMs (Cont'd)

PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
256x4	80 nsF	TTL	(Cont'd.)					
			TS	16	5	AM27LS11M	† AMD	
						AM27S11M	† AMD	
						29661M	**† Raytheon (1494)**	
	90 nsF	TTL	OC	16	5	M3601	† Intel	
	450 nsF	CMOS	TS	16	5	**HM6611-2**	**† Harris (1184)**	
						HM6611-9	**Harris (1184)**	
256x8	60 nsF	TTL	OC	20	5	DM74S470	National	
			TS	20	5	DM74S471	National	
				24	5	N82S114	Signetics	10
	70 nsF	TTL	OC	20	5	**6308-1**	**MMI (1248)**	
						SN74S470	TI	
			TS	20	5	**6309-1**	**MMI (1248)**	
						SN74S471	TI	
	75 nsF	TTL	OC	20	5	DM54S470	† National	
						29600C	**Raytheon (1494)**	
			TS	20	5	DM54S471	† National	
						29601C	**Raytheon (1494)**	
	80 nsF	TTL	OC	20	5	**5308-1**	**† MMI (1248)**	
						SN54S470	† TI	20
			TS	20	5	**5309-1**	**† MMI (1248)**	
						SN54S471	† TI	
	90 nsF	TTL	OC	24	5	**6335-1**	**† MMI (1248)**	
						63135-1	MMI	
						29600M	**† Raytheon (1494)**	
			TS	24	5	**6336-1**	**MMI (1248)**	
						29601M	**† Raytheon (1494)**	
						S82S114	† Signetics	
	120 nsF	TTL	OC	24	5	**5335-1**	**† MMI (1248)**	
			TS	24	5	**5336-1**	**† MMI (1248)**	30
	550 nsF	Erasable						
			TS	24	-9,5	MK3702-1	Mostek	
	650 nsF	Erasable						
			TS	24	-9,5	1702A-2	Intel	
						1702AL-2	Intel	
	750 nsF	Erasable						
			TS	24	-9,5	9702-1	AMD	
						MK3702-2	Mostek	
						MM1702AQ-1	**National (1365)**	
	800 nsF	Electrically Erasable						40
			TS	24	5,12	**μPD454**	**NEC Micro (1448)**	
	1 μsF	Erasable						
			TS	24	-9,5	1702A	AMD	
						1702A	Intel	
						1702AL	Intel	
						M58563	Mitsubishi	
						MK3702-3	Mostek	
						MM1702AQ	**National (1365)**	
						1702A	Signetics	
					-12,5	MM4203Q	National	
						MM5203Q	National	50
		PMOS	TS	24	-9,5	MK3602P	Mostek	
	1.3 μsF	Erasable						
			TS	24	-9,5	8702A	AMD	
						8702A	Intel	
						MM8702A	National	
	1.5 μsF	Erasable						
			TS	24	-9,5	1702A-6	AMD	

(Continued)

PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
256x8	1.5 μsF	Erasable						
			TS	24	-9,5	(Cont'd.)		60
						1702A-6	Intel	
						ME58563-1	Mitsubishi	
						MM1702AQ-6	**National (1365)**	
	1.7 μsF	Erasable						
			TS	24	-10,5	4702A	AMD	
						4702A	Intel	
						MM4702A	National	
	2.3 μsF	Erasable						
			TS	24	-9,5	MM8702A-4	National	
512x4	45 nsF	TTL	OC	16	5	**HM7620A-5**	**Harris (1202)**	70
			TS	16	5	**HM7621A-5**	**Harris (1202)**	
	50 nsF	TTL	OC	16	5	**93436C**	**Fairchild (1151)**	
						N82S130	Signetics	
			TS	16	5	**93446C**	**Fairchild (1151)**	
						N82S131	Signetics	
	55 nsF	TTL	OC	16	5	**DM74S570**	**National (1266)**	
						29610C	**Raytheon (1494)**	
			TS	16	5	**DM74S571**	**National (1266)**	
						29611C	**Raytheon (1494)**	
	60 nsF	TTL	OC	16	5	**93436M**	**† Fairchild (1151)**	80
						3602A-2	Intel	
						6305-1	**MMI (1248)**	
						29612C	**Raytheon (1494)**	
			TS	16	5	**93446M**	**† Fairchild (1151)**	
						3622A-2	Intel	
						6306-1	**MMI (1248)**	
						29613C	**Raytheon (1494)**	
	70 nsF	TTL	OC	16	5	MB7058	Fujitsu	
						HM7620-5	**Harris (1192)**	90
						3602	Intel	
						3602A	Intel	
						DM54S570	**† National (1266)**	
						S82S130	† Signetics	
			TS	16	5	MB7053	Fujitsu	
						HM7621-5	**Harris (1192)**	
						3622	Intel	
						3622A	Intel	
						DM54S571	**† National (1266)**	
						S82S131	† Signetics	
	70 nsR	TTL	OC	16	5	IM5604C	Intersil	100
						IM5604M	† Intersil	
						29610M	**† Raytheon (1494)**	
			TS	16	5	IM5624C	Intersil	
						IM5624M	† Intersil	
						29611M	**† Raytheon (1494)**	
	75 nsF	TTL	OC	16	5	**5305-1**	**† MMI (1248)**	
						29612M	**† Raytheon (1494)**	
			TS	16	5	**5306-1**	**† MMI (1248)**	
						29613M	**† Raytheon (1494)**	
	85 nsF	TTL	OC	16	5	**HM7620-2**	**† Harris (1192)**	110
			TS	16	5	**HM7621-2**	**† Harris (1192)**	
	1 μsF	Erasable						
			TS	24	-9,±5	TMM121-1	Toshiba	
	1 μsR	Erasable						
			TS	24	-12,5	MM4203Q	National	
						MM5203Q	National	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY–PROMs (Cont'd)

PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
512x4	(Cont'd.)							
	1.5 µsF	Erasable						
			TS	24	-9,±5	TMM121	Toshiba	
512x8	45 nsF	TTL	OC	20	5	N82S146	Signetics	
			TS	20	5	N82S147	Signetics	
	50 nsF	TTL	OC	24	5	**HM7640A-5**	**Harris (1204)**	
			TS	24	5	**HM7641A-5**	**Harris (1204)**	
	55 nsF	TTL	OC	20	5	**29620C**	**Raytheon (1494)**	
				24	5	**93438C**	**Fairchild (1151)**	
						29624C	**Raytheon (1494)**	
			TS	20	5	**29621C**	**Raytheon (1494)**	10
				24	5	**93448C**	**Fairchild (1151)**	
						29625C	**Raytheon (1494)**	
	60 nsF	TTL	OC	20	5	**HM7648-5**	**Harris (1218)**	
				24	5	**HM7640AR-5**	**Harris (1206)**	
						HM7646R-5	**Harris (1212)**	
						HM7646AR-5	**Harris (1212)**	
						3604A-2	Intel	
						N82S140	Signetics	
			TS	20	5	**HM7649-5**	**Harris (1218)**	
				24	5	**HM7641AR-5**	**Harris (1206)**	20
						HM7647R-5	**Harris (1212)**	
						3624A-2	Intel	
						N82S115	Signetics	
						N82S141	Signetics	
						DM74S473	**National (1272)**	
						DM74S472	**National (1272)**	
	65 nsF	TTL	OC	20	5	**29622C**	**Raytheon (1494)**	
				24	5	**DM77S295**	**National (1270)**	
						29626C	**Raytheon (1494)**	
			TS	20	5	**29623C**	**Raytheon (1494)**	30
				24	5	**DM77S296**	**National (1270)**	
						29627C	**Raytheon (1494)**	
	70 nsF	TTL	OC	20	5	**6348-1**	**MMI (1248)**	
						29620M	**† Raytheon (1494)**	
				24	5	**93438M**	**† Fairchild (1151)**	
						HM7640-5	**Harris (1192)**	
						3604	Intel	
						3604A	Intel	
						IM5605C	Intersil	
						6340-1	**MMI (1248)**	40
						MCM7640	Motorola	
						29624M	**† Raytheon (1494)**	
			TS	20	5	**6349-1**	**MMI (1248)**	
						29621M	**† Raytheon (1494)**	
				24	5	**93448M**	**† Fairchild (1151)**	
						HM7641-5	**Harris (1192)**	
						3624	Intel	
						3624A	Intel	
						IM5625C	Intersil	
						6341-1	**MMI (1248)**	50
						MCM7641	Motorola	
						µPB425	**NEC Micro (1466)**	
						29625M	**† Raytheon (1494)**	
	75 nsF	TTL	OC	20	5	SN74S473	TI	
				24	5	SN74S475	TI	
			TS	20	5	SN74S472	TI	
				24	5	SN74S474	TI	

(Continued)

PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
512x8	(Cont'd.)							
	80 nsF	TTL	OC	20	5	**5348-1**	**† MMI (1248)**	
						29622M	**† Raytheon (1494)**	60
						DM54S473	**† National (1272)**	
				24	5	IM5605M	† Intersil	
						5340-1	**† MMI (1248)**	
						DM87S295	**† National (1270)**	
						29626M	**† Raytheon (1494)**	
			TS	20	5	**5349-1**	**† MMI (1248)**	
						29623M	**† Raytheon (1494)**	
						DM54S472	**† National (1272)**	
				24	5	IM5625M	† Intersil	
						5341-1	**† MMI (1248)**	70
						DM87S296	**† National (1270)**	
						29627M	**† Raytheon (1494)**	
	85 nsF	TTL	OC	20	5	SN74S473	TI	
				24	5	**HM7640-2**	**† Harris (1192)**	
						SN74S475	TI	
			TS	20	5	SN74S472	TI	
				24	5	**HM7641-2**	**† Harris (1192)**	
						SN74S474	TI	
	90 nsF	TTL	OC	24	5	3604-4	Intel	
						3604L-6	Intel	80
						3604AL	Intel	
						M3604	† Intel	
						63137-1	MMI	
						63139-1	MMI	
						S82S140	† Signetics	
			TS	24	5	3624-4	Intel	
						M3624	† Intel	
						S82S141	† Signetics	
						S82S115	† Signetics	
	100 nsF	TTL	OC	24	5	**µPB405-E**	**NEC Micro (1466)**	90
			TS	24	5	**µPB425-E**	**NEC Micro (1466)**	
	450 nsF	Erasable						
			TS	24	±5,12	2704	AMD	
						EA2704C	EA	
						2704	Fairchild	
						2704	Intel	
						MM2704	National	
						2704	Signetics	
	500 nsF	Erasable						
			TS	24	±5,12	EA2704L	EA	100
	550 nsF	Erasable						
			TS	24	±5,12	EA2704M	† EA	
	575 nsF	Erasable						
			TS	24	-12,5	**S6834**	**AMI (1067,1563)**	
	750 nsF	Erasable						
			TS	24	-12,5	**S5204A**	**AMI (1057,1591)**	
						S6834-1	**AMI (1067)**	
	1 µsF	Erasable						110
			TS	24	-12,5	**MM5204Q**	**National (1369)**	
	1.25 µsF	Erasable						
			TS	24	-12,5	**MM4204Q**	**National (1369)**	
1024x4	35 nsR	TTL	OC	18	5	SN54S477	† TI	
						SN74S477	TI	
			TS	18	5	SN54S476	† TI	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–PROMs (Cont'd)

PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x4	35 nsR	TTL	TS	18	5	(Cont'd.)		
						SN74S476	TI	
	55 nsF	TTL	OC	18	5	**93452C**	**Fairchild (1151)**	
			TS	18	5	**93453C**	**Fairchild (1151)**	
	60 nsF	TTL	OC	18	5	3605-2	Intel	
						6350-1	**MMI (1248)**	
						6352-1	**MMI (1248)**	
						DM74S572	**National (1268)**	
						N82S136	Signetics	
			TS	18	5	3625-2	Intel	10
						6351-1	**MMI (1248)**	
						6353-1	**MMI (1248)**	
						DM74S573	**National (1268)**	
						N82S137	Signetics	
	70 nsF	TTL	OC	18	5	**93452M**	**† Fairchild (1151)**	
						MB7059	Fujitsu	
						HM7642-5	**Harris (1192)**	
						3605	Intel	
						MCM7642	Motorola	
						μPB406	**NEC Micro (1470)**	20
			TS	18	5	**93453M**	**† Fairchild (1151)**	
						MB7054	Fujitsu	
						HM7643-5	**Harris (1192)**	
						3625	Intel	
						MCM7643	Motorola	
						μPB426	**NEC Micro (1470)**	
			—	16	5	**HM7644-5**	**Harris (1192)**	
	75 nsF	TTL	OC	18	5	**5350-1**	**† MMI (1248)**	
						5352-1	**† MMI (1248)**	
						DM54S572	**† National (1268)**	30
			TS	18	5	**5351-1**	**† MMI (1248)**	
						5353-1	**† MMI (1248)**	
						DM54S573	**† National (1268)**	
	80 nsF	TTL	OC	18	5	S82S136	† Signetics	
			TS	18	5	S82S137	† Signetics	
	85 nsF	TTL	OC	18	5	**HM7642-2**	**† Harris (1192)**	
			TS	18	5	**HM7643-2**	**† Harris (1192)**	
			—	16	5	**HM7644-2**	**† Harris (1192)**	
	100 nsF	TTL	OC	18	5	**μPB406-E**	**NEC Micro (1470)**	
			TS	18	5	**μPB426-E**	**NEC Micro (1470)**	40
1024x8	45 nsF	TTL	OC	24	5	**93450C**	**Fairchild (1151)**	
			TS	24	5	**93451C**	**Fairchild (1151)**	
	60 nsF	TTL	OC	24	5	**93450M**	**† Fairchild (1151)**	
			TS	24	5	**93451M**	**† Fairchild (1151)**	
	70 nsF	TTL	OC	24	5	N82S180	Signetics	
			TS	24	5	N82S181	Signetics	
						N82S2708	Signetics	
	80 nsF	TTL	OC	24	5	**HM7680-5**	**Harris (1220)**	
						HM7680P-5	**Harris (1232)**	
						HM7680R-5	**Harris (1226)**	50
						HM7680RP-5	**Harris (1234)**	
						3608	Intel	
						29640C	**Raytheon (1494)**	
						S82S136	† Signetics	
			TS	24	5	**HM7608-5**	**Harris (1235)**	
						HM7681-5	**Harris (1220)**	
						HM7681P-5	**Harris (1232)**	
						HM7681R-5	**Harris (1226)**	

(Continued)

PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x8	80 nsF	TTL	TS	24	5	(Cont'd.)		
						HM7681RP-5	**Harris (1234)**	60
						3628	Intel	
						29641C	**Raytheon (1494)**	
						29645C	**Raytheon (1494)**	
						S82S137	† Signetics	
			—	20	5	**HM7683-5**	**Harris (1241)**	
	85 nsF	TTL	OC	24	5	**μPB408**	**NEC Micro (1491)**	
			TS	24	5	**μPB428**	**NEC Micro (1491)**	
	90 nsF	TTL	OC	22	5	**6386-1**	**MMI (1248)**	
				24	5	**6380-1**	**MMI (1248)**	
						6384-1	**MMI (1248)**	70
						S82S180	† Signetics	
			TS	22	5	**6387-1**	**MMI (1248)**	
				24	5	**6381-1**	**MMI (1248)**	
						6385-1	**MMI (1248)**	
						S82S181	† Signetics	
						S82S2708	† Signetics	
	95 nsF	TTL	OC	24		**29642C**	**Raytheon (1494)**	
			TS	24		**29643C**	**Raytheon (1494)**	
						29647C	**Raytheon (1494)**	
	100 nsF	TTL	OC	24	5	3608-4	Intel	80
			TS	24	5	3628-4	Intel	
	110 nsF	TTL	OC	24	5	**29640M**	**† Raytheon (1494)**	
			TS	24	5	**29641M**	**† Raytheon (1494)**	
						29645M	**† Raytheon (1494)**	
	125 nsF	TTL	OC	22	5	5386-1	† MMI	
				24	5	5380-1	† MMI	
						5384-1	† MMI	
						29642M	**† Raytheon (1494)**	
			TS	22	5	5387-1	† MMI	
				24	5	5381-1	† MMI	90
						5385-1	† MMI	
						μPB427	**NEC Micro (1491)**	
						29643M	**† Raytheon (1494)**	
						29647M	**† Raytheon (1494)**	
	250 nsF	TTL	OC	24	5	MB7060	Fujitsu	
			TS	24	5	MB7055	Fujitsu	
	300 nsF	Erasable						
			TS	24	±5,12	MCM27A08L	Motorola	
						MCM68A708L	Motorola	
	350 nsF	Erasable						100
			TS	24	±5,12	**2708-1**	**Fairchild (1093)**	
						2708-1	Intel	
						TMS2708-35	TI	
	450 nsF	Electrically Erasable						
			TS	24	5,12	**μPD458**	**NEC Micro (1454)**	
		Erasable						
			TS	24	5	2758	Intel	
					±5,12	2708	AMD	
						EA2708C	EA	
						2708	**Fairchild (1093)**	110
						MB8518H	Fujitsu	
						2708	Intel	
						M2708	† Intel	
						MK2708	Mostek	
						MCM2708L	Motorola	
						MCM68708	Motorola	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY–PROMs (Cont'd)

PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x8	450 nsF	Erasable						
			TS	24	±5,12	(Cont'd.)		
						MCM68708L	Motorola	
						MM2708	National	
						2708	Signetics	
						TMS27L08	TI	
						TMS2708	TI	
						TMS2708M	†TI	
		NMOS	TS	24	±5,12	MCM2708CP	Motorola	
	500 nsF	Erasable						10
			TS	24	±5,12	EA2708L	EA	
	550 nsF	Erasable						
			TS	24	±5,12	EA2708M	†EA	
						TMM322C	Toshiba	
	650 nsF	Erasable						
			TS	24	±5,12	MB8518E	Fujitsu	
2048x4	80 nsF	TTL	OC	18	5	**HM7684-5**	**Harris**	(1242)
						HM7684P-5	**Harris**	(1243)
				20	5	**HM7686-5**	**Harris**	(1244)
						HM7686P-5	**Harris**	(1246) 20
						HM7686R-5	**Harris**	(1245)
						HM7686RP-5	**Harris**	(1247)
			TS	18	5	**HM7685-5**	**Harris**	(1242,1244)
						HM7685P-5	**Harris**	(1243)
				20	5	**HM7687-5**	**Harris**	(1244)
						HM7687P-5	**Harris**	(1246)
						HM7687R-5	**Harris**	(1245)
						HM7687RP-5	**Harris**	(1247)
	100 nsF	TTL	OC	18	5	N82S184	Signetics	30
			TS	18	5	N82S185	Signetics	
	125 nsF	TTL	OC	18	5	S82S184	† Signetics	
			TS	18	5	S82S185	† Signetics	
2048x8	80 nsF	TTL	OC	24	5	N82S190	Signetics	
			TS	24	5	N82S191	Signetics	
	100 nsF	TTL	OC	24	5	S82S190	† Signetics	
			TS	24	5	S82S191	† Signetics	
	450 nsF	Erasable						
			TS	24	5	MBM2716	Fujitsu	
						2716	Intel	40
						μPD2716	**NEC Micro**	(1492)
					±5,12	MCM2716	Motorola	
						MCM2717	Motorola	
						TMS2716	TI	

† Military Temperature Range (−55° to 125°C)
ns*—Nanoseconds Typical
nsF—Nanoseconds over Full Temperature Range
nsR—Nanoseconds at Room Temperature
OC—Open Collector
TS—Three-State
OE—Open Emitter

MEMORY–RAMs

Dynamic

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x1	60 nsF	NMOS	—	18	±15	EA1500A	EA	
	100 nsF	PMOS	—	18	19,22.5	SY1103A-X	Synertek	
	110 nsF	PMOS	—	18	19,22.5	1103A-X	Rockwell	
	120 nsF	NMOS	—	18	±15	EA1500A-1	EA	
		PMOS	—	18	19,22.5	S1103X	AMI	
	125 nsF	PMOS	—	18	19,22.5	S1103A-X	AMI	
	145 nsF	PMOS	—	18	19,22.5	S1103A-1	AMI	
						1103A-1	Intel	
						1103A-2	Intel	
						1103A-1	Rockwell	10
						1103A-2	Rockwell	
						SY1103A-1	Synertek	
	150 nsF	PMOS	—	18	19,22.5	S1103-1	AMI	
						HM3503-1	Hitachi	
						1103-1	Intel	
						1103-1	Nortec	
					20,22,7	TMS4063	TI	
				22	20,22.5,7	IM6002-11	Intersil	
						6002	Nortec	
					20,22,7	TMS4062	TI	20
	205 nsF	PMOS	—	18	16,19.5	S1103A	AMI	
						1103A	Intel	
						1103A	Rockwell	
						SY1103A	Synertek	
					19,22.5	S146	AMI	
						1103-146	Nortec	
	220 nsF	PMOS	—	18	19,22.5	HM3503-2	Hitachi	
	300 nsF	PMOS	—	18	16,19.5	S1103	AMI	
						HM3503	Hitachi	
						1103	Intel	30
						ITT1103	ITT	
						1103	Nortec	
						MN1003	Panasonic	
						1103	Signetics	
	400 nsF	PMOS	—	16	-12,5	S4006	AMI	
						MK4006	Mostek	
	500 nsF	PMOS	—	16	-12,5	S4008	AMI	
						MK4008	Mostek	
	800 nsF	PMOS	—	16	-12,5	S4008-9	AMI	
2048x1	350 nsF	PMOS	—	22	-15,8,5	IM6003-11	Intersil	40
						600311	Nortec	
	460 nsF	PMOS	—	22	-15,8,5	IM6003-10	Intersil	
						600314	Nortec	
4096x1	70 nsF	NMOS	—	22	-5.2,7,12	MB8215H	Fujitsu	
	80 nsF	I²L	TS	16	5	93481B	Fairchild	
	100 nsF	I²L	TS	16	5	93481A	Fairchild	
		NMOS	TS	18	±5,12	MM5287A-1	National	
			—	22	-5.2,7,12	MB8215E	Fujitsu	
			TS	22	±5,12	**MM5280A-1**	**National (1339)**	
	120 nsF	I²L	TS	16	5	93481	Fairchild	50
	125 nsR	NMOS	TS	18	-5,12	**MM5270A-2**	**National (1328)**	
						MM5271A-1	**National (1333)**	
				22	±5,12	**MM5280A-2**	**National (1339)**	
	135 nsF	NMOS	TS	22	±5,15	**μPD411-4**	**NEC Micro (1375)**	
	140 nsF	NMOS	TS	18	-5,12	**MM5271**	**National (1333)**	
	150 nsF	NMOS	TS	16	±5,12	**M4027-2**	**Fairchild (1118)**	

(Continued)

Dynamic (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
4096x1	150 nsF	NMOS	TS	16	±5,12	(Cont'd.)		
						MB8227H	Fujitsu	
						2104A-1	Intel	
						MK4027-2	Mostek	60
						MCM4027-2	Motorola	
						MCM4227-2	Motorola	
						μPD414A-3	**NEC Micro (1395,1488)**	
						2627-2	Signetics	
						TMS4027-15	TI	
				18	-5,12	**MM5270A**	**National (1328)**	
						MM5271A	**National (1333)**	
						μPD418-3	**NEC Micro (1412)**	
				22	±5,12	MB8107Y	Fujitsu	70
						2707C-1	Intel	
						MCM6605A-1	Motorola	
						MM5280A	**National (1339)**	
						μPD411-3	**NEC Micro (1375)**	
	200 nsF	NMOS	TS	16	±5,12	EA4060-2	EA	
						EA4116	EA	
						M4027-3	**Fairchild (1118)**	
						MB8224H	Fujitsu	
						MB8227E	Fujitsu	
						2104A-2	Intel	80
						MK4027-3	Mostek	
						MK4027-83	Mostek	
						MK4227-3	Mostek	
						MCM4027-3	Motorola	
						MCM4227-3	Motorola	
						μPD414-2	**NEC Micro (1395)**	
						μPD414A-2	**NEC Micro (1395,1488)**	
						4096	Rockwell	
						2627-3	Signetics	90
						TMS4027-20	TI	
						TMM415-3	Toshiba	
				18	-5,12	9050E	AMD	
						IM7270-11	Intersil	
						MM5270	**National (1325)**	
						MM5271	**National (1333)**	
						μPD418-2	**NEC Micro (1412)**	
						SY5270	Synertek	
						TMS4050-2	TI	
				22	±5,12	9060E	AMD	100
						EA2107B	EA	
						EA4122-2	EA	
						MB8107H	Fujitsu	
						2107C-2	Intel	
						IM7280-11	Intersil	
						M58755-1	Mitsubishi	
						MCM6605A-2	Motorola	
						MM5280	**National (1336)**	
						MM5281	National	
						μPD411A-2	**NEC Micro (1382)**	110
						μPD411-2	**NEC Micro (1375)**	
						μPD411-2M	**NEC Micro (1390)**	
						MN1001-2	Panasonic	
						M340A	SGS	
						2680	Signetics	
						SY5280	Synertek	
						TMS4060-2	TI	
						TMM414	Toshiba	
					-3,5,12	TMS4030-2	TI	
	220 nsF	NMOS	TS	22	±5,12	EA2107B-2	EA	120

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY–RAMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
Dynamic (Cont'd)								
4096x1	(Cont'd.)							
	230 nsF	NMOS	TS	16	±5,12	MB8224E	Fujitsu	
	250 nsF	NMOS	TS	16	±5,12	EA4060-1	EA	
						M4027-4	**Fairchild (1118)**	
						4096-3	Fairchild	
						MB8227N	Fujitsu	
						2104A-3	Intel	
						IM7005-11	Intersil	
						MK4027-4	Mostek	
						MK4027-84	Mostek	10
						MK4096-6	Mostek	
						MK4096-77	Mostek	
						MK4096-86	Mostek	
						MK4227-4	Mostek	
						MCM4027-4	Motorola	
						MCM4096-6	Motorola	
						MCM4227-4	Motorola	
						MCM6604A-2	Motorola	
						μPD414-1	**NEC Micro (1395)**	
						μPD414A-1	**NEC Micro (1395,1488)**	20
						2660	Signetics	
						2660-3	Signetics	
						TMM415-4	Toshiba	
				18	-5,12	9050D	AMD	
						MM5271	**National (1333)**	
						μPD418-1	**NEC Micro (1412)**	
						SY5271	Synertek	
						TMS4050-1	TI	
						TMS4051-1	TI	30
				22	±5,12	9060D	AMD	
						EA4122-1	EA	
						MB8107E	Fujitsu	
						2107C	Intel	
						MM5281	National	
						μPD411-1	**NEC Micro (1375)**	
						μPD411-1M	**NEC Micro (1390)**	
						μPD411A-1	**NEC Micro (1382)**	
						MN1001-1	Panasonic	
						SY5281	Synertek	40
						TMS4060-1	TI	
						TMM414-1	Toshiba	
					-3,5,12	TMS4030-1	TI	
	270 nsF	NMOS	TS	18	-5,12	IM7270-12	Intersil	
						MM4270	**National (1311)**	
						MM5270-5	**National (1331)**	
				22	±5,12	EA2107B-4	EA	
						IM7280-12	Intersil	
						M58755-2	Mitsubishi	
						MM4280	**National (1314)**	50
						MM5280-5	**National (1342)**	
						M340B	SGS	
						2680-1	Signetics	
	280 nsF	NMOS	TS	16	±5,12	MB8224N	Fujitsu	
				22	±5,12	2107A-1	Intel	
	300 nsF	NMOS	TS	16	±5,12	EA4060	EA	
						M4027-5	**Fairchild (1118)**	
						4096-4	Fairchild	
						2104A-4	Intel	
						IM7005-12	Intersil	60
						MK4096-16	Mostek	
						MK4096-86	Mostek	
						MCM6604A-4	Motorola	
						μPD414	**NEC Micro (1395)**	

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
Dynamic (Cont'd)								
4096x1	300 nsF	NMOS	TS	16	±5,12	(Cont'd.)		
						μPD414A	**NEC Micro (1395,1488)**	
						4096-4	Rockwell	
						2660-1	Signetics	
				18	-5,12	9050C	AMD	70
						μPD418	**NEC Micro (1412)**	
						SY4050	Synertek	
						TMS4050	TI	
						TMS4051	TI	
				22	±5,12	9060C	AMD	
						EA2107B-L	EA	
						EA4122	EA	
						MB8107N	Fujitsu	
						HM4503-1	Hitachi	
						HM4507	Hitachi	80
						2107C-4	Intel	
						MCM6605A	Motorola	
						μPD411	**NEC Micro (1375)**	
						μPD411-M	**NEC Micro (1390)**	
						μPD411A	**NEC Micro (1382)**	
						MN1001	Panasonic	
						HYB4060	Siemens	
						TMS4060	TI	
					-3,5,12	TMS4030	TI	
	350 nsF	NMOS	TS	16	±5,12	4096-5	Fairchild	90
						2104A	Intel	
						IM7005-13	Intersil	
						MK4096-11	Mostek	
						MK4096-85	Mostek	
						MK4200-11	Mostek	
						MCM4096-11	Motorola	
						MCM6604A	Motorola	
						μPD414-E	**NEC Micro (1395)**	
						4096-5	Rockwell	
						2660-2	Signetics	100
				18	-5,12	IM7270-14	Intersil	
				22	±5,12	**μPD411-E**	**NEC Micro (1375)**	
						μPD411A-E	**NEC Micro (1382)**	
						M340C	SGS	
						2680-2	Signetics	
	400 nsF	NMOS	TS	18	±5,12	HM4503	Hitachi	
						2675	Signetics	
	420 nsF	NMOS	TS	22	±5,12	9107-6	AMD	
8192x1	150 nsF	NMOS	TS	22	±5,12	7008-10	Intersil	
	200 nsF	NMOS	TS	16	±5,12	2108-2	Intel	110
						2109-2	Intel	
				22	±5,12	7008-11	Intersil	
	300 nsF	NMOS	TS	16	±5,12	2108-4	Intel	
						2109-4	Intel	
16384x1	120 nsF	NMOS	TS	16	±5,12	MB8116	Fujitsu	
						MK4116-1	Mostek	
	150 nsF	NMOS	TS	16	±5,12	**F16K2**	**Fairchild (1110)**	
						MB8116H	Fujitsu	
						2117-2	Intel	
						MCM4116-15	Motorola	120
						MK4116-2	Mostek	
						μPD416-3	**NEC Micro (1402)**	
						2690-2	Signetics	
						TMS4116-15	TI	
						Z6116-2	Zilog	
	200 nsF	NMOS	TS	16	±5,12	MB8116E	Fujitsu	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–RAMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device
Dynamic (Cont'd)						
16384x1	200 nsF	NMOS	TS	16	±5,12	(Cont'd.)
						2116-2
						2117-3
						MK4116-3
						MCM4116-20
						MM5290-3
						μPD416-2
						2690-3
						TMS4116-20
						Z6116-3
	250 nsF	NMOS	TS	16	±5,12	**F16K3**
						MB8116N
						2116-3
						2117-4
						7116-11
						MK4116-4
						MCM4116-25
						MM5290-4
						μPD416-1
						2690-4
						TMS4116-25
						TMM416-4
						Z6116-4
	300 nsF	NMOS	TS	16	±5,12	**F16K4**
						2116-4
						2117-4
						MCM4116-30
						μPD416
	350 nsF	NMOS	TS	16	±5,12	**F16K5**
						2116
Bubble Memories						
92,304 Bits (641x144x1)				16		TBM0103
CCD Memories						
910 Bits (455x2)				16		CCD321
9216 Bits(1024x9)				16		CCD450A
						CCD450B
				18		CCD451A
						CCD451B
16,384 Bits (256x64x1)				18		2416
65,536 Bits(256x256)				18		2464
65,536 Bits(4096x16x1)				16		**F464**
						MCM0464
						TMS3064
Static						
4x4	20 nsR	TTL	OC	16	5	25LS170C
						25LS170M
			TS	16	5	25LS670C
						25LS670M
	30 nsF	TTL	OC	24	5	3104
	30 nsR	TTL	OC	16	5	54LS170
						74LS170

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† Military Temperature Range (–55° to 125°C) ns*—Nanosecor

OC—Open Collector

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MEMORY–RAMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
Static (Cont'd)								
128x8	(Cont'd.)							
	250 ns*	NMOS	TS	24	5	MCM68B10	Motorola	
	350 nsF	NMOS	TS	24	5	MCM6810A	Motorola	
	350 ns*	CMOS	TS	24	5	CDP1823SC	RCA	
	360 nsF	NMOS	TS	24	5	MCM68A10	Motorola	
	450 nsF	NMOS	TS	24	5	MCM6810A-1	Motorola	
	1 μsF	NMOS	TS	24	5	**S6810**	**AMI** (1061)	
128x9	500 nsF	CMOS	TS	22	5	MN1101	Panasonic	
256x1	15 nsF	ECL	OE	16	-5.2	F100414	Fairchild	
						F10414	Fairchild	10
						MB7042	Fujitsu	
						MCM10152	Motorola	
	25 nsF	ECL	OE	16	-5.2	μPB10144	NEC America	
	26 nsR	ECL	OE	16	-5.2	MCM10144	Motorola	
	30 nsF	ECL	OE	16	-5.2	F10410C	Fairchild	
						10144	Signetics	
	30 nsR	ECL	OE	16	-5.2	SP10144	Plessey	
	35 nsF	ECL	OE	16	-4.25	F10411C	Fairchild	
					-5.2	MBM10410	Fujitsu	
						HM2105	Hitachi	20
						RC10144	Raytheon	
		TTL	TS	16	5	AM27LS00AC	AMD	
	35 nsR	ECL	OE	16	-5.2	SN10144	TI	
	40 nsF	ECL	OE	16	-5.2	RI10144	Raytheon	
		TTL	OC	16	5	N82S117	Signetics	
			TS	16	5	93421AC	Fairchild	
						93421AC	Raytheon	
						N82S116	Signetics	
	45 nsF	TTL	OC	16	5	AM27LS01C	AMD	
						AM29720C	AMD	30
						93410AC	Fairchild	
						93411AC	Fairchild	
						93411AC	Raytheon	
			TS	16	5	AM27LS00C	AMD	
						AM27LS00AM	† AMD	
						AM29721C	AMD	
						93L420C	Fairchild	
	50 nsF	TTL	OC	16	5	N82S17	Signetics	
						74S301	Signetics	
			TS	16	5	93421C	Fairchild	40
						DM74S200	National	
						RC5340	Raytheon	
						93421C	Raytheon	
						N82S16	Signetics	
						74S200	Signetics	
						74S201	Signetics	
	55 nsF	TTL	OC	16	5	AM27LS01M	† AMD	
						AM29720M	† AMD	
						93411C	Fairchild	
						6530	MMI	50
						RC5330	Raytheon	
						93411C	Raytheon	
			TS	16	5	AM27LS00M	† AMD	
						AM29721M	† AMD	
						93L420M	† Fairchild	
						6531	MMI	
	60 nsF	TTL	OC	16	5	AM27S01BC	AMD	

(Continued)

† Military Temperature Range (–55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full

OC—Open Collector TS—Three-State

Bold face indicates additional data is provided on the pag

Organization	Access Time (Max)
Static (Cont'	
256x1	60 nsF
	65 nsF
	70 nsF
	75 nsF
	80 nsF
	80 nsR
	90 nsF
	95 nsF
	100 nsF
	115 nsF
	130 nsF
	150 ns*
	200 ns*
	300 ns*
	380 nsR
	400 nsR
	500 nsR

MEMORY–RAMs (Cont'd)

Dynamic (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
4096x1	(Cont'd.)							
	230 nsF	NMOS	TS	16	±5,12	MB8224E	Fujitsu	
	250 nsF	NMOS	TS	16	±5,12	EA4060-1	EA	
						M4027-4	**Fairchild (1118)**	
						4096-3	Fairchild	
						MB8227N	Fujitsu	
						2104A-3	Intel	
						IM7005-11	Intersil	
						MK4027-4	Mostek	
						MK4027-84	Mostek	10
						MK4096-6	Mostek	
						MK4096-77	Mostek	
						MK4096-86	Mostek	
						MK4227-4	Mostek	
						MCM4027-4	Motorola	
						MCM4096-6	Motorola	
						MCM4227-4	Motorola	
						MCM6604A-2	Motorola	
						μPD414-1	**NEC Micro (1395)**	
						μPD414A-1	**NEC Micro (1395,1488)**	20
						2660	Signetics	
						2660-3	Signetics	
						TMM415-4	Toshiba	
				18	-5,12	9050D	AMD	
						MM5271	**National (1333)**	
						μPD418-1	**NEC Micro (1412)**	
						SY5271	Synertek	
						TMS4050-1	TI	
						TMS4051-1	TI	30
				22	±5,12	9060D	AMD	
						EA4122-1	EA	
						MB8107E	Fujitsu	
						2107C	Intel	
						MM5281	National	
						μPD411-1	**NEC Micro (1375)**	
						μPD411-1M	**NEC Micro (1390)**	
						μPD411A-1	**NEC Micro (1382)**	
						MN1001-1	Panasonic	
						SY5281	Synertek	40
						TMS4060-1	TI	
						TMM414-1	Toshiba	
					-3,5,12	TMS4030-1	TI	
	270 nsF	NMOS	TS	18	-5,12	IM7270-12	Intersil	
						MM4270	**National (1311)**	
						MM5270-5	**National (1331)**	
				22	±5,12	EA2107B-4	EA	
						IM7280-12	Intersil	
						M58755-2	Mitsubishi	
						MM4280	**National (1314)**	50
						MM5280-5	**National (1342)**	
						M340B	SGS	
						2680-1	Signetics	
	280 nsF	NMOS	TS	16	±5,12	MB8224N	Fujitsu	
				22	±5,12	2107A-1	Intel	
	300 nsF	NMOS	TS	16	±5,12	EA4060	EA	
						M4027-5	**Fairchild (1118)**	
						4096-4	Fairchild	
						2104A-4	Intel	
						IM7005-12	Intersil	60
						MK4096-16	Mostek	
						MK4096-86	Mostek	
						MCM6604A-4	Motorola	
						μPD414	**NEC Micro (1395)**	

(Continued)

Dynamic (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
4096x1	300 nsF	NMOS	TS	16	±5,12	(Cont'd.)		
						μPD414A	**NEC Micro (1395,1488)**	
						4096-4	Rockwell	
						2660-1	Signetics	
				18	-5,12	9050C	AMD	70
						μPD418	**NEC Micro (1412)**	
						SY4050	Synertek	
						TMS4050	TI	
						TMS4051	TI	
				22	±5,12	9060C	AMD	
						EA2107B-L	EA	
						EA4122	EA	
						MB8107N	Fujitsu	
						HM4503-1	Hitachi	
						HM4507	Hitachi	80
						2107C-4	Intel	
						MCM6605A	Motorola	
						μPD411	**NEC Micro (1375)**	
						μPD411-M	**NEC Micro (1390)**	
						μPD411A	**NEC Micro (1382)**	
						MN1001	Panasonic	
						HYB4060	Siemens	
						TMS4060	TI	
					-3,5,12	TMS4030	TI	
	350 nsF	NMOS	TS	16	±5,12	4096-5	Fairchild	90
						2104A	Intel	
						IM7005-13	Intersil	
						MK4096-11	Mostek	
						MK4096-85	Mostek	
						MK4200-11	Mostek	
						MCM4096-11	Motorola	
						MCM6604A	Motorola	
						μPD414-E	**NEC Micro (1395)**	
						4096-5	Rockwell	
						2660-2	Signetics	100
				18	-5,12	IM7270-14	Intersil	
				22	±5,12	**μPD411-E**	**NEC Micro (1375)**	
						μPD411A-E	**NEC Micro (1382)**	
						M340C	SGS	
						2680-2	Signetics	
	400 nsF	NMOS	TS	18	±5,12	HM4503	Hitachi	
						2675	Signetics	
	420 nsF	NMOS	TS	22	±5,12	9107-6	AMD	
8192x1	150 nsF	NMOS	TS	22	±5,12	7008-10	Intersil	
	200 nsF	NMOS	TS	16	±5,12	2108-2	Intel	110
						2109-2	Intel	
				22	±5,12	7008-11	Intersil	
	300 nsF	NMOS	TS	16	±5,12	2108-4	Intel	
						2109-4	Intel	
16384x1	120 nsF	NMOS	TS	16	±5,12	MB8116	Fujitsu	
						MK4116-1	Mostek	
	150 nsF	NMOS	TS	16	±5,12	**F16K2**	**Fairchild (1110)**	
						MB8116H	Fujitsu	
						2117-2	Intel	
						MCM4116-15	Motorola	120
						MK4116-2	Mostek	
						μPD416-3	**NEC Micro (1402)**	
						2690-2	Signetics	
						TMS4116-15	TI	
						Z6116-2	Zilog	
	200 nsF	NMOS	TS	16	±5,12	MB8116E	Fujitsu	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–RAMs (Cont'd)

Dynamic (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
16384x1	200 nsF	NMOS	TS	16	±5,12	(Cont'd.)		
						2116-2	Intel	
						2117-3	Intel	
						MK4116-3	Mostek	
						MCM4116-20	Motorola	
						MM5290-3	**National (1344)**	
						μPD416-2	**NEC Micro (1402)**	
						2690-3	Signetics	
						TMS4116-20	TI	
						Z6116-3	Zilog	10
	250 nsF	NMOS	TS	16	±5,12	**F16K3**	**Fairchild (1110)**	
						MB8116N	Fujitsu	
						2116-3	Intel	
						2117-4	Intel	
						7116-11	Intersil	
						MK4116-4	Mostek	
						MCM4116-25	Motorola	
						MM5290-4	**National (1344)**	
						μPD416-1	**NEC Micro (1402)**	
						2690-4	Signetics	20
						TMS4116-25	TI	
						TMM416-4	Toshiba	
						Z6116-4	Zilog	
	300 nsF	NMOS	TS	16	±5,12	**F16K4**	**Fairchild (1110)**	
						2116-4	Intel	
						2117-4	Intel	
						MCM4116-30	Motorola	
						μPD416	**NEC Micro (1402)**	
	350 nsF	NMOS	TS	16	±5,12	**F16K5**	**Fairchild (1110)**	
						2116	Intel	30

Bubble Memories

92,304 Bits (641x144x1)								
				16		TBM0103	TI	

CCD Memories

910 Bits (455x2)								
				16		CCD321	Fairchild	
9216 Bits(1024x9)								
				16		CCD450A	Fairchild	
						CCD450B	Fairchild	
				18		CCD451A	Fairchild	
						CCD451B	Fairchild	
16,384 Bits (256x64x1)								
				18		2416	Intel	40
65,536 Bits(256x256)								
				18		2464	Intel	
65,536 Bits(4096x16x1)								
				16		**F464**	**Fairchild (1083)**	
						MCM0464	Motorola	
						TMS3064	TI	

Static

4x4	20 nsR	TTL	OC	16	5	25LS170C	Raytheon	
						25LS170M	†Raytheon	
			TS	16	5	25LS670C	Raytheon	50
						25LS670M	†Raytheon	
	30 nsF	TTL	OC	24	5	3104	Intel	
	30 nsR	TTL	OC	16	5	54LS170	†Raytheon	
						74LS170	Raytheon	

(Continued)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
4x4	(Cont'd.)							
	40 nsR	TTL	OC	16	5	SN54LS170	†AMD	
						SN74LS170	AMD	
						54170	†Fairchild	
						74170	Fairchild	
						54LS170	†Fairchild	60
						74LS170	Fairchild	
						ZN54170	†Ferranti	
						ZN74170	Ferranti	
						ITT74LS170	ITT	
						SN54LS170	†Motorola	
						SN74LS170	Motorola	
						DM54170	†National	
						DM74170	National	
						DM54LS170	†National	
						DM74LS170	National	70
						54170	†Raytheon	
						74170	Raytheon	
						54LS170	†Signetics	
						74LS170	Signetics	
						SN54170	†TI	
						SN74170	TI	
						SN54LS170	†TI	
						SN74LS170	TI	
			TS	16	5	SN54LS670	†AMD	
						SN74LS670	AMD	80
						54LS670	†Fairchild	
						74LS670	Fairchild	
						ITT74LS670	ITT	
						SN54LS670	†Motorola	
						SN74LS670	Motorola	
						DM54LS670	†National	
						DM74LS670	National	
						54LS670	†Raytheon	
						74LS670	Raytheon	
						54LS670	†Signetics	90
						74LS670	Signetics	
						SN54LS670	†TI	
						SN74LS670	TI	
	1 μsR	CMOS	—	24	4.5-15	MC14580BA	†Motorola	
	1.5 μsR	CMOS	—	24	3-15	MC14580BC	Motorola	
4x8	1 μsR	CMOS	—	24	3-15	CD4036B	†RCA	
						CD4039B	†RCA	
						CM4036A	†Solitron	
						CM4039A	†Solitron	
8x2	12 nsF	ECL	OE	18	-5.2	10155	Signetics	100
	14.5 nsR	ECL	—	24	-5.2	MCM10143	Motorola	
	50 nsR	TTL	TS	24	5	74S172	Signetics	
						TL74172	Telefunken	
						SN74172	TI	
8x4	40 nsF	TTL	OC	24	5	N82S12	Signetics	
			TS	24	5	N82S112	Signetics	
16x1	12 nsR	ECL	OE	14	12	HM2101	Hitachi	
	20 nsR	TTL	OC	14	5	SN5481A	†TI	
						SN7481A	TI	
				16	5	SN5484A	†TI	110
						SN7484A	TI	
	35 nsR	TTL	OC	14	5	MC4004	Motorola	
						MC4005	Motorola	
						MC4304	†Motorola	
						MC4305	†Motorola	
16x4	6 nsR	ECL	OE	16	-5.2	F10145	Fairchild	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

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MEMORY–RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source
16x4	(Cont'd.)						
	10 ns*	ECL	OE	16	-5.2	HD10145	Hitachi
	15 nsF	ECL	OE	16	-5.2	MCM10145	† Motorola
	15 nsR	16	ECL	OE	-5.2	10145	Signetics
	20 nsF	TTL	TS	18	5	9410C	Fairchild
	35 nsF	TTL	OC	16	5	AM27S02C	AMD
						SN74S289	AMD
						93404C	Fairchild
						93404M	† Fairchild
						3101A	Intel
						6560	MMI
						DM74S289	National
						N3101A	Signetics
						SN74S289	TI
			TS	16	5	AM27S03C	AMD
						SN74S189	AMD
						93405C	Fairchild
						93405M	† Fairchild
						6561	MMI
						DM74S189	**National (1292)**
						74S189	Signetics
						SN74S189	TI
	40 nsF	TTL	TS	18	5	**DM85S68**	**National (1295)**
	45 nsF	TTL	OC	16	5	AM27S02M	† AMD
						M3101A	† Intel
			TS	16	5	AM27S03M	† AMD
	50 nsF	TTL	OC	16	5	SN54S289	† AMD
						DM54S289	† National
						N82S25	Signetics
						S3101A	† Signetics
						74S89	Signetics
						SN54S289	† TI
			TS	16	5	SN54S189	† AMD
						DM54S189	**† National (1292)**
						DM8599	National
						54S189	† Signetics
						SN54S189	† TI
	55 nsF	TTL	TS	18	5	**DM75S68**	**† National (1295)**
	60 nsF	TTL	OC	16	5	3101	AMD
						3101	Intel
						5560	† MMI
						DM7489	**National (1287)**
						S82S25	† Signetics
			TS	16	5	5561	† MMI
	60 nsR	TTL	OC	16	5	SN7489	AMD
						7489	Fairchild
						HM2502	Hitachi
						IM5501C	Intersil
						IM5501M	† Intersil
						M53289	Mitsubishi
						MC4064	Motorola
						SN7489	TI
						7489	TRW
	70 nsF	TTL	OC	16	5	AM27LS02C	AMD
			TS	16	5	AM27LS03C	AMD
						DM7599	† National
						DM74LS189	**National (1289)**
	75 nsF	TTL	OC	16	5	31013	† AMD
						M3101	† Intel
	80 nsF	TTL	OC	16	5	L6560	MMI

(Continued)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source
16x4	80 nsF	TTL	OC	16	5	(Cont'd.)	
						DM5489	**† National (1287)**
						DM74LS289	National
			TS	16	5	L6561	MMI
	85 nsF	TTL	OC	16	5	AM27LS02M	† AMD
			TS	16	5	AM27LS03M	† AMD
	100 nsF	TTL	OC	16	5	L5560	† MMI
						DM54LS289	† National
			TS	16	5	L5561	† MMI
						DM54LS189	**† National (1289)**
	110 nsR	TTL	OC	16	5	31L01C	AMD
						31L01M	† AMD
	120 nsR	CMOS	TS	18	4.5-12.5	F4710BC	Fairchild
						F4710BM	† Fairchild
	280 nsR	CMOS	TS	16	3-15	HD54C89	† Harris
						HD74C89	Harris
						MM54C89	**† National (1352)**
						MM74C89	**National (1352)**
32x2	50 nsF	TTL	OC	16	5	DM86S21	National
						N82S21	Signetics
32x8	300 ns*	CMOS	TS	18	10	HCMP1824	† Hughes
						CMP1824	† RCA
	600 ns*	CMOS	TS	18	5	HCMP1824C	† Hughes
						CDP1824C	† RCA
64x1	10 nsR	ECL	OE	16	-5.2	SN10142	TI
	12 nsF	ECL	OE	16	-5.2	μPB10142	NEC America
	15 nsF	ECL	OE	16	-5.2	μPB10148	NEC America
	15 nsR	ECL	OE	16	-5.2	10140	Signetics
						10148	Signetics
						10151	Signetics
						SN10140	TI
						SN10148	TI
	270 nsR	CMOS	—	14	3-18	MCM14505BA	† Motorola
	350 nsR	CMOS	—	14	4.5-16	MCM14505BC	Motorola
64x4	200 ns*	CMOS	TS	24	5-15	SCM5555D	SSS
	700 nsF	CMOS	TS	16	5	**MM74C910**	**National (1358)**
	860 nsF	CMOS	TS	16	5	**MM54C910**	**† National (1358)**
	1.05 μsR	CMOS	TS	24	5-15	MCM14552A	† Motorola
	2.1 μsR	CMOS	TS	24	5-15	MCM14552C	Motorola
64x8	450 nsF	NMOS	TS	20	5	TMS4036-2	TI
	650 nsF	NMOS	TS	20	5	TMS4036-1	TI
	1 μsF	NMOS	TS	20	5	TMS4036	TI
64x9	45 nsF	TTL	OC	28	5	93419C	Fairchild
						N82S09	Signetics
	60 nsF	TTL	OC	28	5	93419M	† Fairchild
	80 nsF	TTL	OC	28	5	S82S09	† Signetics
128x1	12 nsR	ECL	OE	16	-5.2	MCM10147	Motorola
						GXB10147	Siemens
	14 nsF	ECL	OE	16	-5.2	MB7047	Fujitsu
	15 nsF	ECL	OE	16	-5.2	F10405C	Fairchild
	15 nsR	ECL	OE	16	-5.2	10147	Signetics
						SN10147	TI
128x8	150 ns*	CMOS	—	24	5	MWS5080	RCA
	200 ns*	CMOS	TS	24	10	CDP1823S	RCA

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
128x8	(Cont'd.)							
	250 ns*	NMOS	TS	24	5	MCM68B10	Motorola	
	350 nsF	NMOS	TS	24	5	MCM6810A	Motorola	
	350 ns*	CMOS	TS	24	5	CDP1823SC	RCA	
	360 nsF	NMOS	TS	24	5	MCM68A10	Motorola	
	450 nsF	NMOS	TS	24	5	MCM6810A-1	Motorola	
	1 µsF	NMOS	TS	24	5	**S6810**	**AMI** (1061)	
128x9	500 nsF	CMOS	TS	22	5	MN1101	Panasonic	
256x1	15 nsF	ECL	OE	16	-5.2	F100414	Fairchild	
						F10414	Fairchild	10
						MB7042	Fujitsu	
						MCM10152	Motorola	
	25 nsF	ECL	OE	16	-5.2	µPB10144	NEC America	
	26 nsR	ECL	OE	16	-5.2	MCM10144	Motorola	
	30 nsF	ECL	OE	16	-5.2	F10410C	Fairchild	
						10144	Signetics	
	30 nsR	ECL	OE	16	-5.2	SP10144	Plessey	
	35 nsF	ECL	OE	16	-4.25	F10411C	Fairchild	
					-5.2	MBM10410	Fujitsu	
						HM2105	Hitachi	20
						RC10144	Raytheon	
		TTL	TS	16	5	AM27LS00AC	AMD	
	35 nsR	ECL	OE	16	-5.2	SN10144	TI	
	40 nsF	ECL	OE	16	-5.2	RI10144	Raytheon	
		TTL	OC	16	5	N82S117	Signetics	
			TS	16	5	93421AC	Fairchild	
						93421AC	Raytheon	
						N82S116	Signetics	
	45 nsF	TTL	OC	16	5	AM27LS01C	AMD	
						AM29720C	AMD	30
						93410AC	Fairchild	
						93411AC	Fairchild	
						93411AC	Raytheon	
			TS	16	5	AM27LS00C	AMD	
						AM27LS00AM	† AMD	
						AM29721C	AMD	
						93L420C	Fairchild	
	50 nsF	TTL	OC	16	5	N82S17	Signetics	
						74S301	Signetics	
			TS	16	5	93421C	Fairchild	40
						DM74S200	National	
						RC5340	Raytheon	
						93421C	Raytheon	
						N82S16	Signetics	
						74S200	Signetics	
						74S201	Signetics	
	55 nsF	TTL	OC	16	5	AM27LS01M	† AMD	
						AM29720M	† AMD	
						93411C	Fairchild	
						6530	MMI	50
						RC5330	Raytheon	
						93411C	Raytheon	
			TS	16	5	AM27LS00M	† AMD	
						AM29721M	† AMD	
						93L420M	† Fairchild	
						6531	MMI	
	60 nsF	TTL	OC	16	5	AM27S01BC	AMD	

(Continued)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
256x1	60 nsF	TTL	OC	16	5	(Cont'd.)		
						93410C	Fairchild	
						IM5503AC	Intersil	60
						IM5533AC	Intersil	
						DM74S206	**National** (1297)	
			TS	16	5	AM27S00BC	AMD	
						93421M	† Fairchild	
						IM5523AC	Intersil	
						93421M	† Raytheon	
	65 nsF	TTL	OC	16	5	93411M	† Fairchild	
						93411M	† Raytheon	
						SN54S301A	† TI	
			TS	16	5	HM2505	Hitachi	70
						SN74LS201	TI	
	70 nsF	TTL	OC	16	5	93410M	† Fairchild	
						IM5503AM	† Intersil	
						IM5533AM	† Intersil	
						5530	† MMI	
						S82S17	† Signetics	
						54S301	† Signetics	
			TS	16	5	IM5523AM	† Intersil	
						5531	† MMI	
						DM54S200	† National	80
						RM5340	† Raytheon	
						S82S16	† Signetics	
						54S200	† Signetics	
						54S201	† Signetics	
	75 nsF	TTL	OC	16	5	RM5330	† Raytheon	
	80 nsF	TTL	OC	16	5	AM27LS01LC	AMD	
						IM5503C	Intersil	
						IM5533C	Intersil	
						DM54S206	† **National** (1297)	
			TS	16	5	AM27LS00LC	AMD	90
						IM5523C	Intersil	
	80 nsR	TTL	OC	16	5	IM5503M	† Intersil	
						IM5533M	† Intersil	
			TS	16	5	IM5523M	† Intersil	
	90 nsF	TTL	TS	16	5	93L421C	Fairchild	
	95 nsF	TTL	OC	16	5	AM27LS01LM	† AMD	
			TS	16	5	AM27LS00LM	† AMD	
	100 nsF	CMOS	TS	16	3-15	SCM5520S	† SSS	
		TTL	TS	16	5	93L421M	† Fairchild	
	115 nsF	TTL	OC	16	5	L6530	MMI	100
			TS	16	5	L6531	MMI	
	130 nsF	TTL	OC	16	5	L5530	† MMI	
			TS	16	5	L5531	† MMI	
	150 ns*	CMOS	TS	16	10	CD40061A	† RCA	
	200 ns*	CMOS	TS	16	4.5-12.5	F4720C	Fairchild	
						F4720M	† Fairchild	
					3-15	F4720AC	Fairchild	
	300 ns*	CMOS	TS	16	5	CD40061	RCA	
	380 nsR	CMOS	TS	16	3-15	CD4061A	† RCA	
	400 nsR	CMOS	TS	16	3-15	HD54C200	† Harris	110
						HD74C200	Harris	
						MM54C200	† **National** (1355)	
						MM74C200	**National** (1355)	
	500 nsR	CMOS	—	16	3-7	IM6523C	Intersil	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY–RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
256x1	500 nsR	CMOS	—	16	3-7	(Cont'd.) IM6523M	† Intersil	
		PMOS	TS	16	-9,5	MM1101A2	National	
	650 nsF	PMOS	TS	16	-9,5	MM4250	† National	
	900 nsF	PMOS	—	16	-12,5	MK4007	Mostek	
	1 µsF	PMOS	TS	16	-9.5	MM1101A1 2501	National Signetics	
					-12,5	25L01	Signetics	
	1 µsR	PMOS	TS	16	-9,5	1101A1 1101A1	AMD Intel	10
	1.4 µsR	CMOS	—	16	3-15	MCM14537A	† Motorola	
	1.5 µsF	PMOS	TS	16	-9,5	1101A 1101AM 1101A MM1101A	AMD † AMD Intel National	
	2 µsR	CMOS	—	16	3-15	MCM14537C	Motorola	
256x4	10 nsF	ECL	OE	22	-5.2	MB7072H	Fujitsu	
				24	-5.2	MB7017H	Fujitsu	
	15 nsF	ECL	OE	22	-5.2	MB7072N	Fujitsu	
				24	-5.2	MB7071N	Fujitsu	20
	40 nsR	TTL	TS	16	5	SN54S207 SN74S207	† TI TI	
				20	5	SN54S208 SN74S208	† TI TI	
	45 nsF	TTL	OC	22	5	93412C	Fairchild	
			TS	22	5	**93422C**	**Fairchild** (1132)	
	60 nsF	TTL	OC	22	5	93L412C 93412M	Fairchild † Fairchild	
			TS	22	5	**93L422C** **93422M**	**Fairchild** (1132) **† Fairchild** (1132)	30
	75 nsF	TTL	OC	22	5	93L412M	† Fairchild	
			TS	22	5	**93L422M**	**† Fairchild** (1132)	
	75 nsR	TTL	TS	16	5	SN54LS207	† TI	
				20	5	SN54LS208	† TI	
	80 ns*	CMOS	TS	22	5	MWS5040A	RCA	
	90 ns*	CMOS	TS	22	10	MWS5040	RCA	
	100 nsR	CMOS	TS	16	4-11	**HM6562A-2** **HM6562A-9**	**† Harris** (1183) **Harris** (1183)	
				18	4-11	**HM6561A-2** **HM6561A-9**	**† Harris** (1182) **Harris** (1182)	40
				22	4-11	**HM6551A-2** **HM6551A-9**	**† Harris** (1175) **Harris** (1175)	
	150 nsF	NMOS	TS	16	5	SY21H12-1	Synertek	
				18	5	SY21H11-1	Synertek	
				22	5	SY21H01-1	Synertek	
	160 nsR	CMOS	TS	16	4-11	**HM6562C-2** **HM6562C-9**	**† Harris** (1183) **Harris** (1183)	
				18	4-11	**HM6561C-2** **HM6561C-9**	**† Harris** (1182) **Harris** (1182)	
				22	4-11	**HM6551C-2** **HM6551C-9**	**† Harris** (1175) **Harris** (1175)	50
	175 nsF	NMOS	TS	16	5	SY21H12	Synertek	
				18	5	SY21H11	Synertek	
				22	5	SY21H01	Synertek	
	180 nsR	CMOS	TS	22	10	IM6551AC IM6551AM	Intersil † Intersil	
	200 nsF	NMOS	TS	16	5	SY21H12-2	Synertek	
				18	5	SY21H11-2	Synertek	
				22	5	SY21H01-2	Synertek	60
	200 ns*	CMOS	TS	22	10	CDP1822S	RCA	
	250 nsF	CMOS	TS	18	5	**MM74C921**	**National** (1361)	
				22	5	**MM74C920**	**National** (1361)	
		NMOS	TS	16	5	9112D MB8112E 2112A-2 MM2112A-2 MM2112A-2L SY2112A-2	AMD Fujitsu Intel National National Synertek	
				18	5	9111D MB8111E 2111A-2 MM2111A-2 MM2111A-2L **µPD2111AL-2** SY2111A-2	AMD Fujitsu Intel National National **NEC Micro** (1433) Synertek	70
				22	5	9101D MB8101E 2101A-2 MM2101A-2 MM2101A-2L **µPD2101AL-2** SY2101A-2	AMD Fujitsu Intel National National **NEC Micro** (1424) Synertek	80
	275 nsF	CMOS	TS	18	5	**MM54C921**	**† National** (1361)	
				22	5	**MM54C920**	**† National** (1361)	
	300 nsF	CMOS	TS	16	5	**HM6562B-2** **HM6562B-9**	**† Harris** (1183) **Harris** (1183)	
				18	5	**HM6561B-2** **HM6561B-9**	**† Harris** (1182) **Harris** (1182)	
				22	5	**HM6501B-2** **HM6501B-9** **HM6551B-2** **HM6551B-9**	**† Harris** (1174) **Harris** (1174) **† Harris** (1175) **Harris** (1175)	90
		NMOS	TS	16	5	91L12C 9112C 9112CM EA2112	AMD AMD † AMD EA	
				18	5	91L11C 9111C 9111CM EA2111	AMD AMD † AMD EA	100
				22	5	91L01C 9101C 9101CM EA2101	AMD AMD † AMD EA	
	350 nsF	NMOS	TS	16	5	2112A MM2112A MM2112A-L 2112 SY2112A	Intel National National Signetics Synertek	110
				18	5	2111A MM2111	Intel National	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
256x4	350 nsF	NMOS	TS	18	5	(Cont'd.)		
						MM2111A-L	National	
						µPD2111AL	**NEC Micro (1433)**	
						2111	Signetics	
						SY2111A	Synertek	
				22	5	3538F	Fairchild	
						2101A	Intel	
						MM2101A	National	
						MM2101A-L	National	
						µPD2101AL	**NEC Micro (1424)**	10
						2101	Signetics	
						SY2101A	Synertek	
	350 ns*	CMOS	TS	22	5	CDP1822SC	RCA	
	400 nsF	NMOS	TS	16	5	91L12B	AMD	
						9112B	AMD	
						9112BM	†AMD	
						EA2112M	†EA	
						2612	Signetics	
				18	5	91L11B	AMD	
						9111B	AMD	20
						9111BM	†AMD	
						EA2111M	†EA	
						2611	Signetics	
				22	5	91L01B	AMD	
						9101B	AMD	
						9101BM	†AMD	
						EA2101M	†EA	
						2601	Signetics	
	425 nsF	CMOS	TS	16	5	**HM6562-9**	**Harris (1183)**	
				18	5	**HM6561-9**	**Harris (1182)**	30
				22	5	**HM6501-9**	**Harris (1174)**	
						HM6551-9	**Harris (1175)**	
	450 nsF	CMOS	TS	22	5	S5101L-1	AMI	
						S5101L-2	AMI	
						S5101-1	**AMI (1041)**	
						S5101-2	**AMI (1041)**	
						5101-1	Intel	
						5101L-1	Intel	
						µPD5101L-1	**NEC Micro (1443)**	
		NMOS	TS	16	5	MB8112N	Fujitsu	40
						2112A-4	Intel	
						MM2112A-4	National	
						MM2112A-4L	National	
						2112-4	Signetics	
						SY2112A-4	Synertek	
						TMS4043-2	TI	
				18	5	MB8111N	Fujitsu	
						2111A-4	Intel	
						MM2111-4	National	
						MM2111A-4	National	50
						µPD2111AL-4	**NEC Micro (1433)**	
						2111-4	Signetics	
						SY2111A-4	Synertek	
						TMS2111-1	TI	
						TMS4042-2	TI	
				22	5	3538-1	Fairchild	
						MB8101N	Fujitsu	
						2101A-4	Intel	
						MM2101A-4	National	
						MM2101A-4L	National	60
						µPD2101AL-4	**NEC Micro (1424)**	
						2101-4	Signetics	
						SY2101A-4	Synertek	

(Continued)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
256x4	450 nsF	NMOS	TS	22	5	(Cont'd.)		
						TMS2101-1	TI	
						TMS4039-2	TI	
	475 nsF	CMOS	TS	16	5	**HM6562-2**	**†Harris (1183)**	
				18	5	**HM6561-2**	**†Harris (1182)**	
				22	5	**HM6501-2**	**†Harris (1174)**	
						HM6551-2	**†Harris (1175)**	70
	500 nsF	NMOS	TS	16	5	2112-1	AMD	
						91L12A	AMD	
						9112A	AMD	
						9112AM	†AMD	
						2606-1	Signetics	
						SY2112-1	Synertek	
				18	5	2111-1	AMD	
						91L11A	AMD	
						9111A	AMD	
						9111AM	†AMD	80
						MM2111-1	National	
						SY2111-1	Synertek	
				22	5	2101-1	AMD	
						91L01A	AMD	
						9101A	AMD	
						9101AM	†AMD	
						MM2101-1	National	
						MM5269-1	**National (1317)**	
						SY2101-1	Synertek	
				24	5	RA3-4256	GI	90
	530 nsF	CMOS	TS	22	5	IM6551C	Intersil	
						IM6551M	†Intersil	
	550 nsF	CMOS	TS	22	5	TC5007-1	Toshiba	
						TC5017-1	Toshiba	
	650 nsF	CMOS	TS	22	5	**S5101**	**AMI (1041)**	
						S5101-3	**AMI (1041)**	
						S5101L	AMI	
						S5101L-3	AMI	
						5101	Intel	
						5101L	Intel	100
						5101-3	Intel	
						5101L-3	Intel	
						µPD5101L	**NEC Micro (1443)**	
						SY5101	Synertek	
		NMOS	TS	16	5	2112-2	AMD	
						MM2112A-6	National	
						MM2112A-6L	National	
						2112-6	Signetics	
						SY2112-2	Synertek	
						TMS2112-2	TI	110
						TMS4043-1	TI	
						TMM312-1	Toshiba	
				18	5	2111-2	AMD	
						MM2111A-6	National	
						MM2111A-6L	National	
						2111-6	Signetics	
						SY2111-2	Synertek	
						TMS2111-2	TI	
						TMS4042-1	TI	
						TMM311-1	Toshiba	120
				22	5	2101-2	AMD	
						RA3-4265B	EMM/Semi	
						3538-2	Fairchild	
						RA3-4256B	GI	
						MM2101A-6	National	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY–RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
256x4	650 nsF	NMOS	TS	22	5	(Cont'd.)		
						MM2101A-6L	National	
						2101-6	Signetics	
						SY2101-2	Synertek	
						TMS2101-2	TI	
						TMS4039-1	TI	
				24	5	RA3-4256A	EMM/Semi	
						RA3-4256A	GI	
	750 nsF	NMOS	TS	16	5	2606	Signetics	
	800 nsF	CMOS	TS	22	5	**S5101-8**	**AMI (1041)**	10
						5101-8	Intel	
						M5101-4	Intel	
						M5101L-4	Intel	
						μPD5101-E	**NEC Micro (1438)**	
						TC5007-2	Toshiba	
						TC5017-2	Toshiba	
	1 μsF	NMOS	TS	16	5	2112	AMD	
						2112	Signetics	
						SY2112	Synertek	
						TMS2112	TI	20
						TMS4043	TI	
						TMM312	Toshiba	
				18	5	2111	AMD	
						2111	Signetics	
						SY2111	Synertek	
						TMS2111	TI	
						TMS4042	TI	
						TMM311	Toshiba	
				22	5	2101	AMD	
						RA3-4256B	EMM/Semi	30
						2101	Signetics	
						SY2101	Synertek	
						TMS2101	TI	
						TMS4039	TI	
256x8	60 nsF	TTL	TS	22	5	N82S208	Signetics	
	400 nsF	NMOS	TS	22	5	**35391**	**EMM/Semi (1074)**	
						3539-1	Fairchild	
	500 nsF	NMOS	TS	22	5	**35392**	**EMM/Semi (1074)**	
						3539-2	Fairchild	
	650 nsF	NMOS	TS	22	5	**3539**	**EMM/Semi (1076)**	40
						3539	Fairchild	
256x9	60 nsF	TTL	TS	22	5	N82S210	Signetics	
512x1	200 nsF	CMOS	—	16	10	S2222	AMI	
						2222	Nortec	
						SCM5522	SSS	
	400 nsF	CMOS	—	16	10	S2222A	AMI	
						2222A	Nortec	
1024x1	20 nsF	ECL	OE	16	-5.2	**F10415AC**	**Fairchild (1128)**	
	29 nsF	ECL	OE	16	-5.2	MCM10145	Motorola	
						MCM10416	Motorola	50
	30 nsF	TTL	OC	16	5	**93415AC**	**Fairchild (1137)**	
						N82S110	Signetics	
						N93415A	Signetics	
			TS	16	5	93425AC	Fairchild	
						N82S111	Signetics	
						N93425A	Signetics	
	30 ns*	TTL	OC	16	5	DM93415A	National	
			TS	16	5	DM93425A	National	
	35 nsF	ECL	OE	16	-5.2	MBM10415A	Fujitsu	

(Continued)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x1	(Cont'd.)							60
	35 nsR	ECL	—	24	-4.5	**F100415C**	**Fairchild (1128)**	
			OE	16	-5.2	**F10415C**	**Fairchild (1128)**	
	35 ns*	TTL	OC	16	5	RM5500	† Raytheon	
						RC5500	Raytheon	
	40 nsF	TTL	OC	16	5	N82S10	Signetics	
	45 nsF	NMOS	OC	16	5	MBM2115Y	Fujitsu	
						2115A	Intel	
						2115AL	Intel	
						2115A	Signetics	
						2115AL	Signetics	70
			TS	16	5	MBM2125Y	Fujitsu	
						2125A	Intel	
						2125AL	Intel	
						2125A	Signetics	
						2125AL	Signetics	
		VMOS	OC	16	5	**S4015**	**AMI (1032)**	
		TTL	OC	16	5	93415A	AMD	
						93415C	**Fairchild (1137)**	
						93415M	**† Fairchild (1137)**	
						IM55S08AC	Intersil	80
						μPB2205	**NEC Micro (1418)**	
						93415AC	Raytheon	
						N93415A	Signetics	
			TS	16	5	**93425C**	**Fairchild (1137)**	
						93425M	**† Fairchild (1137)**	
						MBM93415A	Fujitsu	
						IM55S18AC	Intersil	
						93425AC	Raytheon	
						N82S11	Signetics	
						N93425	Signetics	90
	50 nsF	TTL	OC	16	5	**μPB2205**	**NEC Micro (1418)**	
						SN74S314A	TI	
			TS	16	5	SN74S214A	TI	
	55 nsF	NMOS	OC	16	5	M2115A	† Intel	
			TS	16	5	M2125A	† Intel	
	60 nsF	ECL	OE	16	-5.2	MBM10415	Fujitsu	
		NMOS	—	22	-3,7,15	IM7001-12	Intersil	
						MCM7001	Motorola	
						7001	Nortec	
						MW7001	RCA	100
		TTL	OC	16	5	**93L415C**	**Fairchild (1137)**	
			TS	16	5	**93L425C**	**Fairchild (1137)**	
	65 nsF	TTL	OC	16	5	S82S10	† Signetics	
			TS	16	5	S82S11	† Signetics	
	70 nsF	NMOS	OC	16	5	**S4015-2**	**AMI (1032)**	
						MBM2115H	Fujitsu	
						2115-2	Intel	
						2115A-2	Intel	
						2115AL-2	Intel	
			TS	16	5	**S4025-2**	**AMI (1032)**	110
						MBM2125H	Fujitsu	
						2125-2	Intel	
						2125A-2	Intel	
						2125AL-2	Intel	
				18	-3,5,15	1802	EMM/Semi	
		TTL	OC	16	5	93415C	AMD	
						93L415M	**† Fairchild (1137)**	
						MBM93415	Fujitsu	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x1	70 nsF	TTL	OC	16	5	(Cont'd.)		
						HM2510	Hitachi	
						IM55S08C	Intersil	
						DM93415	National	
						93415C	Raytheon	
						S82S10	† Signetics	
						SN74S314	TI	
			TS	16	5	**93L425M**	**† Fairchild (1137)**	
						IM55S18C	Intersil	
						DM93425	National	10
						93425C	Raytheon	
						S82S11	† Signetics	
						SN74S214	TI	
			--	22	-3,7,15	IM7001-15	Intersil	
	75 nsF	NMOS	OC	16	5	M2115AL	† Intel	
			TS	16	5	M2125AL	† Intel	
		TTL	OC	16	5	93415M	† AMD	
						IM55S08M	† Intersil	
			TS	16	5	IM55S18M	† Intersil	
	75 nsR	TTL	OC	16	5	93415M	† Raytheon	20
			TS	16	5	93425M	† Raytheon	
	75 ns*	TTL	OC	16	5	SN54LS315	† TI	
						SN74LS315	TI	
			TS	16	5	SN54LS215	† TI	
						SN74LS215	TI	
	80 nsF	NMOS	—	22	-3,7,15	IM7001-16	Intersil	
	80 ns*	CMOS	TS	16	5	MWS5001A	RCA	
	90 nsF	NMOS	TS	18	-3.5,5,15	1801	EMM/Semi	
	90 ns*	CMOS	TS	16	10	MWS5501	RCA	
	95 nsF	NMOS	OC	16	5	**S4015**	**AMI (1032)**	30
						MBM2115E	Fujitsu	
						2115	Intel	
						2115L	Intel	
			TS	16	5	**S4025**	**AMI (1032)**	
						MBM2125E	Fujitsu	
						2125	Signetics	
						2125L	Signetics	
		TTL	OC	16	5	SN74LS314	TI	
			TS	16	5	SN74LS214	TI	
	95 nsR	CMOS	TS	16	10	IM6508A-1	Intersil	40
				18	10	IM6518A-1	Intersil	
	100 nsR	CMOS	TS	16	4-11	**HM6508A-2**	**† Harris (1180)**	
						HM6508A-9	**Harris (1180)**	
				18	4-11	**HM6518A-2**	**† Harris (1181)**	
						HM6518A-9	**Harris (1181)**	
		NMOS	OC	16	5	IM5508C	Intersil	
	120 nsF	NMOS	OC	16	5	MBM2115N	Fujitsu	
			TS	16	5	MBM2125N	Fujitsu	
	140 nsF	TTL	OC	16	5	SN54LS314	† TI	
			TS	16	5	SN54LS214	† TI	50
	150 nsF	NMOS	TS	16	5	3542	Fairchild	
						SY21H02-1	Synertek	
						SYMC21H02-1	† Synertek	
	150 nsR	CMOS	TS	16	10	IM6508A	Intersil	
				18	10	IM6518A	Intersil	

(Continued)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x1	(Cont'd.)							
	150 ns*	CMOS	TS	16	5	MWS5001	RCA	
	160 nsR	CMOS	TS	16	4-11	**HM6508C-2**	**† Harris (1180)**	
						HM6508C-9	**Harris (1180)**	
				18	4-11	**HM6518C-2**	**† Harris (1181)**	60
						HM6518C-9	**Harris (1181)**	
	175 nsF	NMOS	TS	16	5	SY21H02	Synertek	
	200 nsF	CMOS	TS	16	4-11	**S6508A**	**AMI (1046)**	
		NMOS	TS	16	5	3524A	Fairchild	
						SY21H02-2	Synertek	
						SYMC21H02-2	† Synertek	
	200 ns*	CMOS	TS	16	10	CDP1821S	RCA	
	250 nsF	CMOS	TS	16	3-10	IM6508C	Intersil	
						IM6508M	† Intersil	
						μPD6508-1	**NEC Micro (1488)**	70
					5	**MM74C929**	**National (1363)**	
				18	3-10	IM6518C	Intersil	
						IM6518M	† Intersil	
					5	**MM74C930**	**National (1363)**	
		NMOS	TS	16	5	9102D	AMD	
						2102H	Fairchild	
						2102HM	† Fairchild	
						2102LH	Fairchild	
						2102LHM	† Fairchild	
						21L02H	Fairchild	80
						2102A-2	Intel	
						2102AL-2	Intel	
						MM2102A-2	**National (1300)**	
						MM2102A-2L	**National (1300)**	
						μPD2102AL-2	**NEC Micro (1429)**	
						2102A-2	Signetics	
						21F02-2	Signetics	
						2101AL-2	Signetics	
						TMM313-1	Toshiba	
	275 nsF	CMOS	TS	16	5	**MM54C929**	**† National (1363)**	90
				18	5	**MM54C930**	**† National (1363)**	
		NMOS	TS	16	5	SY4102-6	Synertek	
	300 nsF	CMOS	TS	16	5	**S6508-1**	**AMI (1046)**	
						IM6508-1	Intersil	
						μPD6508	**NEC Micro (1488)**	
				18	5	IM6518-1	Intersil	
		NMOS	TS	16	5	91L02C	AMD	
						91L02CM	† AMD	
						9102C	AMD	
						9102CM	† AMD	100
	305 nsF	CMOS	TS	16	5	**HM6508B-2**	**† Harris (1180)**	
						HM6508B-9	**Harris (1180)**	
				18	5	**HM6518B-2**	**† Harris (1181)**	
						HM6518B-9	**Harris (1181)**	
	350 nsF	NMOS	TS	16	5	2102F	Fairchild	
						2102FM	† Fairchild	
						2102LF	Fairchild	
						21L02F	Fairchild	
						2102A	Intel	
						2102AL	Intel	110
						MM2102A	**National (1300)**	
						MM2102AL	**National (1300)**	
						μPD2102AL	**NEC Micro (1429)**	
						2102A	Signetics	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

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MEMORY–RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x1	350 nsF	NMOS	TS	16	5	(Cont'd.)		
						2102AL	Signetics	
						21F02	Signetics	
						21L02	Signetics	
						SY2102A	Synertek	
						SYMC2102A	†Synertek	
						TMM313	Toshiba	
	300 ns*	CMOS	TS	16	5	CDP1821SC	RCA	
	350 nsR	CMOS	TS	16	4-11	**S6508A**	**AMI** (1046)	
	400 nsF	NMOS	TS	16	5	91L02B	AMD	10
						9102B	AMD	
						91L02BM	†AMD	
						9102BM	†AMD	
						21L02-3	Signetics	
						SY21L02B	Synertek	
						SYMC21L02B	†Synertek	
	425 nsF	CMOS	TS	16	5	**HM6508-9**	**Harris** (1180)	
				18	5	**HM6518-9**	**Harris** (1181)	
	450 nsF	NMOS	TS	16	5	21021	Fairchild	
						21021M	†Fairchild	20
						2102L1	Fairchild	
						2102L1M	†Fairchild	
						21L021	Fairchild	
						MB8102	Fujitsu	
						2102A-4	Intel	
						M2102A-4	†Intel	
						2102AL-4	Intel	
						M58751	Mitsubishi	
						MK4102-1	Mostek	
						MK4102-11	Mostek	30
						MM2102A-4	**National** (1300)	
						MM2102AL-4	**National** (1300)	
						μPD2102AL-4	**NEC Micro** (1429)	
						2102-4	Signetics	
						2102A-4	Signetics	
						2102AL-4	Signetics	
						21F02-4	Signetics	
						TMS2102-1	TI	
						TMS4033	TI	
	460 nsF	CMOS	TS	16	5	**S6508**	**AMI** (1046)	40
						IM6508	Intersil	
				18	5	IM6518	Intersil	
	465 nsF	CMOS	TS	16	5	**HM6508-2**	**†Harris** (1180)	
				18	5	**HM6518-2**	**†Harris** (1181)	
	500 nsF	NMOS	TS	16	5	2102-1	AMD	
						9102A	AMD	
						9102AM	†AMD	
						91L02A	AMD	
						91L02AM	†AMD	
						MM2102-1	National	50
						M330C	SGS	
						SY21L02-1	Synertek	
						SYMC21L02-1	†Synertek	
	550 nsF	CMOS	TS	16	5	TC5016-1	Toshiba	
	650 nsF	CMOS	TS	16	5	**HM6508D**	**Harris** (1180)	
						SY5102-3	Synertek	
				18	5	**HM6518D**	**Harris** (1181)	
		NMOS	TS	16	5	2102-2	AMD	
						91L02	AMD	
						21022	Fairchild	60
						21022M	†Fairchild	
						2102L2	Fairchild	

(Continued)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x1	650 nsF	NMOS	TS	16	5	(Cont'd.)		
						2102L2M	†Fairchild	
						21L022	Fairchild	
						2102A-6	Intel	
						M2102A-6	†Intel	
						MM2102A-6	**National** (1300)	
						MM2102AL-6	**National** (1300)	
						M330B	SGS	70
						21L02-6	Signetics	
						2102-6	Signetics	
						2102A-6	Signetics	
						TMS2102-2	TI	
						TMS4034	TI	
	800 nsF	CMOS	TS	16	5	SIL1902A	Mitel	
						SIL1902AF	†Mitel	
						TC5016-2	Toshiba	
	1 μsF	NMOS	TS	16	5	2102	AMD	
						MK4102	Mostek	80
						MK4102-12	Mostek	
						MM2102-MD	†National	
						21L02-1	Signetics	
						2102-1	Signetics	
						SY2102	Synertek	
						SY21L02	Synertek	
						TMS2102	TI	
						TMS4035	TI	
1024x4	80 nsF	NMOS	TS	18	5	9135J	AMD	
	100 nsF	NMOS	TS	18	5	9135H	AMD	90
	120 nsF	NMOS	TS	18	5	9135G	AMD	
		VMOS	TS	18	5	S2114	AMI	
						S4016	**AMI** (1035)	
	150 nsF	CMOS	TS	18	5	MD4114	Mitel	
		NMOS	TS	18	5	9135F	AMD	
						MB8114	Fujitsu	
						TMS4045-15	TI	
				20	5	TMS4047-15	TI	
				22	±5,12	**4104B**	**EMM/Semi** (1070)	
	200 nsF	NMOS	TS	18	5	2114-2	Fairchild	100
						2114L-2	Fairchild	
						2114-2	Intel	
						2114L-2	Intel	
						IM7114L-2	Intersil	
						MK4414-3	Mostek	
						MCM2114-20	Motorola	
						MCM21L14-20	Motorola	
						MM2114L-2	**National** (1303)	
						μPD2114-2	**NEC Micro** (1489)	
						2614-20	Signetics	110
						TMS4045-20	TI	
				20	5	2142-2	Intel	
						2142L-2	Intel	
						TMS4047-20	TI	
				22	5	9130EC	AMD	
						S9130EC	AMI	
					±5,12	**4104**	**EMM/Semi** (1070)	
						M4104AS	**EMM/Semi** (1070)	
	250 nsF	NMOS	TS	18	5	IM7114-11	Intersil	
						MK4114-4	Mostek	120
						MCM2114-25	Motorola	
						MCM21L14-25	Motorola	
						SY5255	Synertek	
						TMS4045-25	TI	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x4	250 nsF	NMOS	TS	18	5	(Cont'd.)		
						TMM314-1	Toshiba	
				20	5	TMS4047-25	TI	
				22	5	91L30DC	AMD	
					±5,12	**M4104UM**	**† EMM/Semi (1070)**	
	300nsF	NMOS	TS	18	5	2114-3	Fairchild	
						2114C-3	Fairchild	
						2114-3	Intel	
						2114L-3	Intel	
						IM7114L-3	Intersil	10
						MK4114-5	Mostek	
						MCM2114-30	Motorola	
						MCM21L14-30	Motorola	
						MM2114L-3	**National (1303)**	
						μPD2114-1	**NEC Micro (1489)**	
						2614-30	Signetics	
						SY2114-3	Synertek	
				20	5	TMS4045-30	TI	
						2142-3	Intel	
						2142L-3	Intel	20
						TMS4047-30	TI	
				22	5	91L30CC	AMD	
						91L30CM	† AMD	
						9130CC	AMD	
						9130CM	† AMD	
						S9130CC	AMI	
						S9130CM	† AMI	
	300 ns*	CMOS	TS	18	5	**HM6514-5**	**Harris (1178)**	
						HM6514-2	**† Harris (1178)**	
	350 nsF	NMOS	TS	18	5	MK4114-6	Mostek	
	400 nsF	NMOS	TS	18	5	**4804B**	**EMM/Semi (1074)**	
				22	5	91L30BC	AMD	
						91L30BM	† AMD	
						9130BC	AMD	
						9130BM	† AMD	
						S9130BC	AMI	
						S9130BM	† AMI	
	450 nsF	NMOS	TS	18	5	**2114**	**EMM/Semi (1078)**	
						L2114	**EMM/Semi (1078)**	
						4804A	**EMM/Semi (1074)**	
						2114	Fairchild	
						2114L	Fairchild	
						2114	Intel	40
						2114L	Intel	
						MCM2114-45	Motorola	
						MCM21L14-45	Motorola	
						MM2114L	**National (1303)**	
						μPD2114	**NEC Micro (1489)**	
						R2114	Rockwell	
						2614-45	Signetics	
						SY2114	Synertek	
						TMS4045-45	TI	
						TMM314	Toshiba	50
				20	5	2142	Intel	
						2142L	Intel	
						TMS4047-45	TI	
	500 nsF	NMOS	TS	22	5	91L30AC	AMD	
						91L30AM	† AMD	
						9130AC	AMD	
						9130AM	† AMD	
						S91L30AC	AMI	
						S91L30AM	† AMI	60

(Continued)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x4	(Cont'd.)							
	550 nsF	CMOS	TS	20	5	TC5047-1	Toshiba	
	600 nsF	NMOS	TS	22	5	**4804U**	**EMM/Semi (1074)**	
	800 nsF	CMOS	TS	20	5	TC5047	Toshiba	
1024x8	300 nsF	NMOS	TS	22	5	**8108A**	**EMM/Semi (1080)**	
				24	5	**8308A**	**EMM/Semi (1080)**	
2048x1	60 nsF	NMOS	—	22	-3,7,15	IM7003	Intersil	
4096x1	30ns*	ECL	—	18	-5.2	**F10470C**	**Fairchild (1125)**	70
	50 nsF	TTL	OC	18	5	**93470C**	**Fairchild (1146)**	
			TS	18	5	**93471C**	**Fairchild (1146)**	
	55 nsF	NMOS	TS	18	5	2147-3	Intel	
	60 nsF	TTL	OC	18	5	**93470M**	**Fairchild (1146)**	
			TS	18	5	**93471M**	**† Fairchild (1146)**	
	70 nsF	NMOS	TS	18	5	2147	Intel	
						2147L	Intel	
						μPB2401	**NEC Micro (1489)**	
	80 nsF	NMOS	TS	18	5	9145J	AMD	
	100 nsF	NMOS	TS	18	5	9145H	AMD	80
						Z6104-1	Zilog	
				22	±5,12	**μPD410-2**	**NEC Micro (1420)**	
	120 nsF	NMOS	TS	18	5	9145G	AMD	
		VMOS	TS	18	5	**S4017**	**AMI (1038)**	
	125 nsF	NMOS	TS	18	-5,12	4402B	EMM/Semi	
	150 nsF	NMOS	TS	18	5	9145S	AMD	
						2141	Intel	
						2613-5	Signetics	
						TMS4044-15	TI	
						Z6104-2	Zilog	90
				22	5	TMS4046-15	TI	
					-5,12	4402A	EMM/Semi	
					±5,12	**4200B**	**EMM/Semi (1072)**	
						μPD410-1	**NEC Micro (1420)**	
	200 nsF	NMOS	TS	18	5	2141-2	Intel	
						IM7141-2	Intersil	
						IM7141L-2	Intersil	
						MK4104-3	Mostek	
						MCM2141-20	Motorola	
						MM5257-2	**National (1319)**	100
						μPD4104	**NEC Micro (1490)**	
						2613-20	Signetics	
						TMS4044-20	TI	
						Z6104-3	Zilog	
				20	5	MCM2143-20	Motorola	
						TMS4046-20	TI	
				22	5	91L0EC	AMD	
						9140EC	AMD	
						S9140EC	AMI	
					-5,12	RA3-4402	GI	110
						4402A	Nitron	
					±5,12	**4200A**	**EMM/Semi (1072)**	
						M4200AS	**EMM/Semi (1072)**	
						RA3-4200	GI	
						μPD410	**NEC Micro (1420)**	
						4200A	Nitron	
	250 nsF	NMOS	TS	18	5	MK4104-4	Mostek	
						MCM2141-25	Motorola	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

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MEMORY–RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
4096x1	250 nsF	NMOS	TS	18	5	(Cont'd.)		
						MCM21L41-25	Motorola	
						SY5257	Synertek	
						TMS4044-25	TI	
						Z6104-4	Zilog	
				20	5	MCM2143-25	Motorola	
						MCM21L43-25	Motorola	
						TMS4046-25	TI	
				22	5	91L40DC	AMD	
					±5,12	**M4200UM**	**†EMM/Semi (1072)**	10
	300 nsF	NMOS	TS	18	5	IM7141-3	Intersil	
						MK4104-5	Mostek	
						MCM2141-30	Motorola	
						MCM21L41-30	Motorola	
						Z6104-5	Zilog	
						MM5257	**National (1319)**	
						2613-30	Signetics	
						TMS4044-30	TI	
				20	5	MCM2143-30	Motorola	
						MCM21L43-30	Motorola	20
						TMS4046-30	TI	
				22	5	91L40CC	AMD	
						91L40CM	†AMD	
						9140CC	AMD	
						9140CM	†AMD	
						S9140CC	AMI	
	300 ns*	CMOS	TS	18	5	**HM6504-2**	**†Harris (1176)**	
						HM6504-5	**Harris (1176)**	
	350 nsF	NMOS	TS	18	5	MK4104-6	Mostek	
						MK4104-86	†Mostek	30
	400 nsF	NMOS	TS	18	5	**4801B**	**EMM/Semi (1074)**	
				22	5	91L40BC	AMD	
						91L40BM	†AMD	
						9140BC	AMD	
						9140BM	†AMD	
						S9140BC	AMI	
	450 nsF	NMOS	TS	18	5	**4801A**	**EMM/Semi (1074)**	
						IM7141	Intersil	
						MCM2141-45	Motorola	
						MCM21L41-45	Motorola	40
						MM5257-4	**National (1319)**	
						2613-45	Signetics	
						TMS4044-45	TI	
				20	5	MCM2143-45	Motorola	
						MCM21L43-45	Motorola	
						TMS4046-45	TI	
				22	5	**4801A**	**EMM/Semi (1074)**	
	500 nsF	NMOS	TS	18	5	91L40AC	AMD	
						91L40AM	†AMD	
						9140AC	AMD	50
						9140AM	†AMD	
						S9140AC	AMI	
	600 nsF	NMOS	TS	18	5	**4801U**	**EMM/Semi (1074)**	
	650 nsF	NMOS	TS	18	5	**MM5257-6**	**National (1319)**	

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–ROMs

Dynamic

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
512x10	450 nsF	PMOS	TS	28	-12,5	S8771	AMI	
1024x5	450 nsF	PMOS	TS	28	-12.5	S8771	AMI	
1024x8	500 nsF	PMOS	TS	24	-12,5	MCS2023	MOS	
1024x12	3.6 µsF	PMOS	TS	28	-12,-24	EA3800	EA	
2048x4	1.3 µsF	PMOS	TS	28	-12,5	S8865	AMI	
	1.6 µsF	PMOS	—	24	-12,5	RO5-8192	GI	
2048x8	450 nsF	PMOS	—	28	-12,5	MCS2026	MOS	
	1.8 µsF	PMOS	TS	24	-12,5	S9996	AMI	
4096x4	1.8 µsF	PMOS	TS	28	-12,5	S8996	AMI	
4096x8	800nsF	PMOS	TS	28	-12,5	MCS2029	MOS	10

Static

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
32x8	45 nsR	TTL	OC	16	5	SN5488A SN7488A	† TI TI	
	50 nsF	TTL	OC	16	5	**6230-1** DM7488	**MMI** (1252) National	
			TS	16	5	6231-1 DM8598	MMI National	
	50 nsR	TTL	OC	16	5	MCM4002L MCM4002P	† Motorola Motorola	
	60 nsF	TTL	OC	16	5	**5230-1**	**MMI** (1252)	
			TS	16	5	**5231-1**	**† MMI** (1252)	20
	70 nsF	TTL	OC	16	5	DM5488	† National	
			TS	16	5	DM7598	National	
128x8	650 nsR	PMOS	—	24	±12	MM4220 MM5220	† National National	
	950 nsR	PMOS	—	24	-12,5	MM4221 MM5221	† National National	
	1 µsR	PMOS	TS	24	-12,5	RO6-1024-8 RO7-1024-8	† GI GI	
	4 µsR	PMOS	—	24	-13,-27	MM3501	National	
256x4	45 nsF	TTL	OC	16	5	93457C **6200-1**	Fairchild **MMI** (1252)	30
			TS	16	5	93467C **6201-1**	Fairchild **MMI** (1252)	
	50 nsF	TTL	OC	16	5	DM74S187 N82S226	National Signetics	
			TS	16	5	DM85S97 N82S229	National Signetics	
	60 nsF	TTL	OC	16	5	93457M **5200-1** DM54S187	† Fairchild **† MMI** (1252) † National	40
			TS	16	5	93467M **5201-1** DM75S97	† Fairchild **† MMI** (1252) † National	
	60 nsR	TTL	OC	16	5	DM54187 DM74187 SN54187 SN74187	† National National † TI TI	
			TS	16	5	DM7597 DM8597	† National National	
	70 nsF	TTL	OC	16	5	S82S226	† Signetics	50
			TS	16	5	S82S229	† Signetics	
	130 nsR	TTL	TS	16	5	DM76L97 DM86L97	† National National	

(Continued)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
256x4	(Cont'd.)							
	650 nsR	PMOS	—	16	±12	MM4210 MM5210	† National National	
				24	±12	MM4220 MM5220	† National National	
	950 nsR	PMOS	—	16	-12,5	MM4211 MM5211	† National National	60
				24	-12,5	MM4221 MM5221	† National National	
	1 µsR	PMOS	TS	16	-12,5	RO6-1024-4 RO7-1024-4	† GI GI	
	1.8 µsR	CMOS	—	16	3-15	MCM14524A MCM14524C	† Motorola Motorola	
256x5	75 nsR	TTL	OC	16	5	**6210-1**	**MMI** (1252)	
	80 nsR	TTL	OC	16	5	**5210-1**	**† MMI** (1252)	
256x8	60 nsF	TTL	OC	20	5	DM87S201 DM74S271	National National	70
			TS	20	5	DM74S371 DM87S202	National National	
				24	5	N82S214	Signetics	
	70 nsF	TTL	OC	20	5	SN74S271	TI	
			TS	20	5	SN74S371	TI	
	75 nsF	TTL	OC	20	5	DM54S271 DM77S201	† National † National	
			TS	20	5	DM54S371 DM77S202	† National † National	
	90 nsF	TTL	OC	24	5	**6235-1**	**MMI** (1252)	80
			TS	24	5	**6236-1** S82S214	**MMI** (1252) † Signetics	
	95 nsF	TTL	OC	20	5	SN54S271	† TI	
			TS	20	5	SN54S371	† TI	
	120 nsF	TTL	OC	24	5	**5235-1**	**† MMI** (1252)	
			TS	24	5	**5236-1**	**MMI** (1252)	
	180 nsR	TTL	OC	16	5	DM54L187A DM74L187A	† National National	
	450 nsF	NMOS	TS	24	5,12	**µPD464**	**NEC Micro** (1474)	
	750 nsR	PMOS	—	24	±12	MM4230 MM5230	National National	90
	850 nsR	PMOS	—	24	-12,5	MM4213 MM5213	† National National	
	950 nsR	PMOS	—	24	-12,5	MM4231 MM5231	† National National	
	1 µsF	PMOS	TS	24	-9,5	1302	Intel	
	1.5 µsR	PMOS	TS	24	-12.5	RO5-1302 RO6-2048-8 RO7-2048-8	GI † GI GI	
256x10	600 nsF	PMOS	—	24	-12,5	MK2400	Mostek	100
				28	-12,5	MK2400	Mostek	
256x12	1.4 µsF	PMOS	—	28	-12,5	MM4229 MM5229	† National National	
320x7	700 nsR	PMOS	—	28	-14,-28	MK2000	Mostek	
	1 µsF	PMOS	—	24	-12,5	MK2300	Mostek	
384x8	900 nsR	PMOS	TS	24	-12,5	MM4241 MM5251	† National National	

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY–ROMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
512x4	50 nsF	TTL	OC	16	5	93431C N82S230	Fairchild Signetics	
			TS	16	5	93441C N82S231	Fairchild Signetics	
	55 nsF	TTL	OC	16	5	**DM74S270**	**National (1279)**	
			TS	16	5	**DM74S370**	**National (1279)**	
	60 nsF	TTL	OC	16	5	93431M **6205-1**	† Fairchild **MMI (1252)**	
			TS	16	5	93441M **6206-1**	† Fairchild **MMI (1252)**	10
	70 nsF	TTL	OC	16	5	**DM54S270** S82S230 SN74S270	**† National (1279)** † Signetics TI	
			TS	16	5	**DM54S370** S82S231 SN74S370	**† National (1279)** † Signetics TI	
	75 nsR	TTL	OC	16	5	**5205-1**	**† MMI (1252)**	
			TS	16	5	**5206-1**	**† MMI (1252)**	
	95 nsF	TTL	OC	16	5	SN54S270	† TI	
			TS	16	5	SN54S370	† TI	20
	725 nsR	PMOS	—	24	±12	MM4230 MM5230	† National National	
	850 nsR	PMOS	TS	24	-12,5	MM4213 MM5213	† National National	
	950 nsR	PMOS	—	24	-12,5	MM4231 MM5231	† National National	
	1 μsR	PMOS	TS	24	-12,5	MM4243 MM5243	National National	
	1.5 μsR	PMOS	—	24	-12,5	RO6-2048-4 RO7-2048-4	† GI GI	30
512x5	75 nsR	TTL	OC	16	5	**6225-1**	**MMI (1252)**	
	90 nsR	TTL	OC	16	5	**5225-1**	**† MMI (1252)**	
	450 nsF	NMOS	TS	18	5	RO3-2560 RO3-2560	EMM/Semi GI	
	500 nsR	PMOS	TS	24	±12	MM4240 MM5240	† National National	
512x8	55 nsF	TTL	OC	24	5	93432C	Fairchild	
			TS	24	5	93442C	Fairchild	
	60 nsF	TTL	OC	24	5	N82S240	Signetics	
			TS	24	5	N82S215 N82S241	Signetics Signetics	40
	65 nsF	TTL	OC	24	5	**DM87S95**	**National (1281)**	
			TS	24	5	**DM87S96**	**National (1281)**	
	70 nsF	TTL	OC	24	5	93432M	† Fairchild	
			TS	24	5	93442M	† Fairchild	
	75 nsR	TTL	OC	24	5	3304AL-6	Intel	
	80 nsF	TTL	OC	24	5	**DM77S95**	**† National (1281)**	
			TS	24	5	**DM77S96**	**† National (1281)**	
	90 nsF	TTL	OC	24	5	**6240-1** S82S240	**MMI (1252)** † Signetics	
			TS	24	5	**6241-1** S82S215 S82S241	**MMI (1252)** † Signetics † Signetics	50
	120 nsF	TTL	OC	24	5	**5240-1** DM8595	**† MMI (1252)** National	

(Continued)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
512x8	120 nsF	TTL	OC	24	5	(Cont'd.) DM8795	 National	
			TS	24	5	**5241-1** DM8596 DM8796	**† MMI (1252)** National National	60
	150 nsF	TTL	OC	24	5	DM7595 DM7795	† National † National	
			TS	24	5	DM7596 DM7796	† National † National	
	400 ns*	CMOS	TS	24	10	CDP1831 CDP1832 HCMP1831 HCMP1832	† RCA † RCA † Hughes † Hughes	
	500 nsF	NMOS	TS	22	5	RO3-4096 RO3-4096	EMM/Semi GI	70
				24	5	9214C 9214M SY2530 SY3515	AMD † AMD Synertek Synertek	
	600 nsF	PMOS	TS	24	-12,5	351519 3515192	Fairchild Fairchild	
	700 nsF	PMOS	TS	24	-12,5	MK2500 MK2600 2530	Mostek Mostek Signetics	
	850 nsF	PMOS	TS	24	-12,5	3514191	Fairchild	80
	850 ns*	CMOS	TS	24	5	CDP1831C CDP1832C HCMP1831C HCMP1832C	RCA † RCA † Hughes † Hughes	
	1 μsF	PMOS	TS	24	-12,5	S3514 S5232 3514192 MM1742 MM5244	AMI AMI Fairchild National National	
	1 μsR	PMOS	TS	24	-12,5	MM4214 MM5214 MM4232 MM5232 MM4233 MM5233	† National National † National National † National National	90
	1.25 μsF	PMOS	TS	24	-12,5	MM4244	National	
512x9	700nsF	PMOS	TS	24	-12,5	2526	Signetics	
512x10	500 nsF	NMOS	TS	24	5	RO3-5120 RO3-5120	EMM/Semi GI	
	725 nsF	PMOS	—	24	±12	EA4000	EA	100
1024x4	60 nsF	TTL	OC	18	5	**6250-1** **6252-1**	**MMI (1252)** **MMI (1252)**	
			TS	18	5	**6251-1** **6253-1**	**MMI (1252)** **MMI (1252)**	
	70 nsF	TTL	—	16	5	N8228	Signetics	
	75 nsF	TTL	OC	18	5	**5250-1** **5252-1**	**† MMI (1252)** **† MMI (1252)**	
			TS	18	5	**5251-1** **5253-1**	**† MMI (1252)** **† MMI (1252)**	
	700 nsF	PMOS	TS	24	-12,5	MK2500 MK2600	Mostek Mostek	110
	1 μsF	PMOS	TS	24	-12,5	S5232	AMI	
	1 μsR	PMOS	TS	24	-12,5	MM4232	† National	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–ROMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x4	1 µsR	PMOS	TS	24	-12,5	(Cont'd.)		
						MM5232	National	
1024x8	45 nsF	TTL	OC	24	5	93454C	Fairchild	
			TS	24	5	93464C	Fairchild	
	55 nsF	TTL	OC	22	5	**6286-2**	**MMI** (1252)	
				24	5	**6280-2**	**MMI** (1252)	
			TS	20	5	**6289-2**	**MMI** (1252)	
				22	5	**6287-2**	**MMI** (1252)	
				24	5	**6281-2**	**MMI** (1252)	
	60 nsF	TTL	OC	24	5	93454M	† Fairchild	10
			TS	24	5	93464M	† Fairchild	
	70 nsF	TTL	OC	24	5	**DM85S29**	**National** (1283)	
						N82S280	Signetics	
			TS	24	5	**DM85S28**	**National** (1283)	
						N82S281	Signetics	
	75 nsF	TTL	OC	22	5	**5286-2**	**† MMI** (1252)	
				24	5	**5282-2**	**† MMI** (1252)	
			TS	20	5	**5289-2**	**† MMI** (1252)	
				22	5	**5287-2**	**† MMI** (1252)	
				24	5	**5281-2**	**† MMI** (1252)	20
	90 nsF	TTL	OC	24	5	**DM75S29**	**† National** (1283)	
			TS	24	5	**DM75S28**	**† National** (1283)	
	100 nsF	TTL	OC	22	5	**6286-1**	**MMI** (1252)	
				24	5	**6280-1**	**MMI** (1252)	
						6282-1	**MMI** (1252)	
						6284-1	MMI	
						S82S280	† Signetics	
			TS	20	5	**6289-1**	**MMI** (1252)	
				22	5	**6287-1**	**MMI** (1252)	
				24	5	**6281-1**	**MMI** (1252)	30
						6283-1	**MMI** (1252)	
						6285-1	MMI	
						S82S281	† Signetics	
	175 nsF	TTL	OC	22	5	**5286-1**	**† MMI** (1252)	
				24	5	AM27S80C	AMD	
						5280-1	**† MMI** (1252)	
						5282-1	**† MMI** (1252)	
						5284-1	† MMI	
			TS	20	5	**5289-1**	**† MMI** (1252)	
				22	5	**5287-1**	**† MMI** (1252)	40
				24	5	AM27S81C	AMD	
						5281-1	**† MMI** (1252)	
						5283-1	**† MMI** (1252)	
						5285-1	† MMI	
	250 nsF	NMOS	TS	24	5,12	9208DC	AMD	
					±5,12	MB8308E	Fujitsu	
	275 nsF	TTL	OC	24	5	AM27S80M	† AMD	
			TS	24	5	AM27S81M	† AMD	
	290 nsF	NMOS	TS	24	±5,12	NC6560A	Nitron	
	300 nsF	NMOS	TS	24	5,12	9208CC	AMD	50
	350 nsF	NMOS	TS	24	5	MCM68A308	Motorola	
					±5,12	MCM65308	Motorola	

(Continued)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x8	350 nsF	NMOS	TS	24	(Cont'd.)			
					-3,5,12	MCM6560	Motorola	
						NC6560	Nitron	
	350 ns*	CMOS	TS	24	10	CDP1833	† RCA	
						CDP1834	† RCA	
						HCMP1833	† Hughes	
						HCMP1834	† Hughes	
	400 nsF	NMOS	TS	24	5	ER2308AC	EA	60
						EA4700C	EA	
						EA8308AC	EA	
					5,12	9208BC	AMD	
						9208BM	† AMD	
	450 nsF	NMOS	TS	24	5	MM5242	National	
						2608-1	Signetics	
						2607	Signetics	
					5,12	MK30000	Mostek	
					±5,12	8308	AMD	
						3508	Fairchild	70
						MB8308N	Fujitsu	
						µPD2308	**NEC Micro** (1478)	
						TMS4700	TI	
	500 nsF	NMOS	TS	24	5	MCM6830A	Motorola	
	550 nsF	NMOS	TS	24	5	EA2308AL	EA	
						EA4700	EA	
						EA8308AL	EA	
						2608	Signetics	
	575 nsF	NMOS	TS	24	5	MM4242	National	
	600 nsF	NMOS	TS	24	5,12	9208M	† AMD	80
	850 nsF	NMOS	TS	24	±5,12	M58730	Mitsubishi	
	850 ns*	CMOS	TS	24	5	CDP1833C	† RCA	
						CDP1834C	† RCA	
						HCMP1833C	† Hughes	
						HCMP1834C	† Hughes	
1024x9	100 nsF	TTL	OC	24	5	6260-1	MMI	
			TS	24	5	6261-1	MMI	
		150 nsF						
			OC	24	5	5260-1	† MMI	
			TS	24	5	5261-1	† MMI	90
1024x10	100 nsF	TTL	OC	24	5	6255-1	MMI	
			TS	24	5	6256-1	MMI	
		150 nsF						
			OC	24	5	5255-1	† MMI	
			TS	24	5	**5286-1**	**† MMI** (1252)	
1024x12	200 ns*	CMOS	TS	18	10	IM6312	Intersil	
	250 nsR	CMOS	TS	18	4-11	HM6312A-2	† Harris	
						HM6312A-9	Harris	
	500 nsR	CMOS	TS	18	5	HM6312-2	† Harris	
						HM6312-9	Harris	100
	500 ns*	CMOS	TS	18	5	IM6312	Intersil	
	3 µsR	PMOS	—	28	±12	MM5215	National	
	5 µsR	PMOS	—	28	-12,5	MM5212	National	
2048x4	125 nsF	TTL	OC	18	5	S82S184	† Signetics	
			TS	18	5	S82S185	† Signetics	
	290 nsF	NMOS	TS	24	±5,12	NC6560A	Nitron	
	350 nsF	NMOS	TS	24	-3,5,12	MCM6560	Motorola	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY–ROMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
2048x4	350 nsF	NMOS	TS	24	-3,5,12	(Cont'd.)		
						NC6560	Nitron	
	950 nsR	PMOS	—	24	-12,5	2580	Signetics	
2048x8	80 nsF	TTL	OC	24	5	N82S290	Signetics	
			TS	24	5	N82S291	Signetics	
	110 nsF	TTL	OC	24	5	**6275-1**	**MMI** (1252)	
			TS	24	5	**6276-1**	**MMI** (1252)	
	120 nsF	TTL[&]	OC	24	5	**5275-1**	**†MMI** (1252)	
			TS	24	5	**5276-1**	**†MMI** (1252)	
	125 nsF	VMOS	TS	24	5	**S4216B-1**	**AMI** (1051)	10
						S4216D-1	**AMI** (1051)	
	150 ns*	I²L	OC/TTL	24	ma	SBP9818C	TI	
						SBP9818M	†TI	
	200 nsF	VMOS	TS	24	5	**S4216B-2**	**AMI** (1051)	
						S4216D-2	**AMI** (1051)	
	300 nsF	NMOS	TS	24	5,12	9216CC	AMD	
					5	2600-1	Signetics	
	350 nsF	NMOS	TS	24	5	9218CC	AMD	
						RO3-8316C	GI	20
						RO3-9316C	GI	
						MK34000-3	Mostek	
	350 ns*	I²L	OC/TTL	24	5	SBP8316M	TI	
						SBP8316M	†TI	
						MCM68A316	Motorola	
						2616-1	Signetics	
						2617-1	Signetics	
	400 nsF	NMOS	TS	24	5	9216BC	AMD	
						9216BM	†AMD	30
	450 nsF	NMOS	TS	24	5	9217BC	AMD	
						9217BM	†AMD	
						S6831A	**AMI** (1062,1560)	
						S6831B	**AMI** (1062,1560)	
						S6831C	**AMI** (1062,1560)	
						S8316	AMI	
						EA8316EC	EA	40
						RO3-8316B	EMM/Semi	
						3516	Fairchild	
						RO3-8316B	GI	
						RO3-9316B	GI	
						2316E	Intel	
						2616-11	Intersil	
						MM2316A	**National** (1307,1372)	
						MM5246	National	
						MM5258	National	50
						μPD2316A	**NEC Micro** (1481)	
						μPD2316E	**NEC Micro** (1492)	
						R2316B	Rockwell	
						2616	Signetics	
						2617	Signetics	
						SY2316B	Synertek	
						SY8316B	Synertek	
	475 nsF	NMOS	TS	24	±5,12	NC6590A	Nitron	
	500 nsF	NMOS	TS	24	5	**S6831**	**AMI** (1062,1560)	60

(Continued)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
2048x8	500 nsF	NMOS	TS	24	5	(Cont'd.)		
						MCM68316E	Motorola	
						MM5246	National	
						2600	Signetics	
					±5,12	MCM6832	Motorola	
						MCM65317	Motorola	
	525 nsF	NMOS	TS	24	5	EA8316EL	EA	
	550 nsF	NMOS	TS	24	5	9217AC	AMD	
						9217AM	†AMD	
						MK31000-3	Mostek	70
						R2316B	Rockwell	
						SY2316A	Synertek	
						SY4600	Synertek	
						SY8316A	Synertek	
	575 nsF	NMOS	TS	24	5	MM4246	†National	
	600 nsF	NMOS	TS	24	5	EA2316A	EA	
						EA4600C	EA	
						EA8316AC	EA	
		PMOS	—	24	-12,5	MK28000	Mostek	
	700 nsF	PMOS	—	24	-12,5	TMS4800	TI	80
	750 nsF	NMOS	TS	24	5	EA4600L	EA	
						EA8316AL	EA	
	800 nsF	NMOS	TS	24	-3,5,12	MCM6590	Motorola	
						NC6590	Nitron	
	850 nsF	NMOS	TS	24	5	RO3-8316A	EMM/Semi	
						RO3-8316A	GI	
						RO3-9316A	GI	
						2316A	Intel	
						M58731	Mitsubishi	
						μPD2316A	**NEC Micro** (1481)	90
						TMM331	Toshiba	
	950 nsF	PMOS	—	24	-12,5	EA4900C	EA	
	1.35 μsF	PMOS	—	24	-12,5	EA4900L	EA	
2048x10	500 nsF	NMOS	TS	24	5	RO3-20480	GI	
4096x1	45 nsF	TTL	OC	18	5	N82S400A	Signetics	
			TS	18	5	N82S401A	Signetics	
	70 nsF	TTL	OC	18	5	N82S400	Signetics	
			TS	18	5	N82S401	Signetics	
4096x4	550 nsF	NMOS	TS	24	5	EA4600C	EA	
						SY4600	Synertek	100
	600 nsF	PMOS	—	24	-12,5	MK28000	Mostek	
	700 nsF	PMOS	—	24	±12,5	TMS4800	TI	
	750 nsF	NMOS	TS	24	5	EA4600M	†EA	
	1 μsF	NMOS	TS	24	5	RO3-16384	EMM/Semi	
						RO3-16384	GI	
4096x8	300 nsF	NMOS	TS	24	5	MK32000-5	Mostek	
	350 nsF	NMOS	TS	24	5	RO3-9332C	GI	
						MCM68A332	Motorola	
				28	5	EA3200	EA	
	450 nsF	NMOS	TS	24	5	**μPD2332**	**NEC Micro** (1485)	110
						R2332	Rockwell	
						2633	Signetics	
						SY2332	Synertek	
						TMS4732	TI	
8192x8	300 nsF	NMOS	TS	24	5	MK36000-5	Mostek	
						2665	Signetics	
	350 nsF	VMOS	TS	24	5	**S4264**	**AMI** (1054)	
	800 nsF	NMOS	TS	28	5	MM4235	†National	
						MM5235	National	

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–Shift Registers

Dynamic

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
16	4	SS	PMOS	3.0 M	-28	EA1208	EA	
32	4	SS	PMOS	1.0 M	-28	EA1201	EA	
				3.0 M	-28	EA1200	EA	
64	1	SS	PMOS	1.0 M	-14,-28	EA1203	EA	
				3.0 M	-14,-28	EA1202	EA	
	2	SS	PMOS	0.1 M	-14	HD3213	Hitachi	
					-14,9	HD3214	Hitachi	
				10.0 M	-17	HDSR2164	Hughes	
	3	SS	PMOS	0.1 M	-14	HD3214	Hitachi	
	4	SS	PMOS	5.0 M	-12,5	TMS3417	TI	10
					±5	HD3508	Hitachi	
66	3	SS	PMOS	1.0 M	-14	CRC1505	Rockwell	
				2.0 M	-24,-14	MTS1016	MOS	
72	3	SS	PMOS	5.0 M	±5	HD3523	Hitachi	
						HD3524	Hitachi	
80	4	SS	PMOS	2.5 M	-12,5	MK1007	Mostek	
						SY7780	Synertek	
				5.0 M	-12,5	TMS3409	TI	
100	2	SS	PMOS	1.0 M	±5	HD3506	Hitachi	
						HD3507	Hitachi	20
				2.0 M	-10	MTS1001	MOS	
					±5	1406	†AMD	
						1407	†AMD	
						1506	AMD	
						1507	AMD	
				2.5 M	-12,5	MM4006	†National	
						MM5006	National	
				3.0 M	±5	MTS2013	MOS	
						2506	Signetics	
						2507	Signetics	30
						2517	Signetics	
128	2	SS	PMOS	5.0 M	±5	HD3509	Hitachi	
200	1	SS	CMOS	5.0 M	3-15	CD4062A	†RCA	
			PMOS	1.0 M	-28	EA1221	EA	
256	1	SS	PMOS	1.0 M	-28	EA1205	EA	
				2.0 M	-12,5	3383	Fairchild	
				2.5 M	±5	HD3510	Hitachi	
				3.0 M	-14	EA1204	EA	
	2	SS	PMOS	2.5 M	-14	EA1210	EA	
	4	SS	PMOS	2.5 M	±5	SY1402B	Synertek	40
						SY1402BR	Synertek	
				3.0 M	±5	HDSR1026	Hughes	
				5.0 M	±5	1402AC	AMD	
						1402AM	†AMD	
						HD3502	Hitachi	
						1402A	Intel	
						MM1402A	National	
						1402	Nortec	
						1402A	Nortec	
						M141	SGS	50
						SY1402A	Synertek	
						SY1402AR	Synertek	
				8.0 M	±5	2502	Signetics	
				10.0 M	±5	AM2802C	AMD	
						AM2802M	†AMD	

(Continued)

Dynamic (Cont'd)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
256	4	SS	PMOS	10.0 M	±5	(Cont'd.)		
						SY2802	Synertek	
	64	SS	CCD	1.0 M	-5,12	2416	Intel	
360	2	SS	PMOS	2.5 M	-12,5	MM4104	†National	
						MM5104	National	60
455	2	SS	CCD	20.0 M	17	CCD321	Fairchild	
512	1	SS	PMOS	2.0 M	±5	1405A	Intel	
				2.5 M	±5	2505	Signetics	
					-12,5	MM4016	†National	
						MM5016	National	
				3.0 M	±5	AM2805M	†AMD	
						AM2807M	†AMD	
						2524	Signetics	
					-14	EA1212	EA	
				4.0 M	±5	AM2805C	AMD	70
						AM2807C	AMD	
				5.0 M	±5	HD3505	Hitachi	
						MTS2100	MOS	
					-12,5	TMS3401	TI	
					-27	EA1206	EA	
	2	SS	PMOS	2.5 M	±5	SY1403B	Synertek	
						SY1403BR	Synertek	
				5.0 M	±5	1403AC	AMD	
						1403AM	†AMD	
						HD3503	Hitachi	80
						1403A	Intel	
						MM1403A	National	
						1403A	Nortec	
						M136	SGS	
						SY1403A	Synertek	
						SY1403AR	Synertek	
				8.0 M	±5	HDSR1025	Hughes	
						2503	Signetics	
				10.0 M	±5	AM2803C	AMD	
						AM2803M	†AMD	90
						SY2803	Synertek	
1024	1	SS	NMOS	1.0 M	5	2405	Intel	
						SY2405	Synertek	
			PMOS	2.5 M	±5	2512	Signetics	
						SY1404B	Synertek	
						SY1404BR	Synertek	
				3.0 M	±5	AM2806M	†AMD	
						AM2808M	†AMD	
						2512	Nortec	
						2525	Signetics	100
				4.0 M	±5	AM2806C	AMD	
						AM2808M	AMD	
						2512	Nortec	
						SY7712	Synertek	
						SY7722	Synertek	
				5.0 M	±5	1404AC	AMD	
						1404AM	†AMD	
						HD3504	Hitachi	
						1404A	Intel	
						MM1404A	National	110
						MM5024A	National	
						1404A	Nortec	
						1404A	Signetics	
					5	SY1404A	Synertek	

(Continued)

† Military Temperature Range (−55° to 125°C)

SS = Serial In, Serial Out

PP = Parallel In, Parallel Out

* Typical Values

MEMORY–Shift Registers (Cont'd)

Dynamic (Cont'd)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
1024	1	SS	PMOS	5.0 M	5	(Cont'd.)		
						SY1404AR	Synertek	
				8.0 M	±5	HDSR1024	Hughes	
						2504	Signetics	
						M130	SGS	
				10.0 M	±5	AM2804C	AMD	
						AM2804M	†AMD	
						SY2804	Synertek	
	2	SS	NMOS	1.0 M	5	AM2401	AMD	
						2401	Intel	10
						SY2401	Synertek	
				2.0 M	5	9401C	AMD	
						9401M	†AMD	
				2.5 M	5	SY2401-1	Synertek	
			PMOS	1.0 M	-12,5	MM4025	†National	
						MM4026	†National	
				3.0 M	-12,5	MM5025	National	
						MM5026	National	
						SY5025	Synertek	
						SY5026	Synertek	20
				4.0 M	-10.5,5	AM2825M	†AMD	
						AM2826M	†AMD	
				6.0 M	-10.5,5	AM2825C	AMD	
						AM2826C	AMD	
						SY2825A	Synertek	
						SY2826A	Synertek	
				8.0 M	±5	HDSR2048	Hughes	
	9	SS	CCD	2.0 M	-2.5,5,12	CCD450A	Fairchild	
				1.0 M	-2.5,5,12	CCD450	Fairchild	
				2.0 M	-2.5,5,12	CCD450A	Fairchild	30
						CCD451	Fairchild	
				4.0 M	-2.5,5,12	CCD451A	Fairchild	
2048	1	SS	PMOS	1.0 M	-12,5	MM4027	†National	
				3.0 M	-12,5	MM5027	National	
						SY5027	Synertek	
				4.0 M	-10.5,5	AM2827M	†AMD	
					-12,5	SY5028	Synertek	
				6.0 M	-10.5,5	AM2827C	AMD	
						SY2827	Synertek	
4096	4	PP	CCD	5.0 M	±5,12	CCD460	Fairchild	40
65536	1	SS	CCD	5.0 M	—	**F464**	**Fairchild**	**(1083)**
					±5,12	TMS3064	TI	

Static

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
4	1	PP	Bipolar	3 M	5	SN54L95	TI	
						SN54L99	†TI	
						SN74L99	TI	
						SN74L95	TI	
				5 M	5	93L00C	†AMD	
						93L00M	†AMD	
				6 M	5	DM54L95	†National	
						DM74L95	National	50
				15 M	5	9300C	AMD	
						9300M	†AMD	
						93L00C	†Fairchild	
						93L00M	†Fairchild	

(Continued)

Static (Cont'd)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
4	1	PP	Bipolar	15 M	5	(Cont'd.)		
						IT9300-1	†ITT	
						IT9300-5	ITT	
						MC8300	Motorola	
						MC9300	†Motorola	
						RC9300	Raytheon	60
						RM9300	†Raytheon	
						N8270	Signetics	
						N8271	Signetics	
				20 M	5	HD2534	Hitachi	
						MC7270	Motorola	
						MC7271	Motorola	
						MC8270	Motorola	
						MC8271	Motorola	
						DM54LS295A	†National	
						DM74LS295A	National	70
						DM5495	†National	
						DM7495	National	
						RC8270	Raytheon	
						RM8270	†Raytheon	
						RC8271	Raytheon	
						RM8271	†Raytheon	
				25 M	5	SN54194	†AMD	
						SN74194	AMD	
						5495	†Fairchild	
						7495	Fairchild	80
						54178	†Fairchild	
						74178	Fairchild	
						54179	†Fairchild	
						74179	Fairchild	
						54194	†Fairchild	
						74194	Fairchild	
						ITT5495	†ITT	
						ITT7495	ITT	
						ITT54194	†ITT	
						ITT74194	ITT	90
						MC54194	†Motorola	
						MC74194	Motorola	
						54194	†Raytheon	
						74194	Raytheon	
						5495	†Signetics	
						7495	Signetics	
						54194	†Signetics	
						74194	Signetics	
						SN5495A	†TI	
						SN7495A	TI	100
						SN54178	†TI	
						SN74178	TI	
						SN54179	†TI	
						SN74179	TI	
						SN54194	TI	
						SN74194	TI	
				30 M	5	SN54195	†AMD	
						SN74195	AMD	
						5495	†Fairchild	
						7495	Fairchild	110
						54LS95	†Fairchild	
						74LS95	Fairchild	
						54LS194	Fairchild	
						74LS194	Fairchild	
						54LS195	†Fairchild	
						74LS195	Fairchild	
						54LS295	†Fairchild	
						74LS295	Fairchild	
						IT54195	†ITT	
						IT74195	ITT	120

(Continued)

† Military Temperature Range (−55° to 125°C)

SS = Serial In, Serial Out

PP = Parallel In, Parallel Out

* Typical Values

Bold face indicates additional data is provided on the page noted.

MEMORY–Shift Registers (Cont'd)

Static (Cont'd)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
4	1	PP	Bipolar	30 M	5	(Cont'd.)		
						MC54195	† Motorola	
						MC74195	Motorola	
						DM5495	† National	
						DM7495	National	
						DM54195	† National	
						DM74195	National	
						DM54LS95	† National	
						DM74LS95	National	
						DM8300	National	10
						DM9300	† National	
						54195	† Raytheon	
						74195	Raytheon	
						9LS95BC	Raytheon	
						9LS95BM	† Raytheon	
						54LS95	† Raytheon	
						74LS95	Raytheon	
						9LS195C	Raytheon	
						9LS195M	† Raytheon	
						54LS195	† Raytheon	20
						74LS195	Raytheon	
						54195	† Signetics	
						74195	Signetics	
						SN54195	† TI	
						SN74195	TI	
				31 M	5	MC5495	† Motorola	
						MC7495	Motorola	
				35 M	5	MC4012	Motorola	
				38 M	5	9300C	Fairchild	
						9300M	† Fairchild	30
				55 M	5	93H00C	† Fairchild	
						93H00M	† Fairchild	
				60 M	5	93H72C	Fairchild	
						93H72M	† Fairchild	
						N82S70	Signetics	
						N82S71	† Signetics	
				70 M	5	SN54S194	† AMD	
						SN74S194	AMD	
						SN54S195	† AMD	
						SN74S195	AMD	40
						93S00C	Fairchild	
						93S00M	† Fairchild	
						93S194C	Fairchild	
						93S194M	† Fairchild	
						DM54S194	† National	
						DM74S194	National	
						DM54S195	† National	
						DM74S195	National	
						SN54S194	† TI	
						SN74S194	TI	50
						SN54S195	† TI	
						SN74S195	TI	
				75 M	5	74S194	Signetics	
				150 M	-4.5	F10000	Fairchild	
					-5.2	MC10141	Motorola	
						10141	Signetics	
				190 M	-5.2	95H00C	Fairchild	
				250 M	-5.2	F10141	Fairchild	
		PS	Bipolar	1 M	11	MC794	Motorola	
				10 M	5	5494	† Fairchild	60
						7494	Fairchild	
						MC5494	† Motorola	

(Continued)

Static (Cont'd)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
4	1	PS	Bipolar	10 M	5	(Cont'd.)		
						MC7494	Motorola	
						5494	Signetics	
						7494	Signetics	
						SN5494	† TI	
						SN7494	TI	
		SP		325 M	-5.2	MC1694	† Motorola	
		SS		0.5 M	15	MC686	Motorola	70
		PP	CMOS	2 M	3-15	F4035BM	† Fairchild	
						F4019BM	† Fairchild	
						F40195BM	† Fairchild	
						MC14035BC	Motorola	
						CD4035BE	RCA	
						SCL4035B	SSS	
						CM4035AE	Solitron	
						TC4035	Toshiba	
				3 M	3-15	F4035BC	Fairchild	
						F40194BC	Fairchild	80
						F40195BC	Fairchild	
						SIL4035B	† Mitel	
						SIL4035BE	Mitel	
						MC14035BA	† Motorola	
						CD4035B	† RCA	
						CM4035A	† Solitron	
						TP4035B	TI	
				9 M*	3-15	CD40104B	RCA	
						CD40104BE	† RCA	
	2	SP	CMOS	1 M	5	CM4015AE	Solitron	90
				1.5 M	5	CM4015AD	† Solitron	
					3-15	TP4015A/B	TI	
				2.5 M	3-15	34015BC	Fairchild	
					3-16	MC14015BC	Motorola	
					3-15	CD4015AC	National	
						CD4015BE	RCA	
						TC4015	Toshiba	
				3 M	3-15	34015BM	† Fairchild	
						SIL4015B	† Mitel	
						SIL4015BE	Mitel	100
					3-18	MC14015A	† Motorola	
					3-15	CD4015AM	† National	
						CD4015B	† RCA	
						SCL4015B	† SSS	
						SCL4015BE	SSS	
5	1	PP	Bipolar	10 M	5	5496	† Fairchild	
						7496	Fairchild	
						ITT5496	† ITT	
						ITT7496	ITT	
						MC5496	† Motorola	110
						MC7496	Motorola	
						DM5496	† National	
						DM7496	National	
						5496	† Signetics	
						7496	Signetics	
						SN5496	† TI	
						SN7496	TI	
						7496	TRW	
	2	PP	Bipolar	35 M	5	HD2546	Hitachi	
	4	SS	CMOS	1.2 M	5	CM4006AE	Solitron	120
				1.5 M	5	CM4006AD	† Solitron	
				2 M	3-15	CM4006A	† Solitron	

(Continued)

† Military Temperature Range (−55° to 125°C)

SS = Serial In, Serial Out

PP = Parallel In, Parallel Out

* Typical Values

MEMORY–Shift Registers (Cont'd)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
Static (Cont'd)								
5	4	SS	CMOS	2 M	3-15	(Cont'd.)		
						CM4006AE	Solitron	
						CD4006AE	RCA	
				2.5 M	3-15	CD4006A	†RCA	
				3 M	3-15	SCL4006A	†SSS	
						SCL4006A	SSS	
				4 M	5-15	MC14006BC	Motorola	
				7 M	5-15	MC14006BA	†Motorola	
8	1	PP	Bipolar	25 M	5	54198	†Fairchild	
						74198	Fairchild	10
						54199	†Fairchild	
						74199	Fairchild	
						DM54198	†National	
						DM74198	National	
						DM54199	†National	
						DM74199	National	
						54198	†Raytheon	
						74198	Raytheon	
						54199	†Raytheon	
						74199	Raytheon	20
						54198	†Signetics	
						74198	Signetics	
						54199	†Signetics	
						74199	Signetics	
						SN54198	†TI	
						SN74198	TI	
						SN54199	†TI	
						SN74199	†TI	
				50 M	5	SN54S299	†TI	
						SN74S299	TI	30
		PS	Bipolar	14 M	5	DM7590	†National	
						DM8590	National	
				20 M	5	54165	†Fairchild	
						74165	Fairchild	
						MC54165	†Motorola	
						MC74165	Motorola	
						DM54165	†National	
						DM74165	National	
						54165	†Raytheon	
						74165	Raytheon	40
						54165	†Signetics	
						74165	Signetics	
						SN54165	†TI	
						SN74165	TI	
				25 M	5	54166	†Fairchild	
						74166	Fairchild	
						DM54166	†National	
						DM74166	National	
						54166	†Raytheon	
						74166	Raytheon	50
						54166	†Signetics	
						74166	Signetics	
						SN54166	†TI	
						SN74166	TI	
		SP	Bipolar	12 M	5	DM54L164	†National	
						DM74L164	National	
						SN54L164	†TI	
						SN74L164	TI	
				14 M	5	DM7570	†National	
						DM8570	National	60
				25 M	5	9LS164C	Fairchild	
						9LS164M	†Fairchild	
						54164	†Fairchild	

(Continued)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
Static (Cont'd)								
8	1	SP	Bipolar	25 M	5	(Cont'd.)		
						74164	Fairchild	
						54LS164	†Fairchild	
						74LS164	Fairchild	
						ITT74LS164	ITT	
						54LS164	†Motorola	
						74LS164	Motorola	70
						DM54LS164	†National	
						DM74LS164	National	
						μPB74LS164	NEC America	
						9LS164C	**Raytheon (272)**	
						9LS164M	**†Raytheon (272)**	
						54LS164	**†Raytheon (272)**	
						74LS164	**Raytheon (272)**	
						54164	†Raytheon	
						74164	Raytheon	
						54LS164	†Signetics	80
						74LS164	Signetics	
						54164	†Signetics	
						74164	Signetics	
						SN54LS164	†TI	
						SN74LS164	TI	
		SS	Bipolar	3 M	5	SN54L91	†TI	
						SN74L91	TI	
				4 M	5	DM54L91	†National	
						DM74L91	National	
				10 M	5	5491	†Fairchild	90
						7491	Fairchild	
						HD2524	Hitachi	
						MC5491A	†Motorola	
						MC7491A	Motorola	
						9LS91C	**Raytheon (272)**	
						9LS91M	**†Raytheon (272)**	
						54LS91	**†Raytheon (272)**	
						74LS91	**Raytheon (272)**	
						5491	†Signetics	
						7491	Signetics	100
						SN5491A	†TI	
						SN7491A	TI	
				15 M	5	N8276	Signetics	
		PP	CMOS	2.5 M	3-18	MC14034BC	Motorola	
					3-15	SCL4034BE	SSS	
					5	CM4034AE	Solitron	
				3 M	3-18	MC14034B	Motorola	
					3-15	CD4034BM	National	
						CD4034B	†RCA	
						SCL4034B	†SSS	110
					5	CM4034A	†Solitron	
					3-15	TC4034	Toshiba	
		PS	CMOS	1 M	3-15	F4014BC	Fairchild	
						F4021BC	Fairchild	
						CM4014A	†Solitron	
				1.3 M	3-15	TP4021A	TI	
				2.5 M	3-15	MC14021BC	Motorola	
						CD4014BE	RCA	
						CD4021B	†RCA	
						CD4021BE	RCA	120
						TC4014	Toshiba	
						TC4021	Toshiba	
				3 M	3-15	F4014BM	†Fairchild	
						F4021BM	†Fairchild	
						SIL4010B	†Mitel	

(Continued)

† Military Temperature Range (−55° to 125°C)

SS = Serial In, Serial Out

PP = Parallel In, Parallel Out

* Typical Values

Bold face indicates additional data is provided on the page noted.

MEMORY–Shift Registers (Cont'd)

Static (Cont'd)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source
8	1	PS	CMOS	3 M	3-15	(Cont'd.)	
						SIL4014E	Mitel
						SIL4021B	† Mitel
						SIL4021BE	Mitel
						MC14021B	† Motorola
						CD4014B	† RCA
						CD4021B	† RCA
						SCL4014B	† SSS
						SCL4021B	† SSS
						CM4021A	† Solitron
	2	SS	Bipolar	10 M	5	93L28C	AMD
						93L28M	† AMD
						93L28M	† Fairchild
						93L28C	Fairchild
						MC8328	Motorola
						MC9328	† Motorola
				15 M	5	RC8277	Raytheon
						RM8277	† Raytheon
						N8277	Signetics
				20 M	5	9328C	AMD
						9328M	† AMD
						9328C	Fairchild
						9328M	† Fairchild
10	1	PP	TTL	0.5 M	5	RC8274	Raytheon
						RM8274	† Raytheon
						N8274	Signetics
						S8274	† Signetics
		SP	PMOS	0.5 M	5	RC8273	Raytheon
						RM8273	† Raytheon
						N8273	Signetics
						S8273	† Signetics
	2	SS	CMOS	2 M	5-10	HSSR0321	† Hughes
						HSSR0351	† Hughes
16	2	SS	PMOS	2 M	-12,5	SS5-8211	GI
						SS5-8212	GI
						SS6-8211	† GI
						SS6-8212	† GI
	4	SS	PMOS	2 M	-12,5	SL5-4016	GI
20	1	SP	PMOS	5 K	-14,9	HD32112	Hitachi
24	4	SS	CMOS	2.5 M	5-16	MS618	† RTC
25	4	SS	PMOS	1 M	-12,5	SL5-4025	GI
						SL6-4025	† GI
				2 M	-12,5	MCS2104	† MOS
30	1	SS	CMOS	1M	3-15	MD4330B	Mitel
						MD4330BE	Mitel
32	1	SS	PMOS	1 M	-12,5	SS5-1032	GI
						SS6-1032	† GI
	2	SS	PMOS	1 M	-16,-10	MTS1002	MOS
				1.5 M	-28	EA1003	EA
						EA1007	EA
				2 M	-12,5	MTS2103	† MOS
	4	SS	PMOS	1 M	-12,5	SL5-4032	GI
						SL6-4032	† GI
	6	SS	PMOS	1 M	-12,5	3348	Fairchild
						3349	Fairchild
				2 M	-12,5	2518	Signetics
33	1	SP	PMOS	0.25 M	-10,-20	MM5559	National
40	6	SS	PMOS	2 M	-12,5	2519	Signetics
50	2	SS	PMOS	1 M	-12,5	SL5-2050	GI
						SL6-2050	† GI
				1.5 M	-14,12	EA1013	EA
					-12,±5	2509	Signetics
				3 M	-14,12	EA1012	EA
64	1	SS	CMOS	1 M	3-15	CD4031BE	RCA
				2 M	3-15	CD4031B	† RCA
				2.7 M	3-15	F4557BM	† Fairchild
					3-16	MC14557BA	† Motorola
				5 M	3-15	F4557BC	Fairchild
					3-18	MC14557B	Motorola
				10 M	5-16	MS612	RTC
	2	SS	Bipolar	30 M	5	TDC1005J	TRW
			CMOS	4 M	3-15	MC14517BC	Motorola
						MC14517BA	† Motorola
			PMOS	1 M	-12,5	SL5-2064	GI
						SL6-2064	† GI
				2 M	-12,5	MTS2105	† MOS
	4	SS	CMOS	4 M	4.5-12.5	F4731BC	Fairchild
						F4731BM	† Fairchild
			PMOS	1.5 M	-12,5	3342	Fairchild
80	2	SS	PMOS	1.5 M	-14,12	EA1009	EA
					-12,5	3341	Fairchild
				2.2 M	-12,5	MM4052	National
						MM5052	National
				2.5 M	-12,5	AM2847M	† AMD
				3 M	-12,5	AM2847C	AMD
					-14,12	EA1008	EA
	4	SS	NMOS	1 M	5	SR5015-80	SMC
				3 M	5	M142	SGS
			PMOS	1.5 M	-12,5	3347	Fairchild
						2532	Signetics
				2 M	-12,5	3357-2	Fairchild
				2.5 M	-12,5	AM2847M	† AMD
						TMS3120	TI
				3 M	-12,5	AM2847C	AMD
				4 M	-12,5	3357-1	Fairchild
64,72,80		SS	PMOS	1.5 M	-12,5	MM5054	National
81	4	SS	NMOS	1 M	5	SR5015-81	SMC
						SR5018	SMC
96	2	SS	PMOS	2.5 M	-12,5	TMS3126	TI
	4	SS	PMOS	2.5 M	-12,5	AM2896M	† AMD
				3 M	-12,5	AM2896C	AMD
100	1	SS	PMOS	1.5 M	-14,12	EA1005	EA
				2.5 M	-12,5	TMS3127	TI
				3 M	-14,12	EA1004	EA
	2	SS	PMOS	1 M	-28,-14	MTS1102	MOS
				1.5 M	-27,-13	M127	SGS
					-12,±5	2510	Signetics
				1.6 M	-12,5	MM4053	National

(Continued)

† Military Temperature Range (−55° to 125°C)

SS = Serial In, Serial Out

PP = Parallel In, Parallel Out

* Typical Values

MEMORY–Shift Registers (Cont'd)

Bits Per Register	No. of Reg.	Oper-ation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
Static (Cont'd)								
100	2	SS	PMOS	1.6 M	-12,5	(Cont'd.) MM5053	National	
				2 M	-12,5	SL5-C2100	GI	
	4	SS	PMOS	2.2 M	-12,5	MM5061	National	
20-100	2	SS	PMOS	2.5 M	-12,5	MM4007	National	
125	1	SS	PMOS	1 M	-12,5	ITT1144	ITT	
128	1	SS	CMOS	5 M	12	MS625	RTC	
	2	SS	PMOS	1 M	-12,5	MK1002 MK1002 SL5-2128	AMD Mostek GI	10
				1.5 M	-12,5	2521 MTS2107 MM5060AA	Signetics †MOS National	
				2 M	-12,5	AM2809M AM2810 TMS3114 SL5-C2128 MTS2108 TMS3114	†AMD AMD AMD GI †MOS TI	
				2.5 M	-12,5	AM2809C AM2814M TMS3128	AMD †AMD TI	20
	4	SS	PMOS	1 M	-12,5	MM4055	†National	
				1.5 M	-12,5	MM5055	National	
				2.5 M	-12,5	AM2855 AM4055 AM5055	AMD †AMD AMD	
16-128	1	SS	CMOS	5.6 M	3-15	MC14562B	Motorola	
132	2	SS	PMOS	1.5 M	-12,5	MM5060AB 2522	National Signetics	30
				2.5 M	-12,5	TMS3129	TI	
133	2	SS	PMOS	1.5 M	-12,5	MM5060AC	National	
				2 M	-12,5	TMS3113	TI	
				2.5 M	-12,5	TMS3130	TI	
	4	SS	NMOS	1 M	5	SR5015-133 SR5017	SMC SMC	
1-134	4	SS	NMOS	1 M	5	SR5015	SMC	
125 144	2	SS	PMOS	1.5 M	-12,5	MM5060	National	
144	1	SS	PMOS	1 M	-12,5	ITT1144	ITT	40
	2	SS	PMOS	1.5 M	-12,5	MM5060AD	National	
				2 M	-12,5	3346	Fairchild	
				2.5 M	-12,5	TMS3132	TI	
200	2	SS	PMOS	1.5 M	-12,±5	2511	Signetics	
240	2	SS	PMOS	1.5 M	-12,5	2529	Signetics	
250	2	SS	PMOS	1.5 M	-12,5	2528	Signetics	
256	1	SS	Bipolar	30M	5	TDC1006J	TRW	
	2	SS	PMOS	1 M	-12,5	MM4056	†National	
				1.5 M	-12,5	MM5056 2527	National Signetics	50
				2.5 M	-12,5	AM2856C AM4056 AM5056	AMD †AMD AMD	
480	2	SS	NMOS	1.5 M	5	SY2535	Synertek	
						(Continued)		

Bits Per Register	No. of Reg.	Oper-ation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
Static (Cont'd)								
480	2	SS	NMOS	(Cont'd.) 3 M	5	SY2535A	Synertek	
512	1	SS	PMOS	1.0 M	-12,5	MM4057	†National	
				1.5 M	-12,5	MM5057	National	
				2.5 M	-12,5	AM2857C AM4057 AM5057	AMD †AMD AMD	60
	2	SS	NMOS	1.5 M	5	SY2534	Synertek	
				3 M	5	SY2534A	Synertek	
1024	1	SS	NMOS	1.5 M	5	SY2533	Synertek	
				2 M	5	SY2833	Synertek	
				3 M	5	SY2833A	Synertek	
				4 M	5	SY2833B	Synertek	
				5 M	5	SY2833C	Synertek	
			PMOS	1.5 M	-12,5	AM2533C 2533 MM5058 2533	AMD Fairchild National Signetics	70
				2 M	-12,5	AM2833C AM2833M	AMD †AMD	
				4 M	-12,5	3355C	Fairchild	
92304	1	SS	Bubble	0.1 M	—	TBM0103 91L40BM	TI †AMD	

† Military Temperature Range (−55° to 125°C)

SS = Serial In, Serial Out

PP = Parallel In, Parallel Out

* Typical Values

Bold face indicates additional data is provided on the page noted.

1024 Bit (1024×
Static High Speed VMOS RAI

Features

- Pin Compatible with 93415 (S4015) and 93425 (S4025)
- Single +5V Supply
- Directly TTL Compatible
- Open Collector Output — S4015
- Three State Output — S4025
- Fan-Out of 10 TTL — I_{OL} = 16mA @ 0.45V
- Completely Static — No Clocks or Refreshing

Absolute Maximum Ratings*

Ambient Temperature Under Bias	-10° C to +85° C
Storage Temperature	-65° C to +150° C
Output or Supply Voltages	-0.5V to +7V
Input Voltages	-0.5V to +5.5V
Power Dissipation	1 Watt

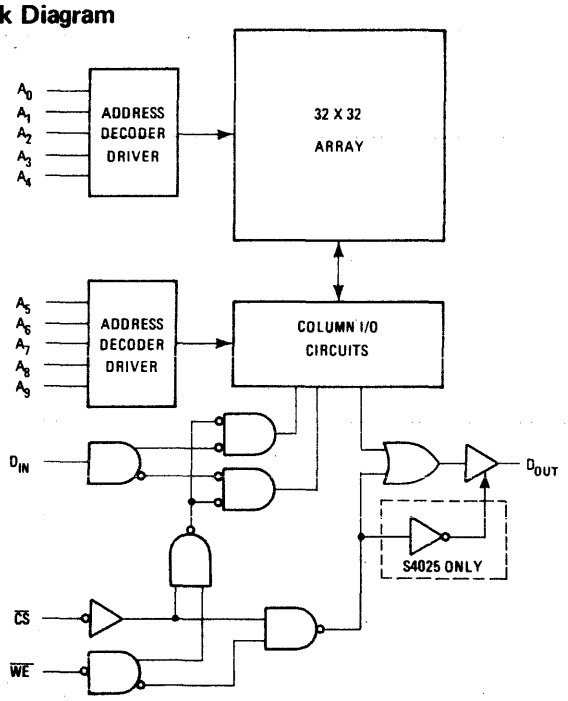
General Description

The AMI S4015/S4025 family of 1024x1 bit high spe VMOS RAMs offers fully static operation with a single supply. The device is completely TTL compatible on inputs and output. The family is available in two outp configurations. The S4015 has an open collector (op drain) output and the S4025 has a three state output. T stored data is read out nondestructively and is the sa polarity as the original input data.

The family is completely static requiring no clocks or freshing for operation. Chip Select (CS) controls the o put and simplifies memory system expansion. The f chip select time allows decoding the chip select from address without increasing address access time.

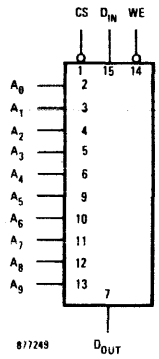
The S4015/S4025 is fabricated using AMI's propriet VMOS process, thus allowing the production of high spe MOS RAMs that are fully compatible with bipolar RA but offering the advantage of lower power dissipation.

Block Diagram

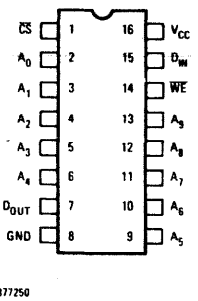


*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol



Pin Configuration



Pin Names

$\overline{CS}$	Chip Select	D_{IN}	Data Input
$A_0 - A_9$	Address Inputs	D_{OUT}	Data Output
$\overline{WE}$	Write Enable		

Truth Table

Inputs			Output (D_{OUT})		Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	S4015	S4025	
H	X	X	H	H — Z	Not selected
L	L	L	H	H — Z	Write "0"
L	L	H	H	H — Z	Write "1"
L	H	X	D_{OUT}	D_{OUT}	Read

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MEMORY–Shift Registers (Cont'd)

Static (Cont'd)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
100	2	SS	PMOS	1.6 M	-12,5	(Cont'd.)		
						MM5053	National	
				2 M	-12,5	SL5-C2100	GI	
	4	SS	PMOS	2.2 M	-12,5	MM5061	National	
20-100	2	SS	PMOS	2.5 M	-12,5	MM4007	National	
125	1	SS	PMOS	1 M	-12,5	ITT1144	ITT	
128	1	SS	CMOS	5 M	12	MS625	RTC	
	2	SS	PMOS	1 M	-12,5	MK1002	AMD	
						MK1002	Mostek	
						SL5-2128	GI	10
				1.5 M	-12,5	2521	Signetics	
						MTS2107	†MOS	
						MM5060AA	National	
				2 M	-12,5	AM2809M	†AMD	
						AM2810	AMD	
						TMS3114	AMD	
						SL5-C2128	GI	
						MTS2108	†MOS	
						TMS3114	TI	
				2.5 M	-12,5	AM2809C	AMD	20
						AM2814M	†AMD	
						TMS3128	TI	
	4	SS	PMOS	1 M	-12,5	MM4055	†National	
				1.5 M	-12,5	MM5055	National	
				2.5 M	-12,5	AM2855	AMD	
						AM4055	†AMD	
						AM5055	AMD	
16-128	1	SS	CMOS	5.6 M	3-15	MC14562B	Motorola	
132	2	SS	PMOS	1.5 M	-12,5	MM5060AB	National	
						2522	Signetics	30
				2.5 M	-12,5	TMS3129	TI	
133	2	SS	PMOS	1.5 M	-12,5	MM5060AC	National	
				2 M	-12,5	TMS3113	TI	
				2.5 M	-12,5	TMS3130	TI	
	4	SS	NMOS	1 M	5	SR5015-133	SMC	
						SR5017	SMC	
1-134	4	SS	NMOS	1 M	5	SR5015	SMC	
125 144								
	2	SS	PMOS	1.5 M	-12,5	MM5060	National	
144	1	SS	PMOS	1 M	-12,5	ITT1144	ITT	40
	2	SS	PMOS	1.5 M	-12,5	MM5060AD	National	
				2 M	-12,5	3346	Fairchild	
				2.5 M	-12,5	TMS3132	TI	
200	2	SS	PMOS	1.5 M	-12,±5	2511	Signetics	
240	2	SS	PMOS	1.5 M	-12,5	2529	Signetics	
250	2	SS	PMOS	1.5 M	-12,5	2528	Signetics	
256	1	SS	Bipolar	30M	5	TDC1006J	TRW	
	2	SS	PMOS	1 M	-12,5	MM4056	†National	
				1.5 M	-12,5	MM5056	National	
						2527	Signetics	50
				2.5 M	-12,5	AM2856C	AMD	
						AM4056	†AMD	
						AM5056	AMD	
480	2	SS	NMOS	1.5 M	5	SY2535	Synertek	

(Continued)

Static (Cont'd)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
480	2	SS	NMOS	(Cont'd.)				
				3 M	5	SY2535A	Synertek	
512	1	SS	PMOS	1.0 M	-12,5	MM4057	†National	
				1.5 M	-12,5	MM5057	National	
				2.5 M	-12,5	AM2857C	AMD	
						AM4057	†AMD	60
						AM5057	AMD	
	2	SS	NMOS	1.5 M	5	SY2534	Synertek	
				3 M	5	SY2534A	Synertek	
1024	1	SS	NMOS	1.5 M	5	SY2533	Synertek	
				2 M	5	SY2833	Synertek	
				3 M	5	SY2833A	Synertek	
				4 M	5	SY2833B	Synertek	
				5 M	5	SY2833C	Synertek	
			PMOS	1.5 M	-12,5	AM2533C	AMD	
						2533	Fairchild	70
						MM5058	National	
						2533	Signetics	
				2 M	-12,5	AM2833C	AMD	
						AM2833M	†AMD	
				4 M	-12,5	3355C	Fairchild	
92304	1	SS	Bubble	0.1 M	—	TBM0103	TI	
						91L40BM	†AMD	

† Military Temperature Range (−55° to 125°C)

SS = Serial In, Serial Out

PP = Parallel In, Parallel Out

* Typical Values

Bold face indicates additional data is provided on the page noted.

Random Access Memories

Part No.	Description	Process	Organization	Maximum T_{ACC} (ns)	Maximum I_{CC} (mA)	Power Supplies	Packages*
S2114	4096 Bit Static RAM	VMOS	1024x4	200	100	+5V	18 Pin P, E, C
S4015-2	1024 Bit Static RAM	VMOS	1024x1	60	125	+5V	16 Pin P, E, C
S4015-3	1024 Bit Static RAM	VMOS	1024x1	45	100	+5V	16 Pin P, E, C
S4015-4	1024 Bit Static RAM	VMOS	1024x1	45	125	+5V	16 Pin P, E, C
S4015-5	1024 Bit Static RAM	VMOS	1024x1	35	135	+5V	16 Pin P, E, C
S4016	4096 Bit Static RAM	VMOS	1024x4	200	100	+5V	18 Pin P, E, C
S4017-1	4096 Bit Static RAM	VMOS	4096x1	90	160	+5V	18 Pin P, E, C
S4017-2	4096 Bit Static RAM	VMOS	4096x1	70	160	+5V	18 Pin P, E, C
S4017-3	4096 Bit Static RAM	VMOS	4096x1	55	180	+5V	18 Pin P, E, C
S4017-4	4096 Bit Static RAM	VMOS	4096x1	55	150	+5V	18 Pin P, E, C
S4025-2	1024 Bit Static RAM	VMOS	1024x1	60	125	+5V	16 Pin P, E, C
S4025-3	1024 Bit Static RAM	VMOS	1024x1	45	100	+5V	16 Pin P, E, C
S4025-4	1024 Bit Static RAM	VMOS	1024x1	45	125	+5V	16 Pin P, E, C
S4025-5	1024 Bit Static RAM	VMOS	1024x1	35	135	+5V	16 Pin P, E, C
S5101	1024 Bit Static RAM	CMOS	256x4	650	22	+5V	22 Pin P, E, C
S5101-1	1024 Bit Static RAM	CMOS	256x4	450	22	+5V	22 Pin P, E, C
S5101-3	1024 Bit Static RAM	CMOS	256x4	650	22	+5V	22 Pin P, E, C
S5101-8	1024 Bit Static RAM	CMOS	256x4	800	22	+5V	22 Pin P, E, C
S5101L	1024 Bit Static RAM	CMOS	256x4	650	22	+5V	22 Pin P, E, C
S5101L-1	1024 Bit Static RAM	CMOS	256x4	450	22	+5V	22 Pin P, E, C
S5101L-3	1024 Bit Static RAM	CMOS	256x4	650	22	+5V	22 Pin P, E, C
S6508	1024 Bit Static RAM	CMOS	1024x1	460	2	+5V	16 Pin P, E, C
S6508-1	1024 Bit Static RAM	CMOS	1024x1	300	2	+5V	16 Pin P, E, C
S6508A	1024 Bit Static RAM	CMOS	1024x1	185	2 to 4.3	+4V to +11V	16 Pin P, E, C
S6508A-1	1024 Bit Static RAM	CMOS	1024x1	115	2 to 4.3	+4V to +11V	16 Pin P, E, C
S68A10	1024 Bit RAM	N-SiGate	128x8	360	80	+5V	24 Pin Side Brazed
S68B10	1024 Bit RAM	N-SiGate	128x8	250	80	+5V	24 Pin Side Brazed

Read Only Memories and Erasable and Electrically Reprogrammable Read Only Memories

Part No.	Description	Process	Organization	Maximum T_{ACC} (ns)	Maximum I_{CC} (mA)	Power Supplies	Packages*
S4216B	16,384 Bit Static ROM	VMOS	2048x8	250	80	+5V ± 10%	24 Pin P, E, C
S4264	65,536 Bit Static ROM	VMOS	8192x8	350	145	+5V ± 10%	24 Pin P, E, C
S5204A	4096 Bit EPROM	P-SiGate	512x8	750	50	+5V, -12V	24 Pin C
S6831	16,384 Bit ROM	N-SiGate	2048x8	450	30	+5V	24 Pin P, E, C
S6831A	16,384 Bit ROM	N-SiGate	2048x8	450	30	+5V	24 Pin P, E, C
S6831B	16,384 Bit ROM	N-SiGate	2048x8	450	30	+5V	24 Pin P, E, C
S6831C	16,384 Bit ROM	N-SiGate	2048x8	450	30	+5V	24 Pin P, E, C
S6834	4096 Bit EPROM	P-SiGate	512x8	500	50	+5V, -12V	24 Pin C

* (P) = Plastic Package, (E) = Cer-DIP Package, (C) = Ceramic Package

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VMOS—The New Technology from AMI

VMOS is the patented new technology developed by AMI to produce low-cost, high-density integrated circuits with a process that yields products with very high operating speeds. VMOS has literally opened up a new dimension in the design and manufacture of electronic memory and other circuits for large computer systems, minicomputer systems, microcomputers, microprocessors and hundreds of other applications for consumer and communications products employing large scale integrated circuits.

The first product manufactured at AMI using the VMOS technology was the S4015 1Kx1 static RAM. Having proved the viability of VMOS for static RAMs, AMI started numerous designs in both random access memories and read only memories. These new designs will also undergo extensive quality and reliability tests.

The secret of VMOS is a process which produces tens of thousands of transistors in an integrated circuit as tiny V-shaped grooves. The acronym "VMOS" stands for V-groove Metal-Oxide-Silicon. Metal, oxide and silicon comprise the layers making up the transistors in the most widely manufactured types of LSI circuits. The VMOS process, unlike others, deposits these layers into the small three-dimensional grooves rather than over a larger two-dimensional area on the small piece of silicon that comprises a complete integrated circuit.

The VMOS process produces very small circuits hence many more per wafer than competitive processes such as N-channel MOS and digital bipolar. Because VMOS takes advantage of the third dimension of the wafer and employs special processing techniques, VMOS transistors are smaller than competing types of technologies. The result is high density VMOS circuits which are very fast and as much as 50 percent smaller (and more economical) than circuits made with other technologies.

Ordering Information

Any product in this Condensed MOS Products Catalog can be ordered using the simple system described below. With this system it is possible to completely specify any standard device in this catalog in a manner that is compatible with AMI's order processing methods. The example below shows how this ordering system works and will help you to order your parts in a manner that can be expedited rapidly and accurately.

All orders (except those in sample quantities) are normally shipped in plastic carriers or aluminum tube containers, which protect the devices from static electricity damage under all normal handling conditions. Either container is compatbile with standard automatic IC handling equipment.

Any device described in this catalog is an AMI Standard Product. However, ROM devices that require mask preparation or programming to the requirements of a particular user, devices that must be tested to other than AMI Quality Assurance standard procedures, or other devices requiring special masks are sold on a negotiated price basis.

S 6 8 2 0 A — 1 P

Device Number — prefix S, followed by four numeric digits that define the basic device type. If there are versions to the basic device, the four numeric digits will be followed by additional alphanumeric digits, in this example A-1. The last digit should always be followed by a space.

Package Type — a single letter designation which identifies the basic package type. The letters are coded as follows:

P — Plastic package

E — Cer-DIP package

S — SLAM package

C — Ceramic (three-layer) package

T — TO type package

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1024 Bit (1024×1) Static High Speed VMOS RAM

Features

- Pin Compatible with 93415 (S4015) and 93425 (S4025)
- Single +5V Supply
- Directly TTL Compatible
- Open Collector Output — S4015
- Three State Output — S4025
- Fan-Out of 10 TTL — I_{OL} = 16mA @ 0.45V
- Completely Static — No Clocks or Refreshing

Absolute Maximum Ratings*

Ambient Temperature Under Bias	-10° C to +85° C
Storage Temperature	-65° C to +150° C
Output or Supply Voltages	-0.5V to +7V
Input Voltages	-0.5V to +5.5V
Power Dissipation	1 Watt

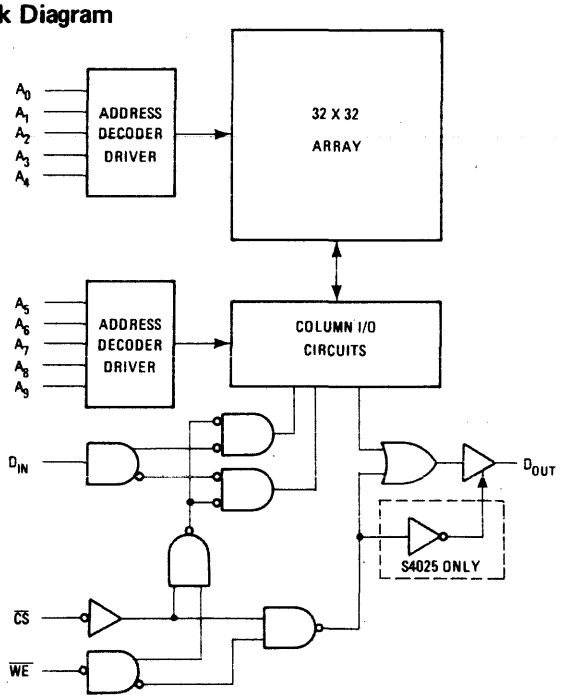
General Description

The AMI S4015/S4025 family of 1024x1 bit high speed VMOS RAMs offers fully static operation with a single 5V supply. The device is completely TTL compatible on all inputs and output. The family is available in two output configurations. The S4015 has an open collector (open drain) output and the S4025 has a three state output. The stored data is read out nondestructively and is the same polarity as the original input data.

The family is completely static requiring no clocks or refreshing for operation. Chip Select (CS) controls the output and simplifies memory system expansion. The fast chip select time allows decoding the chip select from the address without increasing address access time.

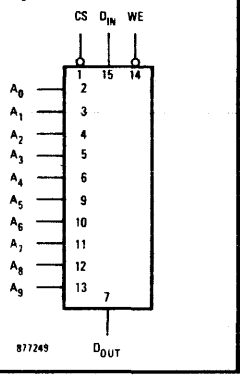
The S4015/S4025 is fabricated using AMI's proprietary VMOS process, thus allowing the production of high speed MOS RAMs that are fully compatible with bipolar RAMs but offering the advantage of lower power dissipation.

Block Diagram

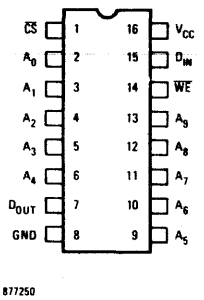


*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol



Pin Configuration



Pin Names

$\overline{CS}$	Chip Select	D_{IN}	Data Input
$A_0 - A_9$	Address Inputs	D_{OUT}	Data Output
$\overline{WE}$	Write Enable		

Truth Table

Inputs			Output (D_{OUT})		Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	S4015	S4025	
H	X	X	H	H — Z	Not selected
L	L	L	H	H — Z	Write "0"
L	L	H	H	H — Z	Write "1"
L	H	X	D_{OUT}	D_{OUT}	Read

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D. C. Characteristics: V_{CC} = 5V ± 5%, T_A = 0°C to 75°C.

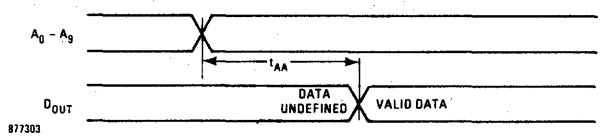
Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage				0.45	V	V_{CC}=Min, I_{OL}=16mA
V_{OH}	Output HIGH Voltage (S4025 Family)		2.4			V	V_{CC}=Min, I_{OH}=-5.2mA
V_{IL}	Input LOW Voltage				0.8	V	
V_{IH}	Input HIGH Voltage		2.0			V	
I_{IL}	Input LOW Current				-40	μA	V_{CC}=Max, V_{IN}=0.4V
I_{IH}	Input HIGH Current				40	μA	V_{CC}=Max, V_{IN}=4.5V
I_{CEX}	Output Leakage Current (S4015 Family)				50	μA	V_{CC}=Max, V_{OUT}=4.5V
I_{OFF}	Output Current (High Z — (S4025 Family)				50	μA	V_{CC}=Max, V_{OUT}=2.4V
					-50	μA	V_{CC}=Max, V_{OUT}=0.5V
I_{OS}	Output Current Short Circuit to Ground (S4025 Family)				-100	mA	V_{CC}=Max, for not more than 1 second
I_{CC}	Power Supply Current	S4015 (25) -3			100	mA	V_{CC}=Max
		S4015 (25) -2,4			125	mA	All Inputs Grounded
		S4015 (25) -5			135	mA	Output Open

Capacitance

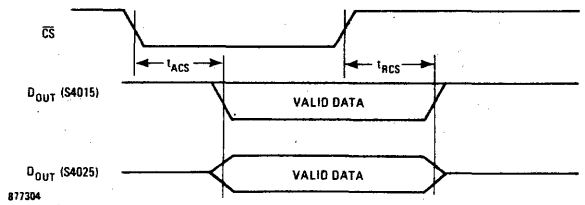
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			5	pF	All inputs=0V
C_{OUT}	Output Capacitance			8	pF	Output=0V

Read Cycle

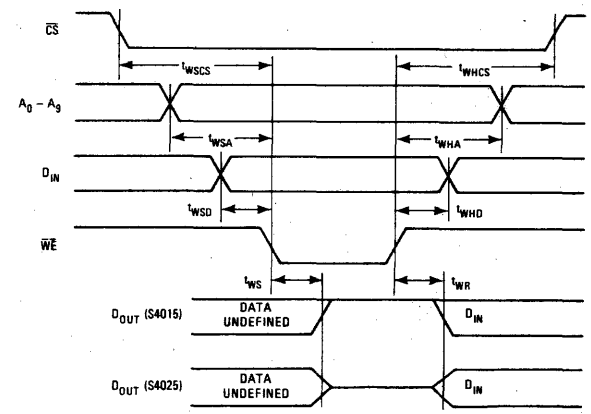
Propagation Delay From Address Inputs



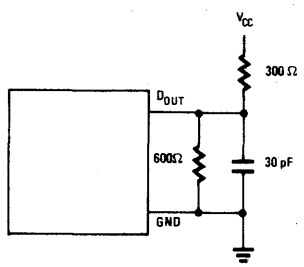
Propagation Delay From Chip Select



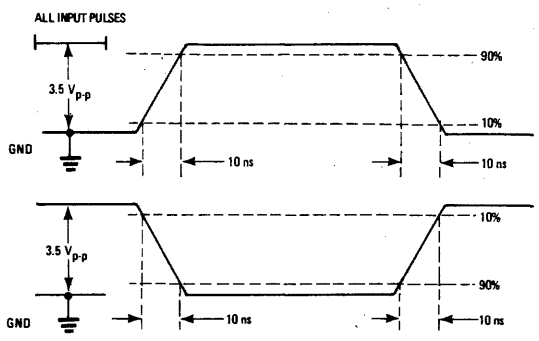
Write Cycle



A.C. Test Load



A.C. Test Conditions



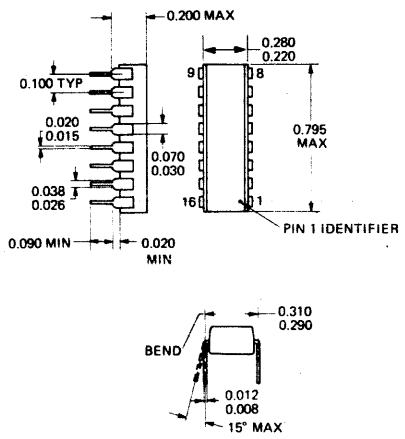
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A.C. Characteristics: V_{CC} = 5V ± 5%, T_A = 0°C to 75°C

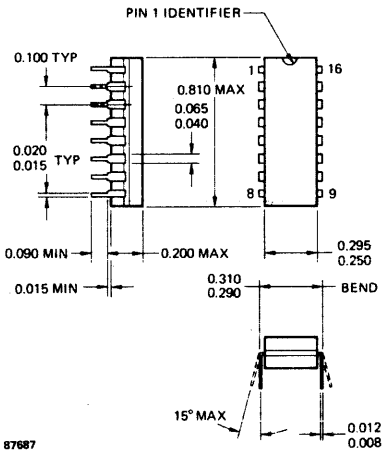
Symbol	Parameter	S4015(25) - 5 Min.	S4015(25) - 5 Typ.	S4015(25) - 5 Max.	S4015(25) - 3,4 Min.	S4015(25) - 3,4 Typ.	S4015(25) - 3,4 Max.	S4015(25) - 2 Min.	S4015(25) - 2 Typ.	S4015(25) - 2 Max.	Units	Conditions
READ CYCLE												
t_{ACS}	Chip Select Time			25			30			40	ns	See Test
t_{RCS}	Chip Select Recovery Time			25			30			40	ns	Circuit &
t_{AA}	Address Access Time			35			45			60	ns	Waveforms
WRITE CYCLE												
t_{WS}	Write Disable Time			25			35			40	ns	
t_{WR}	Write Recovery Time	0		25	0		35	0		40	ns	
t_W	Write Pulse Width	25			30			40			ns	See Test
t_{WSD}	Data Set-up Time Prior to Write	5			5			5			ns	Circuit & Waveforms
t_{WHD}	Data Hold Time After Write	5			5			5			ns	
t_{WSA}	Address Set-up Time	5			5			5			ns	
t_{WHA}	Address Hold Time	5			5			5			ns	
t_{WSCS}	Chip Select Set-up Time	5			5			5			ns	
t_{WHCS}	Chip Select Hold Time	5			5			5			ns	

Physical Dimensions

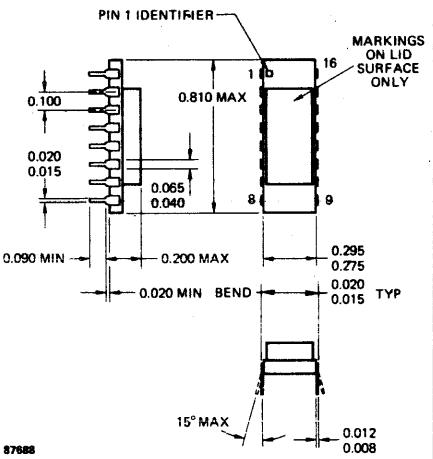
16-Pin Plastic



16-Pin Cer-DIP



16-Pin Ceramic



Ordering Information

Device	Output	T_{AA} (ns) Max.	I_{CC} (mA) Max.	Order Number Plastic	Order Number Cer-DIP	Order Number Ceramic
S4015 — 2	O.C.	60	125	S40152P	S40152E	S40152C
S4015 — 3	O.C.	45	100	S40153P	S40153E	S40153C
S4015 — 4	O.C.	45	125	S40154P	S40154E	S40154C
S4015 — 5	O.C.	35	135	S40155P	S40155E	S40155C
S4025 — 2	T.S.	60	125	S40252P	S40252E	S40252C
S4025 — 3	T.S.	45	100	S40253P	S40253E	S40253C
S4025 — 4	T.S.	45	125	S40254P	S40254E	S40254C
S4025 — 5	T.S.	35	135	S40255P	S40255E	S40255C

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4096 Bit (1024×4) Static VMOS RAM

Features

- ☐ High Density 18 Pin Package
- ☐ Single +5V Supply
- ☐ Completely Static Operation: No Clocks Required
- ☐ Completely TTL Compatible
- ☐ Common Data I/O: Three State Outputs
- ☐ High Speed Operation: Access Time: 200ns Maximum
- ☐ Fan-Out of 5 TTL – I_{OL} = 8mA @ 0.4V

Absolute Maximum Ratings*

Ambient Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin With Respect to Ground	-0.5V to 7V
Power Dissipation	1W

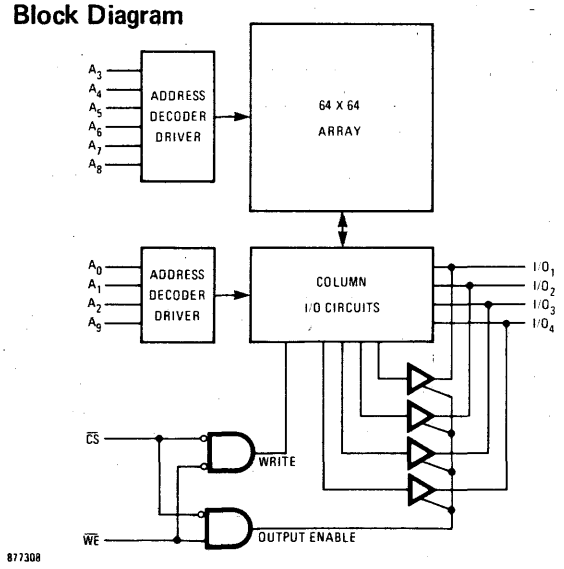
General Description

The AMI S4016 is a 4096 bit fully static RAM organized as 1024 words by 4 bits. The device is fully TTL compatible on all inputs and outputs and has a single + 5V supply. The common data input/output pins facilitate interface with systems utilizing a bidirectional data bus. The stored data is read out non-destructively and is the same polarity as the original input data.

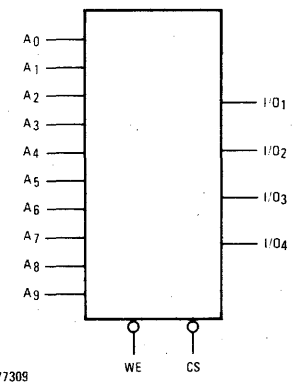
The S4016 is fully static requiring no clocks or refreshing for operations. This simplifies device operation as no address setup times are required. The chip select function facilitates memory system expansion by allowing the input/output pins to be OR-tied to other devices.

The S4016 is fabricated using AMI's proprietary VMOS technology. This process permits the manufacture of high performance memory devices suitable for high volume production.

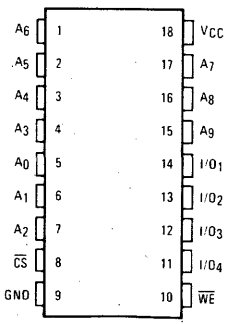
Block Diagram



Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{11}$	Address Inputs	$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select	V_{CC}	+5V Power
$I/O_1 - I/O_4$			Data Input/Output

Truth Table

Inputs				Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	
H	X	X	H – Z	Not Selected
L	L	L	H – Z	Write "0"
L	L	H	H–Z	Write "1"
L	H	X	D_{OUT}	Read

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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D.C. Operating Characteristics: V_{CC} = 5V ± 5%; T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0V to 5.25V
I_{LO}	I/O Leakage Current			10	μA	$\overline{CS}$ = 2.4V $V_{I/O}$ = 0.4V to V_{CC}
I_{CC}	Power Supply Current			95	mA	V_{IN}=5.25V T_A=25°C
				100	mA	V_{IN}=5.25V T_A=0°C
V_{IL}	Input LOW Voltage	-0.3		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 8mA
V_{OH}	Output HIGH Voltage	2.4		V_{CC}	V	I_{OH} = -1mA

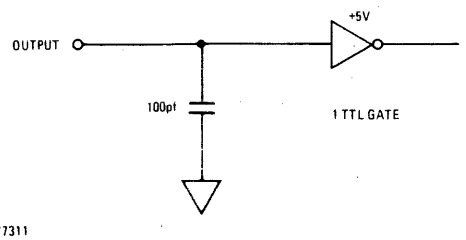
Capacitance: T_A = 25°C; f = 1.0 MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$C_{I/O}$	Input/Output Capacitance			5	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance			5	pF	V_{IN} = 0V

A.C. Characteristics: V_{CC} = 5V ± 5%; T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{CYC}	Read or Write Cycle Time	200			ns	
t_{ACC}	Address Access Time			200	ns	
t_{OHA}	Output Hold from Address	50			ns	
t_{CS}	Chip Select Access Time			70	ns	See Test Circuit
t_{OFF}	Output H-Z from Chip Select			60	ns	and
t_{AWS}	Address Write Setup Time	0			ns	Waveforms
t_W	Write Time	120			ns	
t_{WR}	Write Recovery Time	0			ns	
t_{OTW}	Output H-Z from Write Enable			60	ns	
t_{DWS}	Data Setup Time	120			ns	
t_{DWH}	Data Hold Time	0			ns	
t_{CX}	Chip Select to Output Active	20			ns	

A.C. Test Load

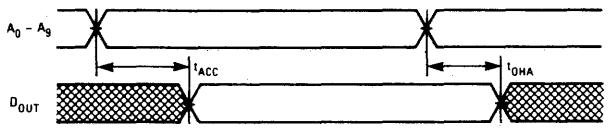


A.C. Test Conditions

Input Pulse Levels	0.8V to 2.4V
Input Rise & Fall Times	10 ns
Input and Output Timing Level	1.5V

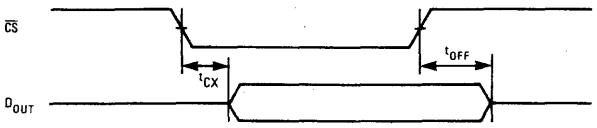
Read Cycle (note 1)

Propagation Delay From Address Inputs



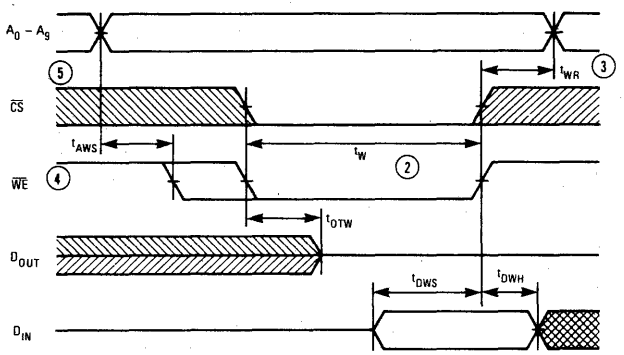
877312

Propagation Delay from Chip Select



877313

Write Cycle



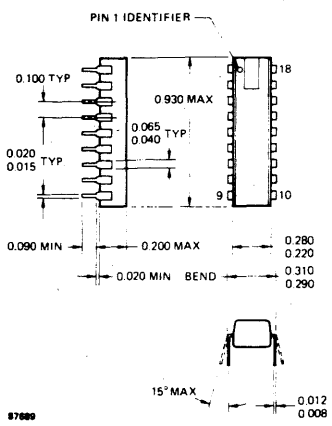
877314

NOTES:

1. A read occurs during the overlap of a LOW $\overline{CS}$ and a HIGH $\overline{WE}$.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is referenced to the positive transition of $\overline{WE}$.
4. $\overline{WE}$ must be HIGH during all address transitions.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with the $\overline{WE}$ LOW transition, then the output buffers remain in the high impedance state.

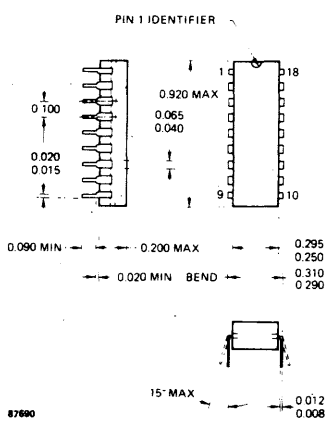
Physical Dimensions

18-Pin Plastic



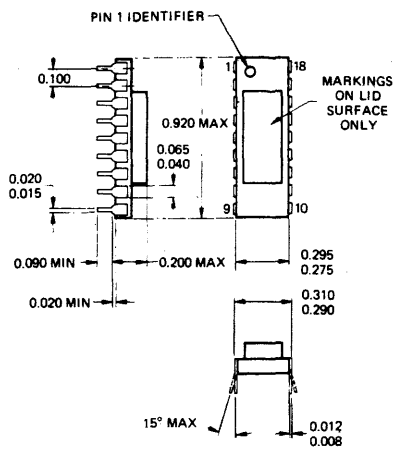
87689

18-Pin Cer-Dip



87690

18-Pin Ceramic



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4096 Bit (4096×1) Static VMOS RAM

Features

- ☐ High Density 18 Pin Package
- ☐ Single +5V Power Supply
- ☐ Completely Static Operation: No Clocks Required
- ☐ Completely TTL Compatible Inputs
- ☐ TTL Compatible Three-State Output
- ☐ High Speed Operation: 55ns Max. Access Time (S4017 — 4)
- ☐ Fan-out of 5 TTL - I_{OL} = 8mA @0.4V

Absolute Maximum Ratings*

Ambient Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin With Respect to Ground	-0.5V to 7V
Power Dissipation	1W

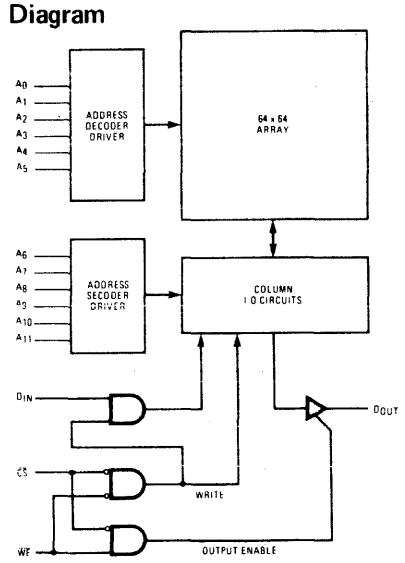
General Description

The AMI 4017 is a 4096 bit fully static RAM organized as 4096 one-bit words. The device is fully TTL compatible on all inputs and the output and has a single + 5V power supply. It has separate data input and output pins for maximum design flexibility. The stored data is read out nondestructively and is the same polarity as the original input data.

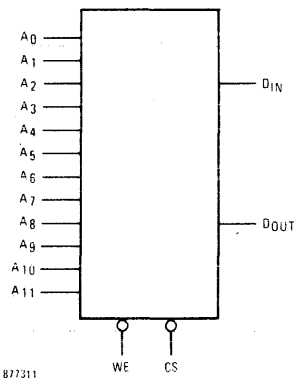
The S4017 is fully static requiring no clocks or refreshing for operation. This simplifies device operation as no address setup times are required. The chip select function facilitates memory system expansion by allowing the data output pin to be OR-tied to other devices.

The S4017 is fabricated using AMI's proprietary VMOS technology. The process permits the manufacture of high performance memory devices suitable for high volume production.

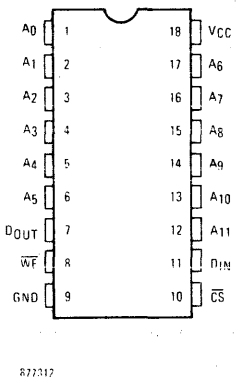
Block Diagram



Logic Symbol



Pin Configuration



Pin Names

A_0 - A_{11}	Address Inputs	D_{IN}	Data Input
$\overline{CS}$	Chip Select	D_{OUT}	Data Output
$\overline{WE}$	Write Enable	V_{CC}	+5V Power

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	
H	X	X	H-Z	Not Selected
L	L	L	H-Z	Write "0"
L	L	H	H-Z	Write "1"
L	H	X	D_{OUT}	Read

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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D.C. Characteristics: V_{CC} = 5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage				0.45	V	I_{OL} = 16mA
V_{OH}	Output HIGH Voltage		2.4			V	I_{OH} = -5.2mA
V_{IL}	Input LOW Voltage				0.8	V	
V_{IH}	Input HIGH Voltage		2.0			V	
I_{LI}	Input Leakage Current				10	μA	V_{CC} = Max., V_{IN} = 0 to V_{CC}
$\|I_{LO}\|$	Output Leakage Current				50	μA	$\overline{CS}$ = 2.0V, V_{CC} = Max., V_{OUT} = 0 to 4.5V
I_{OS}	Output Current Short Circuit to Ground				-100	mA	V_{CC} = Max., for not more than one second.
I_{CC}	Power Supply Current	S4017-4			150	mA	V_{CC} = Max., $\overline{CS}$ = V_{IL}, Output Open
		S4017-3			180	mA	
		S4017-2 (-1)			160	mA	

Capacitance: T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			8	pF	V_{OUT} = 0V

A.C. Characteristics: T_A = 0°C to 75°C, V_{CC} = +5V ± 5%

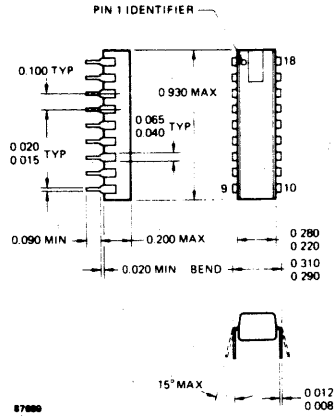
Read Cycle		S4017-3-4		S4017-2		S4017-1			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units	Conditions
t_{RC}	Read Cycle Time	55		70		90		ns	See A.C. test condition and waveform
t_{AA}	Address Access Time		55		70		90	ns	
t_{ACS}	Chip Select Access Time		30		40		50	ns	
t_{OH}	Output Hold from Address Change	10		10		10		ns	
t_{LZ}	Chip Select to Output L — Z	10		10		10		ns	
t_{HZ}	Chip Select to Output H — Z		25		30		40	ns	

Write Cycle		S4017-3-4		S4017-2		S4017-1			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units	Conditions
t_{WC}	Write Cycle Time	55		70		90		ns	See A.C. test conditions and waveforms
t_{CW}	Chip Select to End of Write	30		35		55		ns	
t_{AW}	Address Valid to End of Write	40		45		65		ns	
t_{AS}	Address Setup Time	10		10		15		ns	
t_{WP}	Write Pulse Width	25		25		35		ns	
t_{WR}	Write Recovery Time	15		25		25		ns	
t_{DW}	Data Valid to End of Write	25		25		35		ns	
t_{DH}	Data Hold Time	10		10		10		ns	
t_{WZ}	Write Enable to Output HZ		25		30		40	ns	
t_{OW}	Output Active from End of Write	0	25	0	30	0	40	ns	

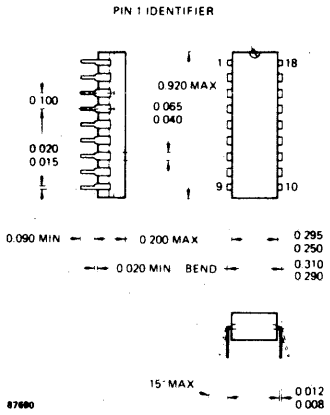
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Physical Dimensions

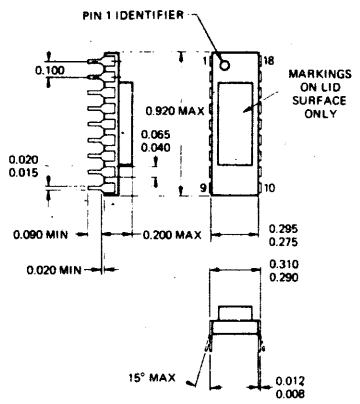
18-Pin Plastic



18-Pin Cer-Dip

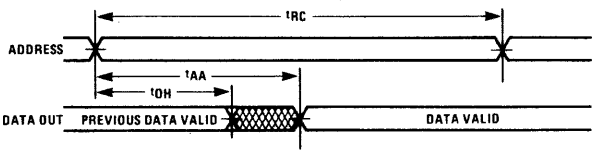


18-Pin Ceramic

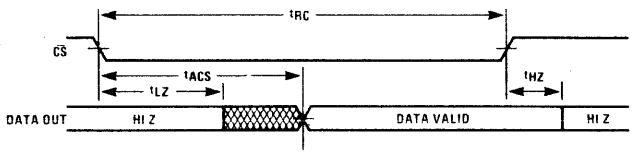


Read Cycle

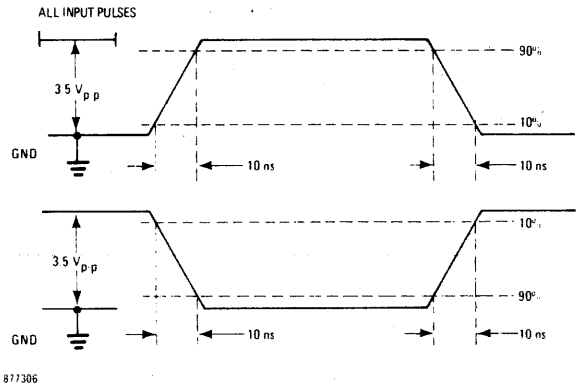
Propogation Delay From Address Inputs



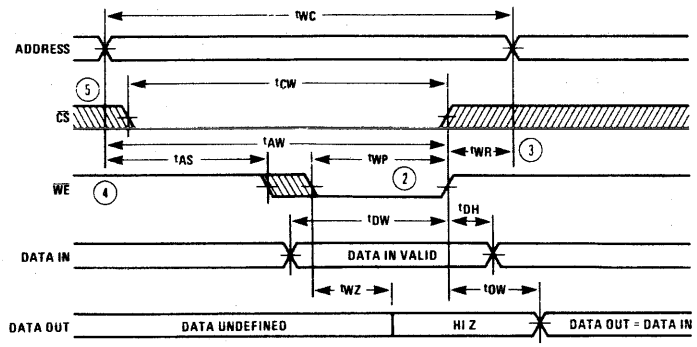
Propogation Delay From Chip Select



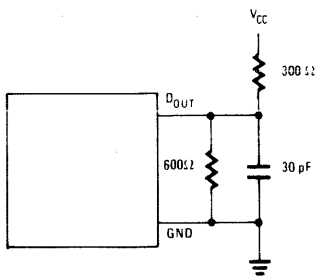
A.C. Test Conditions



Write Cycle



A.C. Test Load



NOTES:

1. A read occurs during the overlap of a LOW $\overline{CS}$ and a HIGH $\overline{WE}$.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is referenced to the positive transition of $\overline{WE}$.
4. $\overline{WE}$ must be HIGH during all address transitions.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with the $\overline{WE}$ LOW transition, then the output buffers remain in the high impedance state.

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1024 Bit (256×4) Static CMOS RAM

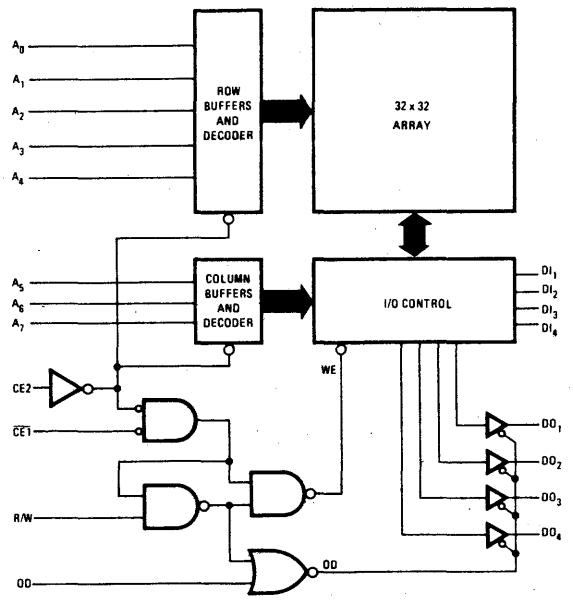
Features

- ☐ Ultra Low Standby Power
- ☐ Data Retention at 2V (5101L)
- ☐ Single +5 Volt Power Supply
- ☐ Completely Static Operation
- ☐ Completely TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs

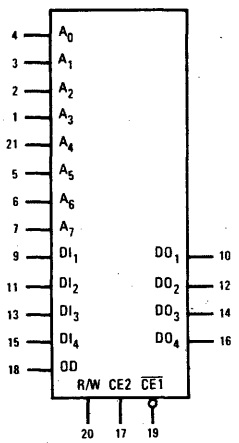
General Description

The AMI S5101 family of 256 x 4-bit ultra low power CMOS RAMs offers fully static operation with a single + 5 volt power supply. All inputs and outputs are directly TTL compatible. With data inputs and outputs on adjacent pins, either separate or common data I/O operations can easily be implemented for maximum design flexibility. The three-state outputs will drive one full TTL load and are disabled (high impedance state) by output disable (OD), either chip enable ($\overline{CE1}$ or CE2), or in a write cycle (R/W = LOW). This facilitates the control of common data I/O systems.

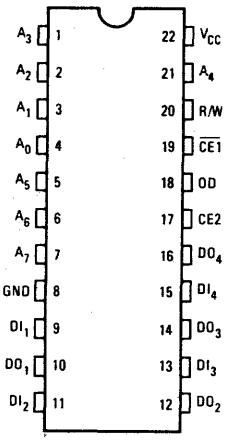
Block Diagram



Logic Symbol



Pin Configuration



Truth Table

$\overline{CE1}$	CE2	OD	R/W	D_{IN}	Output	Mode
H	X	X	X	X	High Z	Not Selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Out Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	High Z	Write
L	H	L	H	X	D_{out}	Read

Pin Names

A_0 - A_7	Address Inputs	$\overline{CE1}$	Chip Enable
DI_1 - DI_4	Data Inputs	CE2	Chip Enable
DO_1 - DO_4	Data Outputs	R/W	Read/Write Input
OD	Output Disable	V_{CC}	+5 Volt Power Supply

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General Description (Continued)

The stored data is read out nondestructively and is the same polarity as the original input data. The S5101 is totally static, making clocks unnecessary for a new address to be accepted. The device has two chip enable inputs ($\overline{CE1}$ and CE2) allowing easy system expansion. CE2 disables the entire device but $\overline{CE1}$ does not disable the address buffers and decoders. Thus, minimum power dissipation is achieved when CE2 is low.

When deselected (CE2 = LOW), the S5101 draws less than 10 microamps from the 5 volt power supply. The S5101L is identical to the S5101 but has the additional feature of guaranteed data retention with the power supply as low as 2 volts. This makes the device an ideal choice when battery augmented non-volatile RAM storage is mandatory.

The S5101 is fabricated using a silicon gate CMOS process suitable for high volume production of ultra low power, high performance memories.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage	11V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics: T_A = 0°C to 70°C, V_{CC} = 5V ± 5% (Unless otherwise specified)

Symbol	Parameter		Limits Min.	Limits Max.	Units	Conditions
I_{LI}	Input Leakage Current			1	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			1	μA	$\overline{CE1}$ = V_{IH} V_{OUT} = 0V to V_{CC}
I_{CC}	Operating Supply Current			22	mA	Outputs = Open, V_{IN} = V_{IL} to V_{CC}
I_{CCL}	Standby Supply Current	S5101-1, S5101		10	μA	V_{IN} = 0V to V_{CC} except CE2 ⩽ 0.2V
		S5101-3		140	μA	
		S5101-8		500	μA	
V_{IL}	Input Low Voltage		-0.3	0.65	V	
V_{IH}	Input High Voltage		2.2	V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage		2.4		V	I_{OH} = -1 mA

Capacitance

Symbol	Parameter	Limits Min.	Limits Max.	Units	Conditions
C_{IN}	Input Capacitance		8	pF	V_{IN} = 0V, on all Input Pins
C_O	Output Capacitance		12	pF	V_O = 0V

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A.C. Characteristics for Read Cycle: T_A = 0°C to 70°C, V_{CC} = 5V ± 5% (Unless otherwise specified)

Symbol	Parameter	S5101-1, S5101L-1 Limits		S5101, S5101L S5101-3, S5101L-3 Limits		S5101-8 Limits		Units	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
T_{RC}	Read Cycle Time	450		650		800		ns	See A.C. Conditions of Test and A.C. Test Load
T_{ACC}	Access Time		450		650		800	ns	
T_{CO1}	$\overline{CE1}$ to Output Delay		400		600		800	ns	
T_{CO2}	CE2 to Output Delay		500		700		850	ns	
T_{OD}	Output Disable to Enabled Output Delay		250		350		450	ns	
T_{DF}	Output Disable to Output H-Z State Delay	0	130	0	150	0	200	ns	
T_{OH1}	Output Data Valid Into Next Cycle with respect to Address	0		0		0		ns	
T_{OH2}	Output Data Valid Into Next Cycle with respect to Chip Enable	0		0		0		ns	

A.C. Characteristics for Write Cycle — Separate or Common Data I/O Using Output Disable

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% (Unless otherwise specified)

Symbol	Parameter	S5101-1, S5101L-1 Limits		S5101, S5101L, S5101-3 S5101L-3 Limits		S5101-8 Limits		Units	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
T_{WC}	Write Cycle Time	450		650		800		ns	See A.C. Conditions of Test and A.C. Test Load
T_{AW}	Address To Write Delay	130		150		200		ns	
T_{CW1}	CE1 to Write Delay	350		550		650		ns	
T_{CW2}	CE2 to Write Delay	350		550		650		ns	
T_{DW}	Data Set-Up to End of Write Time	250		400		450		ns	
T_{DH}	Data Hold After End of Write Time	50		100		100		ns	
T_{WP}	Write Pulse Width	250		400		450		ns	
T_{WR}	End of Write to New Address Recovery Time	50		50		100		ns	
T_{DS}	Output Disable to Data-In Set-Up Time	130		150		200		ns	

Low V_{CC} Data Retention Characteristics for S5101L, S5101L-1, S5101L-3[1]

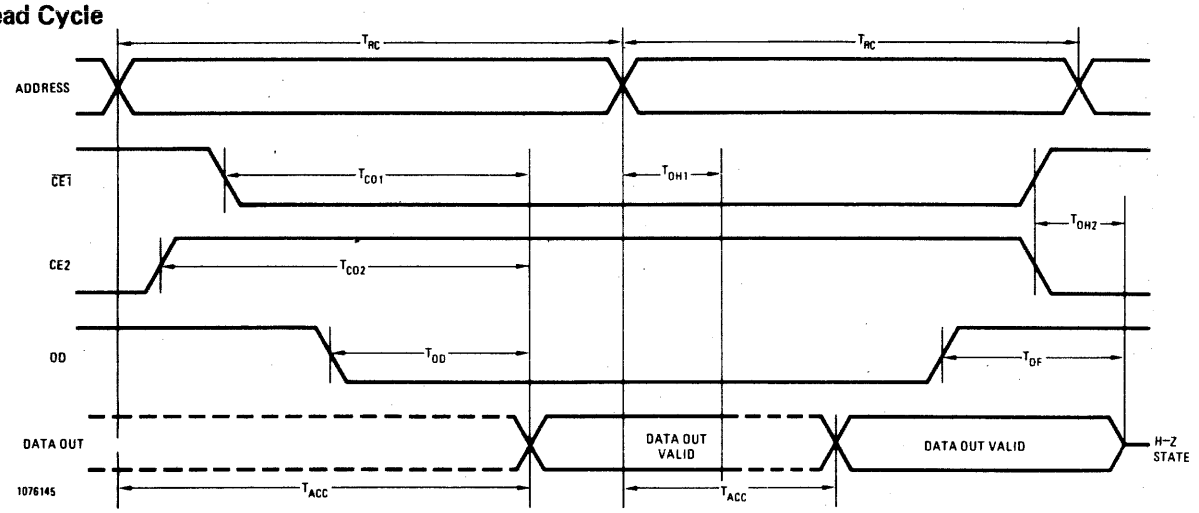
T_A = 0°C to 70°C

Symbol	Parameter		Limits Min.	Limits Max.	Limits Units	Conditions
V_{DR}	V_{CC} for Data Retention		2.0		V	CE2 ⩽ 0.2V
I_{CCDR}	Data Retention Supply Current	S5101L-1, S5101L		10	μA	V_{CC}=V_{DR} T_R=T_F=20 ns
		S5101L-3		140	μA	
T_{CDR}	Chip Deselect to Data Retention Time		0		ns	
T_R	Operation Recovery Time		T_{RC}[2]		ns	

Notes:
[1] For guaranteed low V_{CC} Data Retention @ 2.0V, order must specify S5101L, S5101L-1 or S5101l-3.
[2] T_{RC} = Read Cycle Time.

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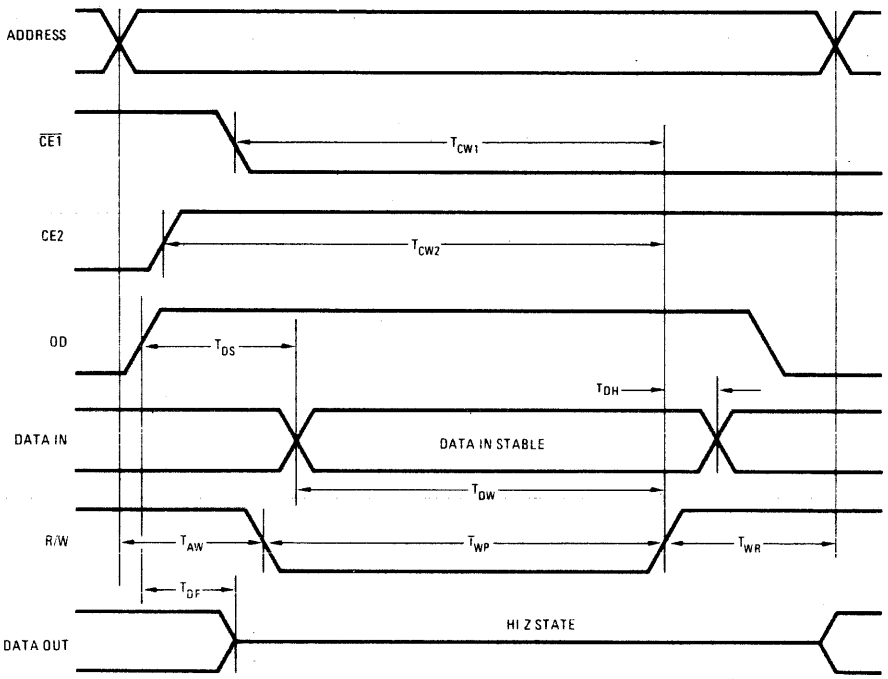
Read Cycle



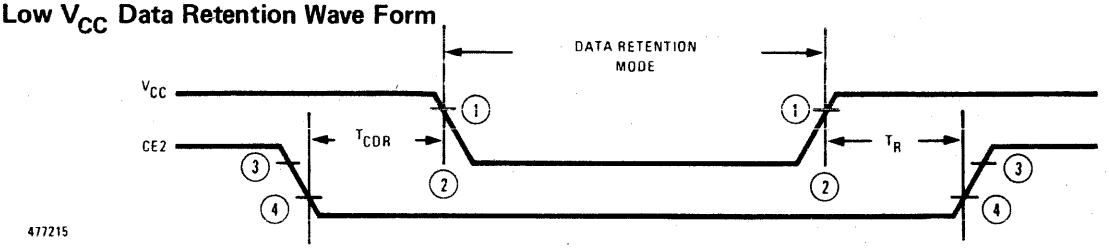
Note:

1. OD may be tied low for separate I/O information.
2. The output will go into a high impedance state if either CE1 is high, CE2 is low, OD is high or R/W is low.

Write Cycle — For Separate or Common Data I/O



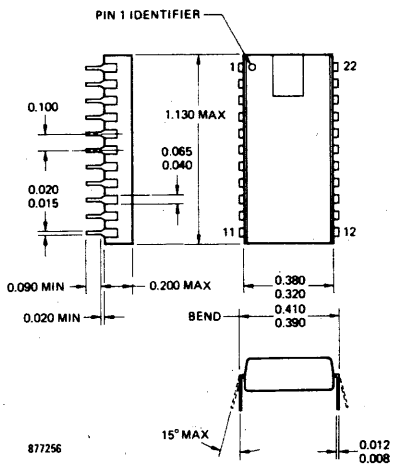
Low V_{CC} Data Retention Wave Form



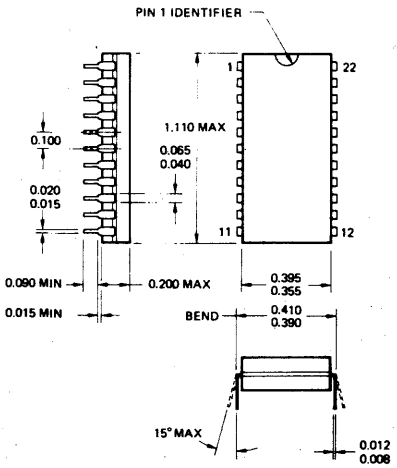
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Physical Dimensions

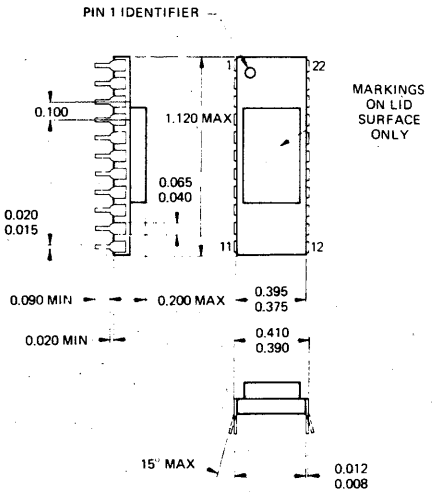
22-Pin Plastic



22-Pin Cer-DIP



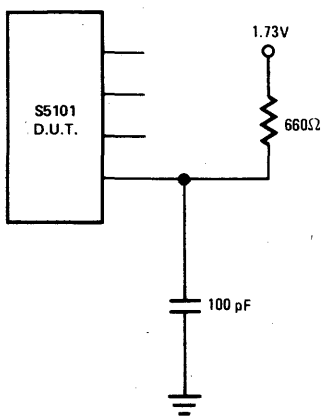
22-Pin Ceramic



Ordering Information

Device	Access Time (ns)	Standby Current (μA)	Data Retention at 2V	Order Number		
				Plastic	Cer-DIP	Ceramic
S5101	650	10	No	S5101P	S5101E	S5101C
S5101-1	450	10	No	S51011P	S51011E	S51011C
S5101-3	650	140	No	S51013P	S51013E	S51013C
S5101-8	800	500	No	S51018P	S51018E	S51018C
S5101L	650	10	Yes	S5101LP	S5101LE	S5101LC
S5101L-1	450	10	Yes	S5101L1P	S5101L1E	S5101L1C
S5101L-3	650	140	Yes	S5101L3P	S5101L3E	S5101L3C

A.C. Test Load



A.C. Conditions of Test

Input Levels	0.65V to 2.2V
Input Rise and Fall Time	20ns
Timing Measurement Reference Level	1.5V

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1024 Bit (1024×1) Static CMOS RAM

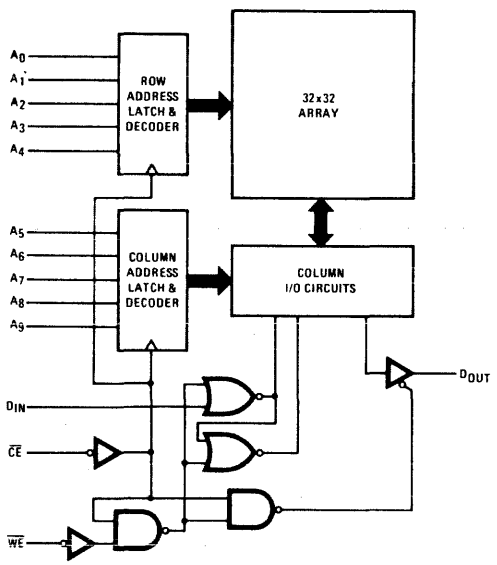
Features

- ☐ Ultra Low Standby Power
- ☐ S6508 Completely TTL Compatible
- ☐ S6508A Completely CMOS Compatible
- ☐ 4V to 11V Operation (S6508A)
- ☐ Data Retention at 2V
- ☐ Three-State Output
- ☐ Low Operating Power: 10mW @ 1MHz (5V)
- ☐ Fast Access Time: 115ns @ 10V

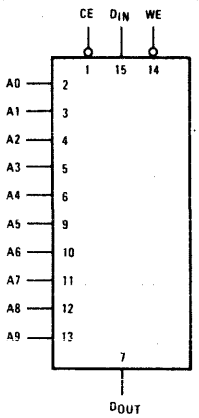
General Description

The AMI S6508 family of 1024x1 bit static CMOS RAMs offers ultra low power dissipation with a single power supply. The device is available in two versions. The basic part (S6508) operates on 5V and is directly TTL compatible on all inputs and the three-state output. The S6508 "A" operates from 4V to 11V and is fully CMOS compatible. The data is stored in ultra low power CMOS static RAM cells (six transistor). The stored data is read out nondestructively and is the same polarity as the original input data. The address is buffered by on-chip address registers. These internal registers are latched by the HIGH to LOW transition of chip enable ($\overline{CE}$). The write enable and chip enable functions are designed such that either separate or common data I/O operations can be easily implemented for maximum design flexibility.

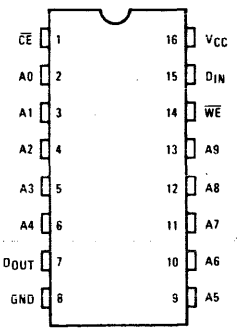
Block Diagram



Logic Symbol



Pin Configuration



Pin Names

A0-A9	Address Inputs	$\overline{CE}$	Chip Enable
D_{IN}	Data Input	$\overline{WE}$	Write Enable
D_{OUT}	Data Output	V_{CC}	Power Supply

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General Description (Continued)

The S6508 is fabricated using a silicon gate CMOS process suitable for high volume production of high performance, ultra low power memories. When deselected ($\overline{CE}$ = HIGH), the S6508-1 draws less than 10 microamps from the 5V supply. In addition, it offers guaranteed data retention with the power supply as low as 2 volts. This process makes the device an ideal choice where battery augmented nonvolatile RAM storage is mandatory.

CMOS to TTL – S6508/S6508-1

Absolute Maximum Ratings

Supply Voltage	8.0V
Input or Output Voltage Supplied	GND - 0.5V to V_{CC} + 0.5V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range, Commercial	0°C to 70°C

D.C. Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter		Min.	Max.	Units	Conditions
V_{IH}	Logical "1" Input Voltage		V_{CC} - 2.0		V	
V_{IL}	Logical "0" Input Voltage			0.8	V	
I_{IL}	Input Leakage		-1.0	1.0	μA	$0V < V_{IN} < V_{CC}$
V_{OH2}	Logical "1" Output Voltage		V_{CC} - 0.01		V	$I_{OUT} = 0$
V_{OH1}	Logical "1" Output Voltage		2.4		V	I_{OH} = -0.2mA
V_{OL2}	Logical "0" Output Voltage			GND+0.01	V	$I_{OUT} = 0$
V_{OL1}	Logical "0" Output Voltage			0.45	V	I_{OL} = 2.0mA
I_O	Output Leakage		-1.0	1.0	μA	$0V < V_O < V_{CC}$, $\overline{CE} = V_{IH}$
I_{CCL}	Standby Supply Current	S6508		100	μA	$V_{IN} = V_{CC}$, $\overline{CE} = V_{IH}$
		S6508-1		10	μA	
I_{CC}	Supply Current S6508/S6508-1			2.0	mA	f = 1MHz
C_{IN}	Input Capacitance			7.0	pF	
C_O	Output Capacitance			10.0	pF	

A.C. Characteristics (V_{CC} = 5.0V ±10%, C_L = 50pF (One TTL Load), T_A = 0°C to 70°C)

Symbol	Parameter	S6508-1		S6508		Units	Conditions
		Min.	Max.	Min.	Max.		
t_{ACC}	Access Time from $\overline{CE}$		300		460	ns	See A.C. conditions of test and A.C. test load.
t_{EN}	Output Enable Time		180		285	ns	
t_{DIS}	Output Disable Time		180		285	ns	
t_{CEH}	$\overline{CE}$ HIGH	200		300		ns	
t_{CEL}	$\overline{CE}$ LOW	300		460		ns	
t_{WP}	Write Pulse Width (LOW)	200		300		ns	
t_{AS}	Address Setup Time	7		15		ns	
t_{AH}	Address Hold Time	90		130		ns	
t_{DS}	Data Setup Time	200		300		ns	
t_{DH}	Data Hold Time	0		0		ns	
t_{MOD}	Data Modify Time	0		0		ns	

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CMOS to CMOS – S6508A/S6508A-1

Absolute Maximum Ratings

Supply Voltage 12.0V
Input or Output Voltage Applied ..... -0.5V to V_{CC} + 0.5V
Storage Temperature Range ..... -65°C to 150°C
Operating Temperature Range, Commercial ..... 0°C to 70°C

D.C. Characteristics (V_{CC} = 4V to 11V, T_A = 0°C to 70°C)

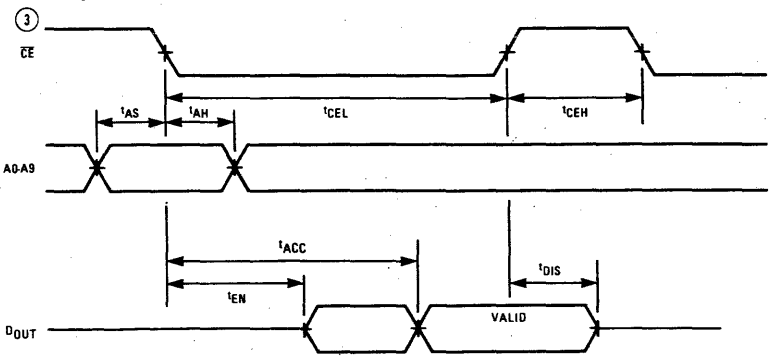
Symbol	Parameter		Min.	Max.	Units	Conditions
V_{IH}	Logical "1" Input Voltage		70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
I_{IL}	Input Leakage		-1.0	1.0	μA	$0V < V_{IN} < V_{CC}$
V_{OH}	Logical "1" Output Voltage		V_{CC} - 0.01		V	$I_{OUT} = 0$
V_{OL}	Logical "0" Output Voltage			GND+0.01	V	$I_{OUT} = 0$
I_O	Output Leakage		-1.0	1.0	μA	$0V < V_O < V_{CC}$, $\overline{CE} = V_{IH}$
I_{CCL}	Standby Supply Current	S6508A		500	μA	$V_{IN} = V_{CC}$, $\overline{CE} = V_{IH}$
		S6508A-1		100	μA	
I_{CC}	Supply Current (S6508A/S6508A-1)	V_{CC} = 5V		2.0	mA	f = 1MHz
		V_{CC} = 10V		4.3	mA	
C_{IN}	Input Capacitance			7.0	pF	
C_O	Output Capacitance			10.0	pF	

A.C. Characteristics (V_{CC} = V_{CC} ± 10%, T_A = 0°C to 70°C)

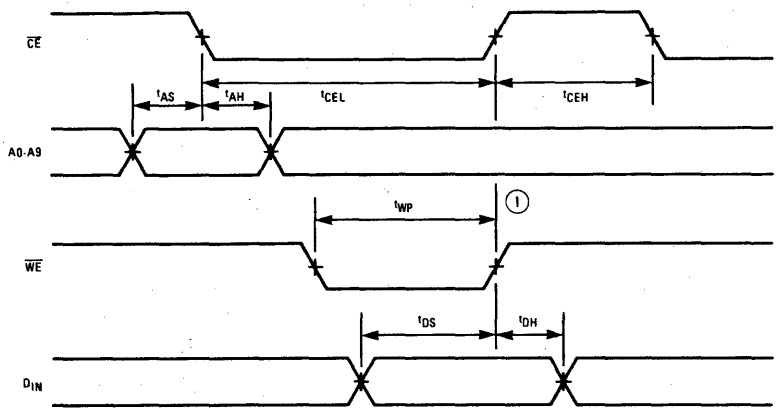
Symbol	Parameter	V_{CC}	S6508A-1		S6508A		Units	Conditions
			Min.	Max.	Min.	Max.		
t_{ACC}	Access Time from $\overline{CE}$	5V		275		460	ns	See A.C. conditions of test and A.C. test load.
		10V		115		185	ns	
t_{EN}	Output Enable Time	5V		165		285	ns	
		10V		75		120	ns	
t_{DIS}	Output Disable Time	5V		165		285	ns	
		10V		75		120	ns	
t_{CEH}	$\overline{CE}$ HIGH	5V	175		300		ns	
		10V	80		125		ns	
t_{CEL}	$\overline{CE}$ LOW	5V	275		460		ns	
		10V	115		185		ns	
t_{WP}	Write Pulse Width (LOW)	5V	175		300		ns	
		10V	80		125		ns	
t_{AS}	Address Setup Time	5V	7		15		ns	
		10V	7		15		ns	
t_{AH}	Address Hold Time	5V	80		130		ns	
		10V	40		60		ns	
t_{DS}	Data Setup Time	5V	175		300		ns	
		10V	80		125		ns	
t_{DH}	Data Hold Time	5V	0		0		ns	
		10V	0		0		ns	
t_{MOD}	Data Modify Time	5V	0		0		ns	
		10V	0		0		ns	

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Read Cycle



Write Cycle



A.C. Test Conditions

Input Levels .... V_{IL} to V_{IH}

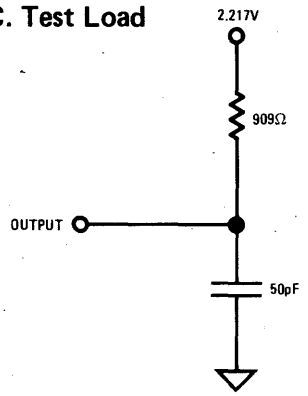
Input Rise & Fall..... 20ns

Timing Measurement Reference Level

S6508/S6508-1 ..... 1.5V

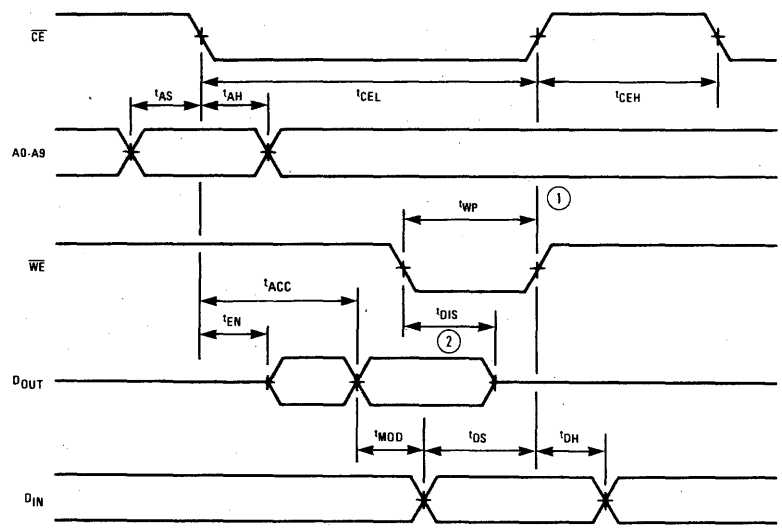
S6508A/S6508-1.... 50% V_{CC}

A.C. Test Load



877244

Read Modify Write Cycle



NOTES:

1. The write operation is terminated on any positive edge of Chip Enable ($\overline{CE}$) or Write Enable ($\overline{WE}$).
2. The data output will be in the high impedance state whenever $\overline{WE}$ is LOW.
3. $\overline{WE}$ is HIGH during a read operation.

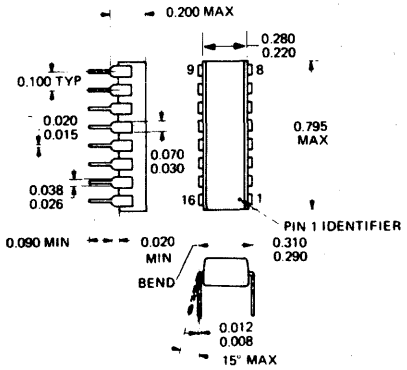
©IC MASTER 1978

Low V_{CC} Data Retention Characteristics (T_A = 0°C to 70°C)

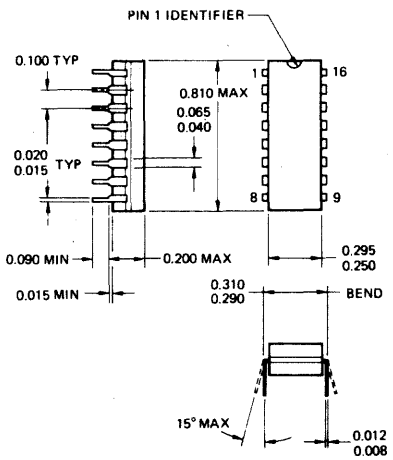
Symbol	Parameter		Min.	Max.	Units	Conditions
V_{DR}	V_{CC} for Data Retention		2.0		V	$\overline{CE}$ = 2.0V
I_{CCDR}	Data Retention Supply Current	S6508, S6508A		10	μA	$V_{CC} = V_{DR}$ Min. $t_R = t_F$ = 20ns
		S6508-1, S6508A-1		1.0	μA	
t_{CDR}	Deselect Setup Time		t_{CEH}		ns	
t_R	Recovery Time		t_{CEH}		ns	

Package Outlines

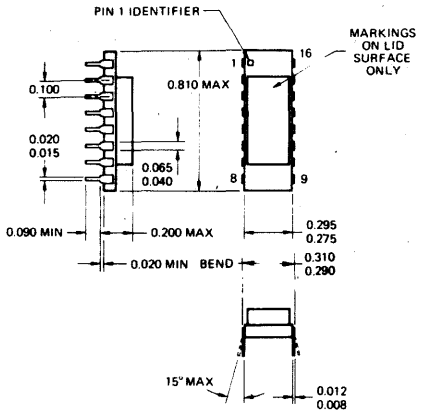
16-Pin Plastic



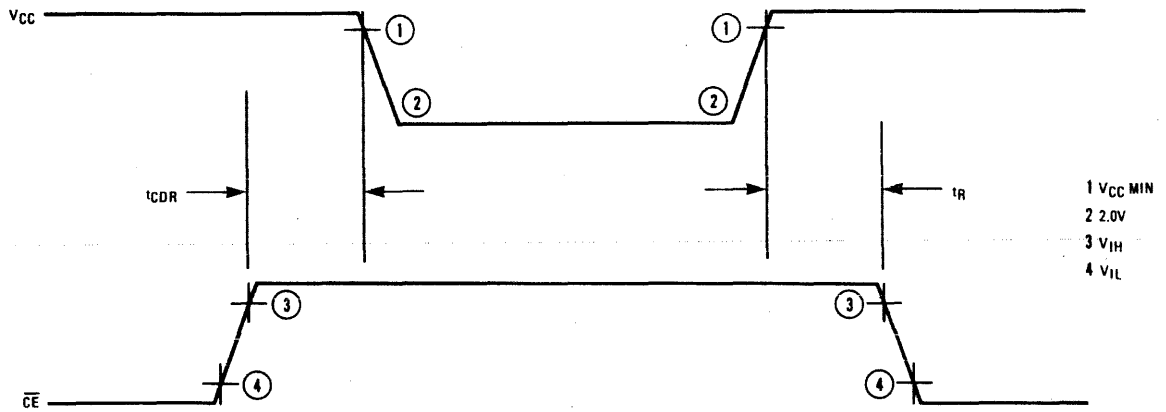
16-Pin Cer-DIP



16-Pin Ceramic



Low V_{CC} Data Retention Waveform



Ordering Information

Device	Access Time	Interface	Order Number Plastic	Cer-Dip	Ceramic
S6508	460ns	TTL	S6508P	S6508E	S6508C
S6508-1	300ns	TTL	S65081P	S65081E	S65081C
S6508A	185ns (10V)	CMOS	S6508AP	S6508AE	S6508AC
S6508A-1	115ns (10V)	CMOS	S6508A1P	S6508A1E	S6508A1C

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16,384 Bit (2048×8) Static VMOS ROM

Features

- ☐ Fast Access Times: 250 ns Maximum
- ☐ Fully Static Operation
- ☐ Single +5V ±10% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Three Programmable Chip Selects
- ☐ EPROM Pin Compatible
- ☐ Fan-out of 5 TTL — I_{OL} = 8mA @ 0.4V

Absolute Maximum Ratings*

Ambient Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to 150°C
Output or Supply Voltages	-0.5V to 7V
Input Voltages	-0.5V to 5.5V
Power Dissipation	1W

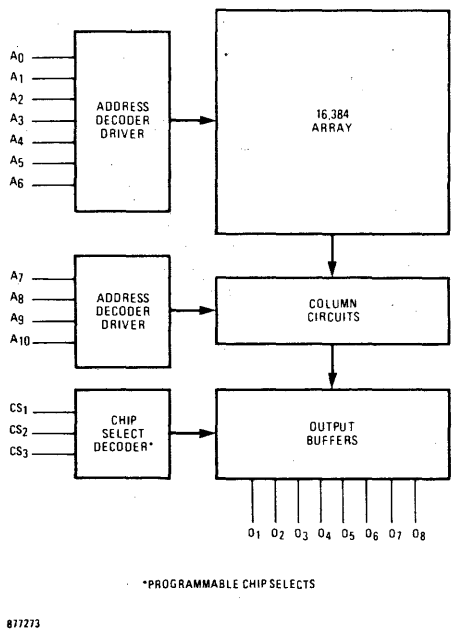
General Description

The AMI S4216B is a 16,384 bit static mask programmable VMOS ROM organized as 2048 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three-state outputs facilitate memory expansion by allowing the outputs to be or-tied to other devices.

The S4216B is fully compatible with 16K UV EPROMs (+5V version) making system development much easier and more cost effective. It is fully static, requiring no clocks for operation. The three chip selects are mask programmable, the active level for each being specified by the user.

The S4216B is fabricated using AMI's proprietary n-channel VMOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

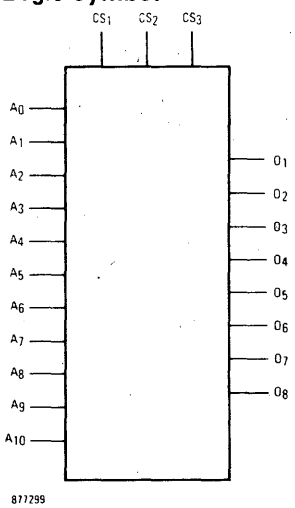
Block Diagram



*PROGRAMMABLE CHIP SELECTS

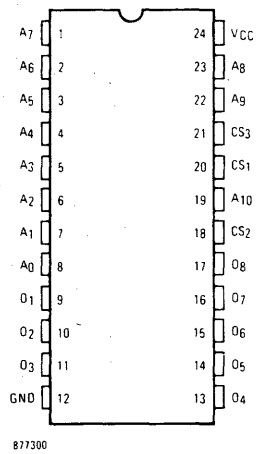
877273

Logic Symbol



877299

Pin Configuration



877300

Pin Names

A_0 - A_{10}	Address Inputs
O_1 - O_8	Data Outputs
CS_1 - CS_3	Chip Select Inputs
V_{CC}	+5V Power Supply

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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D.C. Characteristics: $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 8$ mA
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -1$ mA
V_{IL}	Input LOW Voltage			0.8	V	
V_{IH}	Input HIGH Voltage	2.0			V	
I_{LI}	Input Leakage Current			10	μA	$V_{IN} = 0$ to 5.5V
I_{LO}	Output Leakage Current			10	μA	$V_O = 0.4$ to 5.5V, Chip Deselected
I_{CC}	Power Supply Current			80	mA	V_{CC} = Max., $T_A = 0°C$

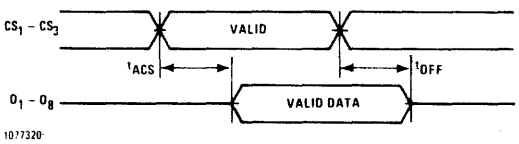
Capacitance: $T_A = 25°C$, f = 1Mhz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			8	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance			10	pF	$V_{OUT} = 0V$

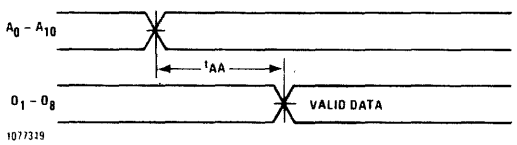
A.C. Characteristics: $T_A = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time			250	ns	See A.C. Test
t_{ACS}	Chip Select Access Time			100	ns	Conditions
t_{OFF}	Chip Select Turn-off Time			100	ns	& Waveforms

Waveforms



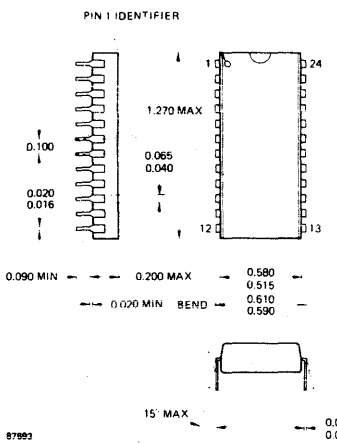
Propagation From Chip Select



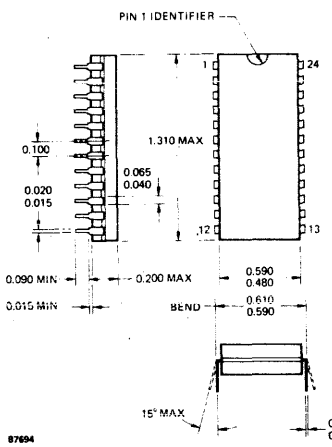
Propagation From Address

Package Outlines

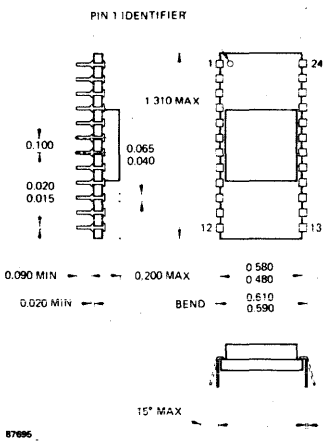
24-Pin Plastic



24-Pin Cer-DIP



24-Pin Ceramic

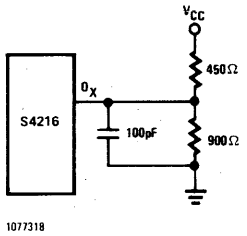


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A.C. Test Conditions

Input Pulse Levels	0.8V to 2.0V
Input Rise and Fall Times	10ns
Input/Output Timing Levels	1.5V

A.C. Test Load



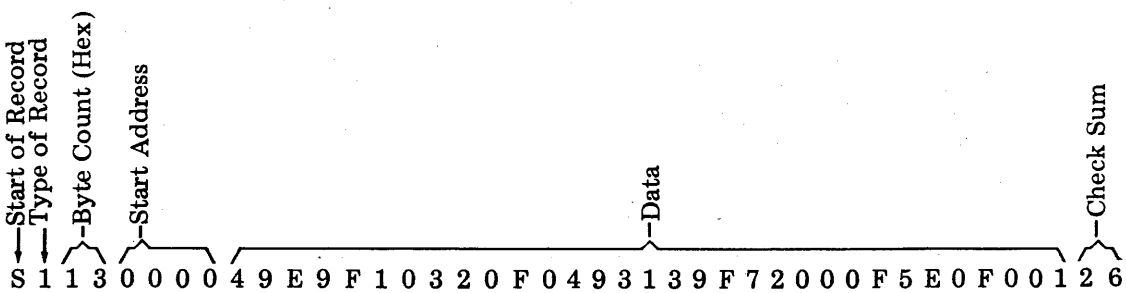
Custom Programming

The preferred method of pattern submission is the AMI Hex format as described below, with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler. The format is as follows and may be on paper tape, punched cards or other media readable by AMI.

Position	Description
1	**Start of record (Letter S)**
2	**Type of record** 0 — Header record (comments) 1 — Data record 9 — End of file record
3 — 4	**Byte Count** Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5, 6, 7, 8	**Address Value** The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9, . . ., N	**Data** Each data byte is represented by two hex characters. Most significant character first.
N+1, N+2	**Checksum** The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example:

```
S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6
S 9 0 3 0 0 0 0 F C
```



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65,536 Bit (8192×8) Static VMOS ROM

Features

- ☐ Single +5V ± 10% Power Supply
- ☐ High Performance: Maximum Access Time: 350ns
- ☐ EPROM Compatible for Cost Effective System Development
- ☐ Completely Static Operation
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs

Absolute Maximum Ratings*

Ambient Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to 150°C
Output or Supply Voltages	-0.5V to 7V
Input Voltages	-0.5V to 5.5V
Power Dissipation	1W

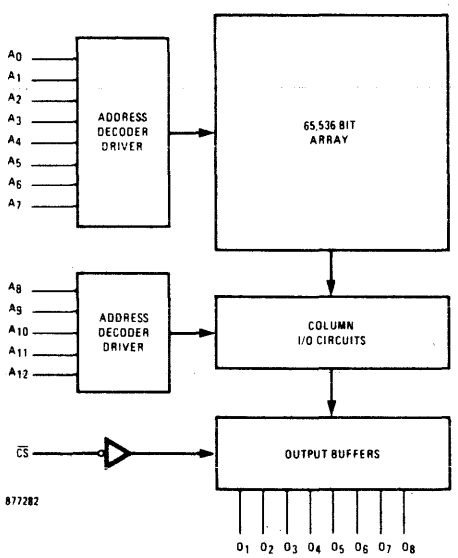
General Description

The AMI S4264 is a 65,536 bit fully static VMOS mask programmable ROM organized as 8192 words by 8 bits. The device if fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three-state outputs facilitate memory expansion by allowing the outputs to be or-tied to other devices.

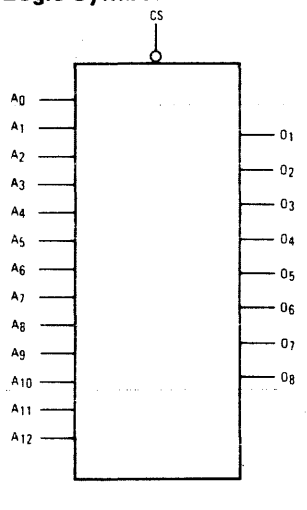
The S4264 is fully static requiring no clocks for operation. The chip select ($\overline{CS}$) function is used to select the device providing for memory system expansion. The byte organization of the S4264 makes it ideal for microprocessor applications.

The S4264 is fabricated using AMI's proprietary VMOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

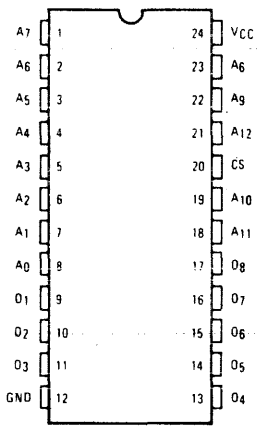
Block Diagram



Logic Symbol



Pin Configuration



Pin Names

A_0-A_{12}	Address Inputs	$\overline{CS}$	Chip Select
O_1-O_8	Data Outputs	V_{CC}	+5V Power

Truth Table

Input	Outputs	Mode
$\overline{CS}$	O_1-O_8	
L	D_{OUT}	Read
H	H-Z	Deselected

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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D.C. Characteristics: $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 10\%$.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 8$ mA
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -400\mu A$
V_{IL}	Input LOW Voltage	-0.3		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	$V_{IN} = 0$ to 5.5V
I_{LO}	Output Leakage Current			50	μA	$\overline{CS} \geq 2.4V$, $V_O = 0.4V$ to 5.5V
I_{CC}	Power Supply Current			145	mA	

Capacitance: $T_A = 25°C$, f = 1 MHz.

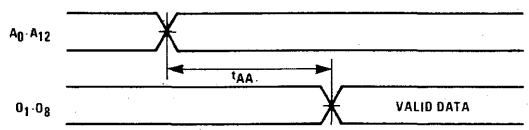
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			8	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance			10	pF	$V_{OUT} = 0V$

A.C. Characteristics: $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 10\%$.

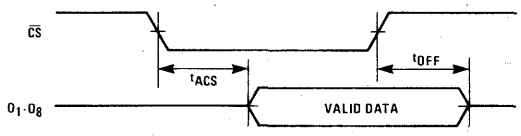
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time			400	ns	See Test Circuit
t_{ACS}	Chip Select Access Time			150	ns	&
t_{OFF}	Chip Deselect Time	0		150	ns	Waveforms

WAVE FORMS

PROPOGATION DELAY FROM ADDRESS

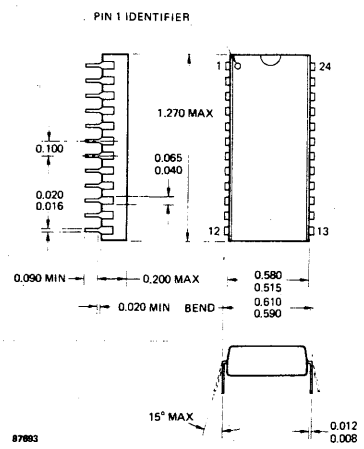


PROPAGATION DELAY FROM CHIP SELECT

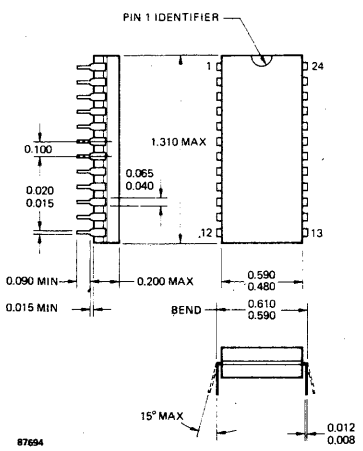


PACKAGE OUTLINES

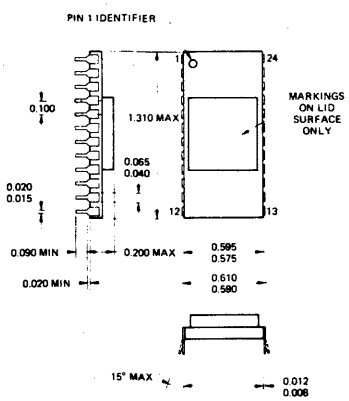
24-PIN PLASTIC



24-PIN Cer-DIP



24-PIN CERAMIC

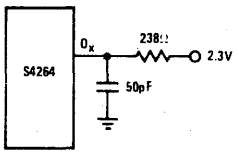


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A.C. Test Conditions

Input Pulse Levels	0.8V to 2.0V
Input Rise and Fall Times	10ns
Input/Output Timing Levels	1.5V

A.C. Test Load



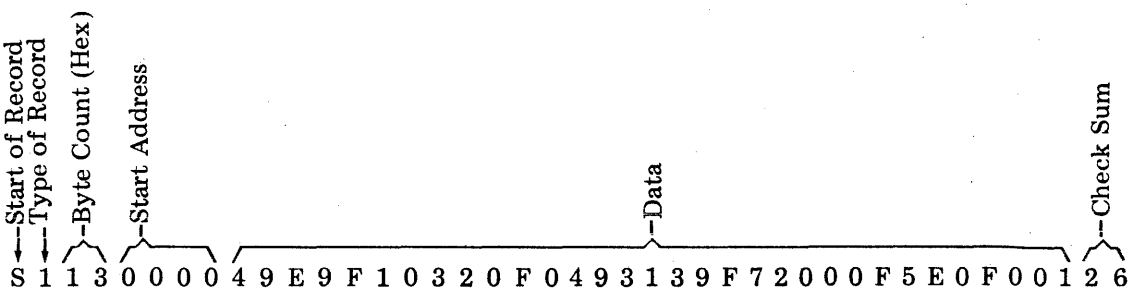
Custom Programming

The preferred method of pattern submission is the AMI Hex format as described below, with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler. The format is as follows and may be on paper tape, punched cards or other media readable by AMI.

Position	Description
1	**Start of record (Letter S)**
2	**Type of record** 0 — Header record (comments) 1 — Data record 9 — End of file record
3 — 4	**Byte Count** Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5, 6, 7, 8	**Address Value** The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9, . . ., N	**Data** Each data byte is represented by two hex characters. Most significant character first.
N+1, N+2	**Checksum** The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example:

```
S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6
S 9 0 3 0 0 0 0 F C
```



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4096 Bit (512×8) Erasable and Electrically Reprogrammable ROM

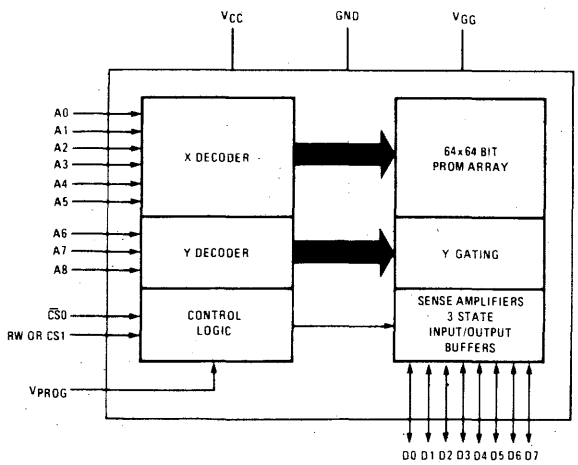
Features

- ☐ On-Board Programmability
- ☐ Fast Access Time — 750ns Max.
- ☐ High Speed Programming — Less than 1 Minute for all 4096 Bits
- ☐ Programmed with R/W, CS and V_{PROG} Pins
- ☐ Completely TTL Compatible — Excluding the V_{PROG} Pin during Read or Write
- ☐ Ultraviolet Light Erasable — Less than 10 Minutes
- ☐ Static Operation — No Clocks Required
- ☐ Three-State Data I/O
- ☐ Standard Power Supplies — +5V and -12V
- ☐ Mature P-Channel Process

General Description

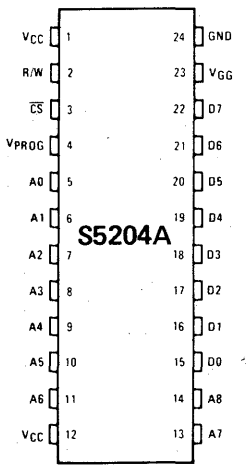
The S5204A is a high speed, static, 512x8 bit, erasable and electrically programmable read only memory designed for use in bus-organized systems. Both input and output are TTL compatible during both read and write modes. Packaged in a 24-pin hermetically sealed dual in-line package, the bit pattern can be erased by exposing the chip to an ultraviolet light source through the transparent lid, after which a new pattern can be written.

Block Diagram



77675

Pin Configuration



877254

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} except the V_{PROG} pin	+0.3V to -20V
Voltage on the V_{PROG} pin relative to V_{SS}	+0.3V to -60V
Operating Temperature	0°C to +70°C
Storage Temperature (programmed)	-55°C to +85°C
Storage Temperature (unprogrammed)	-55°C to +150°C

Typical Applications

- ☐ ROM Program Debugging
- ☐ Code Translation
- ☐ Microprogramming
- ☐ Look-up Tables
- ☐ Random Logic Replacement
- ☐ Programmable Waveforms
- ☐ Character Generation
- ☐ Electronic Keyboards

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

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DC (STATIC) CHARACTERISTICS (V_{CC} = +5.0V ± 5%, V_{GG} = −12.0V ± 5% T_A = 0 − 70°C unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
V_{IL}	INPUT VOLTAGE LOW		0.8	V
V_{IH}	INPUT VOLTAGE HIGH	V_{CC} −2.25	V_{CC} +.3	V
V_{OL}	OUTPUT VOLTAGE LOW I_{OL} = 1.6 ma		0.4	V
V_{OH}	OUTPUT VOLTAGE HIGH I_{OH} = 200 μA	2.4		V
I_{LI}	INPUT LEAKAGE CURRENT		10	μa
I_{LO}	OUTPUT LEAKAGE CURRENT CS = 5V		20	μa
I_{GG}	V_{GG} SUPPLY CURRENT		45	ma
I_{CC}	V_{CC} SUPPLY CURRENT		50	ma
P_D	POWER DISSIPATION		750	mw

NOTE: Program input V_{PROG} may be tied to V_{CC} during the Read.

AC (DYNAMIC) CHARACTERISTICS (Loading is as shown in Figure 1 unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
T_{ACC}	ACCESS TIME		750	ns
T_{CO}	CHIP SELECT TO OUTPUT DELAY		400	ns
T_{DD}	CHIP DESELECT TO OUTPUT DELAY			ns

PROGRAM CHARACTERISTICS (R/W G_{nd}, Program pulse rise and fall time (10% to 90%) are both at 1μs max).

SYMBOL	CHARACTERISTICS	MIN	MAX	UNIT
T_{AS}	ADDRESS SET UP TIME	10		μs
T_{CSS}	CHIP SELECT SET UP TIME	10		μs
T_{DS}	DATA SET UP TIME	10		μs
T_{AH}	ADDRESS HOLD TIME	10		μs
T_{CSH}	CHIP SELECT HOLD TIME	10		μs
T_{DH}	DATA HOLD TIME	10		μs
T_{PWL}	PROGRAM PULSE WIDTH LOW	3	5	ms
T_{PWH}	PROGRAM PULSE WIDTH HIGH	500		μs
V_{PROG}*	PROGRAM AMPLITUDE	−55	−50	V
I_{PROG}	PROGRAM CURRENT		35	ma
T_{WS}	WRITE SET UP TIME	10		μs
T_{WH}	WRITE HOLD TIME	5		μs
T_{RS}	READ SET UP TIME	10		μs

*Note that in the WRITE mode the MIN value of V_{PROG} should not be exceeded and that chip select, address, and data lines may remain at TTL level, as in the READ mode

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INTERFACE DESCRIPTION

Pin	Label	Function
(15)	D0	**Data Lines** – with the R/W line selected for Read (V_{IH}), the Data Line (D0 through D7) are set to reflect the contents of the selected memory location. When the R/W line is set for Write (V_{IL}), the Data Lines are stored at the addressed location of the 5204A when V_{PROG} is present. The Data Bus output drivers are three-state devices that remain in the high impedance (off) state whenever CS is in the V_{IH} state or when R/W is in the V_{IL} state.
(16)	D1	
(17)	D2	
(18)	D3	
(19)	D4	
(20)	D5	
(21)	D6	
(22)	D7	
(2)	R/W	**Read/Write** – When this input line is set to V_{IH}, the device is in the Write mode, a low (V_{IL}) signal puts it into the Read mode.
(3)	CS	**Chip Select** – This input line must be set to V_{IL} for a Read or Write operation to be performed. When it is High (V_{IH}) the output data bus is set to a high-impedance three-state condition.
(4)	V_{PROG}	**Program** – In the Write mode, a 50Volt programming pulse at this input causes the data at the Data Lines to be stored in the selected address location. This pin should be tied to V_{CC} for normal Read operations.
(5)	A0	**Address Lines** – These lines select the 8 bit word in memory for Read or Write operation.
(6)	A1	
(7)	A2	
(8)	A3	
(9)	A4	
(10)	A5	
(11)	A6	
(13)	A7	
(14)	A8	

CONTROL FUNCTION TRUTH TABLE

CS	R/W	V_{PROG}	MODE	OUTPUTS
0	1	V_{PROG}	Write	Active Data Inputs
0	0	V_{CC}	Read	Active
1	X	X	Standby	Floating

OPERATION

Initially, and after each erasure, all bits of the 5204A are in the LOW state (output 0 volts). Data is stored by selectively programming a HIGH into the desired bit locations. The R/W input (pin 2) is used to select the desired mode of operation. When the R/W input is HIGH the chip is in the write enable mode of operation. The outputs (D_0 – D_7) are disabled (floating) with the corresponding pins becoming the data inputs. The word address is selected in the same manner as in the Read mode. Data to be programmed is presented 8 bits in parallel and after the address and data are set up a programming pulse (V_P = - 50 volts) is applied. V_{PROG} electrically writes the data into the memory array. Writing may be inhibited by deselecting the chip with the CS input at a HIGH during the write cycle. This feature allows true "on board" programming in bus organized systems where the R/W and V_{PROG} inputs are common and the device to be programmed is selected by means of the chip select input as during read operations.

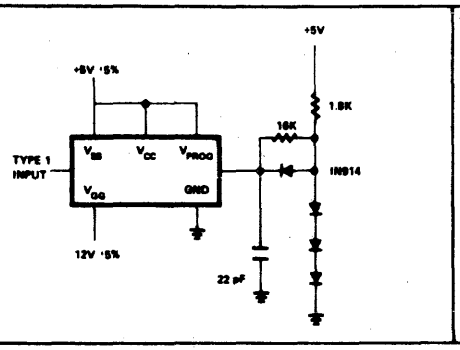
The amount of program energy required to insure memory retention may be defined as a function of the number of program pulses (N) times the program pulse width (t_{pw}) ($N \times t_{pw} \geq 60$ msec). This means if a 3 ms pulse is used, 20 program pulses are required, and if a 5 ms pulse is used 12 program pulses are required.

The read operation is accomplished by a LOW at the R/W input with the program input connected to V_{SS} potential. True data (data out = date in) is valid after the address is stable. The CS input will disable (float) the outputs when HIGH to allow capability with bus organized systems.

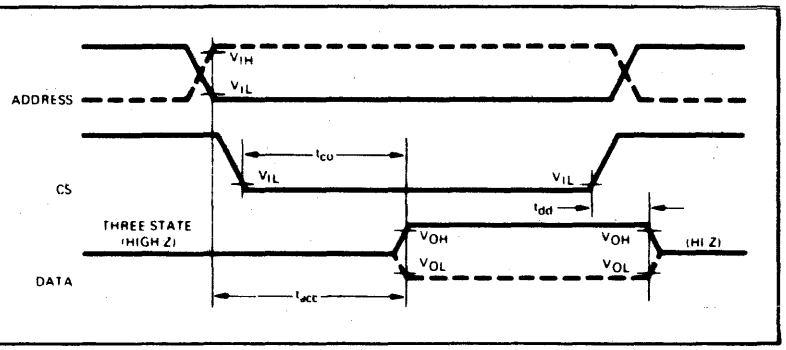
Erasure is accomplished by exposing the array to a 2537Å ultra-violet light source (such as Ultra-Violet Products, Inc. Lamp Model S52 or UVS-54, Turner Designs PROM Eraser, Model 30 or equivalent) for a period of 7 to 10 minutes. The clear optical lid should be approximately one inch away from the lamp tubes.

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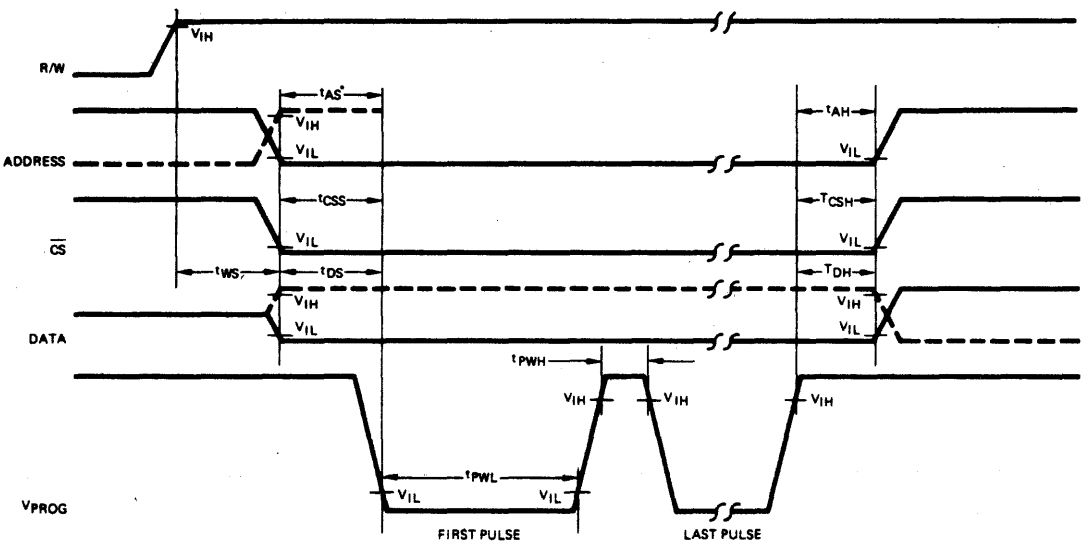
TEST CONDITIONS



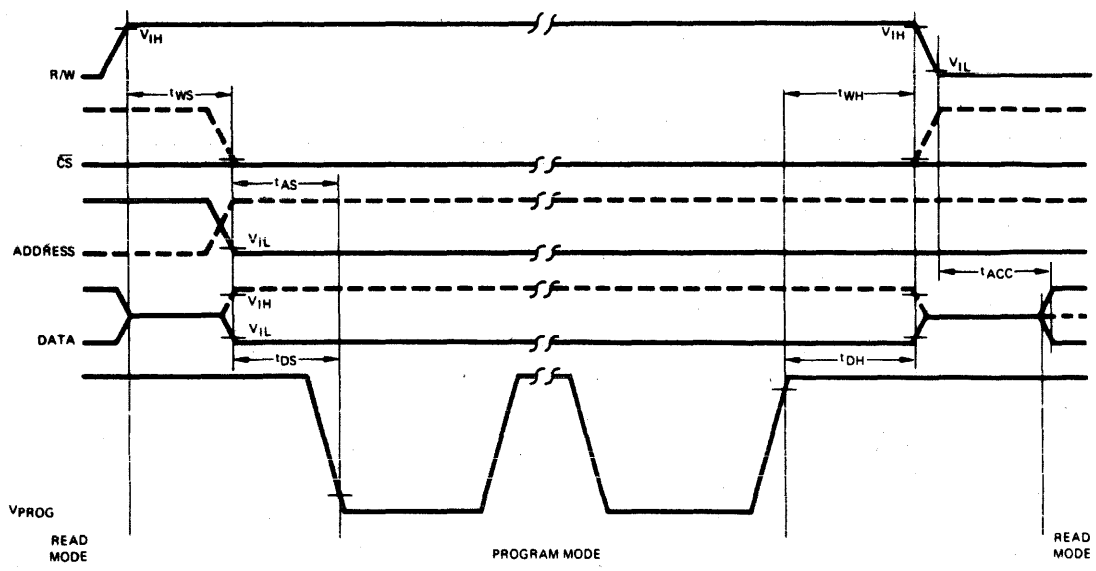
READ CYCLE TIMING WAVEFORMS



PROGRAMMING CYCLE TIMING WAVEFORMS



READ/PROGRAM/READ CYCLE TIMING WAVEFORM



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1024 Bit (128×8) Static Read/Write Memory

Features

- ☐ Organized as 128 Bytes of 8 Bits
- ☐ Static Operation
- ☐ Bidirectional Three-State Data Input/Output
- ☐ Six Chip Enable Inputs (Four Active Low, Two Active High)
- ☐ Single 5 Volt Power Supply
- ☐ TTL Compatible
- ☐ Maximum Access Time:
  —360ns for S68A10
  —250ns for S68B10

General Description

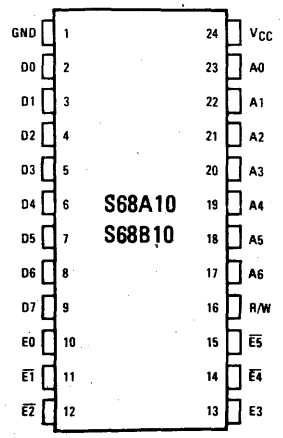
The S68A10 and S68B10 are static 128x8 Read/Write Memories designed and organized to be compatible with the S68A00 and S68B00 Microprocessors. Interfacing to the S68A10 and S68B10 consists of an 8-bit bidirectional data bus, seven address lines, a single Read/Write control line, and six chip enable lines, four negative and two positive.

For ease of use, the S68A10 and S68B10 are a totally static memory requiring no clocks or cell refresh. The S68A10 and S68B10 are fabricated with N-channel silicon gate depletion load technology to be fully DTL/TTL compatible with only a single +5 volt power supply required.

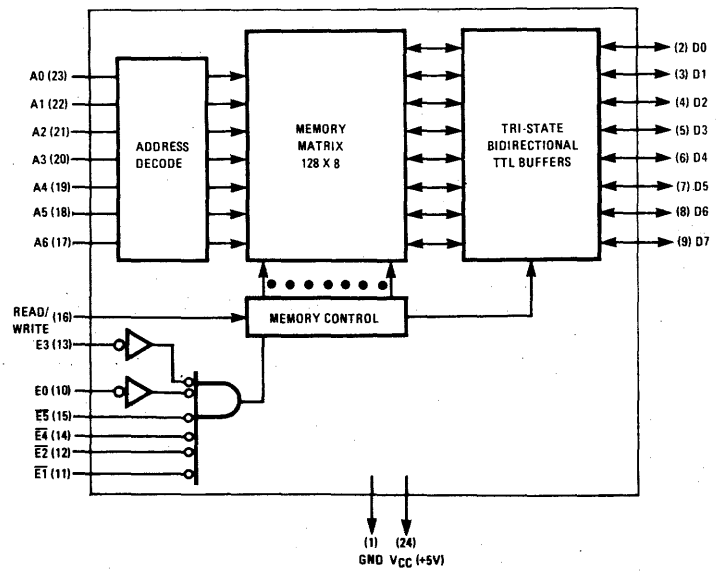
Absolute Maximum Ratings

Supply Voltage	-0.3V to +7.0V
Input Voltage	-0.3V to +7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C

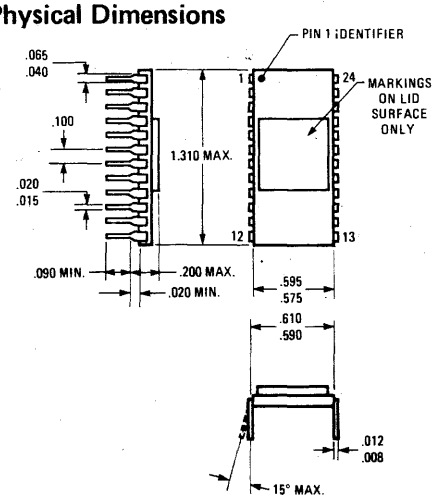
Pin Configuration



Block Diagram



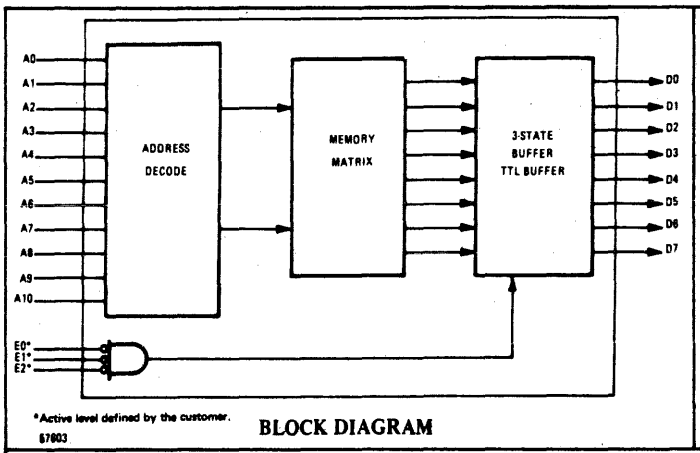
Physical Dimensions



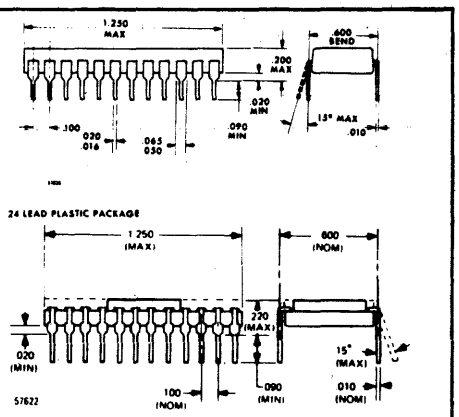
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16,384 Bit (2048×8) ROM

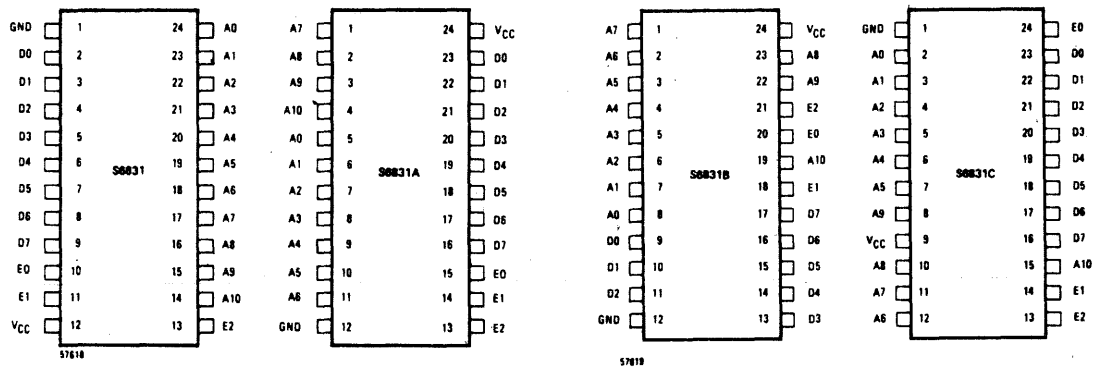
ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION



- Maximum Access Time = 450 ns @ C_L = 130 pF
- Low Power 150 mW avg.
- Organized as 2048-Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- 3 Chip Enable Inputs (Mask Programmable)
- The S6831 is pinout similar with the S6830
- The S6831A is pinout compatible with the 2316A, 8316A
- The S6831B is pinout compatible with the Intel 2316B, MC68317
- The S6831C is pinout compatible with the EA4600
- Single 5-Volt Power Supply
- TTL Compatible Input/Output

FUNCTIONAL DESCRIPTION

The S6831/A/B/C is a 16,384 bit Read Only Memory organized 2K words x 8 bits. This ROM has been designed to supply large bit storage, high performance memory for microprocessors and other demanding applications with simple interface requirements. The device will operate from a single +5V supply and is manufactured with a N-channel silicon gate depletion load technology. This device is available in all common high density ROM pinouts.

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Supply Voltage V_{CC}	- 0.5 to + 7.0V	Operating Temperature Range T_A	0 to + 70°C
Input Voltage V_{in}	- 0.5 to + 7.0V	Storage Temperature Range T_{stg}	- 55 to + 150°C

NOTE 1 Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

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DC (STATIC) CHARACTERISTICS (V_{CC} = + 5 Volt ± 5%; T_A = 0°C to + 70°C)

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage (Norm. Op. Levels)	2.0	–	5.25	Vdc	
V_{IL}	Input Low Voltage (Norm. Op. Levels)	- 0.5	–	0.8	Vdc	
I_I	Input Current (V_I = 0 to 5.25 V)	–	–	2.5	μAdc	
V_{OH}	Output High Voltage (I_{OH} =-100μA)	2.4	–	–	Vdc	
V_{OL}	Output Low Voltage (I_{OL} = 2.1 mA)	–	–	0.4	Vdc	
I_{LOH}	Output Leakage Current (V_O = 2.4, $\overline{E}$ = 0.4V, E = 2.4V)	–	–	10	μAdc	
I_{LOL}	Output Leakage Current (V_O = 0.4V, $\overline{E}$ = 0.4V, E = 2.4V)	–	–	10	μAdc	
I_{CC}	Supply Current (V_{CC} = 5.25V, T_A = 0°C)	–	30		mAdc	

CAPACITANCE

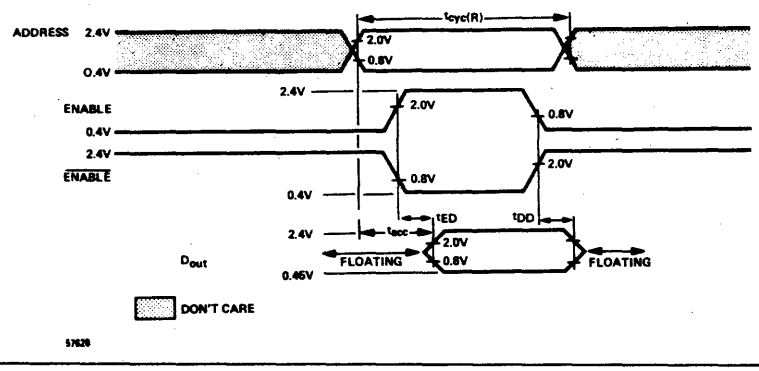
Symbol	Characteristic	Min.	Typ.	Max	Unit	Conditions
C_{in}	Input Capacitance	–	–	7.5	pF	f = 1.0 MHz
C_{out}	Output Capacitance	–	–	10	pF	T_A = 25°C

AC (DYNAMIC) CHARACTERISTICS V_{CC} = + 5 Volt ± 5%; T_A = 0°C to + 70°C

READ CYCLE (All timing with $t_r = t_f$ = 20 ns, Load of Figure 1)

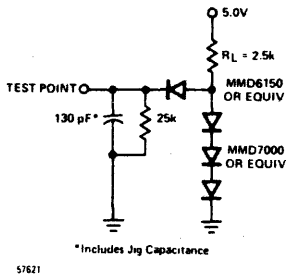
Symbol	Characteristic	Min.	Max.	Unit
t_{cyc} (R)	Read Cycle Time	450	–	ns
t_{ED}	Output Enable Delay Time	–	200	ns
t_{DD}	Output Disable Delay Time	10	150	ns
t_{ACC}	Read Access Time	–	450	ns

READ CYCLE TIMING



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FIGURE 1 – AC TEST LOAD



CUSTOM PROGRAMMING

The preferred method of pattern submission is the AMI Hex format as described below with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler/Loader. The format is as follows and may be on paper tape, punched card or other media readable by AMI.

ASCII Character	Description
1	**Start of record** (S)
2	**Type of record** 0 – Header record 1 – Data record 9 – End of file record
3 – 4	**Byte Count** Since each data byte is represented as two hex characters, the byte count must be multiplied by two fo get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length being defined in each record by the byte count.
5, 6, 7, 8	**Address Value** The memory location where this record is to be stored.
9, . . . , N	**Data** Each data byte is represented by two hex characters. Most significant character first.
N + 1, N + 2	**Checksum** The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

AMI will accept the input format used for the EA4600 or for the Intel 8316A or B in addition to the above format.

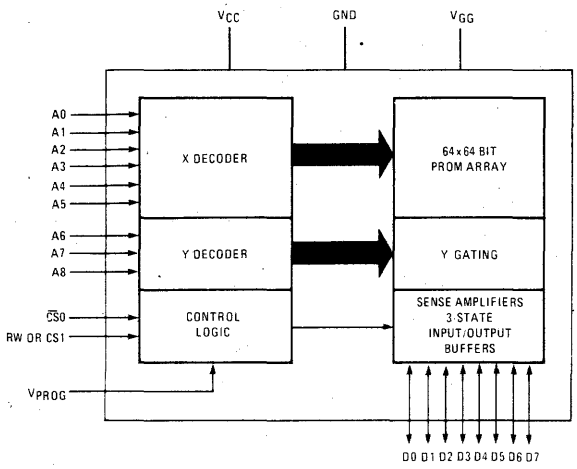
EXAMPLE:

```
S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 1 D
S 9 0 3 0 0 0 0 F C

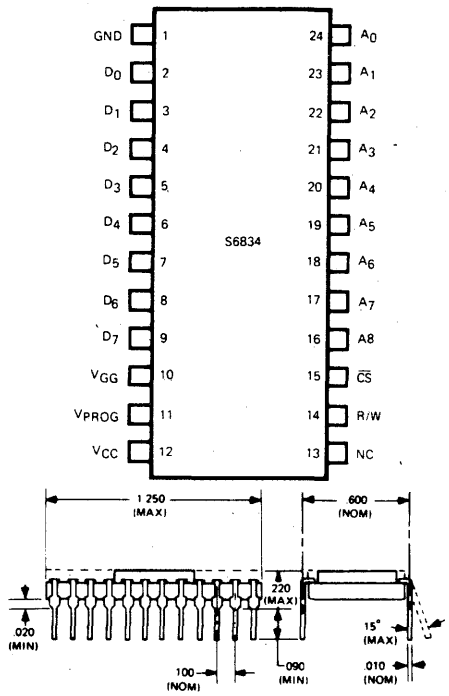
S — START OF RECORD
1 — TYPE OF RECORD
13 — BYTE COUNT (HEX)
0000 — START ADDRESS
49E9F10320F04931 39F72000F5E0F00 — DATA
1D — CHECK SUM
```


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4096 Bit (512×8) Erasable and Electrically Reprogrammable ROM



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- On-Board Programmability
- Fast Access Time – 500 ns Typ.
- Pin Configuration Similar to the S6830 1K x 8 Bit ROM
- High Speed Programming – Less than 1 Minute for all 4096 Bits
- Programmed with R/W, CS and V_{PROG} Pins
- Completely TTL Compatible – Excluding the V_{PROG} Pin during Read and Write
- Ultraviolet Light Erasable – Less than 10 Minutes
- Static Operation – No Clocks Required
- Three-State Data I/O
- Standard Power Supplies +5V and –12V
- Mature P-Chan Process

FUNCTIONAL DESCRIPTION

The S6834 is a high speed, static, 512 x 8 bit, eraseable and electrically programmable read only memory designed for use in bus-organized systems. Both input and output are TTL compatable during both read and write modes. Packaged in a 24 pin hermetically sealed dual in-line package the bit pattern can be erased by exposing the chip to an ultra-violet light source through the transparent lid, after which a new pattern can be written.

TYPICAL APPLICATIONS

- ROM Program Debugging
- Code Translation
- Microprogramming
- Look-up Tables
- Random Logic Replacement
- Programmable Waveforms
- Character Generation
- Electronic Keyboards

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ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} except the V_{PROG} pin	+0.3 to −20V
Voltage on the V_{PROG} pin relative to V_{SS}	+0.3 to −55V
Operating Temperature	0°C to +70°C
Storage Temperature (programmed)	−55°C to +85°C
Storage Temperature (unprogrammed)	−55°C to 150°C

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC (STATIC) CHARACTERISTICS (V_{CC} = +5.0V ± 5%, V_{GG} = −12.0V ± 5% T_A = 0 − 70°C unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
V_{IL}	INPUT VOLTAGE LOW		0.8	V
V_{IH}	INPUT VOLTAGE HIGH	V_{CC} −2.25	V_{CC} to .3	V
V_{OL}	OUTPUT VOLTAGE LOW I_{OL} = 1.6 ma		0.4	V
V_{OH}	OUTPUT VOLTAGE HIGH I_{OH} = 200μA	2.4		V
I_{LI}	INPUT LEAKAGE CURRENT		10	μa
I_{LO}	OUTPUT LEAKAGE CURRENT CS = 5V		20	μa
I_{GG}	V_{GG} SUPPLY CURRENT		45	ma
I_{CC}	V_{CC} SUPPLY CURRENT		50	ma
P_D	POWER DISSIPATION		750	mw

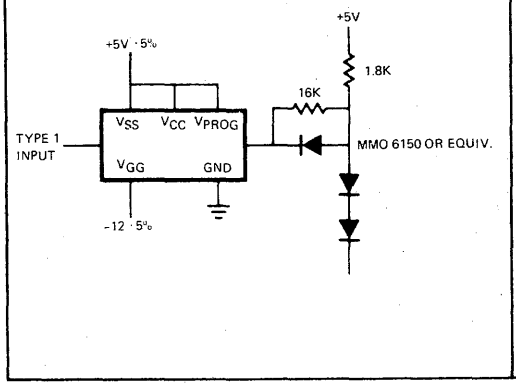
NOTE: Program input V_{PROG} may be tied to V_{CC} during the Read.

AC (DYNAMIC) CHARACTERISTICS (Loading is as shown in Figure 1 unless otherwise noted).

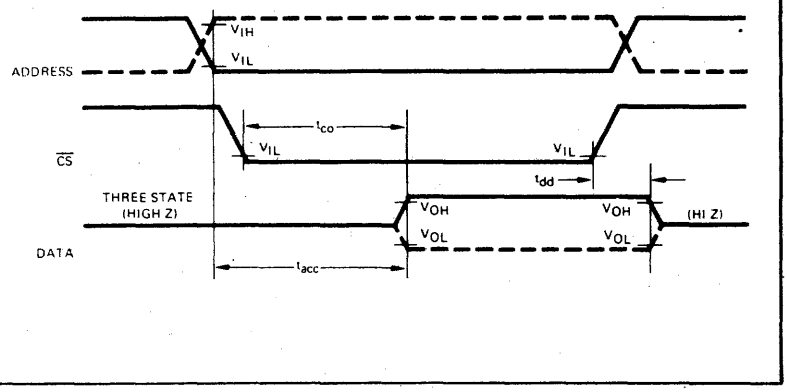
SYMBOL	CHARACTERISTIC	MIN	MAX (6834)	MAX (6834−1)	UNIT
T_{ACC}	ACCESS TIME		575	750	ns
T_{CO}	CHIP SELECT TO OUTPUT DELAY		300	400	ns
T_{DD}	CHIP DESELECT TO OUTPUT DELAY		250	325	ns

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TEST CONDITIONS



READ CYCLE TIMING WAVEFORMS



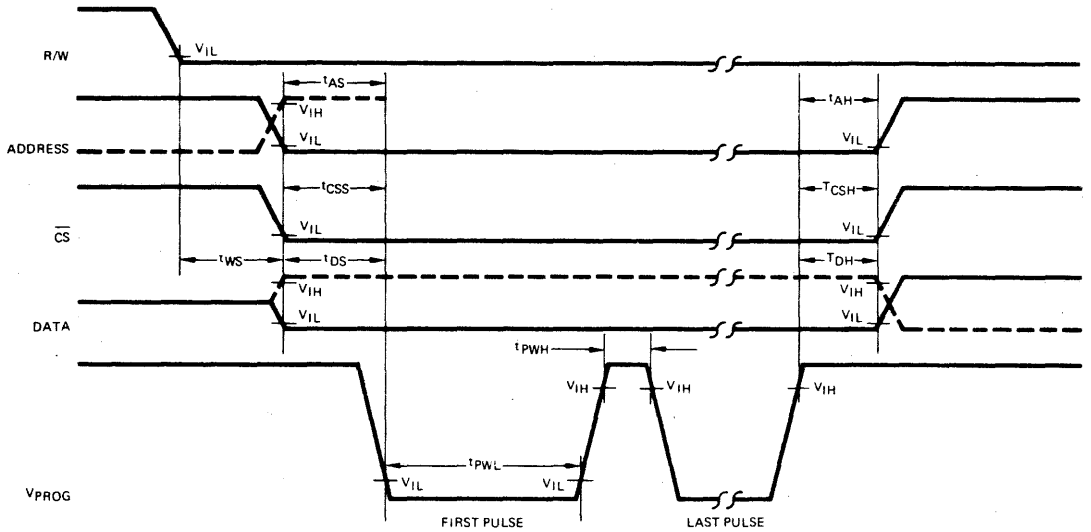
PROGRAM CHARACTERISTICS (R/W G_{nd}, Program pulse rise and fall time (10% to 90%) are both at 1μs max).

SYMBOL	CHARACTERISTICS	MIN	MAX	UNIT
T_{AS}	ADDRESS SET UP TIME	10		μs
T_{CSS}	CHIP SELECT SET UP TIME	10		μs
T_{DS}	DATA SET UP TIME	10		μs
T_{AH}	ADDRESS HOLD TIME	10		μs
T_{CSH}	CHIP SELECT HOLD TIME	10		μs
T_{DH}	DATA HOLD TIME	10		μs
T_{PWL}	PROGRAM PULSE WIDTH LOW	3	5	ms
T_{PWH}	PROGRAM PULSE WIDTH HIGH	500		μs
V_{PROG}*	PROGRAM AMPLITUDE	−55	−50	V
I_{PROG}	PROGRAM CURRENT		35	ma
T_{WS}	WRITE SET UP TIME	10		μs
T_{WH}	WRITE HOLD TIME	5		μs
T_{RS}	READ SET UP TIME	10		μs

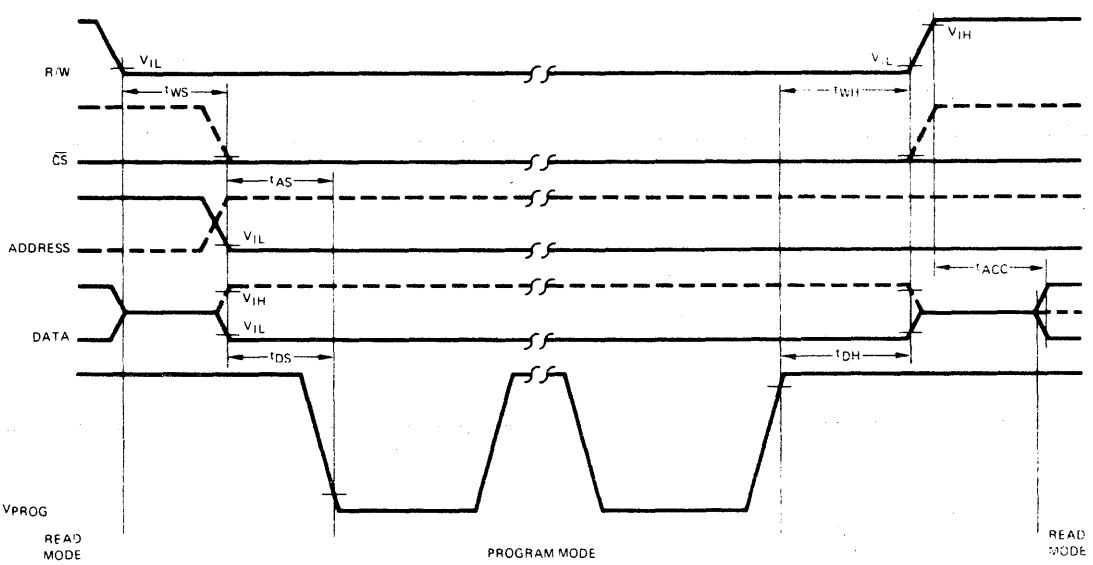
*Note that in the WRITE mode the MIN value of V_{PROG} should not be exceeded and that chip select, address, and data lines may remain at TTL level, as in the READ mode.

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PROGRAMMING CYCLE TIMING WAVEFORMS



READ/PROGRAM/READ CYCLE TIMING WAVEFORM



CONTROL FUNCTION TRUTH TABLE

CS	R/W	V_{PROG}	MODE	OUTPUTS
0	0	V_{PROG}	Write	Active Data Inputs
0	1	V_{CC}	Read	Active
1	X	X	Standby	Floating

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OPERATION

Initially, and after each erasure, all bits of the 6834 are in the logic "0" state (output 0 volts). Data is stored by selectively programming a logic "1" into the desired bit locations. The R/W input (pin 14) is used to select the desired mode of operation. When the R/W input is at logic "0" the chip is in the write enable mode of operation. The outputs (0_1 –0_8) are disabled (floating) with the corresponding pins becoming the data inputs ($0_1 \rightarrow D_{IN\ 1}$ etc.). The word address is selected in the same manner as in the read mode. Data to be programmed are presented 8 bits in parallel and after the address and data are set up a programming pulse (V_P –50 volts) is applied. V_{PROG} electrically writes the data into the memory array. Writing may be inhibited by deselecting the chip with the CS input at a logic "1" during the write cycle. This feature allows true "on board" programming in bus organized systems where the R/W and V_{PROG} inputs are common and the device to be programmed is selected by means of the chip select input as during read operations.

The amount of program energy required to insure memory retention may be defined as a function of the number of program pulses (N) times the program pulse width (t_{pw}) ($N \times t_{pw} \geqslant 60$ msec). This means if a 3 ms pulse is used, 20 program pulses are required, and if a 5 ms pulse is used 12 program pulses are required.

The read operation is accomplished by a logic "1" at the R/W input with the program input connected to V_{SS} potential. True data (data out = data in) is valid after the address is stable. The CS input will disable (float) the outputs when at a logic "1" to allow or tie capability.

Erasure is accomplished by exposing the array to a high intensity ultra-violet light source (such as, Ultra-Violet Products, Inc. Lamp Model S52 or UVS-54) for a period of 7 to 10 minutes. The clear optical lid should be approximately one inch away from the lamp tubes.

INTERFACE DESCRIPTION

Pin	Label	Function
(2)	D0	**Data Lines** – with the R/W line selected for Read (V_{IH}), the Data Lines (D0 through D7) are set to reflect the contents of the selected memory location. When the R/W line is set for Write (V_{IL}), the Data Lines are input to the addressed location of the 6834 when V_{PROG} is present. The Data Bus output drivers are three-state devices that remain in the high impedance (off) state when CS is in the V_{IH} state of when R/W is in the V_{IL} state.
(3)	D1	
(4)	D2	
(5)	D3	
(6)	D4	
(7)	D5	
(8)	D6	
(9)	D7	
(14)	R/W	**Read/Write** – When this input line is set to V_{IH}, the device is in the Read mode, a low (V_{IL}) signal puts it into the Write mode.
(15)	CS	**Chip Select** – This input line must be set to V_{IL} for a Read or Write operation to be performed. When it is High (V_{IH}) the output data bus is set to a high-impedance three-state condition and disables the Write operation.
(11)	V_{PROG}	**Program** – In the Write mode, a programming pulse (–50V dc) at this input causes the data at the Data Lines to be stored in the selected address. This pin should be tied to V_{CC} for normal Read operations.
(24)	A0	**Address Lines** – These lines select the 8 bit word in memory for Read or Write operation
(23)	A1	
(22)	A2	
(21)	A3	
(20)	A4	
(19)	A5	
(18)	A6	
(17)	A7	
(16)	A8	

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EMM 4104

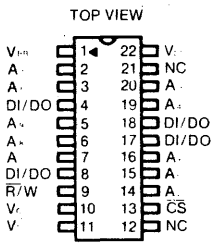
SEMI 4104 150NSEC, STATIC, TTL IN/OUT, 1024x4 N-MOS RAM

FEATURES

- Access time as low as 150 ns max
- Cycle time as low as 350 ns max
- Static—no refresh required
- TTL Compatible Inputs/Outputs
- On Chip Address Register
- 1Kx4 Organization Ideal for Microprocessor Applications
- Low Operating Power 450 mw typ
- Low Standby Power 35mw typ
- Data Retention Mode, $V_{DD} = 4V$; $V_{BB} = -4V$
- Standard 22 pin dip
- Non-Inverted Data Output
- Voltage Compatible with Popular Microprocessors

PIN CONFIGURATION

A_N	Address Inputs
DI/DO	Data Input/Data Output
$\overline{CS}$	Chip Select Input
R/W	Read/Write Input
N/C	No Internal Connection
V_{SS}	Ground
V_{BB}	Supply Voltage (—5V)
V_{CC}	Supply Voltage (+5V)
V_{DD}	Supply Voltage (+12V)



ORDERING INFORMATION

Part Number	Speed Access	Speed Cycle	Package
4104ACC	200	350	Ceramic
4104ACP	200	350	Plastic
4104BCC	150	300	Ceramic
4104BCP	150	300	Plastic

DC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range Unless Otherwise Noted)

CHARACTERISTICS	SYMBOL	4104A MIN	4104A MAX	4104B MIN	4104B MAX	UNIT	CONDITIONS
Input Current	I_{IN}	—20	+20	—20	+20	μA	V_{IN} = 0.7V or 5V
Chip Select Input Current	I_{CS}	—20	+20	—20	+20	μA	V_{CS} = 0.5V or 12V
Output "Low" Voltage	V_{OL}	—	0.5	—	0.5	Vdc	I_{OL} = 2.0mA Fig. 5
Output "High" Voltage	V_{OH}	2.7	—	2.7	—	Vdc	I_{OH} = 500 μA Fig. 5
Output Current (Unselected)	I_{DO}	—20	+20	—20	+20	μA	V_{OUT} = 2.7V, V_{CS} = 12V
Supply Current (Selected and Averaged over one cycle) 4104A / 4104B: T_{CSW} 200 / 150; T_C 350 / 300; For Other Conditions See Figure 3	I_{DD}	—	50	—	55	mA	T_{AMB} = 25°C; V_{DD} = 12V; V_{CC} = 5V; V_{BB} = —5V; V_{CS} = 12V
Supply Current (Unselected) T_{AMB} = 25°C	I_{DD}	—	5	—	5	mA	V_{DD} = 12V
Supply Current (Unselected) T_{AMB} = 70°C7	I_{DD}	—	15	—	15	mA	V_{CC} = 5V
Substrate Current	I_{BB}	—	—3	—	—3	mA	V_{BB} = —5V
Reference Supply Current	I_{CC}	—	100	—	100	μA	V_{CS} = 12V
Standby Current at Reduced Voltages T_{AMB} = 25°C	I_{DDS}	—	2	—	2	mA	V_{CS} = 4V to 15V; V_{DD} = 4V; V_{BB} = —4V; V_{CC} = OV
Standby Current at Reduced Voltages T_{AMB} = 70°C	I_{DDS}	—	6	—	6	mA	V_{CS} = 4V to 15V; V_{DD} = 4V; V_{BB} = —4V; V_{CC} = OV

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READ CYCLE — AC CHARACTERISTICS

CHARACTERISTICS	SYMBOL	4104A MIN	4104A MAX	4104B MIN	4104B MAX	UNIT	CONDITIONS
Chip Select Read Pulse Width	T_{CSR}	200	—	150	—	ns	
Chip Select Rise and Fall Time*	T_{CR}, T_{CF}	—	100	—	100	ns	FULL
Set Up Time	T_P	0	—	0	—	ns	OPERATING
Access Time	T_A	—	200	—	150	ns	VOLTAGE
Cycle Time, $T_{CR}=T_{CF}$ = 10ns	T_C	350	—	300	—	ns	AND
Data Hold Time	T_H	100	—	100	—	ns	TEMPERATURE
Output Recovery Time	T_{DR}	10	—	10	—	ns	RANGE
Read Recovery Time	T_{CRR}	125	—	125	—	ns	

WRITE CYCLE — AC CHARACTERISTICS

CHARACTERISTICS	SYMBOL	4104A MIN	4104A MAX	4104B MIN	4104B MAX	UNIT	CONDITIONS
Chip Select Write Pulse Width	T_{CSW}	200	—	150	—	ns	FULL
Chip Select Rise and Fall Time*	T_{CR}, T_{CF}	—	100	—	100	ns	OPERATING
Set Up Time	T_P	0	—	0	—	ns	VOLTAGE
Cycle Time, $T_{CR}=T_{CF}$ = 10 ns	T_C	350	—	300	—	ns	AND
Data Hold Time	T_H	100	—	100	—	ns	TEMPERATURE
Write Recovery Time	T_{CWR}	125	—	125	—	ns	RANGE

*Typical Chip Select Rise and Fall Time (T_{CR} and T_{CF}) is 10 ns For Read and Write Cycle

Figure 1 — READ CYCLE

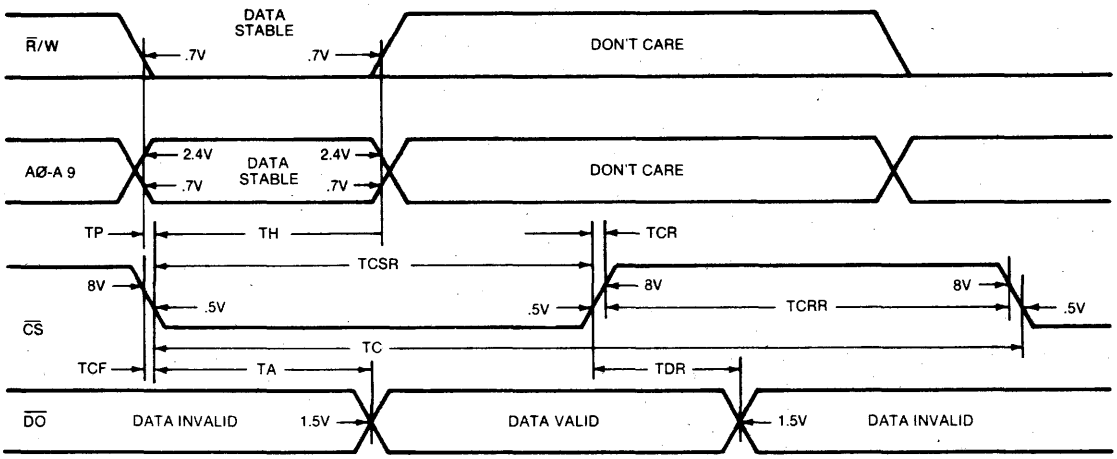
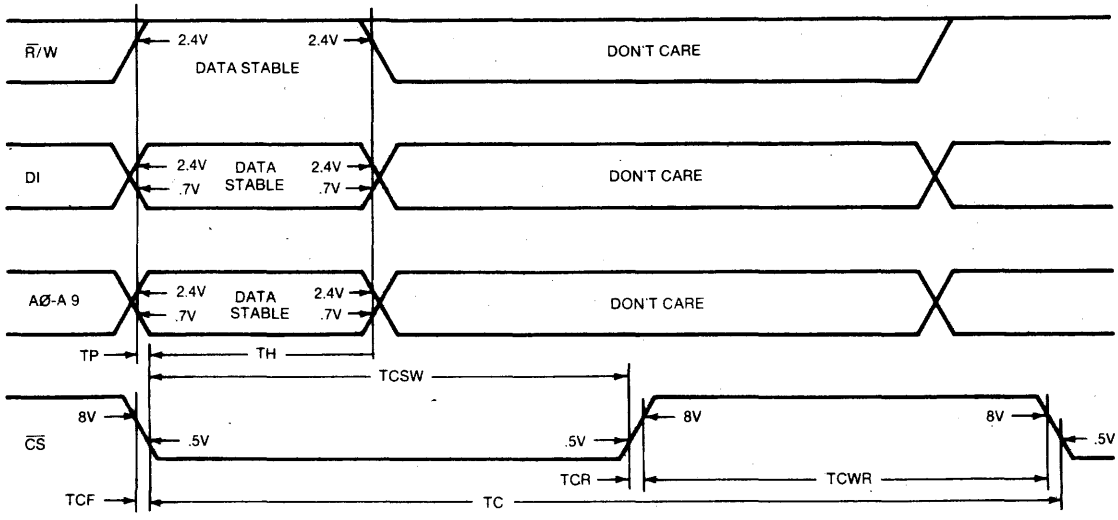


Figure 2 — WRITE CYCLE



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EMM 4200

SEMI 4200 150NSEC, STATIC, TTL IN/OUT, 4096x1 N-MOS RAM

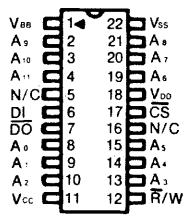
FEATURES

- Completely Static
- Access Time as low as 150 nsec max
- Cycle Time as low as 300 nsec max
- Typical Operating Power Under 450 mw.
- Typical Standby Power Under 35 mw.
- Data Retention with Low V_{DD}
- Pin and Voltage Compatible with Standard 22 Pin 4K Dynamic Rams
- TTL Compatible Three-State Outputs
- Fully Decoded
- Active Low Chip Select

PIN CONFIGURATION

A_N	Address Inputs
DI	Data Input
$\overline{DO}$	Data Output
$\overline{CS}$	Chip Select Input
R/W	Read/Write Input
N/C	No Internal Connection
V_{SS}	Ground
V_{BB}	Supply Voltage (—5V)
V_{CC}	Supply Voltage (+5V)
V_{DD}	Supply Voltage (+12V)

TOP VIEW



ORDERING INFORMATION

Part Number	Speed Access	Speed Cycle	Package
4200ACC	200	350	Ceramic
4200ACP	200	350	Plastic
4200BCC	150	300	Ceramic
4200BCP	150	300	Plastic

DC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range Unless Otherwise Noted)

CHARACTERISTICS	SYMBOL	4200A MIN	4200A MAX	4200B MIN	4200B MAX	UNIT	CONDITIONS
Input Current	I_{IN}	—20	+20	—20	+20	μA	V_{IN} = 0.7V or 5V
Chip Select Input Current	I_{CS}	—20	+20	—20	+20	μA	V_{CS} = 0.5V or 12V
Output "Low" Voltage	V_{OL}	—	0.5	—	0.5	Vdc	I_{OL} = 2.0mA Fig. 5
Output "High" Voltage	V_{OH}	2.7	V_{CC}	2.7	V_{CC}	Vdc	I_{OH} = 500 μA Fig.5
Output Current (Unselected)	I_{DO}	—20	+20	—20	+20	μA	V_{OUT} = 2.7V, V_{CS} = 12V
Supply Current (Selected and Averaged Over One Cycle) 4200A / 4200B: Tcsw 200 / 150; Tc 350 / 300; For Other Conditions See Figure 3	I_{DD}	—	50	—	55	mA	T_{AMB} = 25°C; V_{DD} = 12V; V_{CC} = 5V; V_{BB} = —5V; V_{CS} = 12V
Supply Current (Unselected) T_{AMB} = 25°C	I_{DD}	—	5	—	5	mA	V_{DD} = 12V; V_{CC} = 5V; V_{BB} = —5V; V_{CS} = 12V
Supply Current (Unselected) T_{AMB} = 70°C	I_{DD}	—	15	—	15	mA	
Substrate Current	I_{BB}		—3	—	—3	mA	
Reference Supply Current	I_{CC}	—	100	—	100	μA	
Standby Current At Reduced Voltages T_{AMB} = 25°C	I_{DDS}	—	2	—	2	mA	V_{CS} = 4V to 15V; V_{DD} = 4V; V_{BB} = —4V; V_{CC} = 0V
Standby Current At Reduced Voltages T_{AMB} = 70°C	I_{DDS}	—	6	—	6	mA	

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READ CYCLE — AC CHARACTERISTICS

CHARACTERISTICS	SYMBOL	4200A MIN	4200A MAX	4200B MIN	4200B MAX	UNIT	CONDITIONS
Chip Select Read Pulse Width	T_{CSR}	200	—	150	—	ns	FULL OPERATING VOLTAGE AND TEMPERATURE RANGE
Chip Select Rise and Fall Time*	T_{CR} ,T_{CF}	—	100	—	100	ns	
Set Up Time	T_P	0	—	0	—	ns	
Access Time	T_A	—	200	—	150	ns	
Cycle Time, $T_{CR}=T_{CF}=10$ns	T_C	350	—	300	—	ns	
Data Hold Time	T_H	100	—	100	—	ns	
Output Recovery Time	T_{DR}	10	—	10	—	ns	
Read Recovery Time	T_{CRR}	125	—	125	—	ns	

WRITE CYCLE — AC CHARACTERISTICS

CHARACTERISTICS	SYMBOL	4200A MIN	4200A MAX	4200B MIN	4200B MAX	UNIT	CONDITIONS
Chip Select Write Pulse Width	T_{CSW}	200	—	150	—	ns	FULL OPERATING VOLTAGE AND TEMPERATURE RANGE
Chip Select Rise and Fall Time*	T_{CR} ,T_{CF}	—	100	—	100	ns	
Set Up Time	T_P	0	—	0	—	ns	
Cycle Time, $T_{CR}=T_{CF}=10$ns	T_C	350	—	300	—	ns	
Data Hold Time	T_H	100	—	100	—	ns	
Write Recovery Time	T_{CWR}	125	—	125	—	ns	

*Typical Chip Select Rise and Fall Time (T_{CR} and T_{CF}) is 10 ns For Read and Write Cycle

Figure 1 — READ CYCLE

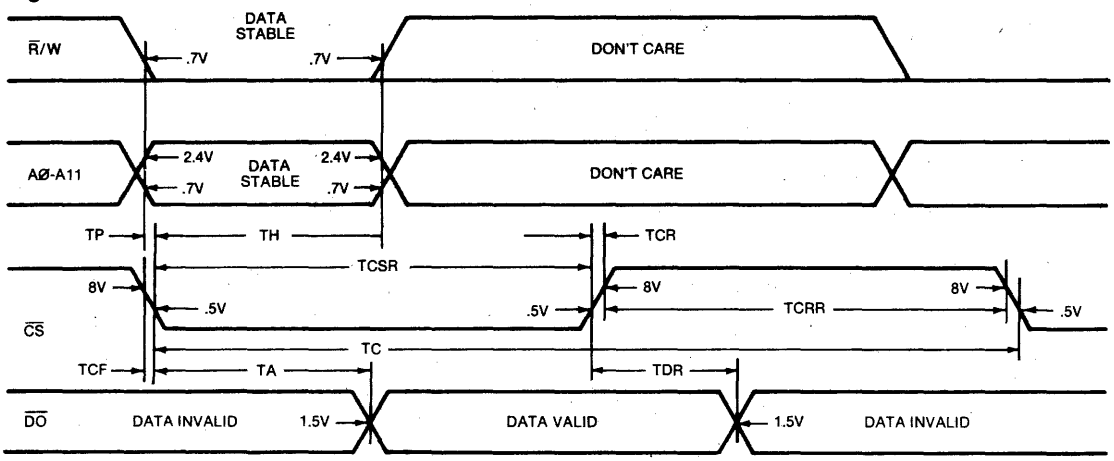
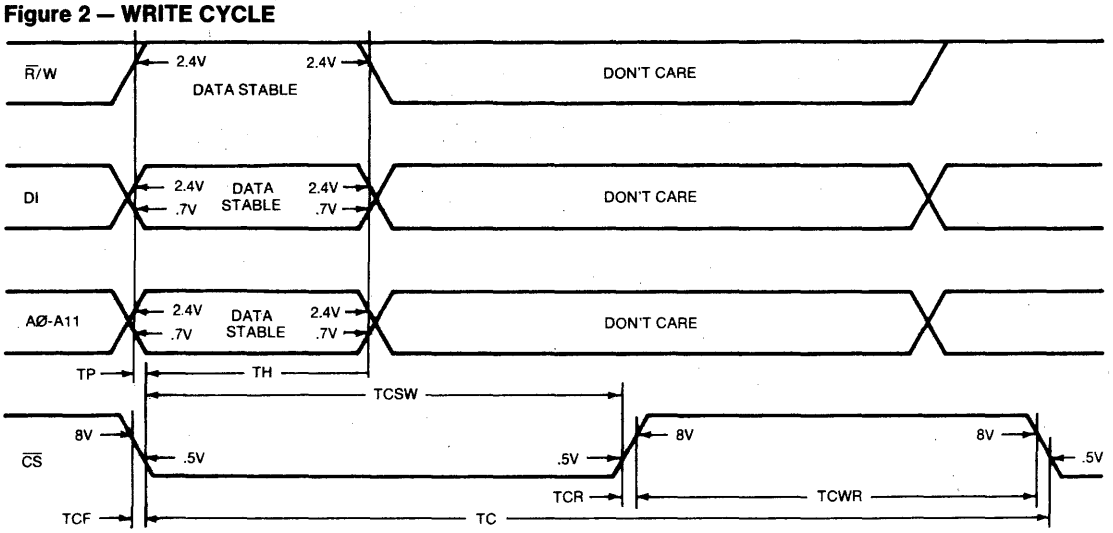


Figure 2 — WRITE CYCLE



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EMM 4801/4804

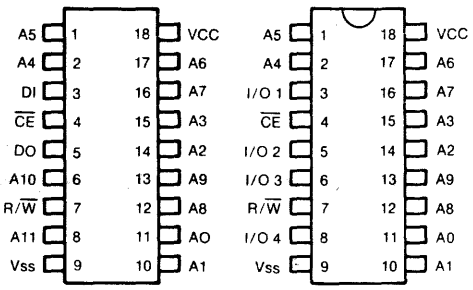
SEMI 4801 450NSEC, STATIC, TTL IN/OUT 4096x1 N-MOS RAM
SEMI 4804 450NSEC, STATIC, TTL IN/OUT 1024x4 N-MOS RAM

FEATURES

- Single +5V Power Supply
- Replaces 4 1024x1 Static RAMs
- Completely Static— No Clocks or Refresh
- 18 Pin Package
- Access/Cycle Times As Low As 400 nsec max
- 250 mw Typical Operating Power
- TTL Compatible I/O
- Three State Outputs

PIN CONFIGURATION

A_N	Address Inputs
DI	Data Input
DO	Data Output
$\overline{CE}$	Chip Enable
R/$\overline{W}$	Read/Write
V_{SS}	Ground
V_{CC}	+5V Power Supply
I/O_N	Data Input/Output



TRUTH TABLE

$\overline{CE}$	R/$\overline{W}$	DI	DO	STATUS	MODE
H	Don't Care	Don't Care	High Z	Deselect	Standby
L	H	Don't Care	Data	Selected	READ
L	L	L	High Z	Selected	Write 0
L	L	H	High Z	Selected	Write 1

ORDERING INFORMATION

Part Number	Speed
4801 UCC	600 nsec
4801 ACC	450 nsec
4801 BCC	400 nsec
4804 UCC	600 nsec
4804 ACC	450 nsec
4804 BCC	400 nsec

DC ELECTRICAL CHARACTERISTICS (Full Operating Voltage & Temperature Range Unless Otherwise Noted)

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Input Leakage Current	I_{LI}	−10		+10	μA	V_{IN} = 0.5V or +5V
Output Leakage Current	I_{LO}	−10		+10	μA	V_{OUT} = 2.4V
Output Voltage High	V_{OH}	2.4		V_{CC}	Vdc	I_{OH} = −200μa
Output Voltage Low	V_{OL}			0.4	Vdc	I_{OL} = 2.0ma
Power Supply Current	I_{CC}		45	75	ma	V_{CC} = 5V; 25°C
	I_{CC}		65	100	ma	V_{CC} = 5V; 70°C

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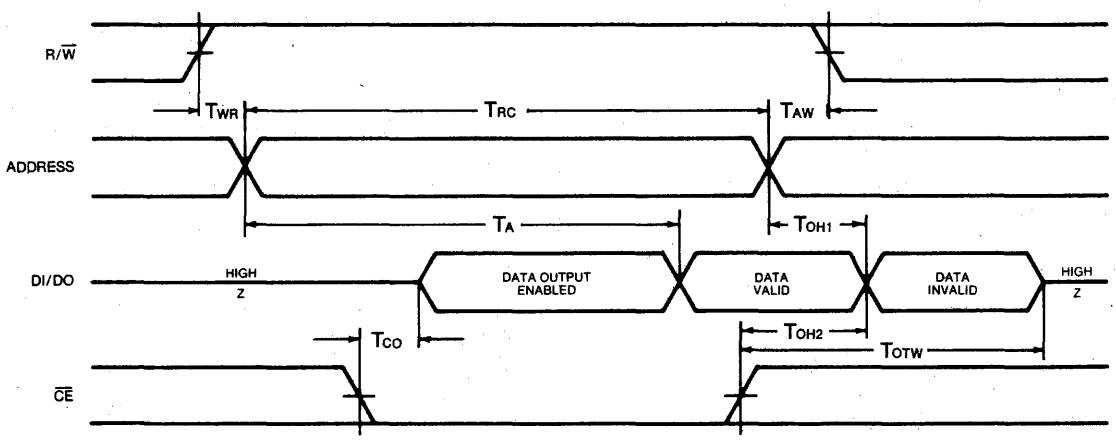
READ CYCLE—AC CHARACTERISTICS

PARAMETER	SYMBOL	4804 MIN	4804 MAX	4804A MIN	4804A MAX	4804B MIN	4804B MAX	CONDITIONS
Read Cycle Time	T_{RC}	600		450		400		Full Operating Voltage and Temperature Range
Access Time	T_A		600		450		400	
Chip Enable to Output Enable	T_{CO}		200		150		140	
Data Valid After Address	T_{OH1}	150		100		85		
Previous Data Valid After Chip De-Select	T_{OH2}	25		25		25		

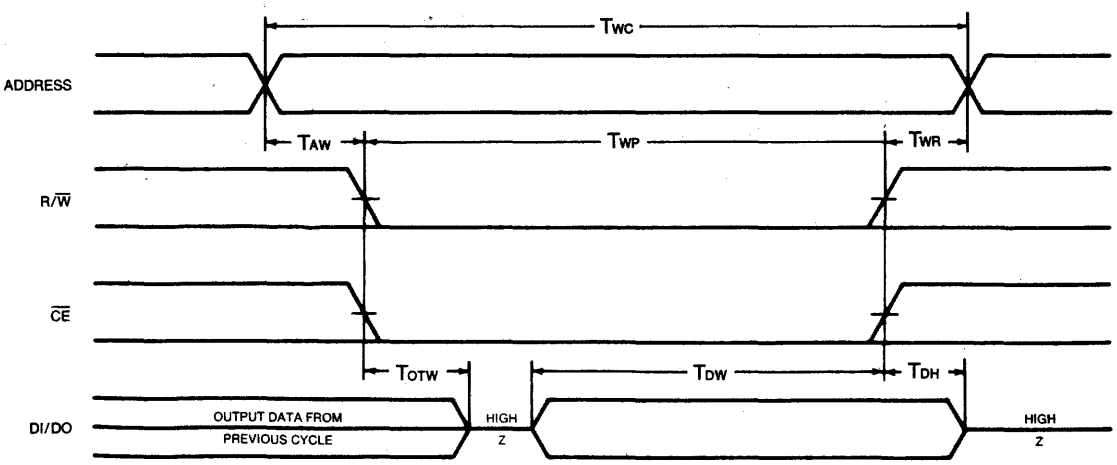
WRITE CYCLE—AC CHARACTERISTICS

PARAMETER	SYMBOL	4804 MIN	4804 MAX	4804A MIN	4804A MAX	4804B MIN	4804B MAX	CONDITIONS
Write Cycle Time	T_{WC}	600		450		400		Full Operating Voltage and Temperature Range
Address To Write Time	T_{AW}	100		75		65		
Write Pulse Width	T_{WP}	500		375		330		
Write Recovery Time	T_{WR}	0		0		0		
Data Set Up Time	T_{DW}	350		250		225		
Data Hold Time	T_{DH}	0		0		0		
Output Disable From Write or Chip Enable	T_{OTW}		150		125		110	

READ CYCLE TIMING



WRITE CYCLE TIMING



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EMM 3539

SEMI 3539 400NSEC, STATIC, TTL IN/OUT 256x8 N-MOS RAM

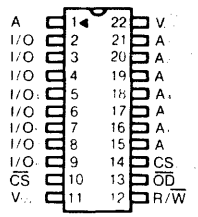
FEATURES

- 256 x 8 with Common I/O Bus
- Standard 22-Pin Dip
- Single +5V Power Supply
- Completely Static — No Clocks or Refresh
- Totally TTL Compatible
- 400 ns Maximum Access Time
- Less than 400 mW Power Dissipation
- Two Separate Chip Select Inputs
- Separate Output Disable Function

PIN CONFIGURATION

A_n	Address Inputs
$\overline{CS}_n$	Chip Select Inputs
$\overline{OD}$	Output Disable
$R/\overline{W}$	Read/Write Control Input
I/O_n	Data Bus Pins
V_{DD}	+5 V Power Supply
V_{SS}	0 V Power Supply

TOP VIEW



TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{OD}$	$R/\overline{W}$	STATUS	I/O BUS MODE
H	X	X	X	DESELECTED	HI Z
X	L	X	X	DESELECTED	HI Z
L	H	L	L	WRITE MODE	OUTPUT DISENABLE DATA CAN BE WRITTEN
L	H	H	L	WRITE MODE	OUTPUT ENABLED DATA CAN NOT BE WRITTEN
L	H	L	H	READ MODE	OUTPUT DISABLED DATA CAN NOT BE READ
L	H	H	H	READ MODE	OUTPUT ENABLED DATA CAN BE READ

X = IRRELEVENT STATE

ORDERING INFORMATION

Part Number	Access Time	Package
3539UCD	650ns	Frit-seal
3539UCP	650ns	Plastic
35392CD	500ns	Frit-seal
35392CP	500ns	Plastic
35391CD	400ns	Frit-seal
35391CP	400ns	Plastic

DC CHARACTERISTICS (Full Operating Voltage & Temperature Range Unless Otherwise Noted)

SYMBOL	PARAMETER	35391		35392		3539		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{IH}	Input HIGH Voltage	2.2		2.2		2.2		V	
V_{IL}	Input LOW Voltage		0.65		0.65		0.65	V	
V_{OH}	Output HIGH Voltage	2.2		2.2		2.2		V	$I_{OH} = -100\ \mu A$
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	$I_{OL} = 1.6$ mA
I_{BH}	Bus HIGH Current		10		10		10	μA	$V_{IN} = V_{DD}$, Chip Deselected
I_{BL}	Bus LOW Current		−10		−10		−10	μA	$V_{DD} = 0$ V, Chip Deselected
I_{IN}	Input Leakage Current		10		10		10	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
I_{DD}	Power Supply Current		75		75		75	mA	$V_{DD} = 5.25$ V
PD	Power Dissipation		394		394		394	mW	$V_{DD} = 5.25$ V

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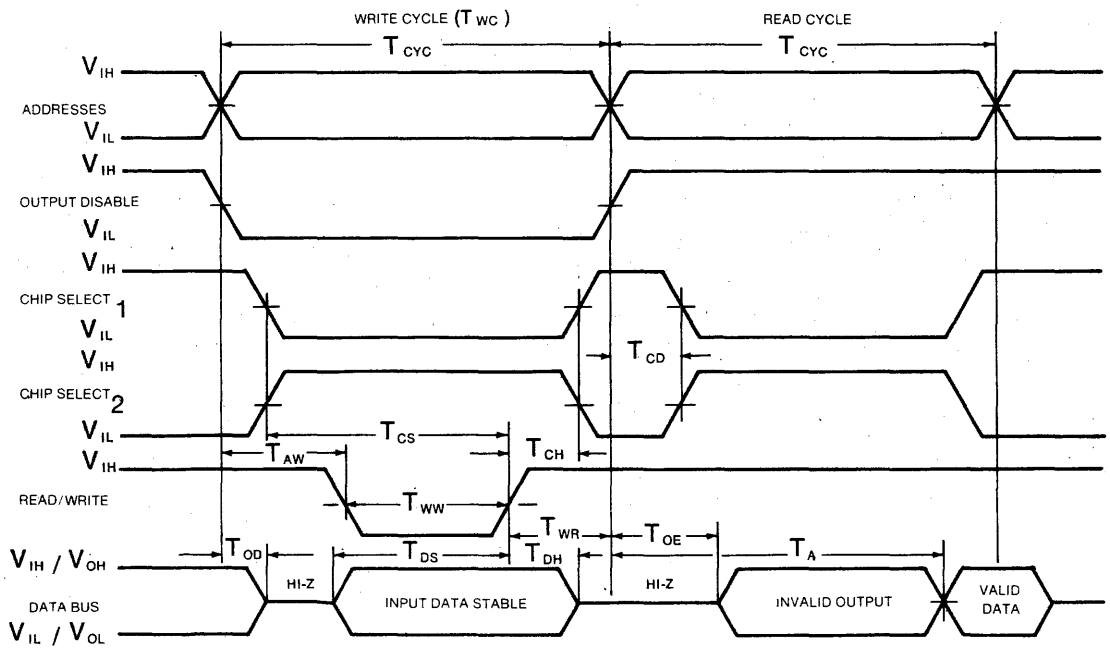
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AC CHARACTERISTICS (Full Operating Voltage & Temperature Range Unless Otherwise Noted)

SYMBOL	PARAMETER	35391		35392		3539		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
T_{CYC}*	Read Cycle Time	400		500		650		ns	
T_A	Read Access Time		400		500		650	ns	
T_{AW}	Address to Write Delay	25		25		25		ns	
T_{DS}	Data Set-Up Time	200		250		275		ns	
T_{DH}	Data Hold Time	0		0		0		ns	
T_{WR}	Write Recovery Time	0		0		0		ns	
T_{WW}	Write Pulse Width	150		175		225		ns	
T_{CS}	Chip select to write set-up time	125		150		200		ns	
T_{CD}	Chip Select Delay Time		100		100		100	ns	
T_{CH}	Chip select to write hold time	0		0		0		ns	
T_{OD}	Output Disable Time		150		150		150	ns	
T_{OE}	Output Enable Time		200		225		250	ns	

*$T_{WC} = (T_{AW} + T_{WW} + T_{WR})$ or $(T_{OD} + T_{DS})$, whichever is relevant.

3539 TIMING DIAGRAM



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EMM 2114

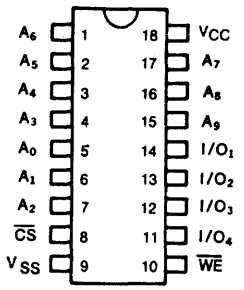
SEMI 2114 450NSEC, STATIC, TTL IN/OUT 1024x4 N-MOS RAM

FEATURES

- 1024 × 4 Organization
- Common I/O Bus
- Single +5 V Power Supply
- Low Power (300 mw)
- Completely Static — No Clock or Refresh
- 450 nSec Maximum Access Time
- Directly TTL Compatible I/O
- Three State Outputs
- 18 Pin Package

PIN CONFIGURATION

A_N	Address Inputs
I/O_N	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{SS}	Ground
V_{CC}	+5 V Power Supply



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	I/O	STATUS	MODE
H	Don't Care	High Z	Deselect	Standby
L	H	Data	Selected	READ
L	L	L	Selected	Write 0
L	L	H	Selected	Write 1

ORDERING INFORMATION

Package	Part Number	Icc Max.
18 Pin Ceramic	2114 UCA	100
18 Pin Plastic	2114 UCB	100
18 Pin Ceramic	L2114 UCA	60
18 Pin Plastic	L2114 UCB	60

DC ELECTRICAL CHARACTERISTICS (Full Operating Voltage & Temperature Range Unless Otherwise Noted)

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Input Leakage Current	I_{LI}	−10		+10	μA	V_{IN} = 0 to 5.25 V
Output Leakage Current	I_{LO}	−10		+10	μA	$\overline{CS}$ = 2.4 V $V_{I/O}$ = 0.4 V to Vcc
Output Voltage High	V_{OH}	2.4			Vdc	I_{OH} = −200μa
Output Voltage Low	V_{OL}			0.4	Vdc	I_{OL} = 2.1 ma
Power Supply Current 2114 UCA/UCB	Icc			60	ma	Vcc = 5.V; 0°C
	Icc			70	ma	Vcc = 5.V; 25°C
	Icc		55	100	ma	Vcc = 5.V; 70°C
Power Supply Current L2114 UCA/UCB	Icc			40	ma	Vcc = 5.V; 0°C
	Icc			45	ma	Vcc = 5.V; 25°C
	Icc		40	60	ma	Vcc = 5.V; 70°C

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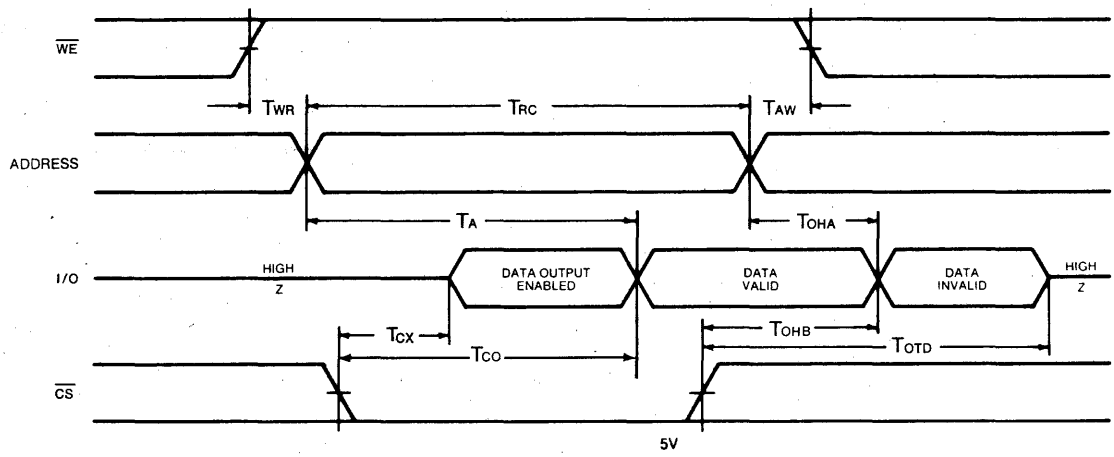
READ CYCLE —AC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	CONDITIONS
Read Cycle Time	T_{RC}	450	300		Full Operating Voltage and Temperature Range
Access Time	T_A		300	450	
Output Valid After Chip Selection	T_{CO}			100	
Output Active After Chip Selection	T_{CX}	20ns			
Data Valid After Address	T_{OHA}	50ns			
Previous Data Valid After Chip Deselection	T_{OHB}	25ns			
Output Disable from Deselection	T_{OTD}			100	

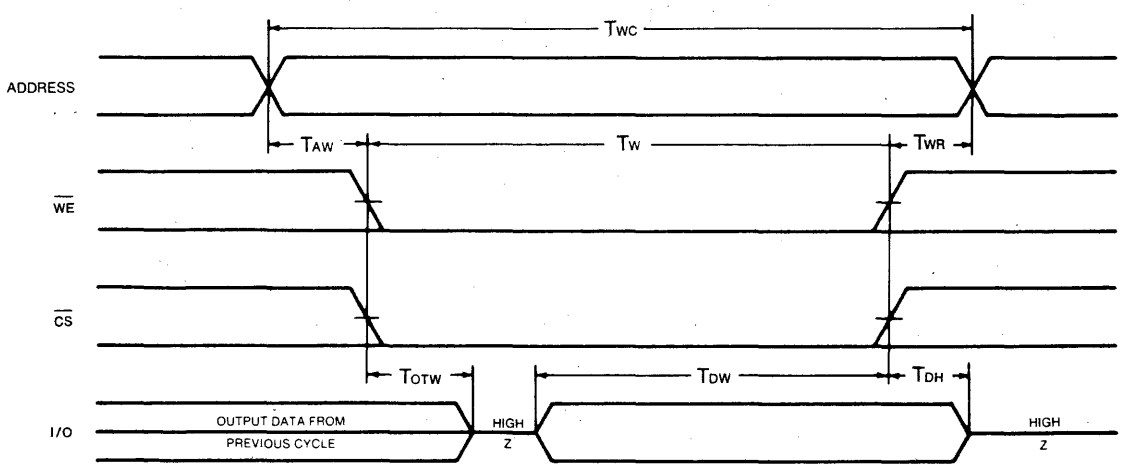
WRITE CYCLE—AC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	CONDITIONS
Write Cycle Time	T_{WC}	450	300		Full Operating Voltage and Temperature Range
Address To Write Time	T_{AW}	0			
Write Pulse Width	T_W	200	150		
Write Recovery Time	T_{WR}	0			
Data Set Up Time	T_{DW}	200			
Data Hold Time	T_{DH}	0			
Output Disable From Write or Chip Enable	T_{OTW}			100	

READ CYCLE TIMING



WRITE CYCLE TIMING



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PRELIMINARY SPECIFICATION

EMM SEMI

8K STATIC N-MOS RAM

8108 8308

1024 X 8, 300 ns, TTL In/Out

GENERAL DESCRIPTION

EMM SEMI part numbers 8108/8308 are 8192-bit static RAMS, ideally suited for microprocessor applications. The 8108/8308 have common data input/output pins for connection to a data bus. They require only a single +5 volt power supply, and are TTL compatible on all inputs and outputs. These devices also have a low power disabled mode which dissipates less than 60 mW power.

FUNCTIONAL DESCRIPTION

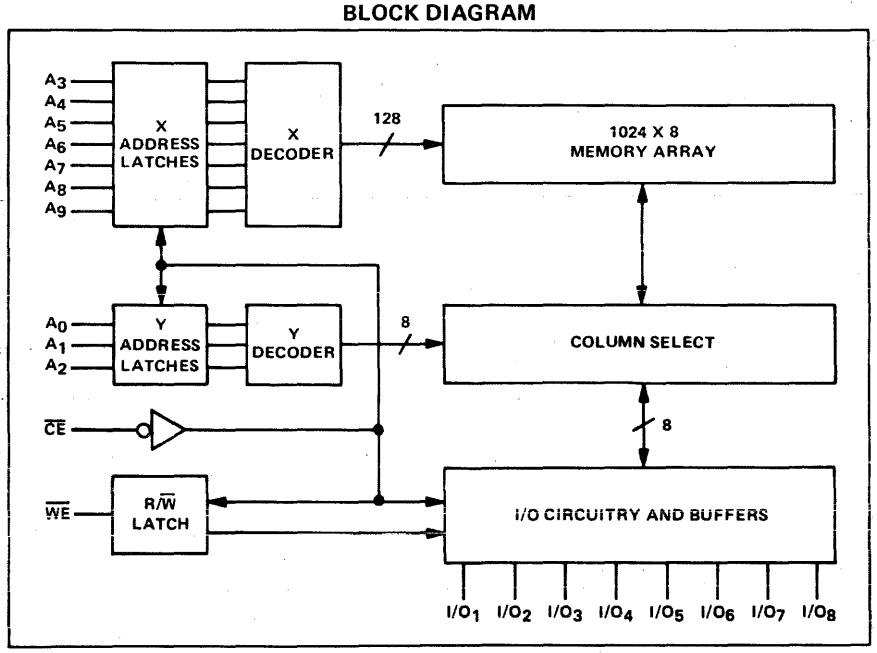
The EMM SEMI 8108/8308 are 8192-bit static RAMS with memory cells organized in eight arrays of 128 rows by 8 columns (1024 words X 8 bits). Each eight-bit word is addressed by simultaneously decoding the X addresses (A_3 through A_9) for the rows, and the Y addresses (A_0 through A_2) for the columns. Data is written or read in parallel on eight common input/output pins (I/O_n). The operation of the 8108/8308 is controlled by Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$).

When $\overline{CE}$ is high, all outputs are in an inoperative high impedance state, and power is supplied only to the memory elements. When $\overline{CE}$ is low, the memory is enabled for reading and writing.

The negative going edge of $\overline{CE}$ begins timing for a read cycle. Data on $\overline{WE}$ and address pins(A_n) must be stable for time T_H. $\overline{WE}$ and A_n will then have been latched into "D" type flip flops and no longer need to be held stable. Output data will be presented on the eight output pins (I/O_n) within time T_A and will remain until time T_{DR} after $\overline{CE}$ goes high. Data will then be invalid. After time T_C another read or write cycle can be initiated.

The negative going edge of $\overline{CE}$ also begins timing for a write cycle. $\overline{WE}$ and I/O must be held stable for time T_H. These inputs will then have been latched and I/O will be entered within time T_{CSW}. Another read or write cycle can be initiated after time T_C.

BLOCK DIAGRAM



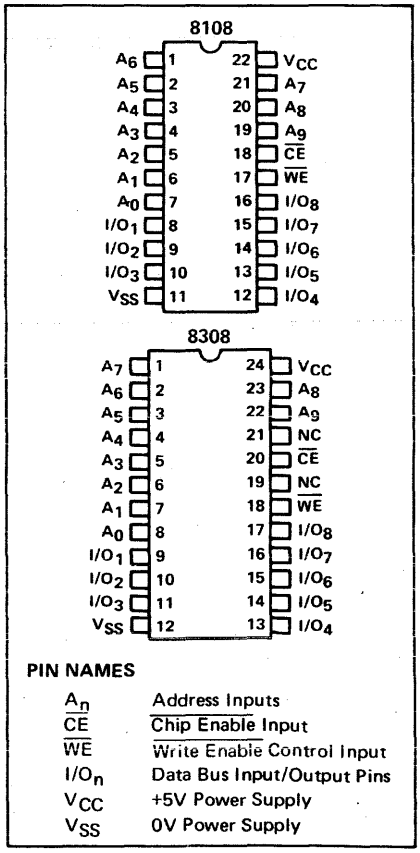
- 1024 words X 8 bits
- EPROM, PROM, ROM pinout compatible
- Common I/O bus
- Single +5V power supply
- No max. limit on Chip Enable ($\overline{CE}$) pulse width
- 300 nSec maximum access time
- Less than 60 mW power (disabled)
- Less than 270 mW power (enabled)
- Standard 22-pin DIP (8108)
- Standard 24-pin DIP (8308)

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	I/O_n	STATUS	MODE
H	Don't Care	High Z	Disabled	Standby
L	H	Data	Enabled	Read
L	L	L	Enabled	Write 0
L	L	H	Enabled	Write 1

CONNECTION DIAGRAMS

DIP (Top View)



PIN NAMES

A_n	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Control Input
I/O_n	Data Bus Input/Output Pins
V_{CC}	+5V Power Supply
V_{SS}	0V Power Supply

EMM SEMI reserves the right to make changes at any time in order to improve design and to supply the best product possible.

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DC CHARACTERISTICS: $T_A = 0^o$ C to $+70^o$ C, $V_{CC} = +5V \pm +5\%$, unless otherwise noted.

SYMBOL	PARAMETER	8108/8308 MIN	8108/8308 MAX	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	2.4		V	–
V_{IL}	Input LOW Voltage		0.8	V	–
V_{OH}	Output HIGH Voltage	2.4		V	$I_{OH} = -200\ \mu A$
V_{OL}	Output LOW Voltage		0.4	V	$I_{OL} = 2.1$ mA
I_{LO}	Output Leakage Current	-10	+10	μA	$V_{I/O} = 0.4$ V to V_{CC}, $\overline{CE} = 2.4$ V
I_{LI}	Input Leakage Current	-10	+10	μA	$V_{SS} < V_{IN} < V_{CC}$
I_{CC1}	Power Supply Current (Device Enabled)		50	mA	$\overline{CE} \leqslant 0.8$ V
I_{CC2}	Power Supply Current (Device Disabled)		10	mA	$\overline{CE} \geqslant 2.4$ V

READ CYCLE – AC CHARACTERISTICS

CHARACTERISTICS	SYMBOL	8108/8308 MIN	8108/8308 MAX	UNIT	CONDITIONS
Chip Enable Read Pulse Width	T_{CER}	300	∞	nS	Full Operating Voltage and Temperature Range
Chip Enable Rise and Fall Time*	T_{CR}, T_{CF}	–	100	nS	
Set Up Time	T_P	0	–	nS	
Access Time	T_A	–	300	nS	
Cycle Time, $T_{CR} = T_{CF} = 10$ nS	T_C	450	–	nS	
Data Hold Time	T_H	100	–	nS	
Output Recovery Time	T_{DR}	50	–	nS	
Read Recovery Time	T_{CRR}	130	–	nS	

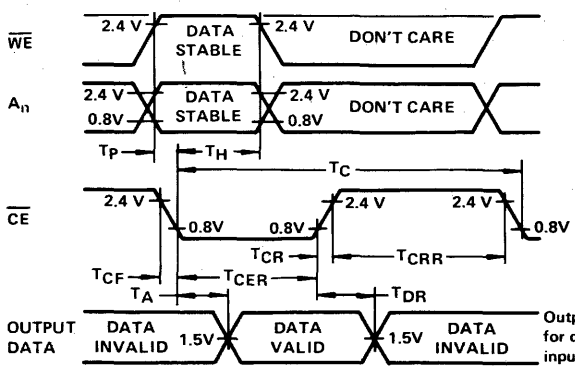
WRITE CYCLE – AC CHARACTERISTICS

CHARACTERISTICS	SYMBOL	8108/8308 MIN	8108/8308 MAX	UNIT	CONDITIONS
Chip Enable Write Pulse Width	T_{CEW}	300	∞	nS	Full Operating Voltage and Temperature Range
Chip Enable Rise and Fall Time*	T_{CR}, T_{CF}	–	100	nS	
Set Up Time	T_P	0	–	nS	
Cycle Time, $T_{CR} = T_{CF} = 10$ nS	T_C	450	–	nS	
Data Hold Time	T_H	100	–	nS	
Write Recovery Time	T_{CWR}	130	–	nS	

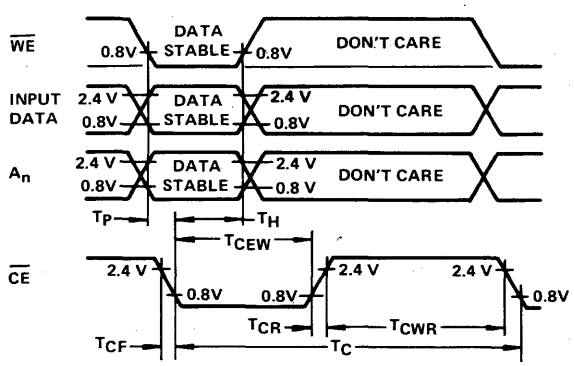
*Typical Chip Select Rise and Fall Time (T_{CR} and T_{CF}) is 10 nS For Read and Write Cycle

8108/8308 TIMING DIAGRAM

READ CYCLE – AC CHARACTERISTICS



WRITE CYCLE – AC CHARACTERISTICS



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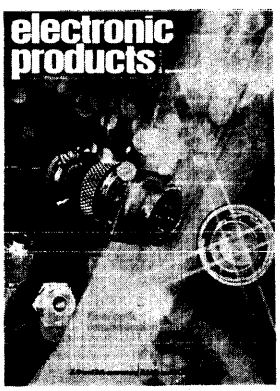
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F464

65,536 X 1 DYNAMIC SERIAL MEMORY

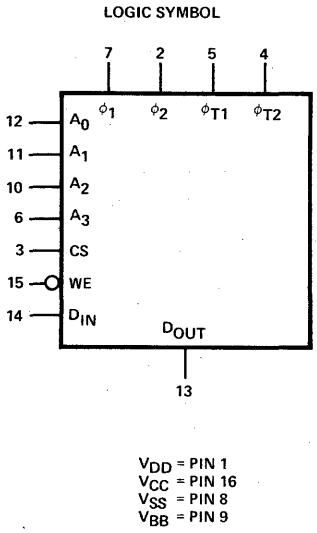
FAIRCHILD CHARGE COUPLED DEVICE

GENERAL DESCRIPTION – The F464 is a 65,536-bit dynamic serial memory configured as 16 randomly accessible shift registers, each 4096 bits long. Each of these shift registers is designed utilizing Charge Coupled Device (CCD) techniques with the interlaced Serial-Parallel-Serial (SPS) register structure which features both low power and high density characteristics. The high density of the F464 is further enhanced through the use of an electrode-per-bit memory cell approach. The high density permits packaging the memory in a standard 16-pin (0.3"-wide) dual in-line package which allows the construction of highly dense memory systems using widely available automated testing and insertion equipment.

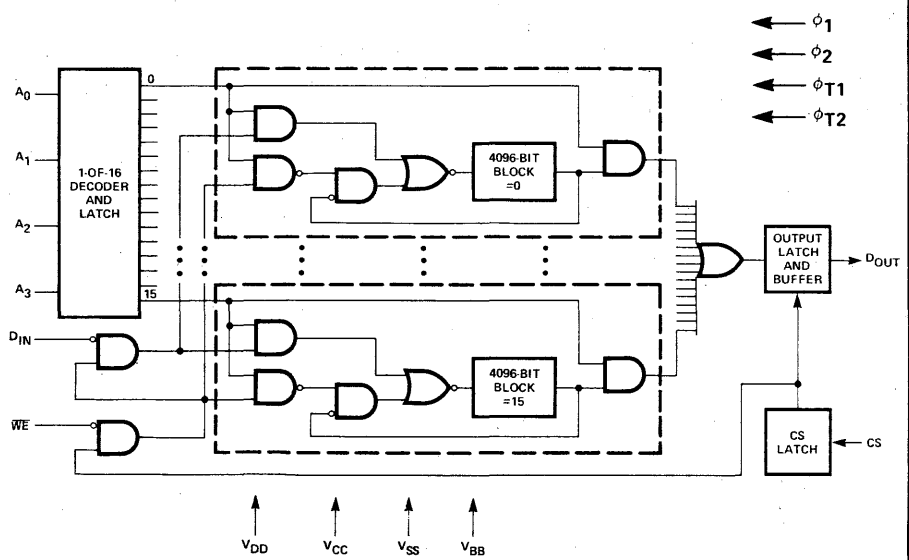
Furthermore, this buried-channel CCD memory is fabricated using Fairchild's double-poly n-channel Isoplanar process. This process allows the F464 to be a high performance, state-of-the-art memory circuit which is manufacturable in large volume.

- INDUSTRY STANDARD 16 PIN (0.3"-WIDE) DUAL IN-LINE PACKAGE.
- OPERATING FREQUENCY RANGE: 1 MHz TO 5 MHz.
- 15 μs HALT TIME AT 2.0 MHz
- LOW CAPACITANCE TTL-COMPATIBLE INPUTS (EXCEPT CLOCKS).
- 3-STATE, TTL-COMPATIBLE, LATCHED DATA OUTPUT.
- OUTPUT DRIVE CAPABILITY: 3.5 mA
- LOW CAPACITANCE 12 V CLOCKS:
  - ϕ_1 AND ϕ_2: 100 pF (TYP)
  - ϕ_{T1} AND ϕ_{T2}: 30 pF (TYP)
- LOW POWER
  - NORMAL OPERATION: <336 mW (MAX) @ f_{max}
  - STANDBY: <66 mW (MAX) @ f_{min}
- STANDARD POWER SUPPLIES (+12 V, +5 V, AND –5 V)

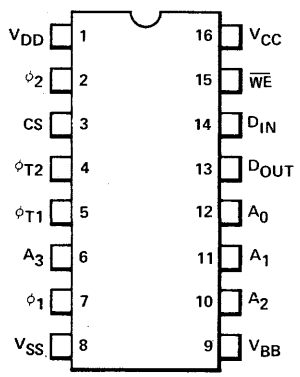
LOGIC SYMBOL



BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



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FAIRCHILD

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PIN NAMES

ϕ_1, ϕ_2	Serial Clocks	D_{IN}	Data Input
ϕ_{T1}, ϕ_{T2}	Transfer Clocks	D_{OUT}	Data Output
A_n	Address Inputs	V_{CC}	+5 V Power Supply
CS	Chip Select Input	V_{SS}	0 V Power Supply, GND
$\overline{WE}$	Write Enable Input (Active LOW)	V_{BB}	−5 V Power Supply
		V_{DD}	+12 V Power Supply

FUNCTIONAL DESCRIPTION

ORGANIZATION – The F464 is a 65,536 x 1 bit dynamic serial memory organized internally as 16 dynamic shift registers (or blocks) of 4096 bits each in length. These 16 shift register blocks are randomly accessible through four internally decoded Address inputs (A_0 – A_3). When a given register is selected, its input and output are internally connected (as needed) to the D_{IN} and D_{OUT} pins, respectively, thus permitting simultaneous read and write operations.

ARCHITECTURE – Each of the sixteen shift register blocks is implemented using a Serial-Parallel-Serial (SPS) register architecture. In this approach N data bits are sequentially shifted into a "serial" input register. When full, the entire N-bit word is shifted in parallel into N "parallel" registers of M bits in length, as illustrated in Figure 1. At the other end of this parallel register structure, bits are loaded in parallel into an N-bit serial output register. Bits in this register are then shifted out toward the sense amplifier at the output and are automatically recirculated back to the input serial register unless a WRITE operation is specified.

The primary advantages of this type of architecture include very high density, low power, and low clock capacitance. These features all result from the fact that in the SPS architecture the parallel registers which encompass most of the total storage capacity within each block are shifted at a considerably slower rate (f_{IN}/N) than the clock rate of the input or output serial registers (f_{IN}).

In actuality, each 4096-bit block of the F464 is implemented using an "interlaced" SPS structure in which each bit of the input serial register services two parallel registers rather than just one. The same is true for the output serial register. In addition, "electrode-per-bit" design techniques are used to reduce the effective cell size by minimizing the number of electrodes used to store each bit of information. These techniques obviously enhance the memory density considerably. The dimensions of the F464's interlaced SPS structure are 32-bit input and output serial registers and 64 parallel registers, each 63 bits in length. See Figure 2. These dimensions were chosen in order to optimize the power/density/latency tradeoffs inherent in the CCD memory approach.

CLOCKS – The F464 requires four MOS level clocks: two high frequency (1 to 5 MHz) serial clocks and two low frequency transfer clocks. The serial clocks, ϕ_1 and ϕ_2, control the movement of data within the input and output serial registers of each 4096-bit block and have a frequency equal to the data rate. The transfer clock ϕ_{T1} is used to transfer data from the input serial register to the parallel registers while the transfer clock ϕ_{T2} is used to transfer data from the parallel registers to the output serial register of each block. The data present in the parallel registers is shifted by internally generated ripple clocks. This ripple clock technique allows a high bit-packing density approaching one electrode per bit.

To achieve proper transfer phasing, the two transfer clocks are asymetrical about a 32-cycle interval (31.5 and 32.5 cycles) but symmetrical about a 64-cycle interval. The phasing between these transfer clocks alternates in order to achieve correct bit storage in each block. When ϕ_{T1} occurs during ϕ_1 time, ϕ_{T2} occurs during ϕ_2 time 1.5 cycles prior to ϕ_{T1}. When ϕ_{T1} occurs during ϕ_2 time, ϕ_{T2} occurs during ϕ_1 time 2.5 cycles prior to ϕ_{T1}. Figure 3 illustrates the clock phase relationships.

The clocking operation may be momentarily halted for as long as 15 μs once each interval of 64 or more clock cycles provided that the clock frequency is at least 2.0 MHz or higher. During this "halt time" it is recommended that all clock signals be in the LOW state in order to limit power dissipation.

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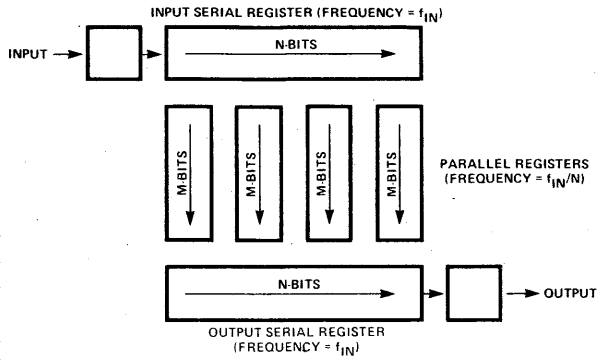


Fig. 1 SIMPLIFIED SPS EXAMPLE WITH N = 4

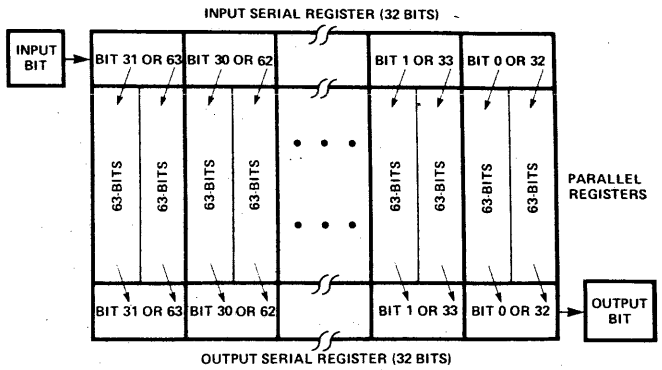
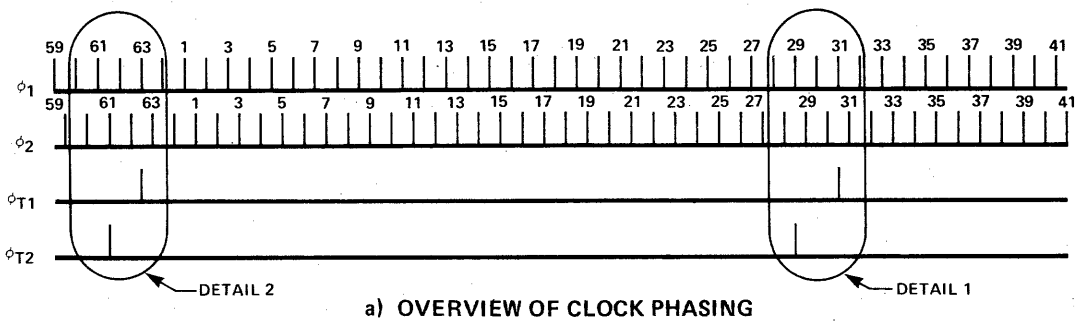
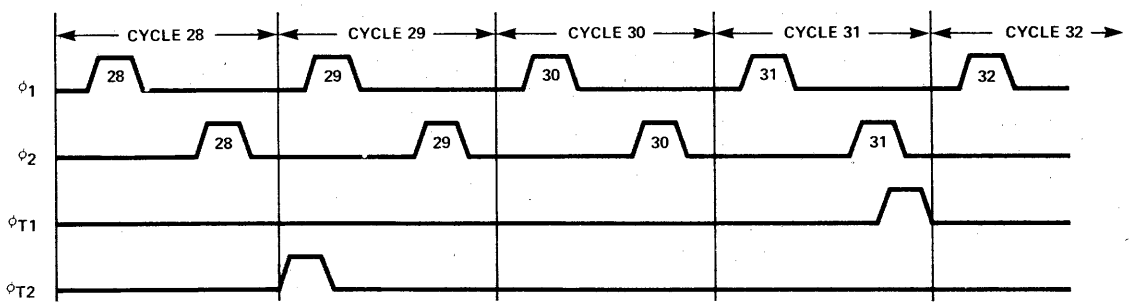


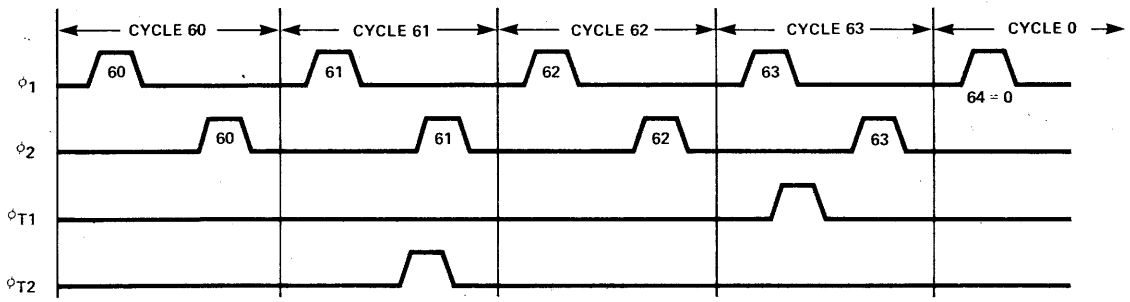
Fig. 2 INTERLACED SPS ARCHITECTURE



a) OVERVIEW OF CLOCK PHASING



b) DETAIL 1



c) DETAIL 2

Fig. 3 F464 CLOCK RELATIONSHIPS

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CONTROLS

In addition to the four Address inputs (A_0 through A_3), other TTL level control signals available on the F464 include Write Enable ($\overline{WE}$) and Chip Select (CS). The CS input, along with the address information, is presented during ϕ_1 HIGH time and dynamically latched with the trailing edge of ϕ_1 which simultaneously disables both the address and CS buffers. This action prevents changes that occur on the external pins from entering the internal circuitry when ϕ_1 is LOW. The $\overline{WE}$ control signal determines whether new data from the D_{IN} pin, or recirculated output data, is presented to the input of the addressed block. The non-addressed blocks are automatically recirculated.

MODES OF OPERATION

STANDBY (Recirculate-only cycle)

In Standby mode (CS LOW), the contents of all 16 blocks are recirculated automatically, and the device disregards the $\overline{WE}$, Address, and D_{IN} inputs. The output latch goes into the high impedance state after the trailing edge of the ϕ_1 clock. Minimum power dissipation results when the device is operated in the recirculate mode with minimum ϕ_1 and ϕ_2 pulse widths at the lowest allowed frequency.

READ-RECIRCULATE MODE

In this mode of operation ($\overline{WE}$ HIGH and CS HIGH) the data from the selected block is presented to the output buffer immediately following the leading edge of ϕ_2 and appears at the output, D_{OUT}, after a delay equal to the access time t_{ACC}. Thus, the access time is referenced from the leading edge of the ϕ_2 pulse and is independent of the duration of ϕ_2. The output data is latched and remains valid at the D_{OUT} pin until the end of the ϕ_1 clock pulse in the next cycle. The data present in all 16 blocks automatically recirculates from the output back to the input regardless of the address inputs, provided that $\overline{WE}$ remains inactive throughout the cycle.

READ AND WRITE MODE

In the Read and Write mode ($\overline{WE}$ LOW and CS HIGH), the output data from the selected block is available at the output pin as in the read-recirculate mode; however, the recirculate path of that particular block is disabled. Input data present at the D_{IN} pin during ϕ_2 is written into the selected block by the falling edge of ϕ_2, while the other 15 blocks automatically recirculate their contents. This form of an "early-write" cycle ($\overline{WE}$ LOW prior to the falling edge of ϕ_1) requires that both $\overline{WE}$ and D_{IN} have set-up times with respect to the trailing edge of ϕ_1. In fact, for successive write operations handled in this mode, $\overline{WE}$ may be held LOW continuously without returning it to the HIGH state between cycles. A "delayed-write" cycle ($\overline{WE}$ goes LOW after the trailing edge of the ϕ_1 clock pulse) is also possible and is discussed in the next paragraph as a subset of the RMW operating mode.

READ-MODIFY-WRITE MODE

The Read-Modify-Write mode (CS HIGH, $\overline{WE}$ HIGH goes LOW) is simplified by the fact that the F464 is always in the read mode whenever it is selected (CS HIGH). Since the access time is referenced to the leading edge of ϕ_2 and the setup times of $\overline{WE}$ and D_{IN} are referenced to the trailing edge of ϕ_2, this mode of operation requires an extended ϕ_2 HIGH time in order to provide the required modify time. This "stretched" ϕ_2 HIGH time may be determined by the following relationship:

$$t_{\phi 2H} = t_{ACC} + t_{MOD} + t_{DS} + t_{WCL} + t_T$$

The modify time, t_{MOD}, is determined by the user and is dependent on the delays of the external logic used to modify the output data. The Read-Modify-Write (RMW) cycle time then, is given by:

$$t_{CYC} = t_{\phi 1H} + t_{UL1} + t_{\phi 2H} + t_{UL2} + 4t_{TC}$$

where $t_{\phi 2H}$ is the new "stretched" version of the ϕ_2 clock pulse.

If no modification of output data is required, then this operating mode reduces to a "delayed-write" mode in which D_{IN} and $\overline{WE}$ may occur after the ϕ_1 clock pulse.

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MEMORY START-UP

When the F464 is initially powered up, the V_{BB} supply (i.e., the –5 volt supply) should be applied to the memory before and removed after the other supplies. This action results in greater protection against accidental violation of the voltage limits specified in the Absolute Maximum Ratings section and, in general, enhances the long term reliability of the memory.

In order to clear the memory of extraneous charge following power-up or after a clock stoppage of greater than 15 μs, the F464 must be clocked through a minimum of 20,000 clock cycles of any type before a valid memory cycle should be attempted.

ABSOLUTE MAXIMUM RATINGS

Voltage of any pin relative to V_{BB} ($V_{SS} - V_{BB} \geqslant 4.5$ V)	–0.5 V to +20 V
Operating Temperature (Ambient)	0°C to 55°C
Storage Temperature (Ambient)	–55°C to 150°C
Power Dissipation	1 W

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC REQUIREMENTS: $T_A = 0°C$ to $55°C$ (See Note 1)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	11.4	12	12.6	V	
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	
V_{SS}	Supply Voltage	0	0	0	V	1
V_{BB}	Supply Voltage	–5.5	–5.0	–4.5	V	
V_{IHC}	Input HIGH Clock Voltage	$V_{DD}-1$		$V_{DD}+1$	V	
V_{ILC}	Input LOW Clock Voltage	–0.5		0.8	V	2
$\lvert\Delta V_{ILC}\rvert$	Voltage Differential Between Any Two Clock LOWS	0		0.8	V	2
V_{IH}	Input HIGH Voltage, all inputs except clocks	2.4		V_{CC}	V	
V_{IL}	Input LOW Voltage, all inputs except clocks	–0.5		0.8	V	

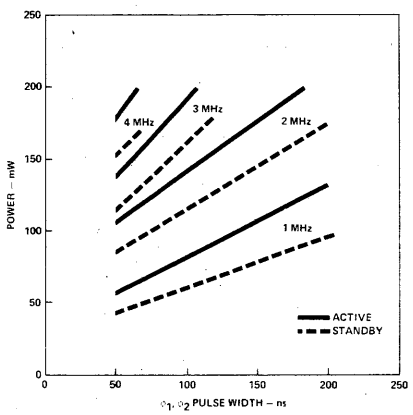


Fig. 4 TYPICAL POWER DEPENDENCE ON CLOCK PULSE WIDTH

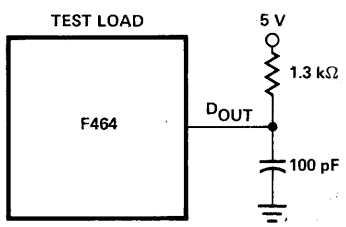


Fig. 5 TEST LOAD

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DC ELECTRICAL CHARACTERISTICS: Over Full Range of Voltage and Temperature (See Note 1)

SYMBOL	PARAMETER			MIN	TYP	MAX	UNITS	NOTES
I_{DD}	Average V_{DD} Current	Active	f_{min}		5	8	mA	3, 10
			f_{max}		15	25	mA	
		Standby	f_{min}		3	5	mA	
			f_{max}		12	19	mA	
I_{CC}	Average V_{CC} Current	Active	f_{min}		1.5	2.5	mA	3, 10
			f_{max}		2.5	4	mA	
		Standby	f_{min}		0.3	0.5	mA	
			f_{max}		1.2	2	mA	
I_{BB}	Average V_{BB} Current					100	μA	4
V_{OH}	Output HIGH Voltage			2.8			V	5
V_{OL}	Output LOW Voltage					0.4	V	6
I_{IN}	Input Leakage Current (any input)			−10		10	μA	7
I_{OUT}	Output Leakage Current			−10		10	μA	8
C_{IN1}	Input Capacitance, ϕ_1 and ϕ_2				100		pF	9
C_{IN2}	Input Capacitance, ϕ_{T1} and ϕ_{T2}				30		pF	9
C_{IN3}	Input Capacitance, $A_0 - A_3$, CS, $\overline{WE}$, and D_{IN}				5		pF	9
C_{OUT}	Output Capacitance, D_{OUT}				7		pF	9

RECOMMENDED CLOCKING CONDITIONS: Over Full Range of Voltage and Temperature (See Note 11)

IEEE SYMBOL	SYMBOL	PARAMETER	F464-2		F464-3		F464-4		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
TE1HE1L	$t_{\phi 1H}$	ϕ_1 HIGH Pulse Width	50	200	60	200	100	200	ns	10
TE2HE2L	$t_{\phi 2H}$	ϕ_2 HIGH Pulse Width	50	300	60	300	100	300	ns	10
TE1LE2H	t_{UL1}	ϕ_1 to ϕ_2 Underlap Time	30		45		100		ns	
TE2LE1H	t_{UL2}	ϕ_2 to ϕ_1 Underlap Time	30		45		100		ns	
TTHEL	t_{OV1}	ϕ_{T1} and (ϕ_1 or ϕ_2) Overlap Time	30		30		50		ns	
TEHTL	t_{OV2}	ϕ_{T2} and (ϕ_1 or ϕ_2) Overlap Time	20		30		50		ns	
TEHTH	t_{T1D}	(ϕ_1 or ϕ_2) to ϕ_{T1} Delay Time	0		0		0		ns	
TTLEH	t_{T1S}	ϕ_{T1} to (ϕ_1 or ϕ_2) Setup Time	0		0		0		ns	
TELTH	t_{T2D}	(ϕ_1 or ϕ_2) to ϕ_{T2} Delay Time	0		0		0		ns	
TTLEL	t_{T2S}	ϕ_{T2} to (ϕ_1 or ϕ_2) Setup Time	5		5		5		ns	
TELTL	t_{T1HD}	ϕ_{T1} Hold Time	20		30		50		ns	
–	t_T	Transition Time (Except Clocks)	3	50	3	50	3	50	ns	11
–	t_{TC}	Clock Transition Time (Rise and Fall)	10	50	10	50	10	50	ns	11,12
–	f	Operating Frequency	1.0	5.0	1.0	4.0	1.0	2.0	MHz	12
–	t_{HALT}	Halt Time @ 2 MHz		15		15		15	μs	17

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RECOMMENDED AC OPERATING CONDITIONS: Over Full Range of Voltage and Temperature

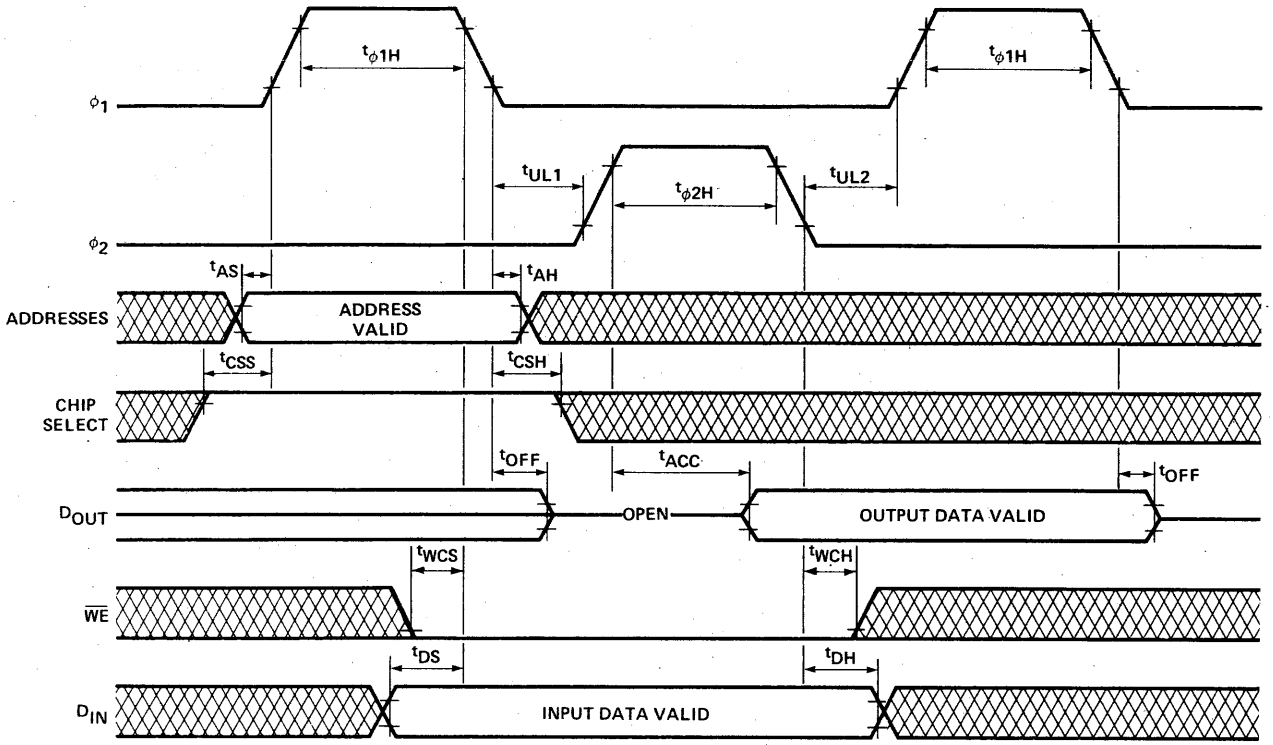
IEEE SYMBOL	SYMBOL	PARAMETER	F464-2		F464-3		F464-4		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
TAVEH	t_{AS}	Address Setup Time	5		5		5		ns	
TELAX	t_{AH}	Address Hold Time	5		5		5		ns	
TSVEH	t_{CSS}	Chip Select Setup Time	5		5		5		ns	
TELSX	t_{CSH}	Chip Select Hold Time	5		5		5		ns	
TWHEL	t_{RCS}	Read-Recirculate Command Setup Time	5		5		5		ns	13
TELWX	t_{RCH}	Read-Recirculate Command Hold Time	25		25		25		ns	13
TWLEL	t_{WCS}	Write Command Setup Time	0		0		0		ns	
TELWX	t_{WCH}	Write Command Hold Time	25		25		25		ns	
TWLEL	t_{WCL}	Write Command Lead Time (RMW Only)	60		60		60		ns	
TDVWL	t_{DS}	Input Data Setup Time	0		0		0		ns	14
TELDX	t_{DH}	Input Data Hold Time	25		25		25		ns	
TELQZ	t_{OFF}	Output Buffer Turn-Off Delay	0	50	0	50	0	50	ns	15
TEHQV	t_{ACC}	Output Data Access Time		50		60		70	ns	16

NOTES:

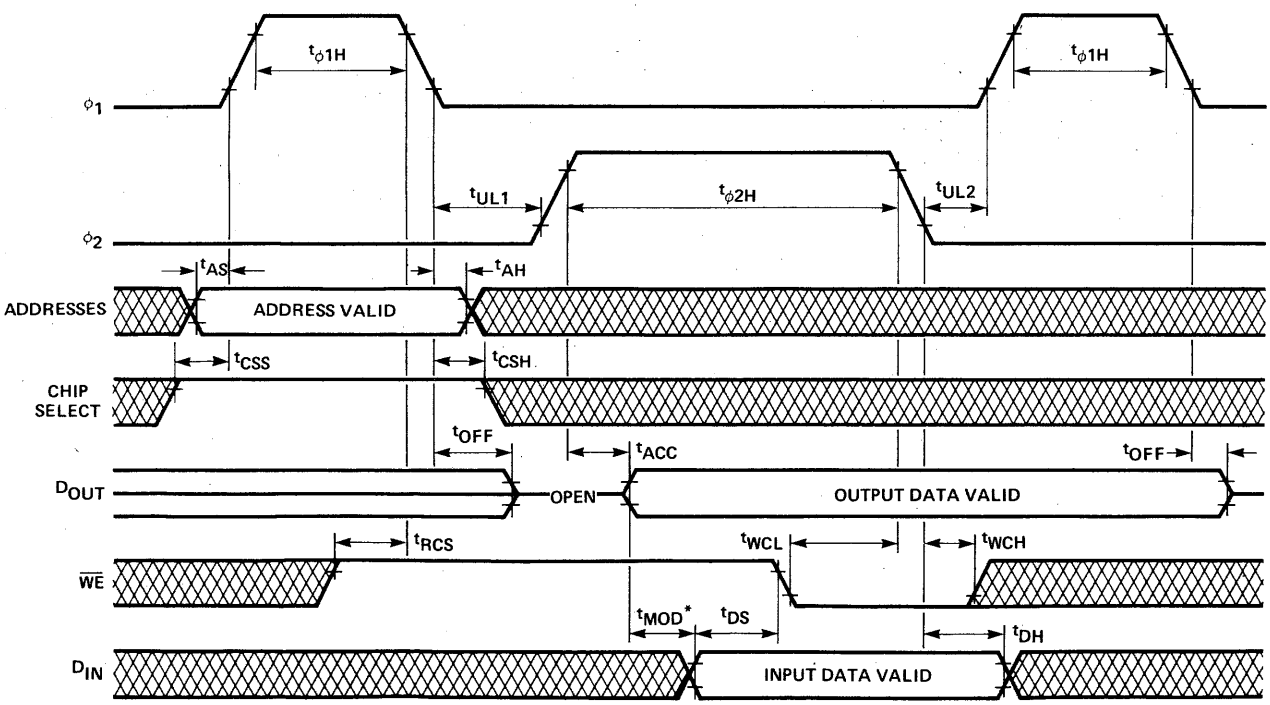
1. All voltages are measured with respect to V_{SS}.
2. The differential voltage between a LOW for any clock input and a LOW for any other clock input should not exceed 0.8 V.
3. Current levels at both minimum and maximum frequencies are specified for minimum ϕ_1 and ϕ_2 clock pulse widths. See Figure 4.
4. Measured at maximum frequency and $V_{BB} = -5.5$ V.
5. Measured with $I_{OUT} = -2.5$ mA.
6. Measured with $I_{OUT} = 3.5$ mA.
7. Input leakage current is measured with $V_{IN} = V_{DD}$ for clock inputs and $V_{IN} = V_{CC}$ for all other inputs.
8. Leakage current at the D_{OUT} pin is measured for both V_{OUT} equal to V_{CC} and V_{SS} when the output buffer is in the high impedance state.
9. Effective capacitance is calculated from the equation $C = I\ \Delta t/\Delta V$ with $\Delta V = 12$ V for clock inputs and with $\Delta V = 3$ V for TTL pins while the device is active. Measured parameters are current and time.
10. Maximum clock pulse widths are specified in order to limit power dissipation. See Figure 4 showing the relationship between power and clock pulse width.
11. Reference levels used for timing measurements are V_{IHC} (min) and V_{ILC} (max) for clock inputs and V_{IH} (min) and V_{IL} (max) for all other inputs. Transition times for both rise and fall are measured between these reference points.
12. Minimum and maximum frequency values assume clock transition times of 10 ns.
13. The Read-Recirculate command is performed by keeping $\overline{WE}$ in the inactive state (i.e. HIGH) for the prescribed set-up and hold times.
14. t_{DS} references D_{IN} to the trailing edge of ϕ_1 in a Read-(early) Write cycle. However, in a Read-Modify Write (i.e. delayed write) cycle, t_{DS} references D_{IN} to the negative-going edge of $\overline{WE}$.
15. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
16. Measured with a load equivalent to two TTL loads and 100 pF. See Fig. 5.
17. The clocking operation maybe momentarily halted for as long as 15 μs once each interval of 64 or more clock cycles provided that the clock frequency is at least 2.0 MHz or higher. During this "halt time" it is recommended that all clock signals be in the LOW state in order to limit power dissipation.

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READ-WRITE CYCLE



READ-MODIFY-WRITE CYCLE



DON'T CARE CONDITION

*$t_{MOD} = t_{\phi 2H} - t_{ACC} - t_{DS} - t_{WCL} - t_T$

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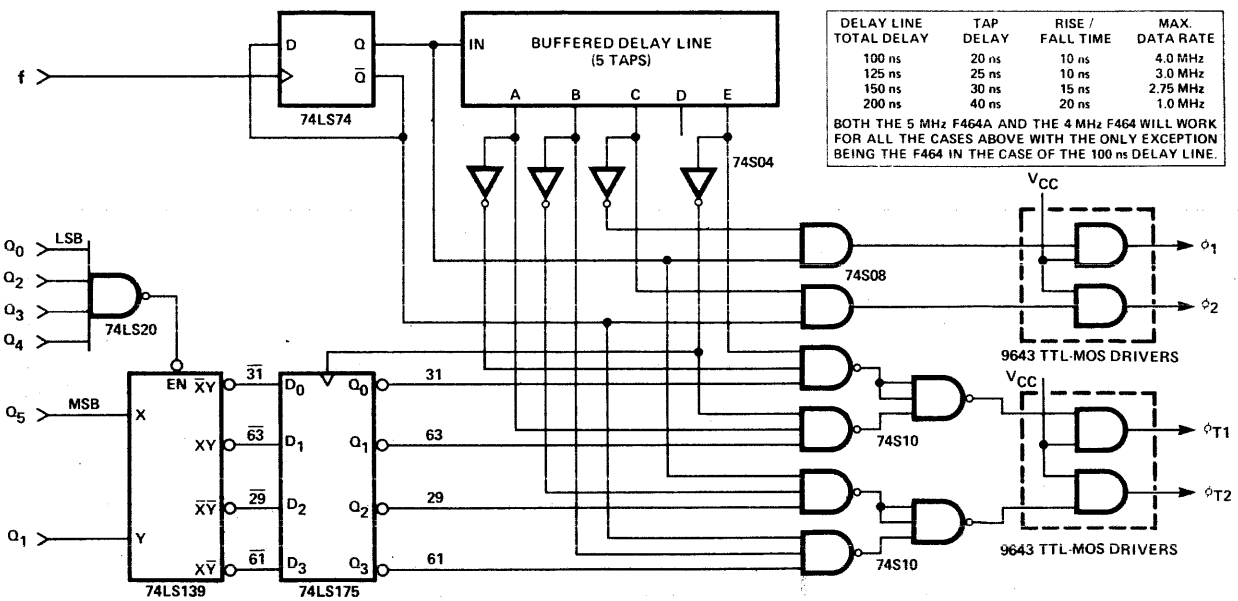
CLOCK GENERATION CIRCUIT –

The circuit shown below may be used to generate the four MOS-level clocks required of the F464 from a single master clock. In this circuit, the master clock frequency f, must be twice the desired data rate at the F464 output pin. Since the input clock frequency is "squared-up" with a divide-by-two flip-flop, the duty cycle of this clock is non-critical. A pulse edge at the input of the buffered delay line produces a sequence of delayed pulse edges from the A, B, C, D and E output taps. These delayed pulse edges are ANDed together to produce the required ϕ_1 and ϕ_2 clocks as well as the ϕ_{T1} and ϕ_{T2} transfer clocks. Since the transfer clocks occur in a symmetrical fashion every 64 clock cycles, a 6-bit, modulo 64 counter is required. The outputs of this 6-bit counter are decoded to enable the appropriate transfer clock gates at counts of 29, 31, 61 and 63. Thus, ϕ_{T1} is passed along to the clock drivers only during cycles 31 and 63, while ϕ_{T2} is gated through only during cycles 29 and 61. These four counts are easily decoded with only a 2-to-4 decoder and one 4-input NAND gate. The 6 bits of the modulo 64 counter comprise the 6 low order bits of the 12-bit, modulo 4096 loop counter. This counter is required to define address locations within each 4K block and will, in most cases, be already present in the system.

One major advantage of using a delay line is that since the clock pulses are generated from delayed edges, the pulse width in all cases is fixed and does not vary as a function of the input master frequency f. Thus minimum pulse widths are always generated regardless of cycle and data rates. This translates directly into lower power dissipation since I_{DD} is a function of clock pulse width.

The maximum clock rates for which this circuit will operate properly depends on the clock transition times (both rise and fall) at the output of the TTL-to-MOS drivers and, the delay between adjacent taps on the delay line. The maximum data rates possible for this circuit are given in the table. Faster and/or more efficient clock generation circuits may be realized by using different types of delay lines (e.g. more taps or unequal tap delays).

SERIAL AND TRANSFER CLOCK GENERATION CIRCUIT



DELAY LINE TOTAL DELAY	TAP DELAY	RISE / FALL TIME	MAX. DATA RATE
100 ns	20 ns	10 ns	4.0 MHz
125 ns	25 ns	10 ns	3.0 MHz
150 ns	30 ns	15 ns	2.75 MHz
200 ns	40 ns	20 ns	1.0 MHz

BOTH THE 5 MHz F464A AND THE 4 MHz F464 WILL WORK FOR ALL THE CASES ABOVE WITH THE ONLY EXCEPTION BEING THE F464 IN THE CASE OF THE 100 ns DELAY LINE.

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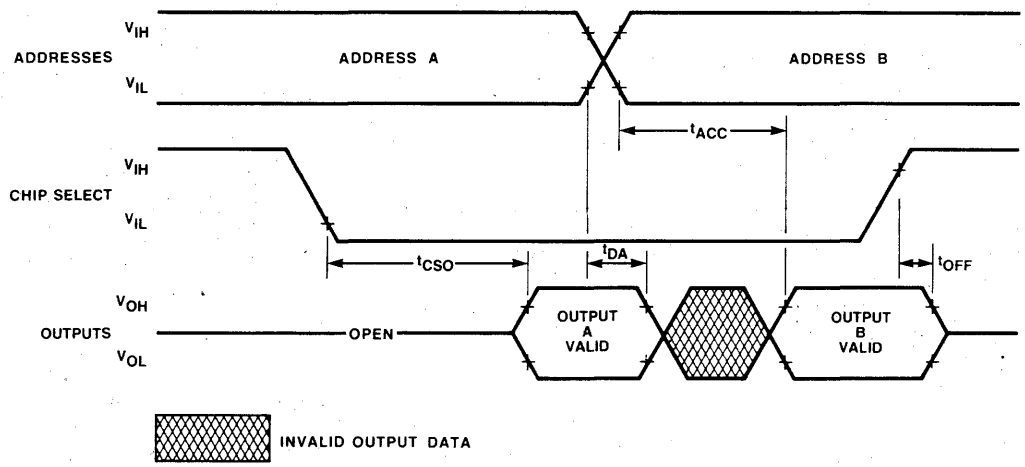
READ MODE: AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER (See Note 8)	F2708-1		F2708		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{ACC}	Address to Output Delay Time		350		450	ns	
t_{CSO}	Chip Select to Output Delay Time		120		120	ns	
t_{OFF}	Chip Deselect to Output High Impedance		120		120	ns	
t_{DA}	Data Valid After Address Time	0		0		ns	

NOTES:

1. All voltage levels are referenced to V_{SS} = 0 V.
2. Worst case supply currents occur when all inputs are HIGH (including $\overline{CS}$/WE = 5.0 V) and the ambient temperature is T_A = 0°C.
3. Measured both with V_{IN} = 5.25 V and V_{IN} = V_{IL} (min) = V_{SS}.
4. Measured both with V_{OUT} = 5.25 V and $\overline{CS}$/WE = 5.0 V.
5. The total power dissipation of the 2708 is specified at 800 mW. It is not calculable by summing the various currents (I_{DD}, I_{CC} and I_{BB}) multiplied by their respective voltages, since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC} and I_{BB} currents should be used to determine power supply capacity only.
6. Measured with V_{IN} = 0 V, T_A = 25°C and f = 1.0 MHz.
7. Measured with V_{OUT} = 0 V, T_A = 25°C and f = 1.0 MHz.
8. Timing parameters are measured with input logic levels of V_{IL} (max) = 0.65 V and V_{IH} (min) = 3.0 V. Timing measurement reference levels are 0.8 V and 2.8 V for inputs and 0.8 V and 2.4 V for outputs. An output load of 1 TTL gate plus 100 pF is assumed.

READ MODE TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every memory cell in the F2708 is in the logic "1" state (as indicated by a HIGH level at the data outputs). An 8-bit byte of data is entered into the memory by programming logic "0"s into the appropriate cell locations at some given address. Word locations in the memory are addressed in the same way as in READ operations. Once a cell is programmed to a logic "0", it can only be altered through ultraviolet light erasure.

In order to program the F2708, the $\overline{CS}$/WE input must first be set to 12 V. Data to be programmed is entered in 8-bit bytes through the output data terminals (Q_0 through Q_7). Input logic levels for the data lines, addresses, and supply voltages are the same as in a READ operation.

Programming is accomplished by executing a number (N) of passes through a programming loop, each of which involves sequencing through all 1024 locations in the address space. In each pass through the loop, a single, high voltage (26 V) pulse is applied to the PRGM input, once at each address. Logic "0"s applied to the data pins (Q_0 through Q_7) are written into the proper bit positions at the location specified by the address inputs (A_0 through A_7). There must be N successive passes through the programming loop in order to guarantee reliable programming of information. The required number of loops (N) is a function of the pulse width (t_{PW}) of the high voltage programming pulse applied to the PRGM input. Total programming time is given by the relationship:

$$t_{TOTAL} = N \times t_{PW} \geq 100 \text{ ms} \quad (1)$$

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The allowed range of pulse widths is from 0.1 ms to 1.0 ms. This implies that the minimum value of N must be in the range of 100 to 1000. WARNING: Applying more than one programming pulse in succession to the same address is not permitted since it will result in damage to the device. At the end of a program sequence, the $\overline{CS}$/WE falling edge transition must occur before the first address transition when changing from the PROGRAM mode to the READ mode. The PRGM pin should be pulled down to approximately V_{SS} (i.e., ground) with an low impedance device since this pin sources several milliamps of current when $\overline{CS}$/WE is at 12 V and the PRGM pin is LOW.

PROGRAMMING EXAMPLES

The programming relationship in Equation 1 above should always be used in determining values of t_{PW} and N.

Example 1 The full capacity of 1024 bytes could be programmed using 0.2 ms programming pulse widths. In this case, the minimum number of passes through the programming loop would be

$$N = \frac{t_{TOTAL}}{t_{PW}} = \frac{100\ ms}{0.2\ ms} = 500\ loops. \quad (2)$$

Each of the 500 programming loops must sequence through address locations 0 through 1023.

Example 2 Word locations 0 to 200 and 300 to 700 are to be programmed. All other bits are "don't cares". The programmed pulses are 0.5 ms wide. Thus, the minimum number of program loops is

$$N = \frac{100\ ms}{0.5\ ms} = 200\ loops. \quad (3)$$

The data entered into the "don't care" locations should consist of all logic "1"s. Even though portions of the address space are not used (or "don't cares"), the programming loop should still sequence through all 1024 addresses on each pass.

Example 3 Extending the case of Example 2, the F2708 is now to be updated to include new data at locations 850 to 880 which previously were programmed as "don't cares"; in this case, logic "1"s. The minimum number or programming loops is the same as in Example 2, N = 200 loops. Address locations 0 to 200 and 300 to 700 must be reprogrammed with their original data pattern. The remaining unused addresses should again be programmed as logic "1"s.

ERASING INSTRUCTIONS

The contents of the F2708 EPROM can be erased by exposure to high intensity shortwave ultraviolet (UV) light with a wavelength of 2537 Angstroms (Å). This can be accomplished with ultraviolet light EPROM erasure devices which are available from several U.S. manufacturers. These erasure devices contain a UV light source which is usually placed approximately one or two inches from the EPROM such that the transparent window on top of the device is illuminated. The minimum required integrated dose (intensity x exposure time) of UV light energy incident on the window of the device in order to reliably insure complete erasure is 12.5 Watt-sec/cm^2. The UV erasure unit should be periodically calibrated if minimum exposure times are to be used. (Minimum exposure times range from 10 to 45 minutes, depending on model type and age of UV lamp). If longer exposure times are possible, variations in the output light intensity of the UV light source are not critical.

PROGRAM MODE DC ELECTRICAL REQUIREMENTS

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage		11.4	12.0	12.6	V	
V_{CC}	Supply Voltage		4.75	5.0	5.25	V	
V_{SS}	Supply Voltage		0	0	0	V	1
V_{BB}	Supply Voltage		−5.25	−5.0	−4.75	V	
V_{IHP}	Input HIGH Voltage During Programming	Address and Data	3.0	–	V_{CC}+1.0	V	
		$\overline{CS}$/WE Input	11.4	12.0	12.6	V	
		PRGM Input	25	–	27	V	2
V_{IL}	Input LOW Voltage	PRGM Input	V_{SS}	–	1.0	V	2
		All Other Inputs	V_{SS}		0.65	V	

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PROGRAM MODE DC ELECTRICAL CHARACTERISTICS

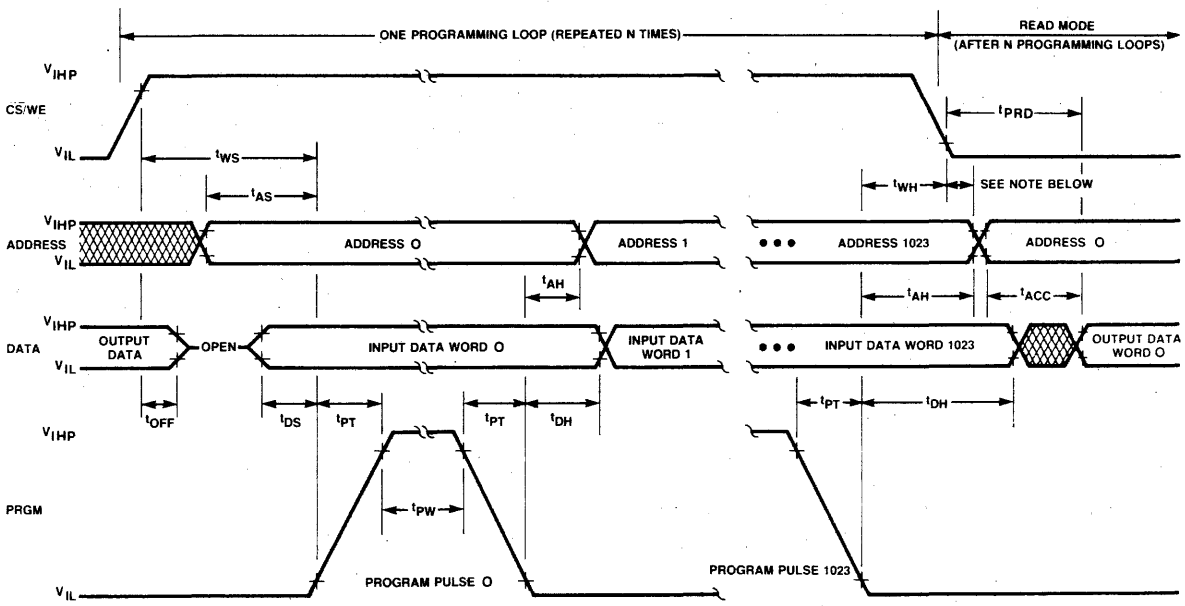
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	NOTES
I_{DD}	Average V_{DD} Current			50	65	mA	3
I_{CC}	Average V_{CC} Current			6	10	mA	3
I_{BB}	Average V_{BB} Current			30	45	μA	3
I_{IN}	Input Leakage Current, Addresses and $\overline{CS}$/WE		−10		10	μA	4
I_{PRGM}	PRGM Input Current	HIGH			20	mA	
		LOW			3.0	mA	5

NOTES:
1. All voltage levels are referenced to V_{SS} = 0 V.
2. The voltage differential between V_{IH} and V_{IL} at the PRGM input pin should be greater than or equal to 25 V.
3. Worst case supply currents occur when all inputs are HIGH (including $\overline{CS}$/WE = 5.0 V) and the ambient temperature is T_A = 0°C.
4. Measured both with V_{IN} = 5.25 V and V_{IN} = V_{IL} (min) = V_{SS}.
5. This is a current sourced by the PRGM pin when it is in the LOW state and when $\overline{CS}$/WE = 12 V.

PROGRAM MODE: AC ELECTRICAL REQUIREMENTS AND CHARACTERISTICS

SYMBOL	PARAMETER		MIN	MAX	UNITS	NOTES
t_{AS}	Address Setup Time		10	–	μs	
t_{AH}	Address Hold Time		1.0	–	μs	
t_{WS}	Write Enable Setup Time		10	–	μs	
t_{WH}	Write Enable Hold Time		0.5	–	μs	
t_{DS}	Data Setup Time		10	–	μs	
t_{DH}	Data Hold Time		1.0	–	μs	
t_{PW}	Program Pulse Width		0.1	1.0	ms	
t_{PT}	Program Pulse Transition Time	Rise	0.5	2.0	μs	
		Fall	0.5	2.0	μs	
t_{PRD}	Program to Read Delay		–	10	μs	
t_{OFF}	Output Buffer Turn-off Delay		0	120	ns	

PROGRAM MODE TIMING DIAGRAM



NOTE: The falling edge of $\overline{CS}$/WE must occur after the falling edge of the program pulse and before the address transition.

DON'T CARE INPUT CONDITION OR INVALID OUTPUT DATA.

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3843 USART

UNIVERSAL SYNCHRONOUS OR ASYNCHRONOUS RECEIVER AND TRANSMITTER

FAIRCHILD ISOPLANAR SILICON GATE NMOS

GENERAL DESCRIPTION—The 3843 is a programmable, full duplex Universal Synchronous or Asynchronous Receiver and Transmitter (USART) designed for use in data communications systems. This device provides the interface between the bus-oriented format of the controller and the serial format of the peripheral unit. The programming inputs of the USART determine the transmission mode, character length, framing format, parity mode and baud rate.

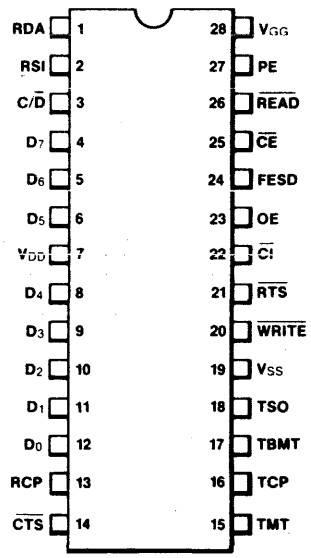
The 3843 is manufactured with the n-channel Isoplanar silicon gate process, and is available in both plastic and ceramic 28-pin dual in line package as well as in commercial and military temperature ranges.

- 5, 6, 7, or 8-BIT SELECTABLE CHARACTER LENGTH
- ODD OR EVEN PARITY GENERATION AND CHECKING
- SELECTABLE NUMBER OF STOP BITS (1, 1½, 2) IN ASYNCHRONOUS MODE
- SEPARATE RECEIVER AND TRANSMITTER CLOCKS
- SELECTABLE CLOCK RATES (16x, 32x, or 64x BAUD RATES)
- STATIC OPERATION—NO MINIMUM FREQUENCY
- MAXIMUM BAUD RATES: (3843-1DC)

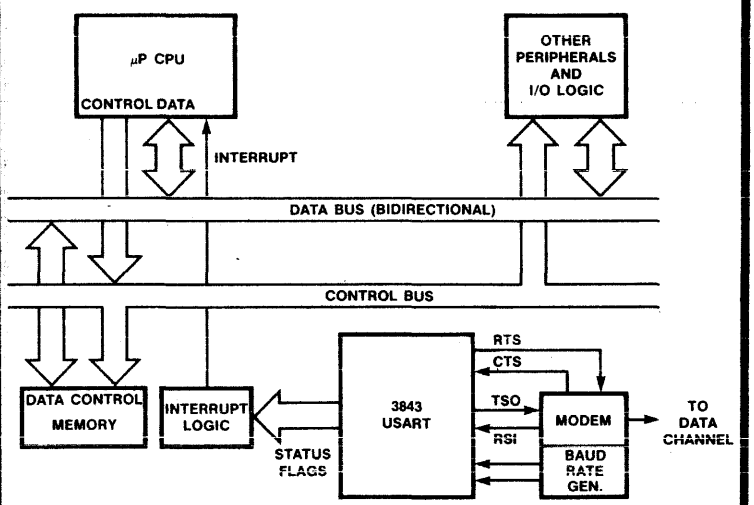
1x CLOCK (SYNC MODE)	-	320K BAUD
16x CLOCK (ASYNC MODE)	-	20K BAUD
32x CLOCK (ASYNC MODE)	-	10K BAUD
64x CLOCK (ASYNC MODE)	-	5K BAUD

- ERROR FLAGS: OVERRUN, PARITY, AND FRAMING ERRORS
- HARDWARE AND SOFTWARE STATUS FLAGS FOR BOTH RECEIVER AND TRANSMITTER STATUS
- DOUBLE BUFFERED, FULL DUPLEX OPERATION
- EXTERNAL OR INTERNAL (ONE OR TWO SYNC WORDS) SYNCHRONIZATION
- TTL COMPATIBLE INPUTS AND OUTPUTS
- 3-STATE DATA BUS WITH OR-TIE CAPABILITY

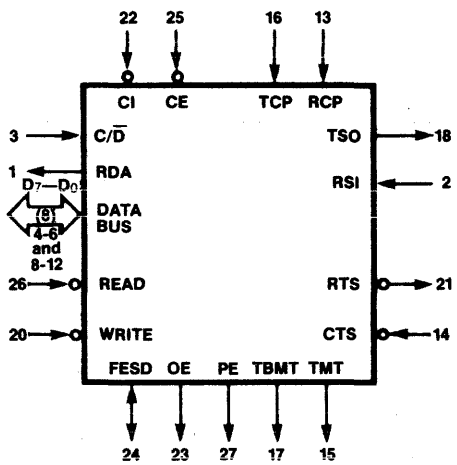
CONNECTION DIAGRAM
DIP (TOP VIEW)



SYSTEM DIAGRAM



LOGIC SYMBOL



VCC (+5V) = Pin 28
VDD (+12V) = Pin 7
VSS (GND) = Pin 19

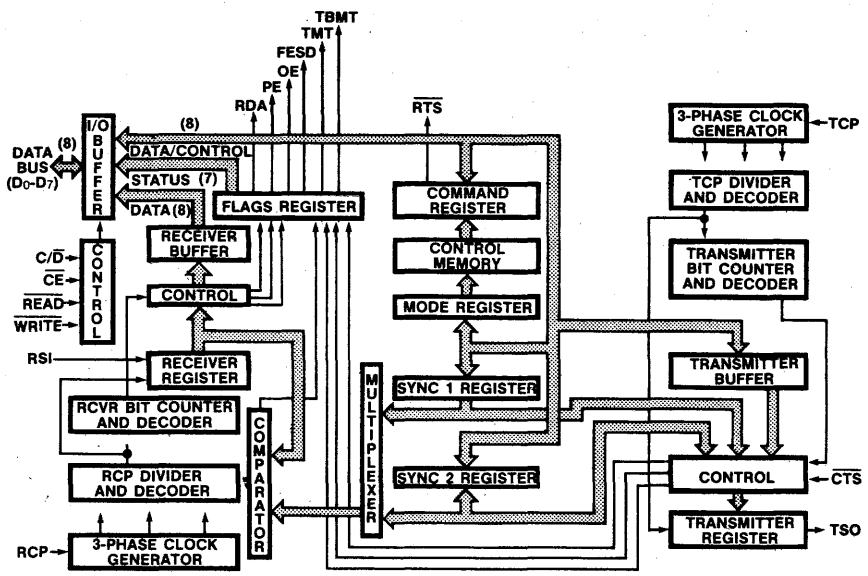
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464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA, 94042 (415) 962-5011/TWX 910-379-6435

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BLOCK DIAGRAM



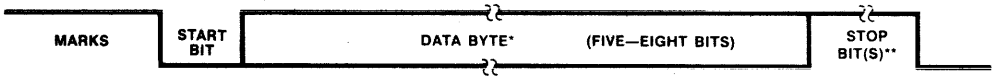
FUNCTIONAL DESCRIPTION

The 3843 USART is a programmable interface device designed for use in CPU-controlled digital data communications applications where parallel-to-serial and serial-to-parallel conversions of digital data are required. In a typical communications system, the USART converts output data from the processor which is formatted in a parallel fashion, into serially formatted data for transmission over a data channel. At the same time, it also converts incoming serial data into parallel formatted bytes of data for use by the processor. The 3843 also inserts bits (async mode) or characters (sync mode) into the serial data stream as dictated by the particular transmission format employed, and then strips them from the data stream during reception. Thus, the USART is a transparent interface which the CPU recognizes simply as an I/O port for bytes of data: the USART handling the reformatting and transmission/reception of data thereby freeing the CPU from this time consuming task. The operational mode of the USART is definable by the CPU software through a sequence of control instructions which completely specify USART functions. (See the Programming Section for details). One of the items specified in the format type which is either synchronous or asynchronous. The following sections provide a general discussion of the 3843's operating modes.

Transmitter Operation: Asynchronous Mode

To transmit data in the asynchronous operating mode the CPU places a byte of data on the data bus and then inputs it into the USART with a strobe pulse on the $\overline{WRITE}$ pin. If the C/$\overline{D}$ (Control or Data) input is HIGH, then the word is loaded into either the Mode Register, one of the Sync Registers, or the Command Register, depending on the current location in the programming sequence. (See the Programming Section). If the C/$\overline{D}$ input is LOW, then the information on the data bus will be loaded into the Transmitter Buffer Register. This register serves as temporary storage for the next data character to be transmitted. The Transmitter Register, on the other hand, contains the data character currently being transmitted. The bits in this register are serially shifted out through the TSO (Transmitter Serial Output) pin as a serial bit stream. When the Transmitter Register become empty, the next word to be transmitted is loaded into this register from the Transmitter Buffer. When this happens, the buffer becomes empty and the TBMT (Transmitter Buffer Empty) status flag is set HIGH. If both the transmitter and the transmitter buffer registers becomes empty then the TMT (Transmitter Empty) status flag is set HIGH. These and other status flags are available as output pins as well as through the status word which can be monitored by the system software.

In the asynchronous format "framing bits are appended to the data character to be transmitted before it is output via the TSO pin. Prior to the sending of actual data bits, a "start-bit" (a logic "0") is inserted before the data to signify the beginning of a character. See Figure 1.



*Variable byte size is defined in the Mode Instruction with unused bits being set to logic "0".

**Either one, one and one half, or two STOP bits as prescribed in the Mode Instruction.

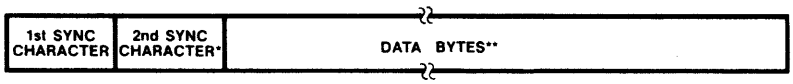
FIG. 1 ASYNCHRONOUS TRANSMISSION/RECEPTION FORMAT

The data character itself may consist of a byte of from five to eight bits in length. This length must be specified by the Mode Instruction prior to transmission. This same instruction also indicates if an optional parity bit should be automatically inserted after the data and whether it should be even or odd. Following the parity bit are the "stop-bits" (logic "1"s) of which there may be one, and one-half, or two. These stop bits indicate the end of the transmitted data character. Each bit is output for an interval of time (referred to as one "bit-time") which is either 16, 32, or 64 clock pulses in length as specified by the Mode Instruction. These clock pulses are input via the TCP (Transmitter Clock Input) pin.

The entire assembly of bits, including START, parity, and STOP bits, is then shifted out through the TSO output as a serial bit stream provided that a logic "1" has been programmed into the TE (Transmitter Enable) bit of the command register. If there is a pause in transmission, the TSO output is forced into the inactive state until the CPU initiates further transmissions. In its inactive state the TSO output is normally HIGH and is said to be in the "marking" state, or sending "marks" continuously.

Transmitter Operation: Synchronous Mode

Transmission of serial data in the synchronous mode is accomplished by transmitting entire blocks of five, six, seven, or eight-bit bytes of data, one after another in a serial data stream, with no framing bits added between bytes. Synchronizing information is supplied with either one or two "sync-characters" which must precede each block of data *(See Figure 2)*.



*The use of an optional second SYNC Character is specified in the Mode Instruction.

**There is no inherent limitation on the number of bytes in the data block.

FIG. 2 SYNCHRONOUS TRANSMISSION/RECEPTION FORMAT

Data presented to the USART from the CPU via the data bus is handled in exactly the same manner as in the previously described asynchronous mode except for the addition of sync-characters between the Mode and Command Instructions. While in the synchronous mode, if the C/D pin is HIGH following the Mode Instruction, then the next word will be interpreted as the first of possibly two sync characters and is loaded into the appropriate register. (See the Block Diagram on page 2). The second sync character (if used) is handled similarly and is loaded into a second sync-word register. These sync characters are output to the TSO pin whenever the transmitter register becomes empty. In this way synchronization is not lost but rather is maintained by the USART automatically transmitting sync words as "sync-fill" characters until the CPU loads a new byte of data. After a Master Reset has been programmed, the TSO output ceases to transmit sync characters and goes to a continuous HIGH state.

Receiver Operation: Asynchronous Mode

Data is received in the async mode from the modem on the RSI (Receiver Serial Input) line. This line, which is normally HIGH, is taken LOW by the reception of a START bit which signals the USART that incoming data is imminent. Through the use of the Mode Instruction, the USART has been programmed to accept a serial data stream with bit times of either 16, 32, or 64 clock periods in length. (Each bit of data lasts for either 16, 32, or 64 pulses of the receiver clock input, RCP). The falling edge of the START bit is used as a reference by an internal clock pulse counter that allows the USART to sample the RSI input at the chronological center or midpoint of each bit time. Incoming bits are reassembled in the Receiver Register where the START, STOP, and parity bits are stripped from the receiver data. The parity bit (if it is used) is recomputed and compared against the received parity bit with the PE (Parity Error) flag being set accordingly. An internal bit counter counts off the expected number of data bits along with a possible parity bit and assumes that any additional bits are stop bits. If any of

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the anticipated number (either one, one and one-half, or two) of STOP bits is detected as a logic "0", then the FE (Framing Error) flag will be set. When the reassembled data character is transferred to the Receiver Buffer Register, the USART then signals the CPU that received data is available for fetching by taking the RDA (Receiver Data Available) line HIGH. The CPU responds by driving the $\overline{READ}$ input LOW which causes the data word to appear on the USART's data bus. Should the CPU fail to read the data word before the next received character is transferred into the receiver buffer, then the previous character is written over by the new character and the OE (Overrun Error) flag is set.

The occurrence of either a parity error, a framing error, or an overrun error does not necessarily preclude other USART operations from continuing. All of the error flags may be reset via the MR bit of the command instruction.

Receiver Operation: Synchronous Mode

Data which is received in the synchronous mode may consist of many bytes of data in one block. If the 3843 is programmed for operation in the internal sync mode, then the incoming block of data must be prefaced with either one or two sync characters. When the RE (Receiver Enable) bit of the command instruction is programmed to a logic "1", the USART begins loading serial bits input via the RSI pin into the Receiver Register. This register is continuously compared on a bit basis to the first sync character until a match occurs. If two sync characters are being used, the next byte is compared to the second sync character and if a match condition occurs, then the USART is properly synchronized for receiving data. If a match condition does not exist for the second sync character, then the USART resumes searching for another occurrence of the first sync character. Once the USART receiver is synchronized, it will remain so until the Receiver Enable bit is reset to a logic "0" or until the EH (Enter Hunt Mode) bit of the command instruction is programmed to a logic "I". The EH command causes the receiver to stop transferring data to the Data Bus until the receiver acquires proper synchronization again.

Reception of data can also be accomplished in the external synchronization mode. This is done by using the FESD pin as an external sync input and taking it HIGH during the second bit of the first non-sync or data word in the block.

PIN DEFINITIONS

The inputs and outputs of the 3843 can be categorized by function since some signals are intended for use between the USART and the CPU, while other signals link the USART to the data channel. Those input and output signals of the 3843 associated with the CPU are:

Chip Initialize	($\overline{CI}$)
Chip Enable	($\overline{CE}$)
Control/Data	($\overline{C/D}$)
Read	($\overline{READ}$)
Write	($\overline{WRITE}$)
Data Bus	($D_0 - D_7$)
Receiver Data Available	(RDA)
Transmitter Buffer Empty	(TBMT)
Transmitter Empty	(TMT)
Framing Error/SYNC Detected	(FESD)
Parity Error	(PE)
Overrun Error	(OE)

The last six of these signals are hardware status signals used by the CPU to monitor USART activity. Since these six signals also appear in the Status Word, they may be read by the software as well as by the hardware. Those input and output signals of the 3843 associated with the channel are:

Request To Send	($\overline{RTS}$)
Clear To Send	($\overline{CTS}$)
Receiver Serial Input	(RSI)
Transmitter Serial Output	(TSO)
Receiver Clock	(RCP)
Transmitter Clock	(TCP)

The functional significance of each of these signals is discussed in the following sections.

Chip Initialize ($\overline{CI}$) – This initialization signal will hold the USART in a reset state as long as it remains LOW. When $\overline{CI}$ goes HIGH, the proper sequence of mode instructions must be executed in order to program the USART for operation (See the programming section).

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Chip Enable ($\overline{CE}$) – This signal enables the USART so that its data bus I/O buffer will respond when a Read or Write Control signal occurs. $\overline{CE}$ does not affect other USART activity when it goes HIGH, but merely prevents any further communication with the CPU and places the data bus I/O buffer in the high impedance state.

Control Data (C/$\overline{D}$) – During a WRITE operation, the 3843 must distinguish command and control information present on its Data Bus from incoming data words. A similar decision must be made during a READ operation to determine if a control status word or a data word should be placed on the Data Bus. In both of these cases, the 3843 distinguishes command, and status information by a HIGH on the C/$\overline{D}$ input pin, while a LOW signifies input/output data.

Read ($\overline{READ}$) – When the CPU supplies a LOW to the 3843's READ input, it causes the USART to output either data (C/$\overline{D}$ = 0) or status (C/$\overline{D}$ = 1) information onto the data bus.

Write ($\overline{WRITE}$) – Instructions or data words placed on the data bus by the CPU are loaded into their respective registers within the 3843 whenever the CPU places a LOW on this input.

Receiver Data Available (RDA) – This signal goes HIGH when there is received data present in the internal receiver register of the 3843 and is used to signal the CPU that it may read the data word from the USART.

Data Bus (D_0 — D_7) – The data bus consists of eight bi-directional lines which connect the CPU and the USART. The bus is used to send both data and command words from the CPU to the USART. It also allows the USART to send received data and status flag information back to the CPU.

Parity Error (PE) – The PE flag is set whenever a parity error is detected by the receiver. It may be reset by programming the Error Reset (ER) bit of the command instruction. The occurence of a parity error does not necessarily preclude other USART operations from continuing and may be handled as desired by the designer. Parity error indication when parity has not been selected is invalid.

Overrun Error (OE) – In the receiving mode, the overrun error flag is set whenever the CPU does not read a character before the next one becomes available. It is reset by programming the Error Reset (ER) bit of the command instruction word. The occurence of an OE does not preclude further USART operations, however the previously overrun character is lost.

Transmitter Buffer Empty (TBMT) – The Transmitter Buffer is an internal register which contains the next character to be transmitted. The TBMT status flag indicates when this buffer becomes empty after its contents have been loaded into the Transmitter Register. The CPU monitors this status flag and may load a new word into the buffer when TBMT goes HIGH.

Transmitter Empty (TMT) – The TMT status flag is a signal which indicates to the CPU whenever both the Transmitter and Transmitter Buffer Registers are empty. When this happens, the USART will automatically start transmitting "sync-fill' characters if in the sync mode or "marks" if in the async mode.

Framing Error/Sync Detected (FESD) – This pin is multi-functional and is used only during reception of serial data from the channel. It functions as a Framing Error output flag during asynchronous operation and a Sync-Detected flag during synchronous operation. It is also the external "sync-found" input for external sync operation.

When receiving data from the channel in the synchronous mode, the FESD pin may be either an input or an output, depending upon whether the USART was programmed for internal or external synchronization. If programmed for internal synchronization, the FESD pin will act as an output indicating that the last character received matched the previously programmed internal sync character, and character assembly will be initiated on the next non-sync character. If programmed for external synchronization, then, the FESD pin will be used as a sync-detected input.

Request To Send ($\overline{RTS}$) – This output signal is activated by programming the TE (Transmitter Enable) bit of the command instruction word and is used to signal the modem that the USART is ready to transmit data.

Clear To Send ($\overline{CTS}$) – This signal is generated by the modem in response to an RTS command and indicates to the USART that the channel is now ready to accept data. Internally, the $\overline{CTS}$ enables the transmitter register to output serial data to the channel via the TSO pin provided that the Transmitter Enable (TE) bit of the command word was set.

Receiver Serial Input (RSI) – Input serial data from the channel is presented to the USART on its RSI pin. Data present on the RSI pin is entered into the internal receiver register of the 3843 at a rate and format as specified by the mode instruction and the receiver clock frequency.

Transmitter Serial Output (TSO) – The TSO output of the USART supplies the serial data to be transmitted by the channel. Data bits stored in the Transmitter Buffer are output, via the TSO, at a rate and format as specified by the Mode Instruction and the transmitter clock frequency.

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Receiver Clock (RCP) – This clock signal controls the rate at which the serial data is received from the channel. In the synchronous receiving mode the clock frequency is equal to the actual baud rate (1x); while in the asynchronous mode the clock frequency is either 16, 32, or 64 times the actual baud rate as prescribed in the Mode Instruction.

Transmitter Clock (TCP) – This clock controls the rate at which serial data is transmitted to the channel. In the synchronous transmission mode, the clock frequency is equal to the actual baud rate (1x); while in the asynchronous mode the clock frequency is either 16, 32, or 64 times the actual baud rate as prescribed in the Mode Instruction.

PROGRAMMING THE USART

Prior to commencing data transmission or reception the 3843 must be programmed for operation in the desired mode. The CPU accomplishes this programming by writing into the 3843, via the data bus, a sequence of specific instruction words which represent a complete functional description of the type of communications format the USART is to use. These instruction words are

1) the Mode Instruction,
2) either zero, one, or two sync characters (depending on the mode selected)
3) the Command Instruction.

This instruction sequence must follow either a pulse on the $\overline{CI}$ (Chip Initialize) pin or a Master Reset command.

The Mode Instruction is the first one in the programming sequence and specifies the details of the operational format. The significance of each bit of the instruction word is described in Table 1.

In the synchronous format—internal sync mode, the Mode Instruction is followed immediately in the programming sequence by either one or two sync characters, depending on whether single or double sync word operation was called for in the previous Mode Instruction. These characters need not be specified and may be omitted if the 3843 was programmed for either the asynchronous mode or the external sync mode.

The last instruction in this sequence is the Command Instruction. Following the SYNC character(s), this instruction controls certain internal operations and status conditions within the USART. The significance of the bits in this instruction word is shown in Table 2. All control words presented to the USART (C/D = 1) after this instruction will also be considered as Command Instructions until a command word indicating a Master Reset is performed. An example is shown in Figure 4.

Status Flags – The status flags of the 3843 collectively form a status word which can be read by the CPU program software. This is accomplished by taking both the $\overline{READ}$ and $\overline{CE}$ lines LOW and the C/$\overline{D}$ line HIGH. The format of the status word is:

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
TBMT	RDA	TMT	PE	OE	FESD	CTS	

These flags have the same meaning as their corresponding output pins and are reset in the same way. See the Pin Definitions section.

TABLE 1 THE MODE INSTRUCTION WORD

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
M1	M2	M3	M4	M5	M6	M7	M8

M1 M2 = Mode and Baud Rate

00 = SYNC mode
01 = 16x in ASYNC mode
10 = 32x in ASYNC mode
11 = 64x in ASYNC mode

M3 M4 = Character Length

00 = 5-bit word
01 = 6-bit word
10 = 7-bit word
11 = 8-bit word

M5 M6 = Parity Control

00 = Disable Parity generation
01 = Even Parity
10 = Odd Parity
11 = Not used

M7 M8 = Stop Bits in ASYNC operation

00 = Not used
01 = 1 Stop Bit
10 = 1½ Stop Bits
11 = 2 Stop Bits

or

M7 M8 = SYNC Control in SYNC Operation

00 = Internal SYNC, Double SYNC Word
01 = Internal SYNC, Single SYNC Word
1X = External SYNC using FESD Pin

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TABLE 2 COMMAND INSTRUCTION WORD

D_0	RE	D_2	D_3	D_4	D_5	D_6	D_7
TE	D_1	EH	SB	ER	SDR	MR	

TE = Transmitter Enable — A "1" programmed in this bit holds the USART in the transmission mode and activates the RTS pin. The transmitter will be enabled after $\overline{CTS}$ goes LOW.

RE = Receiver Enable — A "1" in this bit enables the USART to receive and assemble characters input via the RSI pin.

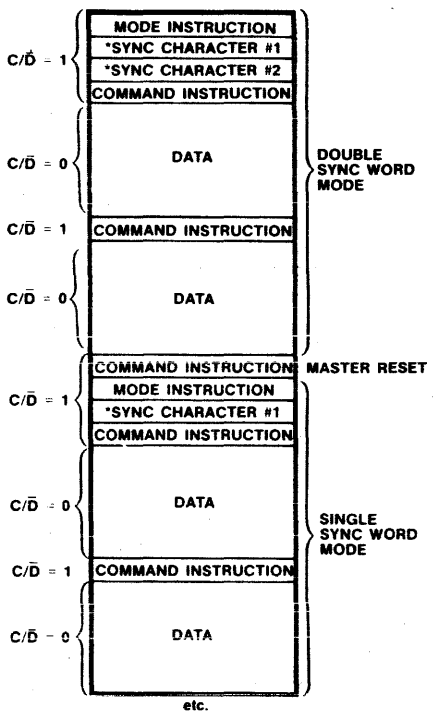
EH = Enter Hunt Mode — A "1" in this bit will cause the USART to "search" for SYNC characters when in the SYNC mode. It is a don't care in ASYNC mode operation. This command is self-cancelling after sync is achieved.

SB = Send Break Character — When programmed to a "1", this bit causes the TSO output line to go LOW continuously until this bit is reset to "0" with another Command Instruction.

ER = Error Reset — A "1" in this bit will reset the PE, OE, and FE (when in ASYNC mode) pins. This command is self-cancelling.

SDR = Sync Detect Reset — A "1" in this bit will reset the FESD pin (when in the internal SYNC mode). This command is self-cancelling.

MR = Master Reset — A "1" in this bit will hold the USART in a reset mode. This bit is equivalent to the $\overline{CI}$ pin. The Master Reset command is self-cancelling.



A programming example showing the sequence of data ($C/\overline{D} = 0$) and control instructions ($C/\overline{D} = 1$) presented to the USART via the data bus is shown at left. The initializing sequence consists of Mode and Command Instructions and either zero, one, or two sync characters depending on what type of format is called for in the Mode Instruction. (No sync characters are used in the async mode or the external sync mode). Any instructions received after a Mode Instruction (except for sync characters) are considered to be a Command Instruction unless a Master Reset command precedes them. The example shows how the USART's operating format may be altered under program control if desired. It applies to both transmission and reception of data in either the synchronous or asynchronous modes.

*May or may not be included, depending on the operating mode.

Fig. 4

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USART CONTROL SIGNALS

FUNCTION	$\overline{CE}$	C/$\overline{D}$	$\overline{READ}$	$\overline{WRITE}$
CPU Writes Control Into USART	0	1	1	0
CPU Writes Data Into USART	0	0	1	0
CPU Reads Data From USART	0	0	0	1
CPU Reads Status From USART	0	1	0	1
USART Disabled, Data Bus HI-Z	1	X	X	X

ABSOLUTE MAXIMUM RATINGS

Voltage of any pin relative to V_{SS}	-0.5 V to +20 V
Operating Temperature (Ambient)	0°C to 70°C
Storage Temperature (Ambient)	-55°C to 150°C
Power Dissipation	1 W

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL REQUIREMENTS: T_A = 0°C to 70°C. All Voltage Referenced to V_{SS}.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	V	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input HIGH Voltage	2.7	—	7.0	V	
V_{IL}	Input LOW Voltage	-0.5	—	0.8	V	

DC ELECTRICAL CHARACTERISTICS: Over Full Range of Voltage and Temperature

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{DD}	Average V_{DD} Current			25	mA	
I_{CC}	Average V_{CC} Current			40	mA	
V_{OH}	Output HIGH Voltage	3.0			V	I_{OUT} = -100 mA
V_{OL}	Output LOW Voltage			0.4	V	I_{OUT} = 3.2 mA
I_{IN}	Input Leakage Current			10	μA	V_{IN} = 10 V
I_{OUT}	Output Leakage Current	-10		10	μA	V_{OUT} = 10 V
C_{IN}	Input Capacitance, all Inputs except D_0-D_7.			10	pF	f = 1 MHz
C_{OUT}	Output Capacitance, all Outputs except D_0-D_7.			10	pF	f = 1 MHz
$C_{I/O}$	Data Bus Capacitance, D_0-D_7.			20	pF	f = 1 MHz

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AC ELECTRICAL REQUIREMENTS: Over the Full Range of Voltage and Temperature

SYMBOL	PARAMETER		3843-1 MIN	3843-1 MAX	3843-2 MIN	3843-2 MAX	3843-3 MIN	3843-3 MAX	UNITS
t_{PC}	Clock Period	PC, DC	3.125		6.25		12.5		μs
		DL, DM	6.25		12.5		25		μs
t_{CL}	Clock LOW Time		850		1700		3400		ns
t_{TC}	Clock Transition Time (Rise and Fall)		3	50	3	50	3	50	ns
t_T	Transition Time (All inputs except clocks)		3	50	3	50	3	50	ns
t_{CI}	Chip Initialize Pulse Width		$3t_{PC}$		$3t_{PC}$		$3t_{PC}$		—
t_{RP}	$\overline{\text{READ}}$ Pulse Width		850		1700		3400		ns
t_{WP}	$\overline{\text{WRITE}}$ Pulse Width		850		1700		3400		ns
t_{SWP}	Time Between Successive $\overline{\text{WRITE}}$ Pulses		3		3		3		μs
t_{CES}	CE Set-Up Time to $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$		1000		2000		4000		ns
t_{CEH}	CE Hold Time From $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$		0		0		0		ns
t_{CDS}	C/D Set-up Time to $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$		1000		2000		4000		ns
t_{CDH}	C/D Hold Time After $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$		250		500		750		ns
t_{DSW}	Data Set-up Time to $\overline{\text{WRITE}}$		250		500		750		ns
t_{DHW}	Data Hold-Time After $\overline{\text{WRITE}}$		250		500		750		ns
t_{CRL}	C/D to $\overline{\text{READ}}$ Lead Time		250		500		750		ns
t_{CWL}	C/D to $\overline{\text{WRITE}}$ Lead Time		250		500		750		ns
t_{RDS}	RSI Data Set-up Time to RCP Clock								ns

AC ELECTRICAL CHARACTERISTICS: Over the Full Range of Voltage Temperature

SYMBOL	PARAMETER	3843-1 MIN	3843-1 MAX	3843-2 MIN	3843-2 MAX	3843-3 MIN	3843-3 MAX	UNITS
t_{WTD}	WRITE to TBMT LOW Delay	300		600		1200		ns
t_{WRD}	WRITE to RTS LOW Delay	300		600		1200		ns
t_{RDD}	READ to Output Data Delay	300		600		1200		ns
t_{RRH}	Center of RSI Bit to RDA HIGH Delay	$3t_{PC}$		$3t_{PC}$		$3t_{PC}$		—
t_{RRL}	READ to RDA LOW Delay							ns
t_{CTD}	Clock to TSO Output Delay	500		1000		2000		ns
t_{OFF}	Device Deselect to Data Bus High Impedance	250		400		800		ns

MAXIMUM USART DATA RATES

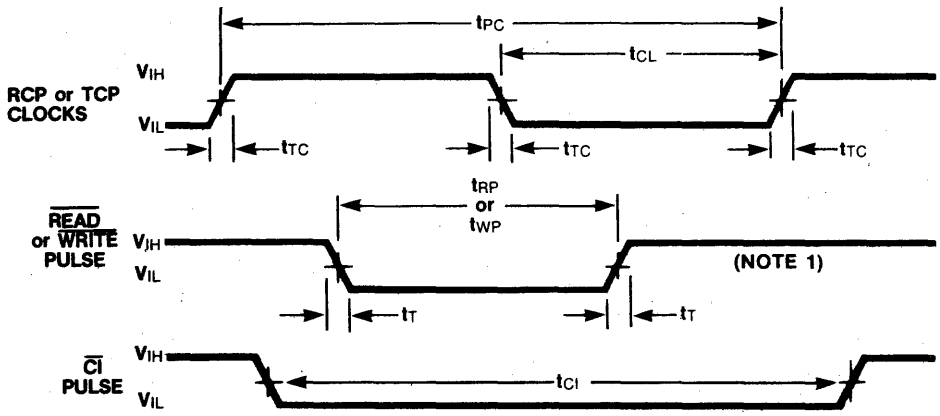
MODE	PART NUMBER	3843-1 C	3843-1 L	3843-1 M	3843-1 C	3843-1 L	3843-1 M	3843-3 C	3843-3 L	3843-3 M
SYNC	1X	320 K Baud	160 K Baud	160 K Baud	160 K Baud	80 K Baud	80 K Baud	80 K Baud	40 K Baud	40 K Baud
ASYNC	16X	20 K Baud	10 K Baud	10 K Baud	10 K Baud	5 K Baud	5 K Baud	5 K Baud	2.5 K Baud	2.5 K Baud
	32X	10 K Baud	5 K Baud	5 K Baud	5 K Baud	2.5 K Baud	2.5 K Baud	2.5 K Baud	1.25 K Baud	1.25 K Baud
	64X	5 K Baud	2.5 K Baud	2.5 K Baud	2.5 K Baud	1.25 K Baud	1.25 K Baud	1.25 K Baud	.625 K Baud	.625 K Baud

NOTE: 1 K BAUD Equals 1000 Bits per Second

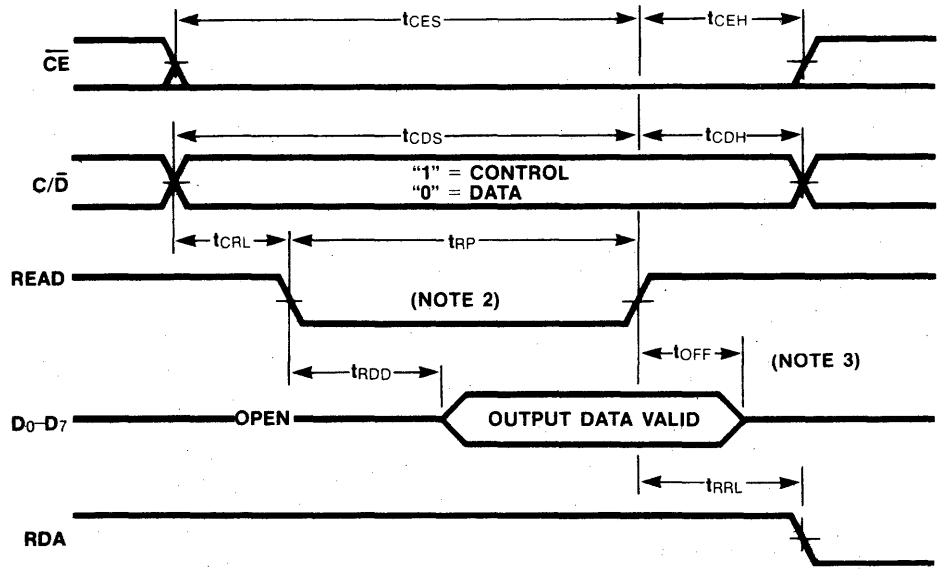
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TIMING DIAGRAMS

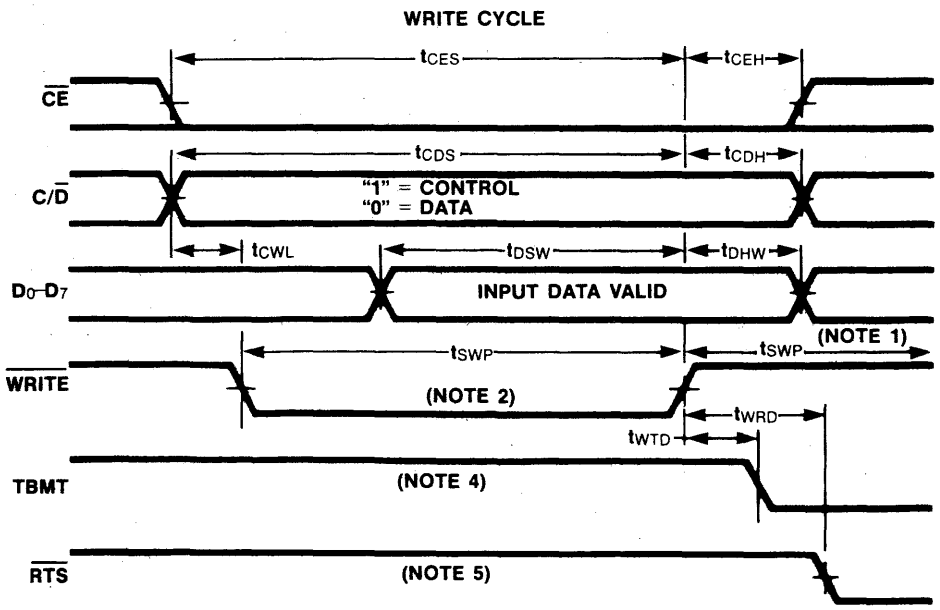
MINIMUM PULSE WIDTHS



READ CYCLE



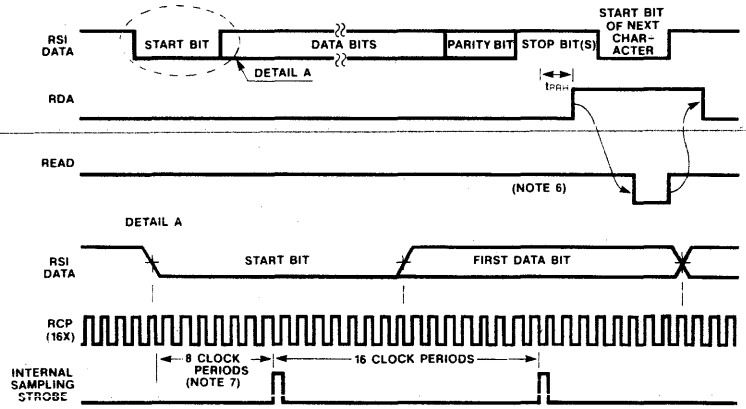
WRITE CYCLE



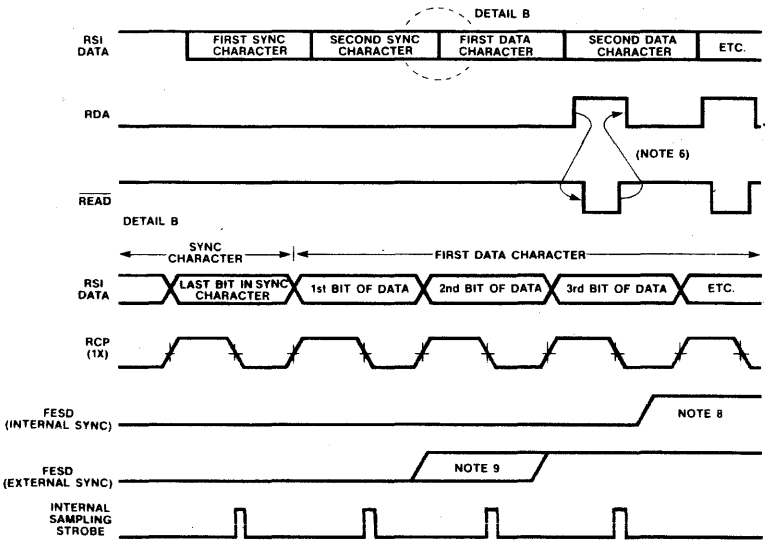
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TIMING DIAGRAMS (Cont'd)

RECEIVER TIMING—ASYNC MODE



RECEIVER TIMING—SYNC MODE



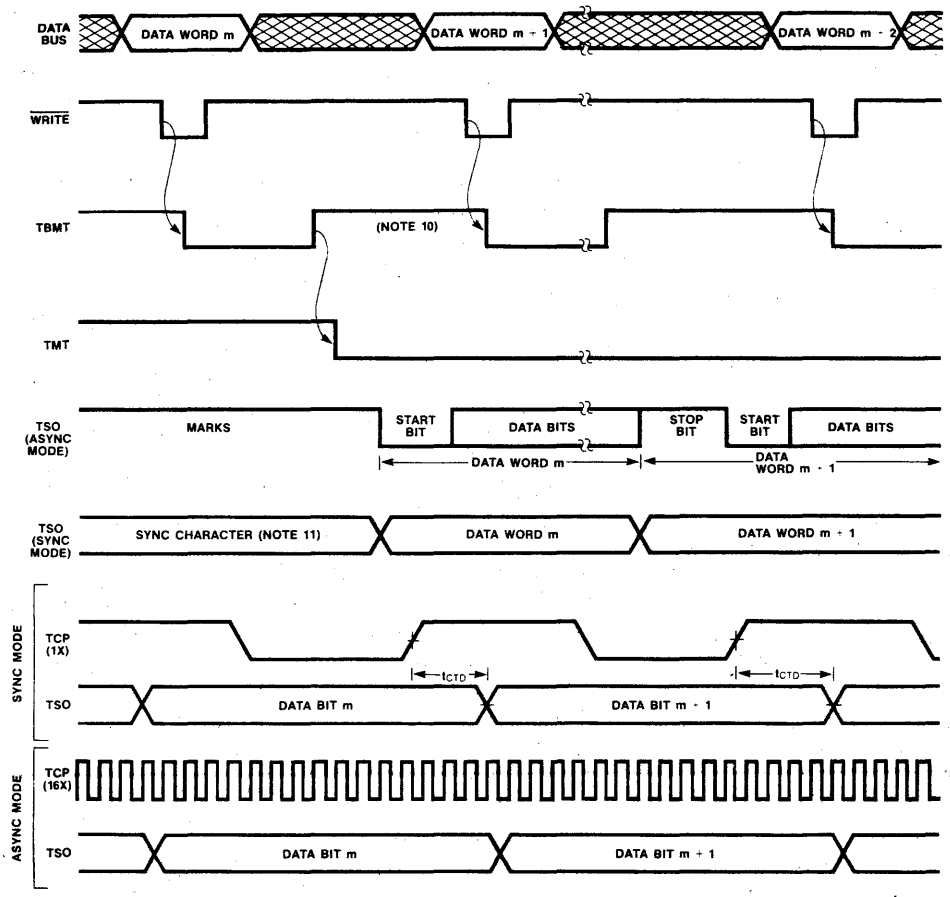
NOTES:

1. The minimum allowable time between successive $\overline{\text{WRITE}}$ pulses is given by the parameter t_{SWP} min.
2. The Chip Enable signal and the $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ signal and ANDed together internally to form an effective $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ signal. Therefore, the last of these two signals to go LOW in a $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ operation generates the leading edge of this internal signal while the first to go HIGH generates the trailing edge. It is to the edges of this internal signal that the $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ timeing parameters are referenced. For purposes of illustration, the timing diagram shows Chip Enable as beginning before and extending beyond the externally applied $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ signal. Thus, the timing parameters are referenced to $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ rather than $\overline{\text{CE}}$.
3. The data bus buffer turn-off delay time, i.e. t_{OFF}, is referenced from the rising edge of either $\overline{\text{READ}}$ or $\overline{\text{CE}}$, whichever occurs first. t_{OFF} max defines the time at which the data I/O bus achieves the open circuit high impedance condition and is not referenced to output voltage levels.
4. For purposes of illustration, the transmitter buffer is assumed to be empty prior to the $\overline{\text{WRITE}}$ cycle shown.
5. For purposes of illustration, $\overline{\text{RTS}}$ is shown going LOW, implying that a command instruction ($C/\overline{D} = 1$) is being input with a "0" programmed in the appropriate bit location. See programming instructions.
6. This diagram illustrates the recommended timing relationship between RDA and $\overline{\text{READ}}$. The external system logic responds to RDA by pulsing the $\overline{\text{READ}}$ line. RDA is then reset after $\overline{\text{READ}}$ returns HIGH again, i.e., inactive.
7. This diagram illustrates receiver timing for the 16x async mode. Other modes are similar in operation. Here the START bit is sampled after eight cycles of the RCP clock. The 8-cycle count-off begins with the first negative transition of the RCP clock after the RSI line goes LOW. Subsequent sampling points are separated by intervals of 16 clock periods each.
8. The sync-detected condition is indicated by the FESD pin going HIGH no sooner than three bit times after the reception of the last sync character in the internal sync mode.
9. In the external sync mode, the external decoding of sync characters must be accomplished and the FESD pin forced HIGH indicating synchronization detected during the bit time interval corresponding to the second data bit.
10. The $\overline{\text{WRITE}}$ pulse causes the TBMT flag to be reset. Another cycle should not be attempted until after the TBMT flag has returned HIGH and the t_{SWP} (min) delay time has elapsed. See Note 1.
11. If the double sync character mode is being used, then sync characters will always be transmitted in pairs, and whenever the first is transmitted, the second character will always follow. Therefore transmitted data will always be immediately preceded by the second sync character in this mode.

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TIMING DIAGRAMS (Cont'd)

TRANSMITTER TIMING—SYNC AND ASYNC MODES



ORDERING INFORMATION

PART NUMBER	MAX DATA RATE (SYNC MODE)	TEMPERATURE RANGE	PACKAGE TYPE	ORDER CODE
3843-1	320 K Baud	0° to 70°C	Plastic	38431PC
	320 K Baud	0° to 70°C	Ceramic	38431DC
	160 K Baud	−55° to 85°C	Ceramic	38431DL
	160 K Baud	−55° to 125°C	Ceramic	38431DM
3843-2	160 K Baud	0° to 70°C	Plastic	38432PC
	160 K Baud	0° to 70°C	Ceramic	38432DC
	80 K Baud	−55° to 85°C	Ceramic	38432DL
	80 K Baud	−55° to 125°C	Ceramic	38432DM
3843-3	80 K Baud	0° to 70°C	Plastic	38433PC
	80 K Baud	0° to 70°C	Ceramic	38433DC
	40 K Baud	−55° to 85°C	Ceramic	38433DL
	40 K Baud	−55° to 125°C	Ceramic	38433DM

Fairchild cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in a Fairchild product. No other circuit patent licenses are implied. Manufactured under one of the following U S Patents: 2981877, 3015048, 3064167, 3108359, 3117260; other patents pending.

F16K

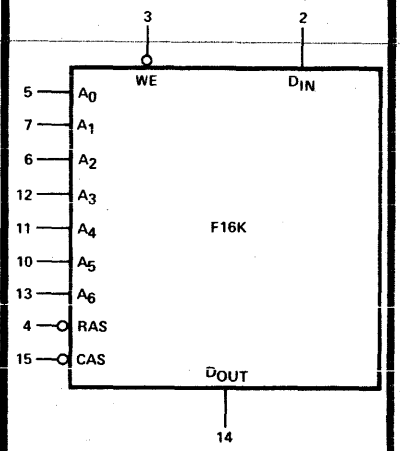
16,384 x 1 DYNAMIC RANDOM ACCESS MEMORY

FAIRCHILD ISOPLANAR SILICON GATE MOS

GENERAL DESCRIPTION – The F16K is a 16,384-bit MOS Dynamic Random Access Memory configured as 16,384 one-bit words, and which is manufactured using Fairchild's n-channel silicon gate, double-poly Isoplanar process. The use of the single-transistor memory cell along with address multiplexing techniques permits the packaging of the F16K in a standard 16-pin dual in-line package. The use of this package allows construction of highly dense memory systems utilizing widely available automated testing and insertion equipment. Furthermore, the pinout, timing and organizational characteristics of the F16K are essentially the same as Fairchild's 4K dynamic RAMs, the M4027 and the 4096. Thus the F16K is ideally suited for easy upgrading of M4027 or 4096-based systems.

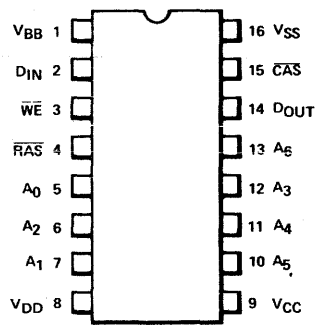
- **INDUSTRY STANDARD 16-PIN DUAL IN-LINE PACKAGE**
- **LOW CAPACITANCE, TTL-COMPATIBLE INPUTS (INCLUDING CLOCKS)**
- **ON-CHIP ADDRESS AND INPUT DATA LATCHES**
- **3-STATE TTL-COMPATIBLE OUTPUT WITH DATA VALID TIME CONTROLLED BY $\overline{CAS}$**
- **COMMON I/O CAPABILITY**
- **TWO DIMENSIONAL SELECTION BY DECODING BOTH $\overline{RAS}$ AND $\overline{CAS}$**
- **STANDARD 10% SUPPLIES (+12 V, +5 V, and –5 V)**
- **FLEXIBLE TIMING WITH PAGE-MODE AND EXTENDED PAGE BOUNDARIES**
- **128-CYCLE $\overline{RAS}$-ONLY REFRESH**
- **PINOUT COMPATIBLE WITH M4027 OR 4096 FOR EASY SYSTEM UPGRADING**

LOGIC SYMBOL

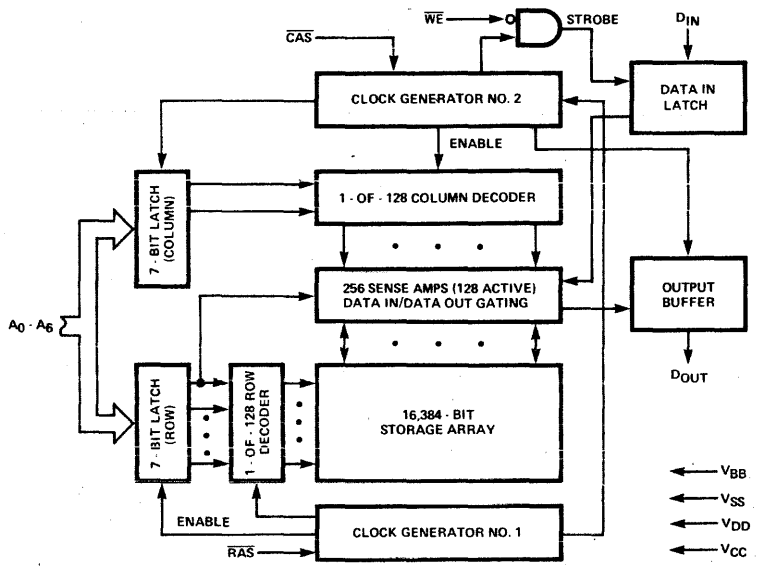


V_{SS} = Pin 16
V_{CC} = Pin 9
V_{DD} = Pin 8
V_{BB} = Pin 1

CONNECTION DIAGRAM
DIP (TOP VIEW)



BLOCK DIAGRAM



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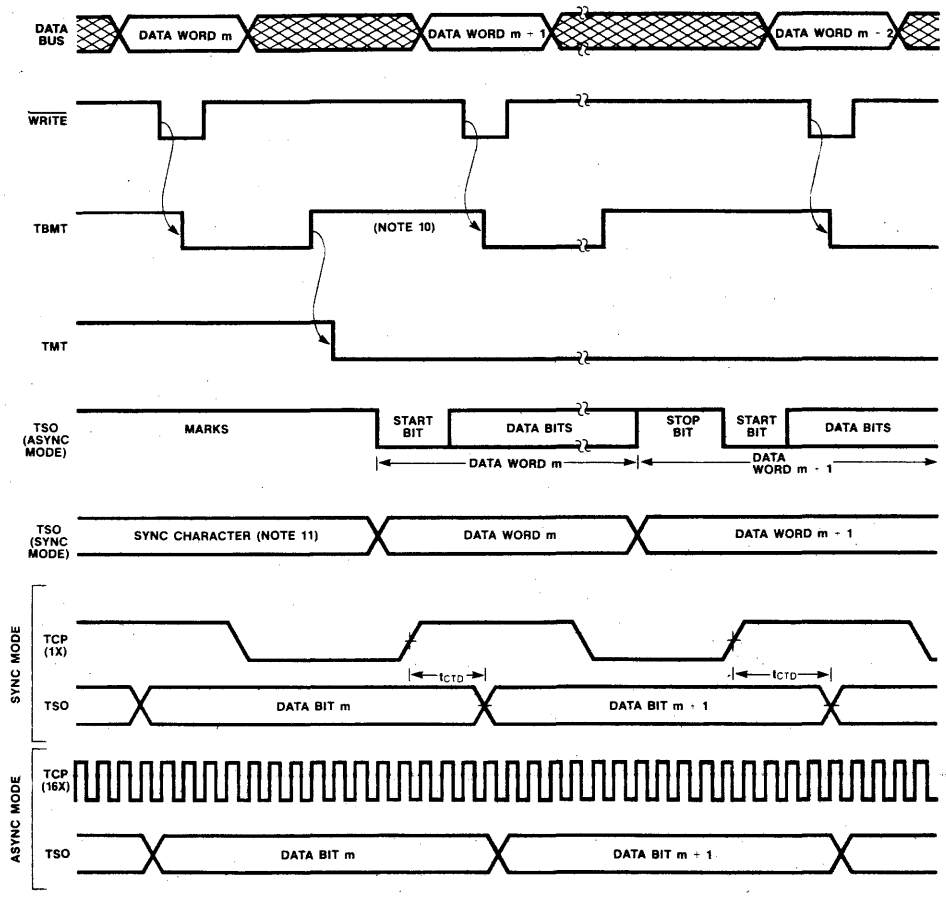
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FAIRCHILD

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TIMING DIAGRAMS (Cont'd)

TRANSMITTER TIMING—SYNC AND ASYNC MODES



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F16K

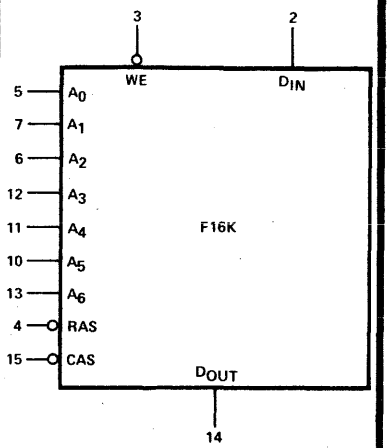
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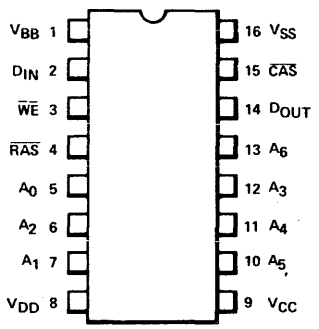
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LOGIC SYMBOL

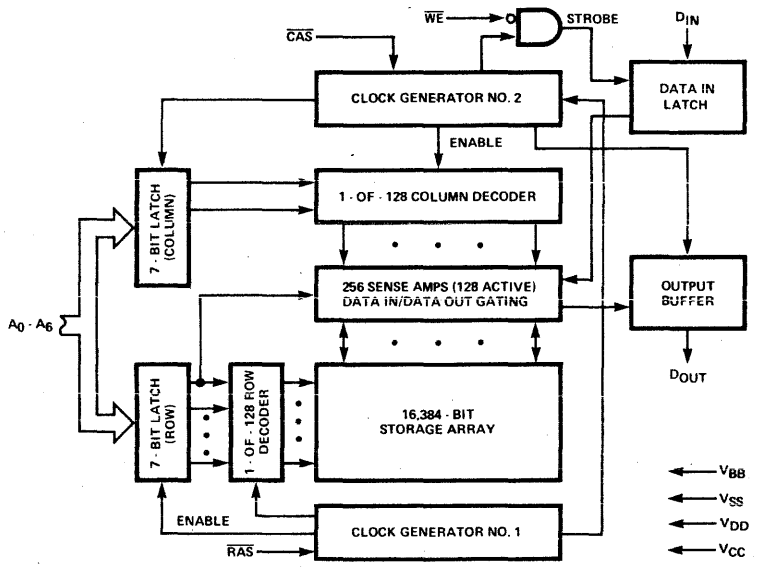


V_{SS} = Pin 16
V_{CC} = Pin 9
V_{DD} = Pin 8
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CONNECTION DIAGRAM
DIP (TOP VIEW)



BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

ADDRESSING – The 14 address bits required to decode one-of-16, 384 cell locations in the F16K are entered using a 2-phase multiplexing operation in which first the 7-bit Row Address is entered followed by the 7-bit Column Address. First the 7-bit Row Address is applied to the seven address inputs of the F16K and latched into the chip by Row Address Strobe ($\overline{RAS}$) which is the first of two externally applied TTL-level clocks. The second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the seven column address bits into the chip. Each of these signals $\overline{RAS}$ and $\overline{CAS}$, trigger on-chip clock generators which control the internal sequencing of events on the chip. Advanced techniques used in handling the row and column address information allow the address multiplexing operation to be performed without lengthening the critical timing path governing the access time. The activation of $\overline{CAS}$ strobes the column address latch but this event as well as other internal events governed by the $\overline{CAS}$ clock generator may be inhibited until certain prerequisite events controlled by the $\overline{RAS}$ clock generator have occured.

More specifically, a "window" of time exists, extending from $t_{RCD(min)}$ to $t_{RCD(max)}$ during which $\overline{CAS}$ may become active without impacting the access time. Stated another way, as long as $\overline{CAS}$ occurs during this window, the access time will be specified by t_{RAC}. If $\overline{CAS}$ occurs a certain delay after this window of time, the $\overline{RAS}$ clock generator no longer inhibits the $\overline{CAS}$ clock generator and the magnitude of this delay will add directly to the overall access time. This lengthened access time is now referenced to $\overline{CAS}$ rather than $\overline{RAS}$ and is lengthened by the amount of time that t_{RCD} exceeds the $t_{RCD(max)}$ limit. This "gated-$\overline{CAS}$" feature allows greater flexibility since the $\overline{CAS}$ clock may be externally activated as soon as the Hold Time for the Row Address has been met and the address inputs have been changed from Row Address to Column Address information.

PAGE MODE OPERATION – The Page-Mode feature of the F16K allows successive memory cycles accessing the same row in the memory matrix to be concatenated together in such a way that the common Row Address need be supplied only once - resulting in faster access times with no corresponding increase in power. The page-mode option may be used in conjunction with any of the defined memory operations, and is accomplished by supplying the Row Address to the chip and holding $\overline{RAS}$ LOW throughout all subsequent memory cycles for which the Row Address is common.

Since $\overline{RAS}$ makes its initial negative transition only once, no additional dynamic power is dissipated due to $\overline{RAS}$ on any subsequent cycles performed within that row. The access and cycle times are also shortened since the time required to supply a Row Address is eliminated.

DATA INPUT – In a write operation, the data to be input into memory is strobed into an on-chip register during $\overline{RAS}$ by a combination of $\overline{CAS}$ and Write Enable ($\overline{WE}$). The strobe is formed by whichever is the latter of these two signals to make its negative transistion. This presents several possibilities in how a write cycle may be performed. In an "early-write" cycle ($\overline{WE}$ active LOW before $\overline{CAS}$ goes LOW), Data In (D_{IN}) is strobed by $\overline{CAS}$ and thus the set-up and hold times are referenced to this signal edge. If D_{IN} is not yet valid at the time $\overline{CAS}$ becomes active (or if the cycle is a read-write or read-modify-write) then $\overline{WE}$ must be delayed. In this delayed-write mode, the D_{IN} set-up and hold times are referenced to $\overline{WE}$ rather than $\overline{CAS}$. (See the timing diagrams).

DATA OUTPUT – The Data Out (D_{OUT}) latch and buffer unconditionally assume the high-impedance state whenever $\overline{CAS}$ is HIGH, i.e. inactive. If the cycle being performed is a read, read-modify-write, or a delayed write cycle then the D_{OUT} latch and buffer will remain high impedance until the access time, after which D_{OUT} will assume the value of the data read from the selected cell. This output data is of the same polarity (not inverted) as the input data and will remain valid as long as $\overline{CAS}$ is kept active, i.e. LOW. However, if the cycle is an "early-write" cycle or if the chip fails to receive both $\overline{RAS}$ and $\overline{CAS}$, then D_{OUT} will remain high impedance throughout the cycle. This feature allows systems which write employing the early write mode exclusively, to common D_{IN} and D_{OUT} directly together.

Another advantage of this "unlatched output" feature is that OR-tied outputs in a memory matrix require no special action to be turned off. Unlike other types of RAMs which require a negative transition of $\overline{CAS}$ to become high impedance, the F16K's output is already high impedance whenever $\overline{CAS}$ is HIGH, i.e. inactive. This means that $\overline{CAS}$ need not be supplied to unused devices and therefore may be used for device selection. Thus a reduction in external decoding logic is possible by using both $\overline{RAS}$ and $\overline{CAS}$ in a 2 dimensional decoding/selection scheme. (see Table 1 below).

$\overline{RAS}$ active during cycle?	$\overline{CAS}$ active during cycle?	RESULT (after t_{OFF} delay)
Yes	Yes	Device active
Yes	No	Device deselected, refresh
No	Yes	Device deselected
No	No	Device deselected

TABLE 1

EXTENDED PAGE BOUNDARY – A further implication of using both $\overline{RAS}$ and $\overline{CAS}$ for device decoding/selection is in extending page boundaries for page-mode operation. If only $\overline{RAS}$ is decoded, then any given "page" is limited to only 128 different column addresses within that page, (i.e. seven column address bits correspond to 2^7 = 128 column addresses). Therefore, for memory systems using more than 16K words of data, page boundaries may be extended from 128 addresses per page up to any multiple of 128 addresses merely by decoding which 16K memory bank also gets a $\overline{CAS}$

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(subject to $t_{RAS(max)}$ limitation). This is accomplished by supplying $\overline{RAS}$ to all devices in order to latch in the Row Address information and then decoding which bank of 16K words is to also get $\overline{CAS}$. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ will respond with a valid memory cycle.

INPUT/OUTPUT LEVELS – All inputs, including the two address strobes, interface directly with TTL. The high-impedance, low-capacitance input characteristics simplify input driver selection by allowing use of standard logic elements rather than specially designed driver elements. Termination resistors are normally required in a system to prevent ringing due to line inductance and reflections. In high-speed memory systems, transmission line techniques must be employed on the signal lines to achieve optimum system speeds. Series termination may be employed at some degradation of system speed.

The 3-state output buffer is a low impedance to V_{CC} for logic "1" and low impedance to V_{SS} for logic "0". The effective resistance to V_{CC} is 420 Ω maximum and 135 Ω typically. The effective resistance to V_{SS} is 95 Ω maximum and 35 Ω typically.

REFRESH – The matrix of 128 X 128 memory cells in the F16K is refreshed by executing a memory cycle at each of the 128 Row Addresses within each interval of 2 milliseconds or less. Although any cycle in which $\overline{RAS}$ occurs accomplishes a refresh operation, the refresh is most easily accomplished in the $\overline{RAS}$-only-refresh mode. This type of refresh operation results in decreased power dissipation since $\overline{CAS}$ remains inactive.

POWER DISSIPATION/STANDBY – Since the F16K uses dynamic memory cells, this means that most of the dissipated power is a result of an address strobe edge. There is, however, a small dc component of dissipated power that is associated with the precharging of the sense amplifiers. Thus, the total power dissipated is a function of both operating frequency and duty cycle. Typically, the power is 350 mW at 1 μs cycle time with a worst case power of less than 462 mW at 375 μs cycle time. To reduce overall system power during standby, $\overline{RAS}$-only-refresh cycles should be performed with $\overline{CAS}$ held HIGH.

The V_{CC} supply is not used in the internal memory operations of the F16K, but rather used only at the output buffer and thus, for some applications, may be powered from the supply voltage of the logic to which the chip's output is interfaced. This means that I_{CC}, the current drawn from the V_{CC} supply, is a function of output loading. During battery standby operation, the V_{CC} pin may be unpowered, if desired, without affecting the refresh operation. This allows all system logic, except the $\overline{RAS}$ timing circuitry and the refresh address logic, to be turned off during battery standby to conserve power.

PIN NAMES

A_n	Address Inputs	D_{OUT}	Data Output
D_{IN}	Data Input	V_{CC}	+5 V Power Supply
$\overline{WE}$	Write Enable Input (Active LOW)	V_{SS}	0 V Power Supply
$\overline{RAS}$	Row Address Strobe (Clock) Input (Active LOW)	V_{BB}	–5 V Power Supply
$\overline{CAS}$	Column Address Strobe (Clock) Input (Active LOW)	V_{DD}	+12 V Power Supply

ABSOLUTE MAXIMUM RATINGS

Voltage of any pin relative to V_{BB} ($V_{SS} - V_{BB} \geq 4.5$ V)	–0.5 V to + 20 V
Operating Temperature (Ambient)	0°C to 70°C
Storage Temperature (Ambient)	–55°C to 150°C
Power Dissipation	1 W

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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DC REQUIREMENTS: T_A = 0°C to 70°C (See Notes 1 and 2)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{DD}	Supply Voltage	10.8	12	13.2	V	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	Note 5
V_{SS}	Supply Voltage	0	0	0	V	
V_{BB}	Supply Voltage	−5.5	−5.0	−4.5	V	
V_{IHC}	Input HIGH Voltage, RAS, CAS, WE	2.7		7.0	V	
V_{IH}	Input HIGH Voltage, All inputs except RAS, CAS, WE	2.4		7.0	V	
V_{IL}	Input LOW Voltage, all inputs	−1.0		0.8	V	

DC ELECTRICAL CHARACTERISTICS: Over Full Range of Voltage and Temperature

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	CONDITIONS
I_{DD}	Average V_{DD} Current	Normal Operation			35	mA	
		Standby			1.5	mA	
		Refresh			27	mA	
		Page Mode			27	mA	Note 3
I_{CC}	Average V_{CC} Current	Normal Operation				mA	
		Standby/Refresh	−10		10	μA	Note 4
I_{BB}	Average V_{BB} Current	Normal Operation			200	μA	
		Standby			100	μA	
V_{OH}	Output HIGH Voltage		2.4			V	I_{OUT} = 5.0 mA, Note 5
V_{OL}	Output LOW Voltage				0.4	V	I_{OUT} = 3.2 mA, Note 5
I_{IN}	Input Leakage Current (any input)		−10		10	μA	
I_{OUT}	Output Leakage Current		−10		10	μA	
C_{IN1}	Input Capacitance, A_0–A_6, D_{IN}			4.0	5.0	pF	Note 6
C_{IN2}	Input Capacitance, RAS, CAS, WE			8.0	10	pF	Note 6
C_{OUT}	Output Capacitance, D_{OUT}			5.0	7.0	pF	CAS = V_{IHC}

NOTES:

1. The ambient temperature, (T_A) is specified here for operation at frequencies up to that frequency determined by the minimum cycle time. Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.
2. All voltages are referenced to V_{SS} = 0 V.
3. I_{DD} depends on frequency of operation. Maximum current is measured at the fastest cycle rate.
4. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only. During readout of HIGH level data, V_{CC} is connected through a low impedance (135Ω typ) to Data Out. At other times I_{CC} consists of leakage currents only.
5. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the $V_{OH(min)}$ specification is not guaranteed in this mode.
6. Effective capacitance calculated from the equation $C = I\frac{\Delta t}{\Delta V}$ with ΔV = 3 V and power supplies at normal levels.
7. The specifications for $t_{RC(min)}$, $t_{RWC(min)}$ and $t_{PC(min)}$ are used only to indicate cycle time at which proper operation over full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
8. Assumes that $t_{RCD} \leq t_{RCD(max)}$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCL} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCS(max)}$.
10. Measured with a load equivalent to two TTL loads and 100 pF.
11. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
13. $V_{IHC(min)}$ or $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
14. t_{WCS} is not a restrictive operating parameter but is included as an electrical characteristic only. If $t_{WCS} \geq t_{WCS(min)}$, the cycle is an early write cycle and the Data Out pin will remain open circuit (high impedance) throughout the entire cycle, otherwise the cycle is a delayed write cycle.
15. The parameters t_{RWL} and t_{CWL} reference WE (for a read-modify-write cycle), to either RAS or CAS respectively, whichever is the first to go HIGH.
16. t_{DS} and t_{DH} are referenced to the leading edge of CAS in early write cycles, and to the leading edge of WE in delayed write or read-modify-write cycles.
17. t_{RWD} and t_{CWD} are not restrictive operating parameters but are included in the data sheet as electrical characteristics only:

    If $t_{CWD} + t_T \leq t_{CWD(min)}$, the Data Out latch will remain in the high impedance state.

    If $t_{CWD} \geq t_{CWD(max)} + t_T$, the Data Out latch will contain the data read from the selected cell.

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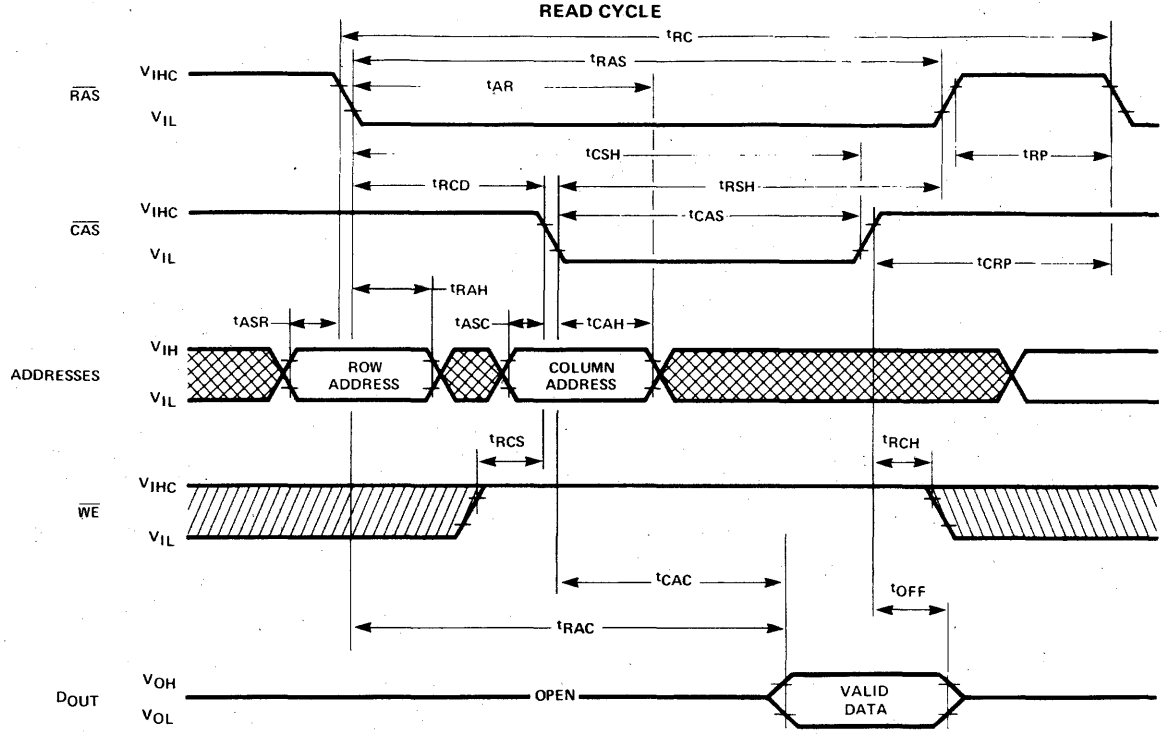
RECOMMENDED AC OPERATING CONDITIONS: Over Full Range of Voltage and Temperature and Voltage Range

SYMBOL	PARAMETER	PART NUMBER								UNITS	NOTES
		F16K-2		F16K-3		F16K-4		F16K-5			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	375		375		410		500		ns	7
t_{RWC}	Read/Write Cycle Time	375		375		515		625		ns	7
t_{PC}	Page Mode Cycle Time	170		225		275		325		ns	
t_{RAC}	Access Time from $\overline{RAS}$		150		200		250		300	ns	8,10
t_{CAC}	Access Time from $\overline{CAS}$		100		135		165		195	ns	9,10
t_{OFF}	Output Buffer Turn-off Delay	0	40	0	50	0	60	0	70	ns	11
t_{RP}	$\overline{RAS}$ Precharge Time	100		120		150		190		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10k	200	10k	250	10k	300	10k	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	100		135		165		195		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	150		200		250		300		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	100	10k	135	10k	165	10k	195	10k	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	65	35	85	80	105	ns	12
t_{ASR}	Row Address Set-up Time	0		0		0		0		ns	
t_{RAH}	Row Address Hold Time	20		25		35		80		ns	
t_{ASC}	Column Address Set-up Time	−10		−10		−10		0		ns	
t_{CAH}	Column Address Hold Time	45		55		75		80		ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	95		120		160		185		ns	
t_T	Transition Time (rise and fall)	3	35	3	50	3	50	3	50	ns	13
t_{RCS}	Read Command Set-up Time (RMW)	0		0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		0		ns	
t_{WCH}	Write Command Hold Time	45		55		75		130		ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		120		160		240		ns	
t_{WCS}	Write Command Set-up Time	−20		−20		−20		0		ns	14
t_{WP}	Write Command Pulse Width	45		55		75		130		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	60		80		100		130		ns	15
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	60		80		100		130		ns	15
t_{DS}	Data In Set-up Time	0		0		0		0		ns	16
t_{DH}	Data In Hold Time	45		55		75		130		ns	16
t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	95		120		160		260		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	−20		−20		−20		0		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Page-mode)	60		80		100		120		ns	
t_{RF}	Refresh Period		2.0		2.0		2.0		2.0	ms	
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	70		95		125		180		ns	17
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	120		160		200		290		ns	17

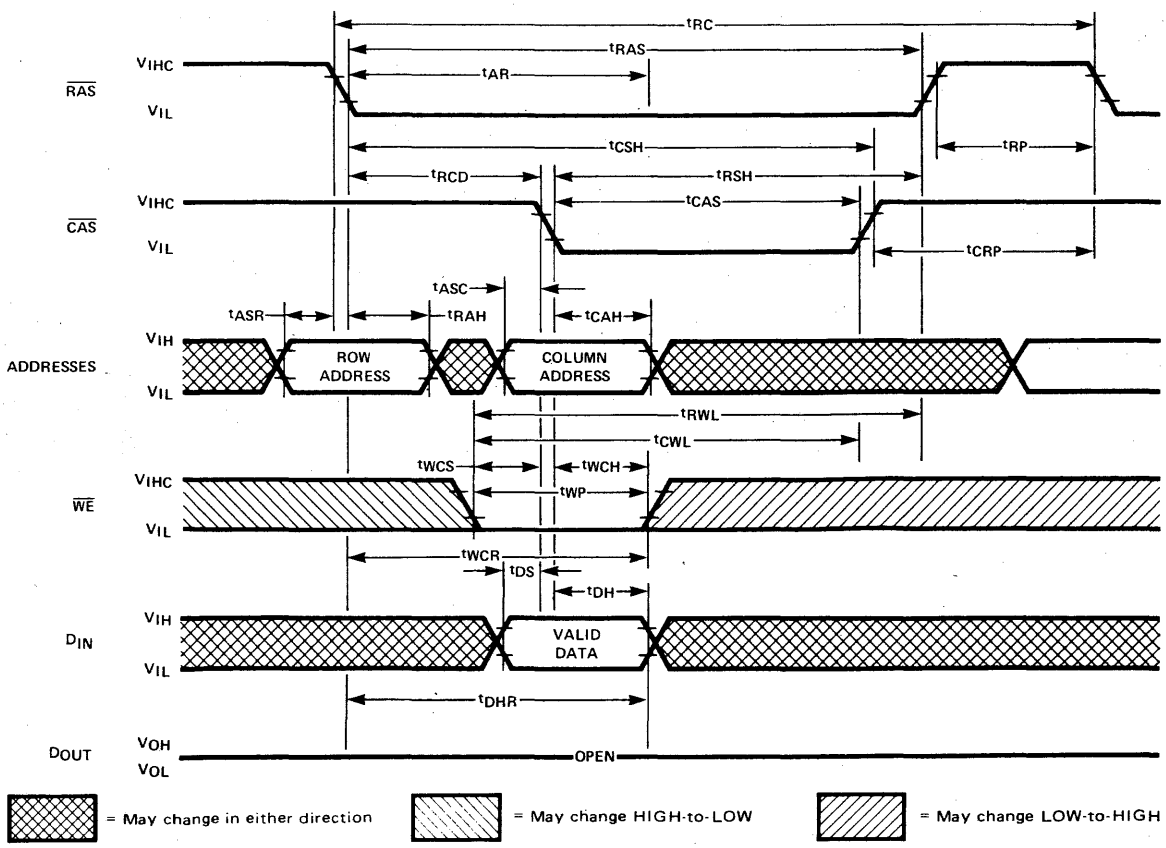
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TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE (EARLY WRITE)

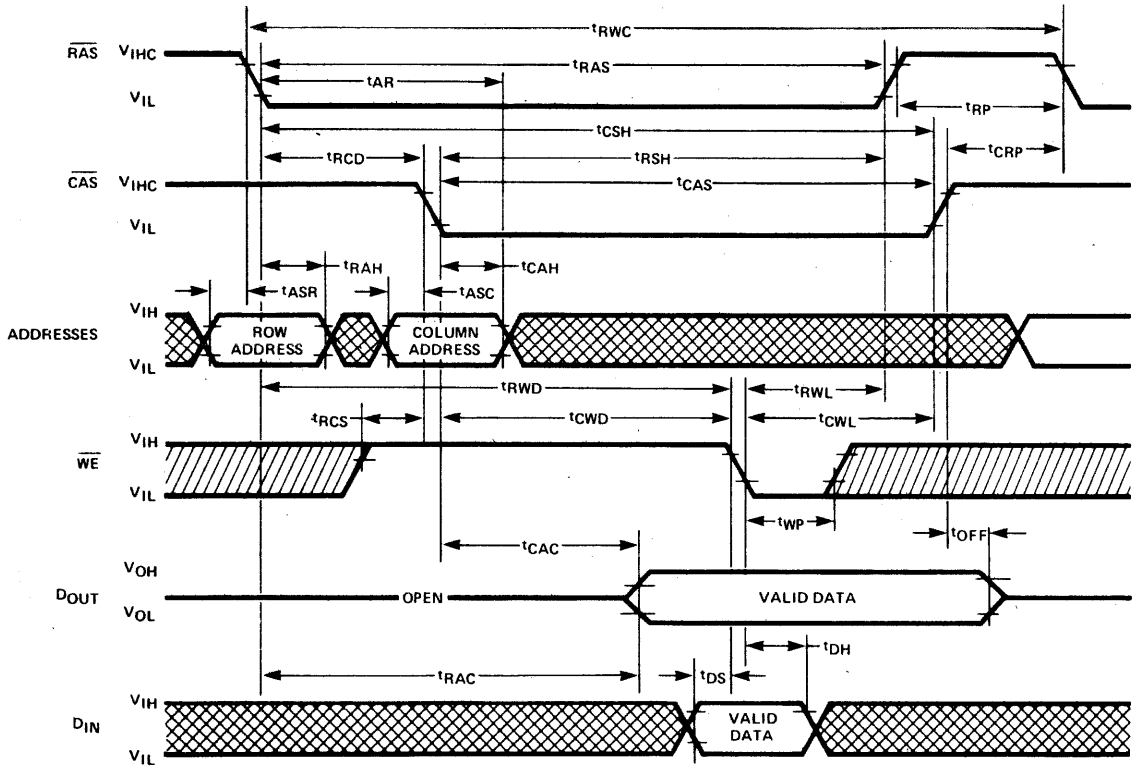


= May change in either direction

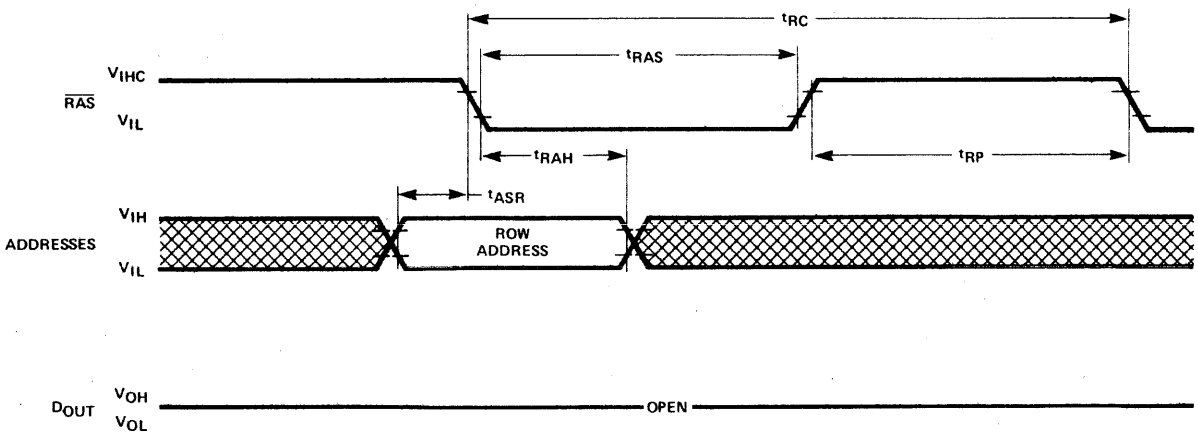
= May change HIGH-to-LOW

= May change LOW-to-HIGH

READ-WRITE/READ-MODIFY-WRITE CYCLE



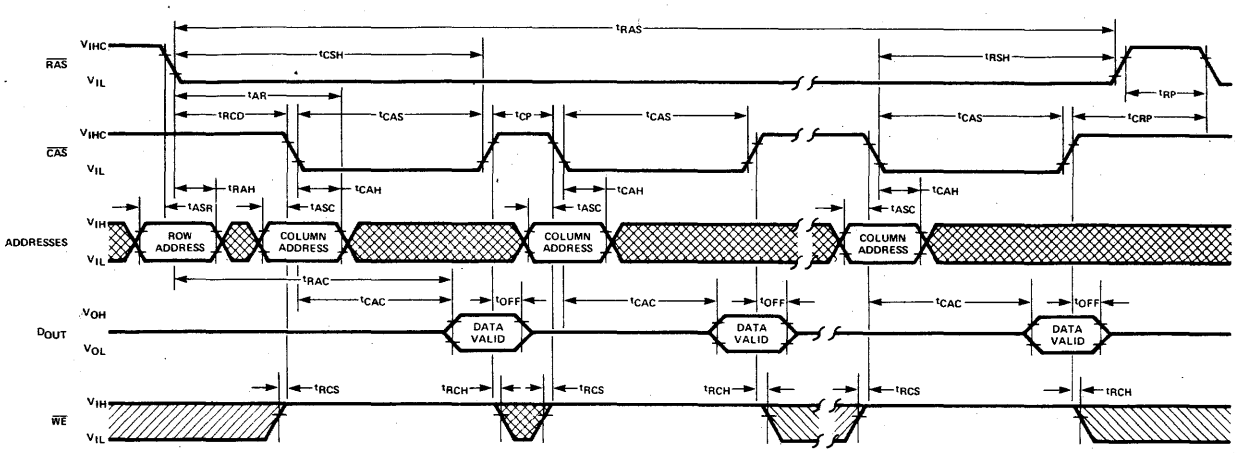
"RAS ONLY" REFRESH CYCLE



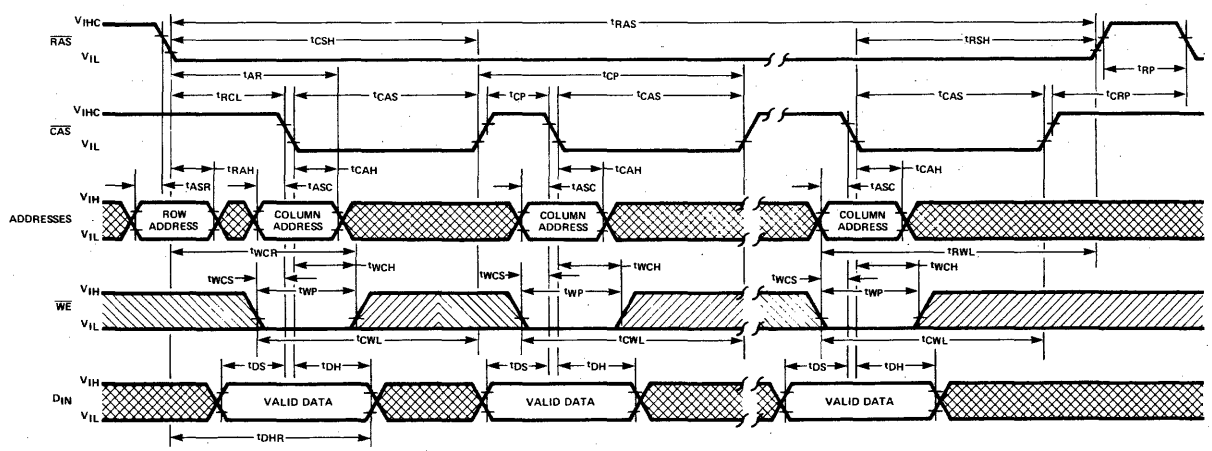
= May change in either direction = May change HIGH-to-LOW = May change LOW-to-HIGH

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PAGE MODE READ CYCLE



PAGE-MODE WRITE CYCLE (EARLY WRITE)



= May change in either direction

= May change HIGH-to-LOW

= May change LOW-to-HIGH

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M4027

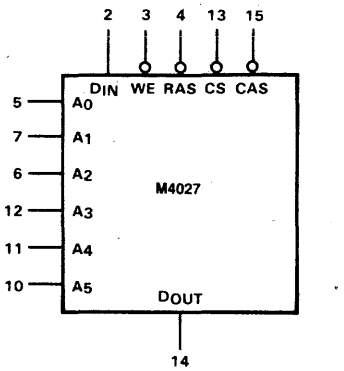
4096 x 1 DYNAMIC RANDOM ACCESS MEMORY

FAIRCHILD ISOPLANAR SILICON GATE MOS

GENERAL DESCRIPTION – The M4027 is a 4096-bit MOS Dynamic Random Access Memory configured as 4096 one-bit words, and which is manufactured using Fairchild's n-channel silicon gate, Isoplanar process. The use of the single-transistor memory cell along with address multiplexing techniques permits the packaging of the M4027 in a standard 16-pin dual in-line package. The use of this package allows construction of highly dense memory systems utilizing widely available automated testing and insertion equipment.

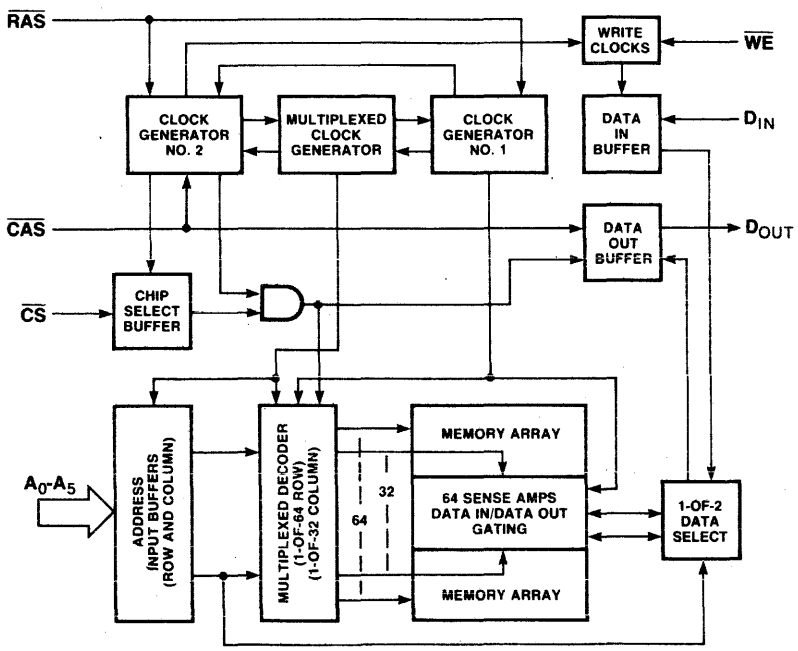
- **INDUSTRY STANDARD 16-PIN DUAL IN-LINE PACKAGE**
- **LOW CAPACITANCE, TTL-COMPATIBLE INPUTS (INCLUDING CLOCKS)**
- **3-STATE TTL-COMPATIBLE OUTPUT**
- **ON-CHIP LATCHES FOR ADDRESSES, CHIP SELECT, DATA INPUT, DATA OUTPUT**
- **ENHANCED PERFORMANCE WITH GATED CAS, RAS-ONLY REFRESH AND PAGE-MODE CAPABILITY**
- **ACCESS TIME: 150 ns TO 300 ns**
- **PAGE MODE ACCESS: AS FAST AS 100 ns**
- **LOW POWER:**
  - **ACTIVE POWER: 470 mW MAXIMUM**
  - **STANDBY POWER: 27 mW MAXIMUM**
  - **STANDBY POWER (INCLUDING REFRESH): 36 mW MAXIMUM**
- **INPUTS PROTECTED AGAINST STATIC CHARGE**
- **STANDARD ±10% SUPPLIES (+12 V, +5 V, and −5 V)**

LOGIC SYMBOL

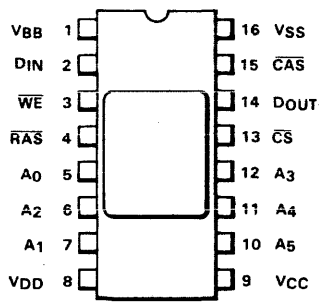


V_{SS} = Pin 16
V_{CC} = Pin 9
V_{DD} = Pin 8
V_{BB} = Pin 1

BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



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464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA, 94042 (415) 962-5011/TWX 910-379-6435

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PIN NAMES

A_n	Address Inputs		
D_{IN}	Data Input	D_{OUT}	Data Output
$\overline{CS}$	Chip Select Input (Active LOW)	V_{CC}	+5 V Power Supply
$\overline{WE}$	Write Enable Input (Active LOW)	V_{SS}	0 V Power Supply
$\overline{RAS}$	Row Address Strobe (Clock) Input (Active LOW)	V_{BB}	−5 V Power Supply
$\overline{CAS}$	Column Address Strobe (Clock) Input (Active LOW)	V_{DD}	+12 V Power Supply

FUNCTIONAL DESCRIPTION

ADDRESSING – The 12 address bits required to decode one-of-4096 cell locations are multiplexed to the six address pins and latched into the on-chip row and column address latches. Row Address Strobe ($\overline{RAS}$) latches the six row address bits onto the chip. Column Address Strobe ($\overline{CAS}$) latches the six column address bits plus Chip Select ($\overline{CS}$) onto the chip. As $\overline{CS}$ is not required until well into the cycle, its decoding time does not add to the system access or cycle time. Since the internal circuitry allows the column information to be externally applied to the chip before it is actually required, the hold time requirements for column address and $\overline{CS}$ are also referenced to $\overline{RAS}$. This gated $\overline{CAS}$ feature allows the system designer to compensate for timing skews that may be encountered in the multiplexing operation. Additional timing margin is gained because column address is not required until $\overline{CAS}$ makes its negative transition. The timing is further simplified by the positive transition of $\overline{CAS}$ not being referenced to the positive transition of $\overline{RAS}$. In fact, $\overline{CAS}$ need not go HIGH until the beginning of the next cycle.

DATA INPUT/OUTPUT – Data to be written into the selected cell is latched into an on-chip register by the combination of $\overline{CAS}$ and Write Enable ($\overline{WE}$) while $\overline{RAS}$ is active. The later of these two signals ($\overline{CAS}$ or $\overline{WE}$), making its negative transition, is the strobe for the Data In register. This permits several options in the write timing. In a write cycle, if $\overline{WE}$ is activated prior to $\overline{CAS}$, Data In (D_{IN}) is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to this signal. If the D_{IN} is not available at $\overline{CAS}$ time or the cycle is a read-write or read-modify-write cycle, then $\overline{WE}$ must be delayed until after $\overline{CAS}$ goes active. In this delayed write mode, the D_{IN} set-up and hold times are referenced to $\overline{WE}$.

At the beginning of a memory cycle, the state of the Data Out latch and buffer depend on the previous memory cycle. Changes in the condition of the Data Out latch are initiated by $\overline{CAS}$. The negative transition of $\overline{CAS}$ causes the Data Output (D_{OUT}) to unconditionally go to its open-circuit state. It will remain open-circuited until after the access time has elapsed. At access time, the D_{OUT} will assume the proper state for the type of cycle performed. If the cycle is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the D_{OUT} latch and buffer will contain the data from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle is an early write cycle ($\overline{WE}$ active LOW before $\overline{CAS}$ goes LOW) and the chip is selected, then D_{OUT} will contain the input data. Once D_{OUT} goes active, it will remain valid until the next negative transition of $\overline{CAS}$. If the cycle is a $\overline{CAS}$-only cycle (no $\overline{RAS}$ signal), then D_{OUT} will assume the open-circuit state. The same is true for normal cycles (both $\overline{RAS}$ and $\overline{CAS}$ present) when the chip is unselected. D_{OUT} remains in the open-circuit state until the next negative transition of $\overline{CAS}$. $\overline{RAS}$-only refresh cycles (no $\overline{CAS}$) have no effect on the D_{OUT}. However, when $\overline{RAS}$-only-refresh cycles are continued for extended periods of time, D_{OUT} may eventually go open-circuit. If the chip is unselected, it will not accept a write command and the D_{OUT} will remain in the open-circuit state.

INPUT/OUTPUT LEVELS – All inputs, including the two address strobes, interface directly with TTL. The high-impedance, low-capacitance input characteristics simplify input driver selection by allowing use of standard logic elements rather than specially designed driver elements. Termination resistors are normally required in a system to prevent ringing and control transition times of input signals due to line inductance and reflections. In high-speed memory systems, transmission line techniques must be employed on the signal lines to achieve optimum system speeds. Series termination may be employed at some degradation of system speed.

The 3-state output buffer is a low impedance to V_{CC} for a logic "1" and a low impedance to V_{SS} for a logic "0". The output resistance to V_{CC} is 420 Ω maximum and 135 Ω typically. The output resistance to V_{SS} is 125 Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may be unpowered without affecting the M4027 refresh operation. This allows all system logic, except the $\overline{RAS}$ timing circuitry and the refresh address logic, to be turned off during battery standby to conserve power.

REFRESH – Refresh of the cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses every 2 ms or less. Any cycle, in which $\overline{RAS}$ occurs, accomplishes a refresh operation. Any read cycle refreshes the selected row, regardless of the state of $\overline{CS}$. A write, read-write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell. Refresh may be accomplished with $\overline{RAS}$-only refresh cycles in which $\overline{RAS}$ is the only active signal. In this case the state of the output is not affected. However, after extended periods of standby using $\overline{RAS}$-only refresh the output may eventually become open-circuit. The output buffer will regain activity with the first cycle in which $\overline{CAS}$ is active.

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PAGE MODE OPERATION – The "Page Mode" feature of the M4027 allows successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is accomplished by strobing the row address into the chip and keeping $\overline{RAS}$ active throughout all successive memory cycles with common row addresses. This page mode operation will not dissipate the power associated with the negative transition of $\overline{RAS}$. The time required to strobe in a new row address is also eliminated, thereby decreasing the access and cycle times. $\overline{CS}$ is operative in page mode cycles just as in normal cycles. It is not necessary that the chip be selected during the first operation of a series of page cycles. Likewise, $\overline{CS}$ can be used to select or deselect any cycle(s) in a series of page cycles. This feature allows the page boundary to be extended beyond the 64-column locations in a single chip. The page boundary can be extended by applying $\overline{RAS}$ to multiple 4K memory blocks and decoding $\overline{CS}$ to select the proper block.

POWER DISSIPATION/STANDBY MODE – Most of the circuitry used in the M4027 is dynamic and draws power only as the result of an address strobe edge. Because power is not drawn during the time the strobe is active, the dynamic power is a function of operating frequency. Typically, the power is 170 mW at 1 μs cycle time with a worst-case power of less than 470 mW at 320 ns cycle time. To reduce the overall system power, $\overline{RAS}$ should be decoded and supplied to only the selected chips. The $\overline{CAS}$ should be supplied to all the chips (to turn off the unselected outputs). Those chips that do not receive $\overline{RAS}$ will not dissipate any power on $\overline{CAS}$ edges, except for that required to turn off the outputs. If $\overline{RAS}$ is decoded and supplied to the selected chips, then the $\overline{CS}$ input of all chips can be at a logic 0. For refresh cycles, however, either $\overline{CS}$ or $\overline{CAS}$ must be held to prevent several wire-OR outputs from turning on with opposing force. Note that the M4027 will dissipate considerably less power when the refresh operation is accomplished with a "$\overline{RAS}$-only" cycle as opposed to a normal $\overline{RAS}/\overline{CAS}$ memory cycle.

POWER UP – The M4027 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, it is recommended that power supplies be sequenced at power up such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

Under system failure conditions in which one or more supplies exceed the specified limits, significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and Data Out to the inactive state.

After power is applied to the device, the M4027 requires several cycles before proper device operation is achieved. The same is true after an interval of time (≥2 ms) has elapsed during which the memory was powered, but not refreshed. Any 8 cycles which perform refresh are adequate for this purpose.

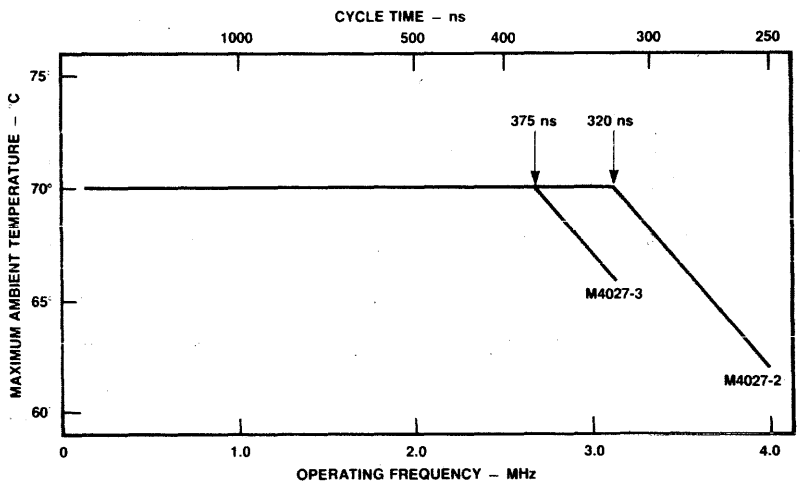


FIG. 1. Maximum Ambient Temperature Versus Cycle Time For Extended Frequency Operation

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ABSOLUTE MAXIMUM RATINGS

Voltage of any pin relative to V_{BB}	−0.5 V to +20.0 V
Voltage of V_{DD} and V_{CC} relative to V_{SS}	−1.0 V to +15 V
Voltage on V_{BB} relative to V_{SS} when $V_{DD} > V_{SS}$	0 V
Operating Temperature (Ambient)	0°C to 70°C
Storage Temperature (Ambient)	−65°C to +150°C
Short Circuit Output Current	50 mA
Power Dissipation	1W

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

DC REQUIREMENTS: T_A = 0°C to 70°C (See Notes 1 and 2)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12	13.2	V	
V_{CC}	Supply Voltage	V_{SS}	5.0	V_{DD}	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{BB}	Supply Voltage	−4.5	−5.0	−5.5	V	
V_{IHC}	Input HIGH Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	2.4		7.0	V	
V_{IH}	Input HIGH Voltage, all inputs except $\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$	2.2		7.0	V	
V_{IL}	Input LOW Voltage, all inputs	−1.0		0.8	V	

DC ELECTRICAL CHARACTERISTICS: Over Full Range of Voltage and Temperature

SYMBOL	PARAMETER (See Notes 1 and 2)		MIN	TYP	MAX	UNITS	NOTES
I_{DD}	Average V_{DD} Current	Normal Operation			35	mA	3
		Standby			2.0	mA	
		Refresh			25	mA	
		Page Mode				mA	
I_{CC}	Average V_{CC} Current	Normal Operation				mA	4
		Standby/Refresh	−10		10	μA	
I_{BB}	Average V_{BB} Current				150	μA	
V_{OH}	Output HIGH Voltage		2.4			V	5
V_{OL}	Output LOW Voltage				0.4	V	5
I_{IN}	Input Leakage Current (any input)		−10		10	μA	6
I_{OUT}	Output Leakage Current		−10		10	μA	7
C_{IN1}	Input Capacitance, A_0−A_5, D_{IN}, $\overline{CS}$			4.0	5.0	pF	8
C_{IN2}	Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$			8.0	10	pF	8
C_{OUT}	Output Capacitance, D_{OUT}			5.0	7.0	pF	8

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RECOMMENDED AC OPERATING CONDITIONS: Over Full Range of Voltage and Temperature

SYMBOL	PARAMETER (See Notes 1, 2, and 9)	M4027-2		M4027-3		M4027-4		M4027-5		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	320		375		375		430		ns	10
t_{RWC}	Read-Modify-Write Cycle Time	330		420		480		615		ns	10
t_{PC}	Page Mode Cycle Time	170		225		285		325		ns	
t_{RAC}	Access Time from $\overline{RAS}$		150		200		250		300	ns	11, 13
t_{CAC}	Access Time from $\overline{CAS}$		100		135		165		165	ns	12, 13
t_{OFF}	Output Buffer Turn-off Delay		40		50		60		80	ns	14
t_{RP}	$\overline{RAS}$ Precharge Time	100		120		120		125		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10K	200	10K	250	10K	300	10K	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	100		135		165		165		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	100		135		165		165		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	65	35	85	80	135	ns	15
t_{ASR}	Row Address Set-up Time	0		0		0		0		ns	
t_{RAH}	Row Address Hold Time	20		25		35		80		ns	
t_{ASC}	Column Address Set-up Time	−10		−10		−10		0		ns	
t_{CAH}	Column Address Hold Time	45		55		75		80		ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	95		120		160		215		ns	
t_{CSC}	Chip Select Set-up Time	−10		−10		−10		0		ns	
t_{CH}	Chip Select Hold Time	45		55		75		100		ns	
t_{CHR}	Chip Select Hold Time Referenced to $\overline{RAS}$	95		120		160		215		ns	
t_T	Transition Time (rise and fall)	3	35	3	50	3	50	5	50	ns	9
t_{RCS}	Read Command Set-up Time	0		0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		0		ns	
t_{WCH}	Write Command Hold Time	45		55		75		130		ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		120		160		215		ns	
t_{WCS}	Write Command Set-up Time	0		0		0		0		ns	16
t_{WP}	Write Command Pulse Width	45		55		75		130		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	50		70		85		130		ns	17
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	50		70		85		130		ns	17
t_{DS}	Data In Set-up Time	0		0		0		0		ns	18
t_{DH}	Data In Hold Time	45		55		75		130		ns	18
t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	95		120		160		215		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		0		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Page-mode)	60		80		110		150		ns	
t_{RF}	Refresh Period		2.0		2.0		2.0		2.0	ms	
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay (RMW)	60		80		90		100		ns	19
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay (RMW)	110		145		175		235		ns	19
t_{DOH}	Data Out Hold Time	10		10		10		10		μs	

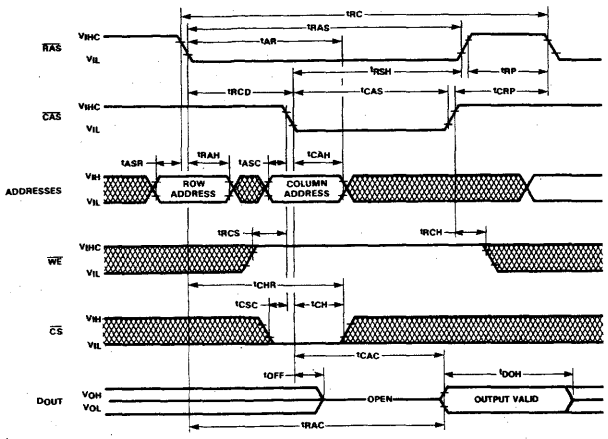
NOTES:

1. The ambient temperature, (T_A) is specified here for operation at frequencies up to that frequency determined by the minimum cycle time. Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met. See derating curve in Figure 1.
2. All voltages are referenced to V_{SS} = 0 V.
3. I_{DD} depends on frequency of operation. Maximum current is measured at the fastest cycle rate. I_{DD} current for page mode operation depends on the number of page cycles because of the $\overline{RAS}$ pulse edges. The level specified assumes 30 page cycles with minimum t_{CAS} and t_{CP}.
4. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only. During readout of HIGH level data, V_{CC} is connected through a low impedance (100 Ω typ) to Data Out. At other times I_{CC} consists of leakage currents only.
5. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of reducing power in the standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the $V_{OH(min)}$ specification is not guaranteed in this mode. V_{OH} is measured with I_{OUT} = −5.0 mA and V_{OL} is measured with I_{OUT} = 3.2 mA.
6. All device pins at 0 V except V_{BB} which is at −5 V and the pin under test which is at +10 V.
7. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic "1". 0 V ≤ V_{OUT} ≤ +10 V.
8. Capacitance measured with Boonton Meter of effective capacitance calculated from the equation: C = IΔt/Δ V with current equal to a constant 20 mA, and Δ V = 3 V.
9. V_{IHC}(min) or V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}. AC measurements assume t_T = 5 ns.
10. The specifications for $t_{RC(min)}$, $t_{RWC(min)}$ and $t_{PC(min)}$ are used only to indicate cycle time at which proper operation over full temperature range (0°C ≤ T_A ≤ 70°C) is assured. See Note 1 and the derating curve in Fig.1.
11. Assumes that $t_{RCD} \leq t_{RCD(max)}$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
12. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
13. Measured with a load equivalent to two TTL loads and 100 pF.
14. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
15. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
16. t_{WCS} is not a restrictive operating parameter but is included as an electrical characteristic only. If $t_{WCS} \geq t_{WCS(min)}$, the cycle is an early write cycle and the Data Out pin will contain the data written into the selected cell.
17. The parameters t_{RWL} and t_{CWL} reference $\overline{WE}$ (for a read-modify-write cycle), to either $\overline{RAS}$ or $\overline{CAS}$ repectively, whichever is the first to go HIGH.
18. t_{DS} and t_{DH} are referenced to the leading edge of $\overline{CAS}$ in early write cycles, and to the leading edge of $\overline{WE}$ in delayed write or read-modify-write cycles.
19. t_{RWD} and t_{CWD} are not restrictive operating parameters but are included in the data sheet as electrical characteristics only:
    If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min). the data out latch will contain the data read from the selected cell.
    If t_{CWD} does not meet these constraints, then the data out latch will contain indeterminate data at the access time.

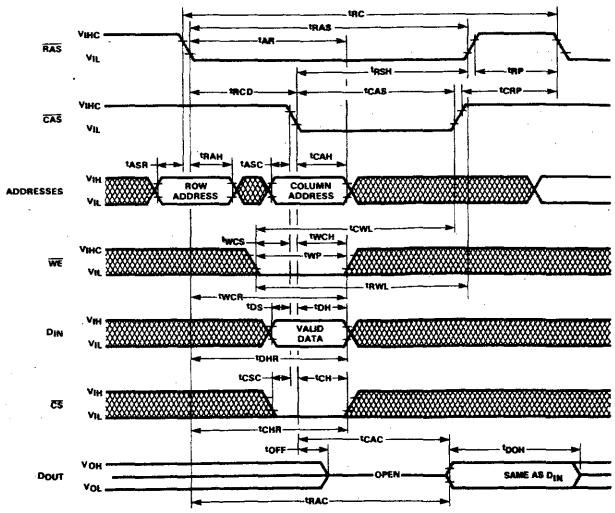
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TIMING DIAGRAMS

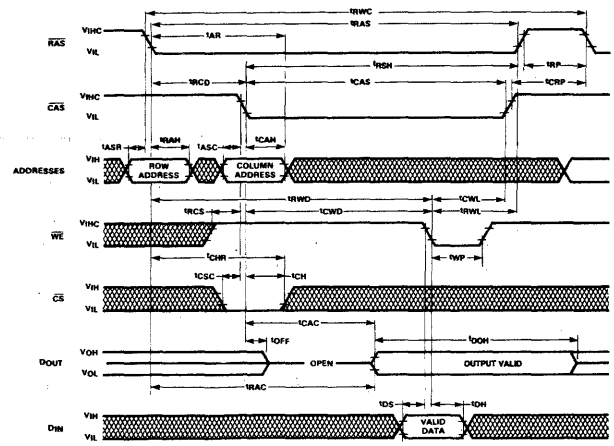
READ CYCLE



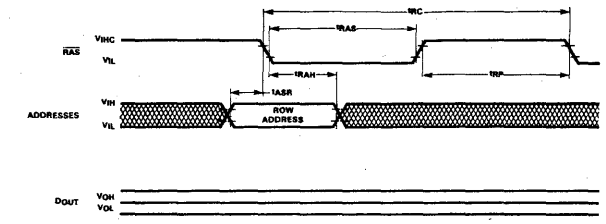
WRITE CYCLE (EARLY-WRITE)



READ-MODIFY-WRITE CYCLE



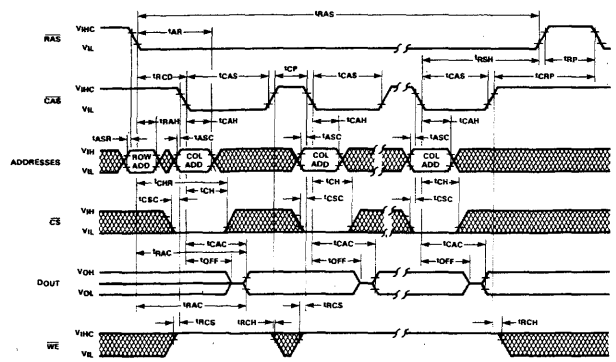
"$\overline{RAS}$ ONLY" REFRESH CYCLE



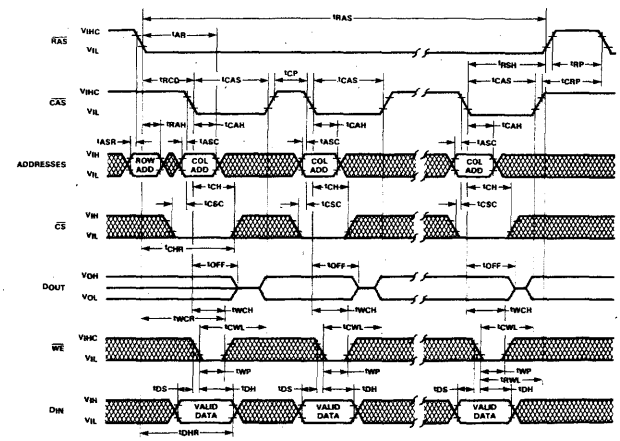
*Read-modify-write cycle time =

$$t_{RCL} + t_{RAC} + t_{MOD} + t_{CWL} + t_{CRL} + t_{RP} + 3\,t_f + t_r.$$

PAGE-MODE-READ CYCLE



PAGE-MODE-WRITE CYCLE



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ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE	TEMPERATURE RANGE	ORDER CODE
M4027-2	150 ns	Plastic	0° to +70°C	M40272PC
		Ceramic	0° to +70°C	M40272DC
		Ceramic	−55°C to +85°C	M40272DL
		Flatpak	0° to +70°C	M40272FC
		Flatpak	−55° to +85°C	M40272FL
M4027-3	200 ns	Plastic	0° to +70°C	M40273PC
		Ceramic	0° to +70°C	M40273DC
		Ceramic	−55° to +85°C	M40273DL
		Flatpak	0° to +70°C	M40273FC
		Flatpak	−55° to +85°C	M40273FL
M4027-4	250 ns	Plastic	0° to +70°C	M40274PC
		Ceramic	0° to +70°C	M40274DC
		Ceramic	−55° to +85°C	M40274DL
		Flatpak	0° to +70°C	M40274FC
		Flatpak	−55° to +85°C	M40274FL
M4027-5	300 ns	Plastic	0° to +70°C	M40275PC
		Ceramic	0° to +70°C	M40275DC
		Ceramic	−55° to +85°C	M40275DL
		Flatpak	0° to +70°C	M40275FC
		Flatpak	−55° to +85°C	M40275FL

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Manufactured under one of the following U.S. Patents: 2981877, 3015048, 3064167, 3108359, 3117260; other patents pending.

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ECL ISOPLANAR MEMORY F10470

4096 × 1-BIT FULLY DECODED RANDOM ACCESS MEMORY

FAIRCHILD VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION – The F10470 is a 4096-bit Read/Write Random Access Memory organized 4096 words by one bit. It is designed for high speed scratch pad, control and buffer storage applications. The Device includes full address decoding on the chip, has separate Data In and non-invertered Data Out lines, and active LOW Chip Select lines. They are compatible with F10K and uncompensated 10K ECL families and include on-chip voltage compensation for improved noise margin.

The F10470 is packaged in a hermetic ceramic 18-pin dual in-line package and is specified for operation over the temperature range 0°C to 75°C.

- **COMPATIBLE WITH F10K AND UNCOMPENSATED 10K ECL LOGIC**
- **TYPICAL READ ACCESS TIME – 30 ns**
- **TYPICAL CHIP SELECT ACCESS TIME – 10 ns**
- **ORGANIZED 4096 WORDS X 1 BIT**
- **OPEN EMITTER OUTPUT FOR EASE OF MEMORY EXPANSION**
- **POWER DISSIPATION 0.25 mW/BIT**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**
- **REPLACES FOUR 1024 BY ONE RAMs**

PIN NAMES

$\overline{CS}$	Chip Select Input
$A_0 - A_{11}$	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

L = LOW Voltage Levels = −1.7 V
H = HIGH Voltage Levels = −0.9 V
(Nominal values)
X = Don't Care

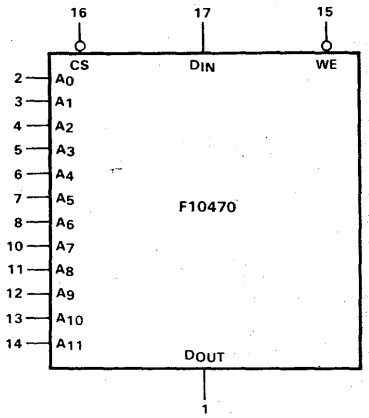
TABLE 1 – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	OPEN EMITTER	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

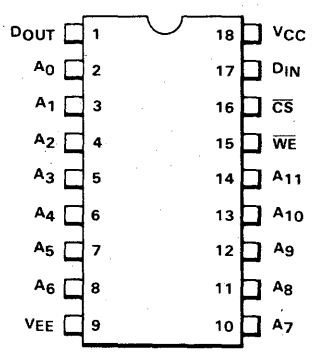
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{EE} Pin Potential to Ground Pin	−7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	−30 mA to +0.1 mA

LOGIC SYMBOL



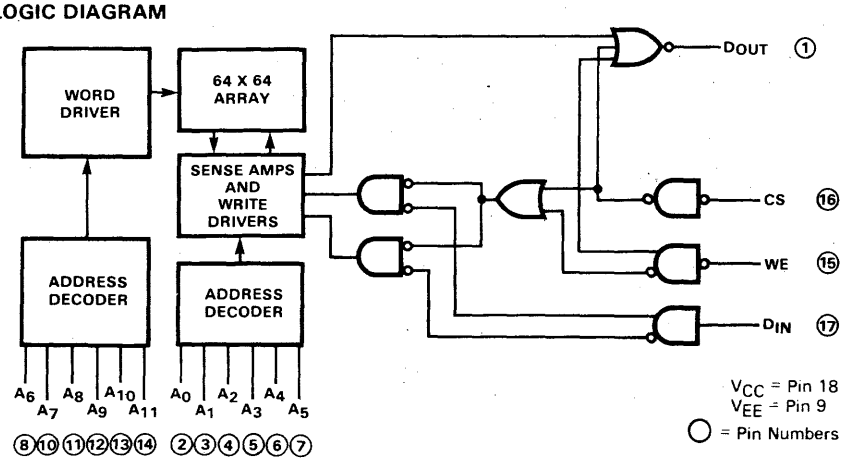
V_{CC} = Pin 18
V_{EE} = Pin 9

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 18
V_{EE} = Pin 9
○ = Pin Numbers

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464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA, 94042 (415) 962-5011/TWX 910-379-6435

FAIRCHILD

FUNCTIONAL DESCRIPTION – The F10470 is a fully decoded 4096-bit Random Access Memoy organized 4096 words by one bit. Word selection is achieved by means of a 12-bit address, A_0 thru A_{11}.

One chip Select input is provided for memory array expansion up to 8192 words without the need for external decoding. For larger memories, the fast Chip Select access time permits the decoding of Chip Select, $\overline{CS}$, from the address withoutincreasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable, $\overline{WE}$ (pin 15). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT} and is non-inverted.

An unterminated emitter-follower output is provided on the F10470 to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F10470s can be tied together. In other applications the wired-OR is not used. In either case an external 50 Ω pull down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is off.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE
	MIN	TYP	MAX	See Note 4
F10470	−5.46 V	−5.2 V	−4.94 V	0°C to 75°C

DC CHARACTERISTICS: V_{EE} = −5.2 V, Output Load = 50 Ω and 30 pF to −2.0 V, T_A = 0°C to 75°C (Note 4)

SYMBOL	CHARACTERISTIC	B LIMIT	TYP (Note 3)	A LIMIT	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	−1000		−840	mV	0°C	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to −2.0 V
		−960		−810		+25°C		
		−900		−720		+75°C		
V_{OL}	Output Voltage LOW	−1870		−1665	mV	0°C		
		−1850		−1650		+25°C		
		−1830		−1625		+75°C		
V_{OHC}	Output Voltage HIGH	−1020			mV	0°C	$V_{IN} = V_{IHB}$ or V_{ILA}	
		−980				+25°C		
		−920				+75°C		
V_{OLC}	Output Voltage LOW			−1645	mV	0°C		
				−1630		+25°C		
				−1605		+75°C		
V_{IH}	Input Voltage HIGH	−1145		−840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		−1105		−810		+25°C		
		−1045		−720		+75°C		
V_{IL}	Input Voltage LOW	−1870		−1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs	
		−1850		−1475		+25°C		
		−1830		−1450		+75°C		
I_{IH}	Input Current HIGH			220	μA	0 to +75°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW, $\overline{CS}$	0.5		170	μA	+25°C	$V_{IN} = V_{ILB}$	
	All others	−50						
I_{EE}	Power Supply Current (Pin 8)		−180		mA	+75°C	All Inputs and Outputs Open	
			−200			0°C		

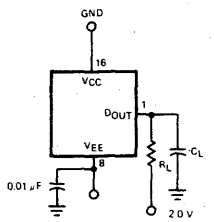
NOTES:
1. Conditions for testing, not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified Limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{EE} = −5.2 V, T_A = 25°C and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C/Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET:
   The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.

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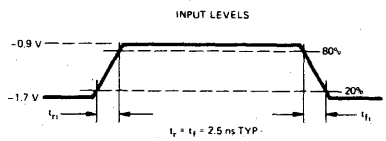
AC CHARACTERISTICS: V_{EE} = −5.2 V ±5%, Output Load = 50 Ω, 30 pF to −2.0 V, T_A = 0°C to 75°C

SYMBOL	PARAMETER	MIN	TYP (Note 3)	MAX	UNITS	CONDITIONS
t_{ACS}	Chip Select Access Time		10		ns	Fig 1a and b measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} or V_{OH})
t_{RCS}	Chip Select Recovery Time		10		ns	
t_{AA}	Address Access Time		30		ns	
t_W	Write Pulse Width (to Guarantee writing)		25		ns	
t_{WSD}	Data Sep-up Time Prior to Write		1		ns	
t_{WHD}	Data Hold Time After Write		1			
t_{WSA}	Address Seo-up Time Prior to Write		5		ns	
t_{WHA}	Address Hold Time After Write		1		ns	
t_{WSCS}	Chip Select Set-up Time Prior to Write		1		ns	Fig. 2 measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})
t_{WHCS}	Chip Select Hold Time After Write		1		ns	
t_{WS}	Write Disable Time		6		ns	
t_{WR}	Write Recovery Time		15		ns	
t_r	Output Rise Time		5		ns	Measured between 20% and 80% points. (Fig. 1a)
t_f	Output Fall Time		5		ns	
C_{IN}	Input Pin Capacitance		4		pF	Measure with a Pulse Technique
C_{OUT}	Output Pin Capacitance		7		pF	

LOADING CONDITIONS



INPUT LEVELS



All Timing Measurements Referenced to 50% of Input Levels

C_L = 30 pF including Jig and Stray Capacitance

R_L = 50 Ω Termination

READ MODE PROPAGATION DELAY FROM CHIP SELECT

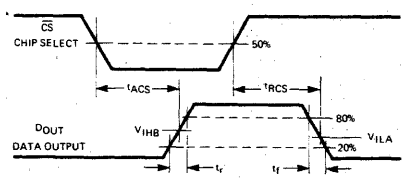


Fig. 1a

WRITE MODE

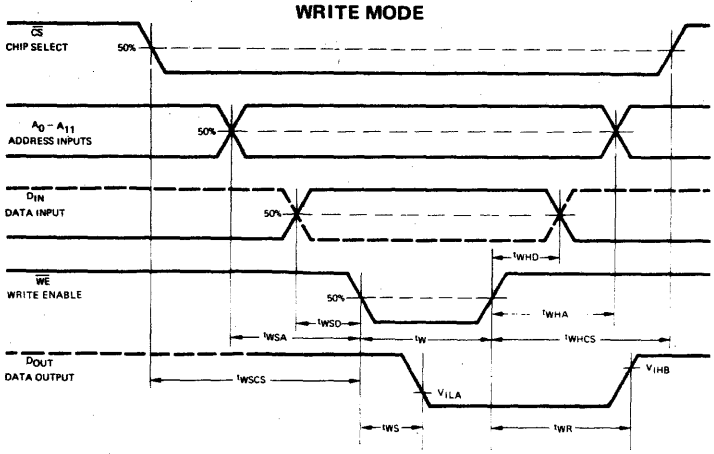


Fig. 2

READ MODE PROPAGATION DELAY FROM ADDRESS

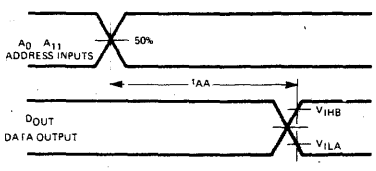


Fig. 1b

NOTE: Timing Diagram represents one solution which results in an optimum cycle time.
Timing may be changed to fit various applications as long as the worst case limits are not violated.

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ECL ISOPLANAR MEMORY
F10415 / F10415A / F100415
1024 x 1-BIT FULLY DECODED RANDOM ACCESS MEMORIES
FAIRCHILD VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION — These devices are 1024-bit Read/Write Random Access Memories organized 1024 words by one bit. They are designed for high speed scratch pad, control and buffer storage applications. Both include full address decoding on the chip, have separate Data In and non-inverted Data Out lines, and active LOW Chip Select lines.

- **TYPICAL READ ACCESS TIME**
  F10415 – 25 ns
  F10415A and F100415 – 12 ns
- **TYPICAL CHIP SELECT ACCESS TIME**
  F10415 – 7 ns
  F10415A and 100415 – 5 ns
- **ORGANIZED 1024 WORDS X 1 BIT**
- **OPEN EMITTER OUTPUT FOR EASE OF MEMORY EXPANSION**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**

PIN NAMES

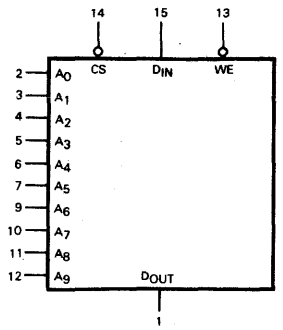
$\overline{CS}$	Chip Select Input
A_0 to A_9	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

TABLE 1 –
TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	OPEN EMITTER	
H	X	X	L	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	L	WRITE "1"
L	H	X	D_{OUT}	READ

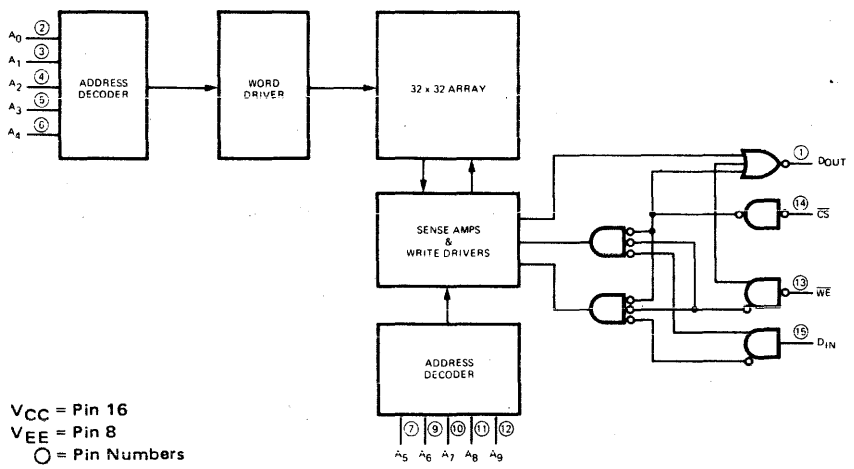
L = LOW Voltage Levels = −1.7 V
H = HIGH Voltage Levels = −0.9 V
(Nominal values)
X = Don't Care

LOGIC SYMBOL



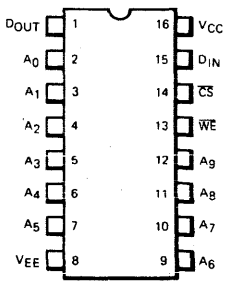
V_{CC} = Pin 16
V_{EE} = Pin 8

LOGIC DIAGRAM



V_{CC} = Pin 16
V_{EE} = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

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FUNCTIONAL DESCRIPTION – The F10415, F10415A and F100415 are fully decoded 1024-bit Read/Write Random Access Memories organized 1024 words by one bit. Bit selection is acheived by means of a 10-bit address, A_0 to A_9. One Chip Select input is provided for memory array expansion up to 2048 words without the need for external decoding. For larger memories, the fast chip select access time permits the decoding of Chip Select ($\overline{CS}$) from the address without increasing address access time. The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$). With $\overline{WE}$ and $\overline{CS}$ held LOW, the data at D_{in} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and $\overline{CS}$ held LOW. Data in the specified location is presented at D_{OUT} and is non-inverted.

An unterminated emitter-follower output is provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F10415s, F10415As or 100415s can be tied together. In other applications the wired-OR is not used. In either case an external 50 Ω pull down resistor to –2 V or an equivalent network must be used to provide a LOW at the output when it is off.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{EE} Pin Potential to Ground Pin	–7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	–30 mA to +0.1 mA

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE
	MIN	TYP	MAX	See Note 4
F10415DC, F10415ADC	–5.46 V	–5.2 V	–4.94 V	0°C to 75°C
F100415DC	–5.7 V	–4.5 V	–4.2 V	0°C to 85°C

10415 and 10415A Only
DC CHARACTERISTICS: V_{EE} = –5.2 V, Output Load = 50 Ω and 30 pF to –2.0 V, T_A = 0°C to 75°C (Note 4)

SYMBOL	CHARACTERISTIC	B LIMIT	TYP (Note 3)	A LIMIT	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	–1000		–840	mV	0°C	V_{IN} = V_{IHA} or V_{ILB}	
		–960		–810		+25°C		
		–900		–720		+75°C		
V_{OL}	Output Voltage LOW	–1870		–1665	mV	0°C		
		–1850		–1650		+25°C		
		–1830		–1625		+75°C		Loading is 50 Ω to –2.0 V
V_{OHC}	Output Voltage HIGH	–1020			mV	0°C	V_{IN} = V_{IHB} or V_{ILA}	
		–980				+25°C		
		–920				+75°C		
V_{OLC}	Output Voltage LOW			–1645	mV	0°C		
				–1630		+25°C		
				–1605		+75°C		
V_{IH}	Input Voltage HIGH	–1145		–840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		–1105		–810		+25°C		
		–1045		–720		+75°C		
V_{IL}	Input Voltage LOW	–1870		–1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs	
		–1850		–1475		+25°C		
		–1830		–1450		+75°C		
I_{IH}	Input Current HIGH			220	µA	0 to +75°C	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW, $\overline{CS}$	0.5		170	µA	+25°C	V_{IN} = V_{ILB}	
	All others	–50						
I_{EE}	Power Supply Current		–90		mA	+75°C	All Inputs and Outputs Open	
	(Pin 8)	–150	–105			0°C		

NOTES:
1. Conditions for testing, not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified Limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{EE} = –5.2 V, T_A = 25°C and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C/Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET:
   The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.

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100415 Only

DC CHARACTERISTICS: V_{EE} = −4.5V, V_{CC} = GND, T_A = 0°C to +85°C (Note A)

SYMBOL	CHARACTERISTIC	LIMITS (Note 6) B	LIMITS (Note 6) TYP (Note 3)	LIMITS (Note 6) A	UNITS	CONDITIONS	
V_{OH}	Output Voltage HIGH	−1025	−955	−880	mV	V_{IN} = V_{IHA} or V_{ILB}	Loading is 50 Ω to −2.0 V
V_{OL}	Output Voltage LOW	−1810	−1705	−1620	mV		
V_{OHC}	Output Voltage HIGH	−1035			mV	V_{IN} = V_{IHB} or V_{ILA}	
V_{OLC}	Output Voltage LOW			−1610	mV		
V_{IH}	Input Voltage HIGH	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input Voltage LOW	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IH}	Input Current HIGH			220	μA	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW, $\overline{CS}$ All others	0.5 −50		170	μA	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	−150	−105		mA	All Inputs and Output open	

AC CHARACTERISTICS: V_{EE} = −5.2 V ± 5%, Output Load = 50 Ω, 30 pF to −2.0 V, T_A = 0°C to 75°C

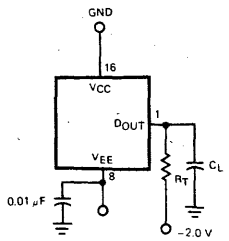
SYMBOL	PARAMETER	F10415ADC/100415 MIN	F10415ADC/100415 TYP (Note 3)	F10415ADC/100415 MAX	F10415DC MIN	F10415DC TYP (Note 3)	F10415DC MAX	UNITS	CONDITIONS
READ MODE									Fig 1a & b measured at
t_{ACS}	Chip Select Access Time		5			7	10	ns	50 % of inpur to valid
t_{RCS}	Chip Select Recovery Time		5			7	10	ns	output (V_{ILA} for V_{OL}
t_{AA}	Address Access Time		12	20		25	35	ns	or V_{IHB} for V_{OH})
WRITE MODE									
t_W	Write Pulse Width (to Guarantee writing)	12	9		25	20		ns	F10415A t_{WSA} = 8 ns; F10415 t_{WSA} = 20 ns
t_{WSD}	Data Set-up Time Prior to Write		0		5	0		ns	
t_{WHD}	Data Hold Time After Write		0		5	0			
t_{WSA}	Address Set-up Time Prior to Write		5		8	5		ns	F10415A t_W = 12 ns; F10415 t_W = 25 ns
t_{WHA}	Address Hold Time After Write		0		4	1		ns	
t_{WSCS}	Chip Select Set-up Time Prior to Write		0		5	0		ns	Fig. 2 measured at 50 % of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})
t_{WHCS}	Chip Select Hold Time After Write		0		5	0		ns	
t_{WS}	Write Disable Time		5			7	10	ns	
t_{WR}	Write Recovery Time		7			7	10	ns	
RISE TIME AND FALL TIME - 10415/10415A ONLY									
t_r	Output Rise Time		5			5		ns	
t_f	Output Fall Time		5			5		ns	
RISE TIME AND FALL TIME - 100415 Only									Measured between 20 % and 80 % points. (Fig. 1a)
t_r	Output Rise Time		4.5					ns	
t_f	Output Fall Time		5.5					ns	
CAPACITANCE									
C_{IN}	Input Pin Capacitance		4	5		4	5	pF	Measure with a Pulse
C_{OUT}	Output Pin Capacitance		7	8		7	8	pF	Technique

*Note: The F10415A Ac limits are preliminary

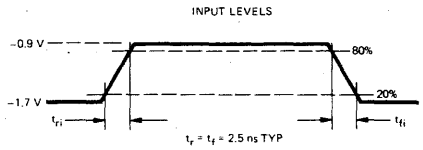
Fairchild Semiconductor MEMORY

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LOADING CONDITIONS



INPUT LEVELS



All Timing Measurements Referenced to 50% of Input Levels

C_L = 30 pF including Jig and Stray Capacitance

R_T = 50 Ω Termination of Scope

READ MODE PROPAGATION DELAY FROM CHIP SELECT

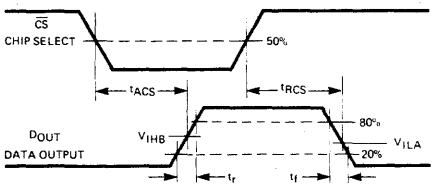


Fig. 1a

READ MODE PROPAGATION DELAY FROM ADDRESS

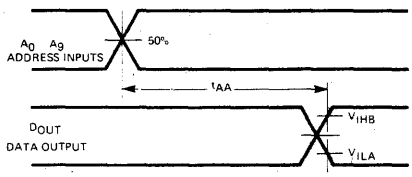


Fig. 1b

WRITE MODE

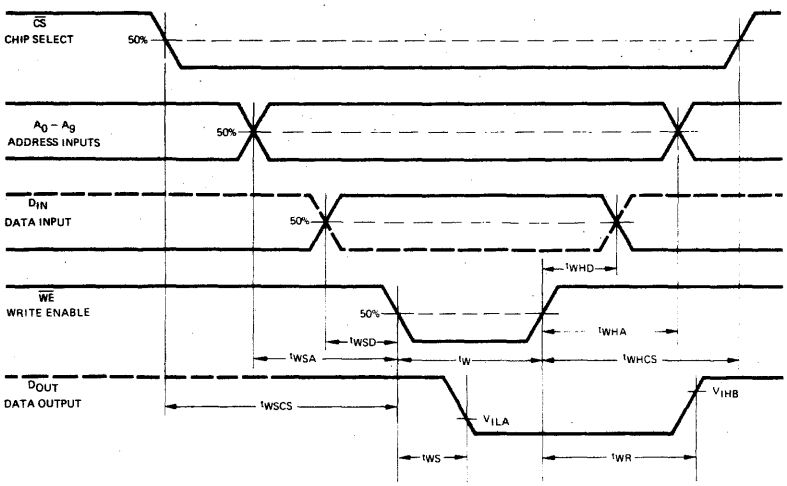


Fig. 2

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

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93422 • 93L422

TTL ISOPLANAR MEMORY

256 x 4-BIT FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION – The 93422 is a 1024-bit Read/Write Access Memory organized 256 words by four bits per word. The 93422 has 3-state outputs, and is designed primarily for buffer control storage and high performance main memory applications. The device has a typical address access time of 30 ns.

- ISOPLANAR TECHNOLOGY
- ORGANIZED – 256 WORDS X 4 BITS
- 3-STATE OUTPUTS
- STANDARD 22-PIN DIP
- TWO CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION
- 0.475 mW/BIT TYP
- TYP READ ACCESS TIME – 30 ns

PIN NAMES

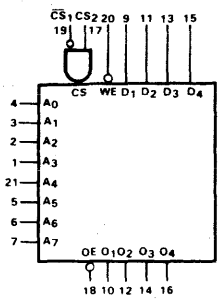
$A_0 - A_7$	Address Inputs
$D_1 - D_4$	Data Inputs
$\overline{CS}_1$, CS_2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$O_1 - O_4$	Data Outputs
$\overline{O}_E$	Output Enable

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	−0.5 V to +5.50 V
Output Current (dc)	+20 mA

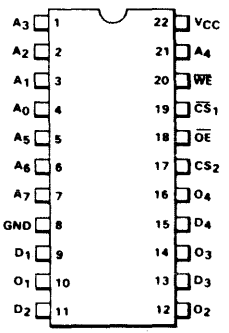
*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

LOGIC SYMBOL

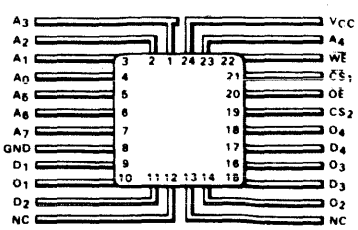


V_{CC} = Pin 22
GND = Pin 8

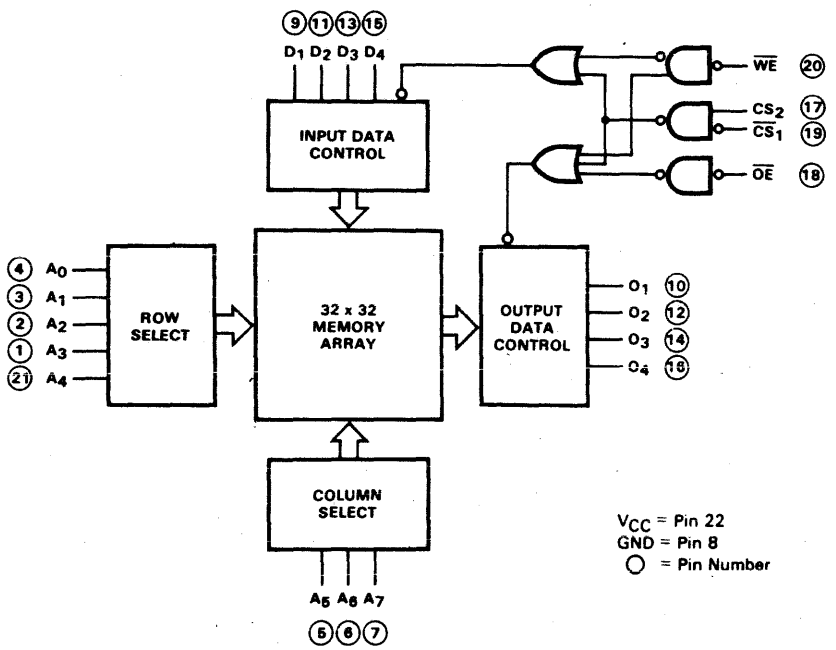
CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



LOGIC DIAGRAM



V_{CC} = Pin 22
GND = Pin 8
○ = Pin Number

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464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA, 94042 (415) 962-5011/TWX 910-379-6435

FAIRCHILD

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FUNCTIONAL DESCRIPTION – The 93422 is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 thru A_7. Two Chip Select inputs are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of Chip Select, CS, from the address without increasing address access time. The read and write operations are controlled by the state of the active LOW Write Enable, WE (pin 20). With WE held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, WE is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT}.

TRUTH TABLE

INPUTS					OUTPUTS	
$\overline{OE}$ PIN 18	$\overline{CS_1}$ PIN 19	CS_2 PIN 17	$\overline{WE}$ PIN 20	$D_1 - D_4$ PINS 9, 11,13, 15	93422 3-STATE	MODE
X	H	X	X	X	HIGH Z	Not Selected
X	X	L	X	X	HIGH Z	Not Selected
L	L	H	H	X	$O_1 - O_4$	Read Stored Data
X	L	H	L	L	HIGH Z	Write "0"
X	L	H	L	H	HIGH Z	Write "1"
H	L	H	H	X	HIGH Z	Output Disabled
H	L	H	L	L	HIGH Z	Write "0" (Output Disabled)
H	L	H	L	H	HIGH Z	Write "1" (Output Disabled)

H = HIGH Voltage, L = LOW Voltage, X = Don't Care (HIGH or LOW); HIGH Z = High Impedance.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93422XC, 93L422XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93422XM, 93L422XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC		LIMITS MIN	LIMITS TYP (Note 3)	LIMITS MAX	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage			0.3	0.45	V	V_{CC} = MIN, I_{OL} = 8 mA	
V_{IH}	Input HIGH Voltage		2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage			1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current			−150	−300	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
V_{CD}	Input Diode Clamp Voltage			−10	−1.5	V	V_{CC} = MAX, IN = −10 mA	
I_{OFF}	Output Current (HIGH Z)				50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V	
					−50		V_{CC} = MAX, V_{OUT} = 0.5 V	
V_{OH}	Output HIGH Voltage		2.4			V	V_{CC} = MIN, I_{OH} = −5.2 mA	
I_{OS}	Output Current Short Circuit to Ground				−70	mA	V_{CC} = MAX, Note 7	
I_{CC}	Power Supply Current	93422XC		95	130	mA	T_A = +75°C	V_{CC} = MAX, All Inputs and Outputs Open
		93422XC			155		T_A = 0°C	
		93422XM			120		T_A = +125°C	
		93422XM			170		T_A = −55°C	
I_{CC}	Power Supply Current	93L422XC		55	75	mA	T_A = +75°C	
		93L422XC		60	80		T_A = 0°C	
		93L422XM		50	70		T_A = +125°C	
		93L422XM		65	90		T_A = −55°C	

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93422 AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

SYMBOL	CHARACTERISTIC	93422XC			93422XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Time		20	30		20	45		
t_{ZRCS}	Chip Select to HIGH Z		20	30		20	45	ns	See Test Circuit
t_{AOS}	Output Enable Time		20	30		20	45		and Waveforms
t_{ZROS}	Output Enable to HIGH Z		20	30		20	45		
t_{AA}	Address Access Time		30	45		40	60		
WRITE MODE	DELAY TIMES								
t_{ZWS}	Write Disable to HIGH Z		20	35		20	45	ns	
t_{WR}	Write Recovery Time		25	40		25	50		
	INPUT TIMING REQUIREMENTS								See Test Circuit
t_W	Write Pulse Width (to guarantee write)	30	20		40	30			and Waveforms
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0			
t_{WSA}	Address Set-Up Time	10	0		10	0		ns	
t_{WHA}	Address Hold Time	5	0		10	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0			
t_{WHCS}	Chip Select Hold Time	5	0		10	0			
C_I	Input Pin Capacitance		3	5		3	5	pF	Measure with
C_O	Output Pin Capacitance		5	8		5	8		Pulse Technique

93L422 AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

SYMBOL	CHARACTERISTIC	93L422XC*			93L422XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Time		20	35		20	45		
t_{ZRCS}	Chip Select to HIGH Z		20	35		20	45	ns	See Test Circuit
t_{AOS}	Output Enable Time		20	35		20	45		and Waveforms
t_{ZROS}	Output Enable to HIGH Z		20	35		20	45		
t_{AA}	Address Access Time		45	60		45	75		
WRITE MODE	DELAY TIMES								
t_{ZWS}	Write Disable to HIGH Z		20	40		20	45	ns	
t_{WR}	Write Recovery Time		25	45		25	50		
	INPUT TIMING REQUIREMENTS								See Test Circuit
t_W	Write Pulse Width (to guarantee write)	45	30		55	35			and Waveforms
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0			
t_{WSA}	Address Set-Up Time	10	0		10	0		ns	
t_{WHA}	Address Hold Time	5	0		10	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0			
t_{WHCS}	Chip Select Hold Time	5	0		10	0			
C_I	Input Pin Capacitance		3	5		3	5	pF	Measure with
C_O	Output Pin Capacitance		5	8		5	8		Pulse Technique

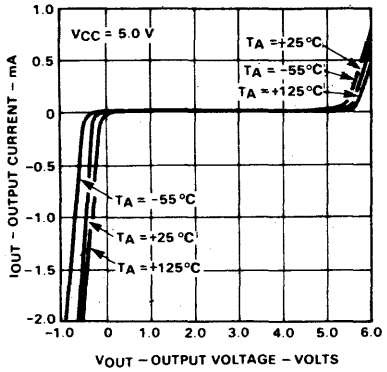
NOTES:

1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

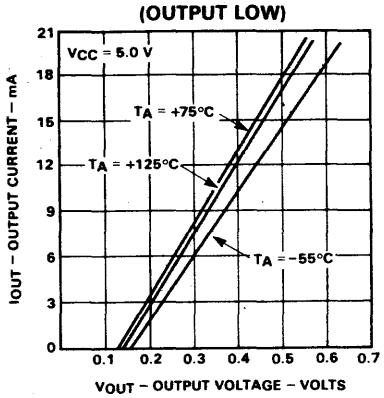
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TYPICAL ELECTRICAL CHARACTERISTIC CURVES

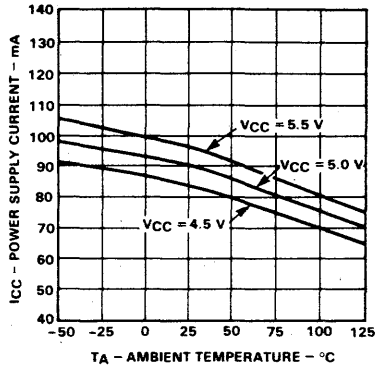
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH Z STATE) 93422 Only



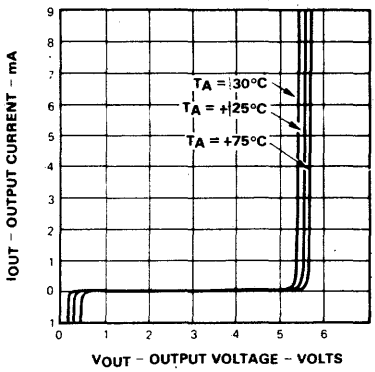
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



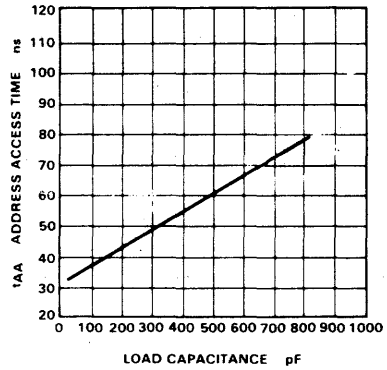
POWER SUPPLY CURRENT VERSUS TEMPERATURE



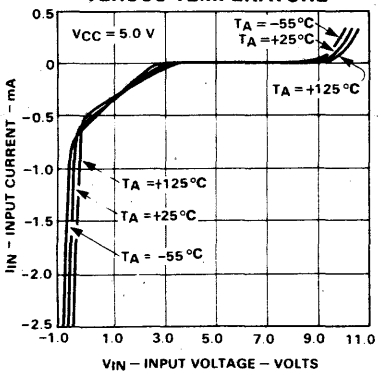
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH Z STATE)



ADDRESS ACCESS TIME VERSUS LOAD CAPACITANCE

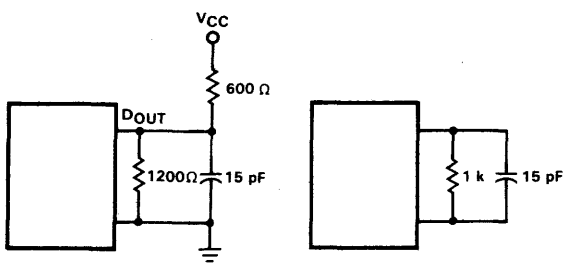


INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE



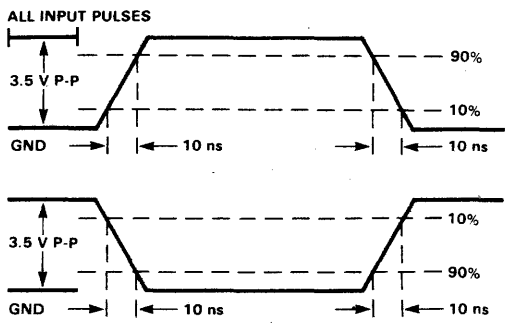
AC TEST LOAD AND WAVEFORM

LOADING CONDITIONS



LOAD A LOAD B

INPUT PULSES

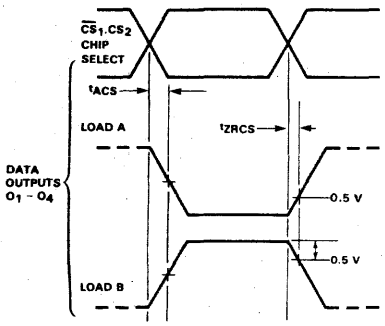


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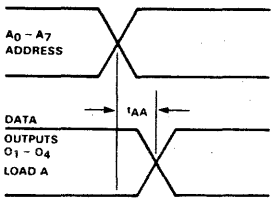
AC TEST WAVEFORMS (Cont'd)

READ MODE

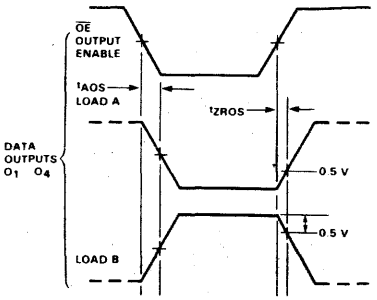
PROPAGATION DELAY FROM CHIP SELECT



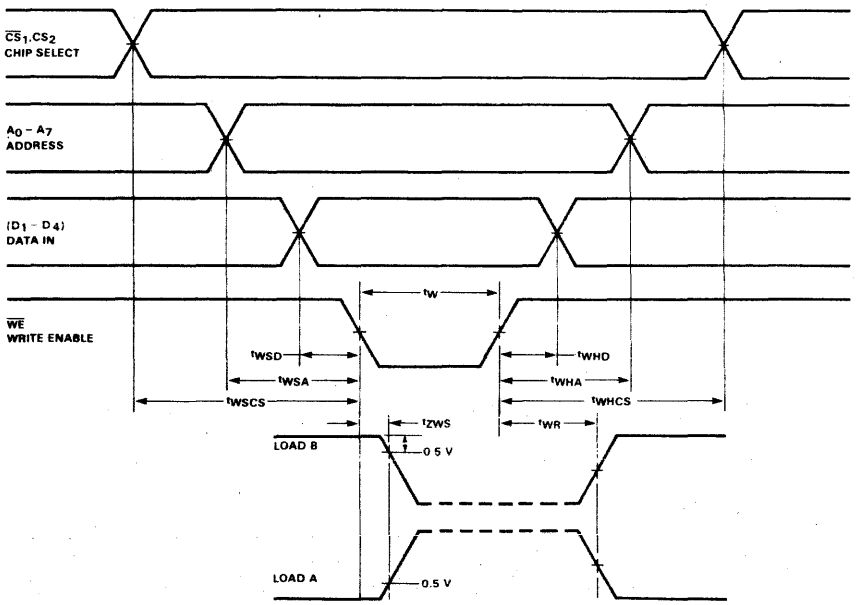
PROPAGATION DELAY FROM ADDRESS INPUTS



PROPAGATION DELAY FROM OUTPUT ENABLE



WRITE MODE



(All above measurements referenced to 1.5 V unless otherwise indicated)

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

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93415 • 93L415 • 93425 • 93L425

TTL ISOPLANAR MEMORY

1024 x 1-BIT FULLY DECODED RANDOM ACCESS MEMORIES

DESCRIPTION — These devices are 1024-Bit Read/Write Random Access Memories organized 1024 words by one bit and are designed for buffer control storage and high performance main memory applications. The typical access time ranges from 25 ns to 40 ns depending upon the device type. The 93L415 and 93L425 are appropriate for systems requiring low power.

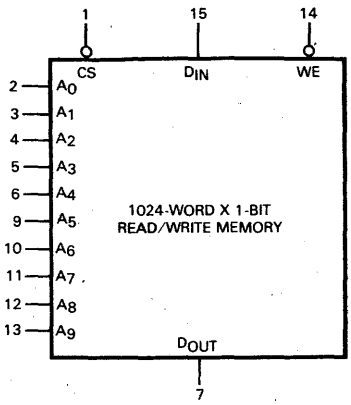
Each 1024-bit memory has full decoding on chip, separate Data Input and Data Output lines and an active LOW Chip Select line. The 93425 and 93L425 have a 3-state output to drive bus organized systems and/or highly capacitive loads and the 93415 and 93L415 have an uncommitted collector output for ease of memory expansion. All of the devices are fully compatible with standard DTL and TTL logic families.

- **FULL MIL AND COMMERCIAL RANGES**
- **3-STATE OUTPUT — 93425 AND 93L425**
- **UNCOMMITTED COLLECTOR OUTPUT — 93415 AND 93L415**
- **NON-INVERTING DATA OUTPUT**
- **ORGANIZED 1024 WORDS x 1 BIT**
- **POWER DISSIPATION 250 mW TYP — 93L415 AND 93L425**
- **POWER DISSIPATION 0.5 mW TYP — 93415 AND 93425**
- **TTL INPUTS AND OUTPUT**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**

PIN NAMES

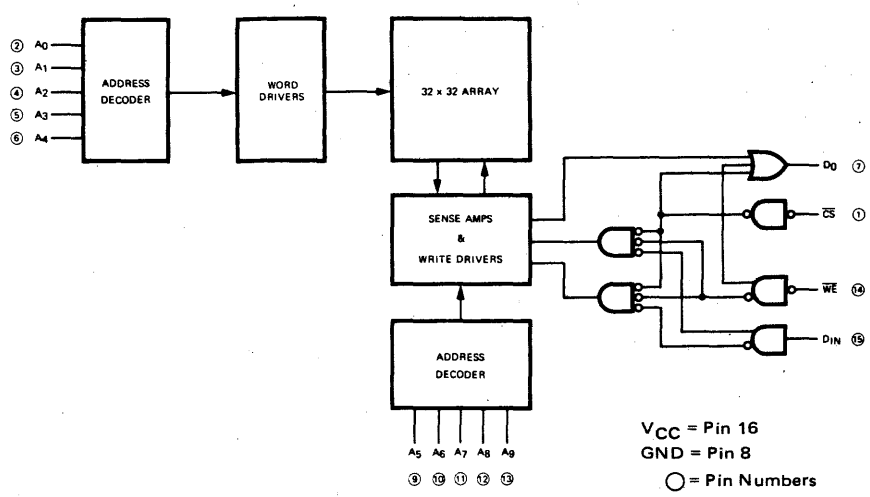
$\overline{CS}$	Chip Select Input
$A_0 - A_9$	Address Inputs
$\overline{WE}$	Write Enable Input
D_{IN}	Data Input
D_{OUT}	Data Output

LOGICAL SYMBOL



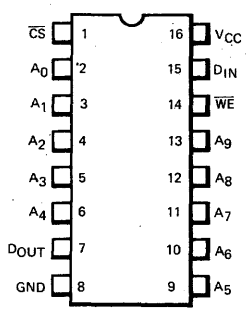
V_{CC} = Pin 16
GND = Pin 8

93415/93L415 LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAMS
DIP (TOP VIEW)



Note:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

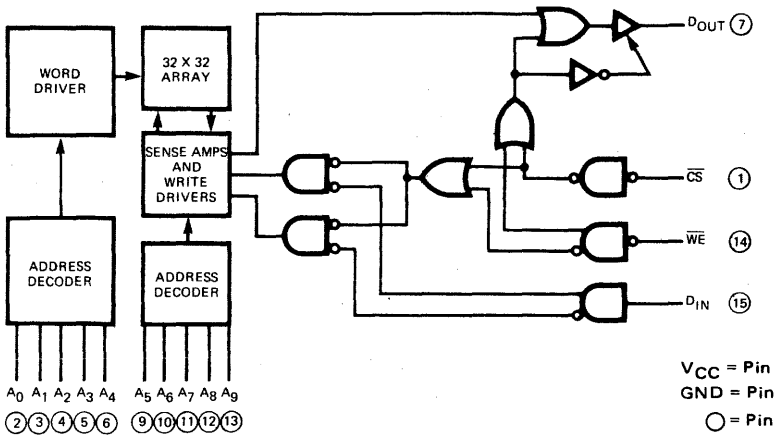
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93425/93L425 LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — These devices are fully decoded 1024-Bit Random Access Memories organized 1024 words by one bit. Word selection is achieved by means of a 10-bit address, A_0-A_9. The Chip Select input allows memory array expansion. For large memories, the fast chip select access time permits decoding of the Chip Select ($\overline{CS}$) from the address without affecting system performance. The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT} and is non-inverted.

93425 and 93L425 Only

The 93425 and 93L425 3-state outputs provide drive capability for higher speeds with high capacitive load systems. The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus. During writing, the output is held in the high impedance state.

93415 and 93L415 Only

The 93415 and 93L415 uncommitted collector outputs are provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93415s or 93L415s can be tied together. In other applications, the wired-OR is not used. In either case, an external pull-up resistor of R_L value must be used to provide a HIGH at the output when it is off. Any R_L value within the range specified below may be used. The minimum R_L value is limited by output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}. One Unit Load = 40 μA HIGH/1.6 mA LOW.

$$\frac{V_{CC}\,(min)}{I_{OL} - FO\,(1.6)} \leq R_L \leq \frac{V_{CC}\,(min) - V_{OH}}{n\,(I_{CEX}) + FO\,(0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output HIGH Level at Output Node
I_{OL} = Output LOW Current

93415/93L415 – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Collector	
H	X	X	H	NOT SELECTED
L	L	L	H	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)

93425/93L425 – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	
H	X	X	HIGH Z	Not Selected
L	L	L	HIGH Z	Write "0"
L	L	H	HIGH Z	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)

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ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	0.5 V to +5.50 V
Output Current (dc) (output LOW)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE (T_A) (Note 4)
	MIN	TYP	MAX	
93415XC, 934L15XC 93425XC, 934L25XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93415XM, 93415XM 93425XM, 934L25XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Packaging Information Section for packages available on this product.

93415 DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN	TYP (Note 3)	MAX			
V_{OL}	Output LOW Voltage		0.3	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current		−250	−400	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
				1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
I_{CEX}	Output Leakage Current		1.0	100	μA	V_{CC} = MAX, V_{OUT} = 4.5 V	
V_{CD}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current		95	130	mA	$T_A \geq 75°C$	V_{CC} = MAX, All Inputs Grounded
				155	mA	T_A = 0°C	
				170	mA	T_A = −55°C	

93L415 DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN	TYP (Note 3)	MAX			
V_{OL}	Output LOW Voltage		0.35	0.50	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current		−150	−300	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
				1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
I_{CEX}	Output Leakage Current		1.0	100	μA	V_{CC} = MAX, V_{OUT} = 4.5 V	
V_{CD}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current			55	mA	$T_A \geq 75°C$	V_{CC} = MAX, All Inputs Grounded
			45	65	mA	T_A = 0°C	
				75	mA	T_A = −55°C	

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93425 DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC		LIMITS MIN	LIMITS TYP (Note 3)	LIMITS MAX	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage			0.3	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage		2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage			1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current			−250	−400	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
I_{OFF}	Output Current (HIGH Z)				50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V	
					−50		V_{CC} = MAX, V_{OUT} = 0.5 V	
I_{OS}	Output Current Short Circuit to Ground				−100	mA	V_{CC} = MAX, Note 7	
V_{OH}	Output HIGH Voltage	93425XC	2.4			V	I_{OH} = −10.3 mA, V_{CC} = 5.0 V ±5%	
		93425XM	2.4			V	I_{OH} = −5.2 mA	
V_{CD}	Input Diode Clamp Voltage			−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current				130	mA	$T_A \geq 75°C$	V_{CC} = MAX, All Inputs Grounded
				95	155	mA	T_A = 0°C	
					170	mA	T_A = −55°C	

93L425 DC CHARACTERISTICS: Over Operating Temperature Ranges. Notes 1, 2 and 4

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP (Note 3)	LIMITS MAX	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage			0.35	0.50	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage		2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage			1.5	0.8	V	Guranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current			−150	−300	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
I_{OFF}	Output Current (HIGH Z)				50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V	
					−50		V_{CC} = MAX, V_{OUT} = 0.5 V	
I_{OS}	Output Current Short Circuit to Ground				−100	mA	V_{CC} = MAX, Note 7	
V_{OH}	Output HIGH Voltage	93L425XC	2.4			V	I_{OH} = −5.2 mA, V_{CC} = 5.0 V ±5%	
		93L425XM	2.4			V	I_{OH} = −5.2 mA, V_{CC} = 5.0 V ±10%	
V_{CD}	Input Clamp Diode Voltage			−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current				55	mA	$T_A \geq 75°C$	V_{CC} = MAX, All Inputs Grounded
				45	65	mA	T_A = 0°C	
					75	mA	T_A = −55°C	

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} (Junction to Ambient) (at 400 lpm air flow) = 50°C/Watt, Ceramic DIP; 65°CC/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

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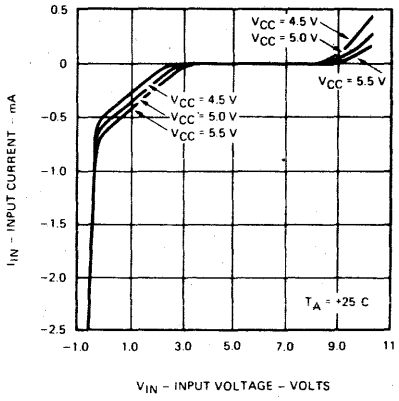
AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

SYMBOL	CHARACTERISTIC	93415/25AXC			93415/25XC			93415/25XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES											
t_{ACS}	Chip Select Time		15	20		15	35		15	45	ns	See Test Circuit and Waveforms
t_{RCS}	Chip Select Recovery Time		15	20		20	35		20	50		
t_{AA}	Address Access Time		25	30		30	45		40	60		
WRITE MODE	DELAY TIMES											
t_{WS}	Write Disable Time		15	20		20	35		20	45	ns	
t_{WR}	Write Recovery Time		20	25		25	40		45	50		
	INPUT TIMING REQUIREMENTS											
t_W	Write Pulse Width (to guarantee write)	20	15		30	25		40	25		ns	See Test Circuit and Waveforms
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0		5	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0			
t_{WSA}	Address Set-Up Time	5	0		10	0		15	0			
t_{WHA}	Address Hold Time	5	0		5	0		5	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0		5	0			
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0			
C_I	Input Pin Capacitance		4	5		4	5		4	5	pF	Measure with Pulse Technique
C_O	Output Pin Capacitance		7	8		7	8		7	8		

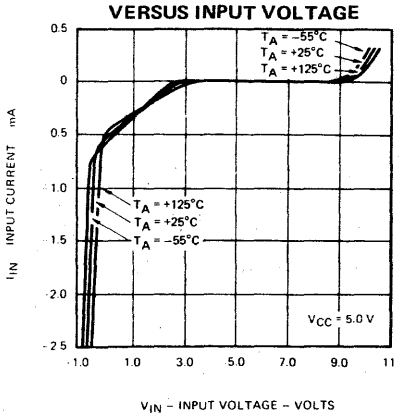
AC CHARACTERISTICS: Over Guaranteed Operating Ranges. Notes 1, 2, 4, 5, 6

SYMBOL	CHARACTERISTIC	93415/25XC			93415/25XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Access Time		20	40		20	45		See Test Circuit
t_{ZRCS}	Chip Select to HIGH Z		20	40		20	50	ns	and Waveforms
t_{AA}	Address Access Time		35	60		35	70		
WRITE MODE	DELAY TIMES								
t_{ZWS}	Write Disable to HIGH Z		20	45		20	45		
t_{WR}	Write Recovery Time		20	45		20	55		
	INPUT TIMING REQUIREMENTS								
t_W	Write Pulse Width (to guarantee write)	45	25		50	25		ns	See Test Circuit and Waveforms
t_{WSD}	Data Set-Up Time Prior to Write	5	0		10	0			
t_{WHD}	Data Hold Time After Write	5	0		10	0			
t_{WSA}	Address Set-Up Time	10	0		10	0			
t_{WHA}	Address Hold Time	5	0		10	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		10	0			
t_{WHCS}	Chip Select Hold Time	5	0		10	0			
C_I	Input Pin Capacitance		4	5		4	5	pF	
C_O	Output Pin Capacitance		7	8		7	8		

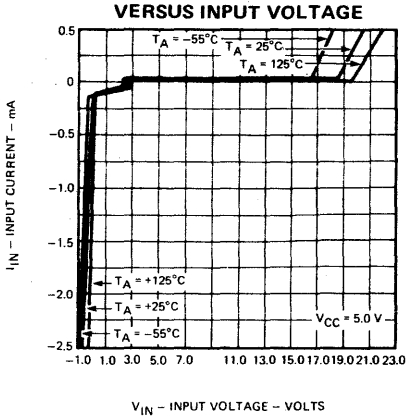
93425
INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS SUPPLY VOLTAGE



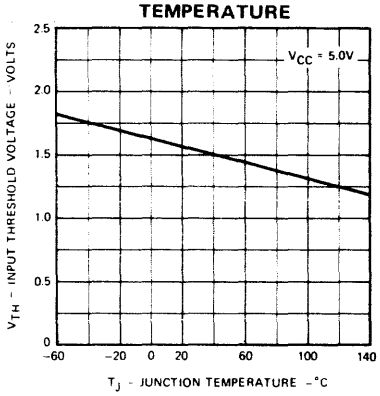
93415/93425
INPUT CURRENT VERSUS INPUT VOLTAGE



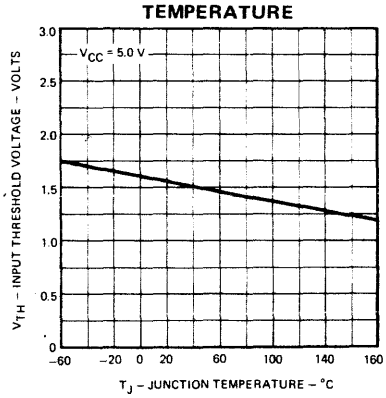
93L415/93L425
INPUT CURRENT VERSUS INPUT VOLTAGE



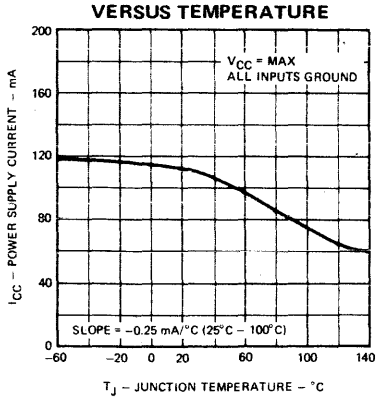
93415/93425
INPUT THRESHOLD VOLTAGE VERSUS TEMPERATURE



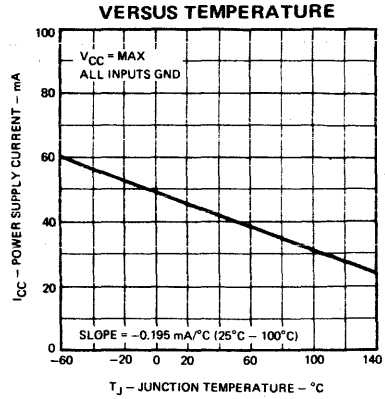
93L415/93L425
INPUT THRESHOLD VOLTAGE VERSUS TEMPERATURE



93415/93425
POWER SUPPLY CURRENT VERSUS TEMPERATURE

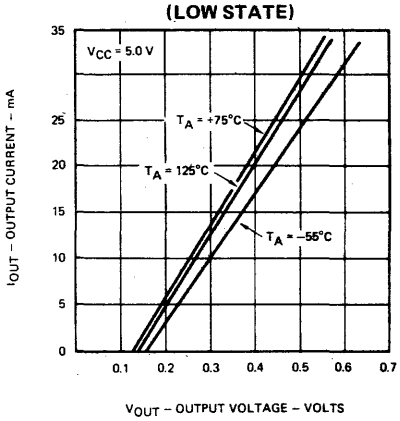


93L415/93L425
POWER SUPPLY CURRENT VERSUS TEMPERATURE

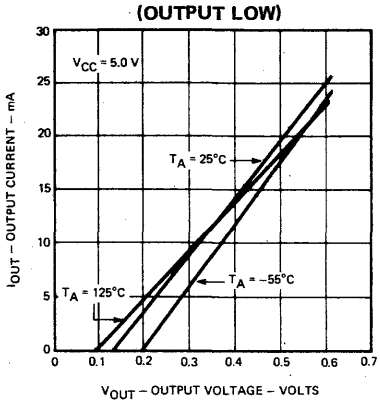


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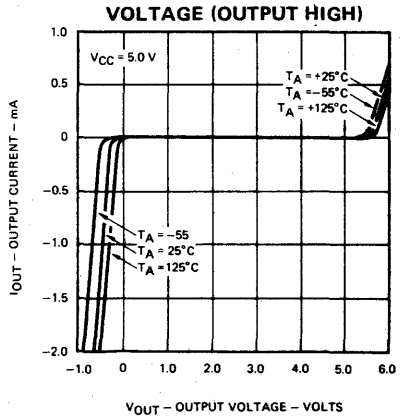
93415
OUTPUT CURRENT
VERSUS OUTPUT VOLTAGE
(LOW STATE)



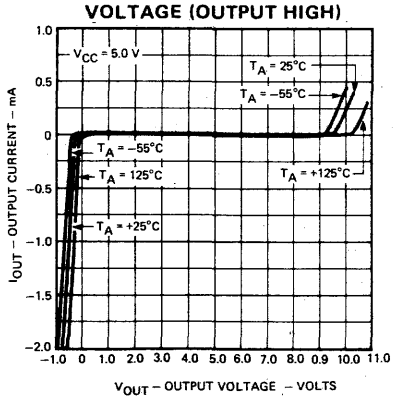
93L415/93L425
OUTPUT CURRENT
VERSUS OUTPUT VOLTAGE
(OUTPUT LOW)



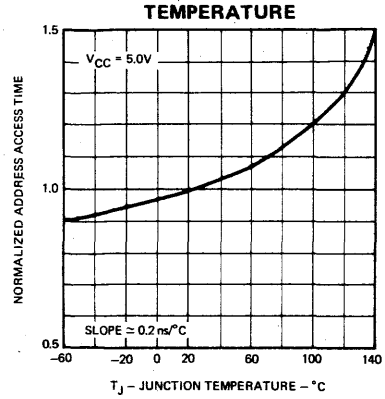
93415
OUTPUT CURRENT
VERSUS OUTPUT
VOLTAGE (OUTPUT HIGH)



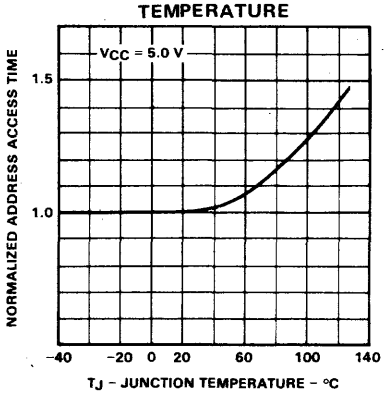
93L415/93L425
OUTPUT CURRENT
VERSUS OUTPUT
VOLTAGE (OUTPUT HIGH)



93415
NORMALIZED ADDRESS
ACCESS TIME VERSUS
TEMPERATURE



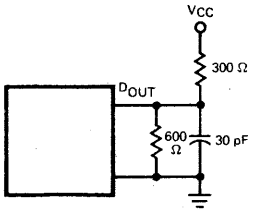
93L415/93L425
NORMALIZED ADDRESS
ACCESS TIME VERSUS
TEMPERATURE



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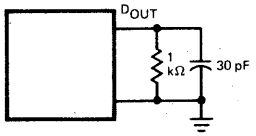
AC Test Load

93415, 93L415, 93425 and 93L425



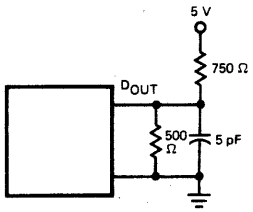
Load A

93425 and 93L425 only



Load B

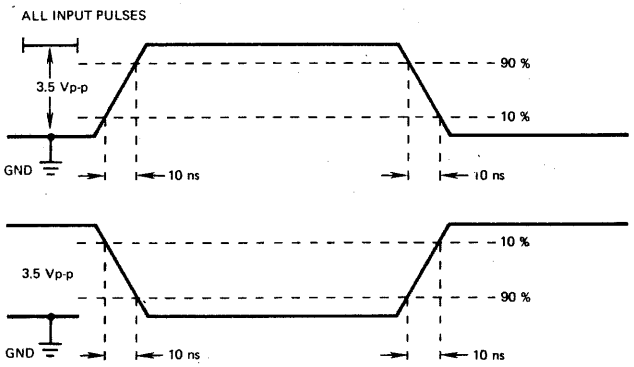
93425 and 93L425 only



Load C

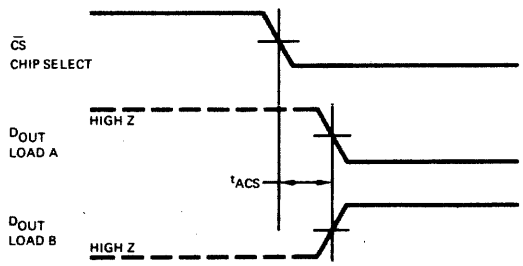
AC WAVEFORMS

93L415
INPUT PULSES

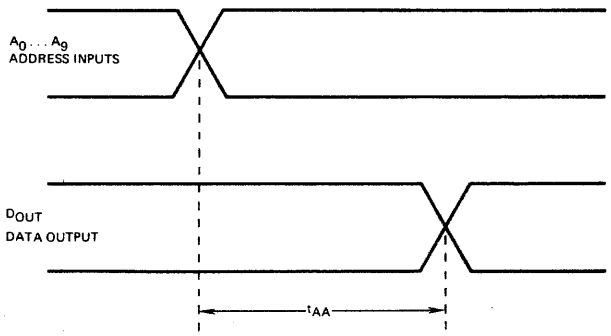


READ MODE

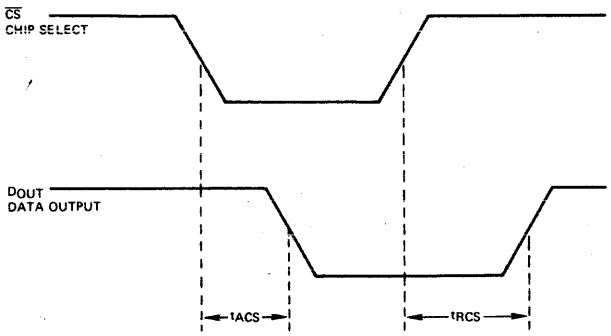
93425/93L425 PROPAGATION DELAY FROM CHIP SELECT



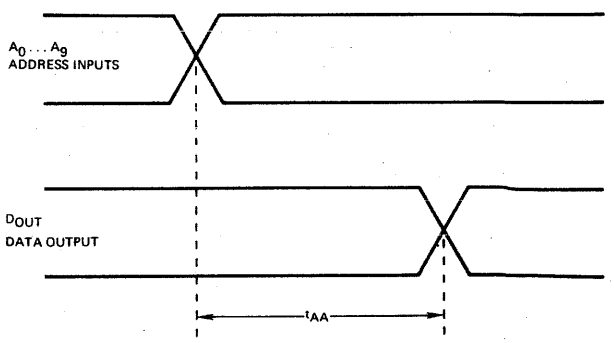
93425/93L425 PROPAGATION DELAY FROM ADDRESS INPUTS



93415/93L415 PROPAGATION DELAY FROM CHIP SELECT



93415/93L415 PROPAGATION DELAY FROM ADDRESS INPUTS

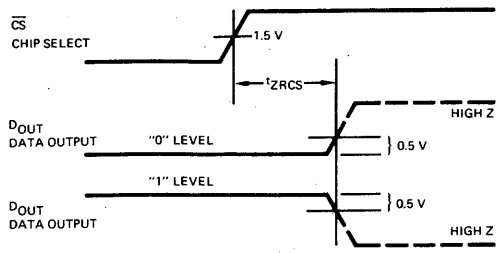


(All time measurements referenced to 1.5 V)

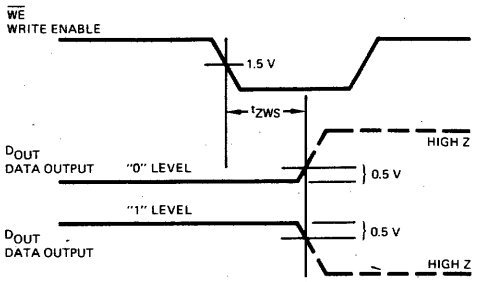
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AC WAVEFORMS (Cont'd)

93425/93L425
PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z

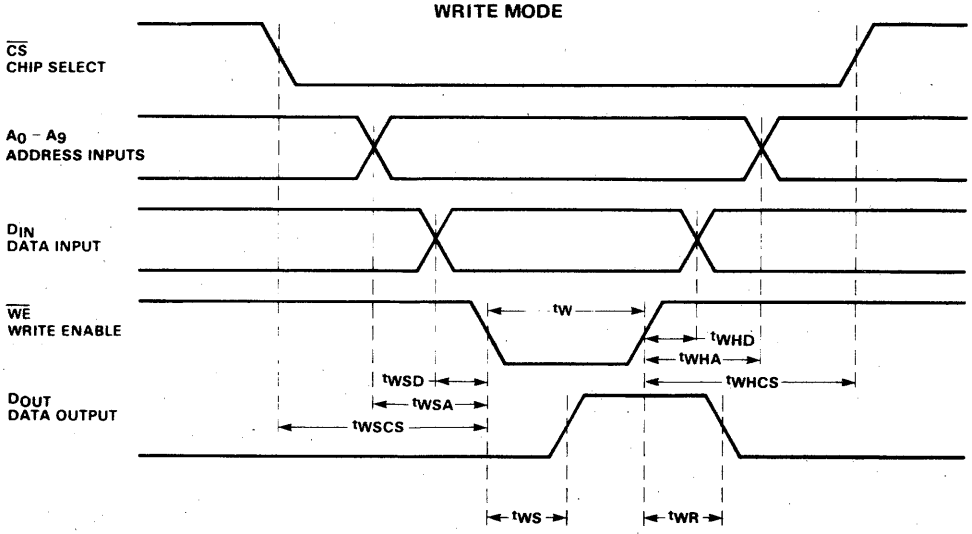


93425/93L425
WRITE ENABLE TO HIGH Z DELAY

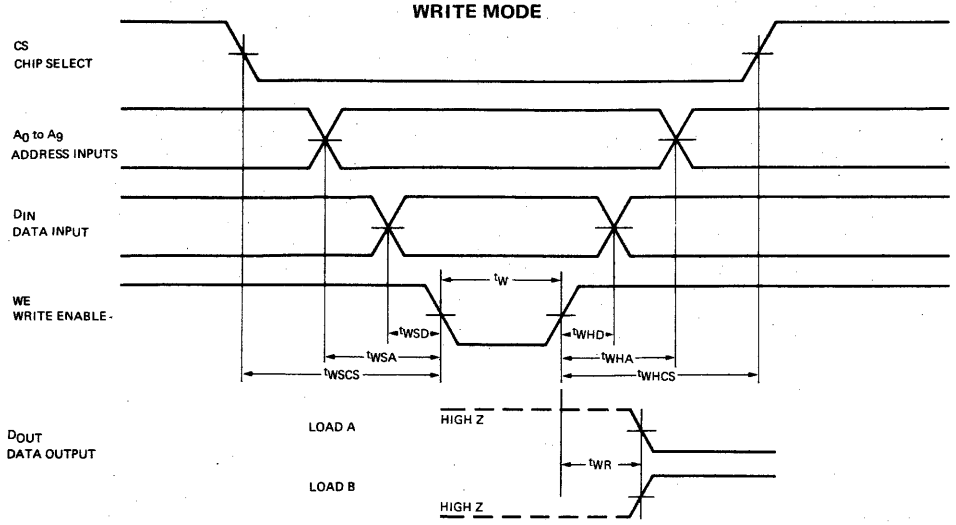


(All t_{ZXXX} parameters are measured at a delta of 0.5 V from the logic level and using Load C.)

93415/93L415
WRITE MODE



93425/93L425
WRITE MODE



(All time measurements referenced to 1.5 V)

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

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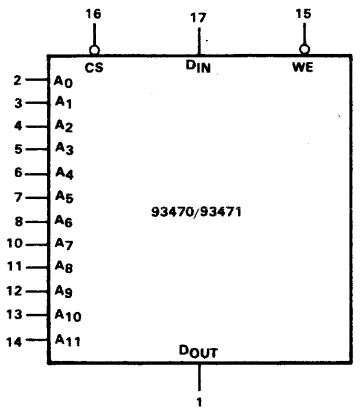
TTL ISOPLANAR MEMORY 93470 • 93471

4096 × 1-BIT FULLY STATIC RANDOM ACCESS MEMORY

DESCRIPTION – The 93470 and 93471 are 4096-bit TTL Read/Write Random Access Memories organized 4096 words by one bit. The devices are identical except for the output stage. The 93470 has an uncommitted collector output, while the 93471 has a 3-state output. The devices have full decoding on chip, separate Data Input and Data Output lines and active LOW Chip Select lines. They are designed for high performance main memory application and can be used to replace four 1024-bit RAMs.

- **FULL MIL AND COMMERCIAL RANGES**
- **ORGANIZATION — 4096 WORDS X 1 BIT**
- **READ ACCESS TIME — 30 ns TYPICAL**
- **CHIP SELECT ACCESS TIME — 15 ns TYPICAL**
- **UNCOMMITTED COLLECTOR OUTPUT — 93470**
- **3-STATE OUTPUT — 93471**
- **NON-INVERTING DATA OUTPUT**
- **POWER DISSIPATION — 0.12 mW/BIT TYPICAL**
- **REPLACES FOUR 1024 BY ONE RAMs**

LOGIC SYMBOL

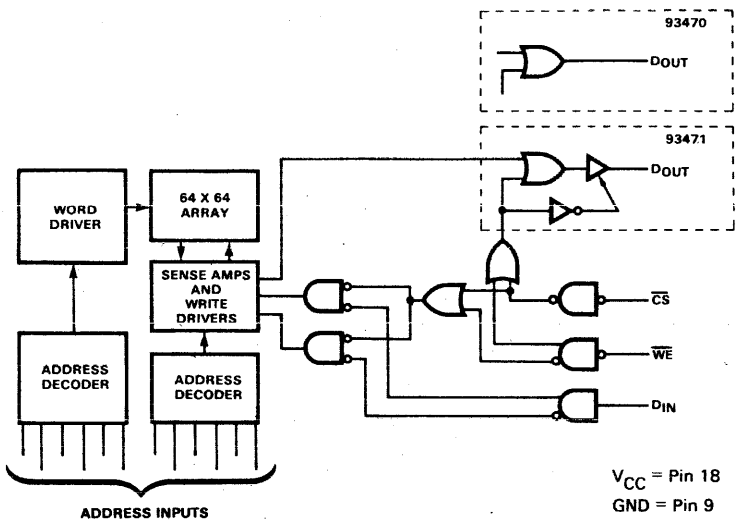


V_{CC} = Pin 18
GND = Pin 9

PIN NAMES

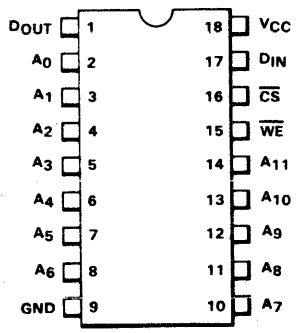
$\overline{CS}$	Chip Select Input
$A_0 - A_{11}$	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

LOGIC DIAGRAM



V_{CC} = Pin 18
GND = Pin 9

CONNECTION DIAGRAM
DIP (TOP VIEW)



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464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA, 94042 (415) 962-5011/TWX 910-379-6435

FAIRCHILD

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FUNCTIONAL DESCRIPTION – The 93470 and 93471 are fully decoded 4096-bit Random Access Memories organized 4096 words by one bit. Word selection is achieved by means of a 12-bit address, A_0 thru A_{11}.

The Chip Select input is provided for logic flexibility. For larger memories, the fast Chip Select access time permits the decoding of Chip Select, $\overline{CS}$, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable, $\overline{WE}$ (pin 5). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at the Data Outputs.

The 93471 has 3-state outputs which provide drive capability for higher speeds with high capacitive load systems. The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

The 93470 has uncommitted collector outputs to allow maximum flexibility in output connection. In many applications, such as memory expansion, the outputs of several 93470s can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of value R_L must be used to provide a HIGH at the output when it is off. Any value of R_L within the range specified below may be used.

$$\frac{V_{CC(max)}}{8 - \text{F.O. } (1.6)} \leqslant R_L \leqslant \frac{V_{CC(min)} - V_{OH}}{N\,(I_{CEX}) + \text{F.O. } (0.04)}$$

R_L is in kΩ
N = number of wired-OR outputs tied together
F.O. = number of TTL Unit Loads (U.L.) driven
I_{CEX} = Memory Output Leakage Current in mA
V_{OH} = Required Output HIGH level at Output Node

The minimum value of R_L is limited by output current sinking ability. The maximum value of R_L is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.

TRUTH TABLE

INPUTS			OUTPUTS		MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	93470 O.C.	93471 3-STATE	
H	X	X	H	HIGH Z	Not Selected
L	L	L	H	HIGH Z	Write "0"
L	L	H	H	HIGH Z	Write "1"
L	H	X	D_{OUT}	D_{OUT}	Read

H = HIGH Voltage; L = LOW Voltage; X = Don't Care (HIGH or LOW)
HIGH Z = High Impedance; OC = Open Collector

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage (dc)*	−0.5 V to +5.5 V
Input Current (dc)*	−12 mA to +5.0 mA
Voltage Applied to Outputs (output HIGH)**	−0.5 V to +5.50 V
Output Current (dc)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93470XC, 93471XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93470XM, 93471XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type, F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

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DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1–4)

SYMBOL	CHARACTERISTIC		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage			0.35	0.45	V	V_{CC} = MIN, I_{OL} = 8 mA
V_{IH}	Input HIGH Voltage		2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs
V_{IL}	Input LOW Voltage			1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs
I_{IL}	Input LOW Current			−250	−400	μA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V
V_{CD}	Input Diode Clamp Voltage			−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA
I_{CEX}	Output Leakage Current	93470		1.0	100	μA	V_{CC} = MAX, V_{OUT} = 4.5 V
I_{OFF}	Output Current (HIGH Z)	93471			50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V
					−50		V_{CC} = MAX, V_{OUT} = 0.5 V
V_{OH}	Output HIGH Voltage	93471	2.4			V	V_{CC} = MIN, I_{OH} = −5.2 mA
I_{OS}	Output Current Short Circuit to Ground	93471			−100	mA	V_{CC} = MAX, Note 7
I_{CC}	Power Supply Current	93470/71XC		110		mA	T_A = +75°C, V_{CC} = MAX,
		93470/71XC		130			T_A = 0°C, All Inputs and
		93470/71XM		100			T_A = +125°C, Outputs Open
		93470/71XM		140			T_A = −55°C

AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1–6)

SYMBOL	CHARACTERISTIC	93470/71XC MIN	93470/71XC TYP	93470/71XC MAX	93470/71XM MIN	93470/71XM TYP	93470/71XM MAX	UNITS	CONDITIONS
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Access Time		15	30		15	35		
t_{RCS}	Chip Select Recovery Time (93470)		25	35		25	45		
t_{ZRCS}	Chip Select to HIGH Z (93471)		25	35		25	45	ns	See Test Circuit and Waveforms
t_{AA}	Address Access Time		30	50		30	60		
WRITE MODE	DELAY TIMES								
t_{WS}	Write Disable Time (93470)		25	35		25	45		
t_{ZWS}	Write Disable to HIGH Z (93471)		25	35		25	45	ns	
t_{WR}	Write Recovery Time		20	30		20	45		
	INPUT TIMING REQUIREMENTS								See Test Circuit and Waveforms
t_W	Write Pulse Width (to guarantee write)	40	25		45	25			
t_{WSD}	Data Set-Up Time Prior to Write	10	5		15	5			
t_{WHD}	Data Hold Time After Write	5	0		10	0			
t_{WSA}	Address Set-Up Time	10	5		15	5		ns	
t_{WHA}	Address Hold Time	5	0		10	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		10	0			
t_{WHCS}	Chip Select Hold Time	5	0		10	0			
C_I	Input Pin Capacitance		4	5		4	5	pF	Measure with Pulse Technique
C_O	Output Pin Capacitance		7	8		7	8		

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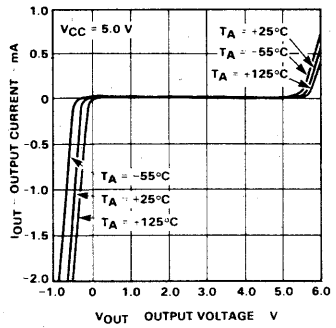
NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 15°C/Watt, Flatpak.

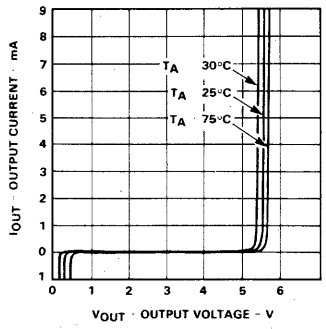
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

TYPICAL ELECTRICAL CHARACTERISTIC CURVES

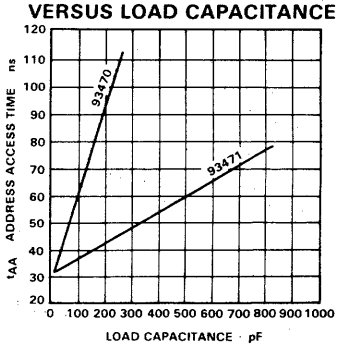
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH) (93470 ONLY)



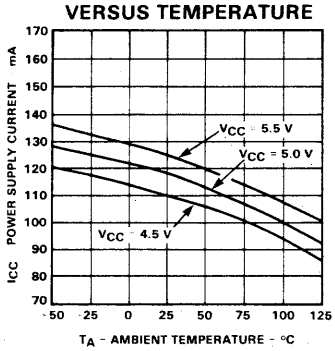
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH Z STATE) (93471 ONLY)



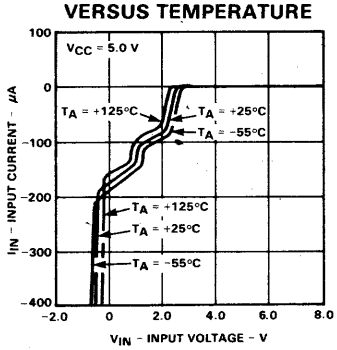
ADDRESS ACCESS TIME VERSUS LOAD CAPACITANCE



POWER SUPPLY CURRENT VERSUS TEMPERATURE

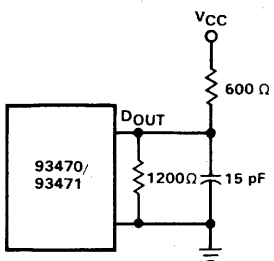


INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE

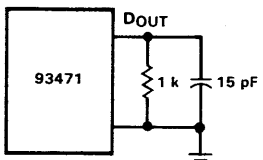


AC TEST LOAD AND WAVEFORM

LOADING CONDITIONS

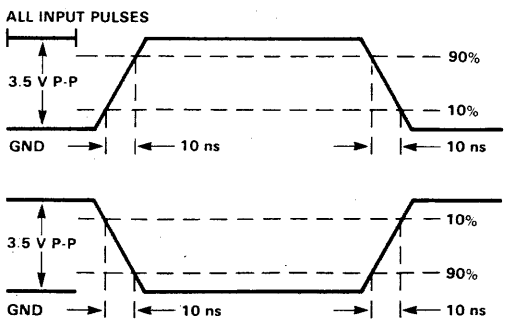


Load A



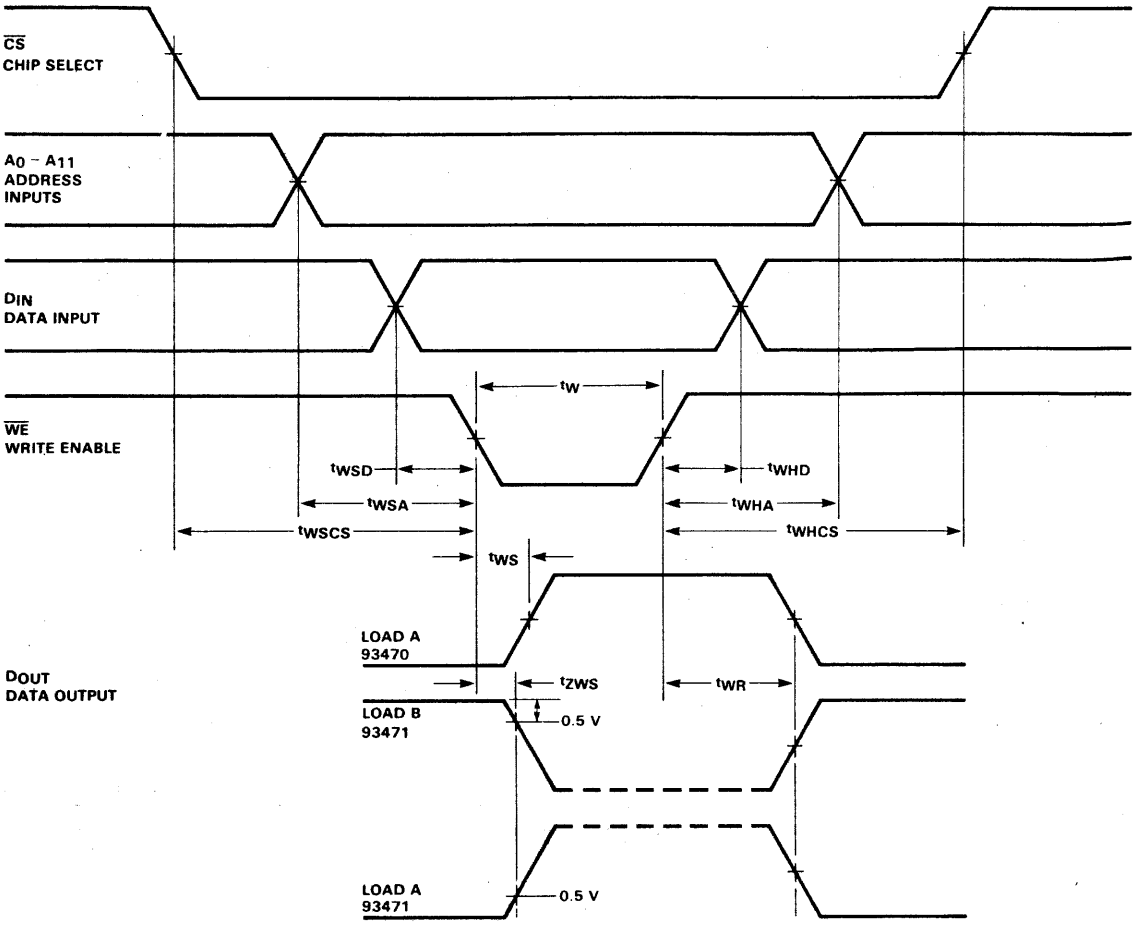
Load B

INPUT PULSES



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WRITE MODE

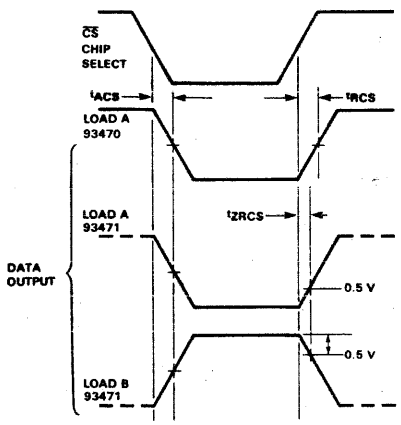


(All above measurements referenced to 1.5 V unless otherwise indicated)

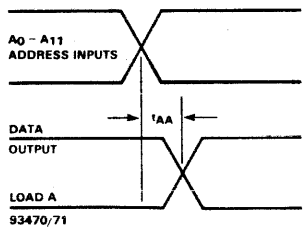
NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

READ MODE

PROPAGATION DELAY FROM CHIP SELECT



PROPAGATION DELAY FROM ADDRESS INPUTS



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93417/27 • 93436/46 • 93438/48
93450/51 • 93452/53
FIELD PROGRAMMABLE READ ONLY MEMORIES

GENERAL DESCRIPTION—Fairchild's family of field programmable ROMs includes 1024, 2048, 4096-bit devices. Each of the five device pairs are identical except for the output stages—the first of each pair has uncommitted collector outputs, the second has 3-state outputs. They are supplied with all bits stored as logic "1" and can be programmed by following the field programming procedure.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55C to +125°C
V_{CC}	-0.5V to +7.0V
Input Voltages	-0.5V to +5.5V
Current Into Output Terminal	100mA
Output Voltages— 94317, 93427, 93452, 93453	-0.5V to +5.5V
Output Voltages— 93436, 93446, 93438, 93448	-0.5V to +4.0VV

- **SILICON NITRIDE PROTECTED**
- **FULL MIL AND COMMERCIAL RANGES**
- **FIELD PROGRAMMABLE**
- **FULLY DECODED — ON-CHIP ADDRESS DECODER AND BUFFER**
- **WIRED-OR CAPABILITY**
- **NICHROME FUSE LINKS FOR HIGH RELIABILITY**
- **UNCOMMITTED COLLECTORS — 94317, 93436, 93438, 93450, 93452**
- **3-STATE OUTPUTS — 93427, 93446, 93448, 93451, 93453**

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE
	MIN	TYP	MAX	
93417/27XC 93436/46XC 93438/48XC 93450/51XC 93452/53XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93417/27XM 93436/46XM 93438/48XM 93450/51XM 93452/53XM	4.50 V	5.0 V	5.50 V	-55 to +125°C

X = package type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP.

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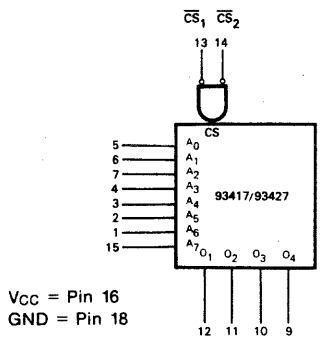
464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA, 94042 (415) 962-5011/TWX 910-379-6435

FAIRCHILD

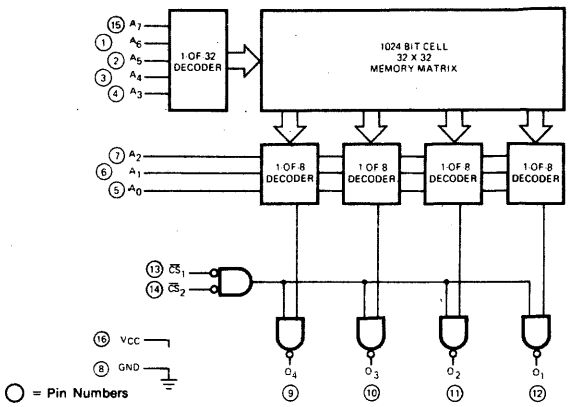
93417/27

256 × 4-BIT PROGRAMMABLE READ ONLY MEMORY

LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION - The 93417 and 93427 are bipolar field Programmable Read Only Memories (PROMs) organized 256 words by four bits per word. Open collector outputs are provided for use in wired-OR systems. The 93427 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Chip Selects are active LOW; conversely, a HIGH (logic "1") on the $\overline{CS_1}$ or $\overline{CS_2}$ will disable all outputs.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_7 inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

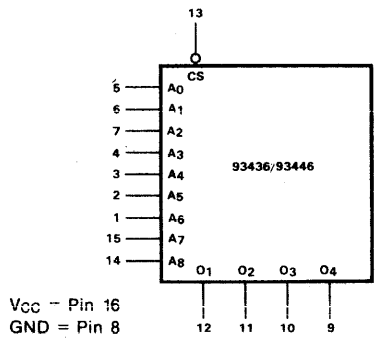
PIN NAMES

A_0 — A_7	Address Inputs
$\overline{CS_1}$, $\overline{CS2}$	Chip Select Inputs (Active LOW)
O_1 — O_4	Data Outputs

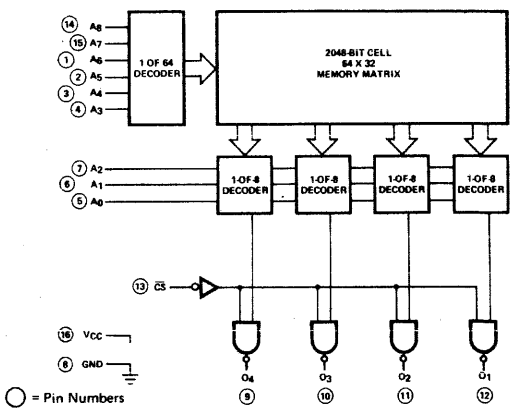
93436/46

512 × 4-BIT PROGRAMMABLE READ ONLY MEMORY

LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION—The 93436 and 93446 are bipolar field Programmable Read Only Memories (PROMs) organized 512 words by four bits per word. Open collector outputs are provided on the 93436 for use in wired-OR systems. Chip select is active LOW; i.e., a HIGH (logic "1") on the $\overline{CS}$ pin will disable all outputs. The 93446 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_8 inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

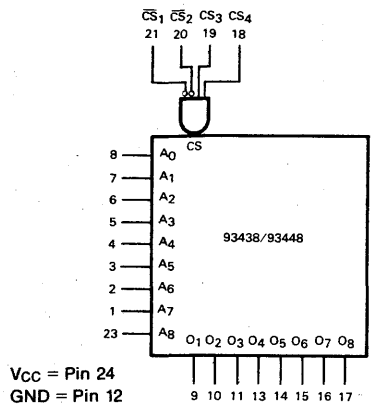
PIN NAMES

A_0-A_8	Address Inputs
$\overline{CS}$	Chip Select Input
O_1 - O_4	Data Outputs

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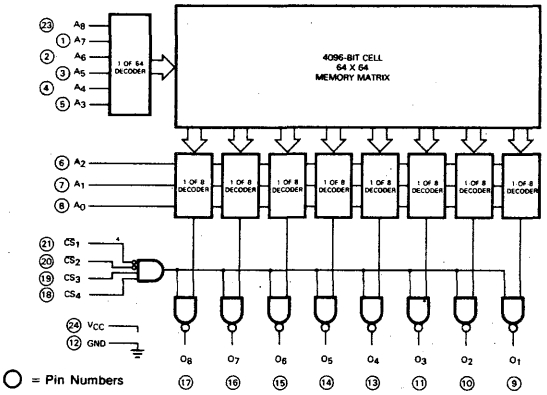
93438/48
512 × 8-BIT PROGRAMMABLE READ ONLY MEMORY

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION—The 93438 and 93448 are bipolar field Programmable Read Only Memories (PROMs) organized 512 words by eight bits per word. Open collector outputs are provided on the 93438 for use in wired-OR systems. The 93448 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Chip Select follows the logic equation: $\overline{CS_1} \bullet \overline{CS_2} \bullet CS_3 \bullet CS_4 = CS$; i.e., if $\overline{CS_1}$ and $\overline{CS_2}$ are both active LOW and CS_3 and CS_4 are both active HIGH, all eight outputs are enabled; for any other condition all eight outputs are disabled.

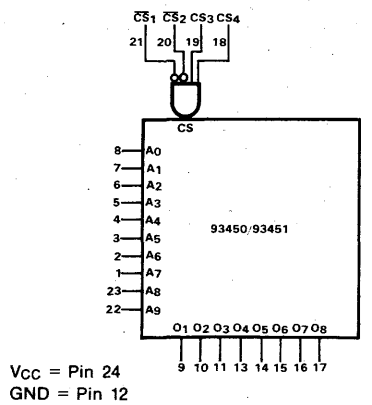
The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_8 inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

PIN NAMES

A_0 — A_8	Address Inputs
$\overline{CS_1}$, $\overline{CS_2}$, CS_3, CS_4	Chip Select Inputs
O_1 — O_8	Data Outputs

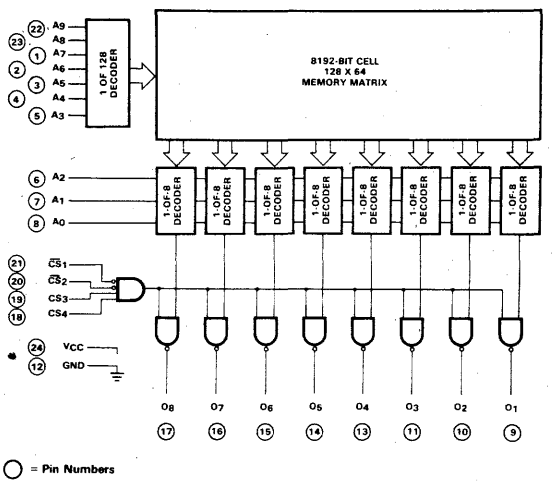
93450/51
1024 × 8-BIT PROGRAMMABLE READ ONLY

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM



PIN NAMES

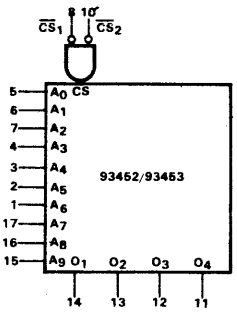
A_0 — A_9	Address Inputs
$\overline{CS_1}$, $\overline{CS_2}$, CS_3, CS_4	Chip Select Inputs
O_1 — O_8	Data Outputs

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93452/53

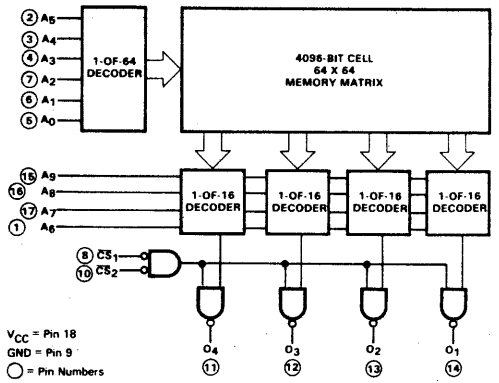
1024 × 4-BIT PROGRAMMABLE READ ONLY MEMORY

LOGIC SYMBOL



VCC = Pin 18
GND = Pin 9

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION—The 93452 and 93453 are bipolar field Programmable Read Only Memories (PROMs) organized 1024 words by four bits per word. Open collector outputs are provided on the 93452 for use in wired-OR systems. The 93453 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Chip Selects for both devices are active LOW; conversely, a HIGH (logic "1") on the $\overline{CS}_1$ or $\overline{CS}_2$ will disable all outputs.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_9 inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

PIN NAMES

A_0 to A_9	Address Inputs
$\overline{CS}_1$, $\overline{CS}_2$	Chip Select Inputs
O_1 to O_4	Data Outputs

93452/93453

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise noted.

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
I_{CEX}	Output Leakage Current (93452 only)			50	μA	V_{CC} = 5.25 V, V_{CEX} = 4.95 V, 0°C to +75°C Address any HIGH Output
I_{CEX}	Output Leakage Current (93452 only)			100	μA	V_{CC} = 5.5 V, V_{CEX} = 5.2 V, −55°C to +125°C Address any HIGH Output
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA A_9 = +10.8 V, A_2 = 10.8 V
V_{OH}	Output HIGH Voltage (93453 only)	2.4			V	V_{CC} = MIN, I_{OH} = −2.0 mA
I_{off}	Output Leakage Current for HIGH Impedance State (93453 only)			50 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V — 0°C to +75°C
I_{off}	Output Leakage Current for HIGH Impedance State (93453 only)			100 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V — −55°C to +125°C
V_{iH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		 −160 −160	 −250 −250	 μA μA	V_{CC} = MAX, V_F = 0.45 V
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			 40 40	 μA μA	V_{CC} = MAX, V_R = 2.4 V
I_{CC}	Power Supply Current		120	170	mA	V_{CC} = MAX, Outputs Open Inputs Grounded and Chip Selected
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
V_C	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_A = −18 mA

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93417 • 93436 • 93438

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise noted.

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
I_{CEX}	Output Leakage Current			50	μA	V_{CC} = 5.25 V, V_{CEX} = 4.95 V, 0°C to +75°C Address any HIGH Output
I_{CEX}	Output Leakage Current			100	μA	V_{CC} = 5.5 V, V_{CEX} = 5.2 V, -55°C to +125°C Address any HIGH Output
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA, A_0 = +10.8 V A_1 through A_7 = HIGH
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		 -160 -160	 -250 -250	 μA μA	V_{CC} = MAX, V_F = 0.45 V
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			 40 40	 μA μA	V_{CC} = MAX, V_R = 2.4 V
I_{CC} 93417	Power Supply Current		85	110	mA	V_{CC} = MAX, Outputs open Inputs Grounded and Chip Selected
I_{CC} 93436	Power Supply Current		95	130	mA	
I_{CC} 93438	Power Supply Current		130	175	mA	
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
V_C	Input Clamp Diode Voltage			-1.2	V	V_{CC} = MIN, I_A = -18 mA

93427 • 93446 • 93448

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise noted.

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA, A_0 = +10.8 V A_1 through A_7 = HIGH
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = MIN, I_{OH} = -2.0 mA
I_{off}	Output Leakage Current for HIGH Impedance State			50 -50	μA μA	V_{OH} = 2.4 V, V_{OL} = 0.4 V, 0°C to +75°C
I_{off}	Output Leakage Current for HIGH Impedance State			100 -50	μA μA	V_{OH} = 2.4 V, V_{OL} = 0.4 V, -55°C to +125°C
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		 -160 -160	 -250 -250	 μA μA	V_{CC} = MAX, V_F = 0.45 V
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			 40 40	 μA μA	V_{CC} = MAX, V_R = 2.4 V
I_{CC} 93427	Power Supply Current		85	110	mA	V_{CC} = MAX, Outputs open Inputs Grounded and Chip Selected
I_{CC} 93446	Power Supply Current		95	130	mA	
I_{CC} 93448	Power Supply Current		130	175	mA	
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
V_C	Input Clamp Diode Voltage			-1.2	V	V_{CC} = MIN, I_A = -18 mA

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93417/93427

AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ± 5%.

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-}	Address to Output Access Time		25	45	ns	See Waveforms and Test Circuits
t_{AA+}			25	45	ns	
t_{ACS-}	Chip Select Access Time		12	20	ns	
t_{ACS+}			12	20	ns	

AC CHARACTERISTICS: T_A = −55°C to +125°C, V_{CC} = 5.0 V ± 10%.

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-}	Address to Output Access Time		25	60	ns	See Waveforms and Test Circuits
t_{AA+}			25	60	ns	
t_{ACS-}	Chip Select Access Time		12	30	ns	
t_{ACS+}			12	30	ns	

Note 1: Typical values are at V_{CC} = 5.0 V, +25°C and max loading.

93436/93446

AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ± 5%.

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-}	Address to Output Access Time		30	50	ns	See Waveforms and Test Circuits
t_{AA+}			30	50	ns	
t_{ACS-}	Chip Select Access Time		15	25	ns	
t_{ACS+}			15	25	ns	

AC CHARACTERISTICS: T_A = −55°C to +125°C, V_{CC} = 5.0 V ± 10%

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-}	Address to Output Access Time		30	60	ns	See Waveforms and Test Circuits
t_{AA+}			30	60	ns	
t_{ACS-}	Chip Select Access Time		15	30	ns	
t_{ACS+}			15	30	ns	

Note 1: Typical values are at V_{CC} = 5.0 V, +25°C and max loading.

93438/93448

AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-}	Address to Output Access Time		35	55	ns	See Waveforms and Test Circuits
t_{AA+}			35	55	ns	
t_{ACS-}	Chip Select Access Time		15	25	ns	
t_{ACS+}			15	25	ns	

AC CHARACTERISTICS: T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-}	Address to Output Access Time		35	70	ns	See Waveforms and Test Circuits
t_{AA+}			35	70	ns	
t_{ACS-}	Chip Select Access Time		15	30	ns	
t_{ACS+}			15	30	ns	

Note (1): Typical values are at V_{CC} = 5.0 V, 5.0 V, +25°C and max loading.

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AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-}	Address to Output Access Time		30	55	ns	See Waveforms and Test Circuits
t_{AA+}			30	55	ns	
t_{ACS-}	Chip Select Access Time		15	25	ns	
t_{ACS+}			15	25	ns	

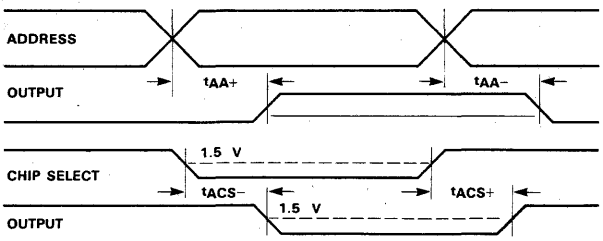
AC CHARACTERISTICS: T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-}	Address to Output Access Time		30	70	ns	See Waveforms and Test Circuits
t_{AA+}			30	70	ns	
t_{ACS-}	Chip Select Access Time		15	30	ns	
t_{ACS+}			15	30	ns	

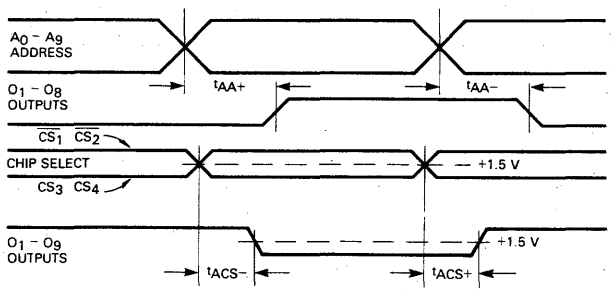
Note 1: Typical limits are at V_{CC} = 5.0 V, +25°C and max loading.

AC WAVEFORMS

93417/27 93436/46 93452/53

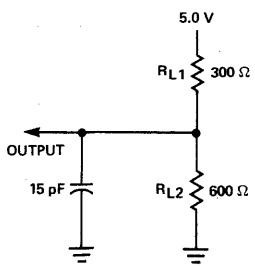


93438/48



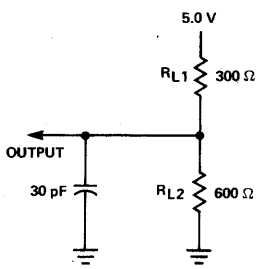
AC TEST OUTPUT LOADS

93417/93436/93438/93450



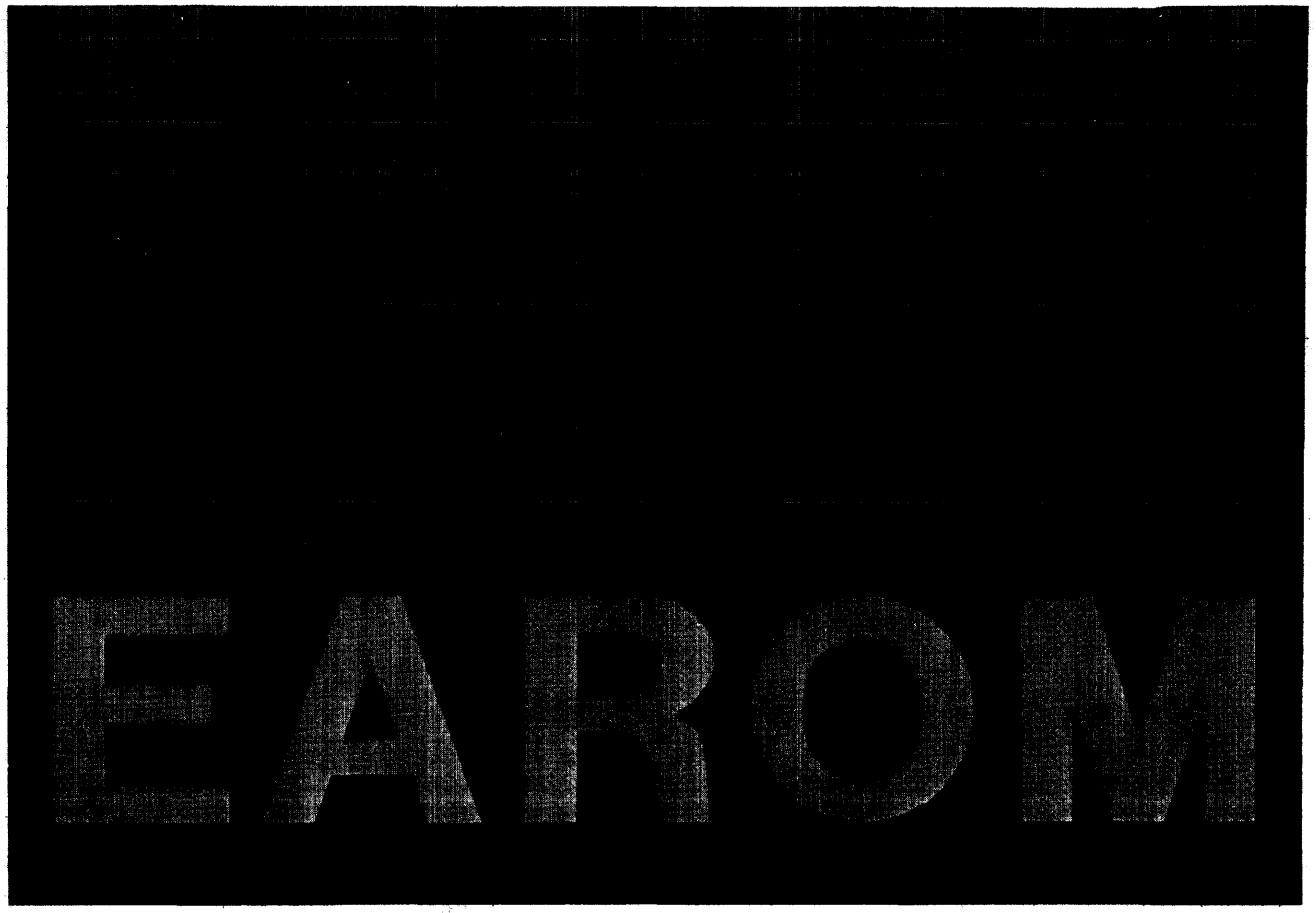
30 mA LOAD

93427/93446/93448/93453



15 mA LOAD

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BITS	MEMORY ORGANIZATION	PART NUMBER	READ ACCESS	ERASE TIME/MODE	WRITE TIME/MODE	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
512	32 x 16	**ER2050**	10 µs	100ms/16 bit word	10ms/16 bit word	+5, -28	28 DIP	10 year data storage @ +70°C.	**1162**
		ER2051	3 µs	50ms/16 bit word	50ms/16 bit word				**1162**
1400	100 x 14	**ER1400**	2.8 µs	16ms/14 bit word	16ms/14 bit word	-35	8 TO/DIP		**1159**
4096	1024 x 4	**ER3400**	650ns	10ms/4 bit word or 1024x4 block	1ms/4 bit word	+5, -12, -30	22 DIP		**1170**
		ER3401	950 ns						**1170**
8192	2048 x 4	**ER2800**	2.6µs	100ms/2048x4 block	10ms/4 bit word	±5, -14, -24	24 DIP		**1164**
		ER2805	2µs						**1164**

MICRO ELECTRONICS

GENERAL INSTRUMENT CORPORATION ▪ MICROELECTRONICS

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1400 Bit Electrically Alterable Read Only Memory

FEATURES

- 100 Word x 14 bit organization
- Word alterable
- 10 years unpowered data storage
- **Write/Erase time 20ms/word**
- Single -35 volt supply
- No voltage switching required
- MOS compatible signal levels

DESCRIPTION

The ER1400 is a serial input/output 1400 bit electrically erasable and reprogrammable ROM, organized as 100 words of 14 bits each. Data and address are communicated in serial form via a one-pin bidirectional bus.

Addressing is by two consecutive one-of-ten codes.

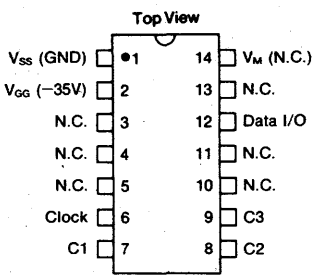
Mode selection is by a 3 bit code applied to C1, C2 and C3.

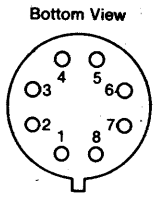
Data is stored by internal negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 1400 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

PIN CONFIGURATIONS

Standard package
14 LEAD DUAL IN LINE

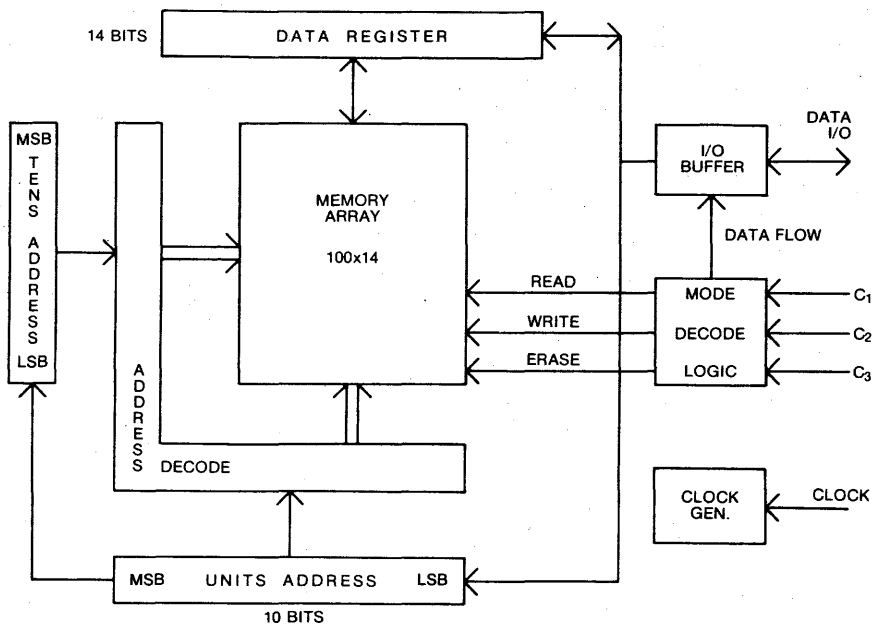
Special Order Package
8 LEAD TO-8 (ER1400T)





1. Data I/O
2. V_M (N.C.)
3. V_{SS} (GND)
4. V_{GG} (−35V)
5. Clock
6. C1
7. C2
8. C3

BLOCK DIAGRAM



General Instrument

MEMORY

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PIN FUNCTIONS

Name	Function
Data	In the Accept Address and Accept Data modes, this pin is an input pin for address and data respectively. In the Shift Data Out mode this pin is an output pin designed to drive MOS. In Standby, Read, Erase and Write, this pin is left floating.
V_M	Used for testing purposes only. Must be left unconnected for normal operation.
V_{SS}	Chip substrate. Normally connected to ground.
V_{GG}	DC supply. Normally connected to −35 volt supply.
Clock	14kHz timing reference. Required for all operations. May be left at logic zero when device is in standby.
C1,C2,C3	Mode control pins. Their operation is as follows:

C1	C2	C3	Function
0	0	0	Standby - contents of Address and Data Register remains unchanged. Output buffer is left floating.
0	1	1	Accept Address - Data presented at the I/O pin is shifted into the Address Register with each clock pulse. Addressing is by two consecutive one-of-ten codes.
1	0	0	Read - The address word is read from memory into the data register.
1	0	1	Shift Data Out - The output driver is enabled and the contents of the Data Register are shifted out one bit with each clock pulse.
0	1	0	Erase - The word stored at the addressed location is erased to all zeros.
1	1	1	Accept Data - The data register accepts serial data presented at the I/O pin. The Address Register remains unchanged.
1	1	0	Write - The word contained in the Data Register is written into the location designated by the Address Register.
0	0	1	Not Used

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs
(except V_{GG}) with respect to V_{SS} ..... −20V to +0.3V
V_{GG} with respect to V_{SS} ..... −40V
Storage temperature (No Data Retention) ..... −65°C to +150°C
Storage temperature (with Data Retention)
Operating ..... −25°C to +75°C
Unpowered ..... −65°C to +80°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

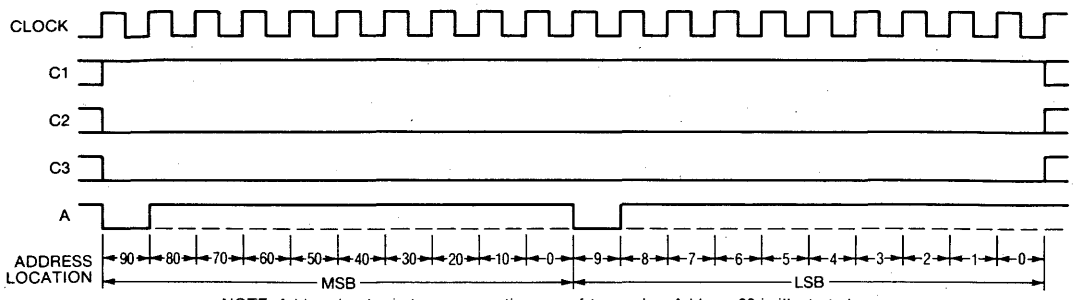
Standard Conditions (unless otherwide noted)
V_{SS} = GND
V_{GG} = −35V ± 8%
Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input logic "1"	VIL	V_{SS}−15.0	—	V_{SS}−8.0	Volts	
Input logic "0"	VIH	V_{SS}−1.0	—	V_{SS}+0.3	Volts	
Input leakage	I_L	—	—	10	μA	V_{IN} = −15V
Output logic "1"	VOL	—	—	V_{SS}−12.0	Volts	Load = 1.5 Meg, 100pF
Output logic "0"	VOH	V_{SS}−1.0	—	V_{SS}+0.3	Volts	I_{SOURCE} = 200μA
Power consumption	P_{GG}	—	—	300	mW	
Power supply currrent	I_{GG}	—	—	8.0	mA	
AC CHARACTERISTICS						
Clock Frequency	fϕ	11.2	14.0	16.8	kHz	
Clock duty cycle	Dϕ	45	50	55	%	
Write time	tw	16.0	20.0	24.0	ms	
Erase time	te	16.0	20.0	24.0	ms	
Rise, fall time	tr, tf	—	—	1.0	μs	
Control, Data set-up and hold time	t_{CS}, t_{CH}	0	—	—	ns	
Propagation delay	tpw	—	—	20.0	μs	Load = 1 Meg, 100pF
Unpowered non-volatile data storage	T_S	10	—	—	Years	
Number of erase/write cycles	N_W	—	—	10^6	—	Per word
Number of read accesses between writes	N_{RA}	10^9	—	—	—	Per word

**Typical values are at +25°C and nominal voltages.

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TIMING DIAGRAMS



NOTE: Addressing is via two consecutive one-of-ten codes. Address 99 is illustrated.

Fig.1 ACCEPT ADDRESS

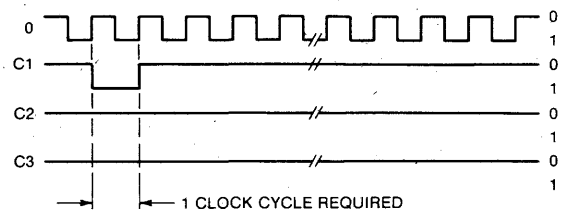
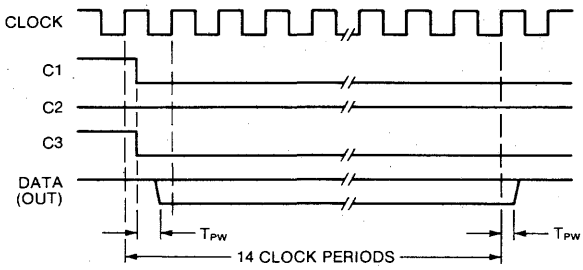


Fig.2 READ



TPW measured initially from control line transition to data out, then measured from the positive clock edges to data changes. Timing measurements are made at V_{SS} −2 and −10 volt points.

Fig.3 SHIFT DATA OUT

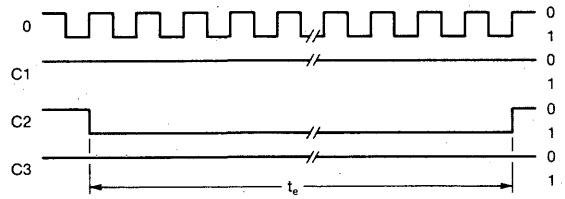


Fig.4 ERASE

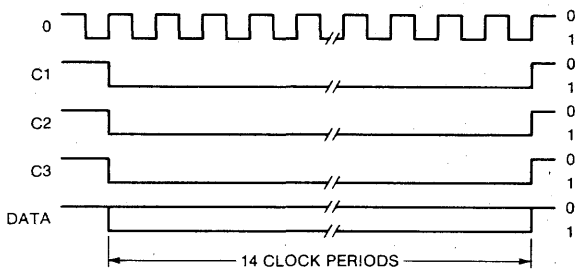


Fig.5 ACCEPT DATA

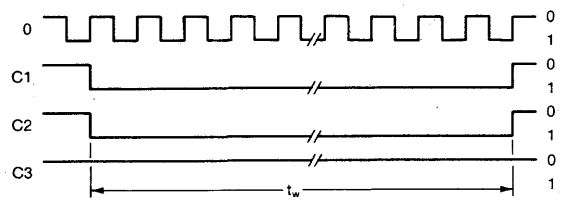


Fig.6 WRITE

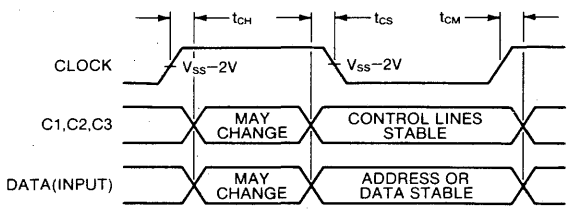


Fig.7 INPUT TIMING

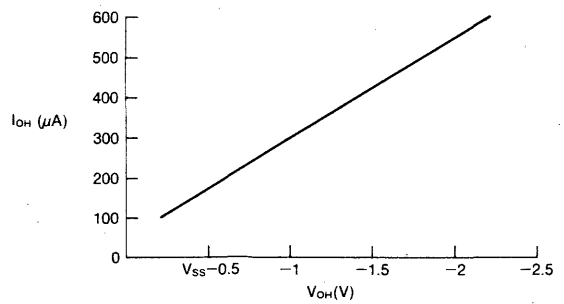


Fig.8 TYPICAL OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE

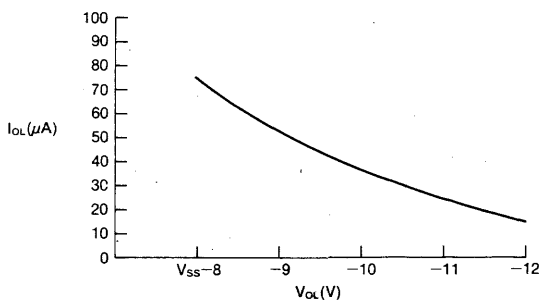


Fig.9 TYPICAL OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

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512 Bit Electrically Alterable Read Only Memories

FEATURES

- 32x16 Organization
- 5-Bit Addressing
- TTL Compatible
- Chip Select
- Word Alterable
- 10 Year Unpowered Data Storage
- 10 μs Access Time (ER2050)
- 3 μs Access Time (ER2051)
- Write/Erase Time 100ms/word (ER2050), 50ms/word (ER2051)
- +5, -28V Supplies
- No Voltage Switching Required

NOTE: Use ER2051 for all new designs.

DESCRIPTION

The ER2050 and ER2051 are fully decoded 32 × 16 electrically erasable and reprogrammable ROMs. Write, erase, and read voltages are switched internally via a 2-bit code applied to C1 and C2.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface at the gate insulator of the 512 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

Two TTL compatible control pins switch voltages internally for write, read and erase control.

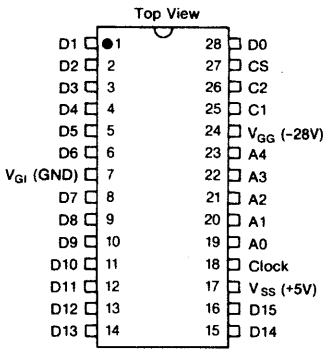
OPERATION

Data is stored in a two transistor memory cell. After the cell is preconditioned by an erase signal (which lowers the threshold of both transistors), data is written into one of the transistors lowering its threshold. A sensing flip flop is used to read the memory cell and presents a logic high or low to the output depending on which transistor is "written".

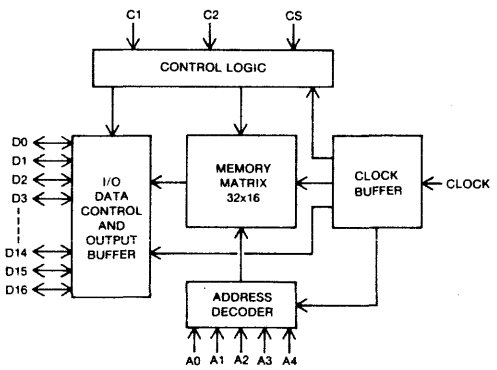
It is important to note two things: first, that an erase is required before a write to precondition the cell, and second, that after an erase, both transistors will have the same threshold voltage and valid data will not be present at the output.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



BLOCK DIAGRAM



PIN FUNCTIONS

A_0-A_4	5-Bit Word Address
D_0-D_{15}	Data input and output pins
CS	Chip Select. Chip selected at logic "1". When chip select is at logic "0", outputs are open circuit, read, write and erase are disabled. Power is reduced.
C1, C2	Mode Control Inputs C1 C2 1 1 Hold Mode: output data from previous read operation stored at output pins. (For the ER2050 only. This code is "read mode" for the ER2051). 0 1 Erase Mode: stored data is erased at addressed location. 1 0 Read Mode: addressed data read after clock pulse. Output data retained at output pins until next read operation. 0 0 Write Mode: input data written at addressed location. Clock not required. NOTE: Care must be exercised to ensure that CS is held at logic "0" during power up or power down to protect all addresses from spurious write or erase inputs.
CLK	Clock Input. Pulse to logic "1" for read operation. The clock may be repetitive or may simply be pulsed when data is to be read. When the clock is repetitive the ER2050 should be maintained in the standby mode when data is not being read, as every clock pulse will constitute a read operation. When the clock is not repetitive data will remain valid for 20 to 60 seconds; the outputs will then become open circuit until another clock pulse is received. The clock should not be repetitive for the ER2051.
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input.
V_{GG}	Power Supply Input. Normally at -28 volts.

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ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (with respect to Vss) ..... -35V to +0.3V
Storage temperature ..... -65°C to +150°C
Soldering temperature of leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

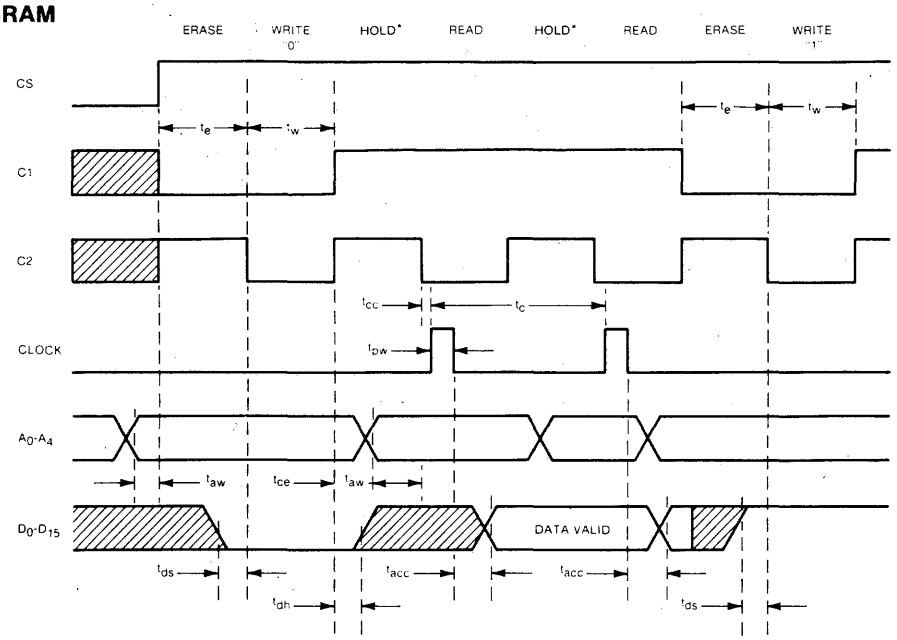
Standard Conditions (unless otherwise noted)

V_{SS} = +5V±5%
V_{GG} = -28V±5%
V_{Gi} = GND
Operating Temperature (T_A) = 0°C to +70C
Output Load = 100pF, 1 TTL load

Characteristic	Symbol	ER2050 Min	ER2050 Typ**	ER2050 Max	ER2051 Min	ER2051 Typ**	ER2051 Max	Units
DC CHARACTERISTICS								
Input Logic "1"	V_{IH}	V_{SS} -1.5	—	V_{SS} +0.3	V_{SS} -1.5	—	V_{SS} +0.3	Volts
Input Logic "0"	V_{IL}	-10.0	—	+0.8	-10.0	—	+0.8	Volts
Output Logic "1"	V_{OH}	V_{SS} -1.5	—	—	V_{SS} -1.5	—	—	Volts
Output Logic "0" (I_{OL} = 1.5mA)	V_{OL}	—	—	+0.8	—	—	+0.8	Volts
Power Supply Current								
Read	I_{GG}	—	-7.0	-8.5	—	—	-13.8	mA
Write	I_{GG}	—	-6.0	-7.5	—	—	-10.3	mA
Erase	I_{GG}	—	-4.0	-5.5	—	—	-10.3	mA
AC CHARACTERISTICS								
Access Time	t_{acc}	—	6.0	10.0	—	—	3.0	μsec
Clock Width	t_{pw}	.75	—	20.0	2.0	—	20.0	μsec
Write Time	t_w	100	—	200	50	—	200	msec
Erase Time	t_e	100	—	200	50	—	200	msec
Address-Clock Time	t_{cc}	100	—	—	100	—	—	nsec
Write/Erase-Address Time	t_{ce}	1	—	—	1	—	—	μsec
Address-Write/Erase Time	t_{aw}	50	—	—	50	—	—	nsec
Clock Period	t_c	10.0	—	—	3.5	—	—	μsec
Data Setup Time	t_{ds}	50	—	—	50	—	—	nsec
Data Hold Time	t_{dh}	50	—	—	50	—	—	nsec
Number of read accesses/ word between refresh	N_{RA}	10^{11}	—	—	10^{11}	—	—	—
Number of times word may be rewritten	N_W	—	—	10^6	—	—	10^6	—

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM



*Hold mode for 2050 only. When used with the 2051 this mode (C1 &C2 = 1's) is used as a Read Mode. With no clocks under this condition no Read will occur.

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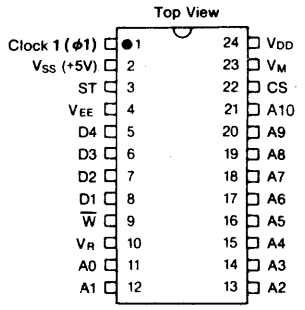
8192 Bit Electrically Alterable Read Only Memories

FEATURES

- 2048 x 4 Organization
- 11-Bit Binary Addressing
- Chip Select Input
- Electrically Reprogrammable
- 2.6 μs Access Time (ER2800)
- 1.65 μs Access Time (ER2805)
- 20 ms/4-bit Word Write Time
- 100 ms Simultaneous Erasure of All Data
- Minimum Data Retention—2 x 10^{11} Read Accesses/Word Between Refresh
- Three-State Outputs
- Unpowered, Nonvolatile Data Storage—10 Years at +70°C
- Control, Address and Data Inputs TTL Compatible.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



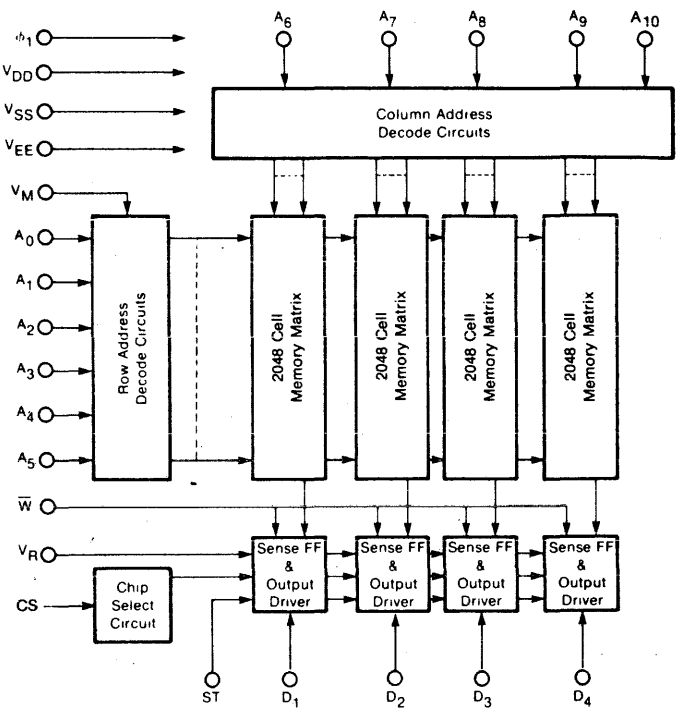
DESCRIPTION

The ER2800 and ER2805 are fully decoded 2048 × 4-bit electrically erasable and reprogrammable ROMs utilizing second-generation MNOS epitaxial processing technology.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface at the gate insulator of the 8192 MNOS memory transistors. When the writing voltage is removed, the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

Stored data may be accessed a minimum of 2 × 10^{11} times without refresh and is non-volatile in the unpowered state in excess of ten years. Data is erased by applying a V_{SS}-28V pulse to the erase substrate of the device. Data can be erased and rewritten up to a maximum of 10^6 times. All outputs are at logic high when the device is in the erased state.

BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs or outputs relative to V_{SS} . . . . . +0.3V to -30V
Operating ambient temperature . . . . . 0°C to +70°C
Storage temperature . . . . . -65°C to +150°C
Soldering temperature of leads (10 seconds) . . . . . +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

RECOMMENDED OPERATING CONDITIONS, T_A = 0°C to +70°C

Symbol	Parameter	Erase Mode			Write Mode			Read Mode			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{DD}	Supply Voltage	4.75	V_{SS}	V_{SS}+0.3	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{SS}	Substrate supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_M	Memory voltage	—	V_{SS}	—	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-10.5	V_{SS}-10	V_{SS}-9.5	V
V_R	Reference voltage	—	V_{SS}	—	V_{SS}	V_{SS}	V_{SS}	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{EEH}	Erase substrate input high	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V
V_{EEL}	Erase substrate input low	V_{SS}-29	V_{SS}-28	V_{SS}-27	Not Applicable			Not Applicable			V
V_{WH}	Write control input high	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{WL}	Write control input low	V_{SS}-29	—	V_{SS}-4.4	V_{SS}-29	—	V_{SS}-4.4	Not Applicable			V
$V\phi_H$	ϕ_1 input high voltage	—	V_{SS}	—	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V
$V\phi_L$	ϕ_1 input low voltage	Not Applicable			V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-25	V_{SS}-19	V_{SS}-18	V
V_{STH}	Strobe input high voltage	—	V_{SS}	—	Not Applicable			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{STL}	Strobe input low voltage	Not Applicable			V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-25	V_{SS}-19	V_{SS}-18	V
V_{IH}	Address and CS input high	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{IL}	Address and CS input low	Don't Care			V_{DD}	—	V_{SS}-4.4	V_{DD}	—	V_{SS}-4.4	V
V_{DH}	Data input high voltage	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	Not Applicable			V
V_{DL}	Data input low voltage	Don't Care			V_{DD}	—	V_{SS}-4.4	Not Applicable			V

STATIC ELECTRICAL CHARACTERISTICS, T_A = 0°C to +70°C (NO EXTERNAL LOADS EXCEPT AS NOTED)

Symbol	Parameter	Conditions All Pins at V_{SS} Unless Noted	Min	Typ	Max	Unit
I_{IN}	Input leakage current (except pins 1, 2, 4, 5, 6, 7, 8, and 24) at V_{SS}-15V	$\phi1$=V_{DD}=V_{SS}-20	—	—	-2.0	μA
$I\phi_1$	ϕ_1 leakage current at V_{SS}-29V	V_{DD}=V_{SS}-29, ST=$\overline{W}$=V_{SS}-25	—	—	-200	μA
I_O	Output leakage current at V_{SS}-15V	Chip deselected	—	—	-10.0	μA
I_{EEL}	Erase leakage current at V_{SS}-28V	W=ST=V_{SS}-25	—	—	-200	μA
I_{DD1}	V_{DD} supply current - read mode at V_{SS}-19V — ER2800	Outputs open (See Figure 6)	—	8.5	12	mA
	V_{DD} supply current - read mode at V_{SS}-19V — ER2805		—	11	13	mA
I_{DD2}	V_{DD} supply current - Write mode at V_{SS}-28V — ER2800	Outputs open (See Figure 5)	—	18	25	mA
	V_{DD} supply current - Write mode at V_{SS}-28V — ER2805		—	24	27	mA
I_{OH}	Data output high voltage - TTL load	One Series 7400 TTL load with R_S = 1KΩ, V_{CC}=V_{SS}	V_{SS}-1.5	—	—	V
I_{OL}	Data output low voltage - TTL load	(See TTL Notes)	—	—	V_{SS}-6.6	V
V_{OH}	Data Output high voltage - MOS		V_{SS}-1.5	—	—	V
V_{OL}	Data Output low voltage — MOS	C_L=100 pF	—	—	V_{SS} -7	V
T_S	Unpowered nonvolatile data storage	Typical write conditions	10	—	—	Years

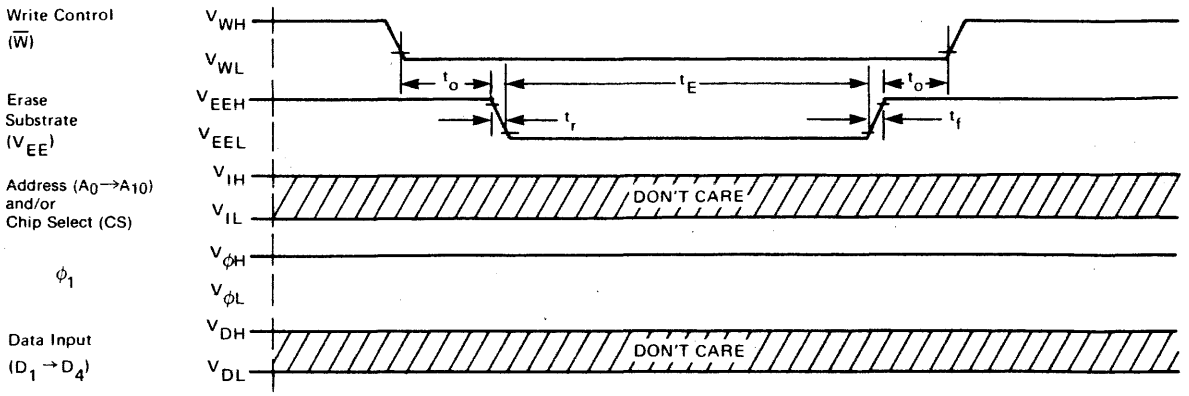
CAPACITANCE AT V_{IN} = V_{SS}, ALL OTHER PINS GROUNDED (V_{SS}), f=1 MHz

Symbol	Parameter	Min	Typ	Max	Unit
C_I	Address and chip select input capacitance	—	5	7	pf
C_W	Write control input capacitance	—	10	20	pf
C_{ST}	Strobe input capacitance	—	10	15	pf
$C\phi_1$	ϕ_1 Input Capacitance	—	40	50	pf
C_{EE}	Erase substrate capacitance	—	600	700	pf
C_D	Data input/output capacitance	—	6	10	pf

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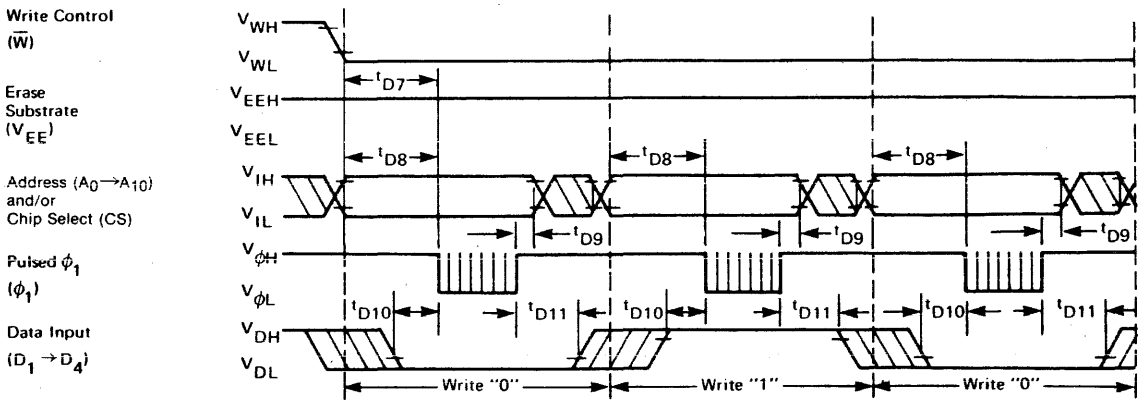
ERASE CYCLE CHARACTERISTICS, T_A = 0°C to +70°C

Symbol	Parameter	Min	Typ	Max	Units
t_E	V_{EE} erase pulse width	100	—	1000	ms
t_r, t_f	V_{EE} rise time, V_{EE} fall time	0.01	—	1.0	ms
t_o	Write-erase overlap	10	—	—	μs



WRITE CYCLE CHARACTERISTICS, T_A=0°C to +70°C ($ST=V_{DD}$) (SEE NOTE 3)

Symbol	Parameter	Min	Typ	Max	Units
$N\phi_W$	Number of ϕ_1 write pulses at 100 μs ±10%, 5 μs min. dead time between pulses)	100	200	300	Pulses
t_{D7}	Write control rise to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D8}	Address change and chip select fall to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D9}	Pulsed ϕ_1 fall to address and chip select change delay	0.0	—	—	μs
t_{D10}	Data input change to pulsed ϕ_1 rise delay	0.0	—	—	μs
t_{D11}	Pulsed ϕ_1 fall to data input change delay	0.0	—	—	μs
N_W	Number of times word may be rewritten	—	—	10^6	—

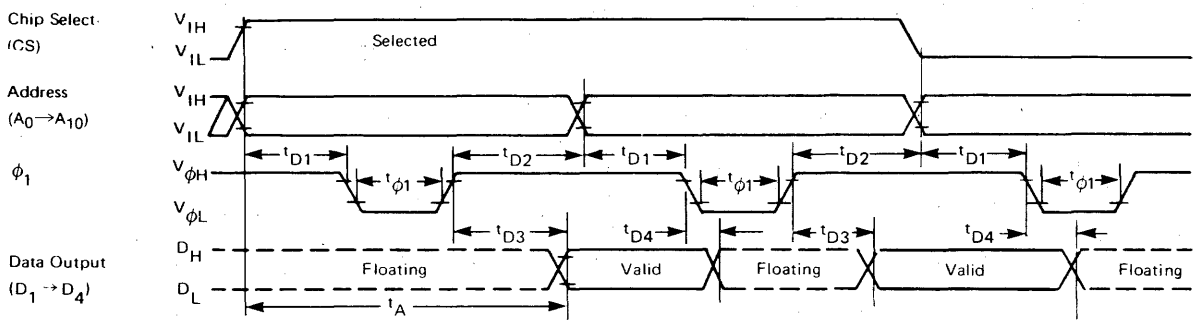


NOTES:
1. Due to the dynamic nature of the circuit a "ϕ_1 NOT" time in excess of 40 μsec. may result in a floated output condition. Consequently data must be resampled with a 40 μsec. time period following the fall of ϕ_1 to ensure its validity.
2. Several seconds may be required following a programming operation for the circuit to become operable in the read mode. If data is to be verified immediately following programming, a forward current of +1 mA ±10% may be forced into the erase substrate junction (Pin 4, V_{EE}), for a period not to exceed 10 milliseconds, to quickly dissipate charge trapped at internal circuit nodes.
3. Maximum power dissipation occurs during programming. When programming multichip systems where the application of programming voltages is required for several minutes, forced air cooling is recommended to reduce package temperature. Power is not reduced when chip is deselected.
4. All typical values are at +25°C and nominal voltages.

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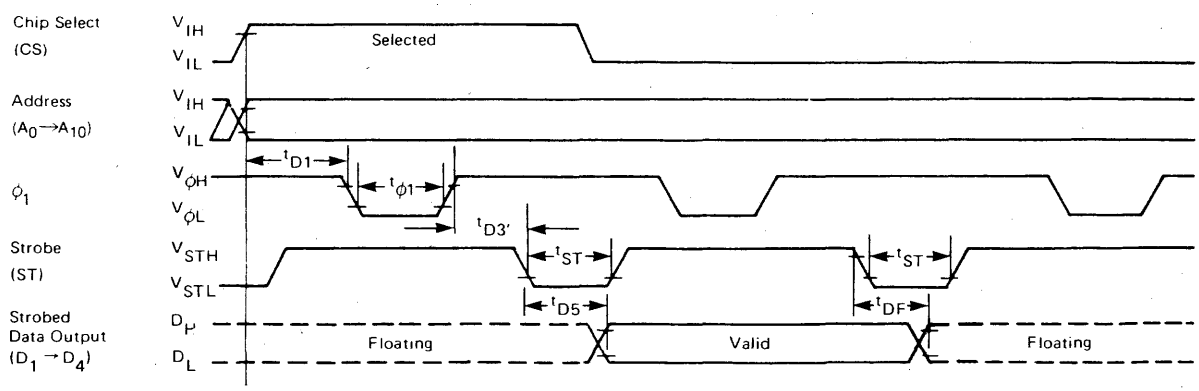
READ CYCLE CHARACTERISTICS FOR NON-STROBED OPERATION, T_A = 0°C to +70°C (ST = V_{DD})

Symbol	Parameter (See Figures 1 through 4)	ER2800 Min	ER2800 Typ	ER2800 Max	ER2805 Min	ER2805 Typ	ER2805 Max	Units
T_A	Access time (strobe=V_{DD})	—	2.0	2.6	—	—	1.65	μs
$t_{\phi 1}$	Pulse width (rise and fall times ⩽50ns) (See Note 1)	950	—	2000	700	—	2000	ns
t_{D1}	Address and chip select change to ϕ_1 rise delay	600	—	—	400	—	—	ns
t_{D2}	ϕ_1 Fall to address and chip select change delay	0.0	—	—	0.0	—	—	μs
t_{D3}	ϕ_1 Fall to data output valid delay (See Notes 1 and 2)	—	—	950	—	—	550	ns
t_{D4}	ϕ_1 Rise to floated output delay	—	—	300	—	—	300	ns
N_{RA}	Number of read accesses/word between refresh	2×10^{11}	—	—	2×10^{11}	—	—	—



READ CYCLE CHARACTERISTICS FOR STROBED OPERATION, T_A = 0°C to +70°C

Symbol	Parameter (See Figures 1 through 4)	ER2800 Min	ER2800 Typ	ER2800 Max	ER2805 Min	ER2805 Typ	ER2805 Max	Units
$t_{\phi 1}$	ϕ_1 Pulse width (rise and fall times ⩽50ns) (See Note 1)	950	—	2000	700	—	2000	ns
t_{D1}	Address and chip select change to ϕ_1 rise delay	600	—	—	400	—	—	ns
$t_{D3'}$	ϕ_1 Fall to strobe rise delay	0.75	—	—	0.75	—	—	μs
t_{ST}	Strobe pulse width (rise and fall ⩽50 ns)	500	—	—	500	—	—	ns
t_{D5}	Strobe rise to strobed data output valid delay (See Notes 1 and 2)	—	—	500	—	—	500	ns
t_{DF}	Strobe rise to strobed floated output on deselect delay	—	—	300	—	—	300	ns
N_{RA}	Number of read accesses/word between refresh	2×10^{11}	—	—	2×10^{11}	—	—	—



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ER2800 TYPICAL OPERATING CHARACTERISTICS, T_A = +25°C and +70°C, R_S = 2K Ohms, V_{SS} = OV

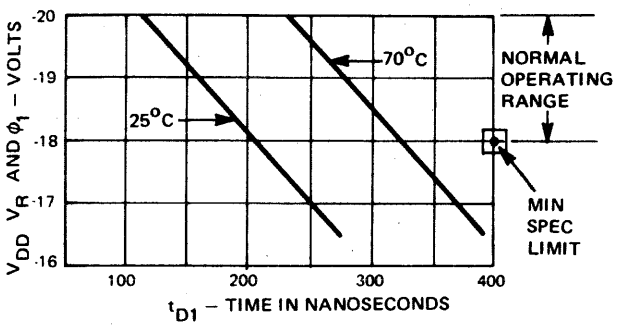


Fig. 1 TYPICAL ϕ1 DELAY IN NANOSECONDS vs. POWER SUPPLY VOLTAGE (ER2800)

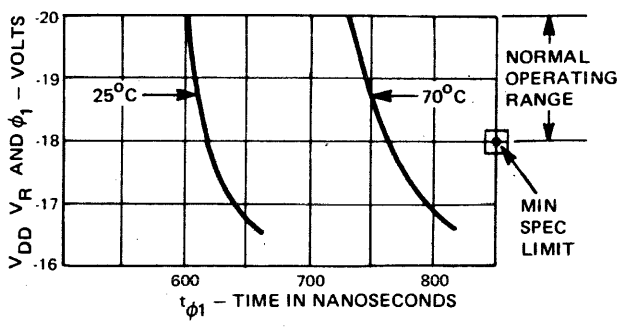


Fig. 2 TYPICAL ϕ1 WIDTH IN NANOSECONDS vs. POWER SUPPLY VOLTAGES (ER2800)

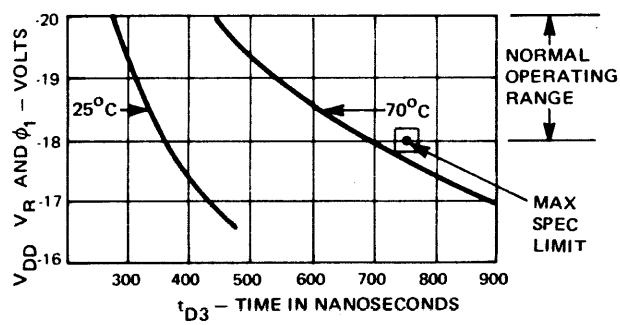


Fig. 3 TYPICAL DATA SETUP TIME IN NANOSECONDS vs. POWER SUPPLY VOLTAGES (ER2800)

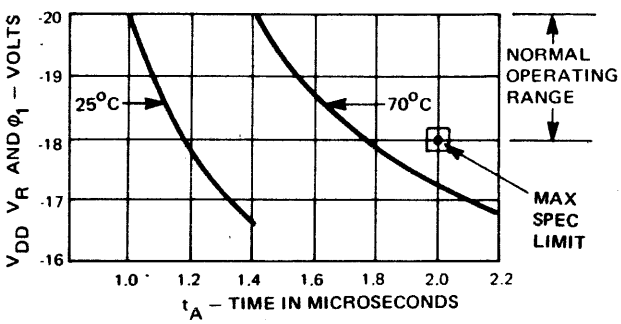


Fig. 4 TYPICAL ACCESS TIME IN MICROSECONDS vs. POWER SUPPLY IN VOLTAGES (ER2800)

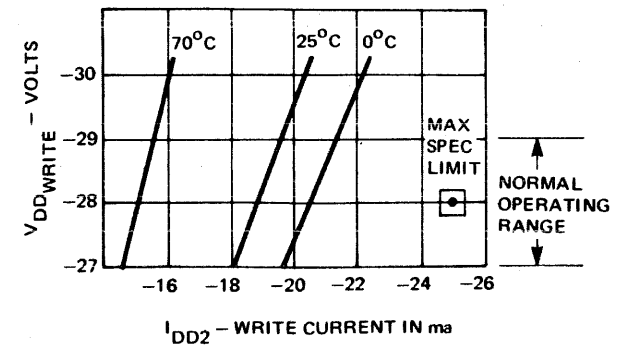


Fig. 5 TYPICAL WRITE CURRENT IN MILLIAMPS vs. POWER SUPPLY VOLTAGES (ER2800) (Deselected I_{DD2} = ½ Graph I_{DD2})

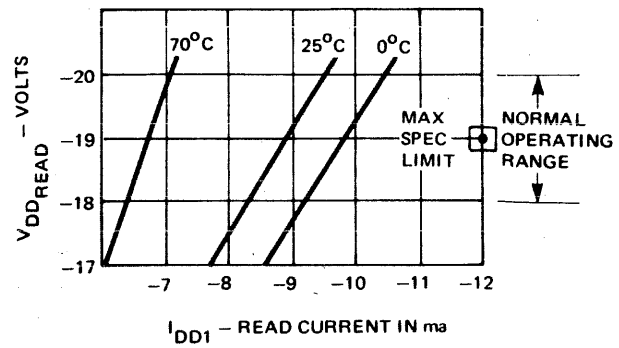


Fig. 6 TYPICAL READ CURRENT IN MILLIAMPS vs. POWER SUPPLY VOLTAGE (ER2800) (Chip selected or deselected)

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PIN FUNCTIONS

Chip Select (CS)
Must be in the high state to enable the data output terminals or write data into the device.

Data Input/Output (D1—D4)
D1 through D4 are bidirectional data terminals. Data are entered on these terminals during the write cycle and read out during the read cycle. When deselected, these terminals are in a floating condition.

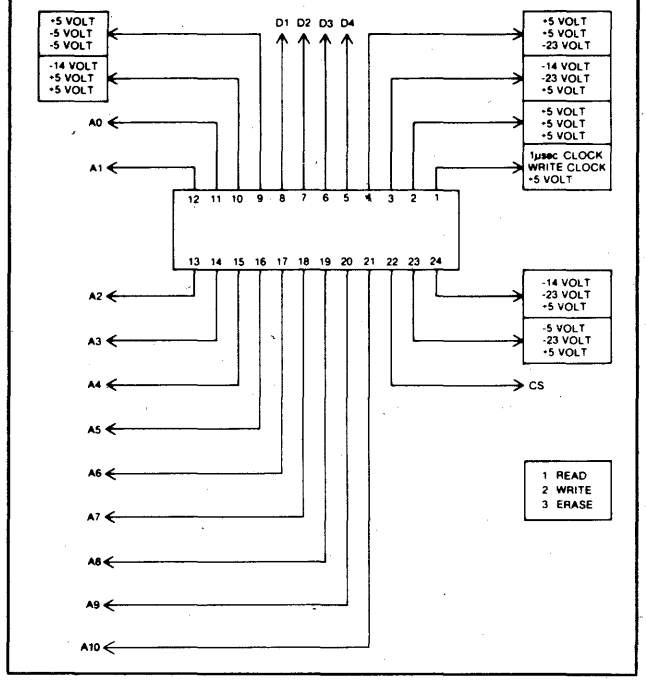
Write Control ($\overline{W}$)
The write control terminal must be in the low state in order to write data into the device.

Strobe (ST)
A strobe input is provided for delayed data clockout. In applications where this feature is not desired, the strobe terminal should be maintained at VDD throughout the entire read cyle. The ST input is high-level and not TTL-compatible.

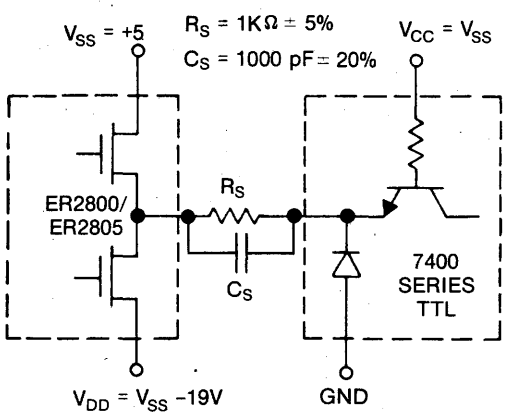
Phase One (ϕ1)
During the write operation, multiple 100μs pulses must be applied to the ϕ1 terminal to fully shift the memory transistor threshold voltge to its most negative state. This is required for voltage bootstrapping in the row-selection circuitry. The ϕ1 input is high level and not TTL-compatible.

NOTE: All control, address and data inputs are TTL-compatible with pull-up resistors.

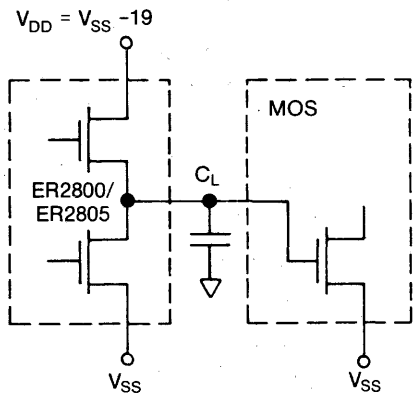
ER2800/ER2805 OPERATION



TTL INTERFACE



MOS INTERFACE



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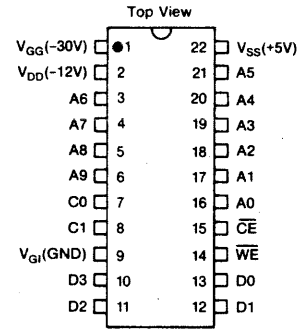
4096 Bit High Speed Electrically Alterable Read Only Memories

FEATURES

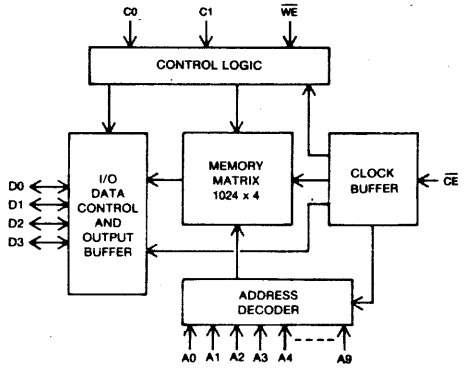
- 1024 × 4 Organization, Fully Decoded
- Single Word or Block Electrically Erasable
- TTL Compatible with Resistor Pull-ups
- Three State Output
- ER3400: 650ns Access Time
- ER3401: 950ns Access Time
- 1.8 us Cycle Time
- 10 ms Word or Block Erase Time
- 1 ms Write Time
- 22 Pin DIP
- P-Channel Metal Gate MNOS Technology
- 0°C to 70°C Operation
- +5, -12, -30V Power Supplies
- 10^5 Erase-Write Cycles per Word
- 2×10^{11} Read Cycles per Word
- 10 Year Unpowered Nonvolatile Data Storage — 10 Years

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM



DESCRIPTION

The ER3400 and ER3401 are word alterable ROMs intended for use as read-mostly memories. Each operates with one clock, CHIP ENABLE ($\overline{CE}$), which also serves for chip selection. All other pins of each device can be paralleled with other EAROMs.

Any one of four possible operating modes can be selected by setting the proper binary code on the C0-C1 control lines and pulsing the device with $\overline{CE}$. The four modes are Read, Write, Word Erase and Block Erase. The ER3400/3401 will sense the control lines and change modes only when pulsed by $\overline{CE}$. When in the Read mode, data is read during each $\overline{CE}$ pulse. Writing or erasing of a word continues for as long as the device is in the Write or Erase mode. Each write or erase word cycle must be ended by a dummy read operation.

A WRITE ENABLE ($\overline{WE}$) input pulse indicates to the ER3400/3401 that the data on the D_0-D_3 data input/output lines is valid input data. This data is then stored internally for use during the write operation.

No particular order of power supply sequencing on or off is required for the ER3400. Circuits are provided to force the device into the read mode during power turn on. Erasing and writing are inhibited if V_{DD} or V_{GG} are not at proper operating levels.

For the ER3401, V_{GG} must be turned on after V_{CC} is stable and removed before V_{CC} is turned off.

PIN FUNCTIONS

A_0-A_9	10-Bit Word Address
D_0-D_3	Data input and output pins
$\overline{CE}$	Chip Enable. Chip selected when $\overline{CE}$ is pulsed to logic "0".
C_0, C_1	Mode Control Inputs
	C0 C1
	0 1 Block Erase Mode: erase operation performed on all words.
	1 1 Word Erase Mode: stored data is erased at addressed location.
	0 0 Read Mode: addressed data read after leading edge of $\overline{CE}$ pulse.
	1 0 Write Mode: input data written at addressed location.
$\overline{WE}$	Write Enable. Input data read when $\overline{WE}$ is pulsed to logic "0".
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input
V_{DD}	Power Supply Input. Normally at -12 volts.
V_{GG}	Power Supply Input. Normally at -30 volts.

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ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (with respect to V_{SS}) ..... -40V to +0.3V
Storage temperature (with data retention) ..... -40°C to +70°C
Storage temperature (without data retention) ..... -65°C to +150°C
Soldering temperature of leads (10 seconds) .....+300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = +5V ±5%
V_{DD} = -12V ±5%
V_{GG} = -30V ±5%
V_{GI} = GND
Operating Temperature (T_A) = 0°C to =70°C

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input Logic "1"	V_{IH}	V_{SS}-1.5	—	V_{SS}+0.3	Volts	
Input Logic "0"	V_{IL}	-10	—	0.8	Volts	
Output Logic "1"	V_{OH}	V_{SS}-1.5	—	—	Volts	I_{OH} = -2mA
Output Logic "0"	V_{OL}	—	—	0.4	Volts	I_{OL} = 2mA
Control Input Leakage	I_{LC}	—	—	-2.0	μA	V_{IN} = V_{SS} -15 Volts
Data Input Leakage	I_{LD}	—	—	-10.0	μA	V_{IN} = V_{SS} -15 Volts
Power Supply Current						
V_{DD} Supply Current: Chip selected	I_{DD}	—	—	-25.0	mA	V_{DD} = V_{SS} -17 Volts
Chip de-selected	I_{DD}	—	—	-7.0	mA	V_{DD} = V_{SS} -17 Volts
V_{GG} Supply Current	I_{GG}	—	—	-3.0	mA	V_{GG} = V_{SS} -35 Volts
V_{SS} Supply Current: Chip selected	I_{SS}	—	—	-29.0	mA	V_{DD} = V_{SS} -17V, V_{GG} = V_{SS} -35V
Chip de-selected	I_{SS}	—	—	-11.5	mA	V_{DD} = V_{SS} -17V, V_{GG} = V_{SS} -35V
AC CHARACTERISTICS						
Input capacitance - control inputs	C_I	—	6	8	pf	
Input capacitance - data inputs	C_D	—	8	10	pf	
Read Mode Characteristics						
Address and control to $\overline{CE}$	t_{D1}	0	—	—	ns	
Address and control hold time	t_{D2}	250	—	—	ns	
$\overline{CE}$ to Data I/O Off	t_{D3}	50	—	200	ns	
$\overline{CE}$ high	t_{D4}	900	—	—	ns	
Access time: ER3400	t_A	—	—	650	ns	RL = 2K to V_{SS}, CL = 100pf
ER3401	t_A	—	—	950	ns	RL = 2K to V_{SS}, CL = 100pf
$\overline{CE}$ pulse width: ER3400	$t_{\overline{CE}}$	650	—	100000	ns	
ER3401	$t_{\overline{CE}}$	950	—	100000	ns	
Read cycle time	t_{CY}	1650+t_r+t_f	—	—	—	
$\overline{CE}$ rise, fall time	t_r, t_f	0	—	100	ns	
Write/Erase Mode Characteristics						
Address and control to $\overline{CE}$	t_{D11}	0	—	—	ns	
Address and control hold time	t_{D12}	250	—	—	ns	
$\overline{CE}$ fall to $\overline{WE}$ fall delay	t_{D13}	0	—	—	ns	$\overline{WE}$ rise may overlap $\overline{CE}$ rise by a maximum of 50ns.
$\overline{WE}$ rise to $\overline{CE}$ rise delay	t_{D14}	-50	—	—	ns	$\overline{WE}$ rise may overlap $\overline{CE}$ rise by a maximum of 50ns.
Data stable to $\overline{WE}$	t_{D15}	0	—	—	ns	$\overline{WE}$ rise may overlap $\overline{CE}$ rise by a maximum of 50ns.
$\overline{WE}$ rise to End of Data Stable	t_{D16}	50	—	—	ns	$\overline{WE}$ rise may overlap $\overline{CE}$ rise by a maximum of 50ns.
$\overline{CE}$ pulse width: ER3400	$t_{\overline{CE}}$	650	—	100000	ns	
ER3401	$t_{\overline{CE}}$	950	—	100000	ns	
WE pulse width	$t_{\overline{WE}}$	400	—	—	ns	
Write time	t_W	1	—	2	ms	
Erase time	t_E	10	—	20	ms	

**Typical values are at +25°C and nominal voltages.

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TIMING DIAGRAMS

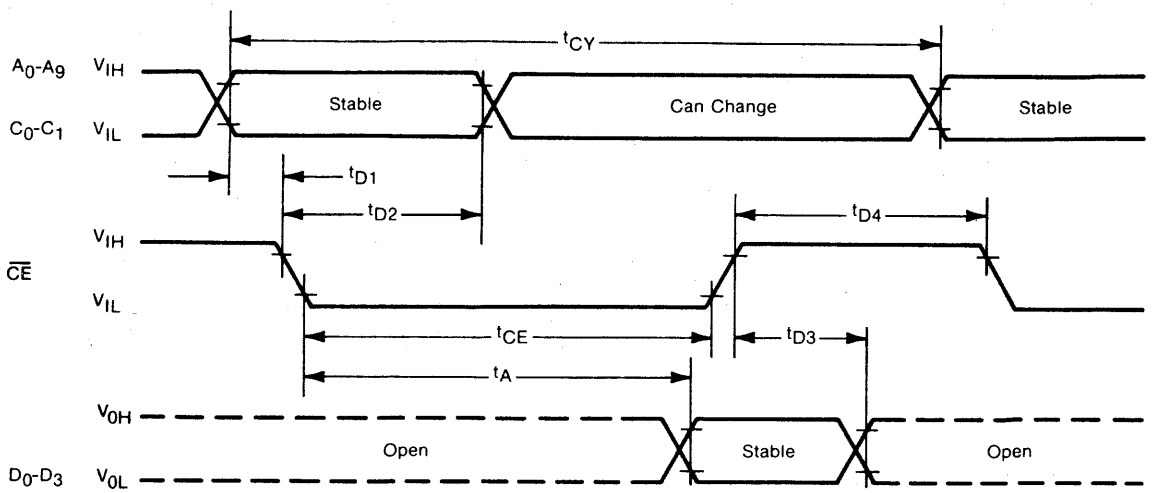


Fig.1: READ MODE TIMING

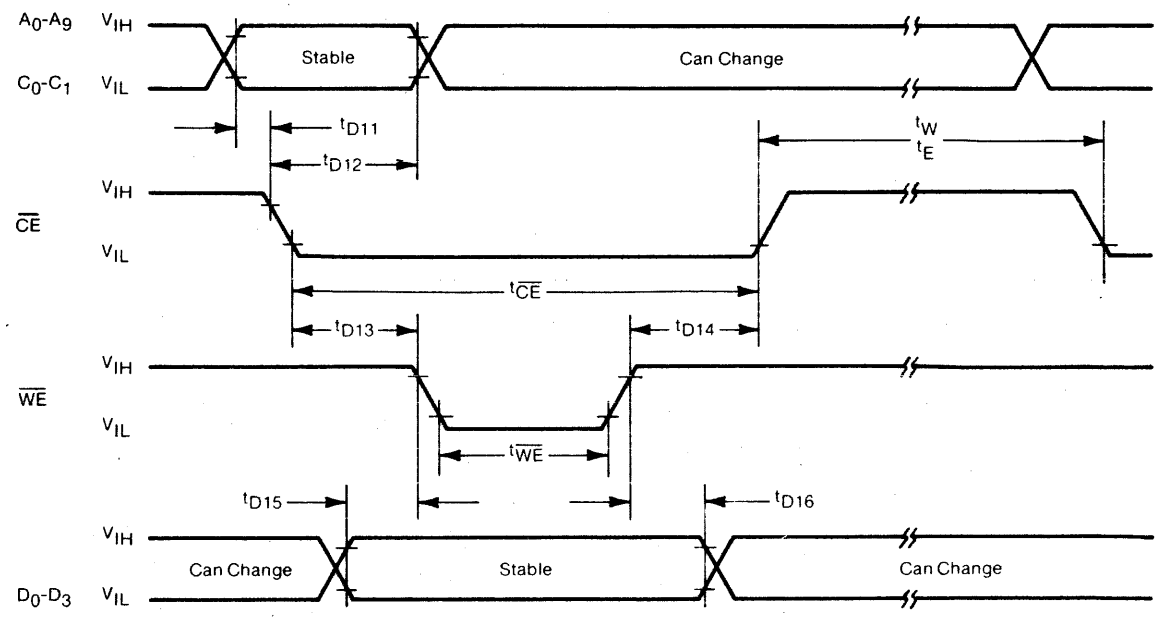


Fig.2: WRITE AND ERASE MODE TIMING

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION

Product Brief

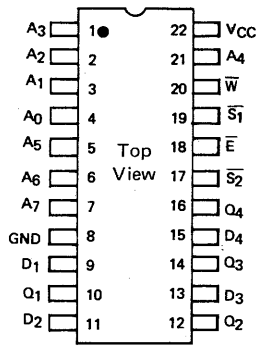
HM-6551

256 x 4 CMOS RAM

Features

- LOW STANDBY POWER . . . . . 55 μW MAX
- LOW OPERATING POWER . . . . . 22mW/MHZ MAX
- FAST ACCESS TIME . . . . . 220nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 volts MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 2 TTL LOADS
- INTERNAL LATCHED CHIP SELECT
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTERS
- LATCHED OUTPUTS
- THREE STATE OUTPUTS
- MILITARY AND INDUSTRIAL TEMPERATURE RANGES

Pinout



A – ADDRESS INPUT
E – CHIP ENABLE
S – CHIP SELECT
W – WRITE ENABLE
D – DATA INPUT
Q – DATA OUTPUT

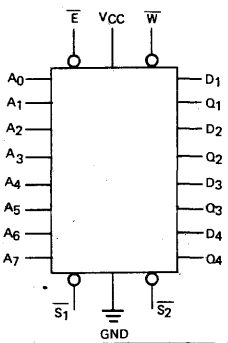
Description

The HM – 6551 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

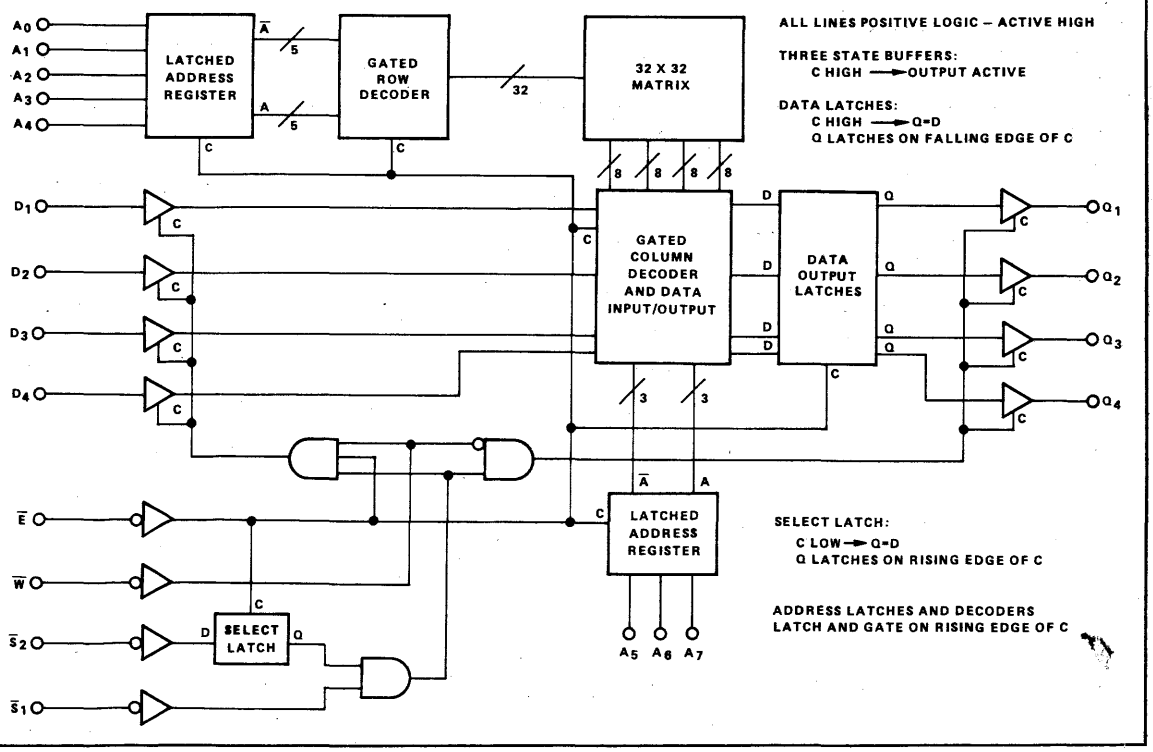
On chip latches are provided for addresses and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM – 6551 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Logic Symbol



Functional Diagram



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Refer to Harris Sales Offices for additional specifications.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION

Preliminary

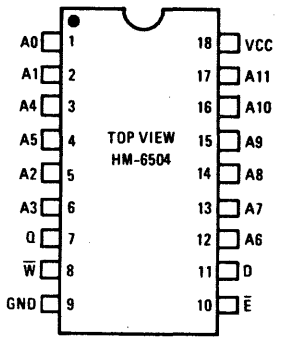
HM-6504

4096 x 1 CMOS RAM

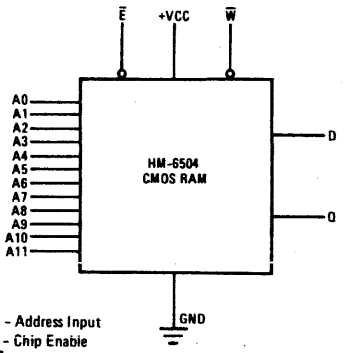
Features

- LOW POWER STANDBY . . . . . ≪1mW MAX.
- LOW POWER OPERATION . . . . . 35mW/MHz MAX.
- EXTREMELY LOW SPEED POWER PRODUCT
- DATA RETENTION . . . . . @ 2.0V MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- THREE-STATE OUTPUT
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME . . . . . 300nsec MAX.
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Pinout



Logic Symbol



A - Address Input
Ē - Chip Enable
W̄ - Write Enable
D - Data Input
Q - Data Output

Description

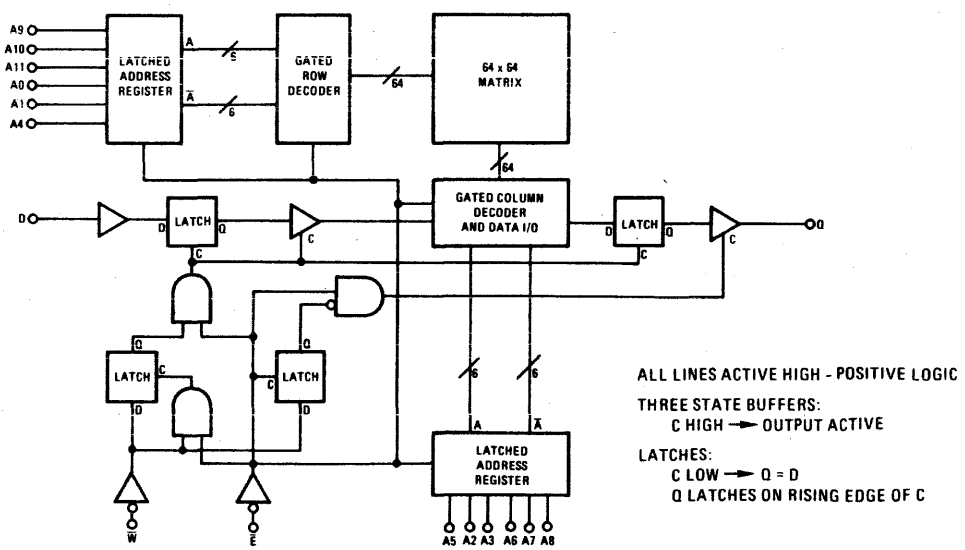
The HM-6504 is a 4096 x 1 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays.

The HM-6504 is a truly static RAM and may be maintained in any state for an indefinite period of time.

Data retention supply voltage and supply current are guaranteed over temperature.

Functional Diagram



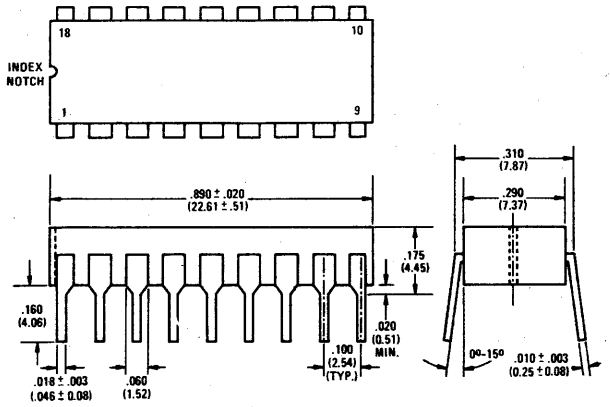
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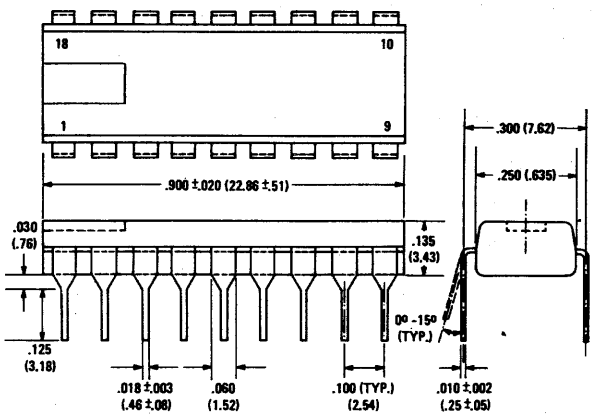
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Packaging

18 LEAD CERDIP



18 LEAD EPOXY D.I.P.



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ± .010 (± 0.25mm) unless otherwise shown.

Ordering Information

Example: HM 1 – 6504 – 9

- HM: HARRIS MEMORY
- 1: PACKAGE
- 6504: DEVICE
- 9: VERSION/TEMP. RANGE

		TEMPERATURE RANGE		
		MILITARY	INDUSTRIAL	COMMERCIAL
PACKAGE		- 2	- 9	- 5
FLAT PACK	9 -	YES	NO	NO
CERDIP	1 -	YES	YES	YES
EPOXY	3 -	NO	YES	YES

NOTICE: Harris Semiconductor's products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders.

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Preliminary

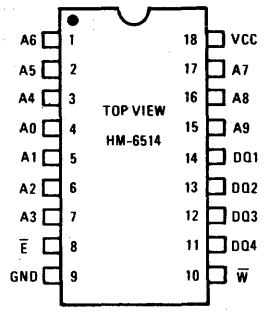
HM-6514

1024 x 4 CMOS RAM

Features-

- LOW POWER STANDBY . . . . . ≪ 1mW MAX.
- LOW POWER OPERATION. . . . . 35mW/MHz MAX.
- DATA RETENTION . . . . . @ 2.0 VOLTS MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- COMMON DATA IN/OUT
- THREE-STATE OUTPUTS
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME . . . . . 300nsec MAX.
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Pinout



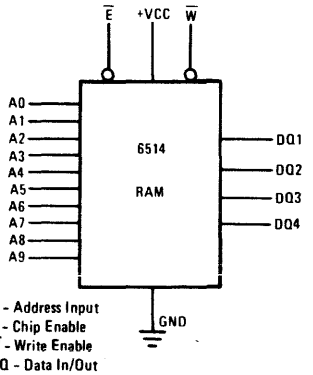
Description

The HM-6514 is a 1024 x 4 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

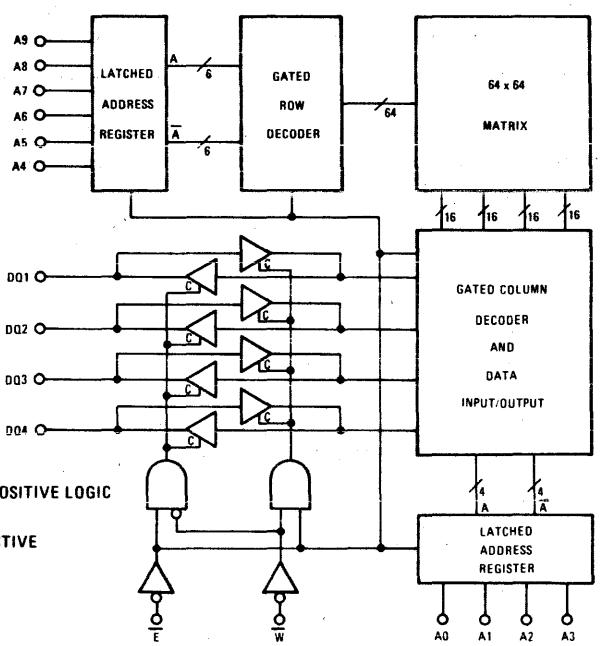
On chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data outputs can be forced to a high impedance state for use in expanded memory systems.

The HM-6514 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Logic Symbol



Functional Diagram



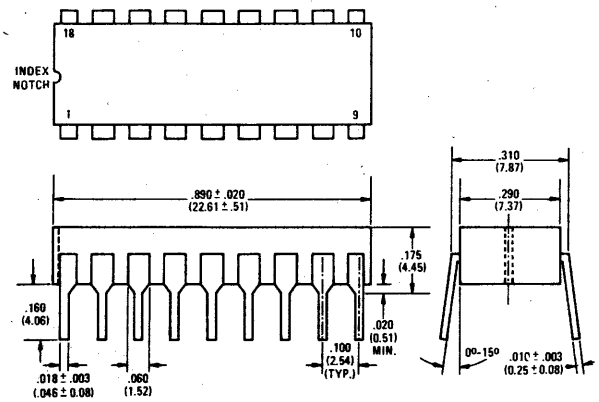
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Refer to Harris Sales Offices for additional specifications.

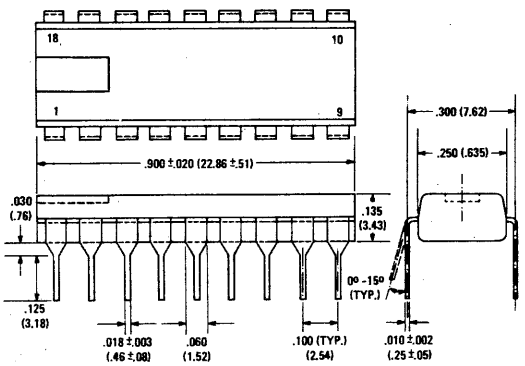
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Packaging

18 LEAD CERDIP



18 LEAD EPOXY D.I.P.



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

Ordering Information

Example: HM 1 – 6514 – 9

- HM: HARRIS MEMORY
- 1: PACKAGE
- 6514: DEVICE
- 9: VERSION/TEMP. RANGE

TEMPERATURE RANGE

PACKAGE		MILITARY -2	INDUSTRIAL -9	COMMERCIAL -5
FLAT PACK	9-	YES	NO	NO
CERDIP	1-	YES	YES	YES
EPOXY	3-	NO	YES	YES

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Product Brief

HM-6508

1024 x 1 CMOS RAM

Features

- LOW STANDBY POWER . . . . . 55μW MAX
- LOW OPERATING POWER . . . . . 22mW/MHz MAX
- FAST ACCESS TIME . . . . . 180nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 volts MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTER
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- THREE-STATE OUTPUTS
- 16 PIN PACKAGE FOR HIGH DENSITY

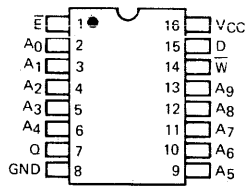
Description

The HM–6508 is a 1024 by 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM–6508 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

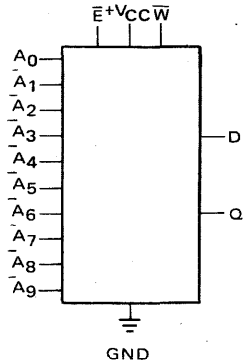
Pinouts



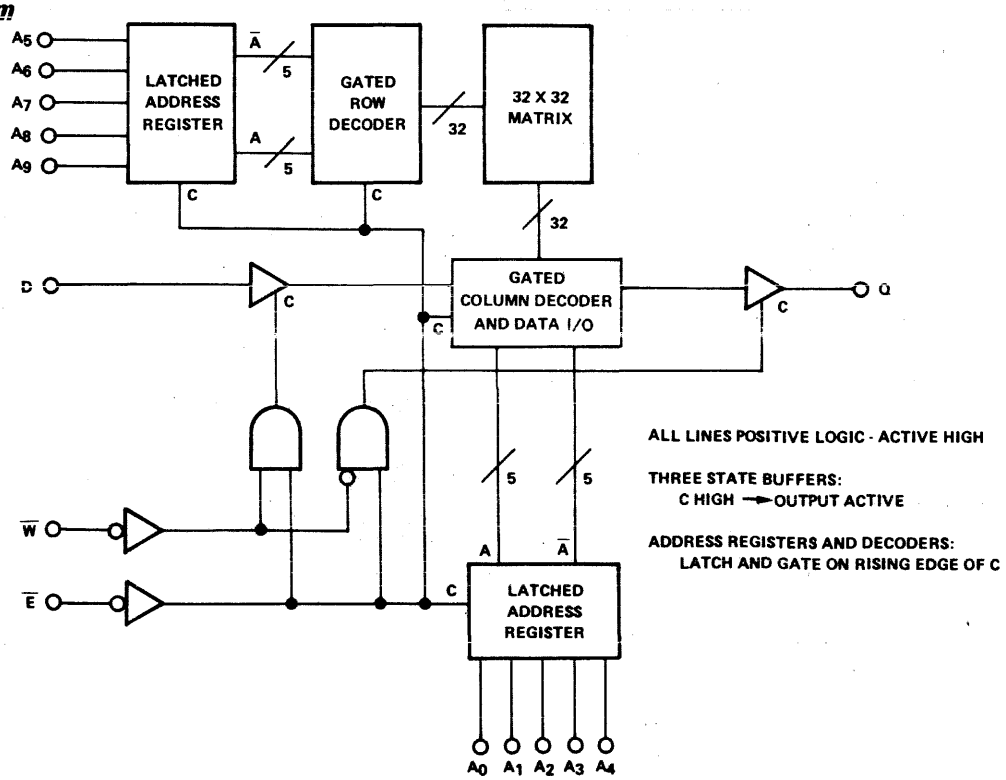
TOP VIEW

A – ADDRESS INPUT
Ē – CHIP ENABLE
W̄ – WRITE ENABLE
D – DATA INPUT
Q – DATA OUTPUT

Logic Symbol



Functional Diagram



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HARRIS SEMICONDUCTOR PRODUCTS DIVISION

Product Brief

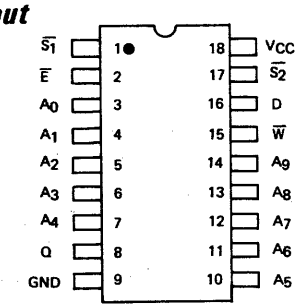
HM-6518

1024 x 1 CMOS RAM

Features

- LOW STANDBY POWER . . . . . 55 μW MAX
- LOW OPERATING POWER . . . . . 22mW/MHZ MAX
- FAST ACCESS TIME . . . . . 180nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 volts MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTER
- TWO CHIP SELECTS FOR EASY ARRAY EXPANSION
- THREE-STATE OUTPUTS
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE

Pinout



A – ADDRESS INPUT
Ē – CHIP ENABLE
S̄ – CHIP SELECT
W̄ – WRITE ENABLE
D – DATA INPUT
Q – DATA OUTPUT

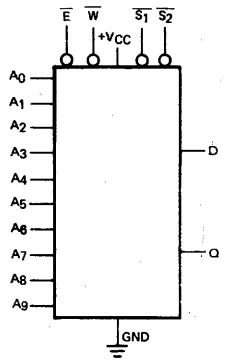
Description

The HM – 6518 is a 1204 by 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

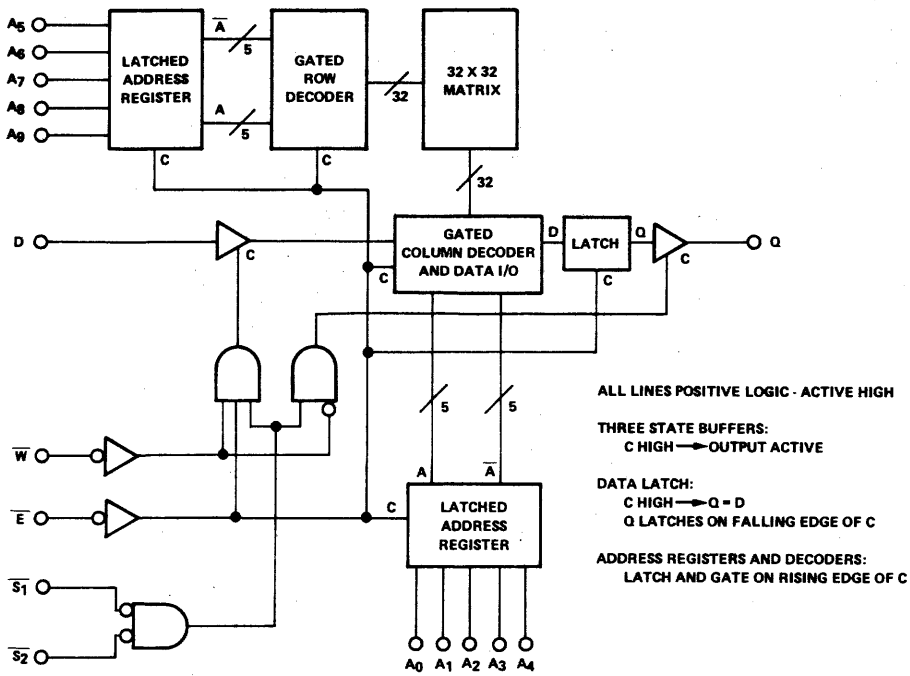
On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM – 6518 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Logic Symbol



Functional Diagram



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Refer to Harris Sales Offices for additional specifications.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION

Product Brief

HM-6561

256 x 4 CMOS RAM

Features

- LOW STANDBY POWER . . . . . 55 μW MAX
- LOW OPERATING POWER . . . . . 22mW/MHZ MAX
- FAST ACCESS TIME . . . . . 220nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 2 TTL LOADS
- ON CHIP ADDRESS REGISTERS
- COMMON DATA IN/OUT
- THREE-STATE OUTPUTS
- EASY MICROPROCESSOR INTERFACING
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE

Description

The HM – 6561 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

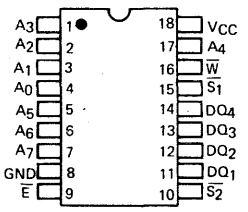
On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

The HM – 6561 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

The HM – 6561 is pin for pin replaceable with the HM – 6661, a 256 X 4 CMOS PROM. This allows a single memory board design with any organization of RAM – ROM.

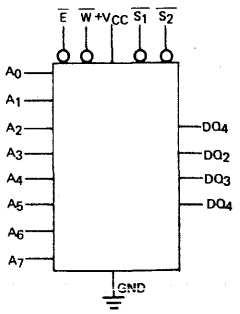
Pinout

TOP VIEW

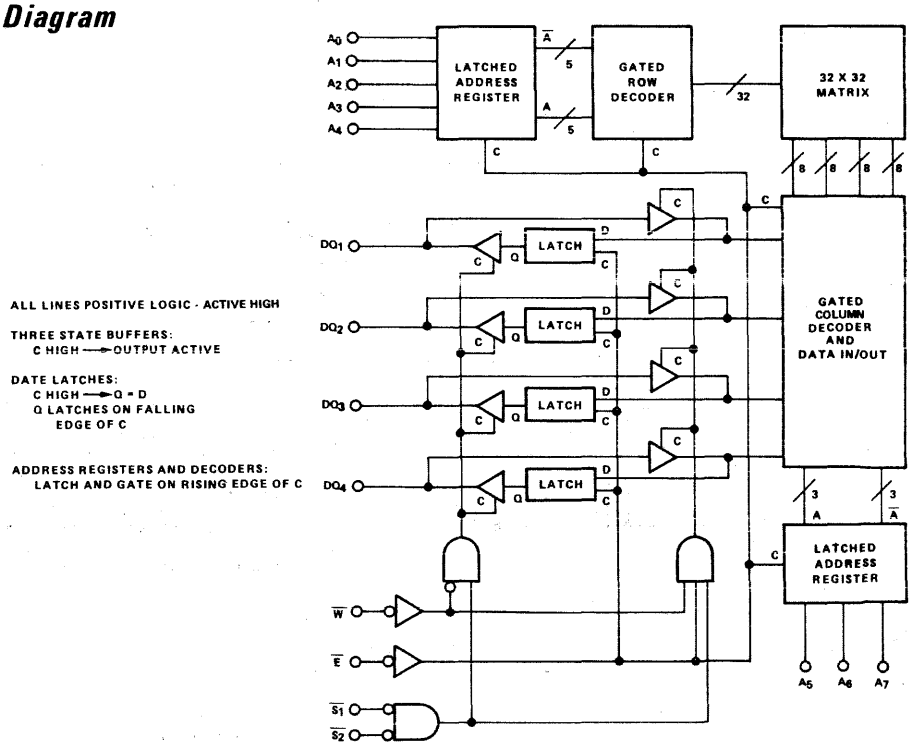


A – ADDRESS INPUT
E – CHIP ENABLE
S – CHIP SELECT
W – WRITE ENABLE
DQ – DATA IN/OUT

Logic Symbol



Functional Diagram



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HARRIS SEMICONDUCTOR PRODUCTS DIVISION

Product Brief

HM-6562

256 x 4 CMOS RAM

Features

- LOW POWER STANDBY . . . . . 55 μW MAX
- LOW POWER OPERATION. . . . . 22mW/MHz MAX
- FAST ACCESS TIME . . . . . 220nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE - 2TTL LOADS
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTER
- 16 PIN PACKAGE FOR HIGH DENSITY
- THREE-STATE OUTPUTS
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE

Description

The HM–6562 is a 256 by 4 static CMOS RAM fabricated using self aligned silicon gate technology. Synchronous circuit design techniques are employed to acheive high performance and low power operation.

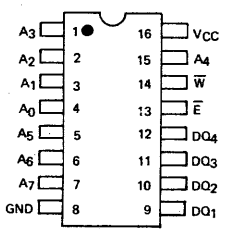
On chip latches are provided for address and data outputs allowing for efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

The HM–6562 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

The HM–6611, 256 x 4 CMOS PROM, is pin for pin replaceable with the HM–6562. This allows a single memory board design with any organization of RAM – ROM.

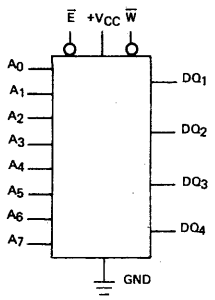
Pinout

TOP VIEW

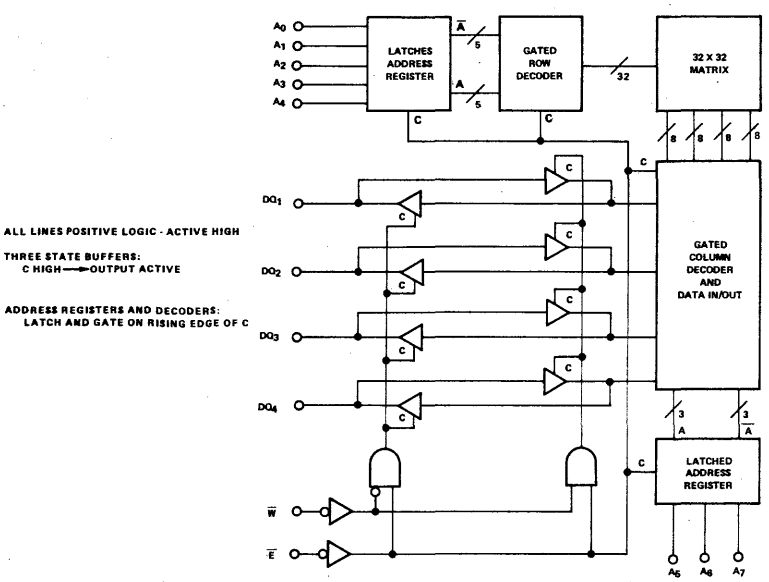


A – ADDRESS INPUT
$\overline{E}$ – CHIP ENABLE
$\overline{W}$ – WRITE ENABLE
DQ – DATA IN/OUT

Logic Symbol



Functional Diagram



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HM-6611

1024-BIT

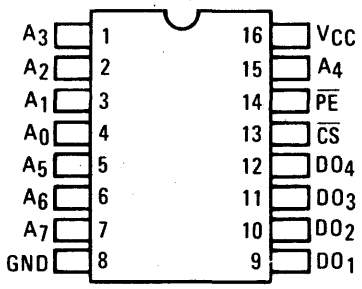
FIELD PROGRAMMABLE CMOS PROM

Features

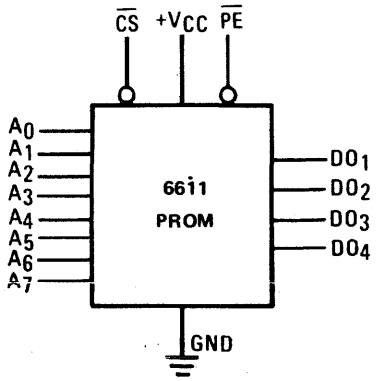
- FUSED LINK PROM
- FIELD-PROGRAMMABLE
- ORGANIZED 256 x 4
- LOW POWER STANDBY 0.1mW
- LOW POWER ENABLED 10mW
- CMOS RAM PINOUT EXCEPT FOR $\overline{PE}$
- TTL COMPATIBLE IN/OUT
- THREE STATE OUTPUTS
- FULLY STATIC OPERATION
- FAST ACCESS TIME . . . . . 450nsec MAX
- HIGH NOISE IMMUNITY
- HIGH RELIABILITY
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- DUAL-IN-LINE PACKAGE

Pinout

TOP VIEW - D.I.P.



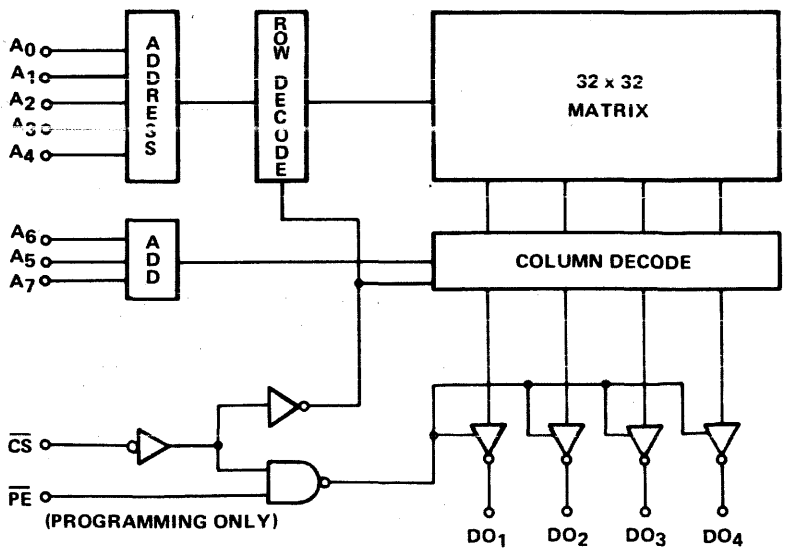
Logic Symbol



Description

The HM-6611 is part of a family of fusible link CMOS PROM's, featuring three-state outputs. This device is static, TTL compatible, and has a 100 μA max. standby current over temp. at a V_{CC} of 5 volts. 10V and full Mil. temp. devices are available. Chip Select ($\overline{CS}$) is used to place the device in the standby state and also forces the outputs into the high impedance state when it is high. Program Enable ($\overline{PE}$) is used only during programming, and must be connected to V_{CC} in the system. Pinout is similar to bipolar PROM's and 256 x 4 CMOS RAM's for flexibility in P.C. board layout and memory allocation by type.

Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.3V to +12.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial	-40°C to +85°C (-9)
Military	-55°C to +125°C (-2)

D.C. ELECTRICAL CHARACTERISTICS 5.

V_{CC} = 4.0V to 11.0V
T_A = -40°C to +85°C (-9), -55°C to +125°C (-2)

SYM	PARAMETER	MIN	TYP 1.	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
I_{IL}	Input Leakage, All Pins Except $\overline{PE}$ 2.	-1.0	0.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC}			V	I_{OUT} = 0
V_{OL}	Logical "0" Output Voltage			GND	V	I_{OUT} = 0
I_O	Output Leakage	-10.0	0.0	10.0	μA	$0V \leq V_O \leq V_{CC}$; $\overline{CS} = V_{CC}$
	Supply Current					
I_{CCS}	Standby		100	500	μA	$V_{IN} = V_{CC}$ or 0; $\overline{CS} = V_{CC}$
I_{CCE}	Enabled 3.		10	30	mA	$V_{IN} = V_{CC}$ or 0; $\overline{CS}$ = 0
C_{IN}	Input Capacitance 4. (Except $\overline{PE}$) 2.		5.0	8.0	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz; V_{CC} = 10V
C_O	Output Capacitance 4.		8.0	10.0	pF	V_{OUT} = 0V; T_A = 25°C; f = 1MHz; $\overline{CS} = V_{CC}$ = 10V

NOTES:
1. Typical parameters at 10V, 25°C, 50% programmed.
2. $\overline{PE}$ is used only during programming. Its characteristics are accounted for in the programming specifications.
3. I_{CC} enabled is proportional to the number of unblown fuses per word addressed. If all 4 fuses in the word are blown $I_{CC} \approx I_{CCS}$
4. Capacitance guaranteed and sampled, but not 100% tested.
5. The HM-6611A will also meet the HM-6611 specifications when operated at V_{CC} = 5.0V ±10%.

A.C. ELECTRICAL CHARACTERISTICS

C_L = 50pF, T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	V_{CC}
t_{AA}	Address Access time	350	ns	5
		275	ns	10
t_{EN}	Output Enable Time	75	ns	5
		50	ns	10
t_{DIS}	Output Disable Time	75	ns	5
		50	ns	10
t_{AC}	Access Time from $\overline{CS}$	400	ns	5
		325	ns	10

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.3V to +8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial	-40°C to +85°C (-9)
Military	-55°C to +125°C (-2)

D.C. ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%;
T_A = -40°C to 85°C (-9); -55°C to +125°C (-2)

SYM	PARAMETER	MIN	TYP [1]	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	V_{CC} -2.0			V	
V_{IL}	Logical "0" Input Voltage			0.8	V	
I_{IL}	Input Leakage, All Pins Except $\overline{PE}$ [2]	-1.0		1.0	µA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -1.0mA
V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 2mA
I_O	Output Leakage	-1.0	0.0	1.0	µA	$0V \leq V_O \leq V_{CC}$; $\overline{CS} = V_{CC}$
	Supply Current					
I_{CCS}	Standby		20	100	µA	$V_{IN} = V_{CC}$ or 0; $\overline{CS} = V_{CC}$
I_{CCE}	Enabled [3]		2	10	mA	$V_{IN} = V_{CC}$ or 0; $\overline{CS}$ = 0
C_{IN}	Input Capacitance [4] (Except $\overline{PE}$) [2]		5.0	8.0	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz; $V_{CC} = V_{CC}$ Max.
C_O	Output Capacitance [4]		8.0	10.0	pF	V_{OUT} = 0V; T_A = 25°C; f = 1MHz; $\overline{CS} = V_{CC} = V_{CC}$ Max.

NOTES:
1. Typical parameters at 5V, 25°C, 50% programmed.
2. $\overline{PE}$ is used only during programming. Its characteristics are accounted for in the programming specifications.
3. I_{CC} enabled is proportional to the number of unblown fuses per word addressed. If all 4 fuses in the word are blown $I_{CC} \approx I_{CCS}$.
4. Capacitance guaranteed and sampled, but not 100% tested.

A.C. ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%; C_L = 50pF; One TTL Load
T_A = -40°C to +85°C (-9), -55°C to +125°C (-2)

SYMBOL	PARAMETER	MAXIMUM	UNITS
t_{AA}	Address Access Time	450	ns
t_{EN}	Output Enable Time	150	ns
t_{DIS}	Output Disable Time	150	ns
t_{AC}	Access Time from $\overline{CS}$	500	ns

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.3V to +7.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	0°C to +75°C

D.C. ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±5%; T_A = 0°C to +75°C

SYM	PARAMETER	MIN	TYP 1.	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	V_{CC} -2.0			V	
V_{IL}	Logical "0" Input Voltage			0.65	V	
I_{IL}	Input Leakage, All Pins Except $\overline{PE}$ 2.	-10.0		10.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -1.0mA
V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 2mA
I_O	Output Leakage	-25.0		25.0	μA	$0V \leq V_O \leq V_{CC}$; $\overline{CS} = V_{CC}$
	Supply Current					
I_{CCS}	Standby		0.2	1.0	mA	$V_{IN} = V_{CC}$ or 0; $\overline{CS} = V_{CC}$
I_{CCE}	Enabled 3.		5	25	mA	$V_{IN} = V_{CC}$ or 0; $\overline{CS}$ = 0
C_{IN}	Input Capacitance 4. (Except $\overline{PE}$) 2.		5.0	8.0	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz; $V_{CC} = V_{CC}$ Max.
C_O	Output Capacitance 4.		8.0	10.0	pF	V_{OUT} = 0V; T_A = 25°C; f = 1MHz; $\overline{CS} = V_{CC} = V_{CC}$ Max.

NOTES:
1. Typical parameters at 5V, 25°C, 50% programmed.
2. $\overline{PE}$ is used only during programming. Its characteristics are accounted for in the programming specifications.
3. I_{CC} enabled is proportional to the number of unblown fuses per word addressed. If all 4 fuses in the word are blown $I_{CC} \approx I_{CCS}$.
4. Capacitance guaranteed and sampled, but not 100% tested.

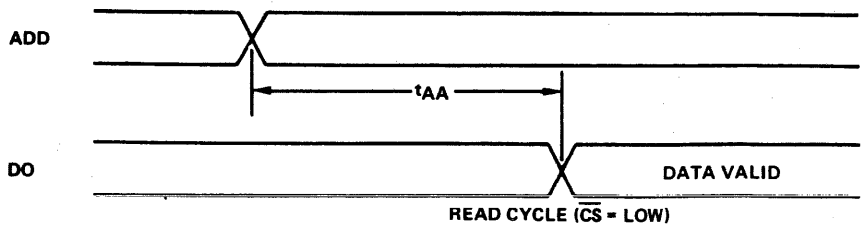
A.C. ELECTRICAL CHARACTERISTICS

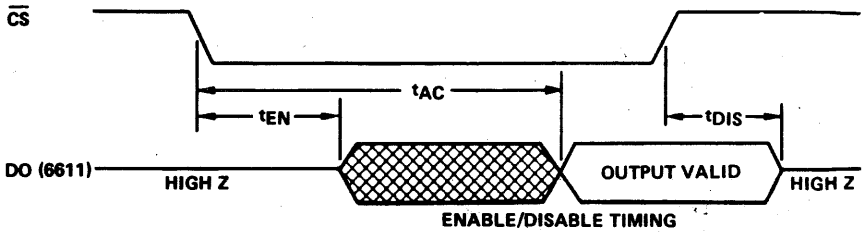
V_{CC} = 5.0V ±5%; C_L = 50pF, One TTL Load
T_A = 0°C to +75°C

SYMBOL	PARAMETER	MAXIMUM	UNITS
t_{AA}	Address Access Time	650	ns
t_{EN}	Output Enable Time	250	ns
t_{DIS}	Output Disable Time	250	ns
t_{AC}	Access Time from $\overline{CS}$	800	ns

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Test Characteristics





Programming

BACKGROUND INFORMATION

The HM-6611 is a 256 x 4 CMOS Programmable Read-Only Memory. It is programmed by the controlled application of programming pulses to selected memory cells. These pulses permanently alter the logic state of the memory cell. The memory array is manufactured with each cell set to the high or "1" logic state. The user may select any memory cell and permanently change its logic state to a "0" or low by programming.

Programming is accomplished by addressing the word to be programmed, applying the programming pulses, and verifying the data programmed. The verification is performed at high voltage (V_{CC}) during the programming sequence, and at low voltage after all programming is completed.

PROGRAMMING SYSTEM CHARACTERISTICS:

1. Power source for the device to be programmed (V_{CC}) variable from +3.0 to +11.0 volts, current capability of 500mA average and 1 amp dynamic currents.
2. Programming pulse is a negative 27.0 volt (±3.0V) pulse of 4 millisecond duration (±25%), rise and fall times of 4 to 400 microseconds, capable of 400mA average and 1 amp dynamic currents.
3. Data output load devices (switchable) capable of sinking 10mA from the output pin without rising more than 0.6 volts above ground. Open collector, open drain or discrete devices with resistive pull-ups of 4.7K to 47K is the recommended implementation.
4. Data output sensing devices capable of sensing valid logic levels ($V_{OH} \geq 70\%\ V_{CC}$, $V_{OL} \leq 20\%\ V_{CC}$).*
5. Address buffers able to maintain high state voltages of $\geq 70\%$ of V_{CC} at both high and low V_{CC},* and low state voltages $\leq 20\%$ V_{CC} at both high and low V_{CC}.
6. Timing and control logic suitable to sequence the required functions.

*Never allow any input to rise more than 0.3 volts above V_{CC}.

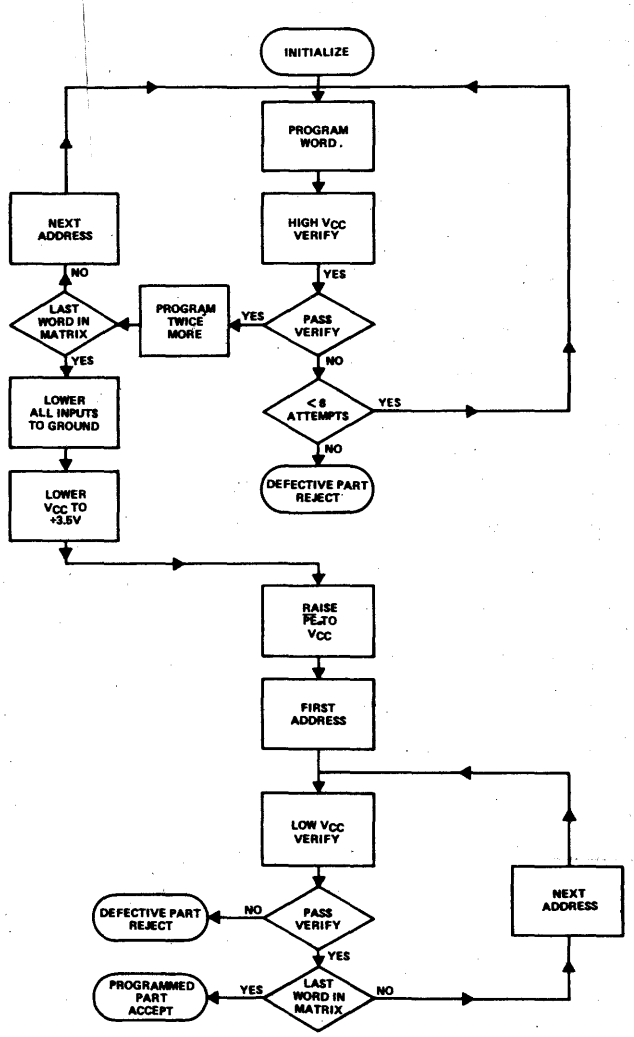
PROGRAMMING PROCEDURE:

OVERALL:

1. Address and program word.
2. Verify data output at high V_{CC} (10V ±10%)
   a. If device fails to verify repeat program – verify sequence (reject device as defective after 8 programming attempts at any one word).
   b. If device passes verify repeat programming sequence twice more then return to step 1 to program the next word.
   c. If device passes verify at the last location to be programmed continue to step 3.
3. Lower V_{CC} to 3.5V ±.5V and verify each location in the matrix.
   a. If any location fails to verify reject the device as defective.
   b. If all locations pass verify the part is properly programmed.

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PROGRAMMING SEQUENCE FLOW CHART



PROGRAMMING STEPS:

INITIALIZE:

V_{CC} = +10.0V ±10%
$\overline{PE}$ = V_{CC}
$\overline{CE}$ = GND (not used during programming)

1. Setup the address of the word to be programmed.
2. Wait 500 nanoseconds or more.
3. Initiate the negative $\overline{PE}$ pulse described in System Characteristics # 2.
4. After the $\overline{PE}$ pulse has crossed zero (ground) going negative enable the data output load devices of each output pin that is to be programmed (to become a low or "0" logic state).
5. Disable the data output loads 4 milliseconds (±25%) after it was enabled.
6. The negative $\overline{PE}$ pulse should rise back to V_{CC} no earlier than the data output loads are disabled.
7. Wait 500 nanoseconds or more.
8. Compare the output data with the desired data.
   a. If any one bit fails to verify, program again starting at step 3. After 8 programming attempts at any one location reject the device as defective. It is acceptable to repulse all desired bits if any one bit does not program.
   b. If all four bits verify apply two more programming pulses (steps 3 thru 7, twice). Then return to step 1 to address and program the next word.

After steps 1 thru 8 are completed for each word to be programmed:

9. Lower all inputs to ground.
10. Lower V_{CC} to +3.5 volts ±.5 volts.
11. Raise $\overline{PE}$ to V_{CC}.*
12. Setup the address of the word to be verified. (High or "1" or V_{IH} inputs must > 2.35 and < 3.8 volts).*
13. Wait 1 microsecond.
14. Compare the output data with the desired data.
    a. If any one bit fails to verify reject the device as defective.
    b. If all four bits verify return to step 12 to verify the next word.

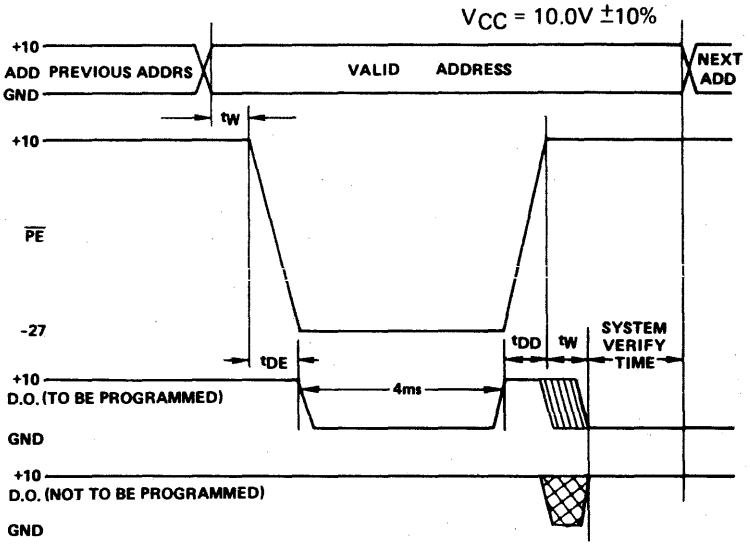
After steps 12 thru 14 are completed for each word in the matrix the device has been properly programmed.

*Never allow any input to rise more than 0.3 volts above V_{CC}.

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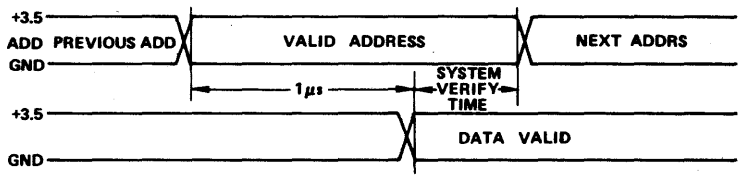
PROGRAMMING CYCLE

V_{CC} = 10.0V ±10%



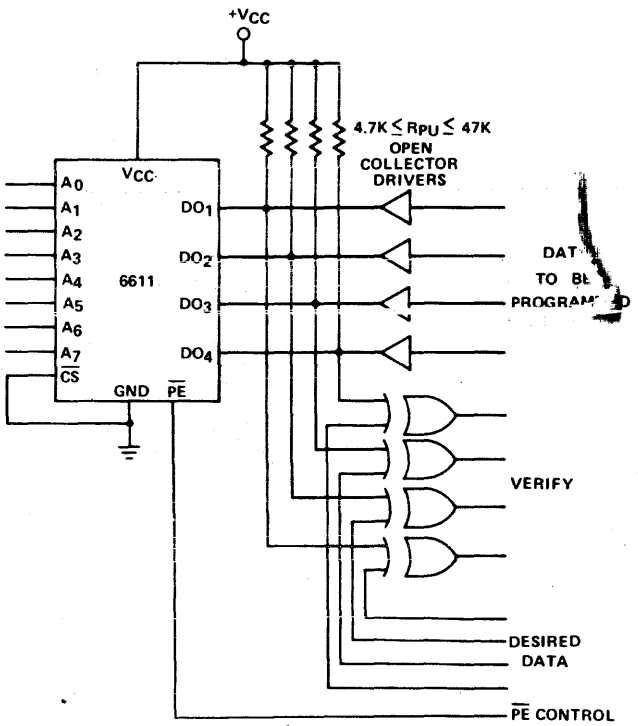
LOW VOLTAGE VERIFY CYCLE

V_{CC} = 3.5V ±0.5V



NOTES: $t_{DD} \leq 3/4\ t_{RISE}$ of $\overline{PE}$
$t_{DE} \geq 1/4\ t_{FALL}$ of $\overline{PE}$
t_W - 500 nanoseconds or More
Timing Events Specified At 90% and 10% Points.

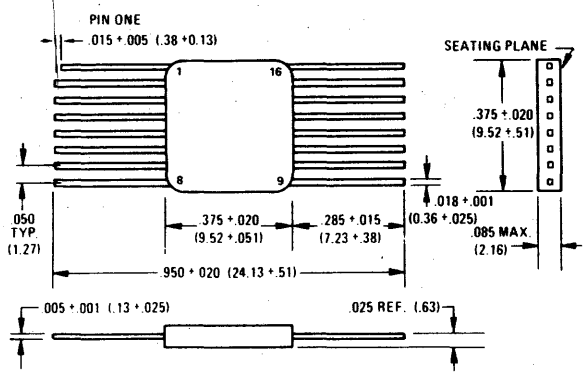
EXAMPLE PROGRAMMING CIRCUIT



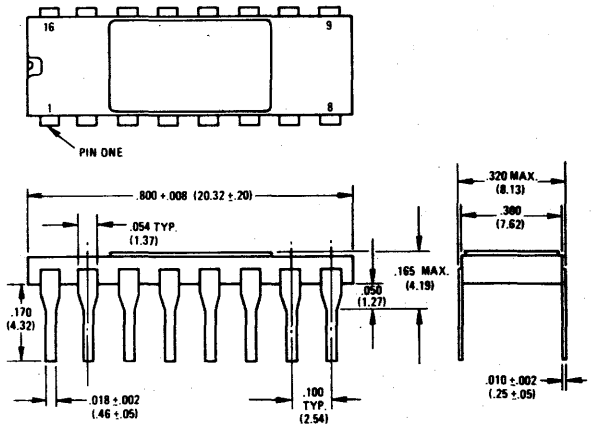
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Packaging

16 LEAD FLAT PACK



16 LEAD D.I.P.



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

Ordering Information

Example: HM 1 – 6611 A – 9

- HARRIS MEMORY
- PACKAGE
- DEVICE
- VERSION
- TEMPERATURE

TEMPERATURE RANGE

PACKAGES		MILITARY		INDUSTRIAL		COMMERCIAL
		A-2	-2	A-9	-9	D-5
FLAT PACKAGE	9-	YES	YES	NO	NO	NO
CERAMIC D.I.P.	1-	YES	YES	YES	YES	YES

NOTICE: Harris Semiconductor's products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders.

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PRODUCTS DIVISION

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HM-76XX

GENERIC PROM FAMILY

ORGANIZATIONS

PART NUMBER	*OUTPUT	TOTAL BITS	WORDS X BITS/WORD
HM-7602 HM-7603	OC TS	256	32 X 8
HM-7610 HM-7611	OC TS	1024	256 X 4
HM-7620 HM-7621	OC TS	2048	512 X 4
HM-7640 HM-7641	OC TS	4096	512 X 8
HM-7642 HM-7643 HM-7644	OC TS APU	4096	1024 X 4

*OC - Open-Collector
*TS - Three-State
*APU - Active Pull-Up

FEATURES

- Common D. C. Electrical Characteristics and Programming Procedure
- Simple, High Speed Programming Procedure (1 Second per 1024 Bits, Typical)
- Expandable - "Open-Collector" or "Three-State" Outputs and Chip Enable Inputs
- Inputs and Outputs TTL Compatible
  - ▶ Low Input Current - 400μA Logic "0", 40μA Logic "1"
  - ▶ Full Output Drive - 16mA Sink, 2mA Source
- Fast Access Time - Guaranteed for Worst Case N^2 Sequencing, Over Commercial and Military Temperature and Voltage Ranges
- Pin Compatible with Industry Standard PROM's and ROM's

DESCRIPTION

The HM-76XX Generic PROM's comprise a completely compatible family having common D.C. electrical characteristics and identical programming requirements. They are fully decoded, high speed, field programmable ROM's and are available in all commonly used organizations, with both open-collector and three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for a logical "0" (outputs low.)

The nichrome fuse technology is the same as is used in the JAN approved MIL 38510/201 PROM and in all other Harris PROM's.

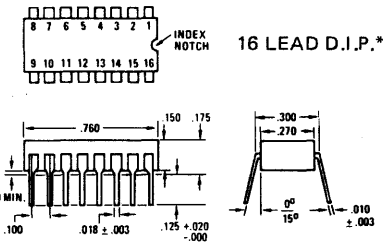
The field programmable PROM can be custom programmed to any pattern using a simple programming procedure. Schottky Bipolar circuitry provides fast access time, and features temperature and voltage compensation to minimize access time variations.

All pinouts are compatible to industry standard PROM's and ROM's.

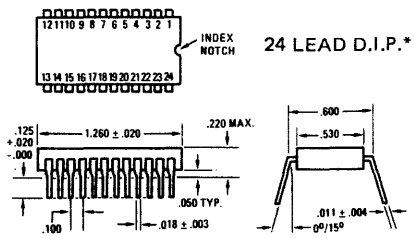
In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and A.C. performance. Fuses in these test rows and columns are blown prior to shipment.

PACKAGES

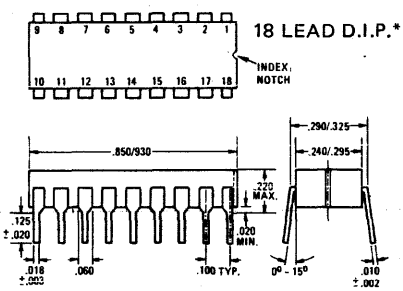
HM-7602/7603, HM-7610/7611
HM-7620/7621



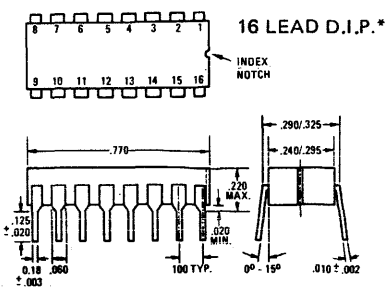
HM-7640/7641



HM-7642/7643



HM-7644



1. ALL DIMENSIONS IN INCHES.
2. ALL DIMENSIONS ±.010 UNLESS OTHERWISE SHOWN.

*Also Available in Flatpacks

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Harris Semiconductor

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	7.0V
Supply Current	650mA
Address/Enable Input Voltage	5.5V
Address/Enable Input Current	-20mA
Output Sink Current	100mA
Storage Temperature	+ 150°C
Operating Temperature (Ambient)	+ 125°C
Maximum Junction Temperature	+ 175°C

Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

ELECTRICAL CHARACTERSITICS (OPERATING)

HM-76XX-5 (V_{CC}= 5.0V ± 5%, T_A = 0°C to 70°C)

HM-76XX-2, HM-76XX-8 (V_{CC} = 5.0V ± 10%, T_A = -55°C to 125°C)

D. C.

PARAMETER		SYMBOL	OPEN-COLLECTOR OUTPUT MIN.	OPEN-COLLECTOR OUTPUT TYP.	OPEN-COLLECTOR OUTPUT MAX.	THREE-STATE OUTPUT MIN.	THREE-STATE OUTPUT TYP.	THREE-STATE OUTPUT MAX.	UNITS	TEST CONDITIONS
Address/Enable Input Current	"1"	I_{RA},I_{RE}			*40			*40	μA	V_{IH} = V_{CC} Max
	"0"	I_{FA},I_{FE}(1)		-0.1	*-0.4		-0.1	±0.4	mA	V_{IL} = 0.45V
Input Threshold Voltage	"1"	V_{IH}	2.0			2.0			V	V_{CC} = V_{CC} Min
	"0"	V_{IL}			0.8			0.8	V	V_{CC} = V_{CC} Max
Output Voltage	"1"	V_{OH}	N/A			*2.4	3.4		V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min
	"0"	V_{OL}		0.35	*0.45		0.35	*0.45	V	I_{OL} = + 16mA, V_{CC} = V_{CC} Min
Output Disabled Current (2)	"1"	I_{OHE}			*100			*100	μA	V_{OH}, V_{CC} = V_{CC} Max
	"0"	I_{OLE}			N/A			*-100	μA	V_{OL} = + 0.3V, V_{CC} = V_{CC} Max
Output Leakage (2)	"1"	I_{OH}			*100			N/A	μA	V_{OH}, V_{CC} = V_{CC} Max
Input Clamp Voltage		V_{CL}			*-1.5			*-1.5	V	I_{in} = - 10mA
Output Short Circuit Current		I_{OS}	N/A		N/A	15		70	mA	V_{CC} = V_{CC} Max, V_{OUT} = 0.0V One Output Only for a Max of 1 Second.
Power Supply Current HM-7602/7603 HM-7610/7611 HM-7620/7621		I_{CC}		90	*130		90	*130	mA	
HM-7640/7641		I_{CC}		125	*170		125	*170	mA	V_{CC} = V_{CC} Max All Inputs Grounded
HM-7642/7643 HM-7644		I_{CC}		100	*140		100	*140	mA	

NOTES: (1) I_{FE} Max = -1.6mA, CS_3 and CS_4 inputs, HM-7640/7641 only.
(2) N/A for HM-7644, active pull-up output.

Typical Measurements are at T_A = 25°C, V_{CC} = + 5V

*100% Tested for Dash 8

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ELECTRICAL CHARACTERSITICS (OPERATING)

A. C.

		HM-76XX-5		HM-76XX-2 HM-76XX-8		
	V_{CC}	5V ±5%		5V ±10%		
	T_A	0°C to 70°C		-55°C to 125°C		
	SYMBOL	TYP.	MAX.*	TYP.	MAX.*	UNITS
HM-7602/7603	T_{AA}	30	40	30	50	ns
	T_{EA}	20	30	20	40	ns
HM-7610/7611	T_{AA}	40	60	40	75	ns
	T_{EA}	15	25	15	30	ns
HM-7620/7621	T_{AA}	45	70	45	85	ns
	T_{EA}	15	25	15	30	ns
HM-7640/7641	T_{AA}	45	70	45	85	ns
	T_{EA}	30	40	30	50	ns
HM-7642/7643	T_{AA}	45	70	45	85	ns
HM-7644	T_{EA}	15	25	15	30	ns

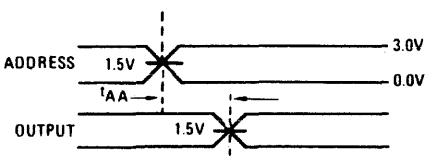
T_{AA} - Address to Output Access Time
T_{EA} - Chip Enable Access Time (N/A HM-7644)
*A. C. Maximum Limits Guarantee Worst Case N^2 Sequencing

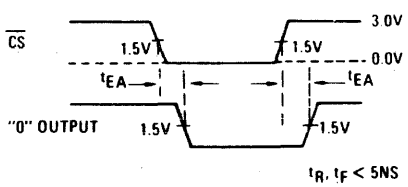
CAPACITANCE (1): T_A = 25°C

PARAMETER	SYMBOL	TYP.	UNITS	TEST CONDITIONS
Add. Input Cap.	C_{INA}, C_{INCS}	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
Output Cap.	C_{OUT}	8	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

NOTE: (1) These parameters are only periodically sampled and are not 100% tested.

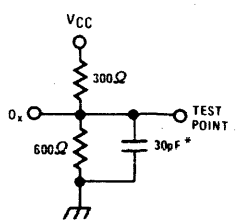
SWITCHING TIME DEFINITIONS





t_R, t_F < 5NS

A.C. TEST LOAD



*Includes jig & probe total capacitance

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PROGRAMMING

The Generic PROM's are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROM's can be programmed automatically or by the manual procedure shown below.

PROGRAMMING SPECIFICATIONS

TABLE 1

PARAMETER	SYMBOL	MIN.	RECOMMENDED OR TYP. VALUE	MAX.	UNITS
Address Input Voltage (1)	V_{IH} V_{IL}	2.4 0.0	5.0 0.4	5.0 0.8	V V
Programming/Verify Voltage to V_{CC} (2)	V_{PH} V_{PL}	11.75 4.5	12.0 4.5	12.25 5.5	V V
Programming Voltage Current Limit	I_{CCP}	600	600	650	mA
Programming (V_{CC}) Voltage Rise and Fall Time	t_r t_f	1 1	1 1	10 10	μs μs
Programming Delay	t_d	10	10	100	μs
Programming Pulse Width	t_p	100		1000	μs
Programming Duty Cycle	D. C.		50	90	%
Output Voltage Enable Disable (3)	V_{OPE} V_{OPD}	10.0 4.5	10.5 5.0	11.0 5.5	V V
Output Voltage Enable Current	I_{OPE}	2	4	10	mA
Case Temp.	T_C		25	75	°C

1. Address and chip select should not be left open for V_{IH}.
2. Verification at V_{CC} = 4.5 Volts, T_A = 25°C is recommended to guardband performance over full temperature and voltage range.
3. Disable condition will be met with output open circuit.

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PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input highs (V_{IH}) to the $\overline{CS}$ input(s). CS inputs (HM-7640/41 only) must remain at V_{IH} for program and verify. The chip select is TTL compatible. An open circuit should not be used to disable the chip. (This step N/A to HM-7644).
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ input(s).
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1mSec of programming time. Bits which do not program within 1mSec may be considered programming rejects. Multiple pulses of durations shorter than 1mSec may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address and desired and actual output data of a location in which a programming failure has occured.

TYPICAL PROGRAMMING CIRCUIT

The circuit and timing diagrams shown in Figures 1 and 2 will establish the proper programming conditions for the output enable pulses. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must be input protected to withstand inputs up to 12.5 Volts during programming.

FIGURE 1

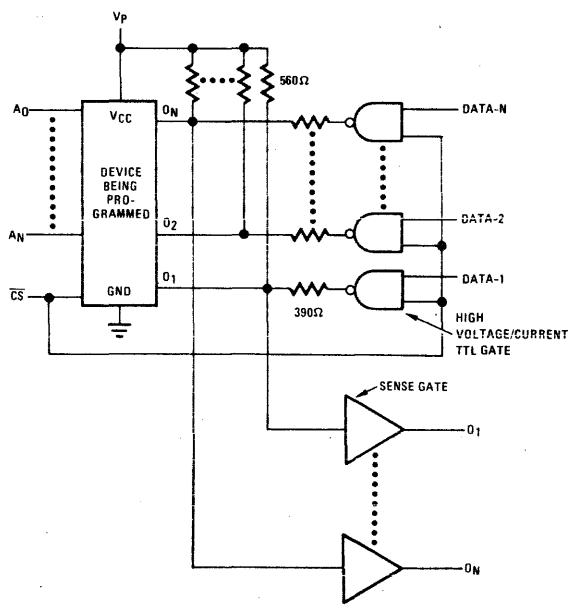
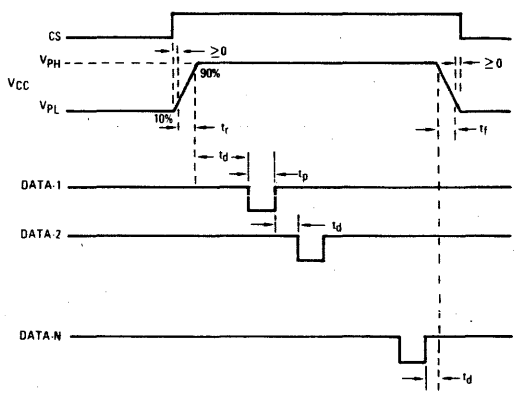
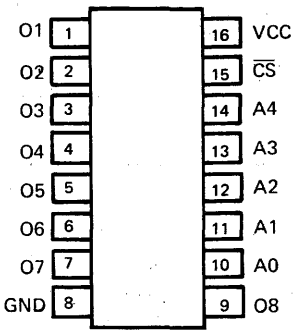


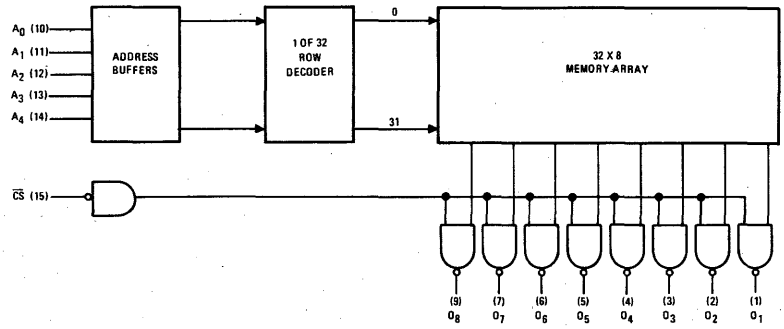
FIGURE 2



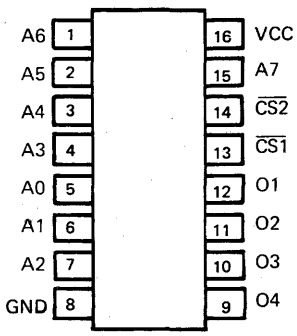
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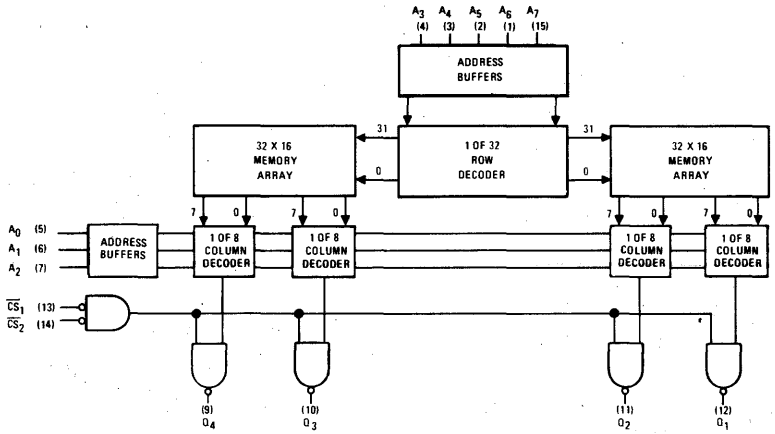
HM-7602/03
32 x 8



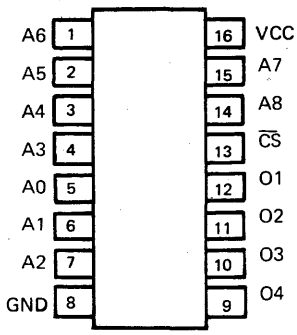


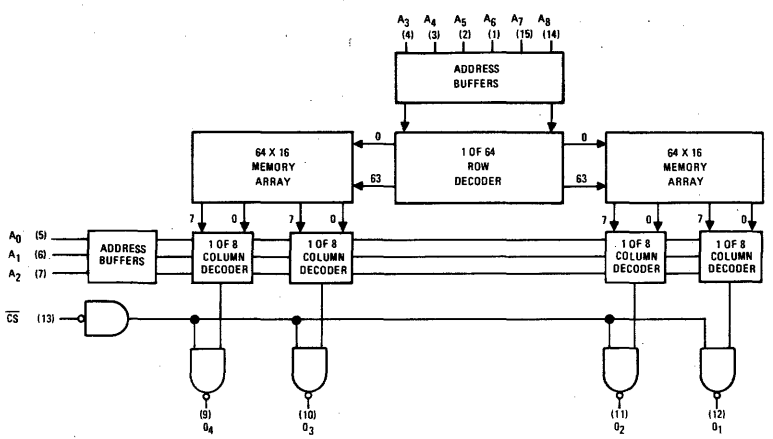
HM-7610/11
256 x 4





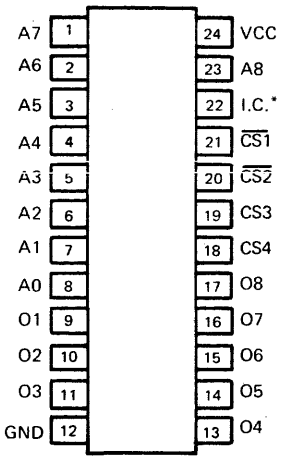
HM-7620/21
512 x 4

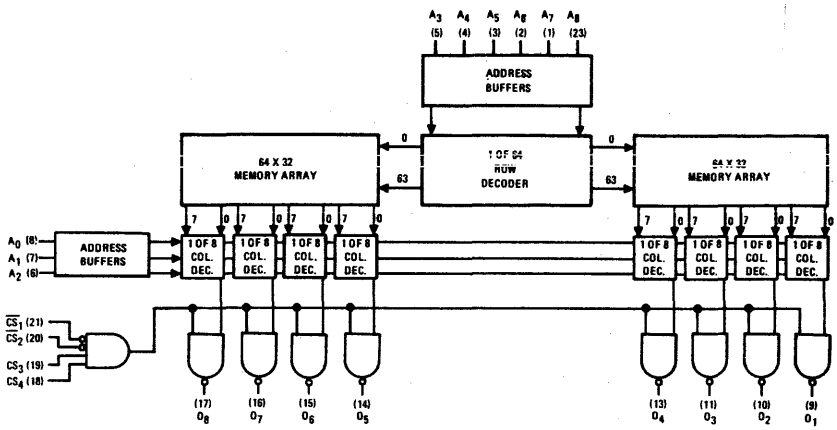




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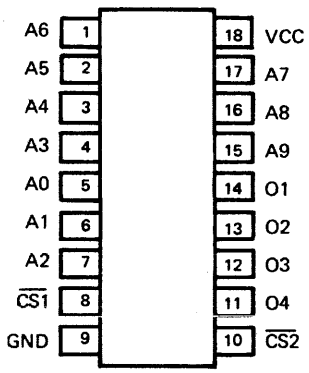
HM-7640/41
512 x 8

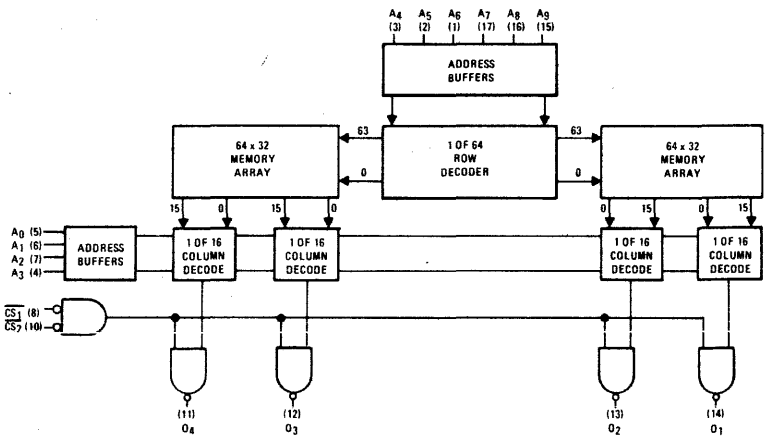




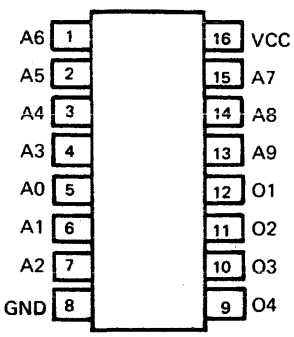
*Internal Connection, recommended to be left open circuit.

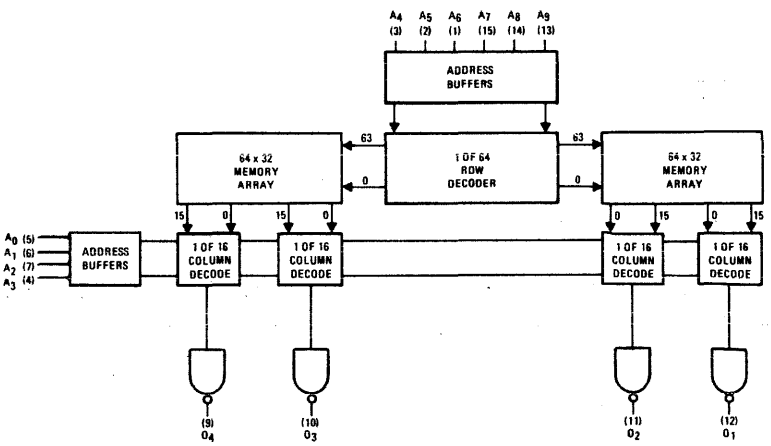
HM-7642/43
1024 x 4





HM-7644
1024 x 4

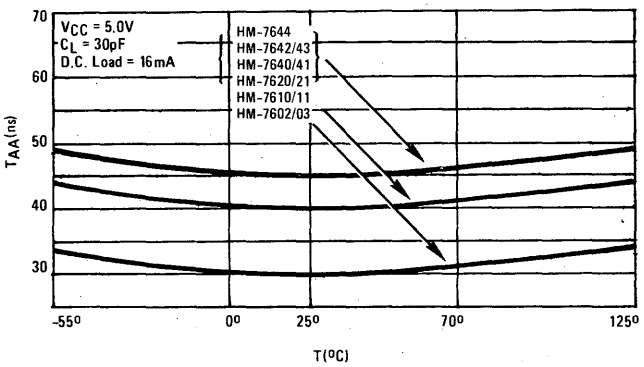




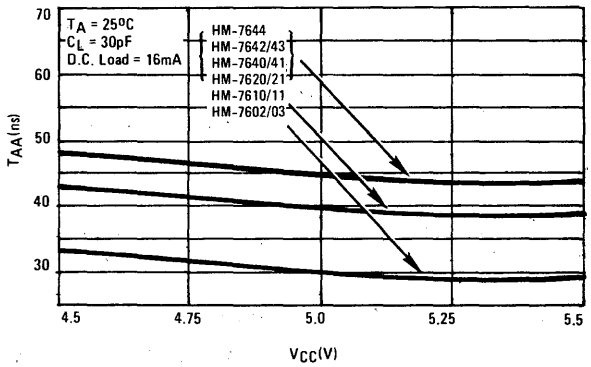
©IC MASTER 1978

TYPICAL A.C. CHACTERISTICS

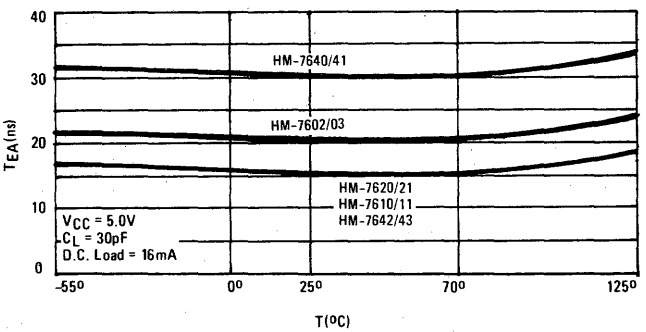
ADDRESS TO OUTPUT DELAY
VS. TEMPERATURE



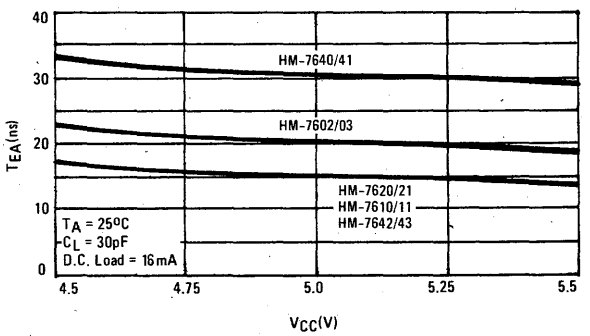
ADDRESS TO OUTPUT DELAY
VS. SUPPLY VOLTAGE



CHIP SELECT TO OUTPUT DELAY
VS. TEMPERATURE



CHIP SELECT TO OUTPUT DELAY
VS. SUPPLY VOLTAGE



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SEMICONDUCTOR
PRODUCTS DIVISION

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Preliminary

HM-7610A/11A

256 x 4 PROM

HM-7610A - Open Collector Outputs
HM-7611A - "Three State" Outputs

Features

- 40ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS
- SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE USING SINGLE PULSES, ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- INPUTS AND OUTPUTS TTL COMPATIBLE
- FAST ACCESS TIME – GUARANTEED FOR WORST CAST N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRYS HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH INDUSTRY STANDARD PROM's AND ROM's

Description

The HM-7610A/11A are fully decoded high speed Schottky TTL 1024-Bit Field Programmable ROMs in a 256 word by 4 bit/word format with open collector (HM-7610A) or "three state" (HM-7611A) outputs. These PROMs are available in 16 pin D.I.P. (ceramic or epoxy) and a 16 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

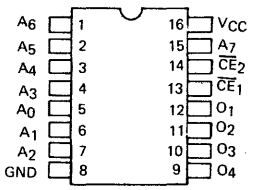
The HM-7610A/11A contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

This PROM is intended for use in state of the art ultra high speed logic systems.

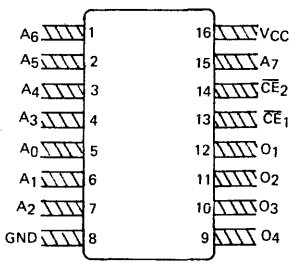
Nichrome fuse technology is used on these and all other Harris Bipolar PROM's.

Pinouts

TOP VIEW – D.I.P.



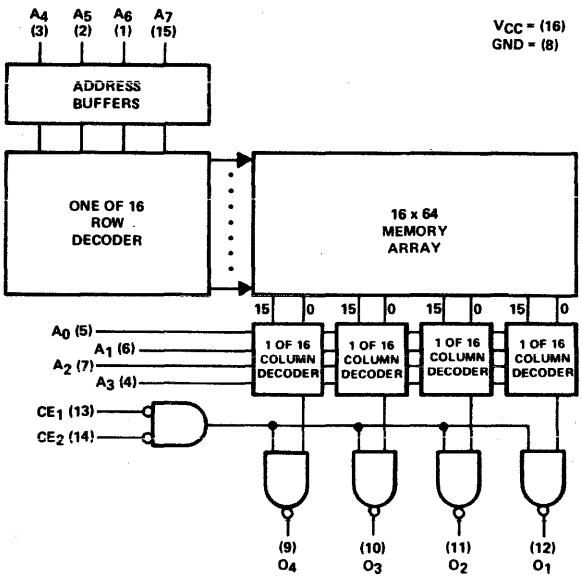
TOP VIEW – FLATPACK



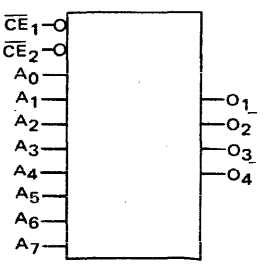
PIN NAMES

$A_0 - A_7$	ADDRESS INPUTS
$\overline{CE}_1 - \overline{CE}_2$	CHIP ENABLE INPUTS
$O_1 - O_4$	DATA OUTPUTS

Functional Diagram



Logic Symbol



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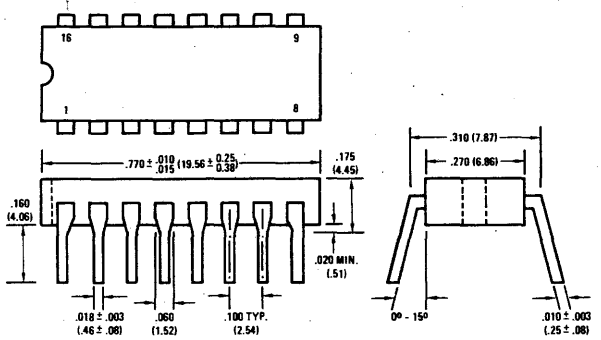
Refer to Harris Sales Offices for additional specifications.

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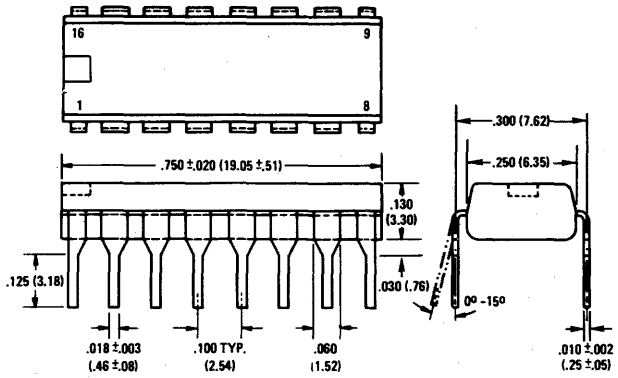
Packaging

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

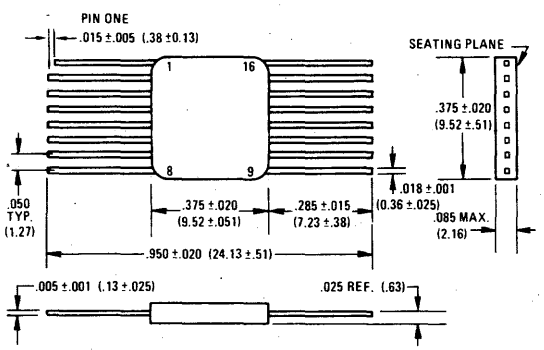
16 LEAD CERDIP
HM1 - 7610A/11A



16 LEAD EPOXY D.I.P.
HM3 - 7610A/11A



16 LEAD FLATPACK
HM9 - 7610A/11A



Ordering Information

HM 1 - 76XX - 5

- HARRIS MEMORY
- DEVICE NUMBER
- PACKAGE
  - 1 — Cerdip
  - 3 — Epoxy
  - 9 — Flat Pack
- TEMPERATURE
  - 2 -55°C to 125°C
  - 5 0°C to 75°C
  - 8 Dash 8 Program MIL-STD-883 Class B

PACKAGE AVAILABILITY

TEMPERATURE	CERDIP	EPOXY	FLAT PACK
-2	YES	NO	YES
-5	YES	YES	NO
-8	YES	NO	YES

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HM-7620A/21A

Preliminary

512 x 4 PROM

HM-7620A - Open Collector Outputs
HM-7621A - "Three State" Outputs

Features

- 45ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS
- SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE USING SINGLE PULSES, ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- INPUTS AND OUTPUTS TTL COMPATIBLE
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH INDUSTRY STANDARD PROM's AND ROM's.

Description

The HM-7620A/21A are fully decoded high speed Schottky TTL 2048-Bit Field Programmable ROM's in a 512 word by 4 bit/word format with open collector (HM-7620A) or "three state" (HM-7621A) outputs. These PROMs are available in 16 pin D.I.P. (ceramic or epoxy) and a 16 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

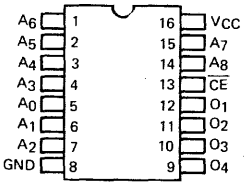
The HM-7620A/21A contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

This PROM is intended for use in state of the art ultra high speed logic systems.

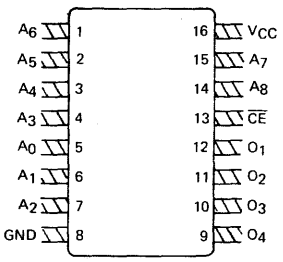
Nichrome fuse technology is used on these and all other Harris Bipolar PROM's.

Pinouts

TOP VIEW – D.I.P.



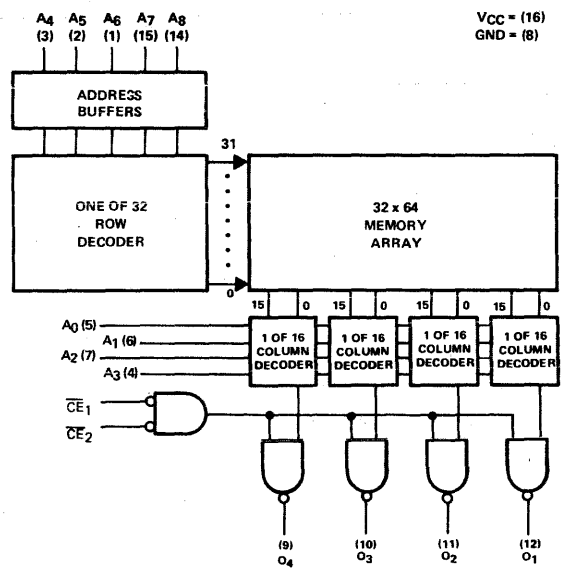
TOP VIEW – FLATPACK



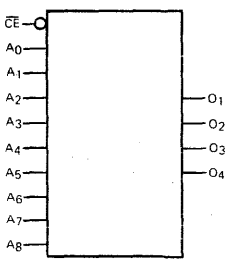
PIN NAMES

$A_0 - A_8$	ADDRESS INPUTS
$\overline{CE}$	CHIP ENABLE INPUT
$O_1 - O_4$	DATA OUTPUTS

Functional Diagram



Logic Symbol



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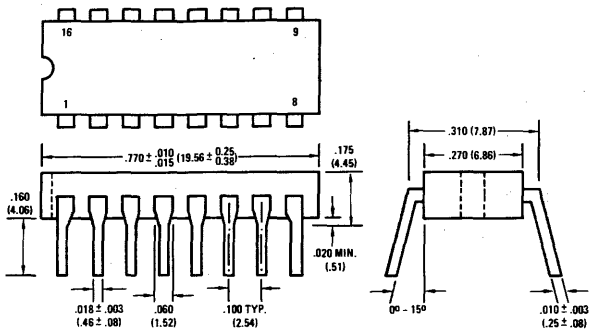
Refer to Harris Sales Offices for additional specifications.

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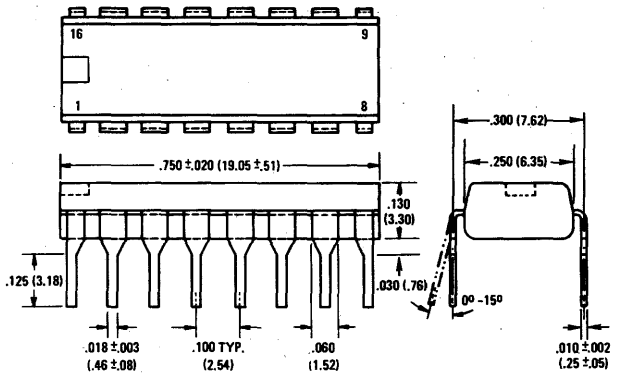
Packaging

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

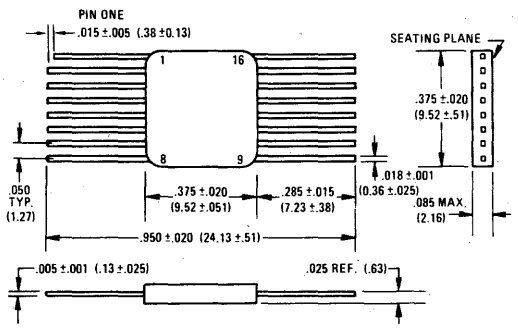
16 LEAD CERDIP
HM1-7620A/21A



16 LEAD EPOXY D.I.P.
HM3-7620A/21A



16 LEAD FLATPACK
HM9-7620A/21A



Ordering Information

HM 1 - 76XX - 5

- HARRIS MEMORY
- PACKAGE: 1 – Cerdip; 3 – Epoxy; 9 – Flat Pack
- DEVICE NUMBER
- TEMPERATURE: 2 -55°C to 125°C; 5 0°C to 75°C; 8 Dash 8 Program MIL-STD-883 Class B

PACKAGE AVAILABILITY

TEMPERATURE	CERDIP	EPOXY	FLAT PACK
-2	YES	NO	YES
-5	YES	YES	NO
-8	YES	NO	YES

NOTICE: Harris Semiconductor's products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders.

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HM-7640A/41A

Preliminary

512 x 8 PROM

HM-7640A - Open Collector Outputs
HM-7641A - "Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS AND FOUR CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LOW INPUT LOADING

Description

The HM-7640A/41A are fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROMs in a 512 word by 8 bit/word format and is available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flatpack.

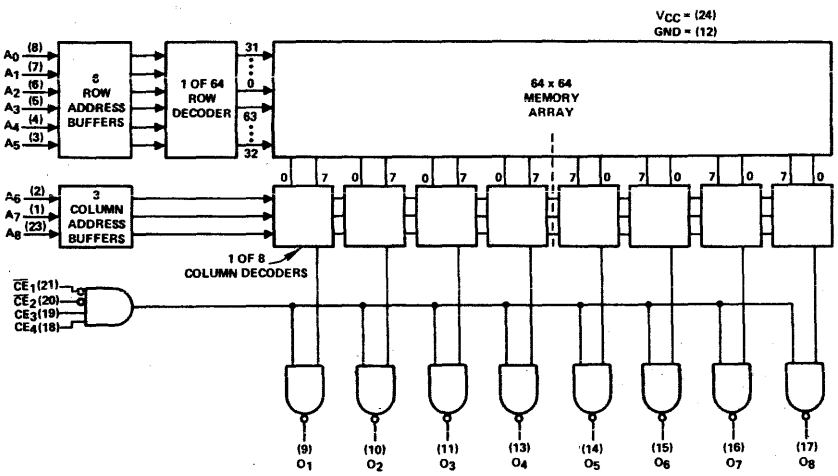
All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROM's.

The HM-7640A/41A contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

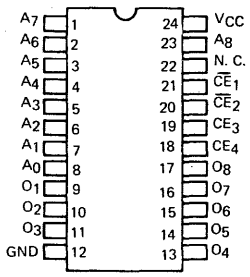
There are four chip enable inputs on the HM-7640A/41A where $\overline{CE}_1$, and $\overline{CE}_2$ low and CE_3 and CE_4 high enables the chip.

Functional Diagram

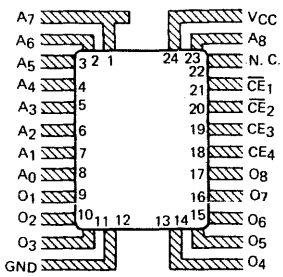


Pinout

TOP VIEW – D.I.P.



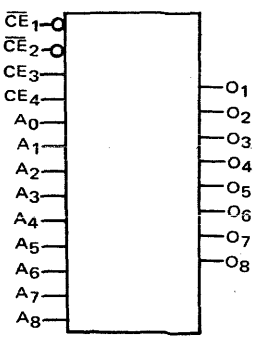
TOP VIEW – FLATPACK



PIN NAMES

$A_0 - A_8$	ADDRESS INPUTS
$O_1 - O_8$	DATA OUTPUTS
$\overline{CE}_1$, $\overline{CE}_2$, CE_3, CE_4,	CHIP ENABLE INPUTS

Logic Symbol



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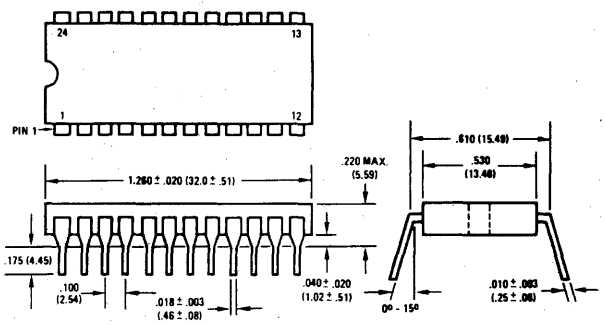
Refer to Harris Sales Offices for additional specifications.

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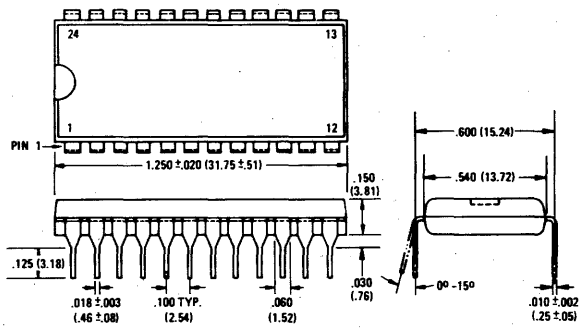
Packaging

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

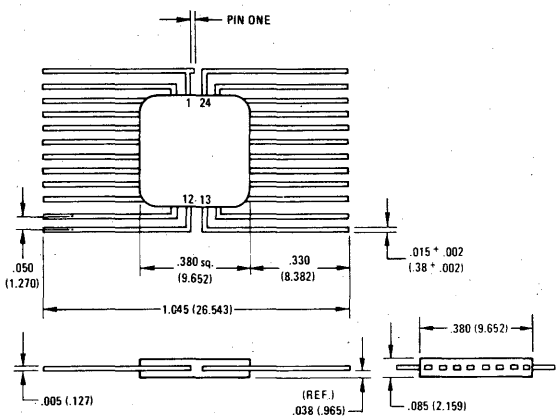
24 LEAD CERDIP
HM1-7640A/41A



24 LEAD EPOXY D.I.P.
HM3-7640A/41A



24 LEAD FLATPACK
HM9-7640A/41A



Ordering Information

HM 1 - 76XX - 5

- HARRIS MEMORY
- PACKAGE
  - 1 – Cerdip
  - 3 – Epoxy
  - 9 – Flat Pack
- DEVICE NUMBER
- TEMPERATURE
  - 2 -55°C to 125°C
  - 5 0°C to 75°C
  - 8 Dash 8 Program MIL-STD-883 Class B

PACKAGE AVAILABILITY

TEMPERATURE	CERDIP	EPOXY	FLAT PACK
-2	YES	NO	YES
-5	YES	YES	NO
-8	YES	NO	YES

NOTICE: Harris Semiconductor's products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders.

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HM-7640AR/41AR

Preliminary

512 x 8 PROM

HM-7640AR - Open Collector Outputs
HM-7641AR - "Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS WITH THREE CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LATCHED OUTPUTS
- INPUT LOADING IS – 100μA, MAXIMUM

Description

The HM-7640AR/41AR are fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROMs in a 512 word by 8 bit/word format and is available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROM's.

The HM-7640AR/41AR contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

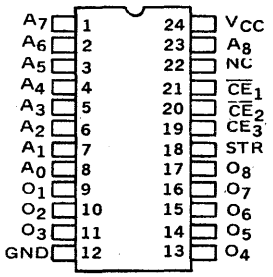
There are three chip enable inputs on the HM-7640AR/41AR; $\overline{CE}_1$, $\overline{CE}_2$ low and CE_3 high enables the chip.

HM-7640AR/41AR are operated in the Transparent Read mode by holding the strobe input high throughout the read operation. This is the normal read mode where the three chip enable inputs will control the outputs.

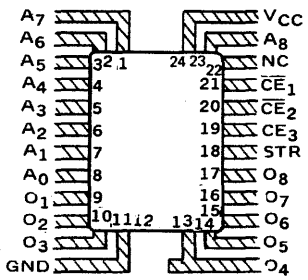
In Latched Read mode, bringing the strobe input low will latch the outputs and chip enable inputs. If the device is disabled, when the strobe input goes low the outputs will be latched in the high impedance state. If the device is in the latched mode the strobe input must be brought high to allow the outputs to respond to new address or chip enable conditions.

Pinouts

TOP VIEW – D.I.P.



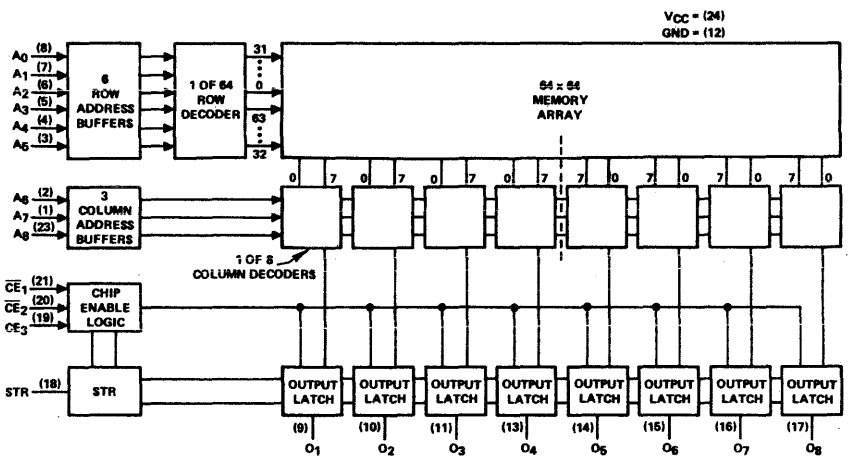
TOP VIEW – FLATPACK



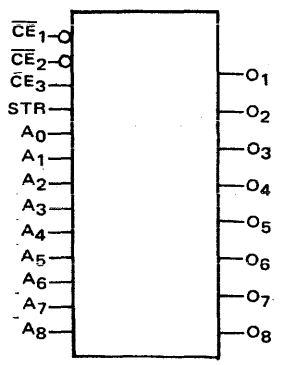
PIN NAMES

$A_0 - A_8$	ADDRESS INPUTS
$O_1 - O_8$	DATA OUTPUTS
$\overline{CE}_1$, $\overline{CE}_2$, CE_3	CHIP ENABLE INPUTS
STR	LATCH INPUT

Functional Diagram



Logic Symbol



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Refer to Harris Sales Offices for additional specifications.

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Specifications

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM - 7640AR/41AR - 5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM - 7640AR/41AR - 21 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/enable "1" Input Current "0"	– –	0.0 -50	+25 -100	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	0.0 0.0	+40 -40	µA µA	V_{OH}, V_{CC} = V_{CC} max V_{OL} = +0.3V, V_{CC} = V_{CC} Max
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current	-20	–	- 70	mA	V_{CC} = V_{CC} Max., V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7640AR/41AR-5 5V ±5% 0°C – +75°C			HM-7640AR/41AR-5 5V ±10% -55°C – +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX*	MIN	TYP	MAX*	UNITS	TEST CONDIT.
T_{AA} T_{EA}	Address Access Time Chip Enable Access Time	– –	45 20	60 40	– –	50 30	80 50	ns ns	Latched or Transparent
T_{ADH} T_{CDH} T_{SW} T_{SL} T_{DL} T_{CDS}	Address Hold Time Chip Enable Hold Time Strobe Pulse Width Strobe Latch Time Strobe Delatch Time Chip Enable Set-Up Time	0 10 30 60 – 40	-10 0 15 35 – –	– – – – 40 –	0 10 30 80 – 40	-10 0 15 45 – –	– – – – 50 –	ns ns ns ns ns ns	Latched Only

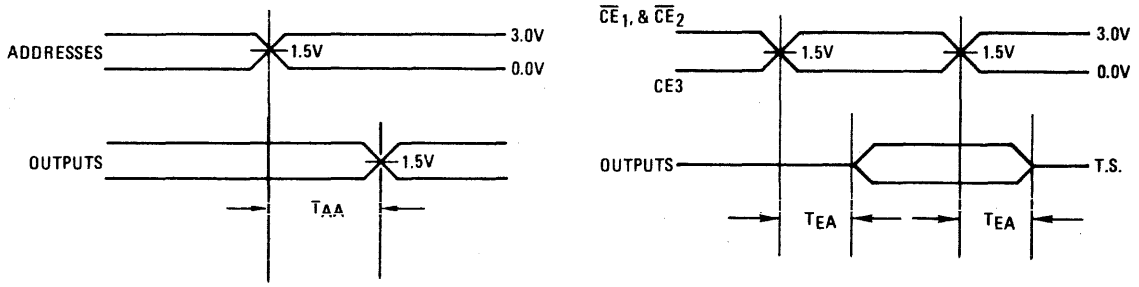
*A.C. Max. limits guarantee worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	12	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	12	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

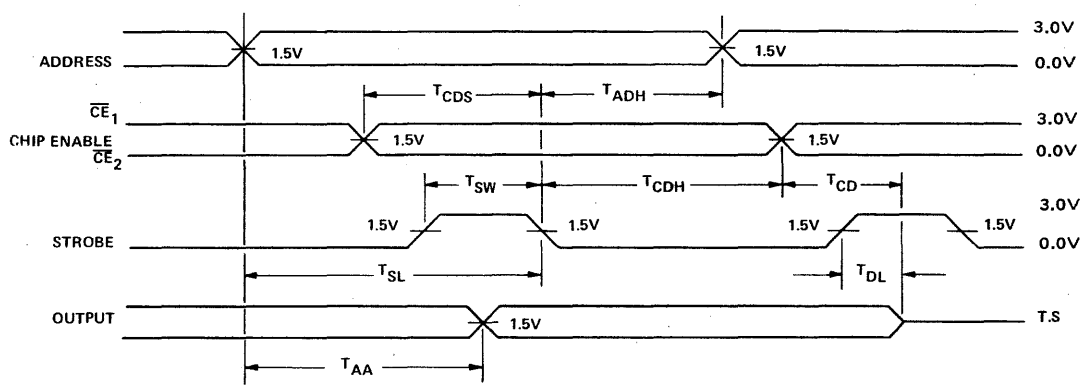
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SWITCHING TIME DEFINITIONS (TRANSPARENT MODE)

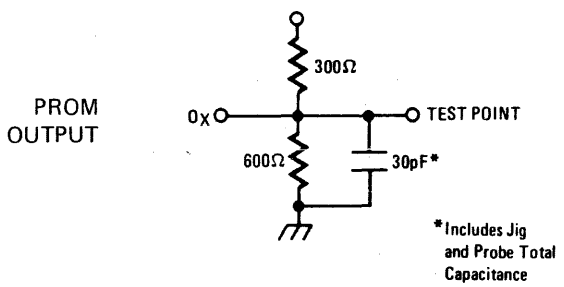


NOTE: Strobe input must remain high throughout read cycle while in transparent mode.

SWITCHING TIME DEFINITIONS (LATCHED MODE)



A.C. TEST LOAD



Programming

The HM-7640AR/41AR PROMs are manufactured with all bits/outputs logical "1" (output high). Any desired bit/output can be programmed to a logical "0" (output low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which can meet these specifications. This PROM can be programmed automatically or by the manual procedure shown below.

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PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS
V_{IH} V_{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V V
V_{PH} (2) V_{PL} (3)	Programming/Verify Voltage to V_{CC}	12.0 4.5	12.0 4.5	12.5 5.5	V V
I_{ILP}	Programming Input Low at V_{PH}	–	.250	.500	mA
t_r t_f	Programming (V_{CC}) Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10.0 10.0	μs μs
t_d	Programming Delay	10	10	100	μs
t_p	Programming Pulse Width (4)	90	100	110	μs
D.C.	Programming Duty Cycle	–	50	90	%
V_{OPE} V_{OPD}	Output Voltage Enable (5) Disable	10.5 4.5	10.5 5.0	11.0 5.5	V V
I_{OPE}	Output Voltage Enable Current	–	–	10.0	mA
TC	Case Temperature	–	25	75	°C

During programming the chip must be disabled for proper operation.

NOTES:
1. No inputs should be left open for V_{IH}.
2. V_{PH} source must be capable of supplying one ampere.
3. It is recommended that dual verification be made at V_{PL} min. and V_{PL} max.
4. Note step 10 in programming procedure.
5. Disable condition will be met with output open circuited.

PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the word to be programmed. Address inputs are TTL compatible. An open circuit should not be used to address the PROM.

2. Bring the $\overline{CE}_1$ and $\overline{CE}_2$ inputs high and the CE_3 input low to disable the device. The deselecting of the device during programming is an essential step in correctly programming this and all other Harris PROM's. The chip enables are TTL compatible. An open circuit should not be used to disable the chip.

3. Apply a logical "1" to the strobe input to place the chip in transparent read mode which is essential during programming. The strobe must remain high throughout the entire programming procedure.

4. Disable the programming circuitry by applying a voltage disable of V_{OPD} to the outputs of the PROM. The output may be left open to achieve the disable.

5. Raise V_{CC} to V_{PH} with rise time equal to t_r.

6. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.

7. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.

8. Lower V_{CC} to 4.5 volts following a delay of t_d from the last programming enable pulse applied to an output.

9. Enable the PROM for verification by applying a logic "0" to $\overline{CE}_1$ and $\overline{CE}_2$ and a logic "1" to CE_3. Repeat verification at V_{CC} = 5.5 volts.

10. If any bit does not verify as programmed, repeat steps 2 through 9 until the bit has received a total of 1mSec. of programming time. Bits which do not program within 1mSec. are programming rejects. No further attempt to program these parts should be made.

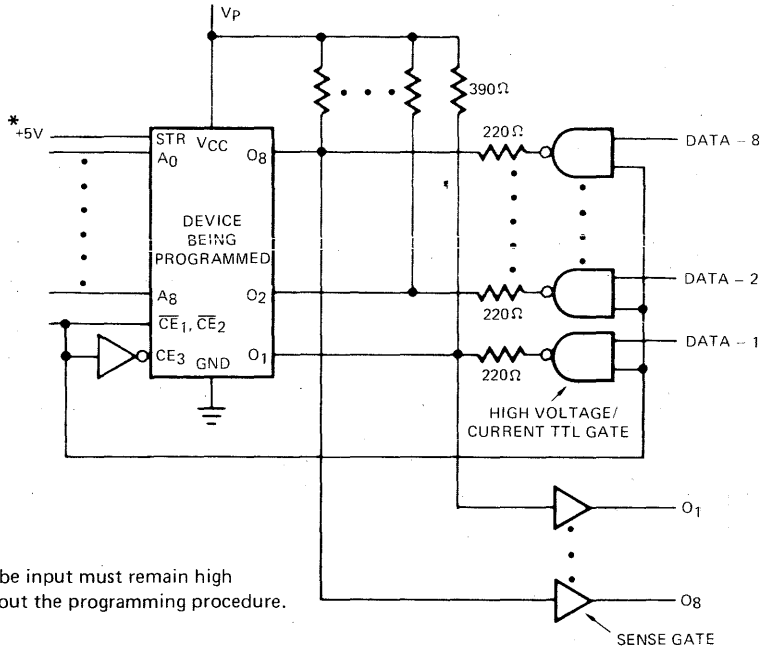
11. Repeat steps 1 through 10 for all other bits to be programmed in the PROM.

12. Programming rejects returned to the factory must be accompanied by data giving address, desired, and actual output data of a location in which a programming failure has occurred.

TYPICAL PROGRAMMING CIRCUIT

The circuit and timing diagrams shown in Figures 1 and 2 will establish the proper programming conditions for the output enable pulses. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must withstand inputs up to 12.5 volts during programming.

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*NOTE: The strobe input must remain high throughout the programming procedure.

FIGURE 1

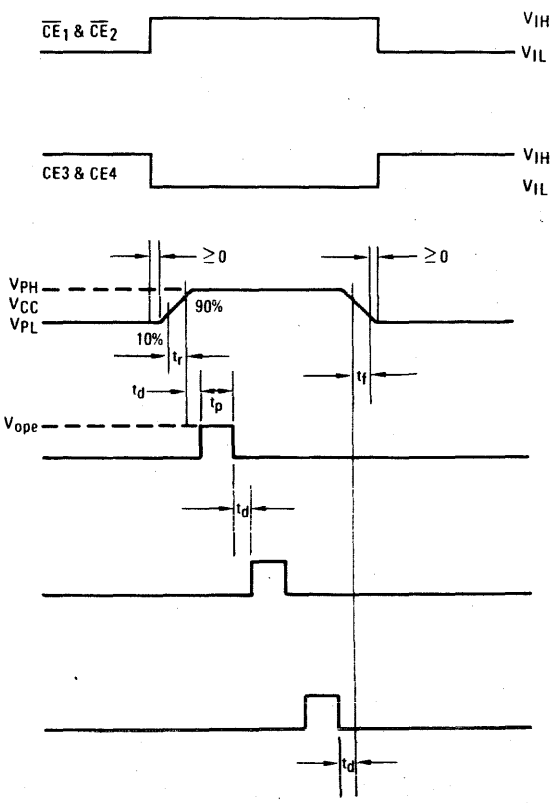


FIGURE 2

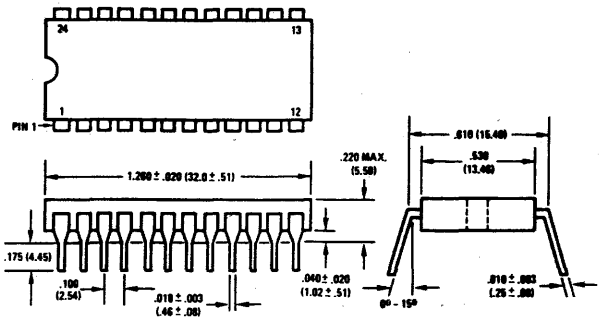
NOTE: The strobe input must remain high throughout the programming procedure. This timing diagram shows device terminal conditions. Each positive going data pulse at the terminal blows the corresponding bit resulting in a low output in that bit, therefore a low input at the DATA-X points of the Figure 1 circuit results in a permanent low output of a bit.

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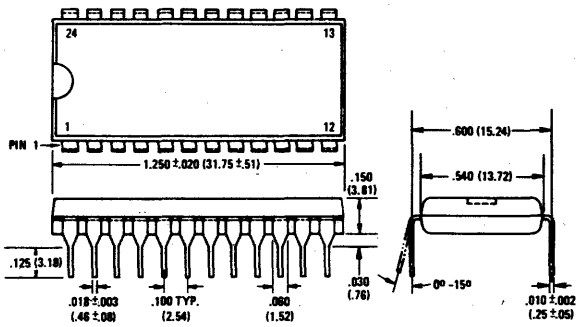
Packaging

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

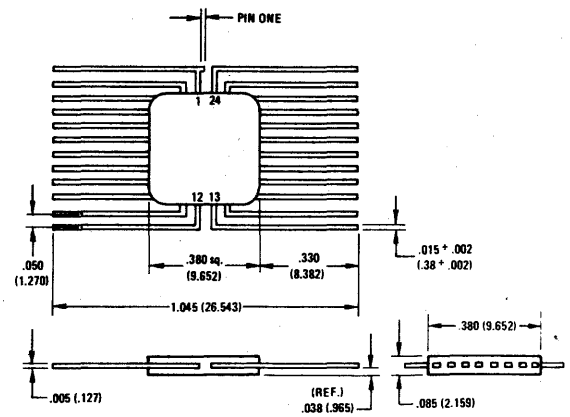
24 LEAD CERDIP
HM1 - 7640AR/41AR



24 LEAD EPOXY D.I.P.
HM3 - 7640AR/41AR



24 LEAD FLATPACK
HM9 - 7640AR/41AR



Ordering Information

HM 1 - 76XX - 5

- HARRIS MEMORY
- DEVICE NUMBER
- PACKAGE
  - 1 – Cerdip
  - 3 – Epoxy
  - 9 – Flat Pack
- TEMPERATURE
  - 2 -55°C to 125°C
  - 5 0°C to 75°C
  - 8 Dash 8 Program MIL-STD-883 Class B

PACKAGE AVAILABILITY

TEMPERATURE	CERDIP	EPOXY	FLAT PACK
-2	YES	NO	YES
-5	YES	YES	NO
-8	YES	NO	YES

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Preliminary

HM-7647R

512 x 8 PROM

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS WITH TWO CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH THE 82S115
- LATCHED OUTPUTS
- INPUT LOADING IS – 100 μA MAXIMUM

Description

The HM-7647R is a fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROM in a 512 word by 8 bit/word format and is available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position. The HM-7647R has three state outputs.

Nichrome fuse technology is used on this and all other Harris Bipolar PROM's.

The pinout is identical to the 82S115 PROM.

The HM-7647R contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A. C. performance. The fuses in these test rows and columns are blown prior to shipment.

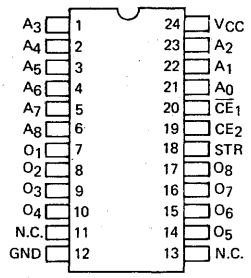
There are two chip enable inputs on the HM-7647R. $\overline{CE}_1$ low and CE_2 high enables the chip.

HM-7647R is operated in the Transparent Read mode by holding the strobe input high throughout the read operation. This is the normal read mode where the two chip enable inputs will control the outputs.

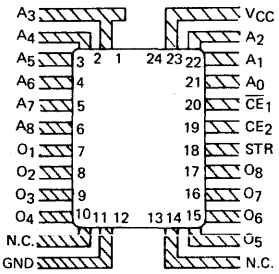
In Latched Read mode, bringing the strobe input low will latch the outputs and chip enable inputs. If the device is disabled, when the strobe input goes low the outputs will be latched in the high impedance state. If the device is in the latched mode the strobe input must be brought high to allow the outputs to respond to new address or chip enable conditions.

Pinout

TOP VIEW – D.I.P.



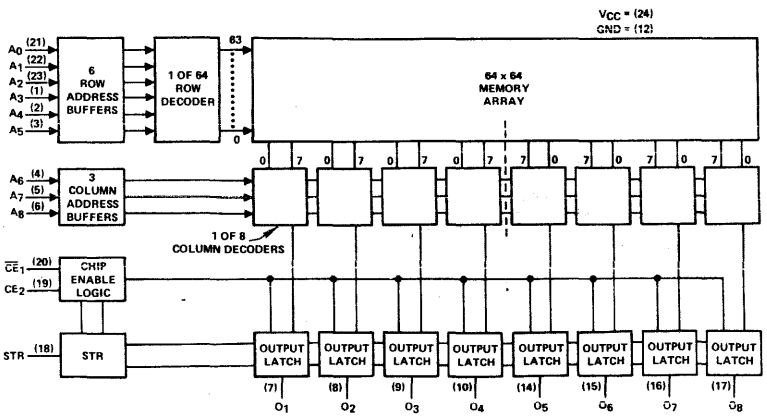
TOP VIEW – FLATPACK



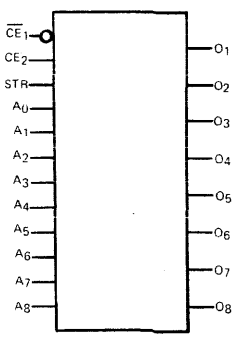
PIN NAMES

$A_0 - A_8$	ADDRESS INPUTS
$O_1 - O_8$	DATA OUTPUTS
$\overline{CE}_1 - CE_2$	CHIP ENABLE INPUTS
STR	LATCH INPUT

Functional Diagram



Logic Symbol



Refer to Harris Sales Offices for additional specifications.

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7647R-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7647R-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125° C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/enable "1" Input Current "0"	– –	0.0 -50	+25 -100	µA µA	V_{IH} = VCC Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.85	V V	VCC = VCC Min. VCC = VCC Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.7 –	3.3 0.35	– 0.45	V V	I_{OH} = -2.0mA, VCC = VCC Min. I_{OL} = +16mA, VCC = VCC Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	µA µA	V_{OH}, VCC = VCC Max. V_{OL} = 0.3V, VCC = VCC Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current	-20	–	-70	mA	VCC = VCC Max., V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	135	170	mA	VCC = VCC Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM - 7647R -2 5V ± 10% -55°C to +125°C			HM - 7647R - 5 5V ± 5% 0°C to +70°C				
SYMBOL	PARAMETER	MIN	TYP	MAX*	MIN	TYP	MAX*	UNITS	TEST CONDIT.
T_{AA} T_{EA}	Address Access Time Chip Enable Access Time	– –	40 30	60 40	– –	50 30	80 50	ns ns	 Transparent
T_{ADH} T_{CDH} T_{SW} T_{SL} T_{DL} T_{CDS}	Address Hold Time Chip Enable Hold Time Strobe Pulse Width Strobe Latch Time Strobe Delatch Time Chip Enable Set-Up Time	0 10 30 60 – 40	-10 0 15 35 – –	– – – – 40 –	0 10 30 80 – 40	-10 0 15 45 – –	– – – – 50 –	ns ns ns ns ns ns	Latched

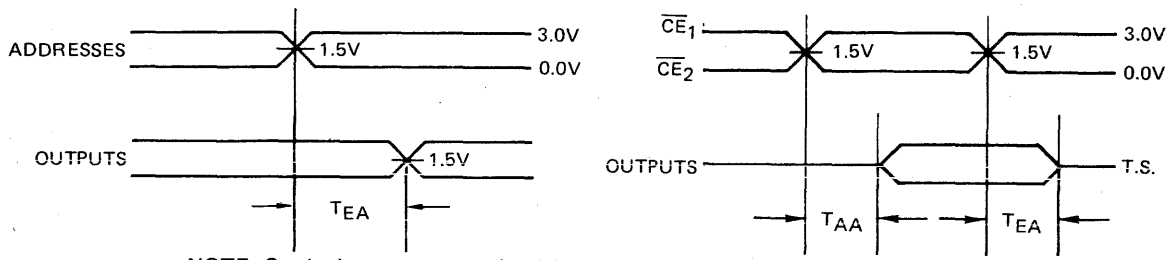
*A.C. Max. limits guarantee worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	12	pF	VCC = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	12	pF	VCC = 5V, V_{OUT} = 2.0V, f = 1MHz

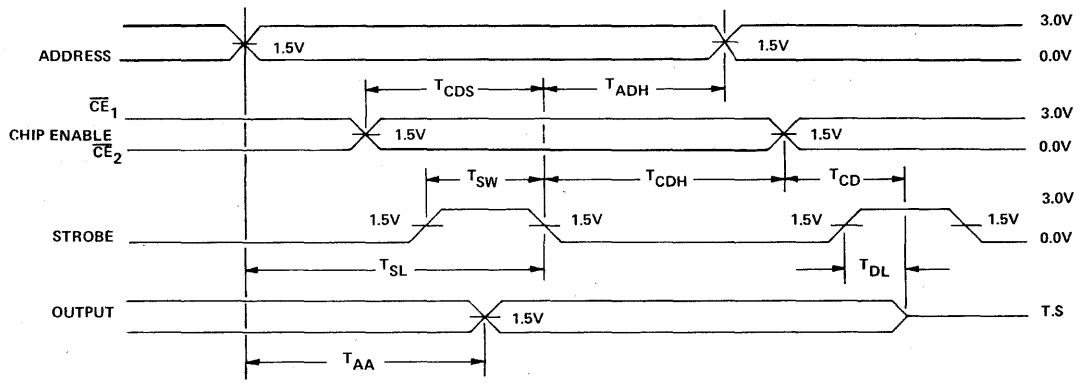
©IC MASTER 1978

SWITCHING TIME DEFINITIONS (TRANSPARENT MODE)

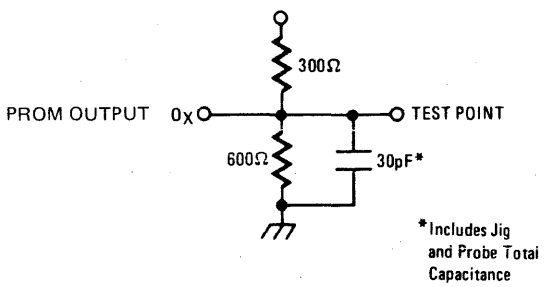


NOTE: Strobe input must remain high throughout read cycle while in transparent mode.

SWITCHING TIME DEFINITIONS (LATCHED MODE)



A.C. TEST LOAD



Programming

The HM-7647R PROM is manufactured with all bits/outputs logical "1" (output high). Any desired bit/output can be programmed to a logical "0" (output low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which can meet these specifications. This PROM can be programmed automatically or by the manual procedure shown below.

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PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS
V_{IH} V_{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V V
V_{PH} (2) V_{PL} (3)	Programming/Verify Voltage to V_{CC}	12.0 4.5	12.0 4.5	12.5 5.5	V V
I_{ILP}	Programming Input Low at V_{PH}	–	-250	-500	μA
tr tf	Programming (V_{CC}) Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10.0 10.0	μs μs
td	Programming Delay	10	10	100	μs
tp	Programming Pulse Width (4)	90	100	110	μs
D.C.	Programming Duty Cycle	–	50	90	%
V_{OPE} V_{OPD}	Output Voltage Enable (5) Disable	10.5 4.5	10.5 5.0	11.0 5.5	V V
I_{OPE}	Output Voltage Enable Current	–	–	10.0	mA
TC	Case Temperature	–	25	75	°C

During programming the chip must be disabled for proper operation.

NOTES:
1. No inputs should be left open for V_{IH}.
2. V_{PH} source must be capable for supplying one ampere.
3. It is recommended that dual verification be made at V_{PL} min. and V_{PL} max.
4. Note step 10 in programming procedure.
5. Disable condition will be met with output open circuited.

PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the word to be programmed. Address inputs are TTL compatible. An open circuit should not be used to address the PROM.

2. Bring the $\overline{CE}_1$ input high and the CE_2 input low to disable the device. The deselecting of the device during programming is an essential step in correctly programming this and all other Harris PROM's. The chip enables are TTL compatible. An open circuit should not be used to disable the chip.

3. Apply a logical "1" to the strobe input to place the chip in transparent read mode which is essential during programming. The strobe must remain high throughout the entire programming procedure.

4. Disable the programming circuitry by applying a voltage disable of V_{OPD} to the outputs of the PROM. The output may be left open to achieve the disable.

5. Raise V_{CC} to V_{PH} with rise time equal to t_r.

6. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.

7. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.

8. Lower V_{CC} to 4.5 volts following a delay of t_d from the last programming enable pulse applied to an output.

9. Enable the PROM for verification by applying a logic "0" to $\overline{CE}_1$ and a logic "1" to CE_2. Repeat verification at V_{CC} = 5.5 volts.

10. If any bit does not verify as programmed, repeat steps 2 through 9 until the bit has received a total of 1mSec. of programming time. Bits which do not program within 1mSec. are programming rejects. No further attempt to program these parts should be made.

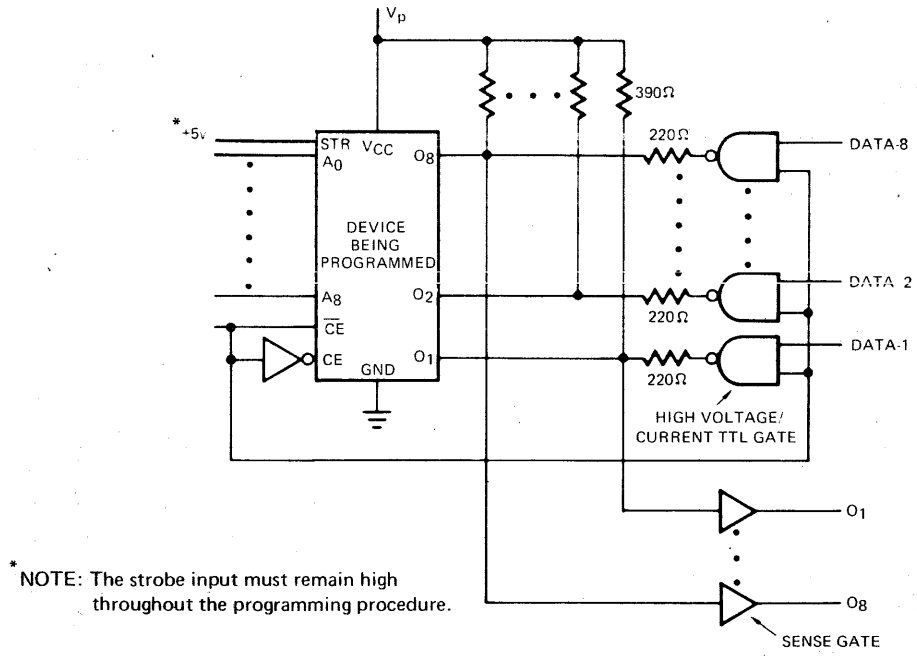
11. Repeat steps 1 through 10 for all other bits to be programmed in the PROM.

12. Programming rejects returned to the factory must be accompanied by data giving address, desired, and actual output data of a location in which a programming failure has occurred.

TYPICAL PROGRAMMING CIRCUIT

The circuit and timing diagrams shown in Figures 1 and 2 will establish the proper programming conditions for the output enable pulses. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must withstand inputs up to 12.5 volts during programming.

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*NOTE: The strobe input must remain high throughout the programming procedure.

FIGURE 1

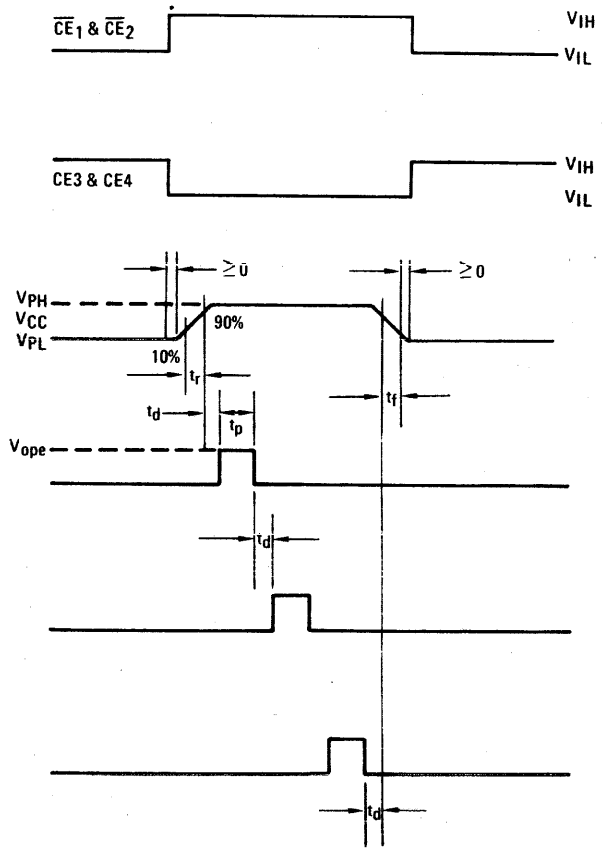


FIGURE 2

The strobe input must remain high throughout the programming procedure.

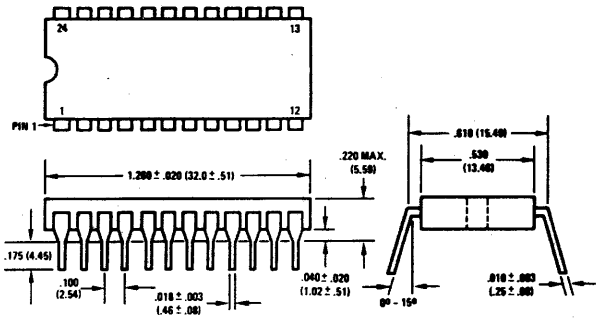
This timing diagram shows device terminal conditions. Each positive going data pulse at the terminal blows the corresponding bit resulting in a low output in that bit, therefore a low input at the DATA-X points of the Figure 1 circuit results in a permanent low output of a bit.

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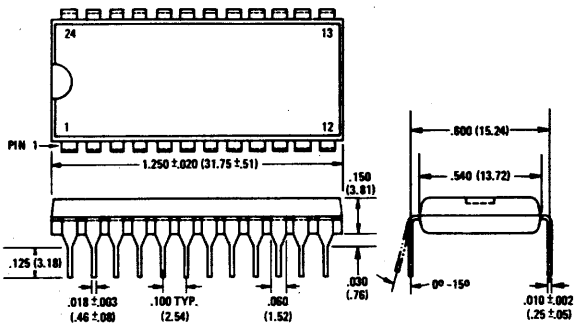
Packaging

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

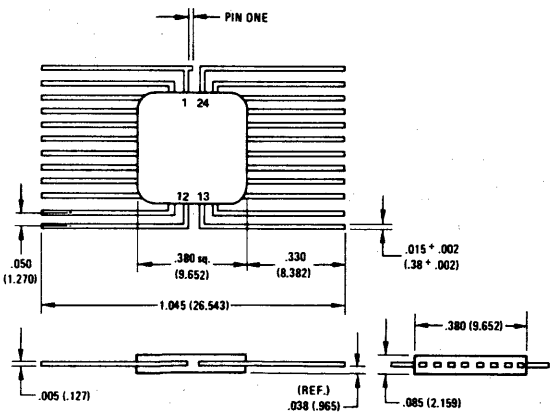
24 LEAD CERDIP
HM1 - 7647R



24 LEAD EPOXY D.I.P.
HM3 - 7647R



24 LEAD FLATPACK
HM9 - 7647R



Ordering Information

HM 1 - 76XX - 5

- HARRIS MEMORY
- DEVICE NUMBER
- PACKAGE
  - 1 – Cerdip
  - 3 – Epoxy
  - 9 – Flat Pack
- TEMPERATURE
  - 2 -55°C to 125°C
  - 5 0°C to 75°C
  - 8 Dash 8 Program MIL-STD-883 Class B

PACKAGE AVAILABILITY

TEMPERATURE	CERDIP	EPOXY	FLAT PACK
-2	YES	NO	YES
-5	YES	YES	NO
-8	YES	NO	YES

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Preliminary

HM-7649

512 x 8 PROM

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS AND A CHIP ENABLE INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH THE 74S472
- LOW INPUT LOADING

Description

The HM-7649 is a fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROM in a 512 word by 8 bit/word format and is available in a 20 pin D.I.P. (ceramic or epoxy) and a 20 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position. The HM-7649 has three state outputs.

Nichrome fuse technology is used on this and all other Harris Bipolar PROM's.

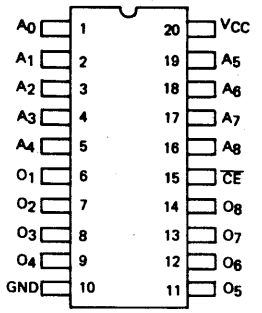
The pinout is identical to the 74S472 PROM.

The HM-7649 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

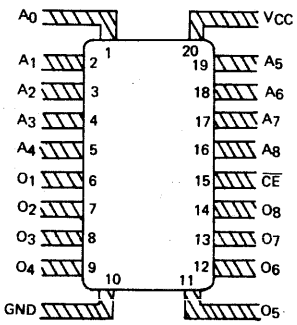
There is a chip enable input on the HM-7649 where $\overline{CE}$ low enables the device.

Pinouts

TOP VIEW – D.I.P.



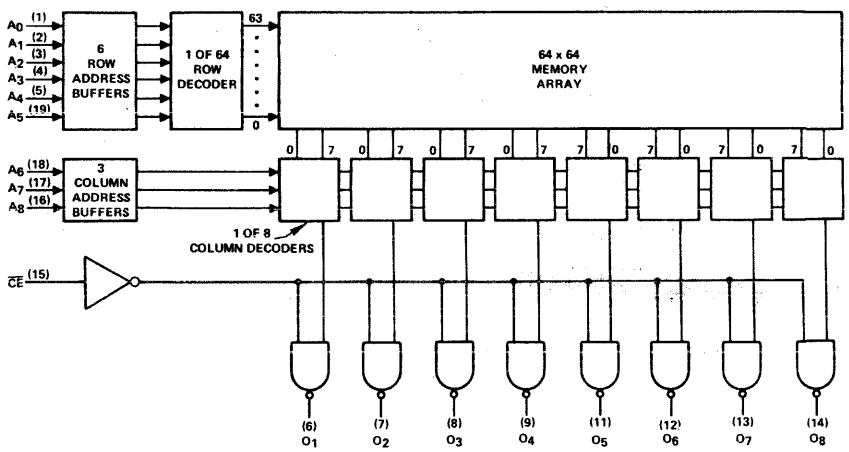
TOP VIEW – FLATPACK



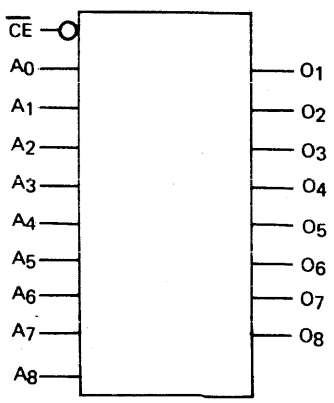
PIN NAMES

$A_0 - A_8$	ADDRESS INPUTS
$O_1 - O_8$	DATA OUTPUTS
$\overline{CE}$	CHIP ENABLE INPUT

Functional Diagram



Logic Symbol



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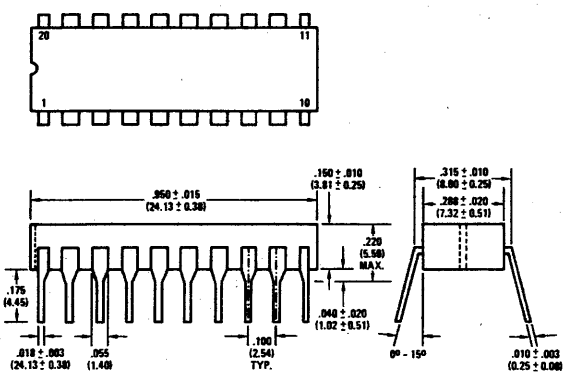
Refer to Harris Sales Offices for additional specifications.

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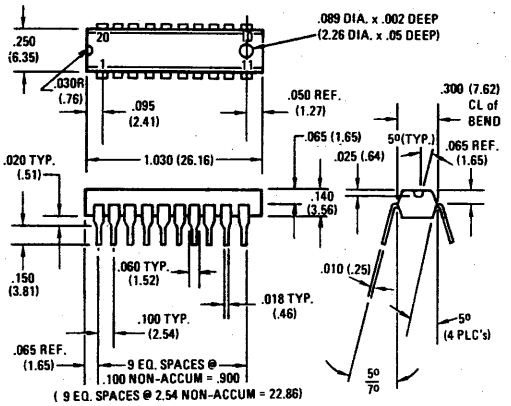
Packaging

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

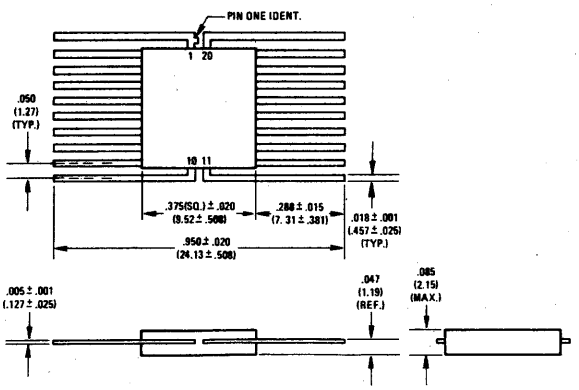
20 LEAD CERDIP
HM1-7649



20 LEAD EPOXY D.I.P.
HM3-7649



20 LEAD CER-PACK
HM9-7649



Ordering Information

HM 1 - 76XX - 5

- HARRIS MEMORY
- PACKAGE
  - 1 — Cerdip
  - 3 — Epoxy
  - 9 — Flat Pack
- DEVICE NUMBER
- TEMPERATURE
  - 2 -55°C to 125°C
  - 5 0°C to 75°C
  - 8 Dash 8 Program MIL-STD-883 Class B

PACKAGE AVAILABILITY

TEMPERATURE	CERDIP	EPOXY	CER-PACK
-2	YES	NO	YES
-5	YES	YES	NO
-8	YES	NO	YES

NOTICE: Harris Semiconductor's products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders.

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Preliminary

HM-7680/81

1K x 8 PROM

HM-7680 - Open Collector Outputs
HM-7681 - "Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE-STATE" OR OPEN COLLECTOR OUTPUTS AND FOUR CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-7680/81 is a fully decoded high speed Schottky TTL 8192/Bit Field Programmable ROM in a 1K word by 8 bit/word format with open collector (HM-7680) or "Three-State" (HM-7681) outputs. These PROM's are available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flat pack.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any one bit position.

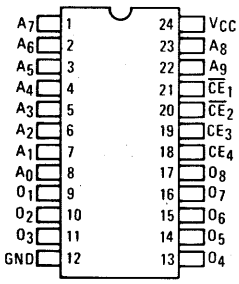
Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7680/81 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

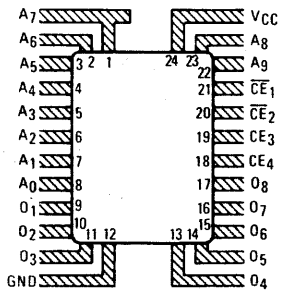
There are four chip enable inputs on the HM-7680/81. $\overline{CE}_1$, $\overline{CE}_2$ low, and CE_3, CE_4 high enables the chip.

Pinouts

TOP VIEW – D.I.P.



TOP VIEW – FLATPACK

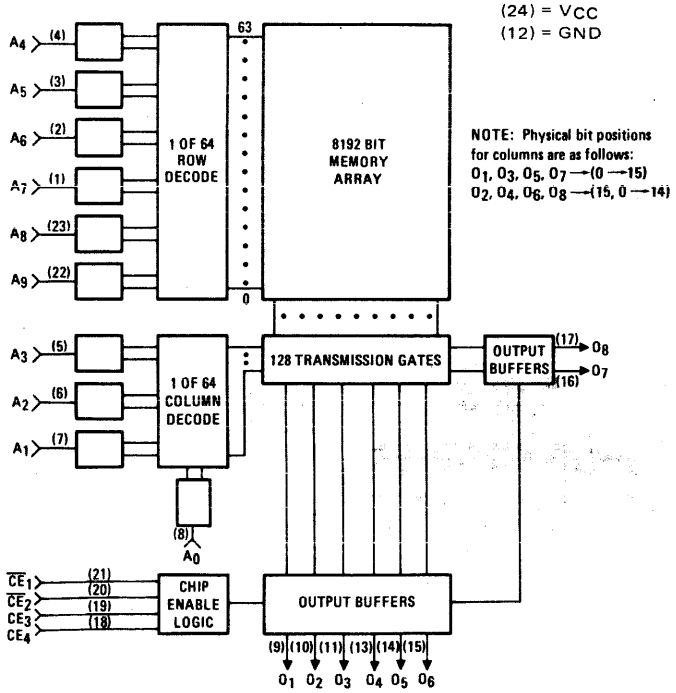


PIN NAMES

$A_0 - A_9$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$, CE_3, CE_4	Chip Enable Input

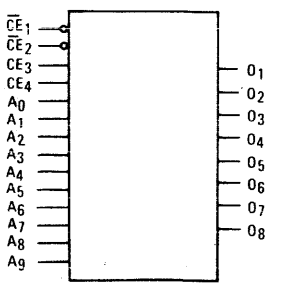
Functional Diagram

( ) = Pin Numbers
(24) = V_{CC}
(12) = GND



NOTE: Physical bit positions for columns are as follows:
$O_1, O_3, O_5, O_7 \rightarrow (0 \rightarrow 15)$
$O_2, O_4, O_6, O_8 \rightarrow (15, 0 \rightarrow 14)$

Logic Symbol



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Refer to Harris Sales Offices for additional specifications.

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7680/81-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7680/81-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/enable "1" Input Current "0"	– –	0.0 -50.0	+40 -100	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	0.0 0.0	+40 -40	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current	-15	–	-100	mA	V_{CC} = V_{CC} Max., V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7680/81-5 5V ±5% 0°C to + 75°C			HM-7680/81-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX*	MIN	TYP	MAX*	UNITS
T_{AA}	Address Access Time	–	45	60	–	–	80	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

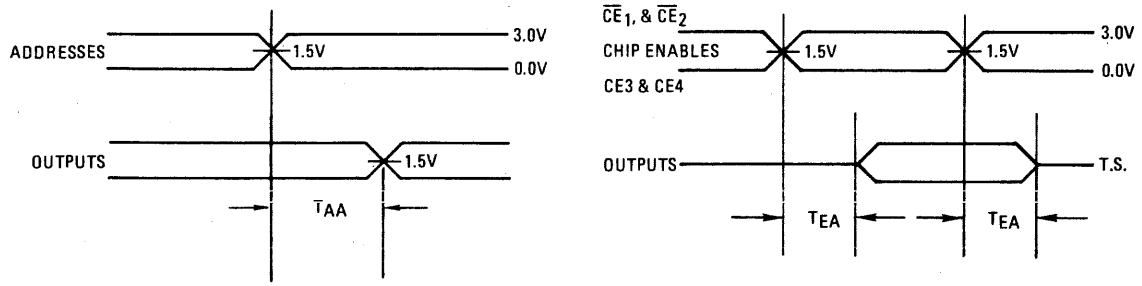
*A.C. Max. limits guarantee worst case N^2 sequencing.

CAPACITANCE : T_A = 25°C

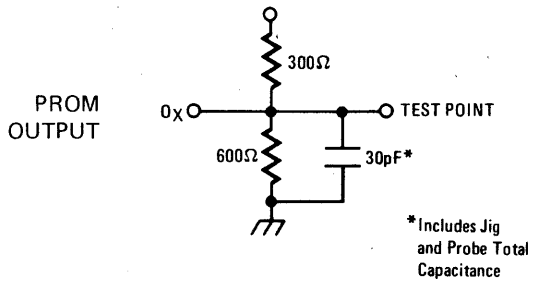
SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Add Input Capacitance	12	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	12	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



Programming

The HM-7680/81 PROM is manufactured with all bits/outputs logical "1" (output high). Any desired bit/output can be programmed to a logical "0" (output low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which can meet these specifications. This PROM can be programmed automatically or by the manual procedure shown below.

PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS
V_{IH} V_{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V V
V_{PH} (2) V_{PL} (3)	Programming/Verify Voltage to V_{CC}	12.0 4.5	12.0 4.5	12.5 5.5	V V
I_{ILP}	Programming Input Low at V_{PH}	–	.250	.500	mA
tr tf	Programming (V_{CC}) Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10.0 10.0	µs µs
td	Programming Delay	10	10	100	µs
tp	Programming Pulse Width (4)	90	100	110	µs
D.C.	Programming Duty Cycle	–	50	90	%
V_{OPE} V_{OPD}	Output Voltage Enable (5) Disable	10.5 4.5	10.5 5.0	11.0 5.5	V V
I_{OPE}	Output Voltage Enable Current	–	–	10.0	mA
TC	Case Temperature	–	25	75	°C

During programming the chip must be disabled for proper operation.

NOTES:
1. No inputs should be left open for V_{IH}.
2. V_{PH} source must be capable for supplying one ampere.
3. It is recommended that dual verification be made at V_{PL} min. and V_{PL} max.
4. Note step 9 in programming procedure.
5. Disable condition will be met with output open circuited.

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PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the word to be programmed. Address inputs are TTL compatible. An open circuit should not be used to address the PROM.

2. Bring the $\overline{CE}_1$ and $\overline{CE}_2$ inputs high and the CE_3 and CE_4 inputs low to disable the device. The deselecting of the device during programming is an essential step in correctly programming this and all other Harris PROM's. The chip enables are TTL compatible. An open circuit should not be used to disable the chip.

3. Disable the programming circuitry by applying a voltage disable of V_{OPD} to the outputs of the PROM. The output may be left open to achieve the disable.

4. Raise V_{CC} to V_{PH} with rise time equal to t_r.

5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.

6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.

7. Lower V_{CC} to 4.5 volts following a delay of t_d from the last programming enable pulse applied to an output.

8. Enable the PROM for verification by applying a logic "0" to $\overline{CE}_1$ and $\overline{CE}_2$ and a logic "1" to CE_3 and CE_4. Repeat verification at V_{CC} = 5.5 volts.

9. If any bit does not verify as programmed, repeat steps 2 through 8 until the bit has received a total of 1msec of programming time. Bits which do not program within 1msec are programming rejects. No further attempt to program these parts should be made.

10. Repeat steps 1 through 9 for all other bits to be programmed in the PROM.

11. Programming rejects returned to the factory must be accompanied by data giving address, desired, and actual output data of a location in which a programming failure has occured.

TYPICAL PROGRAMMING CIRCUIT

The circuit and timing diagrams shown in Figures 1 and 2 will establish the proper programming conditions for the output enable pulses. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must withstand inputs up to 12.5 volts during programming.

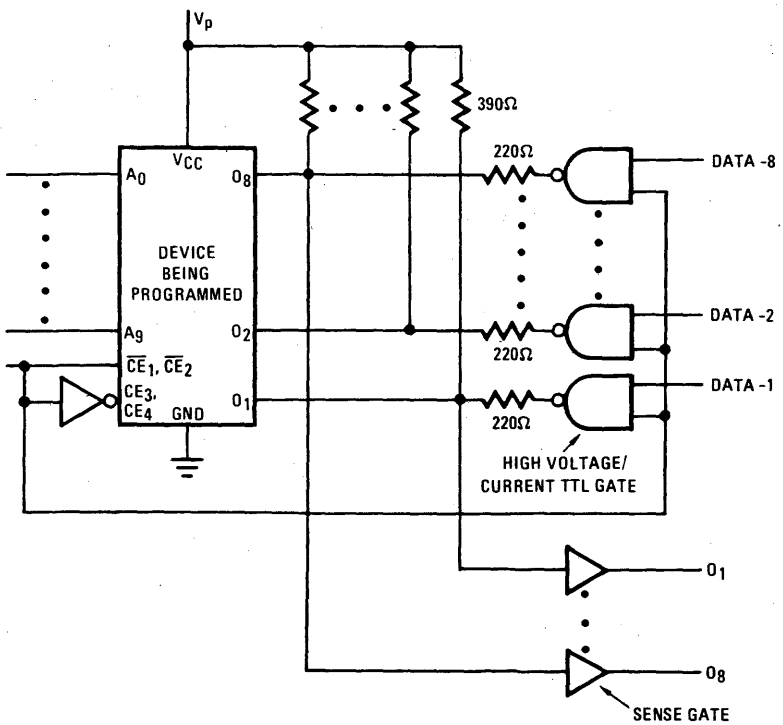


FIGURE 1

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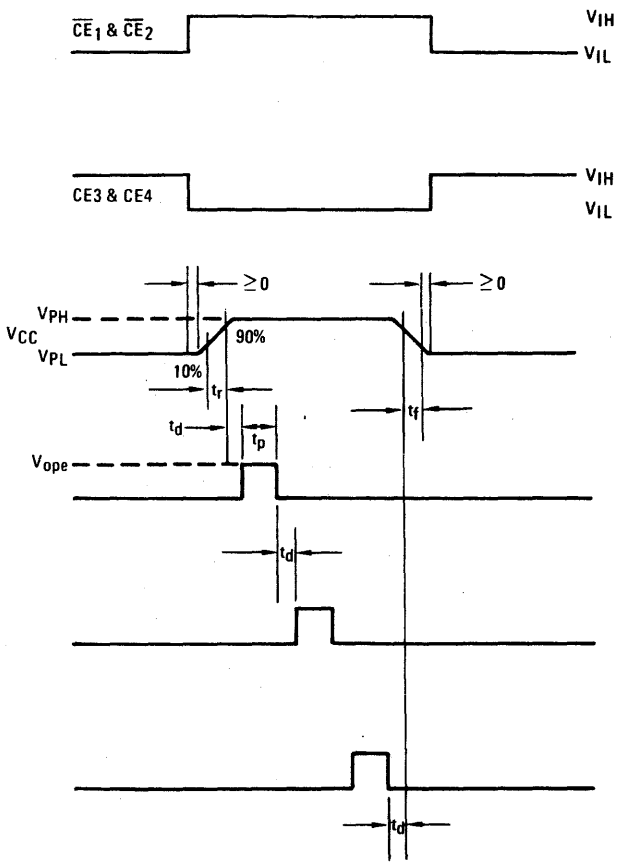


FIGURE 2

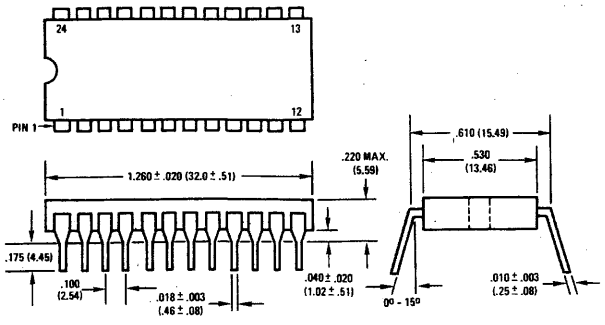
This timing diagram shows device terminal conditions. Each positive going data pulse at the terminal blows the corresponding bit, resulting in a low output for that bit. Therefore, a low input at the DATA-X points of the Figure 1 circuit results in a permanent low output of a bit.

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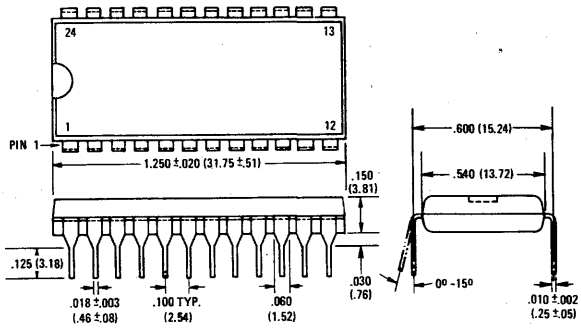
Packaging

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

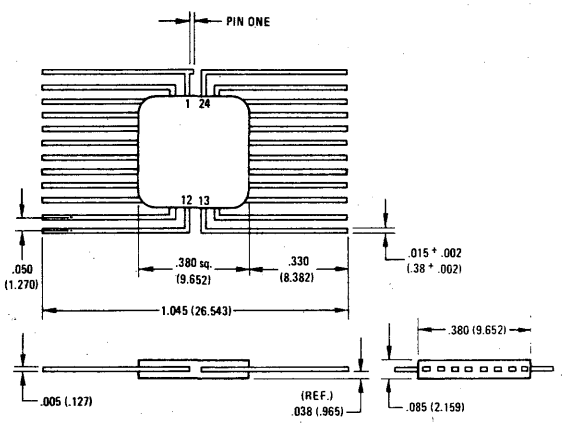
24 LEAD CERDIP
HM1-7680/81



24 LEAD EPOXY D.I.P.
HM3-7680/81



24 LEAD FLATPACK
HM9-7680/81



Ordering Information

HM 1 - 76XX - 5

HARRIS MEMORY

DEVICE NUMBER

PACKAGE
1 – Cerdip
3 – Epoxy
9 – Flat Pack

TEMPERATURE
2 -55°C to 125°C
5 0°C to 75°C
8 Dash 8 Program MIL-STD-883 Class B

PACKAGE AVAILABILITY

TEMPERATURE	CERDIP	EPOXY	FLAT PACK
-2	YES	NO	YES
-5	YES	YES	NO
-8	YES	NO	YES

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Preliminary

HM-7680R/81R
1K x 8 PROM

HM-7680R - Open Collector Outputs
HM-7681R - "Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND THREE CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURES AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LATCHED OUTPUTS

Description

The HM-7680R/81R is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 1K word by 8 bit/word format with open collector (HM-7680R) or "Three State" (HM-7681R) outputs. These PROMs are available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROM's.

The HM-7680R/81R contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

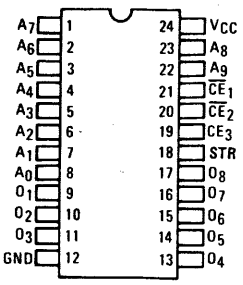
There are three chip enable inputs on the HM-7680R/81R. $\overline{CE}_1$, $\overline{CE}_2$ low and CE_3 high enables the chip.

The HM-7680R/81R is operated in the Transparent Read mode by holding the strobe input high throughout the read operation. This is the normal read mode where the three chip enable inputs will control the outputs.

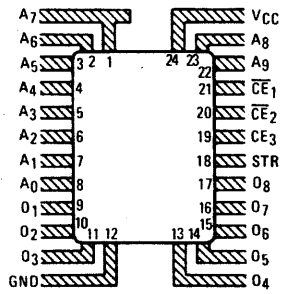
In Latched Read mode, bringing the strobe input low will latch the outputs and chip enable inputs. If the device is disabled when the strobe input is low, the outputs will be latched in the high impedance state. If the device is in the latched mode the strobe input must be brought high to allow the outputs to respond to new address or chip enable conditions.

Pinouts

TOP VIEW – D.I.P.



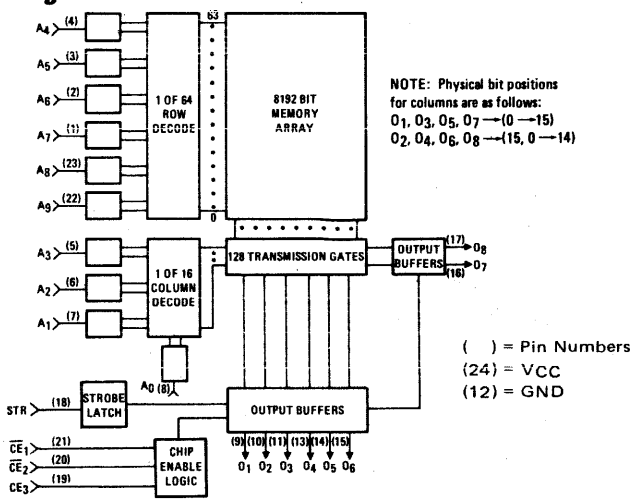
TOP VIEW – FLATPACK



PIN NAMES

A0 – A9	Address Inputs
O1 – O8	Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$, CE_3	Chip Enable Input
STR	Strobe

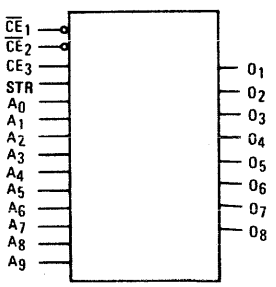
Functional Diagram



NOTE: Physical bit positions for columns are as follows:
O_1, O_3, O_5, O_7 → (0 → 15)
O_2, O_4, O_6, O_8 → (15, 0 → 14)

( ) = Pin Numbers
(24) = VCC
(12) = GND

Logic Symbol



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Refer to Harris Sales Offices for additional specifications.

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7680R/81R-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7680R/81R-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/enable "1" Input Current "0"	– –	0.0 -50.0	+40 -100	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	0.0 0.0	+40 -40	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current	-15	–	-100	mA	V_{CC} = V_{CC} Max., V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7680R/81R-5 5V ±5% 0°C to +75°C			HM-7680R/81R-2 5V ±10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX*	MIN	TYP	MAX*	UNITS	TEST CONDIT.
T_{AA} T_{EA}	Address Access Time Chip Enable Access Time	– –	45 20	60 30	– –	– –	80 40	ns ns	Latched or Transparent
T_{ADH} T_{CDH} T_{SW} T_{SL} T_{DL} T_{CDS}	Address Hold Time Chip Enable Hold Time Strobe Pulse Width Strobe Latch Time Strobe Delatch Time Chip Enable Set-Up Time	0 10 30 60 – 40	-10 0 10 40 – –	– – – – 40 –	0 10 30 60 – 40	-10 0 10 40 – –	– – – – 40 –	ns ns ns ns ns ns	Latched Only

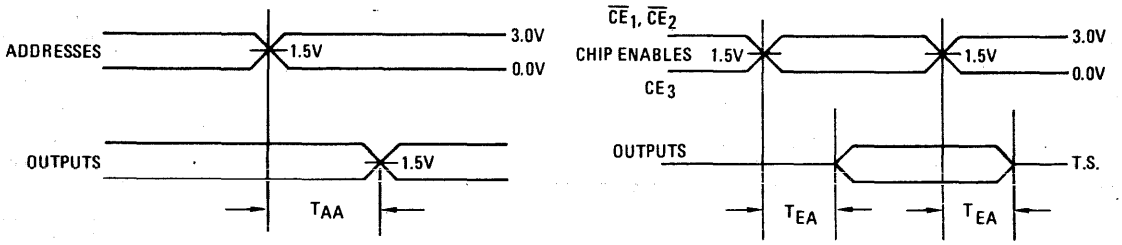
*A.C. Max. limits guarantee worst case N^2 sequencing.

CAPACITANCE : T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Add Input Capacitance	12	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	12	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

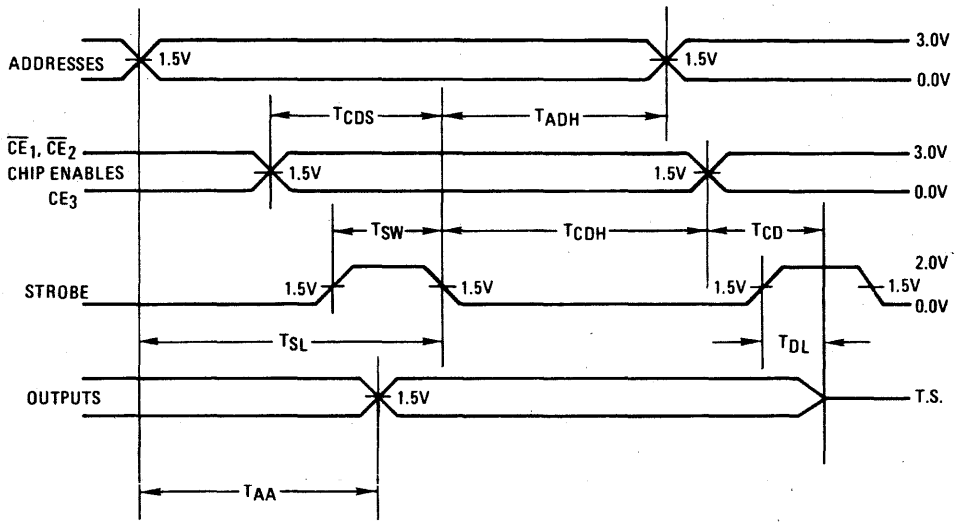
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SWITCHING TIME DEFINITIONS (Transparent Mode)

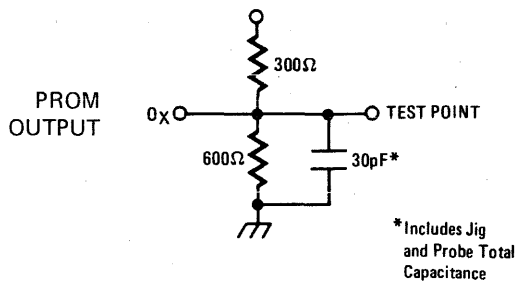


NOTE: Strobe input must remain high throughout read cycle while in transparent mode.

SWITCHING TIME DEFINITIONS (Latched Mode)



A.C. TEST LOAD



Programming

The HM-7680R/81R PROM is manufactured with all bits/outputs logical "1" (output high). Any desired bit/output can be programmed to a logical "0" (output low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which can meet these specifications. This PROM can be programmed automatically or by the manual procedure shown on the next page.

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PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS
V_{IH} V_{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V V
V_{PH} (2) V_{PL} (3)	Programming/Verify Voltage to V_{CC}	12.0 4.5	12.0 4.5	12.5 5.5	V V
I_{ILP}	Programming Input Low at V_{PH}	–	.250	.500	mA
t_r t_f	Programming (V_{CC}) Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10.0 10.0	μs μs
t_d	Programming Delay	10	10	100	μs
t_p	Programming Pulse Width (4)	90	100	110	μs
D.C.	Programming Duty Cycle	–	50	90	%
V_{OPE} V_{OPD}	Output Voltage Enable (5) Disable	10.5 4.5	10.5 5.0	11.0 5.5	V V
I_{OPE}	Output Voltage Enable Current	–	–	10.0	mA
TC	Case Temperature	–	25	75	°C

During programming the chip must be disabled for proper operation.

NOTES:
1. No inputs should be left open for V_{IH}.
2. V_{PH} source must be capable for supplying one ampere.
3. It is recommended that dual verification be made at V_{PL} min. and V_{PL} max.
4. Note step 10 in programming procedure.
5. Disable condition will be met with output open circuited.

PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the word to be programmed. Address inputs are TTL compatible. An open circuit should not be used to address the PROM.

2. Bring the $\overline{CE}_1$ and $\overline{CE}_2$ inputs high and the CE_3 inputs low to disable the device. The deselecting of the device during programming is an essential step in correctly programming this and all other Harris PROM's. The chip enables are TTL compatible. An open circuit should not be used to disable the chip.

3. Apply a logical "1" to the strobe input to place the chip in transparent read mode which is essential during programming. The strobe must remain high throughout the entire programming procedure.

4. Disable the programming circuitry by applying a voltage disable of V_{OPD} to the outputs of the PROM. The output may be left open to achieve the disable.

5. Raise V_{CC} to V_{PH} with rise time equal to t_r.

6. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.

7. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.

8. Lower V_{CC} to 4.5 volts following a delay of t_d from the last programming enable pulse applied to an output.

9. Enable the PROM for verification by applying a logic "0" to $\overline{CE}_1$ and $\overline{CE}_2$ and a logic "1" to CE_3. Repeat verification at V_{CC} = 5.5 volts.

10. If any bit does not verify as programmed, repeat steps 2 through 9 until the bit has received a total of 1msec of programming time. Bits which do not program within 1msec are programming rejects. No further attempt to program these parts should be made.

11. Repeat steps 1 through 10 for all other bits to be programmed in the PROM.

12. Programming rejects returned to the factory must be accompanied by data giving address, desired, and actual output data of a location in which a programming failure has occured.

TYPICAL PROGRAMMING CIRCUIT

The circuit and timing diagrams shown in Figures 1 and 2 will establish the proper programming conditions for the output enable pulses. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must withstand inputs up to 12.5 volts during programming.

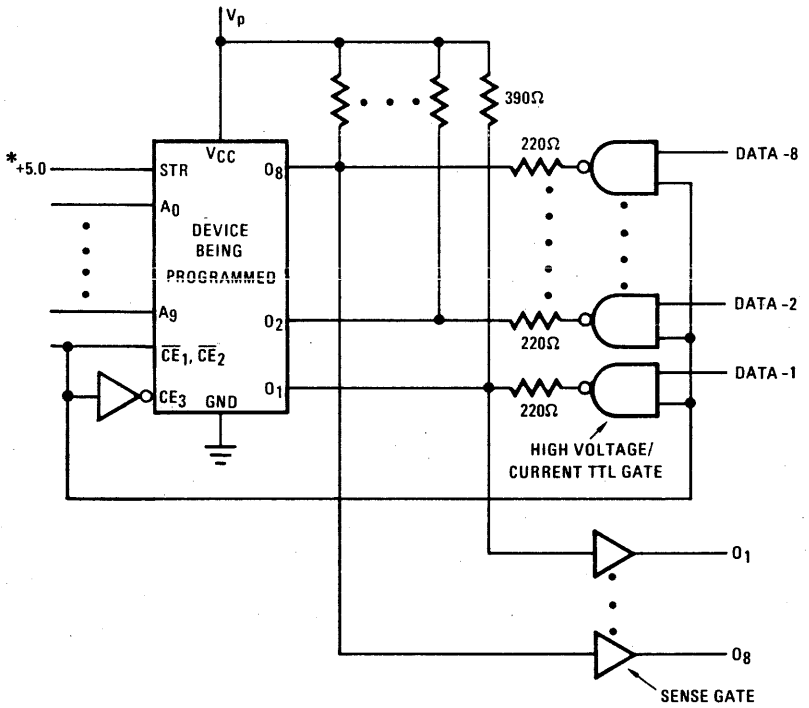


FIGURE 1

*The Strobe Input must remain high throughout the programming procedure.

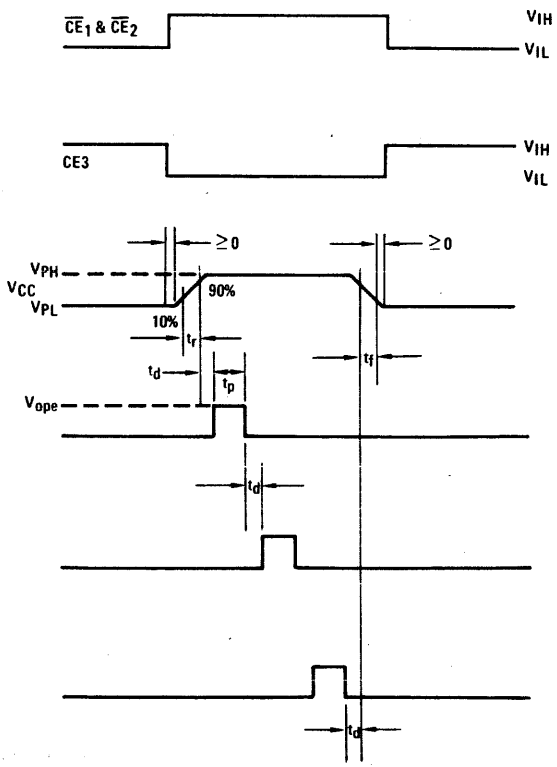


FIGURE 2

The Strobe Input must remain high throughout the programming procedure.

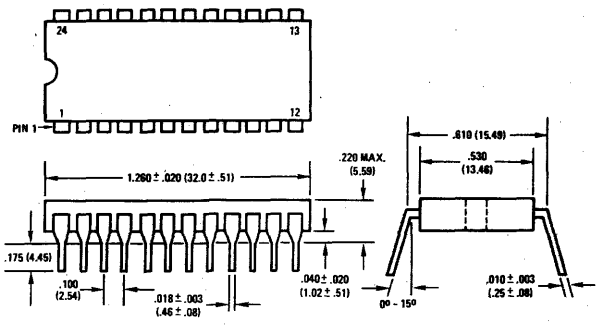
This timing diagram shows device terminal conditions. Each positive going data pulse at the terminal blows the corresponding bit, resulting in a low output for that bit. Therefore, a low input at the DATA-X points of the Figure 1 circuit results in a permanent low output of a bit.

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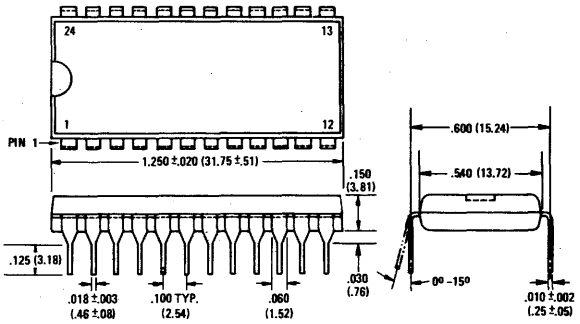
Packaging

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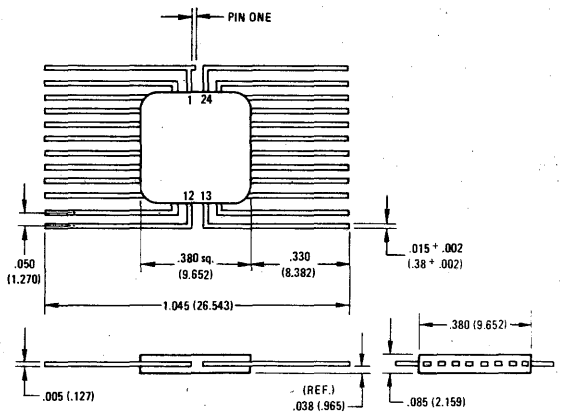
24 LEAD CERDIP
HM1-7680R/81R



24 LEAD EPOXY D.I.P.
HM3-7680R/81R



24 LEAD FLATPACK
HM9-7680R/81R



Ordering Information

HM 1 - 76XX - 5

- HARRIS MEMORY
- DEVICE NUMBER
- PACKAGE
  - 1 – Cerdip
  - 3 – Epoxy
  - 9 – Flat Pack
- TEMPERATURE
  - 2 -55°C to 125°C
  - 5 0°C to 75°C
  - 8 Dash 8 Program MIL-STD-883 Class B

PACKAGE AVAILABILITY

TEMPERATURE	CERDIP	EPOXY	FLAT PACK
-2	YES	NO	YES
-5	YES	YES	NO
-8	YES	NO	YES

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Preliminary

HM-7680P/81P

1K x 8 PROM

HM-7680P - Open Collector Outputs
HM-7681P - "Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND FOUR POWER DOWN INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7680P/81P is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 1K word by 8 bit/word format with open collector (HM-7680P) or "three state" (HM-7681P) outputs. These PROM's are available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flatpack.

All bits are manufactured storing a logical "1" (pcsitive logic) and can be selectively programmed for a logical "0" in any bit position.

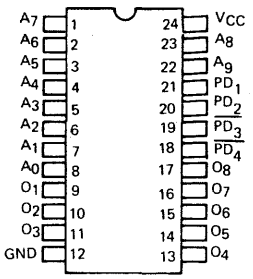
Nichrome fuse technology is used on these and all other Harris Bipolar PROM's.

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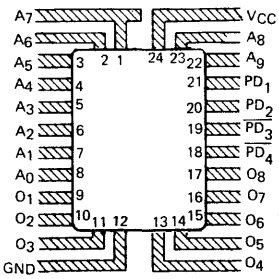
There are four power down inputs on the HM-7680P/81P which are similar to chip enables. The chip is enabled or disabled using the power down inputs where a disabled chip dissipates 30% of nominal power and the outputs go to a high impedance state. The chip is powered up (enabled) when PD_1 and PD_2 are low and $\overline{PD}_3$ and $\overline{PD}_4$ are high.

Pinouts

TOP VIEW – D.I.P.



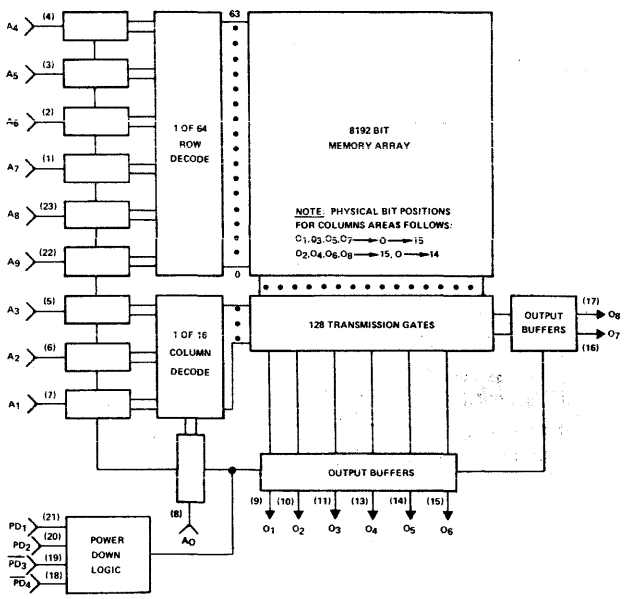
TOP VIEW – FLATPACK



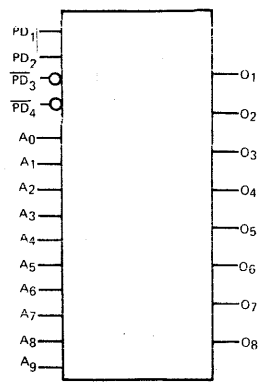
PIN NAMES

$A_0 - A_9$	ADDRESS INPUTS
$O_1 - O_8$	ADDRESS OUTPUTS
$PD_1, PD_2, \overline{PD_3}, \overline{PD_4}$	POWER DOWN INPUTS

Functional Diagram



Logic Symbol



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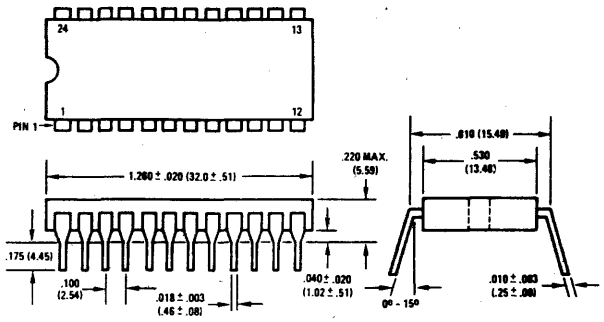
Refer to Harris Sales Offices for additional specifications.

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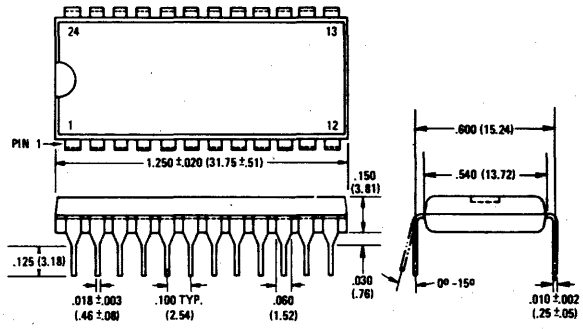
Packaging

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

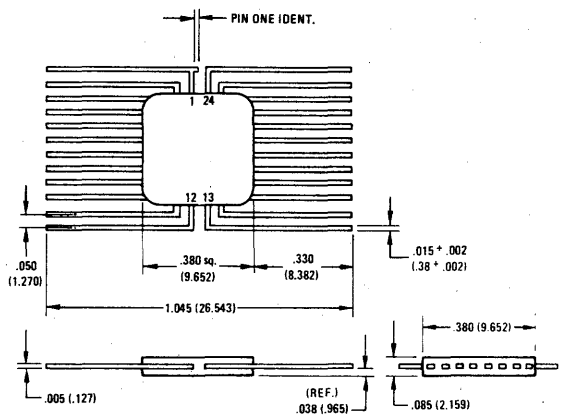
24 LEAD CERAMIC D.I.P.
HM1-7680P/81P



24 LEAD EPOXY D.I.P.
HM3-7680P/81P



24 LEAD FLATPACK
HM9-7680P/81P



Ordering Information

HM 1 - 76XX - 5

- HARRIS MEMORY
- PACKAGE: 1 — Cerdip; 3 — Epoxy; 9 — Flat Pack
- DEVICE NUMBER
- TEMPERATURE: 2 -55°C to 125°C; 5 0°C to 75°C; 8 Dash 8 Program MIL-STD-883 Class B

PACKAGE AVAILABILITY

TEMPERATURE	CERDIP	EPOXY	FLAT PACK
-2	YES	NO	YES
-5	YES	YES	NO
-8	YES	NO	YES

NOTICE: Harris Semiconductor's products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders.

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HM-7680RP/81RP

Preliminary 1K x 8 PROM

HM-7680RP - Open Collector Outputs
HM-7681RP - "Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND TWO CHIP ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.
- LATCHED OUTPUTS.
- A POWER DOWN INPUT ALLOWING 70% REDUCTION IN NOMINAL POWER DISSIPATION.

Description

The HM-7680RP/81RP are fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM's in a 1K word by 8 bit/word format with open collector (HM-7680RP) or "three state." (HM-7681RP) outputs. These PROM's are available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROM's.

The HM-7680RP/81RP contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are two chip enable inputs on the HM-7680RP/81RP. $\overline{CE}_1$, $\overline{CE}_2$ low enables the device.

There is a power down input on this device. A powered down chip has a 70% reduction in power dissipation if the outputs are not latched and a 50% reduction in power if the outputs are latched.

The HM-7680RP/81RP is operated in the Transparent Read mode by holding the strobe input high and the $\overline{PD}$ input high throughout the read operation. This is the normal read mode where the two chip enables and the power down inputs will control the outputs.

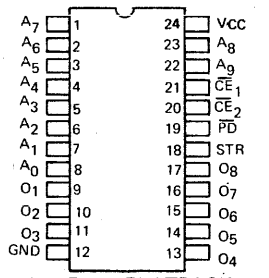
In Latched Read mode, bringing the strobe input low will latch the outputs and the chip enable inputs. However, the power down input is independent of the latched function and can be changed while in the latched mode. If the device is disabled when the strobe input goes low, the outputs will be latched in the high impedance state. If the device is in the latched mode the strobe input must be brought high to allow the outputs to respond to new address or chip enable conditions.

The following is a summary of the functional dependencies of the operating modes:

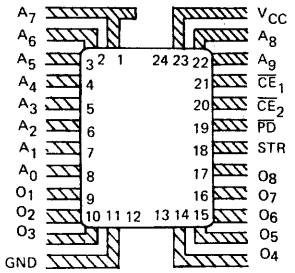
1. Chip enabled, transparent, power up – normal mode where the power down input is effectively a chip enable.
2. Chip enabled, latched, power up – this is normal latched mode where the output remains latched regardless of address and chip enable switching.
3. Chip enabled, latched, power down – this is the powered down latched mode where the output data ramains latched while power is reduced to 50% of its normal value. If the latch strobe changes state while in this mode, the outputs will go to a high impedance state and power will reduce to 30% of nominal power.
4. Chip disabled, transparent, power down – this is the normal powered down mode where the outputs are in a high impedance state and the power is reduced to 30% of the nominal power.

Following is a table to clarify the operational interdependencies.

Pinouts TOP VIEW – D.I.P.



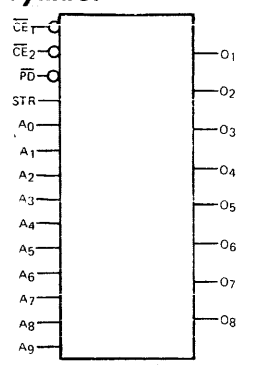
TOP VIEW – FLATPACK



PIN NAMES

$A_6 - A_9$	ADDRESS INPUTS
$O_1 - O_8$	DATA OUTPUTS
$\overline{CE}_1 - \overline{CE}_2$	CHIP ENABLE INPUTS
$\overline{PD}$	POWER DOWN INPUT
STR	STROBE INPUT

Logic Symbol



TRUTH TABLE for HM-7680RP/81RP

$\overline{PD}$	STR	$\overline{CE}_2$	$\overline{CE}_1$	OUTPUTS	POWER
0	0	0	0	LATCHED DATA	50%
0	0	0	1	LATCHED 3-STATE	50%
0	0	1	0	LATCHED 3-STATE	50%
0	0	1	1	LATCHED 3-STATE	50%
0	1	0	0	UNLATCHED 3-STATE	30%
0	1	0	1	UNLATCHED 3-STATE	30%
0	1	1	0	UNLATCHED 3-STATE	30%
0	1	1	1	UNLATCHED 3-STATE	30%
1	0	0	0	LATCHED DATA	100%
1	0	0	1	LATCHED 3-STATE	100%
1	0	1	0	LATCHED 3-STATE	100%
1	0	1	1	LATCHED 3-STATE	100%
1	1	0	0	UNLATCHED DATA	100%
1	1	0	1	UNLATCHED 3-STATE	100%
1	1	1	0	UNLATCHED 3-STATE	100%
1	1	1	1	UNLATCHED 3-STATE	100%

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION

Preliminary

HM-7608

1K x 8 PROM

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE-STATE" OUTPUTS WITH A CHIP ENABLE INPUT
- SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH THE 2708 WITH:
  - ONLY ONE 5 VOLT SUPPLY
  - SUPERIOR ACCESS TIME
  - FASTER PROGRAMMING TIME

Description

The HM-7608 is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 1K word by 8 bit/word format and is available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flat pack.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position, the HM-7608 has three-state outputs.

Nichrome fuse technology is used on this and all other Harris Bipolar PROM's.

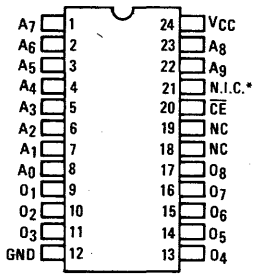
The HM-7608 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

This PROM is a plug in replacement for the 2708 where the V_{SS} pin on the 2708 becomes GND on the HM-7608. The V_{BB}, VDD, and program pins on the 2708 are all N.C. on the HM-7608.

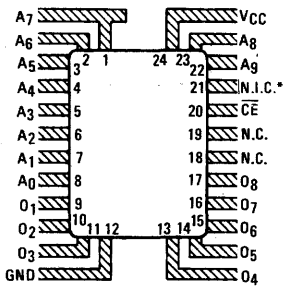
There is a chip enable input on the HM-7608 where $\overline{CE}$ low enables the device.

Pinouts

TOP VIEW – D.I.P.



TOP VIEW – FLATPACK

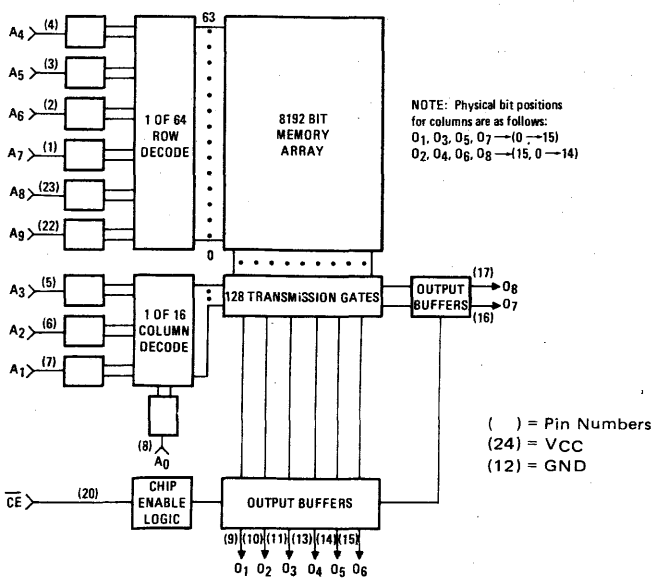


PIN NAMES

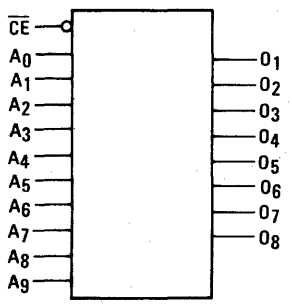
$A_0 - A_9$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}$	Chip Enable Input

*No Internal Connect

Functional Diagram



Logic Symbol



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Refer to Harris Sales Offices for additional specifications.

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7608-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7608-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/enable "1" Input Current "0"	– –	0.0 -50.0	+40 -100	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	0.0 0.0	+40 -40	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current	-15	–	-100	mA	V_{CC} = V_{CC} Max., V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7608-5 5V ±5% 0°C to + 75°C			HM-7608-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX*	MIN	TYP	MAX*	UNITS
T_{AA}	Address Access Time	–	45	60	–	–	80	ns
T_{EA}	Chip Enable Access Time	–	20	30	–	–	40	ns

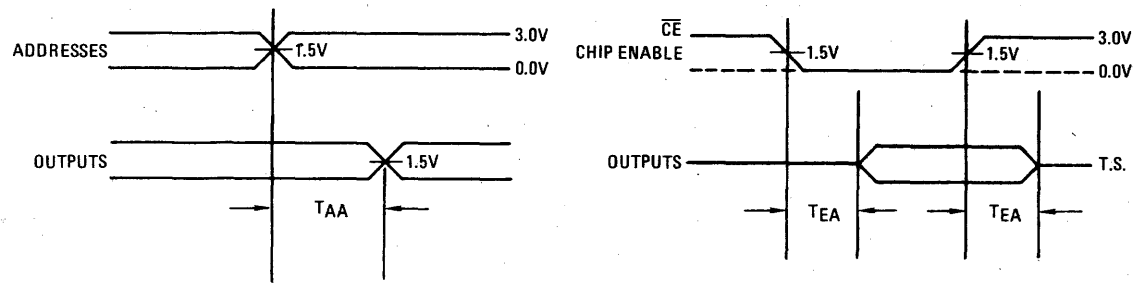
*A.C. Max. limits guarantee worst case N^2 sequencing.

CAPACITANCE : T_A = 25°C

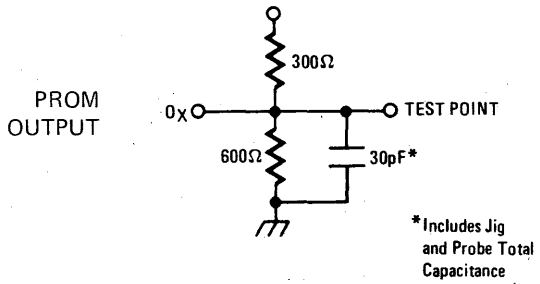
SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Add Input Capacitance	12	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	12	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



Programming

The HM-7608 PROM is manufactured with all bits/outputs logical "1" (output high). Any desired bit/output can be programmed to a logical "0" (output low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which can meet these specifications. This PROM can be programmed automatically or by the manual procedure shown below.

PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS
V_{IH} V_{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.8	V V
V_{PH} (2) V_{PL} (3)	Programming/Verify Voltage to V_{CC}	12.0 4.5	12.0 4.5	12.5 5.5	V V
I_{ILP}	Programming Input Low at V_{PH}	–	.250	.500	mA
tr tf	Programming (V_{CC}) Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10.0 10.0	µs µs
td	Programming Delay	10	10	100	µs
tp	Programming Pulse Width (4)	90	100	110	µs
D.C.	Programming Duty Cycle	–	50	90	%
V_{OPE} V_{OPD}	Output Voltage Enable (5) Disable	10.5 4.5	10.5 5.0	11.0 5.5	V V
I_{OPE}	Output Voltage Enable Current	–	–	10.0	mA
TC	Case Temperature	–	25	75	°C

During programming the chip must be disabled for proper operation.

NOTES:
1. No inputs should be left open for V_{IH}.
2. V_{PH} source must be capable for supplying one ampere.
3. It is recommended that dual verification be made at V_{PL} min. and V_{PL} max.
4. Note step 9 in programming procedure.
5. Disable condition will be met with output open circuited.

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PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the word to be programmed. Address inputs are TTL compatible. An open circuit should not be used to address the PROM.

2. Bring the $\overline{CE}$ input high to disable the device. The deselecting of the device during programming is an essential step in correctly programming this and all other Harris PROM's. The chip enable is TTL compatible. An open circuit should not be used to disable the chip.

3. Disable the programming circuitry by applying a voltage disable of V_{OPD} to the outputs of the PROM. The output may be left open to achieve the disable.

4. Raise V_{CC} to V_{PH} with rise time equal to t_r.

5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.

6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.

7. Lower V_{CC} to 4.5 volts following a delay of t_d from the last programming enable pulse applied to an output.

8. Enable the PROM for verification by applying a logic "0" to $\overline{CE}$. Repeat verification at V_{CC} = 5.5 volts.

9. If any bit does not verify as programmed, repeat steps 2 through 8 until the bit has received a total of 1msec of programming time. Bits which do not program within 1msec are programming rejects. No further attempt to program these parts should be made.

10. Repeat steps 1 through 9 for all other bits to be programmed in the PROM.

11. Programming rejects returned to the factory must be accompanied by data giving address, desired, and actual output data of a location in which a programming failure has occured.

TYPICAL PROGRAMMING CIRCUIT

The circuit and timing diagrams shown in Figures 1 and 2 will establish the proper programming conditions for the output enable pulses. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must withstand inputs up to 12.5 volts during programming.

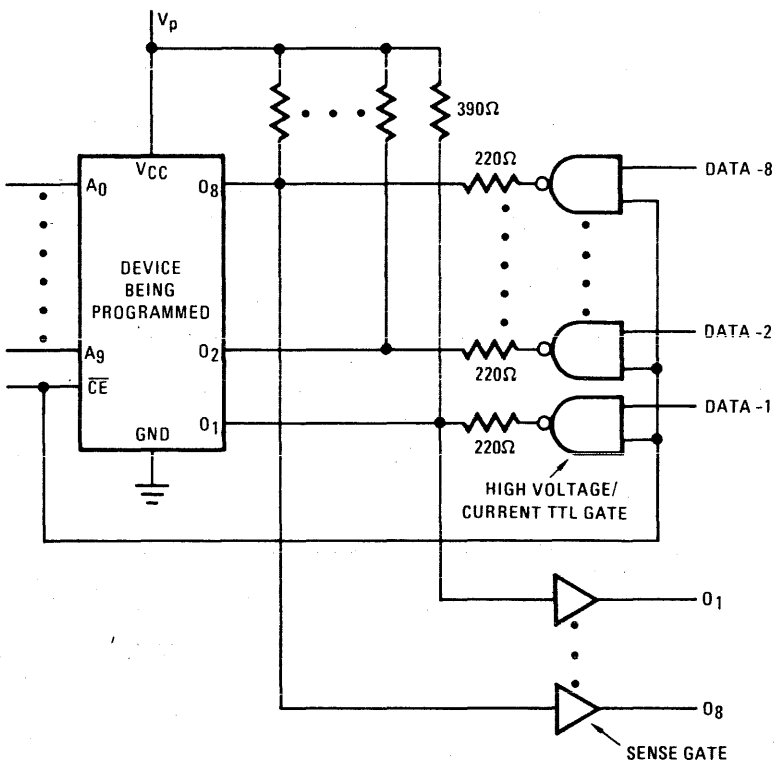


FIGURE 1

©IC MASTER 1978

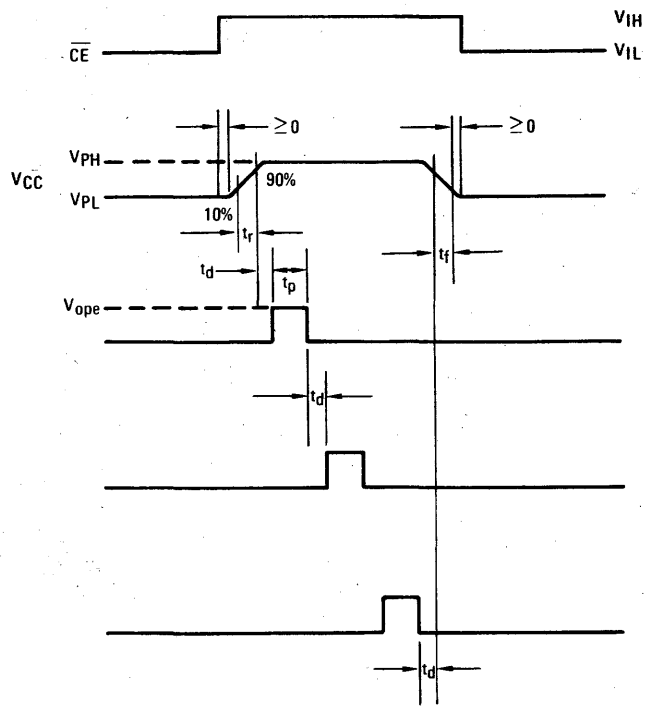


FIGURE 2

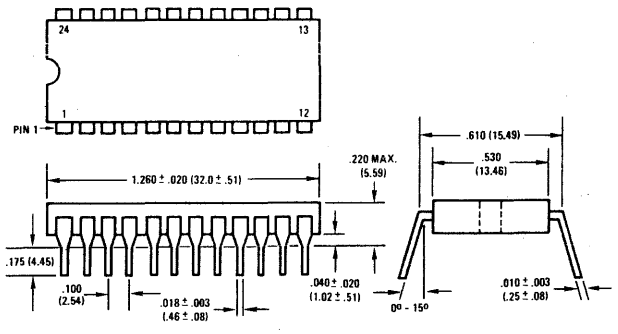
This timing diagram shows device terminal conditions. Each positive going data pulse at the terminal blows the corresponding bit, resulting in a low output for that bit. Therefore, a low input at the DATA-X points of the Figure 1 circuit results in a permanent low output of a bit.

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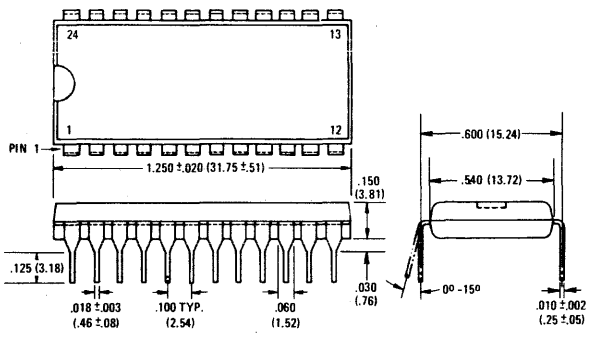
Packaging

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

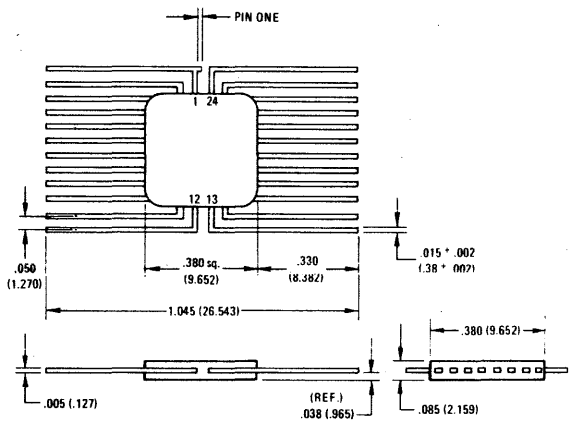
24 LEAD CERDIP
HM1-7608



24 LEAD EPOXY D.I.P.
HM3-7608



24 LEAD FLATPACK
HM9-7608



Ordering Information

HM 1 - 76XX - 5

- HARRIS MEMORY
- PACKAGE
  - 1 – Cerdip
  - 3 – Epoxy
  - 9 – Flat Pack
- DEVICE NUMBER
- TEMPERATURE
  - 2 -55°C to 125°C
  - 5 0°C to 75°C
  - 8 Dash 8 Program MIL-STD-883 Class B

PACKAGE AVAILABILITY

TEMPERATURE	CERDIP	EPOXY	FLAT PACK
-2	YES	NO	YES
-5	YES	YES	NO
-8	YES	NO	YES

NOTICE: Harris Semiconductor's products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders.

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PRODUCTS DIVISION

Preliminary

HM-7683

1K x 8 PROM

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS
- SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-7683 is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 1K word by 8 bit/word format and is available in a 20 pin D.I.P. (ceramic or epoxy) and a 20 pin flatpack.

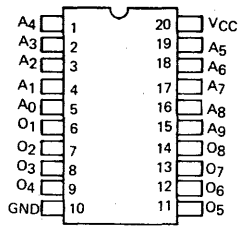
All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position. The HM-7683 has three state outputs.

Nichrome fuse technology is used on this and all other Harris Bipolar PROM's.

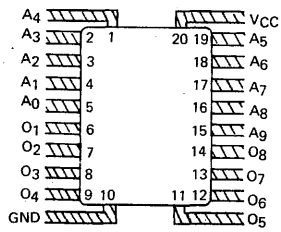
The HM-7683 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

Pinouts

TOP VIEW – D.I.P.



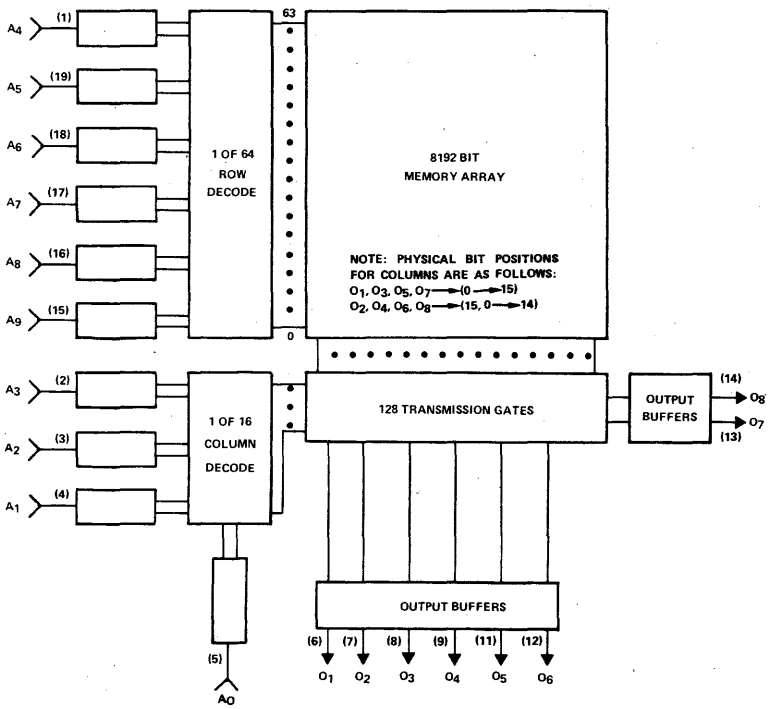
TOP VIEW – FLATPACK



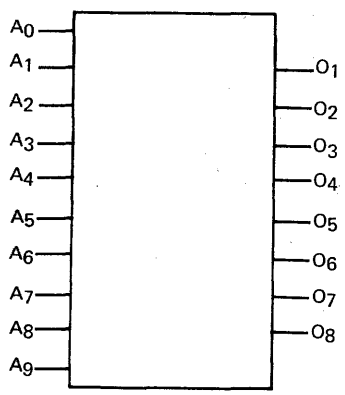
PIN NAMES

$A_0 - A_9$	ADDRESS OUTPUTS
$O_1 - O_8$	DATA OUTPUTS

Functional Diagram



Logic Symbol



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Refer to Harris Sales Offices for additional specifications.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION

HM-7684/85

Preliminary 2K x 4 PROM

HM-7684 - Open Collector Outputs
HM-7685 - "Three State" Outputs

Features

- 80ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND A CHIP ENABLE INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7684/85 is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 2K word by 4 bit/word format with open collector (HM-7684) or "three state" (HM-7685) outputs. These PROM's are available in an 18 pin D.I.P. (ceramic or epoxy) and an 18 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

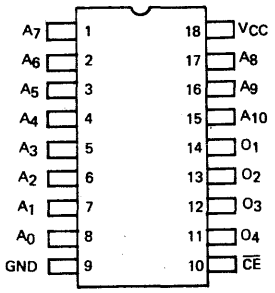
Nichrome fuse technology is used on this and all other Harris Bipolar PROM's.

The HM-7684/85 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

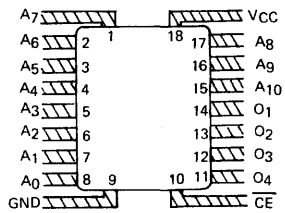
There is a chip enable input on the HM-7684/85. $\overline{CE}$ low enables the chip.

Pinouts

TOP VIEW – D.I.P.



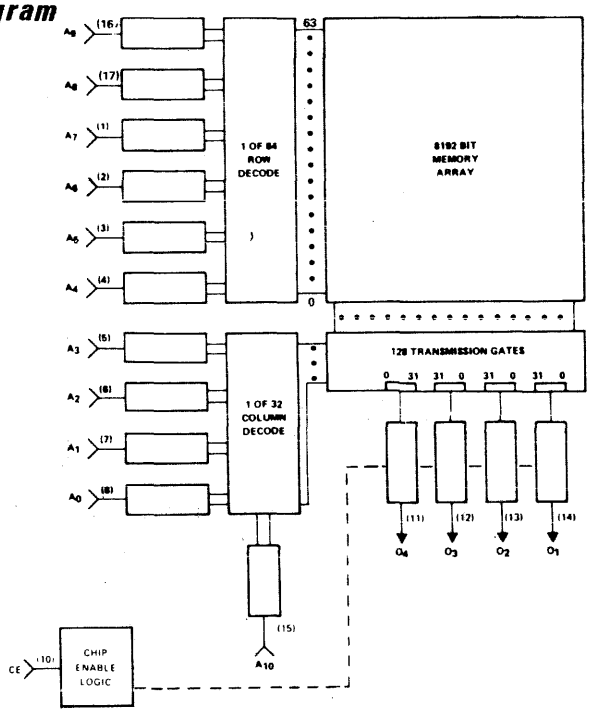
TOP VIEW – FLATPACK



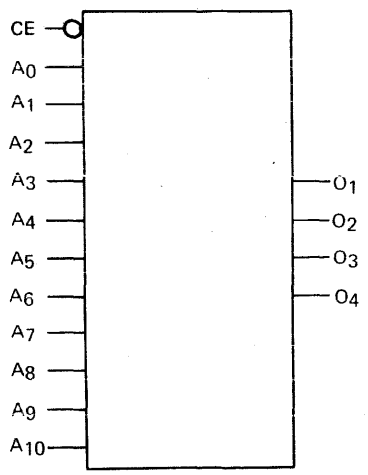
PIN NAMES

$A_0 - A_{10}$	ADDRESS INPUTS
$O_1 - O_2$	DATA OUTPUTS
$\overline{CE}$	CHIP ENABLE INPUT

Functional Diagram



Logic Symbol



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HARRIS SEMICONDUCTOR PRODUCTS DIVISION

HM-7684P/85P

Preliminary

2K x 4 PROM

HM-7684P - Open Collector Outputs
HM-7685P - "Three State" Outputs

Features

- 80ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND A POWER DOWN INPUT.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7684P/85P is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 2K word by 4 bit/word format with open collector (HM-7684P) or "three state" (HM-7685P) outputs. These PROM's are available in an 18 pin D.I.P. (ceramic or epoxy) and an 18 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

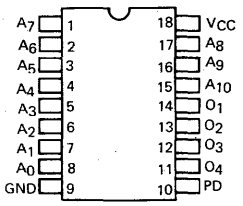
Nichrome fuse technology is used on these and all other Harris Bipolar PROM's.

The HM-7684P/85P contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

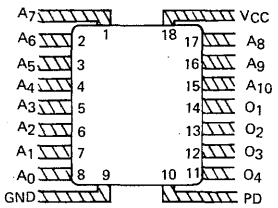
There is a power down input on the HM-7684P/85P which is similar to a chip enable. The chip is enabled or disabled using the power down input where a disabled chip dissipates 30% of nominal power and the outputs go to a high impedance state. The chip is powered up (enabled) when PD is low.

Pinout

TOP VIEW – D.I.P



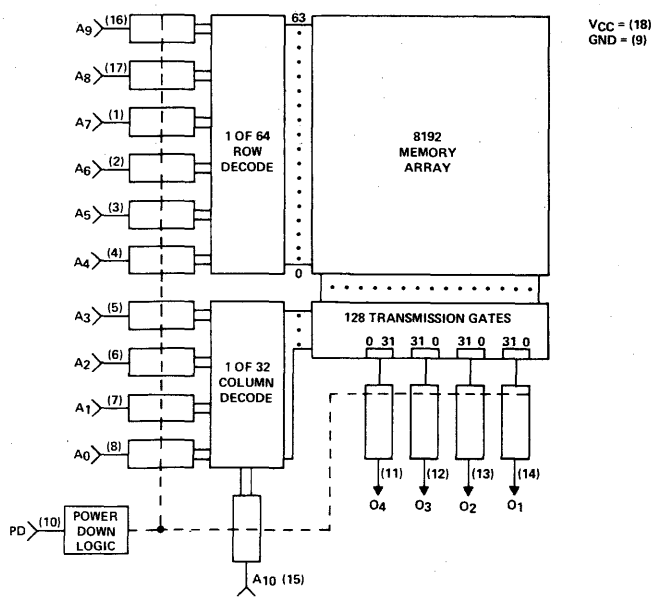
TOP VIEW – FLATPACK



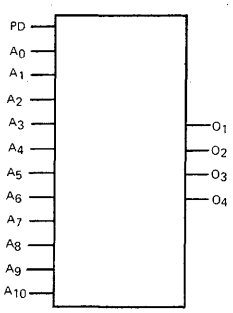
PIN NAMES

$A_0 - A_{10}$	ADDRESS INPUTS
$O_1 - O_4$	DATA OUTPUTS
PD	POWER DOWN INPUT

Functional Diagram



Logic Symbol



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Refer to Harris Sales Offices for additional specifications.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION

Preliminary

HM-7686/87

2K x 4 PROM

HM-7686 - Open Collector Outputs
HM-7687 - "Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND THREE CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-7686/87 are fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROMs in a 2K word by 4 bit/word format with open collector (HM-7686) or "three state" (HM-7687) outputs. These PROM's are available in a 20 pin D.I.P. (ceramic or epoxy) and a 20 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

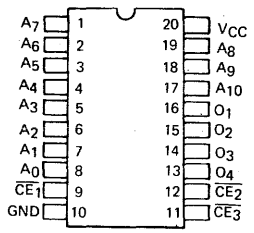
Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7686/87 contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

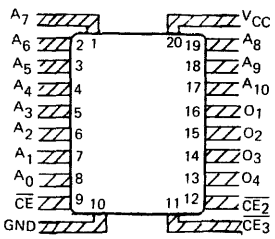
There are three chip enable inputs on the HM-7686/87. $\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$ low enables the chip.

Pinouts

TOP VIEW – D.I.P.



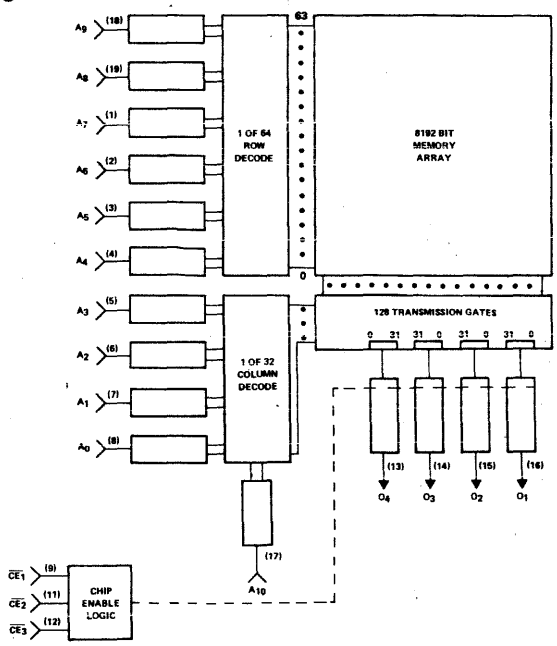
TOP VIEW – FLATPACK



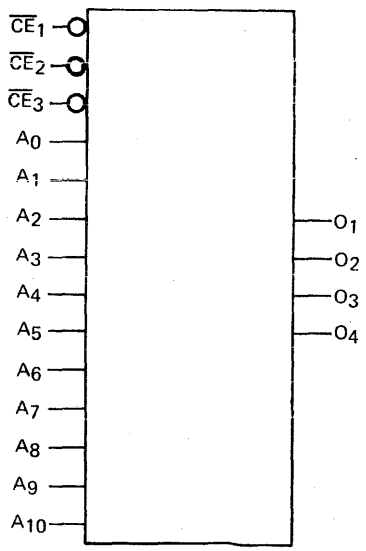
PIN NAMES

$A_0 - A_{10}$	ADDRESS INPUTS
$O_1 - O_4$	DATA OUTPUTS
$\overline{CE}_1, \overline{CE}_2, \overline{CE}_3$	CHIP ENABLE INPUTS

Functional Diagram



Logic Symbol



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HARRIS SEMICONDUCTOR PRODUCTS DIVISION

HM-7686R/87R

Preliminary 2K x 4 PROM

HM-7686R - Open Collector Outputs
HM-7687R - "Three State" Outputs

Features

- 80ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND TWO CHIP ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.
- LATCHED OUTPUTS

Description

The HM-7686R/87R is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 2K word by 4 bit/word format with open collector (HM-7686R) or "three state" (HM-7687R) outputs. These PROM's are available in a 20 pin D.I.P. (ceramic or epoxy) and a 20 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROM's.

The HM-7686R/87R contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

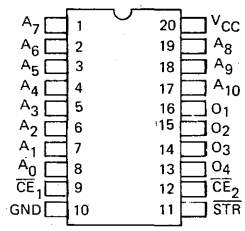
There are two chip enable inputs on the HM-7686R/87R. $\overline{CE}_1$, $\overline{CE}_2$ low enables the chip.

The HM-7686R/87R is operated in the Transparent Read mode by holding the strobe input low throughout the read operation. This is the normal read mode where the two chip enable inputs will control the outputs.

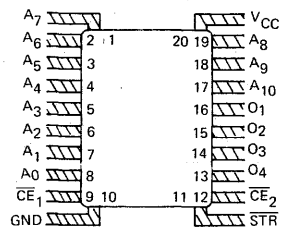
In Latched Read mode, bringing the strobe input high will latch the outputs and chip enable inputs. If the device is disabled when the strobe input goes high, the outputs will be latched in the high impedance state. If the device is in the latched mode the strobe input must be brought low to allow the outputs to respond to new address or chip enable conditions.

Pinout

TOP VIEW – D.I.P.



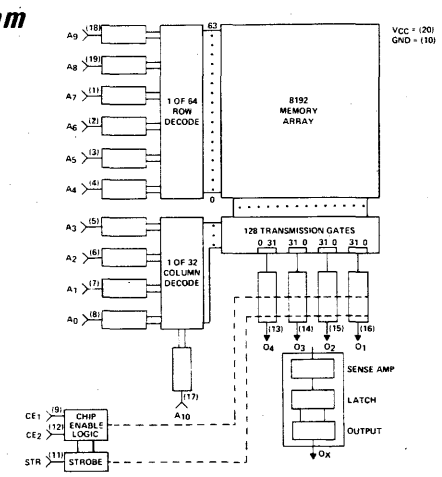
TOP VIEW – FLATPACK



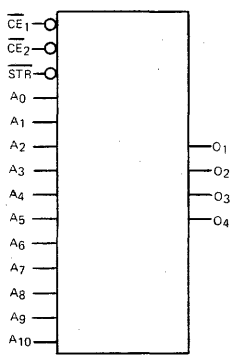
PIN NAMES

$A_0 - A_{10}$	ADDRESS INPUTS
$O_1 - O_4$	DATA OUTPUTS
$\overline{CE}_1 - \overline{CE}_2$	CHIP ENABLE INPUTS
$\overline{STR}$	STROBE INPUT

Functional Diagram



Logic Symbol



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Refer to Harris Sales Offices for additional specifications.

HM-7686P/87P

Preliminary — **2K x 4 PROM**

HM-7686P - Open Collector Outputs
HM-7687P - "Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND THREE POWER DOWN INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-7686P/87P are fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROMs in a 2K word by 4 bit/word format with open collector (HM-7686P) or "three state" (HM-7687P) outputs. These PROMs are available in a 20 pin D.I.P. (ceramic or epoxy) and a 20 pin flatpack.

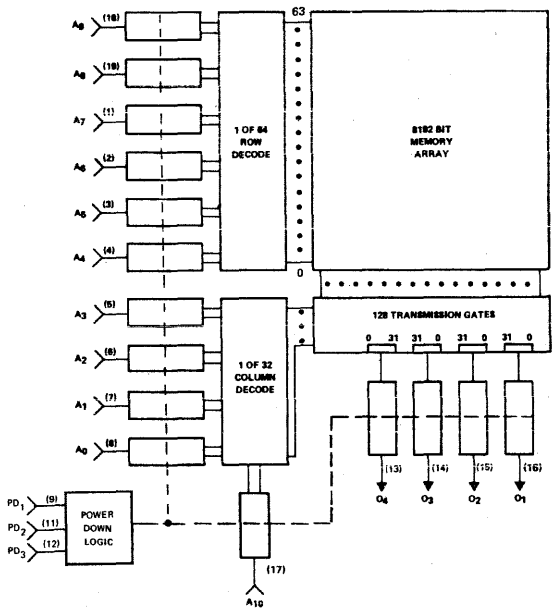
All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7686P/87P contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

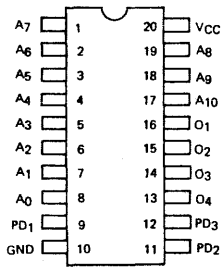
There are three power down inputs on the HM-7686P/87P which are similar to chip enables. The chip is enabled or disabled using the power down inputs where a disabled chip dissipates 30% of nominal power and the outputs go to a high impedance state. The chip is powered up (enabled) when PD_1, PD_2 and PD_3 are low.

Functional Diagram

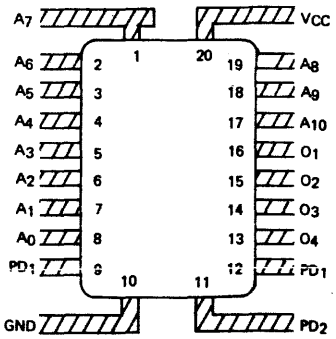


Pinout

TOP VIEW – D.I.P.



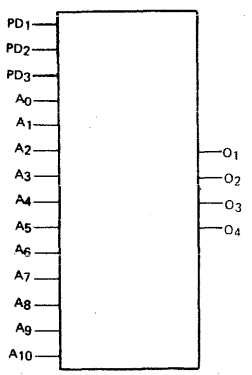
TOP VIEW – FLATPACK



PIN NAMES

$A_0 - A_{10}$	ADDRESS INPUTS
$O_1 - O_4$	DATA OUTPUTS
PD_1, PD_2, PD_3	POWER DOWN INPUTS

Logic Symbol



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HARRIS SEMICONDUCTOR PRODUCTS DIVISION

HM-7686RP/87RP

Preliminary

2K x 4 PROM

HM-7686RP - Open Collector Outputs
HM-7687RP - "Three State" Outputs

Features

- 80ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND A CHIP ENABLE INPUT.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.
- LATCHED OUTPUTS.
- A POWER DOWN INPUT ALLOWING 70% REDUCTION IN NOMINAL POWER DISSIPATION.

Description

The HM-7686RP/87RP are fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM's in a 2K word by 4 bit/word format with open collector (HM-7686RP) or "three state " (HM-7687RP) outputs. These PROM's are available in a 20 pin D.I.P. (ceramic or epoxy) and a 20 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROM's.

The HM-7686RP/87RP contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There is a chip enable input on the HM-7686RP/87RP. $\overline{CE}$ low enables the device.

There is a power down input on this device. A powered down chip has a 70% reduction in power dissipation if the outputs are not latched and a 50% reduction in power if the outputs are latched.

The HM-7686RP/87RP is operated in the Transparent Read mode by holding the strobe input low and the PD input low throughout the read operation. This is the normal read mode where the chip enable and the power down input will control the outputs.

In Latched Read mode, bringing the strobe input high will latch the outputs and the chip enable inputs. However, the power down input is independent of the latched function and can be changed while in the latched mode. If the device is disabled when the strobe input goes high, the outputs will be latched in the high impedance state. If the device is in the latched mode the strobe input must be brought low to allow the outputs to respond to new address or chip enable conditions.

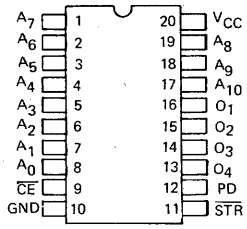
The following is a summary of the functional dependencies of the operating modes:

1. Chip enabled, transparent, power up – normal mode where the power down input is effectively a chip enable.
2. Chip enabled, latched, power up – this is normal latched mode where the output remains latched regardless of address and chip enable switching.
3. Chip enabled, latched, power down – this is the powered down latched mode where the output data remains latched while power is reduced to 50% of its normal value. If the latch strobe changes state while in this mode, the outputs will go to a high impedance state and power will reduce to 30% of nominal power.
4. Chip disabled, transparent, power down – this is the normal powered down mode where the outputs are in a high impedance state and the power is reduced to 30% of the nominal power.

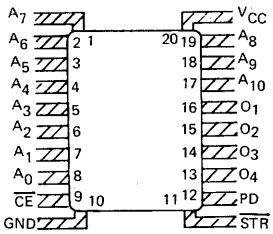
To the right is a table to clarify the operational interdependencies.

Pinout

TOP VIEW – D.I.P.



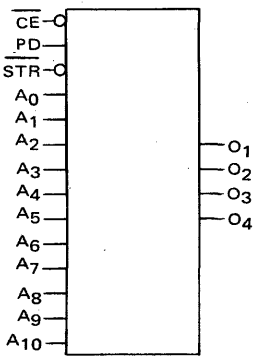
TOP VIEW – FLATPACK



PIN NAMES

$A_0 - A_{10}$	ADDRESS INPUT
$O_1 - O_4$	DATA OUTPUTS
$\overline{PD}$	POWER DOWN INPUT
$\overline{STR}$	STROBE INPUT

Logic Symbol



TRUTH TABLE for HM - 7686RP/87RP

PD	$\overline{STR}$	$\overline{CE}$	OUTPUTS	POWER
1	1	0	LATCHED DATA	50%
1	1	1	LATCHED 3 - STATE	50%
1	0	0	UNLATCHED 3 - STATE	30%
1	0	1	UNLATCHED 3 - STATE	30%
0	1	0	LATCHED DATA	100%
0	1	1	LATCHED 3 - STATE	100%
0	0	0	UNLATCHED DATA	100%
0	0	1	UNLATCHED 3 - STATE	100%

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PROMS

Generic Family

FEATURES

- Largest generic PROM family available
- Reliability proven nichrome fuzes (qualified for MIL-M-38510)
- Drop in compatible ROMs
- PNP inputs for low input current
- Compatible pin configurations for upward expansion
- 4-bit-wide and 8-bit-wide for byte oriented applications
- High speed for microprogrammed applications
- Other applications include:
  - Microprocessor program store
  - Look up table
  - Character generator
  - Random logic
  - Code converter

DESCRIPTION

The 53/6300-series generic PROM family offers the widest selection of sizes and organizations available in the industry. The 4-bit-wide PROMs range from 256x4 to 1024x4 and feature upward/downward pin out compatibility in the space saving 16 and 18 pin packages. The 8-bit-wide PROMs range from 32x8 to 1024x8 in a wide selection of package sizes. All PROMs have the same programming specifications allowing a single generic programmer.

The family features low input current PNP inputs, full Schottky clamping and Three-state and open collector outputs. The nichrome fuzes store a logical high and are programmed to the low state.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

PROM SELECTION GUIDE

MEMORY		PACKAGE		DEVICE TYPE		INTERCHANGEABLE ROM		OUTPUT
Organization	Size	Pins	Type*	0°C to +75°C	-55°C to +125°C	0°C to +75°C	-55°C to +125°C	
256x4	1024	16	J, N, F	6300-1	5300-1	6200-1	5200-1	OC
				6301-1	5301-1	6201-1	5201-1	TS
512x4	2048	16	J, N, F	6305-1	5305-1	6205-1	5205-1	OC
				6306-1	5306-1	6206-1	5206-1	TS
1024x4	4096	18	J, N, F	6350-1	5350-1	6250-1	5250-1	OC
				6351-1	5351-1	6251-1	5251-1	TS
				6352-1	5352-1	6252-1	5252-1	OC
				6353-1	5353-1	6253-1	5253-1	TS
32x8	256	16	J, N, F	6330-1	5330-1	6230-1	5230-1	OC
				6331-1	5331-1	6231-1	5231-1	TS
256x8	2048	20	J, N	6308-1	5308-1	–	–	OC
				6309-1	5309-1	–	–	TS
		24	J, N, F	6335-1	5335-1	6235	5235	OC
				6336-1	5336-1	6236	5236	TS
512x8	4096	24	J, N, F	6340-1	5340-1	6240-1	5240-1	OC
				6341-1	5341-1	6241-1	5241-1	TS
		20	J, N	6348-1	5348-1	–	–	OC
				6349-1	5349-1	–	–	TS
1024x8	8192	24	J, N, F	6380-1	5380-1	6280-1	5280-1	OC
				6381-1	5381-1	6281-1	5281-1	TS
				6384-1	5384-1	6284-1	5284-1	OC
				6385-1	5385-1	6285-1	5285-1	TS
1024x8	8192	22	J	6386-1	5386-1	6286-1	5286-1	OC
				6387-1	5387-1	6287-1	5287-1	TS

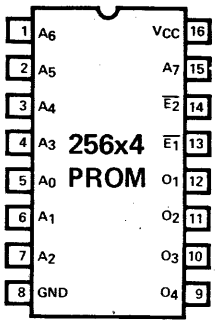
* Package Types: N is Plastic DIP, J is Ceramic DIP and F is Flat Pak

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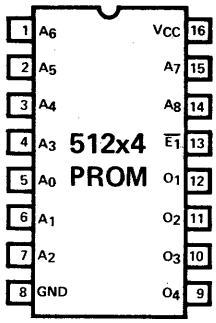
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PIN OUTS

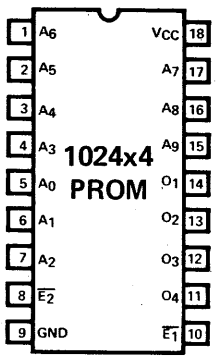
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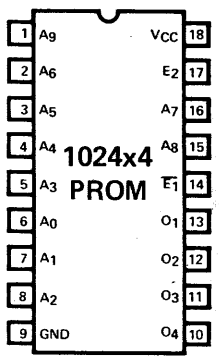
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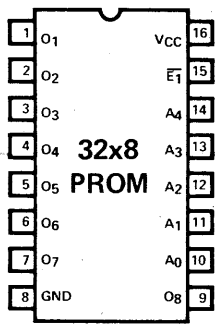
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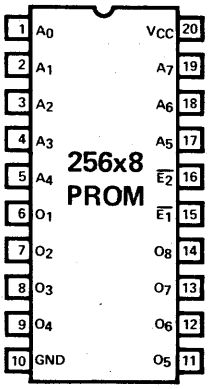
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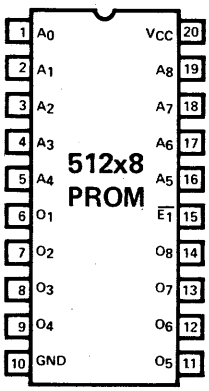
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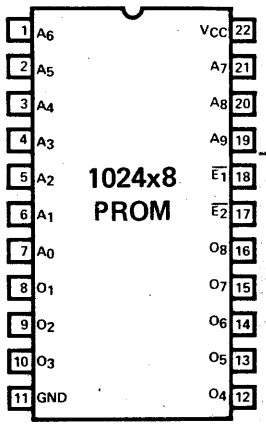
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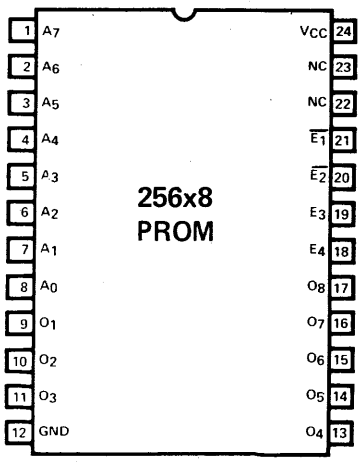
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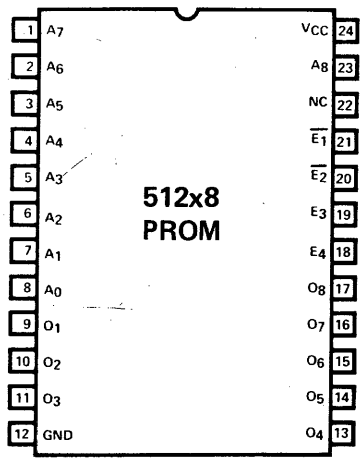
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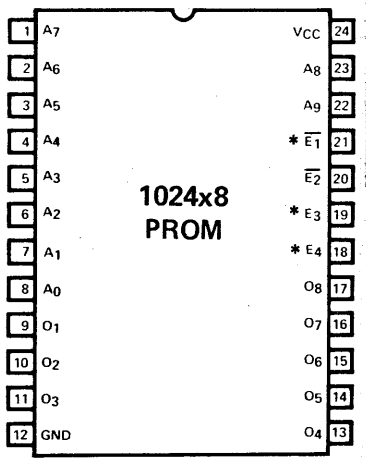
53/6335-1
53/6336-1



53/6340-1
53/6341-1



53/6380-1, *53/6384-1
53/6381-1, *53/6385-1



*NO CONNECTION

NOTE:
Pin assignments for ceramic (J package), plastic (N package) and flat pack (F package) are the same.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . -0.5V to +7.0V
Input Voltage . . . . . -1.5V to +5.5V
Input Current . . . . . -20 mA to +5 mA
Output Current . . . . . -100 mA to +100 mA
Storage Temperature Range . . . . . -65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		53' (Military)			63' (Commercial)			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply Voltage		4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High Level Output Current				-2.0			-3.2	mA
I_{OL}	Low Level Output Current	'00, '01, '05, '06, '08, '09 '40, '41, '50, '51, '52, '53			12			16	mA
		'30, '31, '35, '36, '80, '81 '84, '85, '86, '87			8			12	mA
T_A	Operating Free Air Temperature		-55	25	125	0	25	75	°C

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High Level Input Voltage				2.0			V
V_{IL}	Low Level Input Voltage						0.8	V
V_{IC}	Input Clamp Voltage		V_{CC} = Min, I_I = -18mA			-1.0	-1.5	V
V_{OL}	Low Level Output Voltage		V_{CC} = Min, I_{OL} = Max				.45	V
I_I	Maximum Input Current		V_{CC} = Max, V_I = 4.5V (Program Pin) V_I = 5.5V (Other Inputs)				1.0	mA
I_{IH}	High Level Input Current		V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current		V_{CC} = Max, V_I = 0.45V				-250	μA
C_I	Input Capacitance		V_{CC} = 5.0V, T_A = 25°C, f = 1 MHz	V_I = 2.0V		7		pF
C_O	Output Capacitance			V_O = 2.0V		8		pF
I_{CC}	Supply Current	'30, '31	V_{CC} = Max, All inputs grounded, All outputs open				125	mA
		'00, '01, '05, '06					130	
		'08, '09, '48, '49					155	
		'35, '36, '40, '41					170	
		'50, '51, '52, '53					175	
		'80, '81, '84, '85, '86, '87					180	

OPEN COLLECTOR OUTPUT CURRENT

I_{CEX}	Output Leakage Current	V_{CC} = Max, V_O = 2.4V		100	μA

THREE STATE OUTPUT ONLY

V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	2.4	3.2	V
I_{HZ}	High Level OFF State Output Current	V_{CC} = Max, V_O = 2.4V		100	μA
I_{LZ}	Low Level OFF State Output Current	V_{CC} = Max, V_O = 0.5V		-100	μA
I_{OS}	Output Short Circuit Current	V_{CC} = 5.0V, V_O = 0V	-20	-50 -90	mA

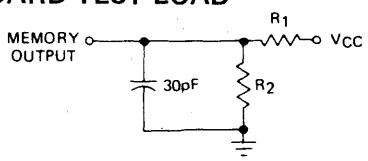
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SWITCHING CHARACTERISTICS

Over recommended ranges of T_A and V_{CC} (unless otherwise noted)

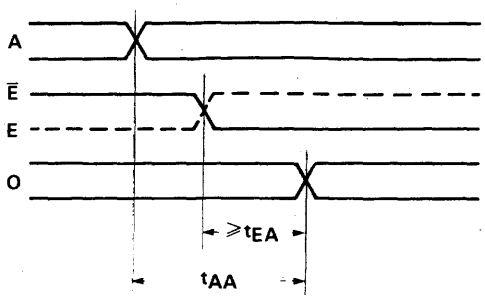
DEVICE TYPE	CONDITIONS (See standard test load)		t_{AA} (ns) ADDRESS ACCESS TIME	t_{EA} (ns) ENABLE ACCESS TIME	t_{ER} (ns) ENABLE RECOVERY TIME
	R_1 (Ω)	R_2 (Ω)	MAX	MAX	MAX
6300-1, 6301-1	300	600	55	30	30
5300-1, 5301-1	375	750	75	30	30
6305-1, 6306-1	300	600	60	30	30
5305-1, 5306-1	375	750	75	40	40
6308-1, 6309-1	375	750	70	30	30
5308-1, 5309-1	560	1120	80	40	40
6330-1, 6331-1	375	750	50	30	25
5330-1, 5331-1	560	1120	60	30	25
6335-1, 6336-1	375	750	90	40	40
5335-1, 5336-1	560	1120	120	40	40
6340-1, 6341-1	375	750	70	30	30
5340-1, 5341-1	560	1120	80	40	40
6348-1, 6349-1	375	750	70	30	30
5348-1, 5349-1	560	1120	80	40	40
6350-1, 6351-1	300	600	60	30	30
5350-1, 5351-1	375	750	75	40	40
6352-1, 6353-1	300	600	60	30	30
5352-1, 5353-1	375	750	75	40	40
6380-1, 6381-1	375	750	90	40	40
5380-1, 5381-1	560	1120	125	40	40
6384-1, 6385-1	375	750	90	40	40
5384-1, 5385-1	560	1120	125	40	40
6386-1, 6387-1	375	750	90	40	40
5386-1, 5387-1	560	1120	125	40	40

STANDARD TEST LOAD

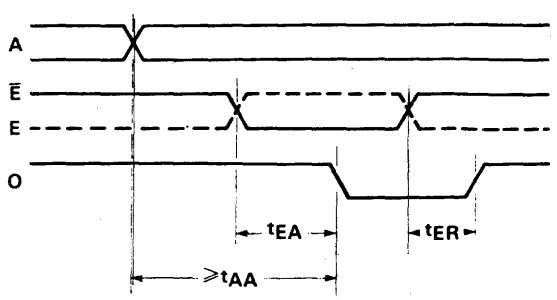


Input Pulse Amplitude 3.0V
Input Rise and Fall Times
5ns from 1.0V to 2.0V
Measurements Made at 1.5V

DEFINITION OF WAVEFORMS



ADDRESS ACCESS TIME



ENABLE ACCESS TIME AND RECOVERY TIME

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ROMS

Generic Family

FEATURES

- Largest generic ROM family available
- PNP inputs for low input current
- Compatible pin configurations for upward expansion
- 4-bit-wide and 8-bit-wide for byte oriented applications
- High speed for microprogrammed applications
- Other applications include:
  - Microprocessor program store
  - Look up table
  - Character generator
  - Random logic
  - Code convertor

DESCRIPTION

The 52/6200-series generic ROM family offers the widest selection of sizes and organizations available in the industry. The 4-bit-wide ROMs range from 256x4 to 1024x4 and feature upward/downward pinout compatibility in the space saving 16 and 18 pin packages. The 8-bit-wide ROMs range from 32x8 to 2048x8 in a wide selection of package sizes.

The family features low input current PNP inputs, full Schottky clamping and three-state and open collector outputs.

The 62 series is specified for operation over the commercial temperature and voltage range. The 52 series is specified for the military ranges.

ROM SELECTION GUIDE

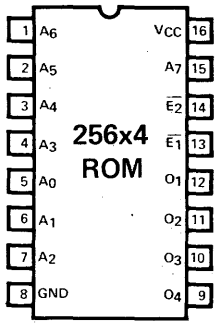
MEMORY		PACKAGE		DEVICE TYPE		INTERCHANGEABLE PROM		OUTPUT
Organization	Size	Pins	Type	0°C to +75°C	-55°C to +125°C	0°C to +75°C	-55°C to +125°C	
256x4	1024	16	J, N, F	6200-1	5200-1	6300-1	5300-1	OC
				6201-1	5201-1	6301-1	5301-1	TS
512x4	2048	16	J, N, F	6205-1	5205-1	6305-1	5305-1	OC
				6206-1	5206-1	6306-1	5306-1	TS
1024x4	4096	18	J, N, F	6250-1	5250-1	6350-1	5350-1	OC
				6251-1	5251-1	6351-1	5351-1	TS
				6252-1	5252-1	6352-1	5352-1	OC
				6253-1	5253-1	6353-1	5353-1	TS
256x5	1280	16	J, N, F	6210-1	5210-1	–	–	OC
512x5	2560	18	J, N	6225-1	5225-1	–	–	OC
32x8	256	16	J, N, F	6230-1	5230-1	6330-1	5330-1	OC
				6231-1	5231-1	6331-1	5331-1	TS
256x8	2048	24	J, N, F	6235-1	5235-1	6335-1	5335-1	OC
				6236-1	5236-1	6336-1	5336-1	TS
512x8	4096	24	J, N, F	6240-1	5240-1	6340-1	5340-1	OC
				6241-1	5241-1	6341-1	5341-1	TS
1024x8	8192	24	J, N, F	6280-1	5280-1	6380-1	5380-1	OC
				6281-1	5281-1	6381-1	5381-1	TS
				6280-2	5280-2	–	–	OC
				6281-2	5281-2	–	–	TS
				6282-1	5282-1	–	–	OC
				6283-1	5283-1	–	–	TS
				6284-1	5284-1	6384-1	5384-1	OC
				6285-1	5285-1	6385-1	5385-1	TS
		22	J, N	6286-1	5286-1	6386-1	5386-1	OC
				6287-1	5287-1	6387-1	5387-1	TS
				6286-2	5286-2	–	–	OC
				6287-2	5287-2	–	–	TS
		20	J, N	6289-1	5289-1	–	–	Active
				6289-2	5289-2	–	–	Pullup
2048x8	16384	24	J, N, F	6275-1	5275-1	–	–	OC
				6276-1	5276-1	–	–	TS
1024x9	9216	24	J, N, F	6260-1	5260-1	–	–	OC
				6261-1	5261-1	–	–	TS
1024x10	10240	24	J, N, F	6255-1	5255-1	–	–	OC
				6256-1	5256-1	–	–	TS

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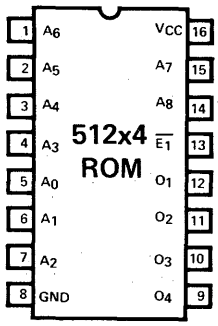
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PIN OUTS

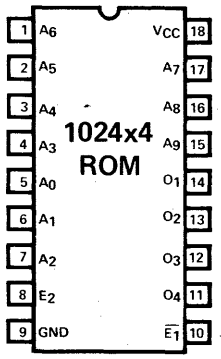
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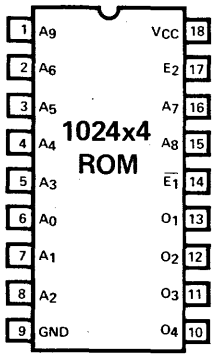
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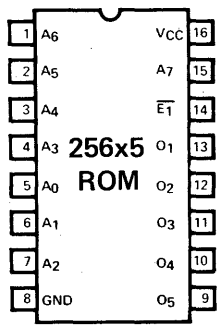
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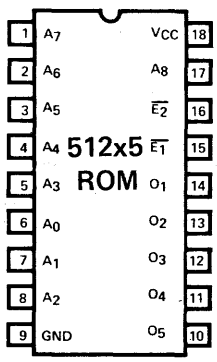
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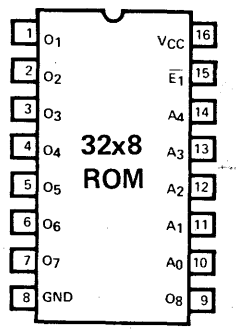
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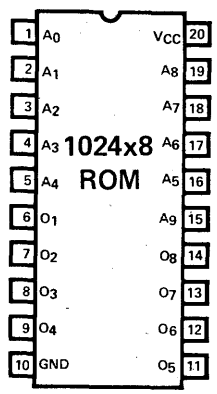
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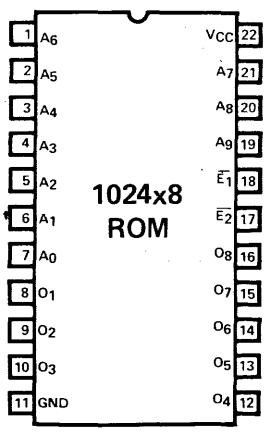
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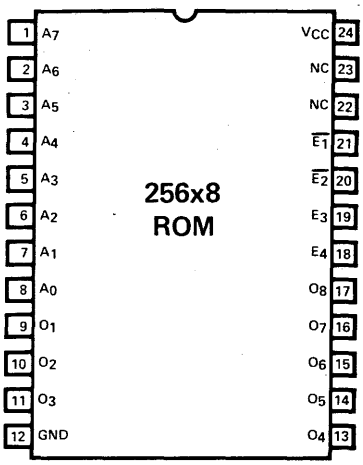
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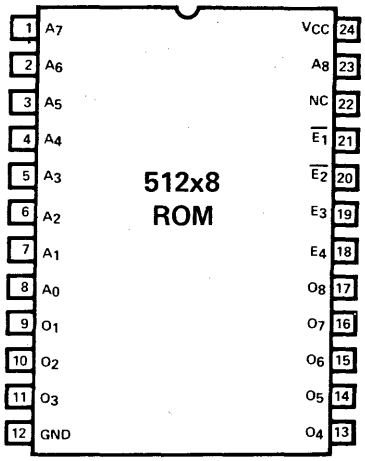
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52/6236-1



52/6240-1
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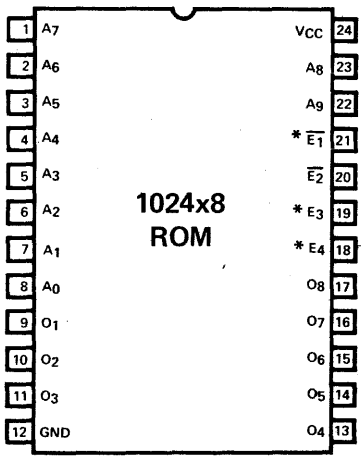


MEMORY MMI

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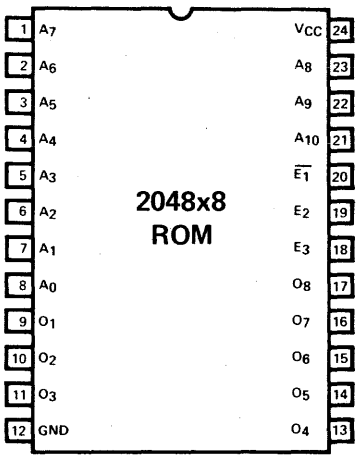
PIN OUTS

52/6280-1 52/6280-2
52/6281-1 52/6281-2
*52/6284-1 **52/6282-1
*52/6285-1 **52/6283-1

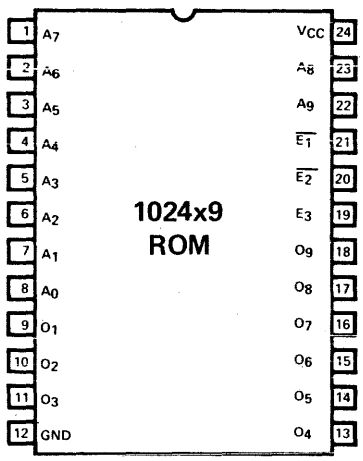


*NO CONNECTION
**"OR" ENABLE

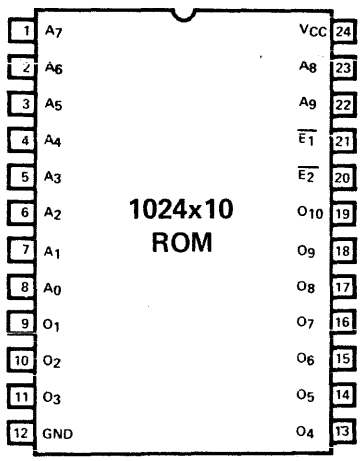
52/6275-1
52/6276-1



52/6260-1
52/6261-1



52/6255-1
52/6256-1



NOTE:
Pin assignments for ceramic (J package), plastic (N package) and flat pack (F package) are the same.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . -0.5V to +7.0V
Input Voltage . . . . . -1.5V to +5.5V
Input Current . . . . . -20 mA to +5 mA
Output Current . . . . . -100 mA to +100 mA
Storage Temperature Range . . . . . -65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		53' (Military)			63' (Commercial)			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply Voltage		4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High Level Output Current				-1.0			-2.0	mA
I_{OL}	Low Level Operating Current	'05, '06, '50, '51, '52, '53			16			12	mA
		'00, '01, '10, '25			15			10	
		'30, '31			12			8	
		'35, '36, '40, '41, '80, '81, '82, '83, '84, '85, '86, '87, '89, '75, '76			10			8	
		'55, '56, '60, '61			6			6	
T_A	Operating Free Air Temperature		-55	25	125	0	25	75	°C

ELECTRICAL CHARACTERISTICS

Over recommended operating free air temperature range (unless otherwise noted)

SYMBOL	PARAMETER		CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High Level Input Voltage				2.0			V
V_{IL}	Low Level Input Voltage						0.8	V
V_{IC}	Input Clamp Voltage		V_{CC} = Min, I_I = -18mA			-1.0	-1.5	V
V_{OL}	Low Level Output Voltage		V_{CC} = Min, I_{OL} = Max				.45	V
I_I	Maximum Input Current		V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH}	High Level Input Current		V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current		V_{CC} = Max, V_I = 0.45V				-250	μA
C_I	Input Capacitance		V_{CC} = 5.0V, T_A = 25°C, f = 1 MHz	V_I = 2.0V		7		pF
C_O	Output Capacitance			V_O = 2.0V		8		pF
I_{CC}	Supply Current	'00, '01, '30, '31	V_{CC} = Max, All Inputs Grounded, All Outputs Open				125	mA
		'05, '06					130	
		'55, '60					165	
		'10, '25, '35, '40, '41, '80, '82, '84, '86, '89					170	
		'36, '50, '51, '52, '53, '56, '61					175	
		'81, '83, '85, '87					180	
		'75, '76					190	

OPEN COLLECTOR OUTPUT CURRENT

I_{CEX}	Output Leakage Current	V_{CC} = Max, V_O = 2.4V			100	μA

THREE STATE OUTPUT ONLY

V_{OH}	High Level Output Voltage		V_{CC} = Min, I_{OH} = Max	2.4	3.2		V
I_{HZ}	High Level Off State Output Current	8K, 9k, 10k	V_{CC} = Max, V_O = 2.4V			50	μA
		All Others				100	
I_{LZ}	Low Level Off State Output Current	8k, 9k, 10k	V_{CC} = Max, V_O = 0.5V			-50	μA
		All Others				-100	
I_{OS}	Output Short Circuit Current		V_{CC} = 5.0V, V_O = 0V	-20	-50	-90	mA

*I_{CC} on 5200-1, 5201-1 is 130 mA

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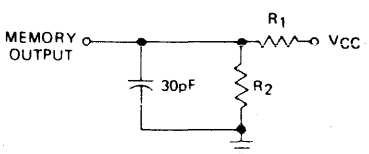
SWITCHING CHARACTERISTICS

Over recommended ranges of T_A and V_{CC} (unless otherwise noted)

DEVICE TYPE	CONDITIONS (SEE STANDARD TEST LOAD) $R_1\Omega$	$R_2\Omega$	t_{AA}(ns) ADDRESS ACCESS TIME MAX	t_{EA}(ns) ENABLE ACCESS TIME MAX	t_{ER}(ns) ENABLE RECOVERY TIME MAX
6200-1, 6201-1	300	600	45	35	35
5200-1, 5201-1	450	900	60	35	35
6205-1, 6206-1	280	560	60	30	30
5205-1, 5206-1	375	750	75	40	40
6210-1	300	600	75*	50*	40*
5210-1	450	900	90*	65*	40*
6225-1	300	600	75*	50*	40*
5225-1	450	900	90*	65*	40*
6230-1, 6231-1	375	750	50	30	25
5230-1, 5231-1	560	1120	60	30	25
6235-1, 6236-1	450	900	100	70	45
5235-1, 5236-1	560	1120	175	90	50
6240-1, 6241-1	450	900	90*	50*	40*
5240-1, 5241-1	560	1120	90*	65*	40*
6250-1, 6251-1	280	560	60	30	30
5250-1, 5251-1	375	750	75	40	40
6252-1, 6253-1	280	560	60	30	30
5252-1, 5253-1	375	750	75	40	40
6255-1, 6256-1	750	1500	100	70	40
5255-1, 5256-1	750	1500	150	80	45
6260-1, 6261-1	750	1500	100	70	40
5260-1, 5261-1	750	1500	150	80	45
6275-1, 6276-1	450	900	110	40	40
5275-1, 5276-1	560	1120	120	50	50
6280-1, 6281-1	450	900	100	70	45
5280-1, 5281-1	560	1120	175	90	50
6280-2, 6281-2	450	900	55	30	30
5280-2, 5281-2	560	1120	75	35	35
6282-1, 6283-1	450	900	100	70	45
5282-1, 5283-1	560	1120	175	90	50
6284-1, 6285-1	450	900	100	70	45
5284-1, 5285-1	560	1120	175	90	50
6286-1, 6287-1	450	900	100	70	45
5286-1, 5287-1	560	1120	175	90	50
6286-2, 6287-2	450	900	55	30	30
5286-2, 5287-2	560	1120	75	35	35
6289-1	450	900	100	70	45
5289-1	560	1120	175	90	50
6289-2	450	900	55	30	30
5289-2	560	1120	75	35	35

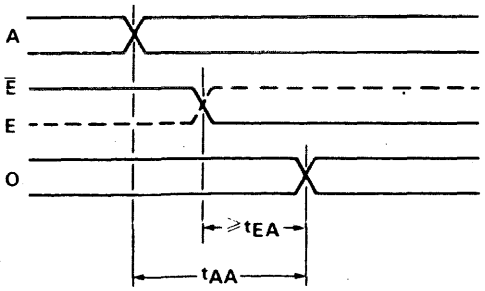
*V_{CC} = +5V, T_A = +25°C

STANDARD TEST LOAD

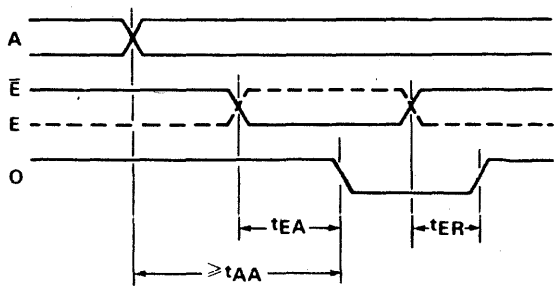


Input Pulse Amplitude 3.0V
Input Rise and Fall Times
5ns from 1.0V to 2.0V
Measurements Made at 1.5V

DEFINITION OF WAVEFORMS



ADDRESS ACCESS TIME



ENABLE ACCESS TIME AND RECOVERY TIME

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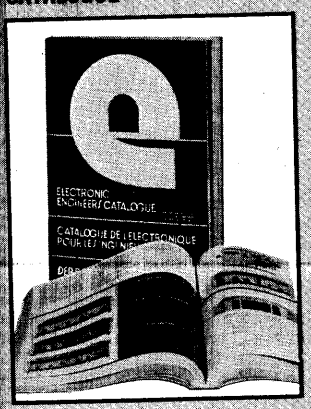
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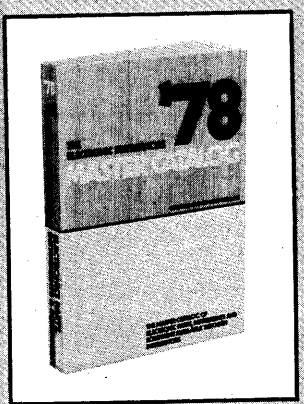
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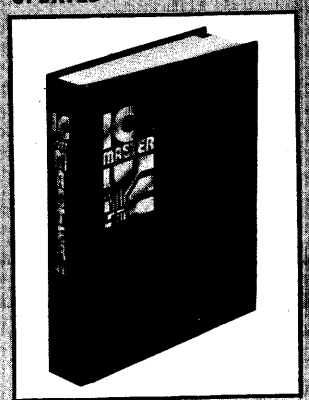


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NATIONAL SEMICONDUCTOR PROM/EPROM CROSS REFERENCE GUIDE

BIPOLAR PROM

SIZE AND ORGANIZATION	OUTPUT	NATIONAL MIL/COM	AMD M = MIL C = COM	FAIRCHILD M = MIL C = COM	HARRIS 2 = MIL 5 = COM	INTEL M = MIL P = COM	INTERSIL M = MIL C = COM	M.M.I. MIL/COM	SIGNETICS S = MIL N = COM	T.I. MIL/COM
256-Bit (32 x 8) 16-Pin	OC	DM54S188/DM74S188*	29750X		HM1-7602-X		IM5600X	5330/6330-1	X82S23	SN54S188/74S188
	TS	DM54S288/DM74S288*	29751X		HM1-7603-X		IM5610X	5331/6331-1	X82S123	SN54S288/74S288
1024-Bit (256 x 4) 16-Pin	OC	DM54S387/DM74S387	29760X	93417X	HM1-7610-X	X3601	IM5603X	5300/6300-1	X82S126	SN54S387/74S387
	TS	DM54S287/DM74S287	29761X	93427X	HM1-7611-X	X3621	IM5623X	5301/6301-1	X82S129	SN54S287/74S287
2048-Bit (512 x 4) 16-Pin	OC	DM54S570/DM74S570	29770X	93436X	HM1-7620-X	X3602	IM5604X	5305/6305-1	X82S130	
	TS	DM54S571/DM74S571	29771X	93446X	HM1-7621-X	X3622	IM5624X	5306/6306-1	X82S131	
4096-Bit (512 x 8) 24-Pin	OC	DM77S295/DM87S295		93438X	HM1-7640-X	X3604	IM5605X	5340/6340-1	X82S140	SN54S474/74S474
	TS	DM77S296/DM87S296		93448X	HM1-7641-X	X3624	IM5625X	5341/6341-1	X82S141	SN54S475/74S475
2048-Bit (256 x 8) 20-Pin	OC	DM54S470/DM74S470						5308/6308-1		SN54S470/74S470
	TS	DM54S471/DM74S471						5309/6309-1		SN54S471/74S471
4096-Bit (512 x 8) 20-Pin	OC	DM54S473/DM74S473*			HM1-7648-X			5348/6348-1	X82S146	SN54S473/74S473
	TS	DM54S472/DM74S472*			HM1-7649-X			5349/6349-1	X82S147	SN54S472/74S472
4096-Bit (1024 x 4) 18-Pin	OC	DM54S572/DM74S572		93452X	HM1-7642-X	X3605		5352/6352-1	X82S136	
	TS	DM54S573/DM74S573		93453X	HM1-7643-X	X3625		5353/6353-1	X82S137	
8192-Bit (1024 x 8) 24-Pin	OC	DM77S229/DM87S229*			HM1-7680-X	X3608		5380/6380-1	X82S180	
	TS	DM77S228/DM87S228*			HM1-7681-X	X3628		5381/6381-1	X82S181	
8192-Bit (2048 x 4) 18-Pin	OC	DM54S672/DM74S672*						63100-1	X82S184	
	TS	DM54S673/DM74S673*						63101-1	X82S185	

Note. All manufacturers' PROMs program differently.
*Future products

See other side also

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NATIONAL SEMICONDUCTOR PROM/EPROM CROSS REFERENCE GUIDE

MOS EPROM

SIZE AND ORGANIZATION	OUTPUT	NATIONAL	AMD	AMI	ELECTRONIC ARRAY	FUJITSU	INTEL	INTERSIL	MOSTEK	MOTOROLA	SIGNETICS	T.I.
8192-Bit (1024 x 8) 24-Pin	TS	MM2708Q	2708		EA2708DC	MB8515	C2708	2708		MCM68708L	N2708	TMS2708JL
2048-Bit (256 x 8) 24-Pin	TS	MM1702AQ/MM1702ALQ	1702A/1702AL				1702A/1702AL		MK3702-3		N1702A/ 1702AL	
4096-Bit (512 x 8) 24-Pin	TS	MM5204/MM4204*		S5204A								

*—55°C to +85°C operating temperature range.

See other side also

NATIONAL SEMICONDUCTOR RAM CROSS REFERENCE GUIDE

BIPOLAR RAMs

OTHER SOURCE	NATIONAL
AMD	
AM27LS0DC	DM74S200
AM27LS00M	DM54S200
AM27LS01C	DM74S206
AM27LS01M	DM54S206
AM27LS02C	DM74LS289
AM27LS02M	DM54LS289
AM72LS03C	DM74LS189
AM27LS03M	DM54LS189
AM27S02C	DM74S289
AM27S02M	DM54S289
AM27S03C	DM74S189
AM27S03M	DM54S189
AM3101	DM7489
AM3101A	DM74S289
AM31L01C	DM74LS289
AM31L01M	DM54LS289
Fairchild	
93403	DM74S289
93411C	DM74S206
93411M	DM54S206
93415AC	DM93415
93415C	DM93415
93421C	DM74S200
93421M	DM54S200
Intel	
3101	DM7489
3101A	DM74S289
M3101	DM5489
M3101A	DM54S289
3106	DM74S200
3106A	DM74S200
3107	DM74S206
3107A	DM74S206
Intersil	
IM5501C	DM7489
IM5501M	DM5489
IM5523C	DM74S200
IM5523M	DM54S200
IM5533C	DM74S206
IM5533M	DM54S206

OTHER SOURCE	NATIONAL
MMI	
5530	DM54S206
5531	DM54S200
5560	DM54S289
5561	DM54S189
6530	DM74S206
6531	DM74S200
6560	DM74S289
6561	DM74S189
L5560	DM54LS289
L5561	DM54LS189
L6560	DM74LS289
L6561	DM74LS189
Signetics	
N8225	DM7489
N82S06	DM74S200
N82S07	DM74S206
N82S10	DM93415
N82S16	DM74S200
N82S17	DM74S206
N82S21	DM86S21
N82S25	DM74S289
N82S116	DM74S200
N82S117	DM74S206
S82S06	DM54S200
S82S07	DM54S206
S82S16	DM54S200
S82S17	DM54S206
S82S25	DM54S289
Texas Instruments	
SN5489	DM5489
SN7489	DM7489
SN54S189	DM54S189
SN54S201	DM54S200
SN54S289	DM54S289
SN54S301	DM54S206
SN74S189	DM74S189
SN74S201	DM74S200
SN74S289	DM74S289
SN74S301	DM74S206
SN74S309	DM93415

MOS RAMs

OTHER SOURCE	NATIONAL
AMD	
AM1101A	MM1101A
AM1101A1	MM1101A1
AM1101A1M	MM4250
AM2101	MM2101A-4*
AM2102	MM2102A-6*
AM2111	MM2111A-6*
AM2112	MM2112A-6*
AM9060C	MM5280-5
AM9060D	MM5280
AM9060E	MM5280
AM9101A	MM2101A-4*
AM9101B	MM2101A*
AM9101C	MM2101A-2*
AM9101D	MM2101A-2*
AM9102	MM2102A-6
AM91L02	MM2102A-6L
AM9102A	MM2102A-4
AM91L02A	MM2102A-4L
AM9102B	MM2102A
AM91L02B	MM2102A-L
AM9102C	MM2102A-2
AM91L02C	MM2102A-2L
AM9102D	MM2102A-2
AM9111A	MM2111A-4*
AM9111B	MM2111A*
AM9111C	MM2111A-2*
AM9111D	MM2111A-2*
AM9112A	MM2112A-4*
AM9112B	MM2112A*
AM9112C	MM2112A-2*
AM9112D	MM2112A-2*
AMS	
AMS6003	MM5262
AMS7270	MM5270
AMS7270-5	MM5270-5
AMS7271	MM5271
AMS7280	MM5280
AMS7280-5	MM5280-5
AMS7281	MM5281

OTHER SOURCE	NATIONAL
Fairchild	
2102	MM2102A-6
21L02	MM2102A-6L
2102-1	MM2102A-4
21L02A	MM2102A-4L
21L02B	MM2102A-L
2102F	MM2102A
2102F2	MM2102A-2
Intel	
1101A	MM1101A
1101A1	MM1101A-1
2101A	MM2101A*
2101A-2	MM2101A-2*
2101A-4	MM2101A-4*
2101	MM2101A-6
2101	MM5269
2101-1	MM2101A-4*
2101-2	MM2101A-6*
2102A	MM2102A
2102A-2	MM2102A-2
2102A-4	MM2102A-4
2102AL	MM2102AL
2102AL-2	MM2102AL-2
2102AL-4	MM2102AL-4
2107B	MM5280
2107B-4	MM5280-5
2111A	MM2111A*
2111A-2	MM2111A-2*
2111A-4	MM2111A-4*
2111	MM2111A-6*
2111-1	MM2111A-4*
2111-2	MM2111A-6*
2112A	MM2112A*
2112A-2	MM2112A-2*
2112A-4	MM2112A-4*
2112	MM2112A-6*
2112-2	MM2112A-6*
MMI	
2170	MM5270
2171	MM5271
2180	MM5280
2181	MM5281

OTHER SOURCE	NATIONAL
Signetics	
21F02	MM2102A
21F02-2	MM2102A-2
21F02-4	MM2102A-4
2102	MM2102A-6
2102-1	MM2102A-4
2102-2	MM2102A-6
21L02-1	MM2102A-L
21L02-3	MM2102A-2L
2501	MM1101A1
2680	MM5280
2680-1	MM5280-5
2613	MM5257
Texas Instruments	
TMS4033	MM2102A-4
TMS4034	MM2102A-6
TMS4035	MM2102A-6
TMS4039	MM2101A-6
TMS4039-1	MM2101A-6
TMS4039-2	MM2101A-4
TMS4042	MM2111A-6
TMS4042-1	MM2111A-6
TMS4042-2	MM2101A-4
TMS4043	MM2112A-6
TMS4043-1	MM2112A-6
TMS4043-2	MM2112A-4
TMS4060	MM5280-5
TMS4060-1	MM5280
TMS4060-2	MM5280

CMOS RAMs

OTHER SOURCE	NATIONAL
Intersil	
IM6551	MM74C920
IM6508	MM74C929
IM6518	MM74C930

*Available 4th quarter 1977
All parts are pin compatible. Check National data sheets for specification details.

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National Semiconductor

PROM programming procedure

These parts are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical "0") for all addresses. In order to generate a high level on the outputs, the part must be programmed. Information on available programming equipment may be obtained from National. However, if it is desired to build your own programmer, the following conditions must be observed.

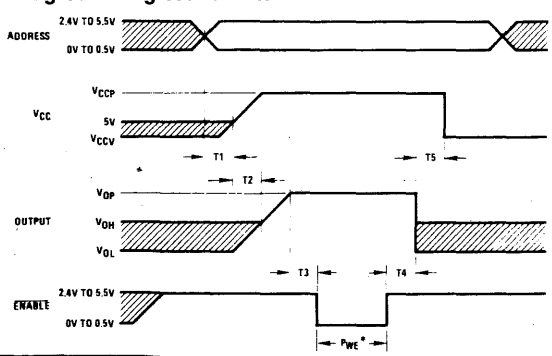
1. Programming should be attempted only at temperatures between 15°C and 30°C.
2. Addresses and chip enable pins must be driven from normal TTL logic levels during both programming and verification.
3. Programming will occur at a selected address when V_{CC} is held at 10.5V, the appropriate output is held at 10.5V and the chip is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedure must be followed:
   a) Select the desired word by applying a high or low level to the appropriate address inputs. Disable the chip by applying a high level to one or both enable inputs.
   b) Increase V_{CC} to 10.5V ±0.5V with the rate of increase being between 1.0 and 10.0V/μs. Since V_{CC} supplies the current to program the fuse as well as the I_{CC} of the device at programming voltage, it must be capable of supplying 400 mA at 11.0V.
   c) Select the output where a high level is desired by raising that output voltage to 10.5V ±0.5V. Limit the rate of increase to a value between 1.0 and 10.0V/μs. This voltage change may occur simultaneously with the increase in V_{CC} but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or tied to a high impedance source of at least 20 kΩ. (Remember that the outputs of the device are still disabled at this time because the chip enables are high.)
   d) Enable the device by taking both chip enables to a low level. This is done with a pulse of 10μs. The 10μs duration refers to the time that the circuit is enabled. Normal input levels are used and rise and fall times are not critical.
   e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0V ±0.2V. Verification at a V_{CC} level of 4.0V will guarantee proper output states over the V_{CC} and temperature range of the programmed part. The chip must be enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c and d must be repeated 10 times or until verification that the bit has programmed.
   f) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.
   g) Repeat steps a through f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at programming voltage must be limited to a maximum of 25%. This is necessary to minimize chip junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Note: Since only an enabled chip is programmed, it is possible to program these parts at the board level if all programming parameters are complied with.

Programming Parameters Do not test or you may program the device.

PARAMETERS		CONDITIONS	MIN	RECOMMENDED VALUE	MAX	UNITS
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} During Programming	V_{CC} = 11V			400	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	V_{OUT} = 11V			20	mA
t_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCV}	Required V_{CC} for Verification		3.8	4.0	4.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Programming Waveforms



T1 = 100 ns min
T2 = 5μs min (T2 may be ≥ 0 if V_{CCP} rises at the same rate or faster than V_{OP})
T3 = 100 ns min
T4 = 100 ns min
T5 = 100 ns min

*P_{WE} is repeated for 5 additional pulses after verification of V_{OH} indicates a bit has programmed

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Preliminary

DM54S188/DM74S188 open-collector 256-bit PROM
DM54S288/DM74S288 TRI-STATE® 256-bit PROM

general description

These Schottky PROM memories are organized in the popular 32 words by 8 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions and are available as ROM's as well as PROM's.

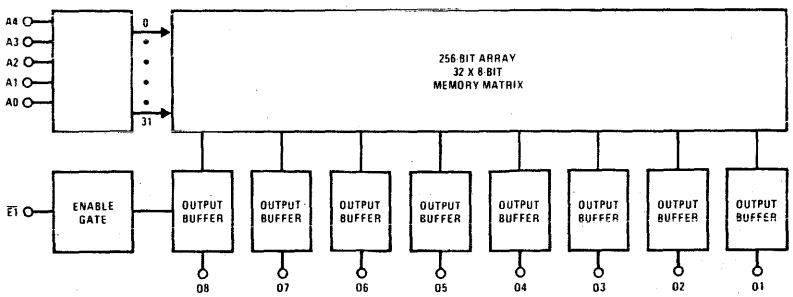
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—30 ns max
  Enable access—20 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming

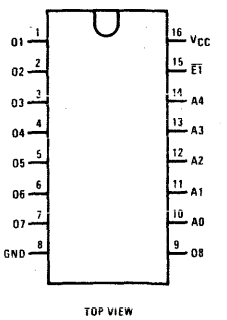
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S188		X	X		N, J
DM74S288		X		X	N, J
DM54S188	X		X		J
DM54S288	X			X	J

block diagram



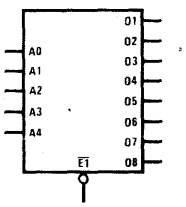
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



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National Semiconductor

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S188, DM54S288	4.5	5.5	V
DM74S188, DM74S288	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S188, DM54S288	−55	+125	°C
DM74S188, DM74S288	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S188, 54S288			DM74S188, 74S288			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.5	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		70	110		70	110	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−30	−60	−100	−30	−60	−100	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S188, 54S288 5V ±10%; −55°C to +125°C			DM74S188, 74S288 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			22	40		22	30	ns
t_{EA}	Enable Access Time			15	30		15	20	ns
t_{ER}	Enable Recovery Time			15	30		15	20	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A7 and A2 (pin 15 and pin 7).

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DM54S287/DM74S287 TRI-STATE® 1024-bit PROM
DM54S387/DM74S387 open-collector 1024-bit PROM

general description

These Schottky memories are organized in the popular 256 words by 4 bits configuration. Two memory enable inputs are provided to control the output states. When both enable inputs are in the low state, the outputs present the contents of the selected word.

If either or both of the enable inputs is raised to a high state, it causes all four outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

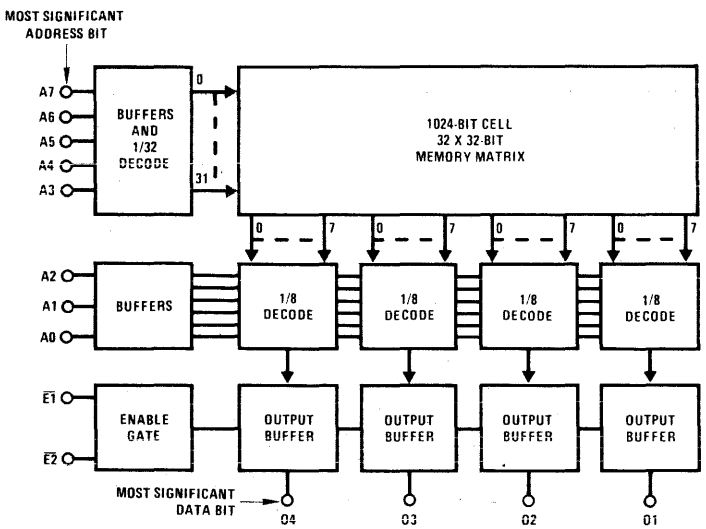
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—50 ns max
  Enable access—25 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM74S187 and DM85S97

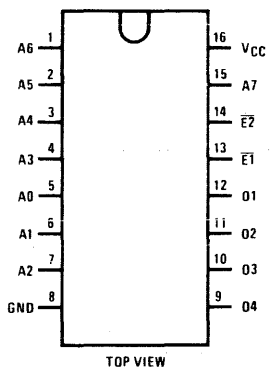
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S387		X	X		N, J
DM74S287		X		X	N, J
DM54S387	X		X		J
DM54S287	X			X	J

block diagram

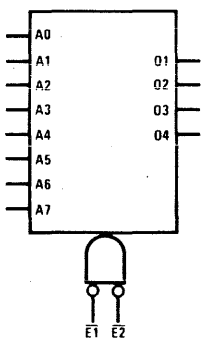


connection diagram

Dual-In-Line Package



logic symbol



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absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S387, DM54S287	4.5	5.5	V
DM74S387, DM74S287	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S387, DM54S287	−55	+125	°C
DM74S387, DM74S287	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S387/287			DM74S387/287			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_F	Input Load Current, All Inputs	V_{CC} = Max, V_F = 0.45V		−80	−250		−80	−250	μA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.7V			25			25	μA
I_{RB}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{RB} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.5	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		80	130		80	130	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 4)	−30	−60	−100	−30	−60	−100	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S387/287 5V ±10%; −55°C to +125°C			DM74S387/287 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time		10	35	60	10	35	50	ns
t_{EA}	Enable Access Time		5	15	30	5	15	25	ns
t_{ER}	Enable Recovery Time		5	15	30	5	15	25	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH} or I_{CEX} on an unprogrammed part, apply 10.5V to both A7 and A2 (pin 15 and pin 7).

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DM54S570/DM74S570 open-collector 2048-bit PROM
DM54S571/DM74S571 TRI-STATE® 2048-bit PROM

general description

These Schottky PROM memories are organized in the popular 512 words by 4 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 4 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

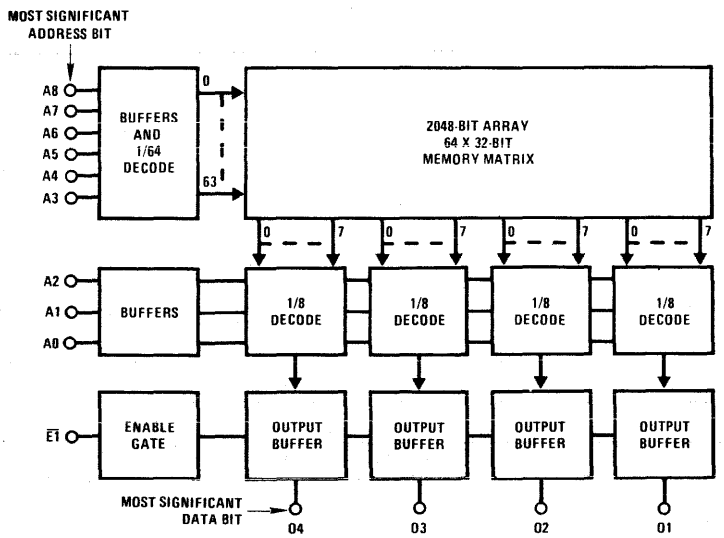
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—55 ns max
  Enable access—30 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM74S270 and DM74S370

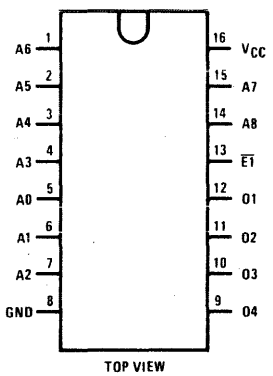
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S570		X	X		N, J
DM74S571		X		X	N, J
DM54S570	X		X		J
DM54S571	X			X	J

block diagram



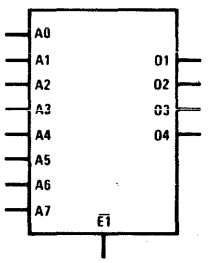
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



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absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S570, DM54S571	4.5	5.5	V
DM74S570, DM74S571	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S570, DM54S571	−55	+125	°C
DM74S570, DM74S571	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S570, 54S571			DM74S570, 74S571			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.5	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		90	130		90	130	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−30	−60	−100	−30	−60	−100	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S570, 54S571 5V ±10%; −55°C to +125°C			DM74S570, 74S571 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			40	65		40	55	ns
t_{EA}	Enable Access Time			20	35		20	30	ns
t_{ER}	Enable Recovery Time			20	35		20	30	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A8 and A2 (pin 14 and pin 7).

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DM54S572/DM74S572 open-collector 4096-bit PROM
DM54S573/DM74S573 TRI-STATE® 4096-bit PROM

general description

These Schottky PROM memories are organized in the popular 1024 words by 4 bits configuration. Two memory enable inputs are provided to control the output states. When the enable inputs are in the low state, the outputs present the contents of the selected word.

If either or both of the enable inputs is raised to a high level, it causes all 4 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

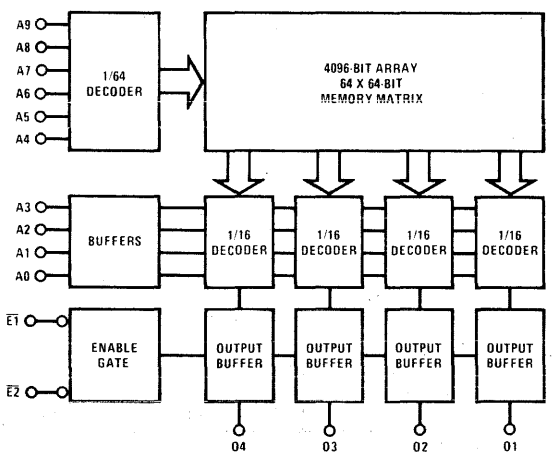
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—60 ns max
  Enable access—35 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- High density 18-pin package

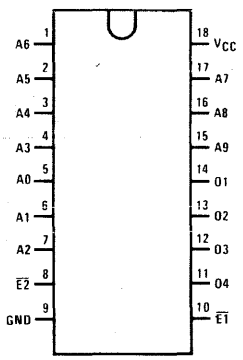
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S572		X	X		N, J
DM74S573		X		X	N, J
DM54S572	X		X		J
DM54S573	X			X	J

block diagram



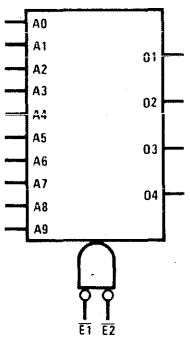
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



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absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S572, DM54S573	4.5	5.5	V
DM74S572, DM74S573	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S572, DM54S573	−55	+125	°C
DM74S572, DM74S573	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S572, 54S573			DM74S572, 74S573			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.5	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		125	140		125	140	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−30	−60	−100	−30	−60	−100	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S572, 54S573 5V ±10%; −55°C to +125°C			DM74S572, 74S573 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			40	75		40	60	ns
t_{EA}	Enable Access Time			25	45		25	35	ns
t_{ER}	Enable Recovery Time			25	45		25	35	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A7 and A2 (pin 15 and pin 7).

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DM77S295/DM87S295 open-collector 4096-bit PROM
DM77S296/DM87S296 TRI-STATE® 4096-bit PROM

general description

These Schottky memories are organized in the popular 512 words by 8 bits configuration. Four memory enable inputs are provided to control the output states. When E1 and E2 are low and E3 and E4 are high, the output presents the contents of the selected word.

If E1 or E2 are high, or E3 or E4 are low, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

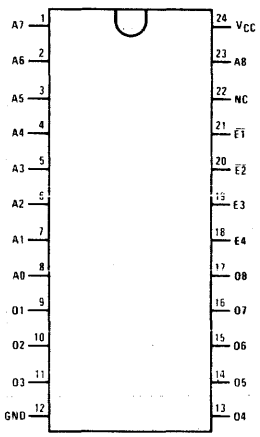
- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—65 ns
  Enable access—35 ns
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM87S95 and DM87S96

selection guide

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM87S295		X	X		N, J
DM87S296		X		X	N, J
DM77S295	X		X		J
DM77S296	X			X	J

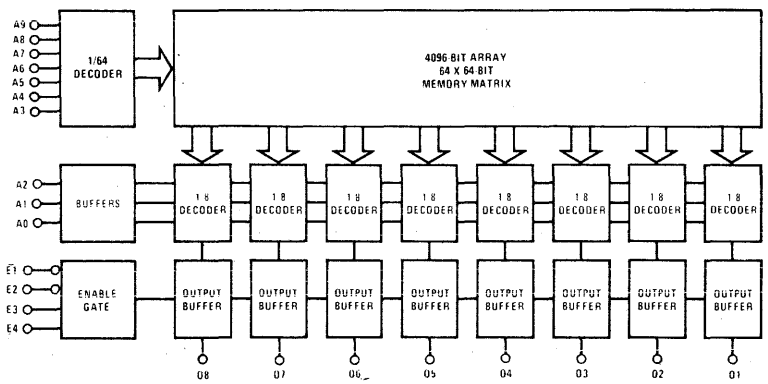
connection diagram

Dual-In-Line Package



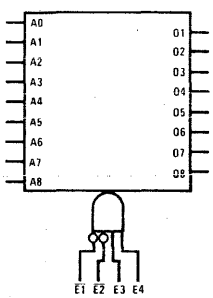
TOP VIEW

block diagram



The device is enabled when: $\overline{E1} \cdot \overline{E2} \cdot E3 \cdot E4$

logic symbol



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absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM77S295, DM77S296	4.5	5.5	V
DM87S295, DM87S296	4.75	5.25	V
Ambient Temperature (T_A)			
DM77S295, DM77S296	−55	+125	°C
DM87S295, DM87S296	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM77S295, 296			DM87S295, 296			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.5	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		115	170		115	170	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−30	−60	−100	−30	−60	−100	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM77S295, 296 5V ±10%; −55°C to +125°C			DM87S295, 296 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			40	75		40	65	ns
t_{EA}	Enable Access Time			20	40		20	35	ns
t_{ER}	Enable Recovery Time			20	40		20	35	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A7 and A2 (pin 1 and pin 6).

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Preliminary

DM54S473/DM74S473 open-collector 4096-bit PROM
DM54S472/DM74S472 TRI-STATE® 4096-bit PROM

general description

These Schottky PROM memories are organized in the popular 512 words by 8 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions.

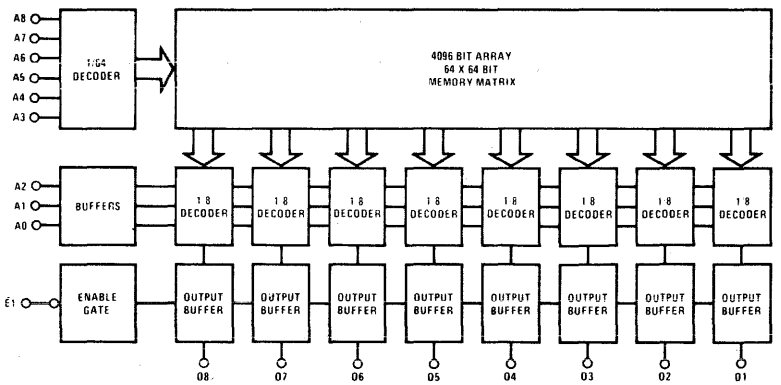
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—65 ns max
  Enable access—40 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- High density 20-pin package

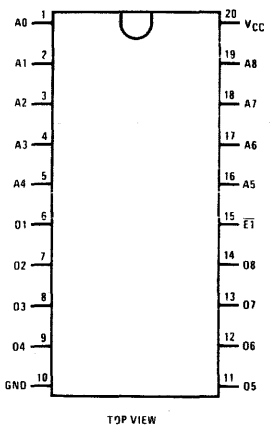
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S473		X	X		N, J
DM74S472		X		X	N, J
DM54S473	X		X		J
DM54S472	X			X	J

block diagram



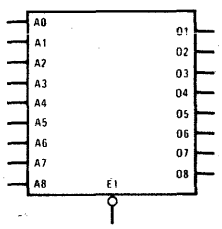
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



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absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S473, DM54S472	4.5	5.5	V
DM74S473, DM74S472	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S473, DM54S472	−55	+125	°C
DM74S473, DM74S472	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S473, 54S472			DM74S473, 74S472			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.5	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		135	165		135	165	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−30	−60	−100	−30	−60	−100	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S473, 54S472 5V ±10%; −55°C to +125°C			DM74S473, 74S472 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			45	80		45	65	ns
t_{EA}	Enable Access Time			28	55		28	40	ns
t_{ER}	Enable Recovery Time			28	55		28	40	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A7 and A2 (pin 15 and pin 7).

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DM8678 bipolar character generator

general description

The DM8678 is a 64-character bipolar character generator with serial output, and packaged in a standard 16-pin DIP designed primarily for the CRT display marketplace. The DM8678 incorporates several CRT system level functions, as well as a 7 x 9 or 5 x 7 row scan character font. The DM8678 performs the system functions of parallel to serial shifting, character address latching, character spacing, and character line spacing which are normally done with extra packages.

Shifted characters can be generated by the on-chip subtractor.

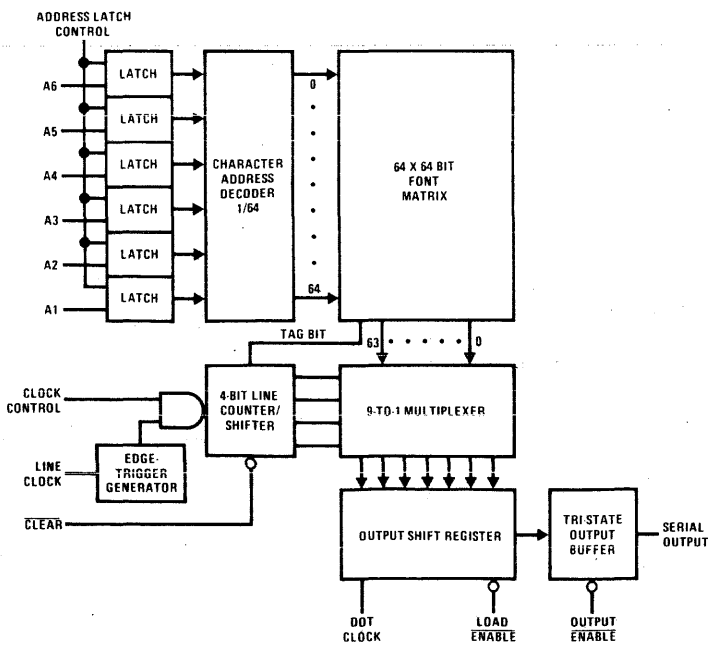
The $\overline{\text{clear}}$ input and the load $\overline{\text{enable}}$ input are active low. load $\overline{\text{enable}}$ is synchronous with the dot clock. Both the line clock and the dot clock are positive edge-triggered. When the address latch control signal is high, the character addresses "Fall Through" the latch. And when the address latch control signal goes low, the character addresses are latched.

features

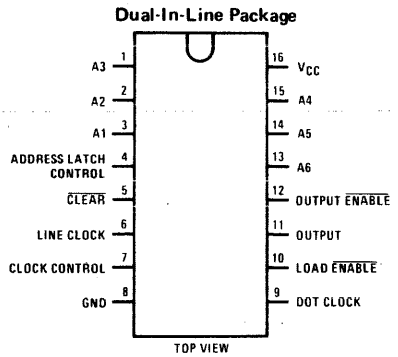
- 64-character—row scan
- 5 x 7 or 7 x 9 font
- Shifted lower case descending characters
- Serial output
- 16-pin package
- 20 MHz clock rate
- On-chip input latches
- On-chip shift register
- On-chip dot blanking
- On-chip row blanking
- TRI-STATE® output

	ROW SCAN	7 x 9	5 x 7	FONT	PACKAGE
DM8678BWF/	X	X		Upper Case Block Letters	N, J
DM8678CAE/	X	X		Shifted Lower Case Block	N, J
DM8678CAB/	X		X	Upper Case Block Letters	N, J
DM8678CAH/	X		X	Shifted Lower Case Block	N, J
DM8678CAD/	X	X		Kata Kana	N, J
DM8678BTK/	X	X		Upper Case Script Letters	N, J
DM8678CAS/	X	X		IBM 3741 Selectric	N, J

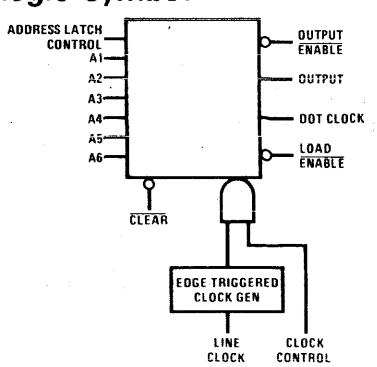
block diagram



connection diagram



logic symbol



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absolute maximum ratings (Note 1)

Supply Voltage	−0.5V to +7V
Input Voltage	−1.2V to +5.5V
Output Voltage	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−0.8	−1.6	mA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.4V			40	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{IL}	Low Level Input Voltage	V_{CC} = Min			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = Min	2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA		−0.8	−1.5	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		115	145	mA
	TRI-STATE PARAMETERS					
I_{SC}	Output Short-Circuit Current	V_O = 0V, V_{CC} = Max	−15		−50	mA
I_{HZ}	Output Leakage	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±40	μA
V_{OH}	Output Voltage High	I_{OH} = −2 mA	2.4	3.2		V

ac electrical characteristics (With standard load) (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Access Time					
T_{DO}	Dot Clock to Output			35	50	ns
T_{EA}	Output Enable			20	40	ns
T_{ER}	Output Disable			20	40	ns
	Set-Up Time					
T_{S1}	Load to Dot Clock		40	25		ns
T_{S2}	Address to Load		350	200		ns
T_{S3}	Clear to Load	See Switching Time Waveforms	350			ns
T_{S4}	Control to Line Clock		40			ns
T_{S5}	Line Clock to Load		950			ns
T_{S6}	Address to Address Latch		40			ns
	Hold Time					
T_{H1}	Load from Dot Clock		0			ns
T_{H2}	Address from Load		0			ns
T_{H3}	Control from Line Clock		100			ns
T_{H4}	Address from Address Latch		40			ns

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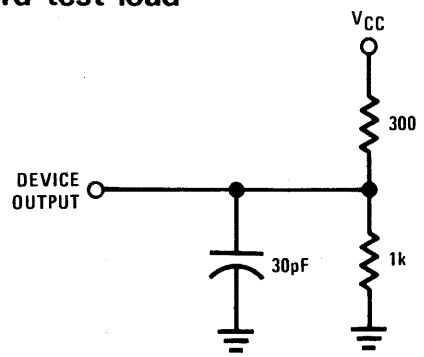
ac electrical characteristics (Continued) (With standard load) (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Minimum Pulse Width					
T_{W1}	Line Clock		40			ns
T_{W2}	Clear		40			ns
T_{W3}	Dot Clock	See Switching Time Waveforms	30			ns
T_{W4}	Load		60			ns
T_{W5}	Address Latch		40			ns
f_{MAX}	Maximum Clock Frequency		16	20		MHz

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

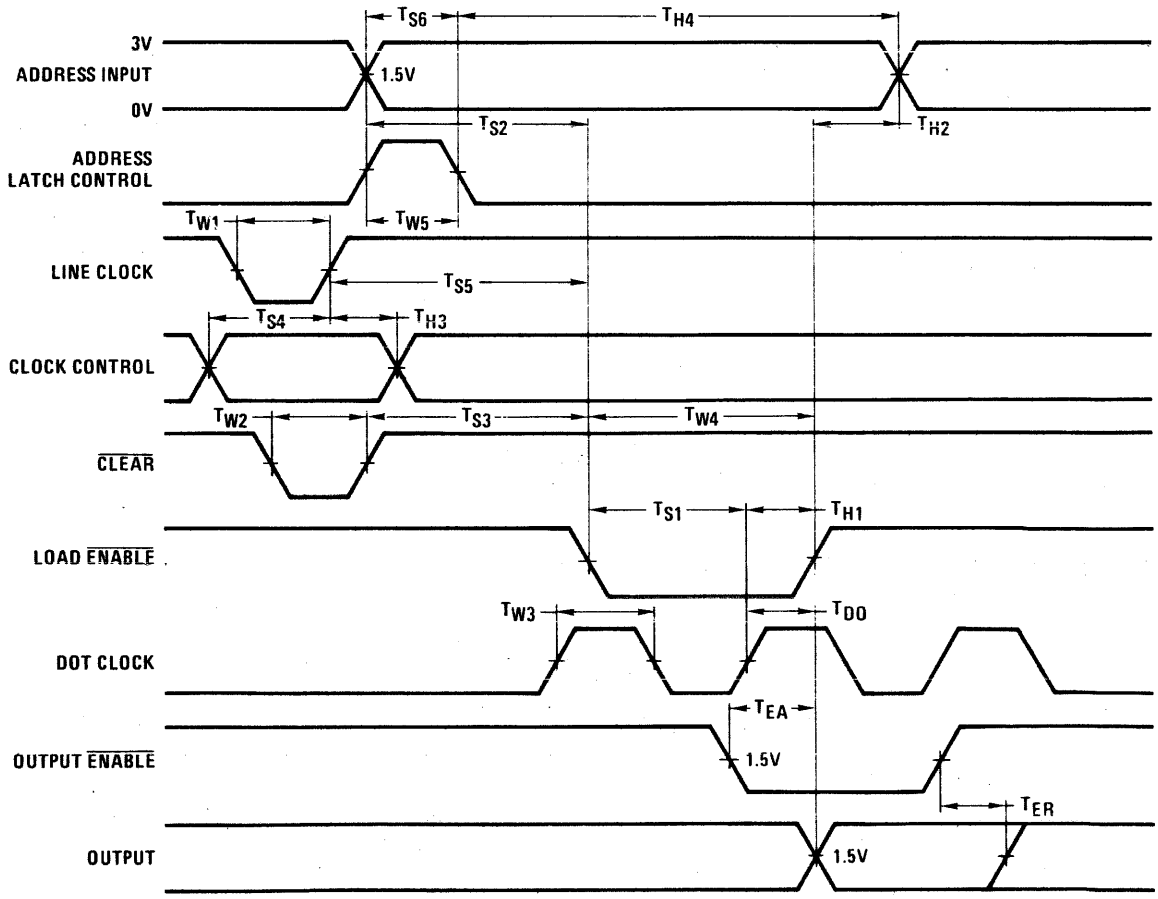
Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

standard test load



- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50 Ω, $t_r < 2.5$ ns and $t_f < 2.5$ ns (between 1.0V and 2.0V).
- T_{DO} is measured with output enable at a steady low level.

switching time waveforms



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truth tables

a) Address Latch

ADDRESS LATCH CONTROL	FUNCTION PERFORMED
0	Latched
1	Fall Through

b) Output

OUTPUT $\overline{\text{ENABLE}}$	STATE OF THE OUTPUT
1	Output Hi-Z
0	Data Out

c) 4-Bit Line Counter

CLOCK CONTROL	LINE CLOCK	$\overline{\text{CLEAR}}$	LINE COUNTER
H	⌐	H	Increment line counter
X	X	L	Asynchronous clear resets counter
L	X	H	Clock inhibited
H	¬	H	No change on high-to-low clock edge

X = Don't care

definitions

A1–A6: Character address. A 6-bit code which selects 1 of the 64 characters in the font.

$\overline{\text{Clear}}$: Active low clear for mod 16 row counter, (can be used to truncate mod 16 counter).

Line Clock: Clock that advances the line counter. Advances counter on the low-to-high transition.

Clock Control: Enables line clock when high and disables line clock when low.

Load $\overline{\text{Enable}}$: Active low load command which routes data from the character ROM to the "D" inputs of the 7-bit shift register.

Dot Clock: A low-to-high transition of the dot clock loads the shift register if load $\overline{\text{enable}}$ is low or shifts data if load $\overline{\text{enable}}$ is high.

Output $\overline{\text{Enable}}$: An active low output enable. When high the output is in the Hi-Z state.

Output: A TTL TRI-STATE output buffer.

functional description

To select a character, a 6-bit binary word must be present at the address inputs A1–A6 when the address latch control is high. This address can be latched by bringing the address latch control signal low after a 40 ns set-up time. When the $\overline{\text{clear}}$ input receives a low pulse, the counter is reset to zero. The shift register can be loaded (t_{ASL} ns) after the character is addressed. Data, representing one horizontal line of the addressed character, is available at the output when the load $\overline{\text{enable}}$ input is brought low. As shown in *Figure 1*, valid data arrives serially at the output. Dot clock pulses beyond that required to shift out one line of the character will add lows to the end of character. This provides a horizontal spacing between characters.

Figure 2 shows how the counter sequences through the rows of addressed lines with the application of clock pulses at the line clock input. Any additional line clocks beyond that required to display the character will put a vertical space between characters. This spacing can be truncated by bringing the $\overline{\text{clear}}$ input low. Detailed system application infomation is contained in application note AN-167 available from National.

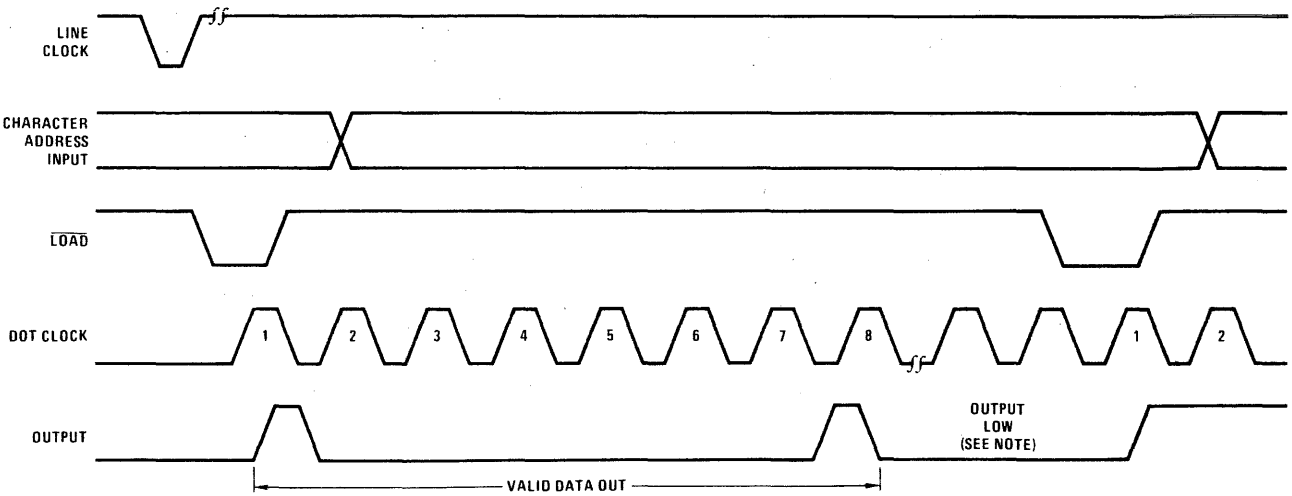
A two character display example is shown in *Figure 3* and a typical system timing waveform is shown in *Figure 4.*

A chip select input is provided for expansion of the character font. The various standard fonts are shown in *Figures 5, 6, 7, 8, 9 and 10.*

functional description (Continued)

Character Cycle – ROM data corresponding to one line of characters is loaded into the shift register t_{ASL} after the ROM is addressed. When load $\overline{\text{enable}}$ goes low, ROM data is allowed to be present at the D input of the shift register via the MUX. The first bit of the ROM data is transferred to the output at the next low-to-high transition of the dot clock. After load $\overline{\text{enable}}$ goes back high, the second to seventh clock pulses shift out the rest of the selected row of the addressed character. Additional clock pulses will shift out low data used for spacing.

Line Cycle – The line counter is a mod 16 counter. A low-to-high transition of the line clock advances the line counter to the next count. If, for any reason, the counts need to be truncated, a low signal at the $\overline{\text{clear}}$ input resets the counter to zero. The clock control may be used as a line clock disable. A high signal at the line clock control terminal enables the counter and a low signal disables the line clock.



Note. Output goes and stays low following the leading edge of the eighth Dot-Clock pulse until load $\overline{\text{enable}}$ is enabled again and new parallel data is loaded into the shift register.

FIGURE 1. Character Cycle

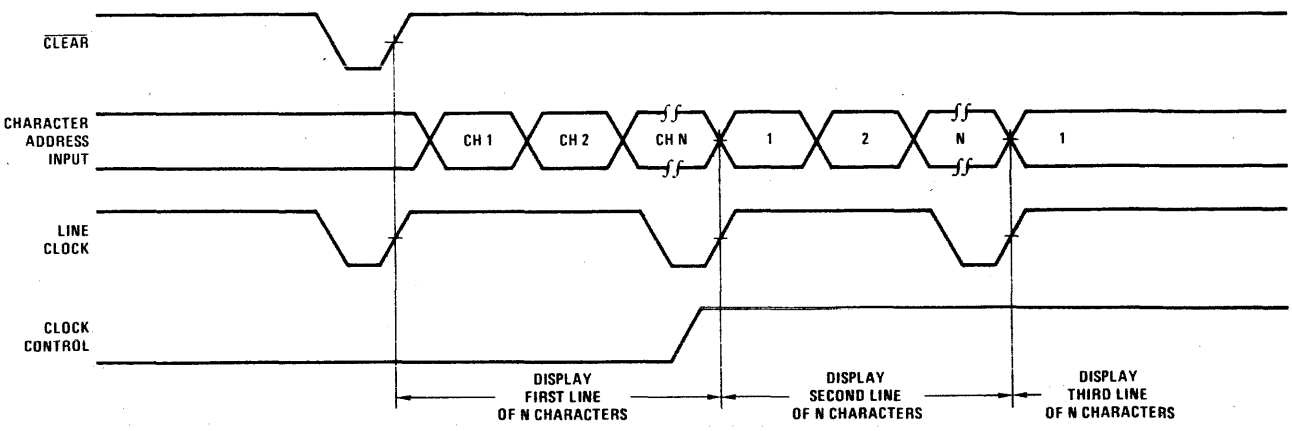


FIGURE 2. Line Cycle

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DM54S270/DM74S270 open-collector 2048-bit ROM
DM54S370/DM74S370 TRI-STATE® 2048-bit ROM

general description

These Schottky ROM memories are organized in the popular 512 words by 4 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

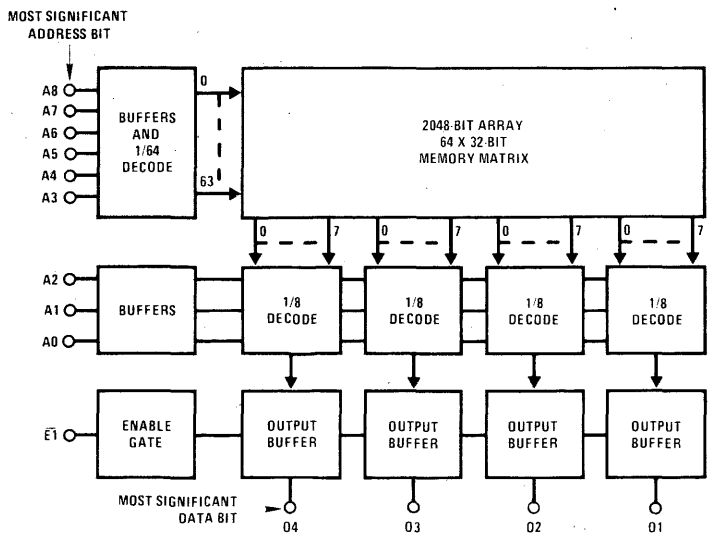
If the enable input is raised to a high level, it causes all 4 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as PROM's as well as ROM's.

features

- Schottky-clamped for high speed
  Address access—55 ns max
  Enable access—30 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- PROM mates are DM74S570 and DM74S571

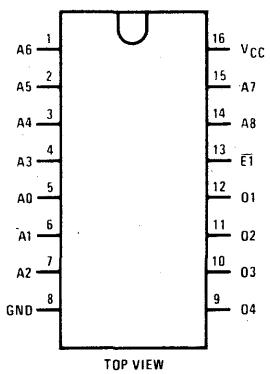
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S270		X	X		N, J
DM74S370		X		X	N, J
DM54S270	X		X		J
DM54S370	X			X	J

block diagram



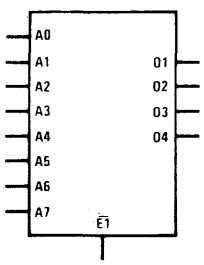
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



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absolute maximum ratings (Note 1)

Supply Voltage	−0.5V to +7V
Input Voltage	−1.2V to +5.5V
Output Voltage	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S270, DM54S370	4.5	5.5	V
DM74S270, DM74S370	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S270, DM54S370	−55	+125	°C
DM74S270, DM74S370	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 2)

PARAMETER		CONDITIONS	DM54S270, 54S370			DM74S270, 74S370			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.5	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25 C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25 C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		80	130		80	130	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 3)	30	60	−100	−30	−60	−100	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			+50			±50	μA
V_{OH}	Output Voltage High	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S270, 54S370 5V ±10%; −55°C to +125°C			DM74S270, 74S370 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			37	70		37	55	ns
t_{EA}	Enable Access Time			18	35		18	30	ns
t_{ER}	Enable Recovery Time			18	35		18	30	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 3: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

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DM77S95/DM87S95 open-collector 4096-bit ROM
DM77S96/DM87S96 TRI-STATE® 4096-bit ROM

general description

These Schottky ROM memories are organized in the popular 512 words by 8 bits configuration. Four memory enable inputs are provided to control the output states. When E1 and E2 are low and E3 and E4 are high, the output presents the contents of the selected word.

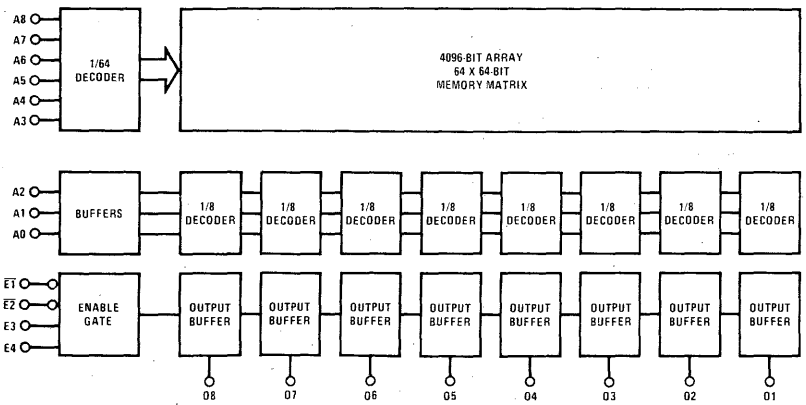
If E1 or E2 are high, or E3 or E4 are low, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions and are available as PROM's as well as ROM's.

features

- Schottky-clamped for high speed
  Address access—65 ns max
  Enable access—35 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- PROM mates are DM87S295 and DM87S296

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM87S95		X	X		N, J
DM87S96		X		X	N, J
DM77S95	X		X		J
DM77S96	X			X	J

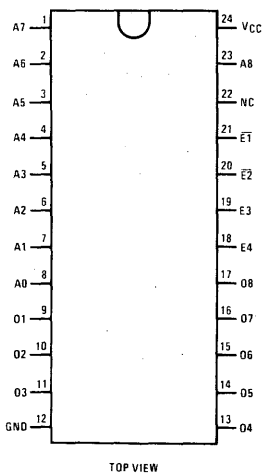
block diagram



The device is enabled when: $\overline{E}_1 \cdot \overline{E}_2 \cdot E_3 \cdot E_4$

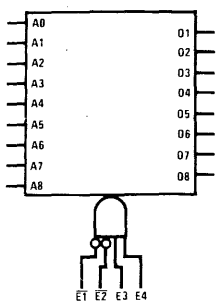
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



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absolute maximum ratings (Note 1)

Supply Voltage	0.5V to +7V
Input Voltage	−1.2V to +5.5V
Output Voltage	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM77S95, DM77S96	4.5	5.5	V
DM87S95, DM87S96	4.75	5.25	V
Ambient Temperature (T_A)			
DM77S95, DM77S96	−55	+125	°C
DM87S95, DM87S96	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 2)

PARAMETER		CONDITIONS	DM77S95, 77S96			DM87S95, 87S96			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.5	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max; All Inputs Grounded, All Outputs Open		110	170		115	170	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 3)	−30	−60	−100	−30	−60	−100	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High,	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM87S95, 87S96 5V ±10%; −55°C to +125°C			DM77S95, 77S96 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			37	80		37	65	ns
t_{EA}	Enable Access Time			18	40		18	35	ns
t_{ER}	Enable Recovery Time			18	40		18	35	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 3: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

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DM75S29/DM85S29 open-collector 8192-bit ROM
DM75S28/DM85S28 TRI-STATE® 8192-bit ROM

general description

These Schottky ROM memories are organized in the popular 1024 words by 8 bits configuration. Four memory enable inputs are provided to control the output states. When E1 and E2 are low and E3 and E4 are high, the output presents the contents of the selected word.

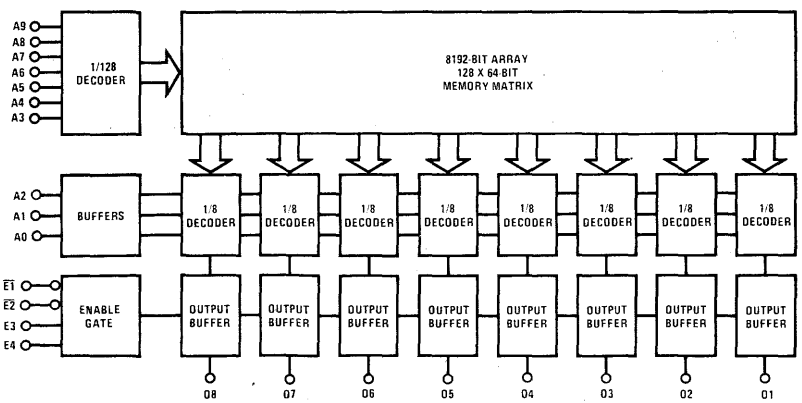
If E1 or E2 are high, or E3 or E4 are low, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as PROM's as well as ROM's.

features

- Schottky-clamped for high speed
  Address access—70 ns max
  Enable access—45 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- PROM mates are DM87S229 and DM87S228

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM85S29		X	X		N, J
DM85S28		X		X	N, J
DM75S29	X		X		J
DM75S28	X			X	J

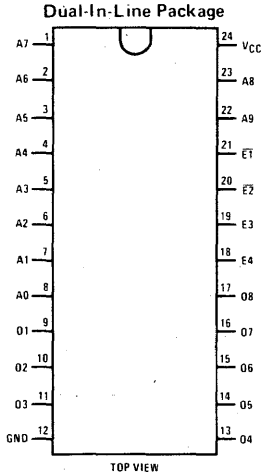
block diagram



The device is enabled when: $\overline{E1} \cdot \overline{E2} \cdot E3 \cdot E4$

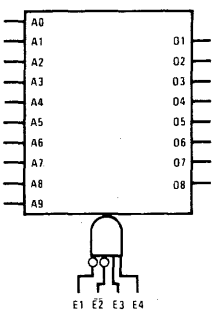
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



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absolute maximum ratings (Note 1)

Supply Voltage	−0.5V to +7V
Input Voltage	−1.2V to +5.5V
Output Voltage	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM75S29, DM75S28	4.5	5.5	V
DM85S29, DM85S28	4.75	5.25	V
Ambient Temperature (T_A)			
DM75S29, DM75S28	−55	+125	°C
DM85S29, DM85S28	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 2)

PARAMETER		CONDITIONS	DM75S29, 75S28			DM85S29, 85S28			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.5	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		140	170		140	170	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 3)	−30	−60	−100	−30	−60	−100	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM75S29, 75S28 5V ±10%; −55°C to +125°C			DM85S29, 85S28 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			47	90		47	70	ns
t_{EA}	Enable Access Time			30	50		30	45	ns
t_{ER}	Enable Recovery Time			30	50		30	45	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 3: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

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Bipolar ROMs

DM7575/DM8575, DM7576/DM8576 programmable logic array (PLA)

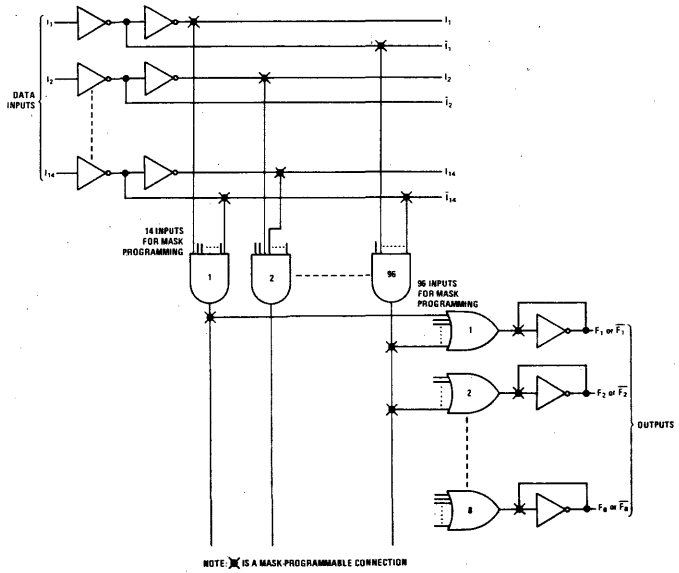
general description

The DM7575/DM8575 and DM7576/DM8576 are mask-programmable logic arrays designed for use in applications where random logic is required. The devices have fourteen data inputs and eight outputs. Each output provides a sum of product terms where each product term can contain any combination of 14 variables or their complements. The total number of product terms which can be provided is 96. Any product term which is repeated is counted only once. Since some functions are more easily represented in their inverted form, an option is provided to allow for either the true or complement of the function on each output. The products are particularly useful in providing control logic for digital systems. The DM7575/DM8575 has a conventional totem-pole output whereas the DM7576/DM8576 is provided with a passive pullup output. This latter configuration is useful in expanding functions by connection of outputs of different packages.

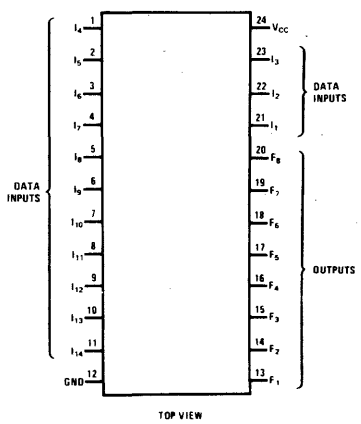
features

- A 2^{14}-by-8 (128k) bit memory would be needed to provide equivalent function
- Typical delay 90 ns
- Typical power dissipation 550 mW
- Series 54/74 compatible

logic and connection diagrams



Dual-In-Line Package



Order Number DM7575J, DM8575J, DM7576J or DM8576J
See Package 11

Order Number DM8575N or DM8576N
See Package 18

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absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7575, DM7576	4.5	5.5	V
DM8575, DM8576	4.75	5.25	V
Temperature (T_A)			
DM7575, DM7576	−55	+125	°C
DM8575, DM8576	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Voltage (DM7575/DM8575 Only)	V_{CC} = Min, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 0.8V, I_{OUT} = −800μA	2.4			V
Logical "1" Output Current (DM7576/DM8576 Only)	V_{CC} = Max, V_{OUT} = 5.5V			100	μA
Logical "0" Output Voltage	V_{CC} = Min, $V_{IN(1)}$ = 2V, $V_{IN(0)}$ = 0.8V, I_{OUT} = +12 mA			0.4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
	V_{CC} = Max, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1.0	mA
Output Short Circuit Current (Note 3) DM7575/76	V_{CC} = Max, V_{OUT} = 0V	−20/−1.75		−55/−3.5	mA
Output Short Circuit Current (Note 3) DM8575/76		−18/−1.65		−55/−3.3	mA
Supply Current	V_{CC} = Max		110	170	mA
Input Diode Clamp Voltage	V_{CC} = Min, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Propagation Delay to a Logical "0" from Data Inputs to Outputs, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω		100	150	ns
Propagation Delay to a Logical "1" from Data Inputs to Outputs, t_{pd1}	V_{CC} = 5.0V, T_A = 25°C		80	150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7575/76 and across the 0°C to 70°C range for the DM8575/76. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

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Bipolar RAMs

DM5489/DM7489 (SN5489/SN7489)
64-bit random access read/write memory

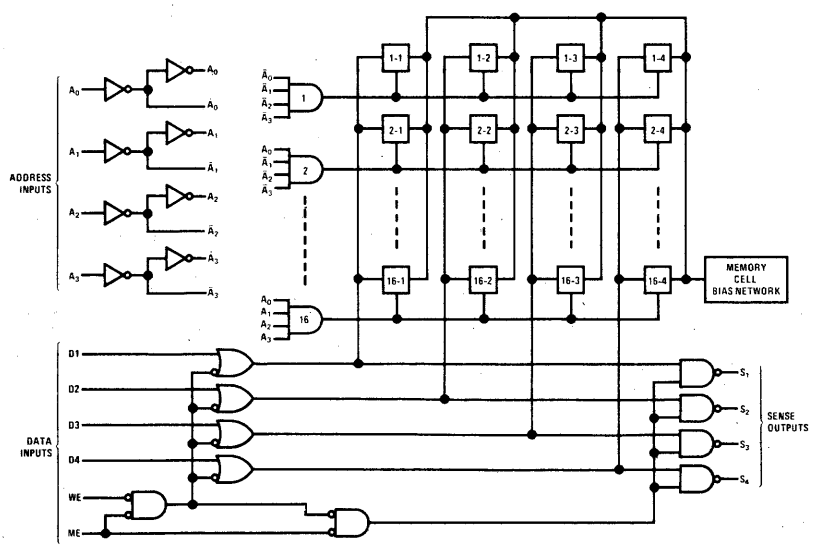
general description

The DM5489/DM7489 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the logical "1" state.

features

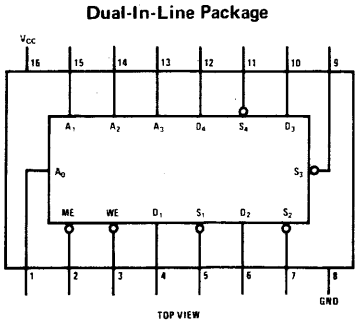
- Series 54/74 compatible
- Organized as 16 4-bit words
- Typical access from chip enable 23 ns
- Typical access 35 ns
- Typical power dissipation 400 mW
- Open collector outputs to permit "wire OR" capability

block diagram



connection diagram

Dual-In-Line Package



Order Number DM5489J
or DM7489J
See Package 10

Order Number DM7489N
See Package 15

truth table

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
0	0	Write	Logical "1" State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Logical "1" State

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absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Operating Temperature Range	
DM5489	−55°C to +125°C
DM7489	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM5489	V_{CC} = 4.5V		2.0			V
	DM7489	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM5489	V_{CC} = 4.5V				0.8	V
	DM7489	V_{CC} = 4.75V					
Logical "1" Output Current	DM5489	V_{CC} = 5.5V	V_O = 5.25V			100	μA
	DM7489	V_{CC} = 5.25V				20	μA
Logical "0" Output Voltage	DM5489	V_{CC} = 4.5V	I_O = 12 mA			0.4	V
	DM7489	V_{CC} = 4.75V					
Logical "1" Input Current	DM5489	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM7489	V_{CC} = 5.25V					
	DM5489	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM7489	V_{CC} = 5.25V					
Logical "0" Input Current	DM5489	V_{CC} = 5.5V				−1.6	mA
	DM7489	V_{CC} = 5.25V					
Supply Current	DM5489	V_{CC} = 5.5V	All Inputs at GND		80	120	mA
	DM7489	V_{CC} = 5.25V					
Input Clamp Voltage	DM5489	V_{CC} = 4.5V	I_{IN} = −12 mA			V_{CC} −1.5	V
	DM7489	V_{CC} = 4.75V					

switching characteristics (Over recommended operating ranges of V_{CC} and T_A)

PARAMETER			CONDITIONS	DM5489			DM7489			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Access Time From Address		R_{L1} = 300Ω, R_{L2} = 600Ω, C_L = 30 pF		34	80		34	60	ns
t_{PHL}					35	80		35	60	ns
t_{PLH}	Disable Time From Memory Enable				23	55		23	40	ns
t_{PHL}	Enable Time From Memory Enable				23	55		23	40	ns
t_{SETUP}	Setup Time	Address to Write Enable		0	−14		0	−14		ns
		Data to Write Enable		0	−15		0	−15		ns
		Memory Enable To Write Enable		0	−10		0	−10		ns
t_{HOLD}	Hold Time	Address From Write Enable		5	−7		5	−7		ns
		Data From Write Enable		0	−14		0	−14		ns
		Memory Enable From Write Enable		0	−10		0	−10		ns
t_{WP}	Write Pulse Width			50	20		40	20		ns
t_{SR}	Sense Recovery Time				31	65		31	55	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5489 and across the 0°C to 70°C range for the DM7489. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

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DM54LS189/DM74LS189 low power 64-bit random access memories with TRI-STATE® outputs

general description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of 4 bits each. They are fully decoded and feature a chip enable input to simplify decoding required to achieve the desired system organization. This device is implemented with low power Schottky technology resulting in one-fifth power while retaining the speed of standard TTL.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast rise time characteristics of the TTL totem-pole output. Systems utilizing data bus lines with a defined pull-up impedance can employ the open-collector DM54LS289.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip enable input and the read/write input are low. While the read/write input is low, the outputs are in the high impedance state. When a number of the DM54LS189 outputs are bus-connected, this high impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

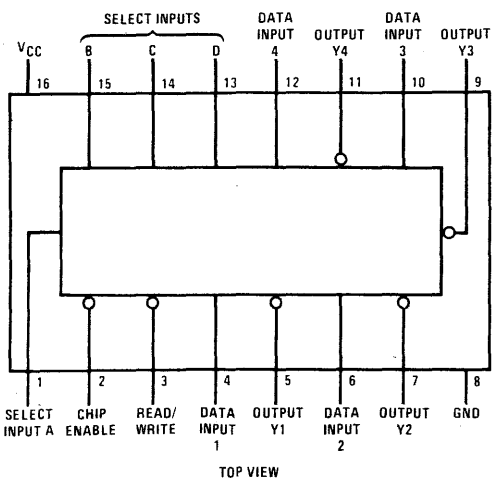
Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip enable is low. When the chip enable input is high, the outputs will be in the high impedance state.

features

- Schottky-clamped for high speed applications
  - Access from chip enable input—40 ns typ
  - Access from address inputs—60 ns typ
- TRI-STATE outputs drive bus-organized systems and/or high capacitive loads
- Low power—75 mW typ
- DM54LS189 is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL and DTL logic circuits
- Chip enable input simplifies system decoding

connection diagram

Dual-In-Line and Flat Package



TOP VIEW

truth table

FUNCTION	INPUTS		OUTPUT
	CHIP ENABLE	READ/ WRITE	
Write (Store Complement of Data)	L	L	H
Read	L	H	Stored Data
Inhibit	H	X	H

H = high level
L = low level
X = don't care

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absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54LS189	4.5	5.5	V
DM74LS189	4.75	5.25	V
Temperature (T_A)			
DM54LS189	55	+125	°C
DM74LS189	0	+70	°C

electrical characteristics

Over recommended operating free-air temperature range (unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2 mA	2.4	3.4		V
				2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 4 mA DM54LS189			0.45	V
			I_{OL} = 8 mA DM74LS189			0.5	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7				10	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V				−100	μA
I_{OS}	Short-Circuit Output Current (Note 4)	V_{CC} = Max, V_O = 0V		−30		−100	mA
I_{CC}	Supply Current (Note 5)	V_{CC} = Max			15	25	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OZH}	TRI-STATE Output Current, High Level Voltage Applied	V_{CC} = Max, V_O = 2.4V				40	μA
I_{OZL}	TRI-STATE Output Current, Low Level Voltage Applied	V_{CC} = Max, V_O = 0.45V				40	μA

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switching characteristics

Over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			CONDITIONS	DM54LS189			DM74LS189			UNITS
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
t_{AA}	Access Times From Address				60	100		60	10	ns
t_{CZH}	Output Enable Time to High Level	Access Times From Chip Enable	C_L = 30 pF, R_L = 1 kΩ,		40	80		40	60	ns
t_{CZL}	Output Enable Time to Low Level				40	80		40	60	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times From Read/Write			60	100		60	80	ns
t_{WZL}	Output Enable Time to Low Level				60	100		60	80	ns
t_{CHZ}	Output Disable Time From High Level	Disable Times From Chip Enable	C_L = 5 pF, R_L = 1 kΩ,		40	80		40	60	ns
t_{CLZ}	Output Disable Time From Low Level				40	80		40	60	ns
t_{WHZ}	Output Disable Time From High Level	Disable Times From Read/Write			40			40		ns
t_{WLZ}	Output Disable Time From Low Level				40			40		
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			100			80			ns
t_{ASW}	Set-Up Time	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		100			80			
t_{CSW}		Chip Enable to Read/Write		0			0			
t_{AHW}	Hold Time	Address From Read/Write		0			0			ns
t_{DHW}		Data From Read/Write		0			0			
t_{CHW}		Chip Enable From Read/Write		0			0			

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54LS189 and across the 0°C to +70°C range for the DM74LS189. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: I_{CC} is measured with all inputs grounded, and the outputs open.

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Bipolar RAMs

DM54S189/DM74S189 64-bit random access memories with TRI-STATE® outputs

general description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of four-bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −0.25 mA, only one-eighth that of a DM54S/DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast-rise-time characteristics of the TTL totem-pole output. Systems utilizing data-bus lines with a defined pull-up impedance can employ the open-collector DM54S289.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-impedance state. When a number of the DM54S189 outputs are bus-connected, this high-impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable input is high, the outputs will be in the high-impedance state.

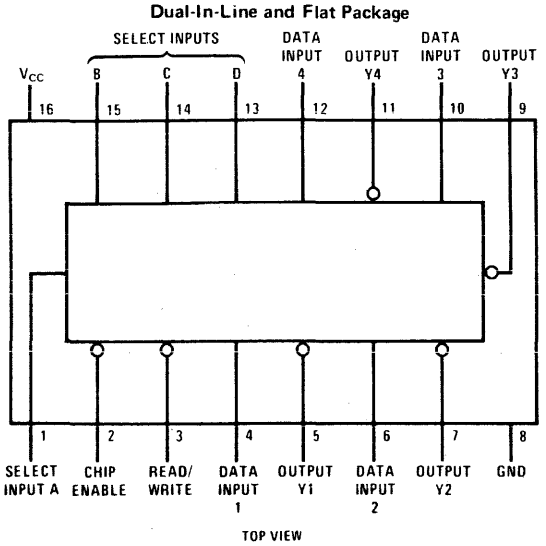
The fast access time of the DM54S189 makes it particularly attractive for implementing high-performance memory functions requiring access times on the order of 25 ns. The high capacitive-drive capability of the outputs permits expansion without additional output buffering. The unique functional capability of the DM54S189 outputs being at a high impedance during writing combined with the data inputs being inhibited during reading means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

features

- Schottky-clamped for high-speed applications:
  - access from chip-enable input 12 ns typ
  - access from address inputs 25 ns typ
- TRI-STATE outputs drive bus-organized systems and/or high capacitive loads
- DM54S289, DM74S289 are functionally equivalent, have open-collector outputs, and are compatible with Intel 3101A in most applications
- DM54S189 is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL and DTL logic circuits
- Chip-enable input simplifies system decoding

connection diagram

Dual-In-Line and Flat Package



TOP VIEW

truth table

FUNCTION	INPUTS		OUTPUT
	CHIP ENABLE	READ/ WRITE	
Write (Store Complement of Data)	L	L	High Impedance
Read	L	H	Stored Data
Inhibit	H	X	High Impedance

H High Level
L Low Level
X Don't Care

Order Number DM54S189J or DM74S189J
See Package 10
Order Number DM74S189N
See Package 15

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absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S189	4.5	5.5	V
DM74S189	4.75	5.25	V
Temperature (T_A)			
DM54S189	−55	+125	°C
DM74S189	0	+70	°C

electrical characteristics

over recommended operating free-air temperature range (unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min, I_{OH} = −2.0 mA, DM54S189		2.4	3.4		V
		V_{CC} = Min, I_{OH} = −6.5 mA, DM74S189		2.4	3.2		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA	DM54S189			0.5	V
			DM74S189			0.45	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7				25	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V				−250	μA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max, V_O = 0V		−30		−100	mA
I_{CC}	Supply Current (Note 5)	V_{CC} = Max			75	110	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OZH}	TRI-STATE Output Current, High Level Voltage Applied	V_{CC} = Max, V_O = 2.4V				50	μA
I_{OZL}	TRI-STATE Output Current, Low Level Voltage Applied	V_{CC} = Max, V_O = 0.45V				−50	μA

switching characteristics

over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			CONDITIONS	LIMITS DM54S189 MIN	DM54S189 TYP(1)	DM54S189 MAX	DM74S189 MIN	DM74S189 TYP(1)	DM74S189 MAX	UNITS
t_{AA}	Access Times From Address		C_L = 30 pF, R_L = 280Ω, *(Figure 1)*		25	50		25	35	ns
t_{CZH}	Output Enable Time to High Level	Access Times From Chip Enable			12	25		12	17	ns
t_{CZL}	Output Enable Time to Low Level				12	25		12	17	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times From Read/Write			22	40		22	35	ns
t_{WZL}	Output Enable Time to Low Level				22	40		22	35	ns

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switching characteristics (con't)

PARAMETER			CONDITIONS	LIMITS						UNITS
				DM54S189			DM74S189			
				MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
t_{CHZ}	Output Disable Time From High Level	Disable Times From Chip Enable	C_L = 5 pF, R_L = 280Ω *(Figure 1)*		12	25		12	17	ns
t_{CLZ}	Output Disable Time From Low Level				12	25		12	17	ns
t_{WHZ}	Output Disable Time From High Level	Disable Times From Read/Write			12			12		ns
t_{WLZ}	Output Disable Time From Low Level				12			12		ns
t_{WP}	Width of Write-Enable Pulse (Read/Write Low)			25			25			ns
t_{ASW}	Set-Up Time *(Figure 1)*	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			25			
t_{CSW}		Chip-Enable to Read/Write		0			0			
t_{AHW}	Hold Time *(Figure 1)*	Address From Read/Write		0			0			ns
t_{DHW}		Data From Read/Write		0			0			
t_{CHW}		Chip-Enable From Read/Write		0			0			

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

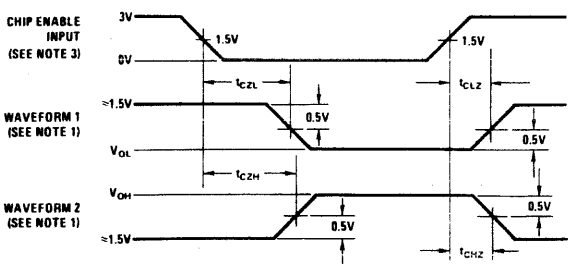
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54S189 and across the 0°C to +70°C range for the DM74S189. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

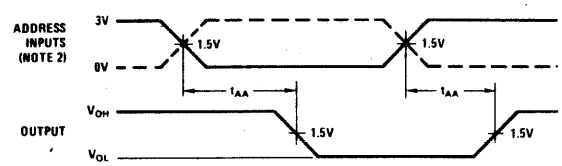
Note 4. Only one output at a time should be shorted.

Note 5: I_{CC} is measured with all inputs grounded, and the outputs open.

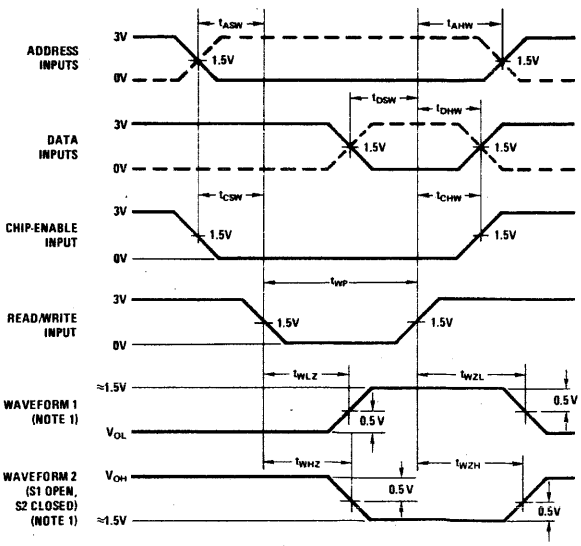
switching time waveforms



Enable and Disable Time From Chip Enable



Access Time From Address Inputs



Write Cycle

FIGURE 1

Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.

Note 2. When measuring delay times from address inputs, the chip enable input is low and the read/write input is high.

Note 3: When measuring delay times from chip enable input, the address inputs are steady-state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{OUT} \approx 50\Omega$.

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DM75S68/DM85S68 64-bit (16×4) edge triggered register

general description

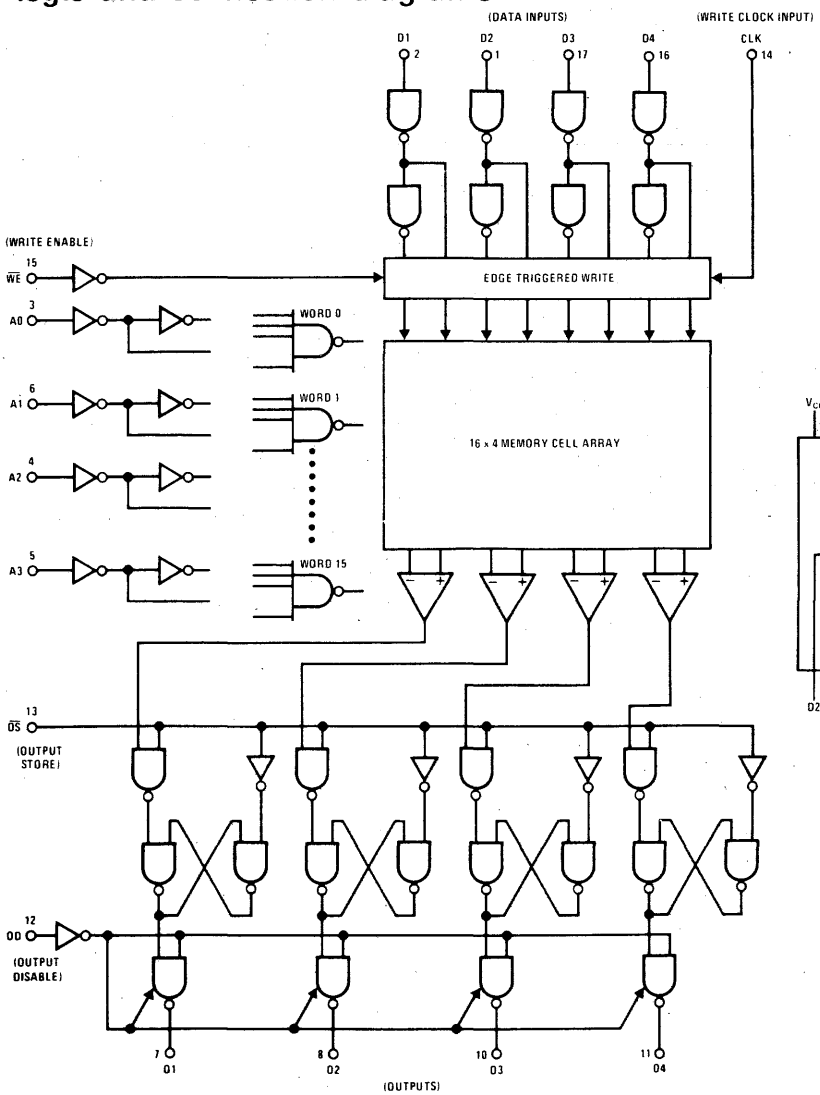
The DM75S68/DM85S68 is an addressable "D" register file. Any of its 16 four-bit words may be asynchronously read or may be written into on the next clock transition. An input terminal is provided to enable or disable the synchronous writing of the input data into the location specified by the address terminals. An output disable terminal operates only as a TRI-STATE® output control terminal. The addressable register data may be latched at the outputs and retained as long as the output store terminal is held in a low state. This memory storage condition is independent of the state of the output disable terminal.

All input terminals are high impedance at all times, and all outputs have low impedance active drive logic states and the high impedance TRI-STATE condition.

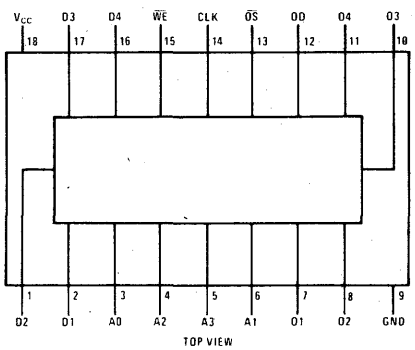
features

- On chip output register
- Edge triggered write
- High speed — 30 ns typ
- TRI-STATE output
- Optimized for register stack applications
- Typical power dissipation — 350 mW
- 18-pin package

logic and connection diagrams



Dual-In-Line Package



Order Number DM75S68D
or DM85S68D
See Package 4
Order Number DM85S68N
See Package 16

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absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DM85S68	4.75	5.25	V
DM75S68	4.5	5.5	V
Temperature, T_A			
DM85S68	0	70	°C
DM75S68	−55	+125	°C

electrical characteristics

over recommended operating free-air temperature range (unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM75S68 I_{OH} = −5.2 mA, DM85S68	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA	DM75S68			0.5	V
			DM85S68			0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_{IH} = 2.4V	Clock Input			50	μA
			All Others			25	
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_{IH} = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{iL} = 0.5V	Clock Input			−500	μA
			All Others			−250	μA
I_{OS}	Short Circuit Output Current(4)	V_{CC} = Max, V_{OL} = 0V		−20		−55	mA
I_{CC}	Supply Current	V_{CC} = Max			70	100	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA				−1.2	V
I_{OZ}	TRI-STATE Output Current	V_{CC} = Max	V_O = 2.4V			+40	μA
			V_O = 0.5V			−40	

switching characteristics over recommended operating range of T_A and V_{CC} (unless otherwise noted)

PARAMETER			DM75S68 MIN	DM75S68 TYP	DM75S68 MAX	DM85S68 MIN	DM85S68 TYP	DM85S68 MAX	UNITS
t_{ZH}	Output Enable to High Level			20	40		20	35	ns
t_{ZL}	Output Enable to Low Level			14	30		14	24	ns
t_{HZ}	Output Disable Time From High Level			10	18		10	15	ns
t_{LZ}	Output Disable Time From Low Level			12	22		12	18	ns
t_{AA}	Access Time	Address to Output		30	55		30	40	
t_{OSA}		Output Store to Output		20	35		20	30	ns
t_{CA}		Clock to Output		25	50		25	40	
t_{ASC}	Set-Up Time	Address to Clock	25	5		15	5		
t_{DSC}		Data to Clock	15	5		5	0		
t_{ASOS}		Address to Output Store	40	15		30	15		ns
t_{WESC}		Write Enable Set-Up Time	10	5		5	0		
t_{OSSC}		Store Before Write	15	0		10	0		
t_{AHC}	Hold Time	Address From Clock	15	5		10	5		
t_{DHC}		Data From Clock	20	5		15	5		ns
t_{AHOS}		Address From Output Store	10	0		5	0		
t_{WEHC}		Write Enable Hold Time	20	5		15	5		

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM75S68 and across the 0°C to +70°C range for the DM85S68. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

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DM54S206/DM74S206 256-bit read/write schottky memories with open-collector outputs

general description

The DM54S206/DM74S206 256-bit active-element memories are monolithic transistor-transistor logic (TTL) integrated circuits organized as 256 words of one bit each. They are fully decoded and have three gated memory-enable inputs to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors which reduce the low-level input current requirement to a maximum of −0.25 milliamperes, only one-eighth that of a normalized Series 54S/74S load factor. The memory-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

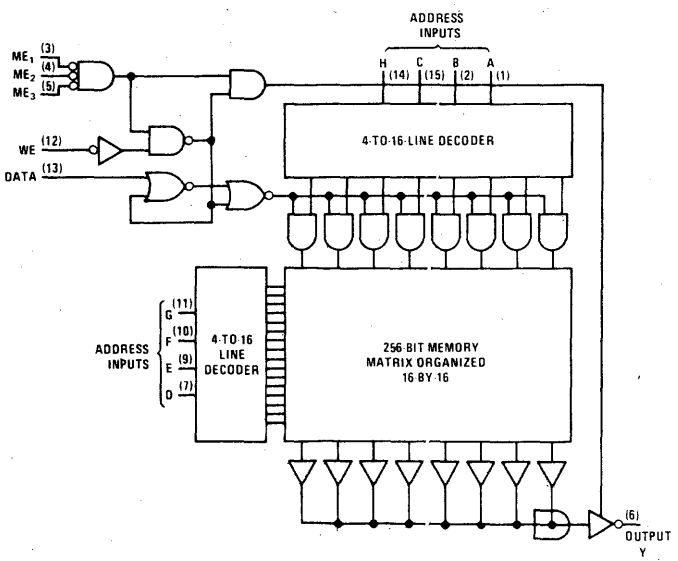
Write Cycle: The complement of the information at the data input is written into the selected location when all memory-enable inputs and write-enable input are low. While the write-enable input is low, the output is off.

Read Cycle: The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the three memory-enable inputs are low. When any one of the memory enable inputs is high, the output will be off.

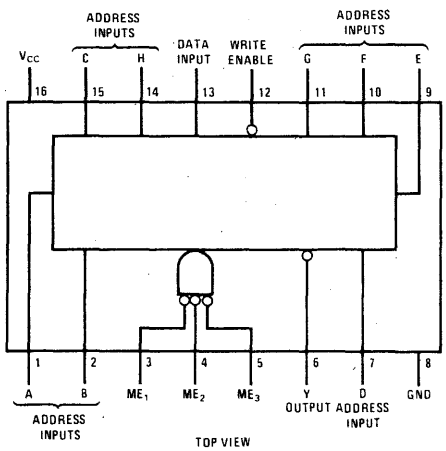
features

- Schottky-clamped for high-speed memory systems:
  - Access from memory-enable inputs 17 ns typ
  - Access from address inputs 35 ns typ
  - Power dissipation 1.4 mW/bit typ
- Open-collector output for word expansion
- Fully decoded, organized as 256 words of one bit each
- Compatible with most TTL and DTL logic circuits
- Multiple memory-enable inputs to minimize external decoding

block and connection diagrams



Dual-In-Line and Flat Package



Order Number DM54S206J or DM74S206J
See Package 10
Order Number DM74S206N
See Package 15
Order Number DM54S206W or DM74S206W
See Package 28

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absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S206	4.5	5.5	V
DM74S206	4.75	5.25	V
Temperature (T_A)			
DM54S206	−55	+125	°C
DM74S206	0	+70	°C

operating conditions

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Low Level Output Current (I_{OL})				16	mA
Width of Write Enable Pulse (t_W)					
DM54S206		50			ns
DM74S206		40			ns
Setup Time (t_{SETUP})					
Address to Write Enable		0			ns
Data to Write Enable		0			ns
Memory Enable to Write Enable		0			ns
Hold Time (t_{HOLD})					
Address from Write Enable		10			ns
Data from Write Enable		10			ns
Memory Enable from Write Enable		0			ns

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High-Level Input Voltage (V_{IH})		2			V
Low-Level Input Voltage (V_{IL})				0.8	V
Input clamp voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
High-Level Output Current (I_{OH})	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V				
	V_{OH} = 2.4V			40	μA
	V_{OH} = 5.5V			100	μA
Low-Level Output Voltage (V_{OL}) DM54S206 / DM74S206	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = Max			0.5 / 0.45	V
Input Current at Maximum Input Voltage (I_I)	V_{CC} = Max, V_I = 5.5V			1	mA
High-Level Input Current (I_{IH})	V_{CC} = Max, V_I = 2.7V			25	μA
Low-Level Input Current (I_{IL})	V_{CC} = Max, V_I = 0.5V			−250	μA
Supply Current (I_{CC})	V_{CC} = Max, Note 2		70	130	mA

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switching characteristics

All typical values are at V_{CC} = 5.0V, T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS	LIMITS						UNITS
		DM54S206			DM74S206			
		MIN	TYP	MAX	MIN	TYP	MAX	
Access Times from Address (t_{PLH})	C_L = 30 pF, R_L = 300Ω		38	80		38	60	ns
Access Times from Address (t_{PHL})			32	80		32	60	ns
Disable Time from Memory Enable (t_{PLH})			21	45		21	35	ns
Enable Time from Memory Enable (t_{PHL})			13	35		13	25	ns
Disable Time from Write Enable (t_{PLH})			20	50		20	40	ns
Sense-Recovery Time (t_{SR})			14	50		14	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for DM54S206 and across the 0°C to +70°C range for the DM74S206. All typicals are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: All voltage values are with respect to network ground terminal.

Note 4: I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.

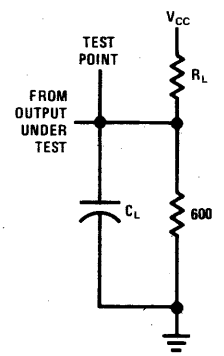
truth table

FUNCTION	INPUTS		OUTPUT
	MEMORY ENABLE†	WRITE ENABLE	
Write (Store Complement of Data)	L	L	H
Read	L	H	Stored Data
Inhibit	H	X	H

H = high level, L = low level, X = irrelevant

†For memory enable: L = all ME inputs low; H = one or more ME inputs high.

ac test circuit



C_L includes probe and jig capacitance.

MM2102A, MM2102AL family
1024-bit (1024 × 1) static random access memories

general description

The MM2102A family of high speed 1024 x 1-bit static random access read/write memories are manufactured using N-channel depletion-mode silicon gate technology. Static storage cells eliminate the need for clocks or refresh circuitry and the resultant cost associated with them.

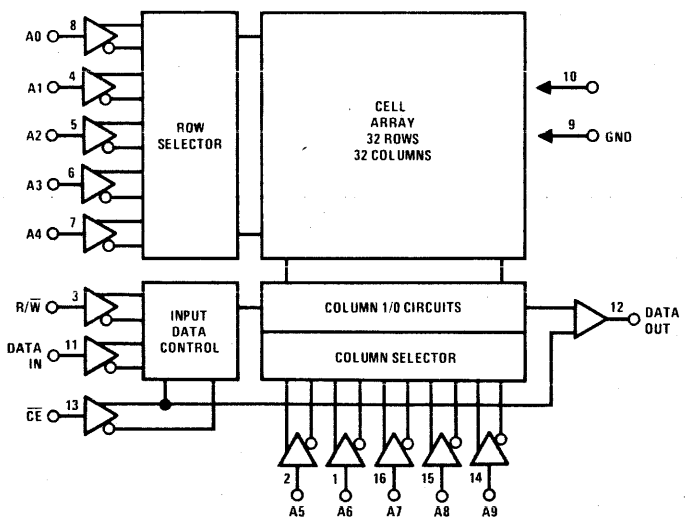
Low threshold silicon gate N-channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single 5V supply. The separate chip enable input ($\overline{CE}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus. Data in and data out have the same polarity.

In addition to the MM2102A, a low power version, the MM2102AL, is also available. This selection offers a maximum operating current of 33 mA and a guaranteed standby mode down to a power supply voltage of 1.5V.

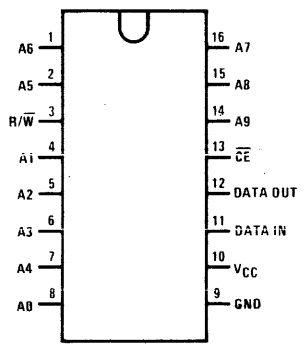
features

- Single 5V supply
- All inputs and outputs directly DTL/TTL compatible
- Static operation—no clocks or refresh
- TRI-STATE output for bus interface
- All inputs protected against static charge
- Access time down to 250 ns

block diagram

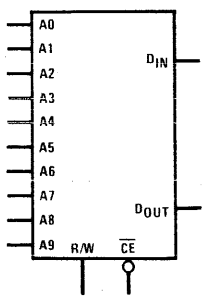


connection diagram



TOP VIEW

logic symbol



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absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.5V to +7V
Voltage at Any Pin	−0.5V to +7V
Storage Temperature	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C
Input Low Voltage	−0.5	0.8	V
Input High Voltage	2.0	V_{CC}	V

dc electrical characteristics T_A = 0°C to +70°C, V_{CC} = ±5%, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MM2102A, MM2102A-2, MM2102A-4		MM2102AL, MM2102A-2L, MM2102A-4L		UNITS
			MIN	MAX	MIN	MAX	
I_{LI}	Input Load Current	V_{IN} = 0 to 5.25V		10		10	μA
I_{LOH}	Output Leakage Current	$\overline{CE}$ = 2V, V_{OUT} = 2.4V		5		5	μA
I_{LOL}	Output Leakage Current	$\overline{CE}$ = 2V, V_{OUT} = 0.4V		−10		−10	μA
I_{CC}	Power Supply Current	All Inputs = 5.25V, Data Output Open, T_A = 25°C		50		31	mA
I_{CC}	Power Supply Current	All Inputs = 5.25V, Data Output Open, T_A = 0°C		55		33	mA
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −200 μA	2.4		2.4		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the device may be permanently damaged. They do not mean the device may be operated at these values.

ac electrical characteristics (With standard load) T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified.

SYMBOL	PARAMETER	MM2102A-2, MM2102A-2L		MM2102A, MM2102AL		MM2102A-4, MM2102A-4L		MM2102A-6, MM2102A-6L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE *(Figure 1)*										
t_{RC}	Read Cycle	250		350		450		650		ns
t_A	Access Time		250		350		450		650	ns
t_{CO}	Chip Enable to Output Time		100		150		200		200	ns
t_{OH1}	Previous Read Data Valid with Respect to Address	40		40		40		50		ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0		0		0		ns

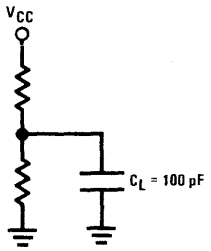
ac electrical characteristics (With standard load) T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified.

SYMBOL	PARAMETER	MM2102A-2, MM2102A-2L		MM2102A, MM2102AL		MM2102A-4, MM2102A-4L		MM2102A-6, MM2102A-6L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
WRITE CYCLE *(Figure 2)*										
t_{WC}	Write Cycle	250		350		450		650		ns
t_{AW}	Address to Write Set-Up	20		20		20		20		ns
t_{WP}	Write Pulse Width	100		150		200		200		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DW}	Date Set-Up Time	85		125		175		175		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{CW}	Chip Enable To Write Set-Up	100		150		200		200		ns

ac electrical characteristics $T_A = 25°C$, f = 1 MHz

SYMBOL	PARAMETER	LIMIT (pF)	
		TYP	MAX
CAPACITANCE [2]			
C_{IN}	Input Capacitance (All Inputs V_{IN} = 0V)	3	5
C_{OUT}	Output Capacitance, V_O = 0V	4	6

ac test circuit



switching time waveforms

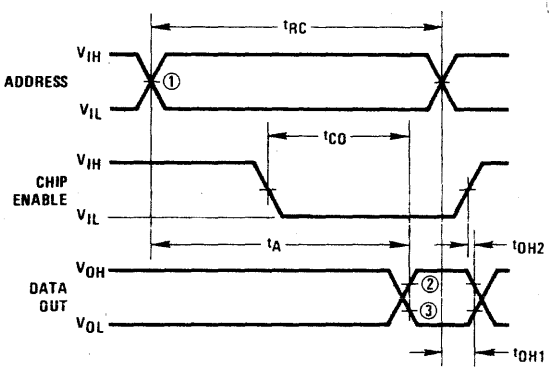


FIGURE 1. Read Cycle

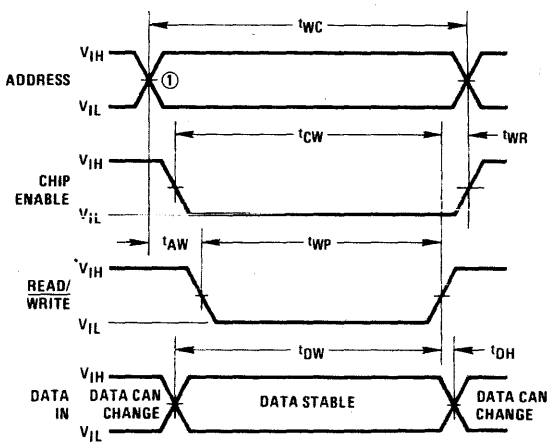


FIGURE 2. Write Cycle

Note ①: Input reference level for timing is 1.5V.
Note ②: V_{OH} = 2V is reference level for output high.
Note ③: V_{OL} = 0.8V is reference level for output low.
Note ④: Input rise and fall times are 10 ns.

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National Semiconductor

MM2114L Family
4096-Bit (1024 x 4) Static Random Access Memories

General Description

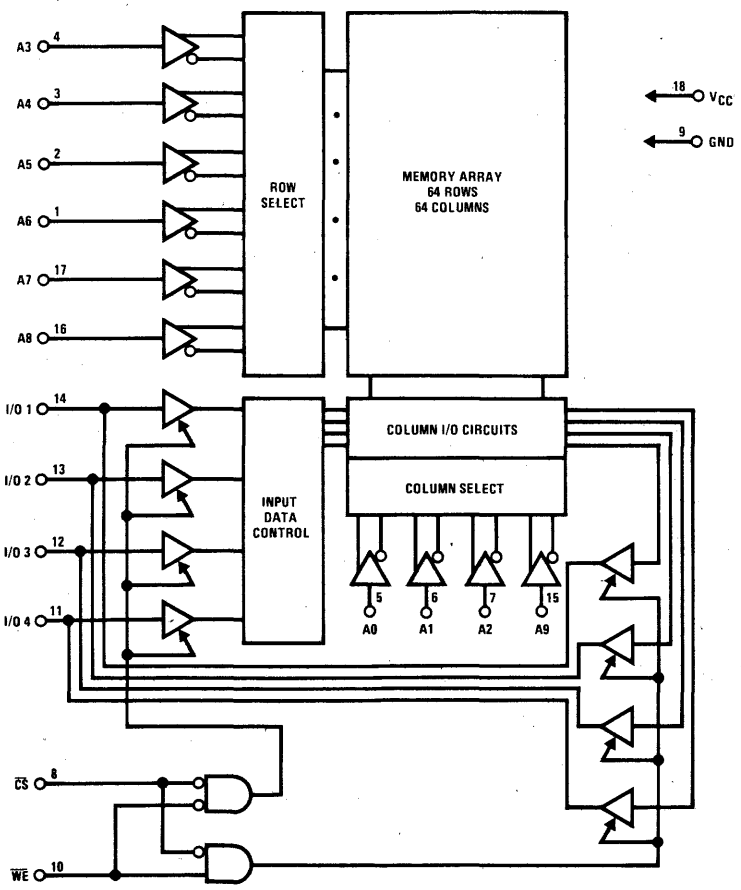
The MM2114L family of high speed 1024 x 4-bit static random access read/write memories are manufactured using N-channel depletion-mode silicon gate technology. Static storage cells eliminate the need for clocks or refresh circuitry and the resultant cost associated with them.

Low threshold silicon gate N-channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single 5V supply. The separate chip select input ($\overline{CS}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus. Data in and data out have the same polarity.

Features

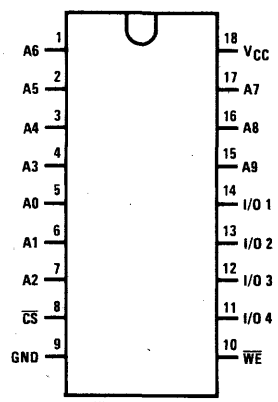
- Single 5V supply
- All inputs and outputs directly DTL/TTL compatible
- Static operation—no clocks or refresh
- TRI-STATE output for bus interface
- All inputs protected against static charge
- Access time down to 250 ns

Block Diagram



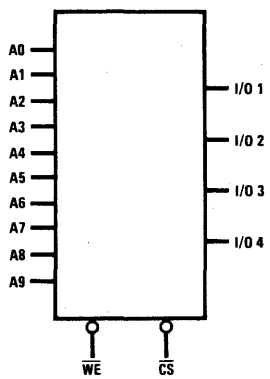
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	MODE
H	X	X	Hi-Z	Not Selected
L	L	L	L	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{OUT}	Read

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Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +7V
Storage Temperature	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{CC} = ±5%, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MM2114L MM2114L-3 MIN	MM2114L MM2114L-3 MAX	UNITS
I_{LI}	Input Lead Current	V_{IN} = 0 to 5.25V		10	μA
I_{LOH}	Output Leakage Current	$\overline{CE}$ = 2V, V_{OUT} = 2.4V		10	μA
I_{LOL}	Output Leakage Current	$\overline{CE}$ = 2V, V_{OUT} = 0.4V		−10	μA
I_{CC}	Power Supply Current	All Inputs = 5.25V, Data Output Open, T_A = 25°C		65	mA
I_{CC}	Power Supply Current	All Inputs = 5.25V, Data Output Open, T_A = 0°C		70	mA
V_{IH}	Logical "1" Input Voltage		−0.5	0.8	V
V_{IL}	Logical "0" Input Voltage		2.0	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −200 μA	2.4		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the device may be permanently damaged. They do not mean the device may be operated at these values.

AC Electrical Characteristics

(With standard load) T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified.

SYMBOL	PARAMETER	MM2114L MIN	MM2114L MAX	MM2114L-3 MIN	MM2114L-3 MAX	UNITS
READ CYCLE *(Figure 1)*						
t_{RC}	Read Cycle Time	450		300		ns
t_A	Access Time		450		300	ns
t_{CO}	Chip Enable to Output Valid		100		100	ns
t_{COT}	Output to Hi-Z from $\overline{CS}$	0	100	0	80	ns
t_{OHA}	Output Hold from Address Change	10		10		ns
WRITE CYCLE *(Figure 2)*						
t_{WC}	Write Cycle Time	450		300		ns
t_{WP}	Write Pulse Width	200		100		ns
t_{WR}	Write Recovery Time	0		0		ns
t_{DS}	Date Set-Up Time	200		150		ns
t_{DH}	Data Hold Time	0		0		ns
t_{WOT}	Output to Hi-Z from $\overline{WE}$	0	100	0	80	ns
t_{AW}	Address to Write Set-Up Time	0		0		ns
t_{WD}	Write Enable to Output Valid	0	150	0	150	ns

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AC Electrical Characteristics

$T_A = 25°C$, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
V_{PD}	V_{CC} in Stand-by		1.5			V
V_{CES}	$\overline{CE}$ Bias in Stand-by	$2 \leq V_{PD} \leq V_{CC(Max)}$	2.0			V
V_{CES}	$\overline{CE}$ Bias in Stand-by	$1.5 \leq V_{PD} \leq 2$	V_{PD}			V
I_{PD1}	Stand-by Current	All Inputs = V_{PD} = 1.5V		15		mA
I_{PD2}	Stand-by Current	All Inputs = V_{PD} = 2V		20		mA
t_{CP}	Chip Deselect to Stand-by Time		0			ns
t_R	Recovery Time (Note 6)		t_{RC}			ns
CAPACITANCE $T_A = 25°C$, f = 1 MHz, (Note 7)						
C_{IN}	Input Capacitance	All Inputs V_{IN} = 0V			5	pF
C_{OUT}	Output Capacitance	V_O = 0V			10	pF

Switching Time Waveforms

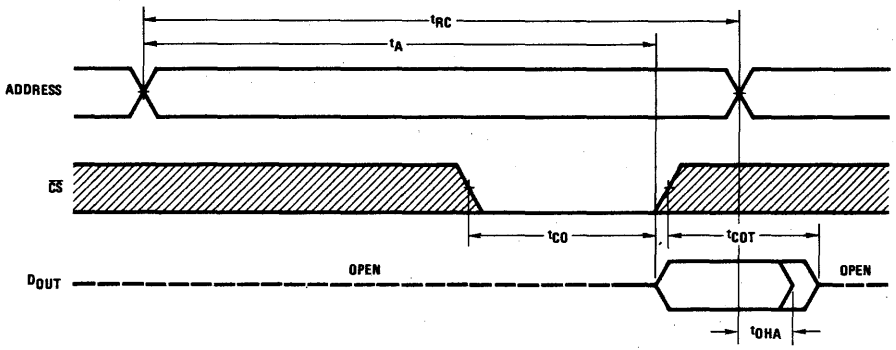


FIGURE 1. Read Cycle (Note 2)

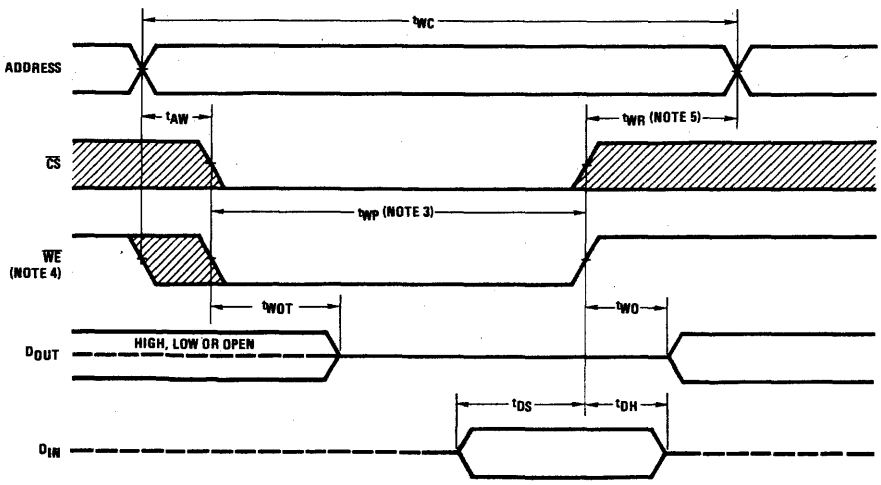
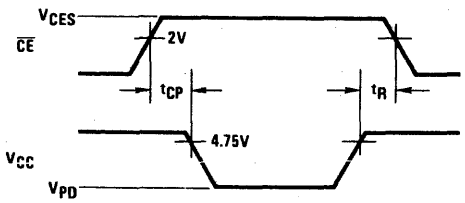


FIGURE 2. Write Cycle

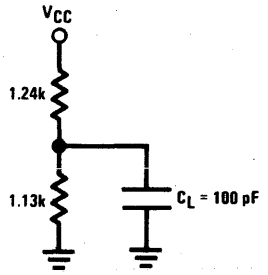
Note 2: $\overline{WE}$ is high for a Read Cycle.
Note 3: t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to $\overline{WE}$ going high.
Note 4: $\overline{WE}$ must be high during all address transitions.
Note 5: t_{WR} is referenced to the high transition of $\overline{WE}$.
Note 6: $t_R = t_{RC}$ = read cycle time.
Note 7: This parameter is guaranteed by periodic testing.

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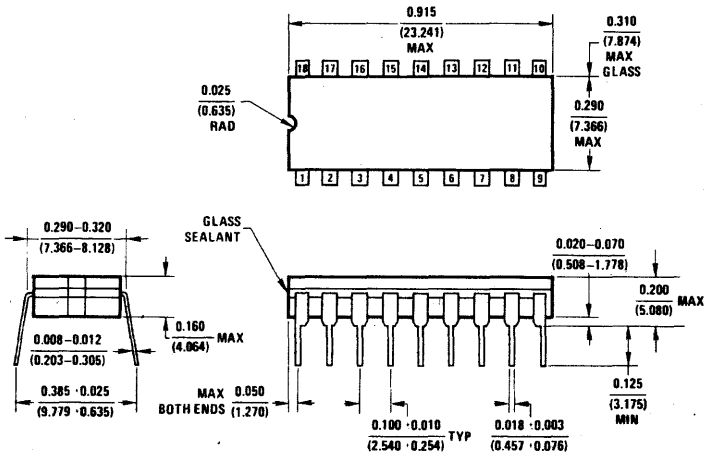
Standby Waveforms



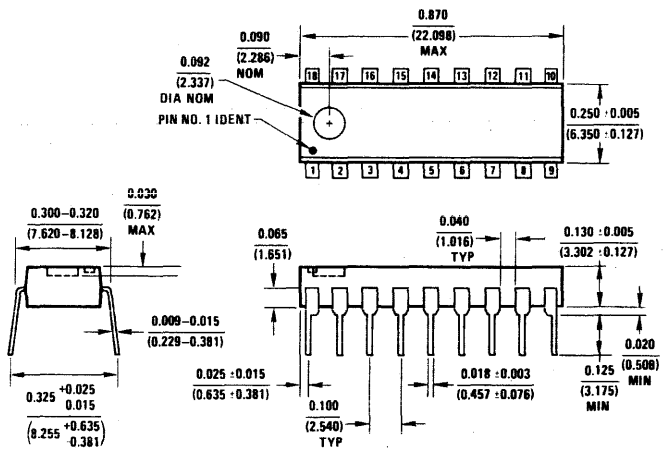
AC Test Circuit



Physical Dimensions inches (millimeters)



Cavity Dual-In-Line Package (J)
Order Number MM2114LJ
NS Package Number J18A



Molded Dual-In-Line Package (N)
Order Number MM2114LN
NS Package Number N18A

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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National Semiconductor

MM2316E 16,384-Bit Read Only Memory

general description

The MM2316E is a static MOS 16,384-bit read-only memory organized in a 2048-word-by-8-bit format. It is fabricated using N-channel enhancement and depletion-mode silicon-gate technology which provides complete DTL/TTL compatibility and single power-supply operation.

Three programmable chip selects controlling the TRI-STATE® outputs allow for memory expansion.

Programming of the memory array and chip-select active levels is accomplished by changing one mask during fabrication.

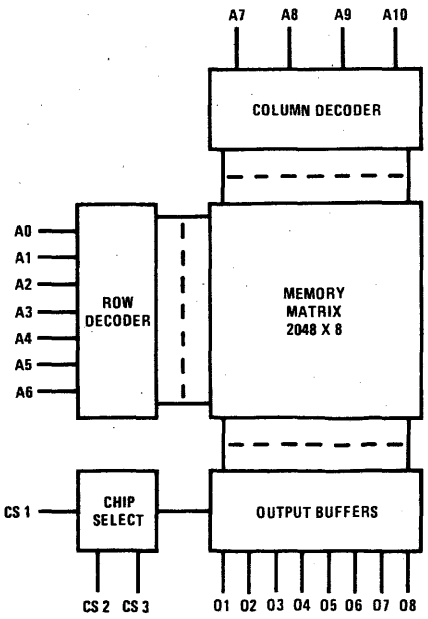
features

- Fully decoded
- Single 5V power supply
- Inputs and outputs TTL compatible
- Static operation
- TRI-STATE outputs for bus interface
- Programmable chip selects
- 2048 word by 8-bit organization
- Maximum access time—450 ns

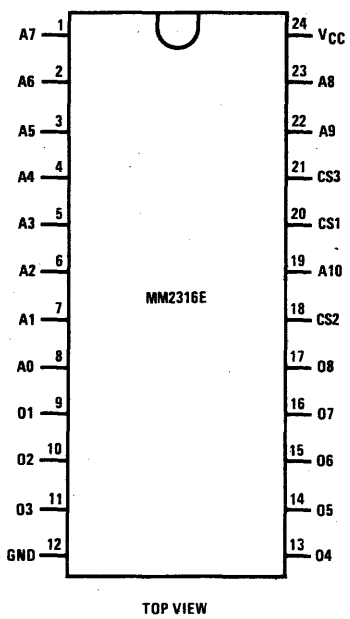
applications

- Microprogramming
- Control logic
- Table look-up

block and connection diagrams

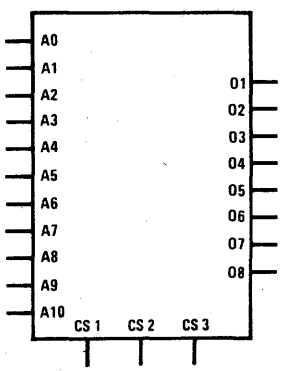


Dual-In-Line Package



TOP VIEW

logic symbol



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Absolute Maximum Ratings (Note 1)

Operating Temperature Range	0°C to +70°C	Voltage on Any Pin Relative to V_{BB}	−0.3V to +20V
Storage Temperature	−65°C to +150°C	($V_{SS} - V_{BB} \geq 4.5V$)	
Power Dissipation	1W	Lead Temperature (Soldering, 10 seconds)	300°C

Recommended DC Operating Conditions

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
T_A	Ambient Temperature	0	70	°C	
V_{DD}	Supply Voltages	10.8	13.2	V	2, 3
V_{CC}		4.5	5.5	V	2, 3
V_{SS}		0	0	V	2, 3
V_{BB}		−4.5	−5.5	V	2, 3
V_{IHC}	Input High Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	2.7	7.0	V	2
V_{IH}	Input High Voltage, A0–A6, DI	2.4	7.0	V	2
V_{IL}	Input Low Voltage, All Inputs	−1.0	0.8	V	2

DC Electrical Characteristics

$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$, (Notes 2 and 3)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD1}	**Operating Current**		35	mA	4
I_{CC1}	Average Power Supply Operating Current				5
I_{BB1}	($\overline{RAS}$, $\overline{CAS}$ Cycling; t_{RC} = 375 ns)		200	μA	
I_{DD2}	**Standby Current**		1.5	mA	
I_{CC2}	Power Supply Standby Current ($\overline{RAS}$ = V_{IHC},	−10	10	μA	
I_{BB2}	DO = High Impedance)		100	μA	
I_{DD3}	**Refresh Current**		25	mA	4
I_{CC3}	Average Power Supply Current, Refresh Mode	−10	10	μA	
I_{BB3}	($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 375 ns)		200	μA	
I_{DD4}	**Page Mode Current**		27	mA	4
I_{CC4}	Average Power Supply Current, Page Mode				5
I_{BB4}	($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling; t_{PC} = 225 ns)		200	μA	
$I_{I(L)}$	**Input Leakage**	−10	10	μA	
	Input Leakage Current, Any Input				
	(V_{BB} = −5V, $0V \leq V_{IN} \leq 7V$, All Other				
	Pins not Under Test = 0V)				
$I_{O(L)}$	**Output Leakage**	−10	10	μA	
	Output Leakage Current (DO is Disabled,				
	$0V \leq V_{OUT} \leq 5.5V$)				
	Output Levels				
V_{OH}	Output High Voltage (I_{OUT} = −5 mA)	2.4		V	
V_{OL}	Output Low Voltage (I_{OUT} = 4.2 mA)		0.4	V	
CAPACITANCE					
C_I	Input Capacitance A0–A6, DI		5	pF	6
C_C	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$		10	pF	6
C_O	Output Capacitance, DO		7	pF	6

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Recommended DC Operating Conditions" provides conditions for actual device operation.

Note 2: All voltages referenced to V_{SS}. When applying voltages to the device, V_{DD}, V_{CC} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Several cycles are required after power-up before proper device operation is achieved. Any 8 RAS cycles are adequate for this purpose.

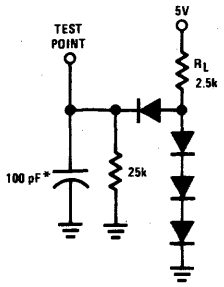
Note 4: I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate.

Note 5: I_{CC} depends on output load.

Note 6: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$. Capacitance is guaranteed by periodic testing.

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ac test circuit and switching time waveforms



*Includes jig capacitance

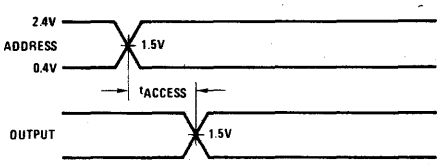


FIGURE 1. Access Time

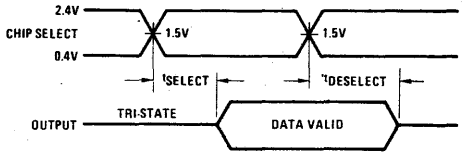


FIGURE 2. Output Enable and Disable

custom ROM programming

Custom ROM programs are submitted to National in three formats: paper tape, punched cards or truth table, with punched cards being the preferred. These programs are converted into machine language and outputted on a magnetic tape. This magnetic tape is used to make the programmable mask and the test tape. The wafers are tested at the wafer level. The wafer is then scribed and the good dice assembled. After assembly, the units are tested using the custom test tape to assure the correct output pattern for every address.

National has programs to convert NEGATIVE logic to POSITIVE or POSITIVE to NEGATIVE so ROMs can be entered in either logic, but the customer must specify which logic definition is used.

PROGRAMMING DEFINITIONS

Logic Definitions

NEGATIVE Logic: "0" = V_H = the more positive voltage. "1" = V_L = the more negative voltage.

POSITIVE Logic: "0" = V_L = the more negative voltage. "1" = V_H = the more positive voltage.

Input/Output Definitions

Address: A0 is the least significant input address.

Outputs: O1 is the least significant output.

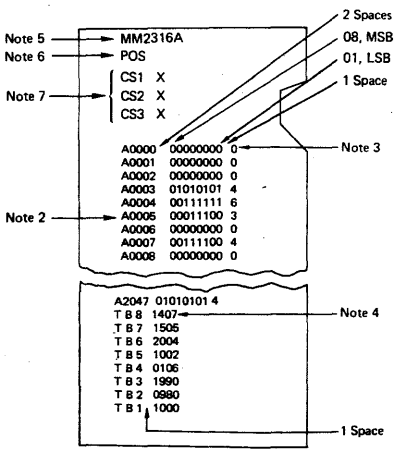
Custom ROM Programming

INFORMATION NEEDED

So that National can better serve its customers, the following information *must* be submitted with each ROM code.

National Semiconductor Corporation 2900 Semiconductor Dr., Santa Clara, CA 95051 Phone (408) 737-5000 TWX 910-339-9240			NATIONAL PART NUMBER
			ROM LETTER CODE (NATIONAL USE ONLY)
NAME			DATE
ADDRESS			CUSTOMER PRINT OR I.D. NO.
CITY		STATE ZIP	PURCHASE ORDER NO.
TELEPHONE	NAME OF PERSON NATIONAL CAN CONTACT (PRINT)	AUTHORIZED SIGNATURE	DATE

tape entry format (Note 1)



MM2316E

8-Bit Tape Format

Note 1: The code is a 7-bit ASCII code on 8 punch tape.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1" bits in the output word.

Note 4: The total number of "1" bits in each output column or bit position.

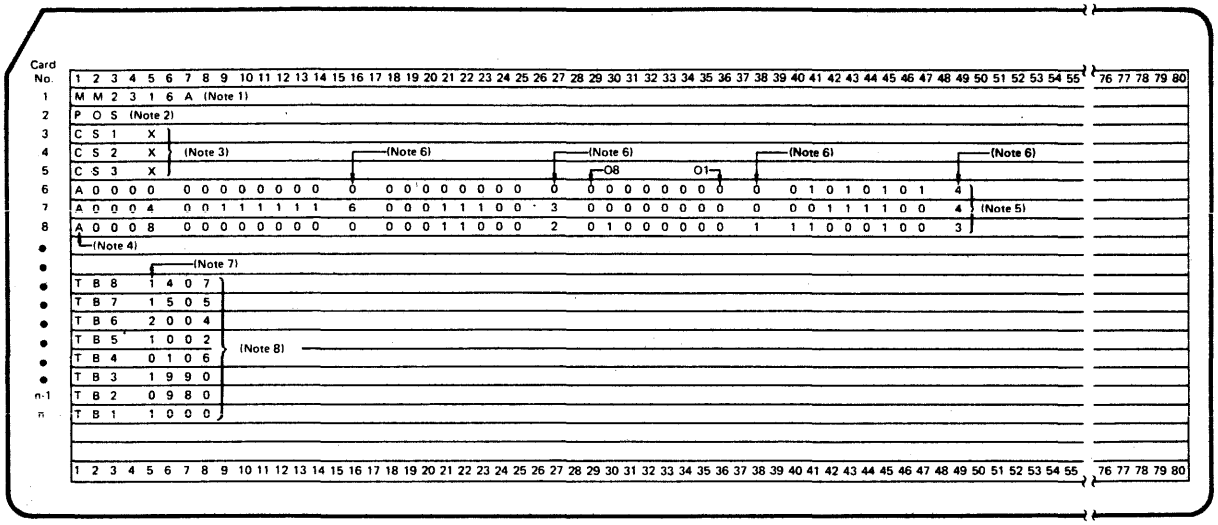
Note 5: Specify product type.

Note 6: Must type POS logic, or NEG logic depending on which is used. Logic on addresses, chip select and outputs must be the same (either POS or NEG).

Note 7: Specify the pattern necessary to select the ROM. (Indicate a "1" or "0" where X is shown).

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card entry format


Card No.
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 76 77 78 79 80
1 M M 2 3 1 6 A (Note 1)
2 P O S (Note 2)
3 C S 1 X
4 C S 2 X (Note 3)
5 C S 3 X
6 A 0 0 0

MM4270 TRI-SHARE™ extended temperature range 4096-bit dynamic random access read/write memory

general description

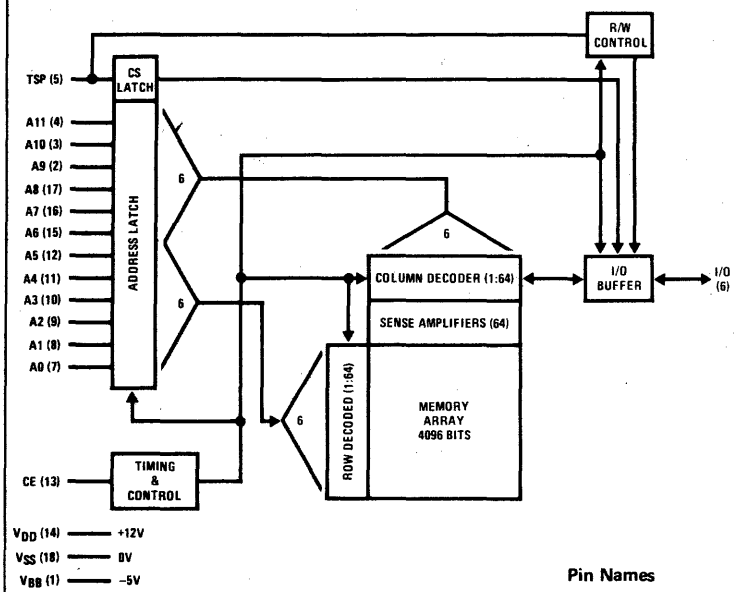
The MM4270 is a 4096-bit dynamic random access memory with TRI-SHARE. Because of this unique design feature, National is able to package a 4k device in an 18-pin dual-in-line package. The device is manufactured using N-channel silicon gate technology with a single transistor cell which provides higher density on a monolithic chip and thus lower cost.

The TRI-SHARE Port (TSP) is a multifunction input that, along with a common input/output, allows National to manufacture an 18-pin version of a 4k RAM. The functions controlled by the TSP are read/write, V_{CC}, and logical chip select. In order to understand how the TSP works, consider the timing diagrams. The state of the TSP at the leading edge of the chip enable clock determines whether the device is selected. If it is at a TTL high level, the chip is selected and the device goes into a read mode after chip enable goes high. This high level also performs a V_{CC} function in that it enables a reference voltage for a TTL high output. The supply for the output buffer is V_{DD}, not the TRI-SHARE Port; thus, no special driver is required. In order to perform a write, the TSP must be pulsed low after the minimum hold time and the appropriate data placed on the I/O. When the MM4270 goes into write, the output circuit is disabled. If the TSP is low at the start of the cycle, the memory is not selected but it will be refreshed if the chip enable clock is pulsed.

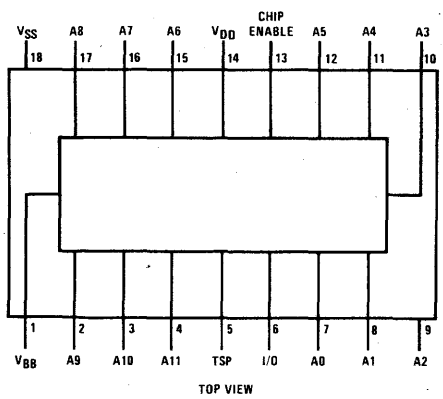
features

- 4096 x 1 bit organization
- Access time 270 ns maximum
- Cycle time 470 ns minimum
- TRI-SHARE port
- High memory density—18-pin package
- TTL compatible inputs (except chip enable)
- TRI-STATE® common input/output
- Registers on chip for addresses and chip select
- Two power supplies, +12V, −5V
- Simple read-modify-write operation

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Pin Names

A0–A11	Address Inputs*	V_{BB}	Power (−5V)
CE	Chip Enable	V_{DD}	Power (+12V)
TSP	TRI-SHARE Port	V_{SS}	Ground
I/O	$D_{IN}/\overline{D_{OUT}}$		

*Refresh Addess A0–A5

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absolute maximum ratings

Operating Temperature Range	−55°C to +85°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.0W

ac electrical characteristics

T_A = −55°C to +85°C, V_{DD} = 12V ±5%, V_{BB} (Note 2) = −5V ±10%, V_{SS} = 0V, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP(3)	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +0.6V, (Note 4)		110	200	μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, T_A = 25°C		20	50	mA
$I_{DD\,AV1}$	Average V_{DD} Current	T_A = 25°C, Cycle Time = 470 ns, t_{CE} = 300 ns		35	70	mA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns, *(Figure 4)*	−1.0		0.6	V
V_{IH}	Input High Voltage		2.2		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4			V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} current is to V_{SS}. The I_{BB} current is the sum of all leakage currents.

ac electrical characteristics T_A = −55°C to +85°C, V_{DD} = 12V ±5%, V_{BB} = −5V ±10%

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				1	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		100			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
t_{TC}	TRI-SHARE Port to CE Set-Up Time		0			ns
t_{TH}	TRI-SHARE Port Hold Time		50			ns
READ CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time	t_T = 20 ns	300		3000	ns
t_{CO}	CE Output Delay	C_{LOAD} = 50 pF, Load = One TTL Gate			250	ns
t_{ACC}	Address to Output Access	Ref 1 = 2.0V, Ref 0 = 0.8V			270	ns
t_{TL}	CE to TSP	$t_{ACC} = t_{AC} + t_{CO} + t_T$	0			ns

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ac electrical characteristics (Continued) $T_A = -55°C$ to $+85°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 10\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_{WI}	TSP to CE "OFF"		150			ns
t_{CW}	CE to TSP	$t_T = 20$ ns			85	ns
t_D	D_{IN} to CE "OFF"		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	TSP Pulse Width		50			ns

ac electrical characteristics (Continued) $T_A = -55°C$ to $+85°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 10\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		650			ns
t_{CRW}	CE Width During RMW		480		3000	ns
t_{WC}	TSP to CE "ON"	$t_T = 20$ ns	0			ns
t_{W2}	TSP to CE "OFF"	$C_{LOAD} = 50$ pF, Load = One TTL Gate	200			ns
t_{WP}	TSP Pulse Width	Ref 1 = 2.0V, Ref 0 = 0.8V	50			ns
t_D	D_{IN} to CE "OFF"	$t_{ACC} = t_{AC} + t_{CO} + t_T$	150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				250	ns
t_{ACC}	Access Time				270	ns
t_{WD}	TSP to Output High Impedance				50	ns
t_M	Modify Time		0			ns
CAPACITANCE (Note 1)						
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2	6	pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15	25	pF
$C_{I/O}$	Data I/O Capacitance	$V_{OUT} = 0V$		8	10	pF
C_{IN}	TSP Capacitance	$V_{IN} = V_{SS}$		5	6	pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

MM4280 4096-bit dynamic random access read/write memory with extended temperature range

general description

National's MM4280 is a 4096 word by 1 bit dynamic RAM. It incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

The MM4280 must be refreshed every 1 ms. This can be accomplished by performing a read cycle at each of the 64 row addresses (A0–A5). The chip select input can be either high or low for refresh. Addresses (A6–A11) must have a stable address during the refresh cycle. Any address is satisfactory as long as the address set-up and hold times are met. The chip select input can be either high or low for refresh.

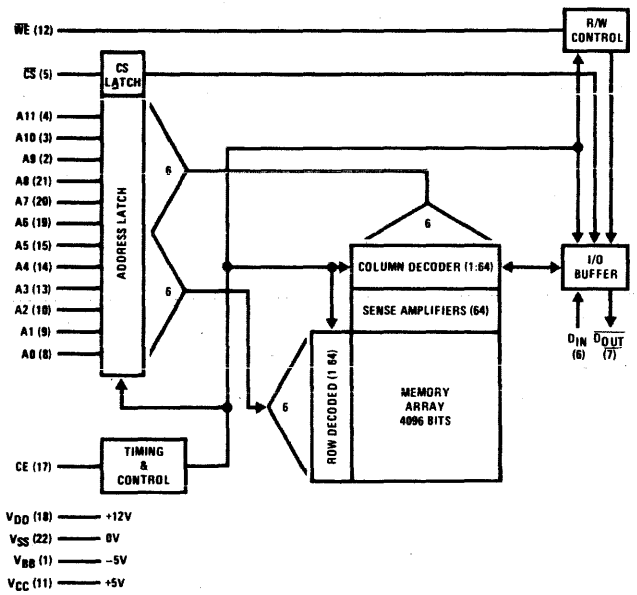
The MM4280 has been designed with minimum production costs as a prime criterion. It is fabricated using N-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The MM4280 uses a single transistor cell to minimize the device area.

The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance memory device.

features

- Extended temperature range: −55°C to +85°C
- Organization: 4096 x 1
- Access time 270 ns maximum
- Cycle time 470 ns minimum
- Easy system interface
  - One high voltage input—chip enable
  - TTL compatible—all other inputs and outputs
- Address registers on-chip
- TRI-STATE® output
- Simple read-modify-write operation
- Industry standard pin configuration

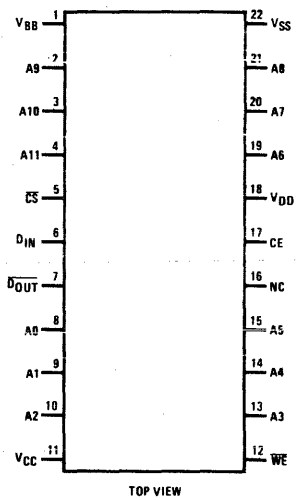
block diagram



Memory Inverts From Data In to Data Out

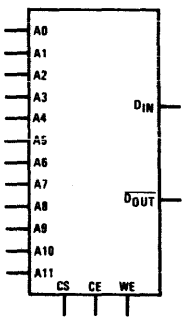
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



Pin Numbers

A0–A11	Address Inputs *	V_{BB}	Power (−5V)
CE	Chip Enable	V_{CC}	Power (+5V)
$\overline{CS}$	Chip Select	V_{DD}	Power (+12V)
D_{IN}	Data Input	V_{SS}	Ground
$\overline{D_{OUT}}$	Data Output	$\overline{WE}$	Write Enable
NC	Not Connected		

* Refresh Address A0–A5

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absolute maximum ratings (Note 1)

Operating Temperature Range	−55°C to +85°C
Storage Temperature	−65°C to +150°C
Voltage on any Pin Relative to V_{BB} ($V_{SS} - V_{BB} \geq 4.5V$)	−0.3V to +20V
Power Dissipation	1.25W

dc electrical characteristics

T_A = −55°C to +85°C, V_{DD} = 12V ±5%, V_{CC} = 5V ±5%, V_{BB} (Note 2) = −5V ±10%, V_{SS} = 0V, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to 0.6V, (Note 4)		110	200	μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, T_A = 25°C		20	50	mA
I_{DDAV1}	Average V_{DD} Current	Cycle Time = 470 ns, t_{CE} = 300 ns		35	70	mA
I_{CC1}	V_{CC} Supply Current During CE "OFF"	CE = V_{ILC} or $\overline{CS}$ = V_{IH} (Note 5)		0.01	10	μA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns	−1.0		0.6	V
V_{IH}	Input High Voltage		2.2		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA	0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2 mA	2.4		V_{CC}	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages referenced to V_{SS} and V_{BB} must be applied before and removed after other supply voltages.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.

Note 5: During CE "ON" V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

ac electrical characteristics T_A = −55°C to +85°C, V_{DD} = 12V ±5%, V_{CC} = 5V ±5%, V_{BB} = −5V ±10%

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				1	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		100			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
READ CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_{CO}	CE Output Delay	C_{LOAD} = 50 pF, Load = 1 TTL Gate, Ref = 2V,			250	ns
t_{ACC}	Address to Output Access	$t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$			270	ns
t_{WL}	CE to $\overline{WE}$		0			ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns

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ac electrical characteristics (Continued)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{CW}	CE to $\overline{WE}$	t_T = 20 ns	130			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns

ac electrical characteristics (Continued) $T_A = -55°C$ to $+85°C$, $V_{DD} = 12V \pm 5V \pm 5\%$, $V_{BB} = -5V \pm 10\%$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read/Modify/Write (RMW) Cycle Time		590			ns
t_{CRW}	CE Width During RMW		420		3000	ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{WP}	$\overline{WE}$ Pulse Width	t_T = 20 ns, C_{LOAD} = 50 pF, Load = 1 TTL Gate,	50			ns
t_D	D_{IN} to CE Set-Up	Ref = 2V, $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$	150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				250	ns
t_{WO}	$\overline{WE}$ to $\overline{D_{OUT}}$ Invalid		0			ns
t_{ACC}	Access Time				270	ns
CAPACITANCE (Note 1) $T_A = 25°C$						
C_{AD}	Address Capacitance, CS	$V_{IN} = V_{SS}$		2	6	pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15	25	pF
C_{OUT}	Data Output Capacitance	$V_{OUT} = 0V$		5	10	pF
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	$V_{IN} = V_{SS}$		4	6	pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

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MM5269 1024-bit (256 × 4) fully decoded static RAM with on chip registers

general description

The National MM5269 is a 256 word x 4 bit Static Random Access Memory device fabricated using N-Channel enhancement mode Silicon Gate technology. Static storage cells eliminate the need for refresh and the additional peripheral circuitry associated with refresh. Data in and data out have the same polarity.

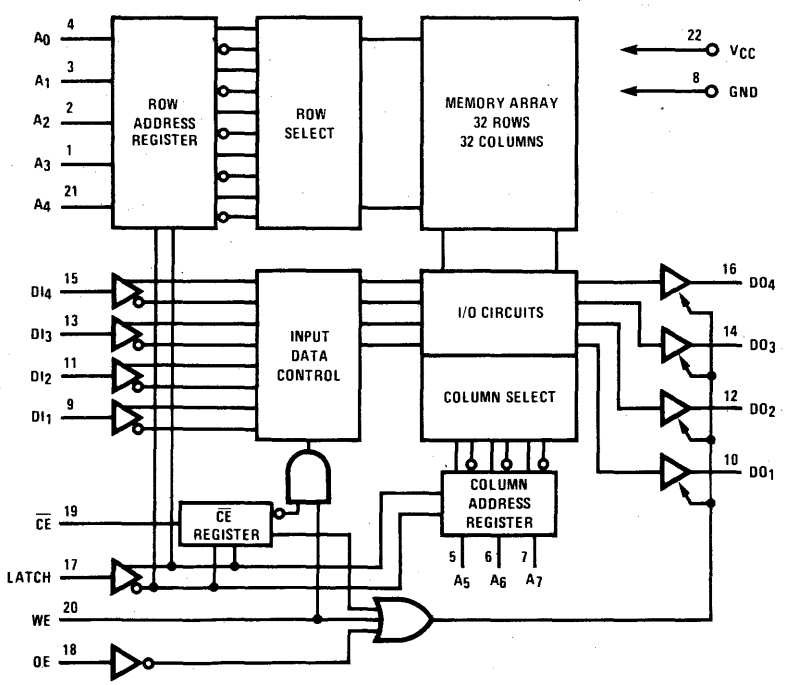
The MM5269 is fully TTL compatible including inputs, outputs and power supply. The chip enable input allows memory expansion and the address latch feature eliminates the need for external address registers. The output enable is provided for systems which use a common input/output data bus. All of the features of this memory device can be combined to make a low cost, high performance and easy to manufacture memory system. System design costs are also minimized because of the ease-of-use of the MM5269.

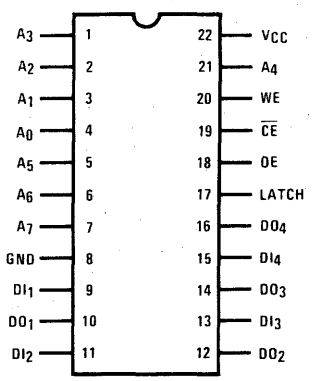
National's Silicon Gate process provides protection against contamination and permits the use of low cost Epoxy B packaging.

features

- Organization 256 Words by 4 Bits
- Access Time – 0.5 to 1.0 μs
- On Chip Address and Chip Enable Registers
- Directly TTL Compatible – All Inputs and Outputs
- Single +5 V Power Supply
- Tri-State ® Output – OR-Tie Capability
- Output Enable for Common Data Bus Systems
- Static Memory – No Refresh Required
- Packaged in a 22 Pin Epoxy B Dual-In-Line

block and connection diagrams





Order Number MM5269D
See Package 5
Order Number MM5269N
See Package 17

absolute maximum ratings

Voltage at Any Pin	-0.5 V to +7.0 V
Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Power Dissipation	1 Watt
Lead Temperature (10 s)	300°C

dc electrical characteristics (V_{CC} = 5.0 V ± 5%, 0°C ≤ T_A ≤ +70°C)

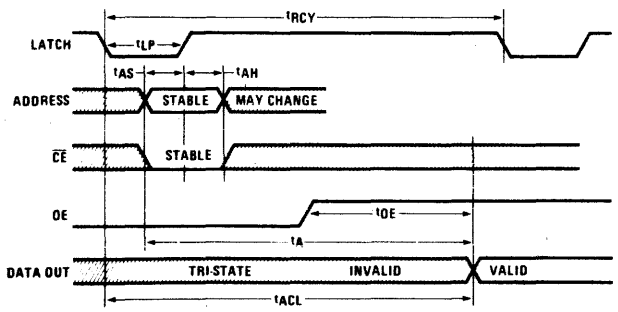
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC}	V	
V_{IL}	Logic "0" Input Voltage	-0.5		0.65	V	
V_{OH}	Logic "1" Output Voltage	2.2			V	I_{OH} = -150 μA
V_{OL}	Logic "0" Output Voltage			0.45	V	I_{OL} = 2.0 mA
I_{LI}	Input Load Current			10	μA	0 V ≤ V_{IN} ≤ 5.0 V
I_{LOH}	Output Leakage Current			15	μA	$\overline{CE}$ = 2.2 V, V_O = 4.0 V
I_{LOL}	Output Leakage Current			-50	μA	$\overline{CE}$ = 2.2 V, V_O = 0.45 V
I_{CC}	Power Supply Current			70	mA	V_{IN} = 5.25 V, I_O = 0 mA, T_A = 0°C

ac electrical characteristics (V_{CC} = 5.0 V ± 5%, 0°C ≤ T_A ≤ +70°C)

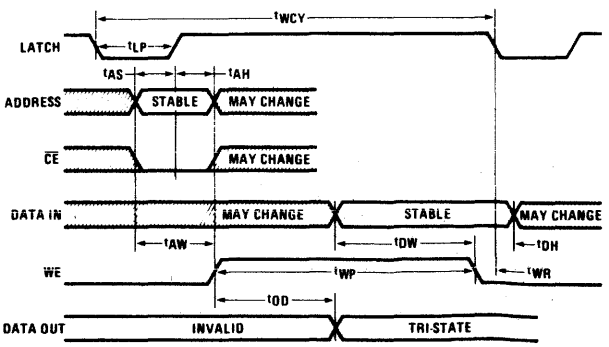
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	1,000			ns	
t_A or t_{ACL}	Access Time			1,000	ns	Input Pulse Levels: +0.65 to +2.2 V Input Pulse Rise and Fall Times: 20 ns
t_{OE}	Output Enable to Output Time			500	ns	Timing Measurement Reference Level: 1.5 V
t_{LP}	Latch Pulse Width	200			ns	Output Load: 1 TTL Gate and C_L = 100 pF
t_{AS}	ADD & $\overline{CE}$ to Latch Setup Time	100			ns	
t_{AH}	ADD & $\overline{CE}$ to Latch Hold Time	100			ns	
WRITE CYCLE						
t_{WCY}	Write Cycle	1,000			ns	
t_{AW}	Address and CE to Write Setup Time	200			ns	
t_{WP}	Write Pulse Width	650			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{WR}	Write Recovery Time	50			ns	Input Pulse Rise and Fall Times: 20 ns
t_{OD}	Write to Output Disable Time			400	ns	Timing Measurement Reference Level: 1.5 V
t_{DW}	Data Setup Time	350			ns	Output Load: 1 TTL Gate and C_L = 100 pF
t_{DH}	Data Hold Time	100			ns	
t_{CW}	Chip Enable to Write	750			ns	
t_{LP}	Latch Pulse Width	200			ns	
t_{AS}	Add & CE to Latch Setup Time	100			ns	
t_{AH}	Add & CE to Latch Hold Time	100			ns	

switching time waveforms

READ CYCLE (WE = "0")



WRITE CYCLE



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National Semiconductor

AUGUST 1977

MM5257 4096x1 Static Random Access Memory

General Description

The MM5257 is a 4096 word by 1-bit static random access memory fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

The separate chip enable input ($\overline{CE}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus.

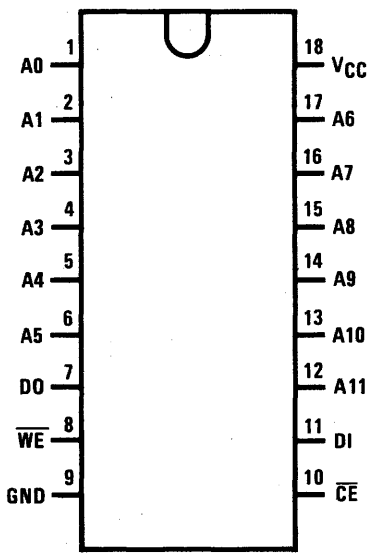
The output is held in a high impedance state during write to simplify common I/O applications.

Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Low power—200 mW typical
- High speed—250 ns typical
- TRI-STATE output for bus interface
- Separate Data In and Data Out pins
- Single +5V supply
- Standard 18-pin dual-in-line package

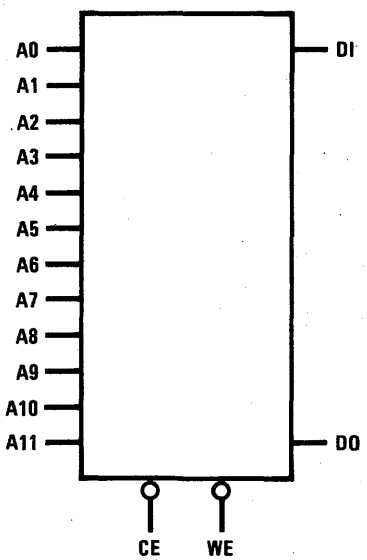
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



Truth Table

$\overline{CE}$	$\overline{WE}$	DI	D_{OUT}	MODE
H	X	X	Hi-Z	Not Selected
L	L	H	Hi-Z	Write 1
L	L	L	Hi-Z	Write 0
L	H	X	D_{OUT}	Read

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Functional Description

Two pins control the operation of the MM5257. Chip Enable ($\overline{CE}$) enables write and read operations and controls TRI-STATING of the data-output buffer. Write Enable ($\overline{WE}$) chooses between READ and WRITE modes and also controls output TRI-STATING. The truth table details the states produced by combinations of the $\overline{CE}$ and $\overline{WE}$ controls.

READ-cycle timing is shown in the section on Switching Time Waveforms. $\overline{WE}$ is kept high. Independent of $\overline{CE}$, any change in address code causes new data to be fetched and brought to the output buffer. $\overline{CE}$ must be low, however, for the output buffer to be enabled and transfer the data to the output pin.

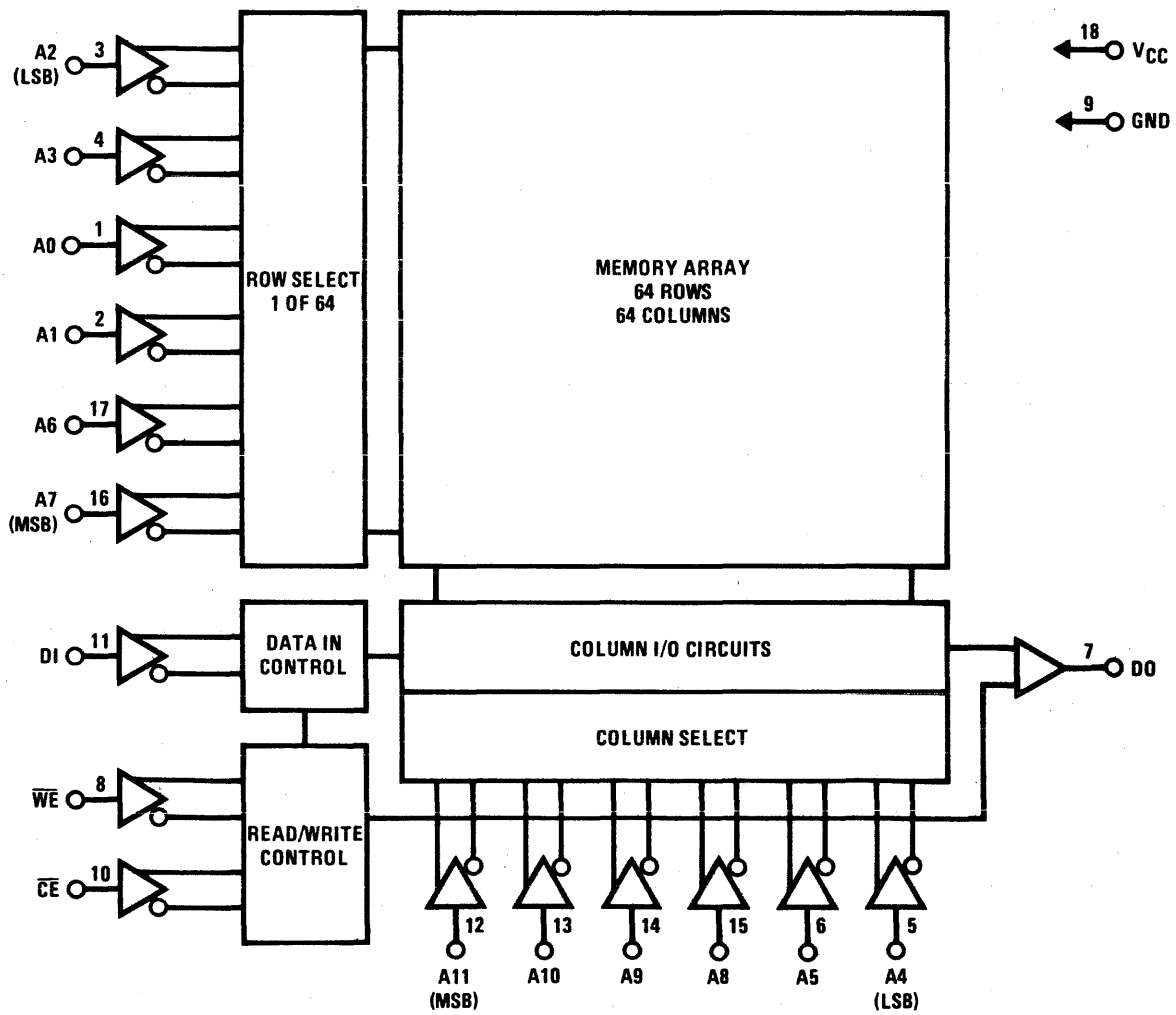
Address access time, t_A, is the time required for an address change to produce new data at the output pin, assuming $\overline{CE}$ has enabled the output buffer prior to data arrival. Chip Enable-to-output delay, t_{CO}, is the time required for $\overline{CE}$ to enable the output buffer and transfer previously fetched data to the output pin. Operation with $\overline{CE}$ continuously held low is permissible.

WRITE-cycle timing is shown in the section on Switching Time Waveforms. Writing occurs only during the time both $\overline{CE}$ and $\overline{WE}$ are low. Minimum write-pulse width, t_{WP}, refers to this simultaneous low region. Data set-up and hold times are measured with respect to whichever control first rises. Successive write operations may be performed with $\overline{CE}$ continuously held low. $\overline{WE}$ then is used to terminate WRITE between address changes. Alternatively, $\overline{WE}$ may be held low for successive WRITES and $\overline{CE}$ used for WRITE interruption between address change.

In any event, either $\overline{WE}$ or $\overline{CE}$ (or both) must be high during address transitions to prevent erroneous WRITE.

Stand-by operation allows data to be maintained with approximately 50% less operating current. The 2 requirements to guarantee data retention are: a) the power supply voltage must meet the condition $V_{CC} \geq 1.5V$, and b) $\overline{CE}$ must be controlled; to disable the chip prior to reducing V_{CC}, to keep it disabled during the time V_{CC} is reduced, and to maintain the disabled state long enough after V_{CC} is increased to normal for the chip to recover. These requirements are shown by the stand-by waveforms and characteristics.

Block Diagram



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Absolute Maximum Ratings

Voltage on Any Pin Relative to V_{SS}	−0.3V to +7V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Short-Circuit Output Current	50 mA
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
V_{IH}	Logical "1" Input Voltage		2.0		V_{CC}	V
V_{IL}	Logical "0" Input Voltage		−0.5		0.8	V
V_{OH}	Logical "1" Output Voltage	$I_{OH} = -200\ \mu A$	2.4			V
V_{OL}	Logical "0" Output Voltage	$I_{OL} = 2.1$ mA			0.4	V
I_{LI}	Input Load Current	$V_{IN} = 0$ to 5.25V	−10		10	μA
I_{LO}	Output Leakage Current	$V_O = 4V$ to 0.4V, $\overline{CE} = V_{IH}$	−10		10	μA
I_{CC}	Power Supply Current	All Inputs = 5.25V		35		mA

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, (Note 2)

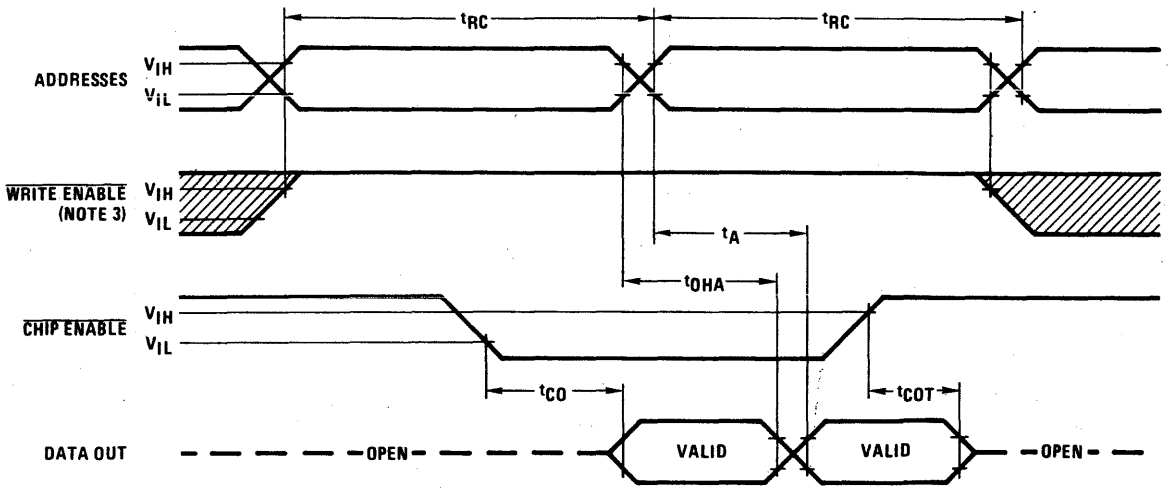
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
READ CYCLE						
t_{RC}	Read Cycle Time	$\overline{WE} = V_{IH}$		250		ns
t_A	Access Time			250		ns
t_{CO}	Chip Enable to Output Valid			85		ns
t_{COT}	Chip Enable to Output TRI-STATE			60		ns
t_{OHA}	Output Hold from Address Change			100		ns
WRITE CYCLE						
t_{WC}	Write Cycle Time			250		ns
t_{AW}	Address to Write Set-Up Time			0		ns
t_{WP}	Write Pulse Width			200		ns
t_{WR}	Write Recovery Time			0		ns
t_{DS}	Data Set-Up Time			85		ns
t_{DH}	Data Hold Time			0		ns
t_{WOT}	Write Enable to Output TRI-STATE			80		ns
t_{WO}	Write Enable to Output Valid			70		ns

Note 1: Typical values at $T_A = 25°C$.

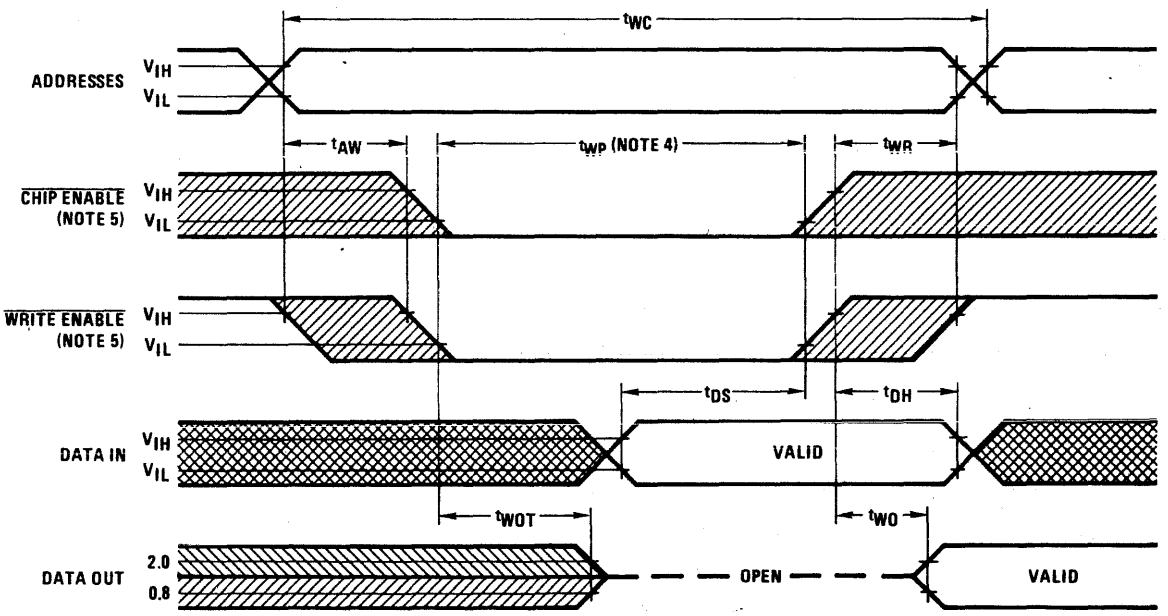
Note 2: All input transitions $\leq$ 10 ns. Timing referenced to $V_{IL(MAX)}$ or $V_{IH(MIN)}$ for inputs, 0.8V and 2V for output. For test purposes, input levels should swing between 0V and 3V. Output load = 1 TTL gate and $C_L = 50$ pF.

Switching Time Waveforms

Read Cycle



Write Cycle



Note 3: $\overline{WE}$ is high during a read cycle ($\overline{WE} \geq V_{IH(MIN)}$).

Note 4: t_{WP} defines the period when both $\overline{CE}$ and $\overline{WE}$ are low. t_{AW} is referenced to the later of $\overline{CE}$ or $\overline{WE}$ going low while t_{DS}, t_{DH} and t_{WR} are referenced to the earlier of $\overline{CE}$ or $\overline{WE}$ going high. t_{WOT} and t_{WO} are referenced to $\overline{WE}$ with $\overline{CE}$ low.

Note 5: Either $\overline{WE}$ or $\overline{CE}$ (or both) must be high during address transitions to prevent erroneous write.

National Semiconductor

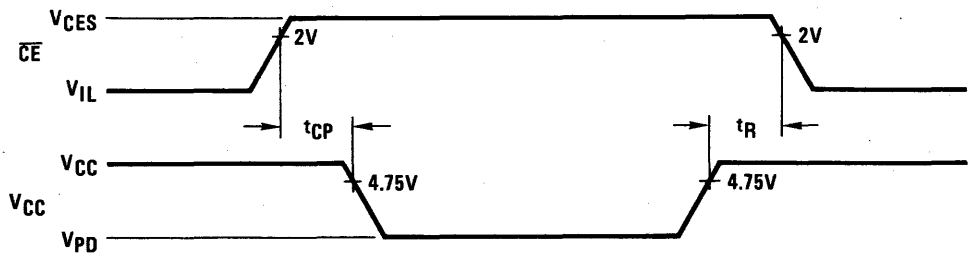
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Standby Characteristics $T_A = 0°C$ to $+70°C$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
V_{PD}	V_{CC} in Stand-by		1.5			V
V_{CES}	$\overline{CE}$ Bias in Stand-by	$2 \leq V_{PD} \leq V_{CC(Max)}$	2.0			V
V_{CES}	$\overline{CE}$ Bias in Stand-by	$1.5 \leq V_{PD} \leq 2$	V_{PD}			V
I_{PD1}	Stand-by Current	All Inputs = V_{PD} = 1.5V		15		mA
I_{PD2}	Stand-by Current	All Inputs = V_{PD} = 2V		20		mA
t_{CP}	Chip Deselect to Stand-by Time		0			ns
t_R	Recovery Time (Note 6)		t_{RC}			ns
CAPACITANCE $T_A = 25°C$, f = 1 MHz, (Note 7)						
C_{IN}	Input Capacitance	All Inputs V_{IN} = 0V			5	pF
C_{OUT}	Output Capacitance	V_O = 0V			10	pF

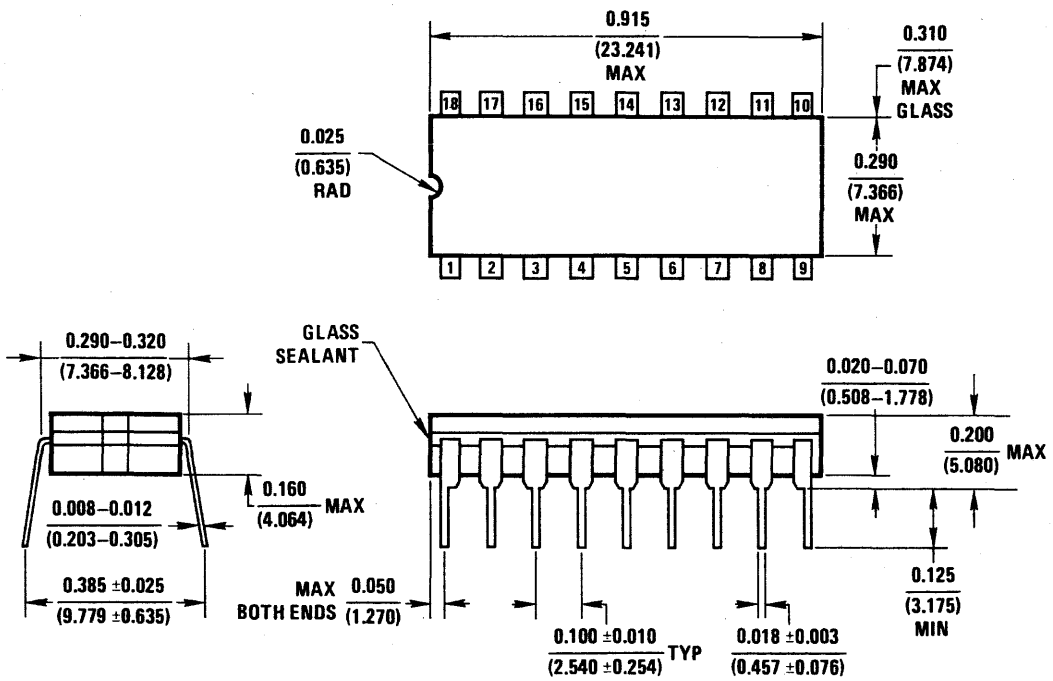
Note 6: $t_R = t_{RC}$ = read cycle time.
Note 7: This parameter is guaranteed by periodic testing.

Standby Waveforms



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Physical Dimensions inches (millimeters)



Cavity Dual-In-Line Package (J)
Order Number MM5257J
NS Package Number J18A

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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MOS RAMs

MM5270 TRI-SHARE™ 4096-bit fully decoded dynamic random access read/write memory

general description

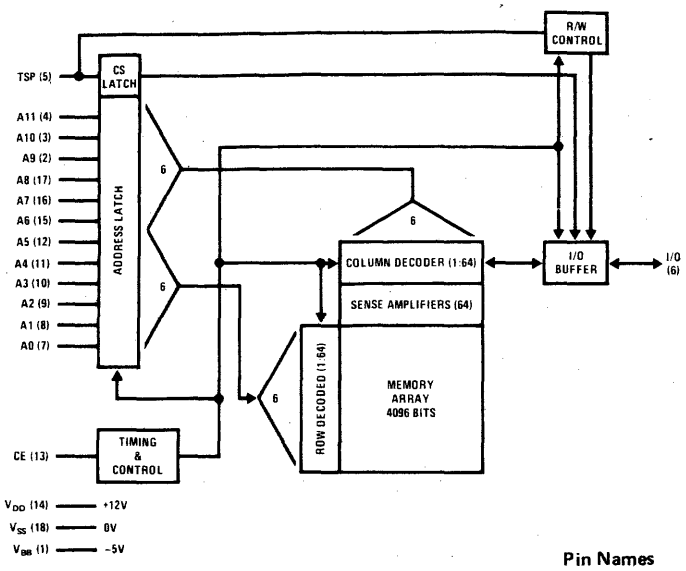
The MM5270 is a 4096-bit dynamic random access memory with TRI-SHARE. Because of this unique design feature, National is able to package a 4k device in an 18-pin dual-in-line package. The device is manufactured using N-channel silicon gate technology with a single transistor cell which provides higher density on a monolithic chip and thus lower cost.

The TRI-SHARE Port (TSP) is a multifunction input that, along with a common input/output, allows National to manufacture an 18-pin version of a 4k RAM. The functions controlled by the TSP are read/write, V_{CC}, and logical chip select. In order to understand how the TSP works, consider the timing diagrams. The state of the TSP at the leading edge of the chip enable clock determines whether the device is selected. If it is at a TTL high level, the chip is selected and the device goes into a read mode after chip enable goes high. This high level also performs a V_{CC} function in that it enables a reference voltage for a TTL high output. The supply for the output buffer is V_{DD}, not the TRI-SHARE Port; thus, no special driver is required. In order to perform a write, the TSP must be pulsed low after the minimum hold time and the appropriate data placed on the I/O. When the MM5270 goes into write, the output circuit is disabled. If the TSP is low at the start of the cycle, the memory is not selected but it will be refreshed if the chip enable clock is pulsed.

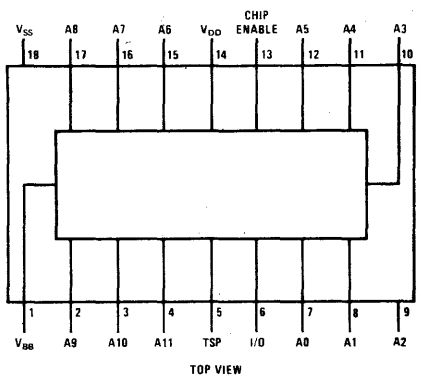
features

- 4096 x 1 bit organization
- Access time 200 ns maximum
- Cycle time 400 ns minimum
- TRI-SHARE port
- High memory density—18-pin package
- TTL compatible inputs (except chip enable)
- TRI-STATE® common input/output
- Registers on chip for addresses and chip select
- Two power supplies, +12V, −5V
- Simple read-modify-write operation

block and connection diagrams



Dual-In-Line Package



Order Number MM5270D
See Package 4

Pin Names

A0–A11	Address Inputs*	V_{BB}	Power (−5V)
CE	Chip Enable	V_{DD}	Power (+12V)
TSP	TRI-SHARE Port	V_{SS}	Ground
I/O	D_{IN}/D_{OUT}		

*Refresh Addess A0–A5

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absolute maximum ratings (Note 1)

Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.0W

dc electrical characteristics

T_A = 0°C to +70°C, V_{DD} = +12V ±5%, V_{BB} (Note 2) = −5V ±5%, V_{SS} = 0V, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (3)	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
I_{LO}	Output Leakage Current Up For High Impedance State	CE = V_{ILC}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +0.6V, (Note 4)		110		μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, T_A = 25°C		20		mA
$I_{DD\ AV1}$	Average V_{DD} Current	T_A = 25°C, Cycle Time = 400 ns, t_{CE} = 230 ns		35		mA
$I_{DD\ AV2}$	Average V_{DD} Current	T_A = 25°C, Cycle Time = 1000 ns, t_{CE} = 230 ns		15		mA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns, (*Figure 4*)	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4			V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} current is to V_{SS}. The I_{BB} current is the sum of all leakage currents.

ac electrical characteristics T_A = 0°C to +70°C, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		50			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
t_{TC}	TRI-SHARE Port to CE Set-Up Time		0			ns
t_{TH}	TRI-SHARE Port Hold Time		50			ns
READ CYCLE						
t_{CY}	Cycle Time	t_T = 20 ns	400			ns
t_{CE}	CE "ON" Time	C_{LOAD} = 50 pF, Load = One TTL Gate	230		3000	ns
t_{CO}	CE Output Delay	Ref 1 = 2.0V, Ref 0 = 0.8V			180	ns
t_{ACC}	Address to Output Access	$t_{ACC} = t_{AC} + t_{CO} + t_T$			200	ns
t_{TL}	CE to TSP		0			ns

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ac electrical characteristics (con't) $T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		400			ns
t_{CE}	CE "ON" Time		230		3000	ns
t_{WI}	TSP to CE "OFF"		150			ns
t_{CW}	CE to TSP	$t_T = 20$ ns			85	ns
t_D	D_{IN} to CE "OFF"		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	TSP Pulse Width		50			ns

ac electrical characteristics (con't) $T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		580			ns
t_{CRW}	CE Width During RMW		410		3000	ns
t_{WC}	TSP to CE "ON"	$t_T = 20$ ns	0			ns
t_{W2}	TSP to CE "OFF"	$C_{LOAD} = 50$ pF, Load = One TTL Gate	200			ns
t_{WP}	TSP Pulse Width	Ref 1 - 2.0V, Ref 0 = 0.8V	50			ns
t_D	D_{IN} to CE "OFF"	$t_{ACC} = t_{AC} + t_{CO} + t_T$	150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				180	ns
t_{ACC}	Access Time				200	ns
t_{WD}	TSP to Output High Impedance				50	ns
t_M	Modify Time		0			ns
CAPACITANCE (Note 1)						
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15		pF
$C_{I/O}$	Data I/O Capacitance	$V_{OUT} = 0V$		8		pF
C_{IN}	TSP Capacitance	$V_{IN} = V_{SS}$		5		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

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MM5270A TRI-SHARE™ 4096-bit fully decoded dynamic random access read/write memory

general description

The MM5270A is a 4096-bit dynamic random access memory with TRI-SHARE. Because of this unique design feature, National is able to package a 4k device in an 18-pin dual-in-line package. The device is manufactured using N-channel silicon gate technology with a single transistor cell which provides higher density on a monolithic chip and thus lower cost.

The TRI-SHARE Port (TSP) is a multifunction input that, along with a common input/output, allows National to manufacture an 18-pin version of a 4k RAM. The functions controlled by the TSP are read/write, V_{CC}, and logical chip select. In order to understand how the TSP works, consider the timing diagrams. The state of the TSP at the leading edge of the chip enable clock determines whether the device is selected. If it is at a TTL high level, the chip is selected and the device goes into a read mode after chip enable goes high. This high level also enables a reference voltage for a TTL high output. The supply for the output buffer is V_{DD}, not the TRI-SHARE Port; thus, no special driver is required. In order to perform a write, the TSP must be pulsed low after the minimum hold time and the appropriate data placed on the I/$\overline{O}$. When the MM5270A goes into write, the output circuit is disabled. If the TSP is low at the start of the cycle, the memory is not selected, but it will be refreshed if the chip enable clock is pulsed.

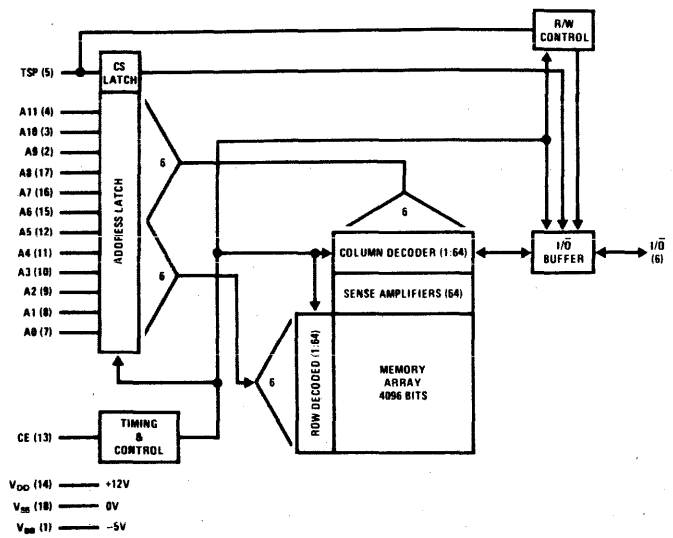
The RAM must be refreshed every 2 ms. This can be accomplished by performing a cycle at each of the 64 row addresses (A0–A5).

Addresses (A6–A11) must have a stable address during the refresh cycle. Any address is satisfactory as long as the address set-up and hold times are met. The chip select input can be either high or low for refresh.

features

- 4096 x 1 bit organization
- Access time–150 ns max
- Cycle time–300 ns min
- TRI-SHARE port
- High memory density–18-pin package
- TTL compatible inputs (except chip enable)
- TRI-STATE® common input/output
- Registers on chip for addresses and chip select
- Two power supplies, +12V, −5V
- Simple read-modify-write operation

block diagram



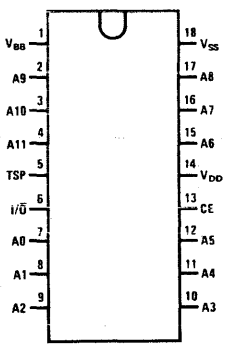
Pin Names

*A0–A11	Address Inputs	V_{BB}	Power (−5V)
CE	Chip Enable	V_{DD}	Power (+12V)
TSP	TRI-SHARE Port	V_{SS}	Ground
I/$\overline{O}$	$D_{IN}/\overline{D_{OUT}}$		

*Row address A0–A5

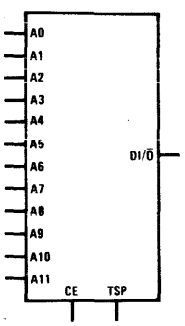
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



MM5270A TRI-SHARE™ 4096-bit fully decoded dynamic random access read/write memory

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absolute maximum ratings

Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin Relative to V_{BB}	−0.3V to +20V
($V_{SS} = V_{BB} \geq 4.5V$)	
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

T_A = 0°C to +70°C, V_{DD} = +12V ±5%, V_{BB} (Note 2) = −5V ±5%, V_{SS} = 0V, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (3)	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +0.6V, (Note 4)		110		μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, T_A = 25°C		20		mA
$I_{DD\ AV1}$	Average V_{DD} Current	T_A = 25°C, Cycle Time = 400 ns, t_{CE} = 160 ns		45		mA
$I_{DD\ AV2}$	Average V_{DD} Current	T_A = 25°C, Cycle Time = 1000 ns, t_{CE} = 160 ns		15		mA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns, (*Figure 4*)	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4			V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} current is to V_{SS}. The I_{BB} current is the sum of all leakage currents.

ac electrical characteristics T_A = 0°C to +70°C, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		40			ns
t_{CC}	CE "OFF" Time		100			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
t_{TC}	TRI-SHARE Port to CE Set-Up Time		0			ns
t_{TH}	TRI-SHARE Port Hold Time		40			ns
READ CYCLE						
t_{CY}	Cycle Time	t_T = 20 ns C_{LOAD} = 50 pF, Load = One TTL Gate Ref 1 = 2.0V, Ref 0 = 0.8V $t_{ACC} = t_{AC} + t_{CO} + t_T$	300			ns
t_{CE}	CE "ON" Time		160		3000	ns
t_{CO}	CE Output Delay				130	ns
t_{ACC}	Address to Output Access				150	ns
t_{TL}	CE to TSP		0			ns

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ac electrical characteristics (con't) $T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		300			ns
t_{CE}	CE "ON" Time		160		3000	ns
t_{WI}	TSP to CE "OFF"		80			ns
t_{CW}	CE to TSP	$t_T = 20$ ns			75	ns
t_D	D_{IN} to CE "OFF"		80			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	TSP Pulse Width		50			ns

ac electrical characteristics (con't) $T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		400			ns
t_{CRW}	CE Width During RMW		260		3000	ns
t_{WC}	TSP to CE "ON"	$t_T = 20$ ns	0			ns
t_{W2}	TSP to CE "OFF"	$C_{LOAD} = 50$ pF, Load = One TTL Gate	120			ns
t_{WP}	TSP Pulse Width	Ref 1 - 2.0V, Ref 0 = 0.8V	50			ns
t_D	D_{IN} to CE "OFF"	$t_{ACC} = t_{AC} + t_{CO} + t_T$	80			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				130	ns
t_{ACC}	Access Time				150	ns
t_{WD}	TSP to Output High Impedance				40	ns
t_M	Modify Time		0			ns
CAPACITANCE (Note 1)						
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15		pF
$C_{I/\overline{O}}$	Data I/$\overline{O}$ Capacitance	$V_{OUT} = 0V$		8		pF
C_{IN}	TSP Capacitance	$V_{IN} = V_{SS}$		5		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

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MOS RAMs

MM5270-5 TRI-SHARE™ 4096-bit random access read/write memory

general description

The MM5270-5 is a slower speed version of National's MM5270 dynamic RAM. Please refer to the MM5270 specification for pin configuration, block diagram and switching time waveforms.

features

- Access time—270 ns
- Cycle time—470 ns

absolute maximum ratings (Note 1)

Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.0W

Order Number MM5270D-5
See Package 4

dc electrical characteristics

T_A = 0°C to +70°C, V_{DD} = +12V ±5%, V_{BB} (Note 2) = −5V ±5%, V_{SS} = 0V, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (3)	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +0.6V, (Note 4)		110		μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, T_A = 25°C		20		mA
$I_{DD\ AV1}$	Average V_{DD} Current	T_A = 25°C, Cycle Time = 470 ns, t_{CE} = 300 ns		35		mA
$I_{DD\ AV2}$	Average V_{DD} Current	T_A = 25°C, Cycle Time = 1000 ns, t_{CE} = 300 ns		15		mA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4			V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} current is to V_{SS}. The I_{BB} current is the sum of all leakage currents.

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ac electrical characteristics

$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		50			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
t_{TC}	TRI-SHARE Port to CE Set-Up Time		0			ns
t_{TH}	TRI-SHARE Port Hold Time		80			ns
READ CYCLE						
t_{CY}	Cycle Time	$t_T = 20$ ns	470			ns
t_{CE}	CE "ON" Time	$C_{LOAD} = 50$ pF, Load = One TTL Gate	300		3000	ns
t_{CO}	CE Output Delay	Ref 1 = 2.0V, Ref 0 = 0.8V			250	ns
t_{ACC}	Address to Output Access	$t_{ACC} = t_{AC} + t_{CO} + t_T$			270	ns
t_{TL}	CE to TSP		0			ns
WRITE CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_{WI}	TSP to CE "OFF"		150			ns
t_{CW}	CE to TSP	$t_T = 20$ ns			115	ns
t_D	D_{IN} to CE "OFF"		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	TSP Pulse Width		50			ns
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		650			ns
t_{CRW}	CE Width During RMW		480		3000	ns
t_{WC}	TSP to CE "ON"	$t_T = 20$ ns	0			ns
t_{W2}	TSP to CE "OFF"	$C_{LOAD} = 50$ pF, Load = One TTL Gate	200			ns
t_{WP}	TSP Pulse Width	Ref 1 = 2.0V, Ref 0 = 0.8V	50			ns
t_D	D_{IN} to CE "OFF"	$t_{ACC} = t_{AC} + t_{CO} + t_T$	150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				180	ns
t_{ACC}	Access Time				270	ns
t_{WD}	TSP to Output High Impedance				250	ns
t_M	Modify Time		0			ns
CAPACITANCE (Note 1)						
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15		pF
$C_{I/O}$	Data I/O Capacitance	$V_{OUT} = 0V$		8		pF
C_{iN}	TSP Capacitance	$V_{IN} = V_{SS}$		5		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

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MOS RAMs
Advance Information

MM5271 TRI-SHARE™ 4096-bit fully TTL compatible dynamic random access read/write memory

general description

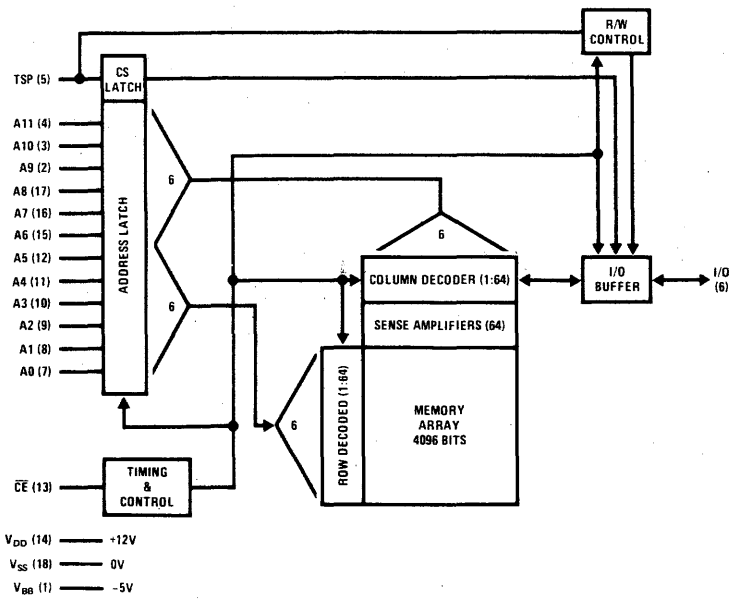
The MM5271 is a fully TTL compatible 4096-bit dynamic random access memory with TRI-SHARE. Because of this unique design feature, National is able to house a 4k device in an 18-pin dual-in-line package. The device is manufactured using N-channel silicon gate technology with a single transistor cell which provides higher density on a monolithic chip and thus lower cost.

The TRI-SHARE Port (TSP) is a multifunction input that, along with a common input/output, allows National to manufacture an 18-pin version of a 4k RAM. The functions controlled by the TSP are read/write, V_{CC}, and logical chip select. In order to understand how the TSP works, consider the timing diagrams. The state of the TSP at the leading edge of the chip enable clock determines whether the device is selected. If it is at a TTL high level, the chip is selected and the device goes into a read mode after chip enable goes high. This high level also controls the V_{CC} function in that it enables a reference voltage for a TTL high output. The supply for the output buffer is V_{DD}, not the TRI-SHARE Port; thus, no special driver is required. In order to perform a write, the TSP must be pulsed low after the minimum hold time and the appropriate data placed on the I/O. When the MM5271 goes into write, the output circuit is disabled. If the TSP is low at the start of the cycle, the memory is not selected but it will be refreshed when the chip enable clock is pulsed.

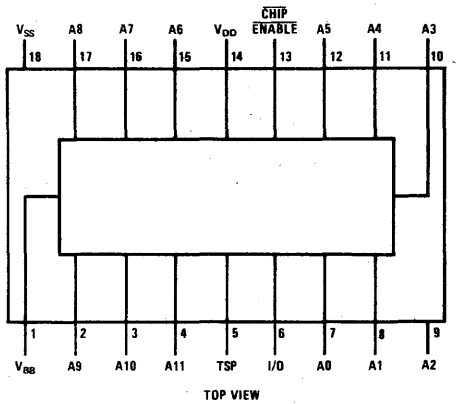
features

- 4096 x 1 bit organization
- Access time 250 ns maximum
- Cycle time 400 ns minimum
- TRI-SHARE port
- High memory density—18-pin package
- TTL compatible inputs
- TRI-STATE® common input/output
- Registers on chip for addresses and chip select
- Two power supplies, +12V, −5V
- Simple read-modify-write operation

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5271D
See Package 4

Pin Names

A0–A11	Address Inputs*	V_{BB}	Power (−5V)
$\overline{CE}$	Chip Enable	V_{DD}	Power (+12V)
TSP	TRI-SHARE Port	V_{SS}	Ground
I/O	$D_{IN}/\overline{D_{OUT}}$		

*Refresh Addess A0–A5

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absolute maximum ratings (Note 1)

Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.0W

dc electrical characteristics

T_A = 0°C to +70°C, V_{DD} = +12V ±5%, V_{BB} (Note 2) = −5V ±5%, V_{SS} = 0V, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (3)	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	$\overline{CE}$ = V_{IH}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During $\overline{CE}$ "OFF"	$\overline{CE}$ = V_{IH}, (Note 4)		1		mA
I_{DD2}	V_{DD} Supply Current During $\overline{CE}$ "ON"	CE = V_{IL}, T_A = 25°C		20		mA
$I_{DD\ AV1}$	Average V_{DD} Current	T_A = 25°C, Cycle Time = 400 ns, t_{CE} = 240 ns		35		mA
$I_{DD\ AV2}$	Average V_{DD} Current	T_A = 25°C, Cycle Time = 1000 ns, t_{CE} = 240 ns		15		mA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 10 ns, *(Figure 4)*	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4			V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} current is to V_{SS}. The I_{BB} current is the sum of all leakage currents.

ac electrical characteristics T_A = 0°C to +70°C, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE					
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to $\overline{CE}$ Set-Up Time	t_{AC} is MeasuredFrom End of Address Transition	0			ns
t_{AH}	Address Hold Time		100			ns
t_{CC}	$\overline{CE}$ "OFF" Time		140			ns
t_T	$\overline{CE}$ Transition Time				40	ns
t_{CF}	$\overline{CE}$ "OFF" to Output High Impedance State		50			ns
t_{TC}	TRI-SHARE Port to $\overline{CE}$ Set-Up Time		0			ns
t_{TH}	TRI-SHARE Port Hold Time		100			ns
	READ CYCLE					
t_{CY}	Cycle Time	t_T = 10 ns	400			ns
t_{CE}	$\overline{CE}$ "ON" Time	C_{LOAD} = 50 pF, Load = One TTL Gate	240		3000	ns
t_{CO}	$\overline{CE}$ Output Delay	Ref 1 = 2.0V, Ref 0 = 0.8V			250	ns
t_{ACC}	Address to Output Access	t_{ACC} = t_{AC} + t_{CO}			250	ns
t_{TL}	$\overline{CE}$ to TSP		0			ns

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ac electrical characteristics (con't) $T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		400			ns
t_{CE}	$\overline{CE}$ "ON" Time		240		3000	ns
t_{WI}	TSP to CE "OFF"		100			ns
t_{CW}	$\overline{CE}$ to TSP	t_T = 10 ns, (Note 4)			130	ns
t_D	D_{IN} to $\overline{CE}$ "OFF"		70			ns
t_{DH}	D_{IN} Hold Time		50			ns
t_{WP}	TSP Pulse Width		50			ns

ac electrical characteristics (con't) $T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		560			ns
t_{CRW}	$\overline{CE}$ Width During RMW	t_T = 10 ns	400		3000	ns
t_{W2}	TSP to $\overline{CE}$ "OFF"	C_{LOAD} = 50 pF, Load = One TTL Gate	150			ns
t_{WP}	TSP Pulse Width	Ref 1 - 2.0V, Ref 0 = 0.8V	50			ns
t_D	D_{IN} to $\overline{CE}$ "OFF"	$t_{ACC} = t_{AC} + t_{CO}$	70			ns
t_{DH}	D_{IN} Hold Time		50			ns
t_{CO}	$\overline{CE}$ to Output Delay				250	ns
t_{ACC}	Access Time				250	ns
t_{WD}	TSP to Output High Impedance				50	ns
t_M	Modify Time		0			ns
CAPACITANCE (Note 1)						
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	$\overline{CE}$ Capacitance	$V_{IN} = V_{SS}$		5		pF
$C_{I/O}$	Data I/O Capacitance	V_{OUT} = 0V		8		pF
C_{IN}	TSP Capacitance	$V_{IN} = V_{SS}$		5		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

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MOS RAMs

MM5280 4096-bit dynamic random access memory

general description

National's MM5280 is a 4096 word by 1 bit dynamic RAM. It incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

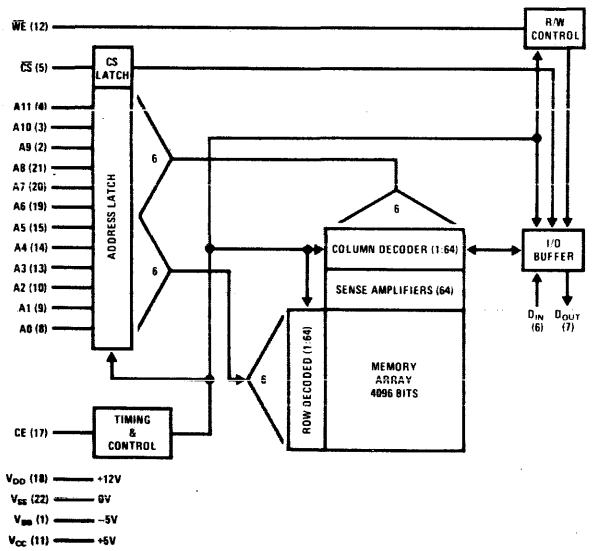
The MM5280 must be refreshed every 2 ms. This can be accomplished by performing a read cycle at each of the 64 row addresses (A0–A5). The chip select input can be either high or low for refresh.

The MM5280 has been designed with minimum production costs as a prime criterion. It is fabricated using N-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The MM5280 uses a single transistor cell to minimize the device area. The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance memory device.

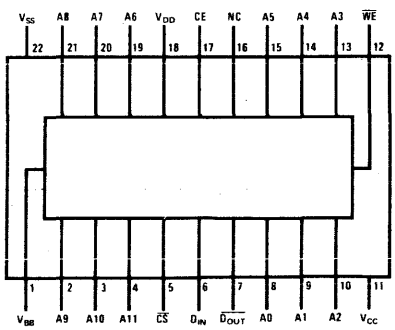
features

- Organization: 4096 x 1
- Access time 200 ns maximum
- Cycle time 400 ns minimum
- Easy system interface
  - One high voltage input—chip enable
  - TTL compatible—all other inputs and output
- Address registers on-chip
- TRI-STATE® output
- Simple read-modify-write operation
- Industry standard pin configuration

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5280D
See Package 5

Pin Names

A0–A11	Address Inputs*	V_{BB}	Power (−5V)
CE	Chip Enable	V_{CC}	Power (+5V)
$\overline{CS}$	Chip Select	V_{DD}	Power (+12V)
D_{IN}	Data Input	V_{SS}	Ground
$\overline{D_{OUT}}$	Data Output	$\overline{WE}$	Write Enable
NC	Not Connected		

*Refresh Address A0–A5

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absolute maximum ratings (Note 1)

Operating Temperature Range	0°C to +70°C	Supply Voltages V_{DD}, V_{CC} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Storage Temperature	−65°C to +150°C	Power Dissipation	1.25W
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V		

dc electrical characteristics

T_A = 0°C to +70°C V_{DD} = +12V ±5%, V_{CC} = +5V ±5%, V_{BB} (Note 2) = −5V ±5%, V_{SS} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +6V, Note 4		110		μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, T_A = 25°C		20		mA
$I_{DD\ AV1}$	Average V_{DD} Current	T_A = 25°C Cycle Time = 400 ns, t_{CE} = 230 ns		35		mA
$I_{DD\ AV2}$	Average V_{DD} Current	T_A = 25°C Cycle Time = 1000 ns, t_{CE} = 230 ns		15		mA
I_{CC1}	V_{CC} Supply Current During CE "OFF"	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, (Note 5)		0.01	10	μA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns *(Figure 4)*	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V_{CC}	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.

Note 5: During CE "ON" V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

ac electrical characteristics T_A = 0°C to +70°C, V_{DD} = 12V ±5%, V_{CC} = 5V ±5%, V_{BB} = −5V ±5%

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		50			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
READ CYCLE						
t_{CY}	Cycle Time		400			ns
t_{CE}	CE "ON" Time		230		3000	ns
t_{CO}	CE Output Delay	C_{LOAD} = 50 pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$			180	ns
t_{ACC}	Address to Output Access				200	ns
t_{WL}	CE to $\overline{WE}$		0			ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns

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ac electrical characteristics (con't)

$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5\% \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		400			ns
t_{CE}	CE "ON" Time		230		3000	ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{CW}	CE to $\overline{WE}$	$t_T = 20$ ns	100			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns

ac electrical characteristics (con't)

$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5\% \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		520			ns
t_{CRW}	CE Width During RMW		350		3000	ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{WP}	$\overline{WE}$ Pulse Width	$t_T = 20$ ns, $C_{LOAD} = 50$ pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\,t_T$	50			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				180	ns
t_{WO}	$\overline{WE}$ to $\overline{D_{OUT}}$ Invalid		0			
t_{ACC}	Access Time				200	ns
CAPACITANCE (Note 1)		$T_A = 25°C$				
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15		pF
C_{OUT}	Data Output Capacitance	$V_{OUT} = 0V$		5		pF
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	$V_{IN} = V_{SS}$		4		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

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MM5280A 4096-bit dynamic random access memory

general description

National's MM5280A is a 4096 word by 1 bit dynamic RAM. It incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

The RAM must be refreshed every 2 ms. This can be accomplished by performing a cycle at each of the 64 row addresses (A0–A5).

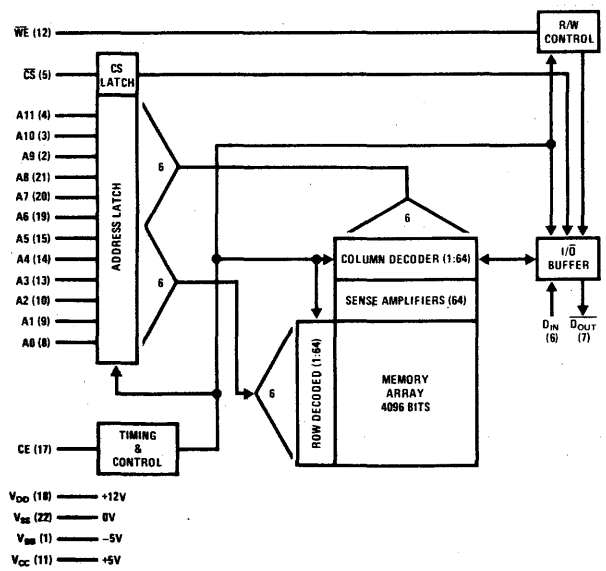
Addresses (A6–A11) must have a stable address during the refresh cycle. Any address is satisfactory as long as the address set-up and hold times are met. The chip select input can be either high or low for refresh.

The MM5280A has been designed with minimum production costs as a prime criterion. It is fabricated using N-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The MM5280A uses a single transistor cell to minimize the device area. The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance memory device.

features

- Organization: 4096 x 1
- Access time—150 ns max
- Cycle time—300 ns min
- Easy system interface
  - One high voltage input—chip enable
  - TTL compatible—all other inputs and output
- Address registers on-chip
- TRI-STATE® output
- Simple read-modify-write operation
- Industry standard pin configuration

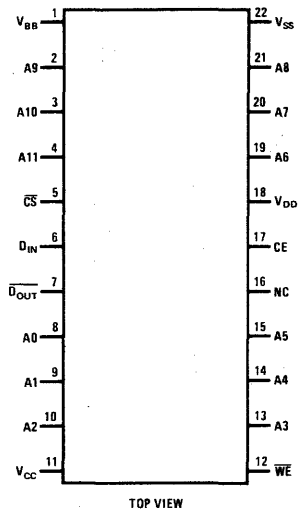
block diagram



Memory inverts from Data In to Data Out.

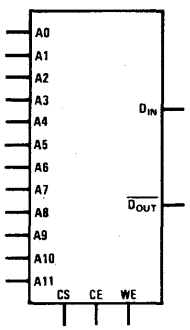
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



Pin Names

*A0–A11	Address Inputs	V_{BB}	Power (−5V)
CE	Chip Enable	V_{CC}	Power (+5V)
$\overline{CS}$	Chip Select	V_{DD}	Power (+12V)
D_{IN}	Data Input	V_{SS}	Ground
$\overline{D_{OUT}}$	Data Output	$\overline{WE}$	Write Enable
NC	Not Connected		

*Row address A0–A5

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absolute maximum ratings

Operating Temperature Range	0°C to +70°C	Voltage on Any Pin Relative to V_{BB} ($V_{SS} - V_{BB} \geq 4.5V$)	−0.3V to +20V
Storage Temperature	−65°C to +150°C		
Power Dissipation	1.25W	Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

$T_A = 0°C$ to $+70°C$ $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, V_{BB} (Note 2) $= -5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +6V, Note 4		110		μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, $T_A = 25°C$		20		mA
$I_{DD\ AV1}$	Average V_{DD} Current	$T_A = 25°C$ Cycle Time = 300 ns, t_{CE} = 160 ns		45		mA
$I_{DD\ AV2}$	Average V_{DD} Current	Cycle Time = 1000 ns, t_{CE} = 160 ns		15		mA
I_{CC1}	V_{CC} Supply Current During CE "OFF"	CE = V_{ILC} or $\overline{CS}$ = V_{IH},(Note 5)		0.01	10	μA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns *(Figure 4)*	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V_{CC}	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.

Note 3: Typical values are for $T_A = 25°C$ and nominal power supply voltages.

Note 4: The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.

Note 5: During CE "ON" V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

ac electrical characteristics $T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		40			ns
t_{CC}	CE "OFF" Time		100			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
READ CYCLE						
t_{CY}	Cycle Time		300			ns
t_{CE}	CE "ON" Time		160		3000	ns
t_{CO}	CE Output Delay	C_{LOAD} = 50 pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$			130	ns
t_{ACC}	Address to Output Access				150	ns
t_{WL}	CE to $\overline{WE}$		0			ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns

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ac electrical characteristics (con't)

$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5\% \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		300			ns
t_{CE}	CE "ON" Time		160		3000	ns
t_W	$\overline{WE}$ to CE "OFF"		80			ns
t_{CW}	CE to $\overline{WE}$	$t_T = 20$ ns	80			ns
t_D	D_{IN} to CE Set-Up		80			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns

ac electrical characteristics (con't) $T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5\% \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		370			ns
t_{CRW}	CE Width During RMW		230		3000	ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns
t_W	$\overline{WE}$ to CE "OFF"		80			ns
t_{WP}	$\overline{WE}$ Pulse Width	$t_T = 20$ ns, $C_{LOAD} = 50$ pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$	50			ns
t_D	D_{IN} to CE Set-Up		80			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				130	ns
t_{WO}	$\overline{WE}$ to $\overline{D_{OUT}}$ Invalid		0			
t_{ACC}	Access Time				150	ns
CAPACITANCE (Note 1)		$T_A = 25°C$				
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15		pF
C_{OUT}	Data Output Capacitance	$V_{OUT} = 0V$		5		pF
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	$V_{IN} = V_{SS}$		4		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

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MM5280-5 4096-bit dynamic random access read/write memory

general description

The MM5280-5 is a slower speed version of National's MM5280. Please refer to the MM5280 specification for pin configuration, block diagram and switching time waveforms.

features

- Access time—270 ns
- Cycle time—470 ns

absolute maximum ratings (Note 1)

Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD}, V_{CC} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.25W

Order Number MM5280D-5
See Package 5

dc electrical characteristics

T_A = 0°C to +70°C V_{DD} = +12V ±5%, V_{CC} = +5V ±5%, V_{BB} (Note 2) = −5V ±5%, V_{SS} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +6V, Note 4		110		μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, T_A = 25°C		20		mA
$I_{DD\ AV1}$	Average V_{DD} Current	T_A = 25°C Cycle Time = 400 ns, t_{CE} = 230 ns		35		mA
$I_{DD\ AV2}$	Average V_{DD} Current	T_A = 25°C Cycle Time = 1000 ns, t_{CE} = 230 ns		15		mA
I_{CC1}	V_{CC} Supply Current During CE "OFF"	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, (Note 5)		0.01	10	μA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V_{CC}	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.

Note 5: During CE "ON" V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

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ac electrical characteristics

$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		50			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
READ CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_{CO}	CE Output Delay	$C_{LOAD} = 50$ pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\,t_T$			250	ns
t_{ACC}	Address to Output Access				270	ns
t_{WL}	CE to $\overline{WE}$		0			ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns
WRITE CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{CW}	CE to $\overline{WE}$	$t_T = 20$ ns	130			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		590			ns
t_{CRW}	CE Width During RMW		420		3000	ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{WP}	$\overline{WE}$ Pulse Width	$t_T = 20$ ns, $C_{LOAD} = 50$ pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\,t_T$	50			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				250	ns
t_{WO}	$\overline{WE}$ to $\overline{D_{OUT}}$ Invalid		0			
t_{ACC}	Access Time				270	ns
CAPACITANCE (Note 1)		$T_A = 25°C$				
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15		pF
C_{OUT}	Data Output Capacitance	$V_{OUT} = 0V$		5		pF
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	$V_{IN} = V_{SS}$		4		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

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National Semiconductor

MM5290 16,384 × 1 Bit Dynamic RAM

General Description

The MM5290 is a 16,384 x 1 bit dynamic RAM. It features a multiplexed address input with separate row and column strobes. This added flexibility allows the MM5290 to be used in page mode operation.

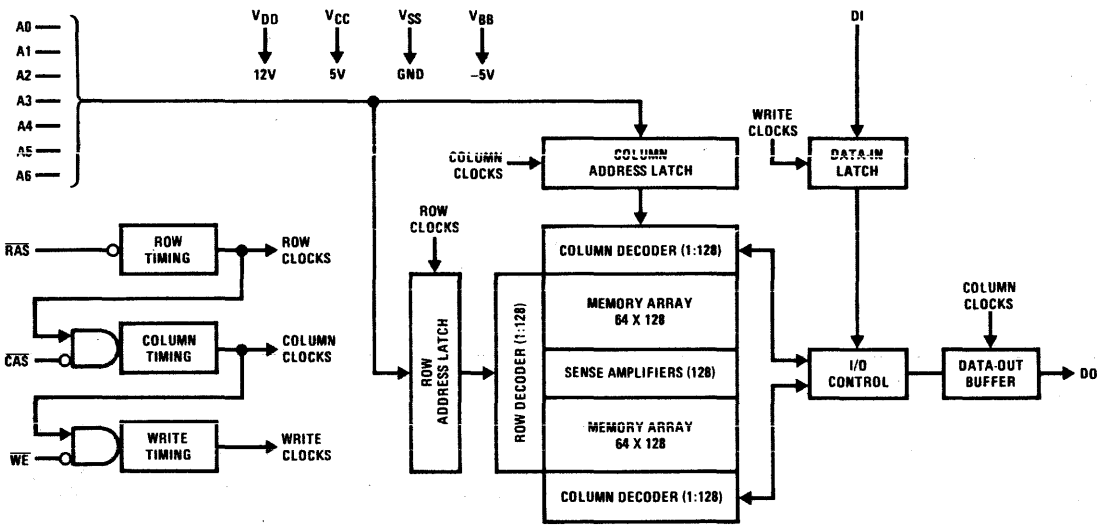
The MM5290 must be refreshed every 2 ms. This can be accomplished by performing any cycle which brings the Row Address Strobe active including a $\overline{RAS}$-only cycle at each of the 128 row addresses.

N-channel double-poly silicon gate technology, developed by National, is used in the manufacture of the MM5290. This process combines high density and performance with reliability. Greater system densities are achievable by the use of a 16-pin dual-in-line package for the MM5290.

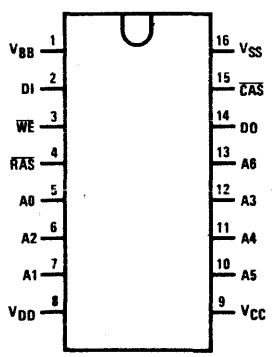
Features

- Access times: 150 ns, 200 ns, 300 ns
- Low power: 462 mW max
- TTL compatible: all inputs and output
- Gated $\overline{CAS}$—noncritical timing
- Read, Write, Read-Modify-Write and $\overline{RAS}$-only Refresh cycles
- Page mode operation
- Industry standard 16-pin configuration

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Pin Names

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0–A6	Address Inputs
DI	Data Input
DO	Data Output
V_{DD}	Power (12V)
V_{CC}	Power (5V)
V_{SS}	Ground
V_{BB}	Power (−5V)

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absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.5V to +7V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics (T_A within operating temperature range, V_{CC} = 5V ±5%, unless otherwise noted).

PARAMETER (Note 3)	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Input Current (I_{LI})	V_{IN} = 0 to V_{CC}			10	μA
Logical "1" Input Voltage (V_{IH})		2.0		V_{CC}+1.0	V
Logical "0" Input Voltage (V_{IL})		−0.5		0.8	V
Logical "1" Output Voltage (V_{OH})	I_{OH} = −400 μA	2.4			V
Logical "0" Output Voltage (V_{OL})	I_{OL} = 2.1 mA			0.4	V
Output Leakage Current (I_{LOH})	V_{OUT} = 4V, Chip Deselected			10	μA
Output Leakage Current (I_{LOL})	V_{OUT} = 0.45V, Chip Deselected			−20	μA
Power Supply Current (I_{CC1})	All Inputs = 5.25V, Data Output Open		40	98	mA

capacitance

PARAMETER (Note 3)	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Input Capacitance (All Inputs) (C_{IN})	V_{IN} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			7.5	pF
Output Capacitance (C_{OUT})	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			15.0	pF

ac electrical characteristics

(T_A within operating temperature range, V_{CC} = 5V ±5%, unless otherwise specified).
See ac test circuit and switching time waveforms.

PARAMETER (Note 3)	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
t_{ACCESS}	See ac Load Circuit. All Times Measured to 1.5V Level with t_r and t_f of Input < 20 ns, *(Figure 1)*			450	ns
t_{SELECT}	See ac Load Circuit. All Times Measured to 1.5V Level with t_r and t_f of Input < 20 ns, *(Figure 2)*			200	ns
$t_{DESELECT}$	See ac Load Circuit. All Times Measured to 1.5V Level with t_r and t_f of Input < 20 ns, *(Figure 2)*			200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: logical "1" = most positive voltage level, logical "0" = most negative voltage level.

Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

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AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = −5V ±10%, V_{SS} = 0, (Notes 2 and 3)

SYMBOL	PARAMETER	MM5290-2		MM5290-3		MM5290-4		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	375		375		475		ns	7, 8
t_{RWC}	Read-Write Cycle Time	375		375		550		ns	7, 8
t_{PC}	Page Mode Cycle Time	170		225		330		ns	
t_{RAC}	Access Time from $\overline{RAS}$		150		200		300	ns	9, 11
t_{CAC}	Access Time from $\overline{CAS}$		100		135		200	ns	10, 11
t_{OFF}	Output Buffer Turn-Off Delay	0	40	0	50	0	70	ns	12
t_T	Transition Time (Rise and Fall)	3	35	3	50	3	50	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	100		120		165		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	150	32,000	200	32,000	300	32,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	100		135		200		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	100	10,000	135	10,000	200	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	65	35	100	ns	9
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	−20		−20		−20		ns	
t_{ASR}	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	Row Address Hold Time	20		25		35		ns	
t_{ASC}	Column Address Set-Up Time	−10		−10		−10		ns	
t_{CAH}	Column Address Hold Time	45		55		75		ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	95		120		175		ns	
t_{RCS}	Read Command Set-Up Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{WCH}	Write Command Hold Time	45		55		75		ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		120		175		ns	
t_{WP}	Write Command Pulse Width	45		55		75		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	60		80		120		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	60		80		120		ns	
t_{DS}	Data-In Set-Up Time	0		0		0		ns	13, 14
t_{DH}	Data-In Hold Time	45		55		75		ns	13, 14
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	95		120		175		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (for Page Mode Cycle Only)	60		80		120		ns	
t_{REF}	Refresh Period		2		2		2	ms	
t_{WCS}	$\overline{WE}$ to $\overline{CAS}$ Set-Up Time	−40		−40		−40		ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	70		95		150		ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	120		160		250		ns	15

Note 7: The specifications for $t_{RC(MIN)}$ and $t_{RWC(MIN)}$ are used only to indicate cycle time at which proper operation over the full temperature range is guaranteed.

Note 8: Transition times are measured between V_{IHC} or V_{IH} and V_{IL}. Timing measurements are made between $V_{IHC(MIN)}$ or $V_{IH(MIN)}$ and $V_{IL(MAX)}$, and assume t_T = 5 ns.

Note 9: Assumes row-limited access, i.e., $t_{RCD} \leq t_{RCD(MAX)}$. If this condition is not satisfied, then note 10 applies.

Note 10: Assumes column-limited access, i.e., $t_{RCD} > t_{RCD(MAX)}$.

Note 11: Equivalent load is 2 standard TTL inputs plus 100 pF.

Note 12: $\overline{CAS}$ going high disables the Data Output. t_{OFF} is the delay to the high impedance state.

Note 13: These parameters are referenced to the negative edge of $\overline{CAS}$ in an early-write cycle and to the negative edge of $\overline{WE}$ in a Read-Modify-Write cycle. (See Note 12, below).

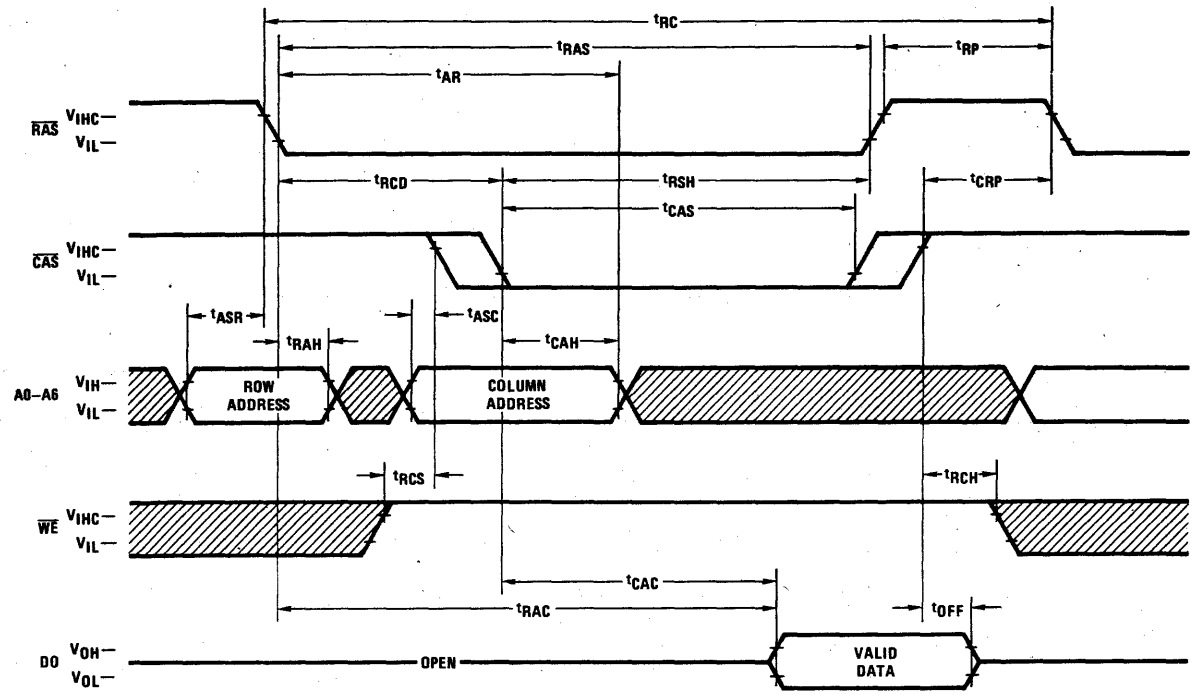
Note 14: If $t_{WCS} \geq t_{WCS(MIN)}$, the Data Output is guaranteed to remain in the high impedance state for the duration of the cycle. This is the "early-write" cycle.

Note 15: If $t_{CWD} \geq t_{CWD(MIN)}$ and $t_{RWD} \geq t_{RWD(MIN)}$, the Data Output will contain the original data in the selected cell. This is the Read-Modify-Write cycle. If either of these conditions is not satisfied, the output will be indeterminate unless the early-write condition of Note 12 is met.

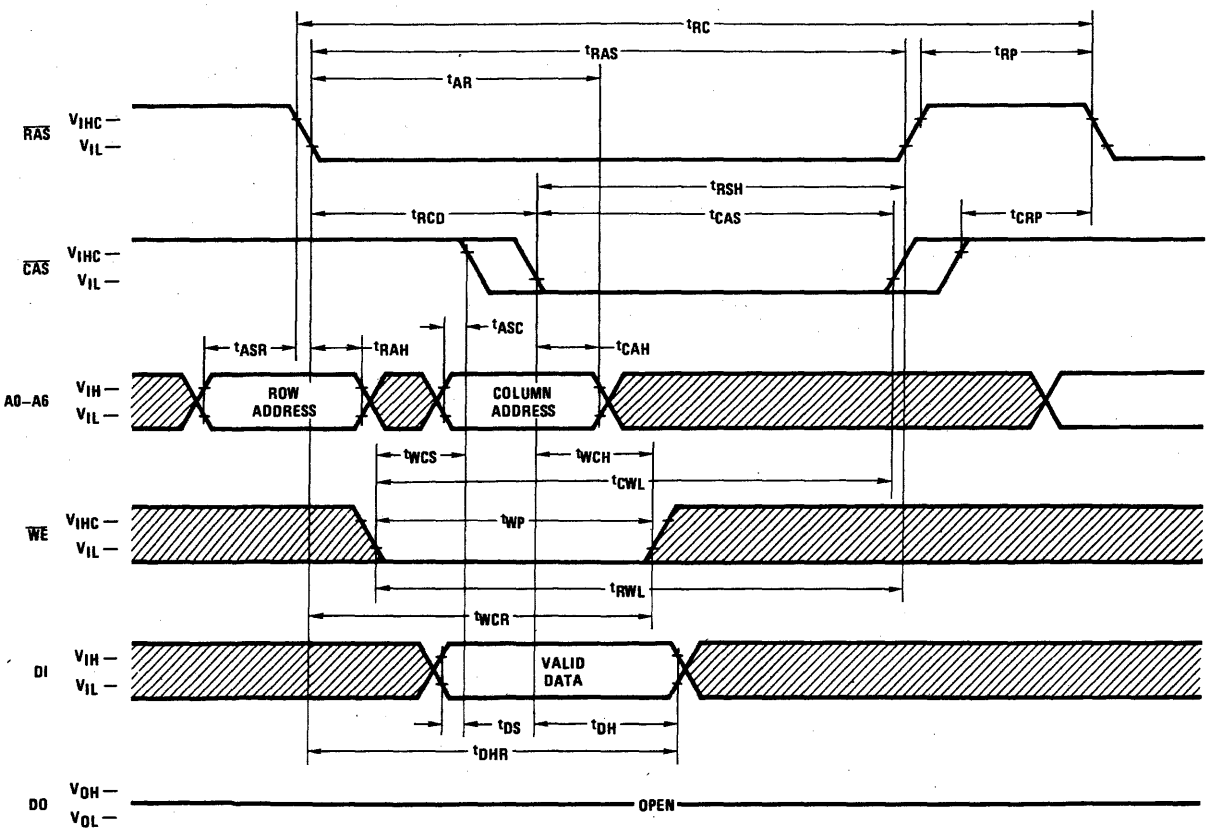
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Switching Time Waveforms

Read Cycle



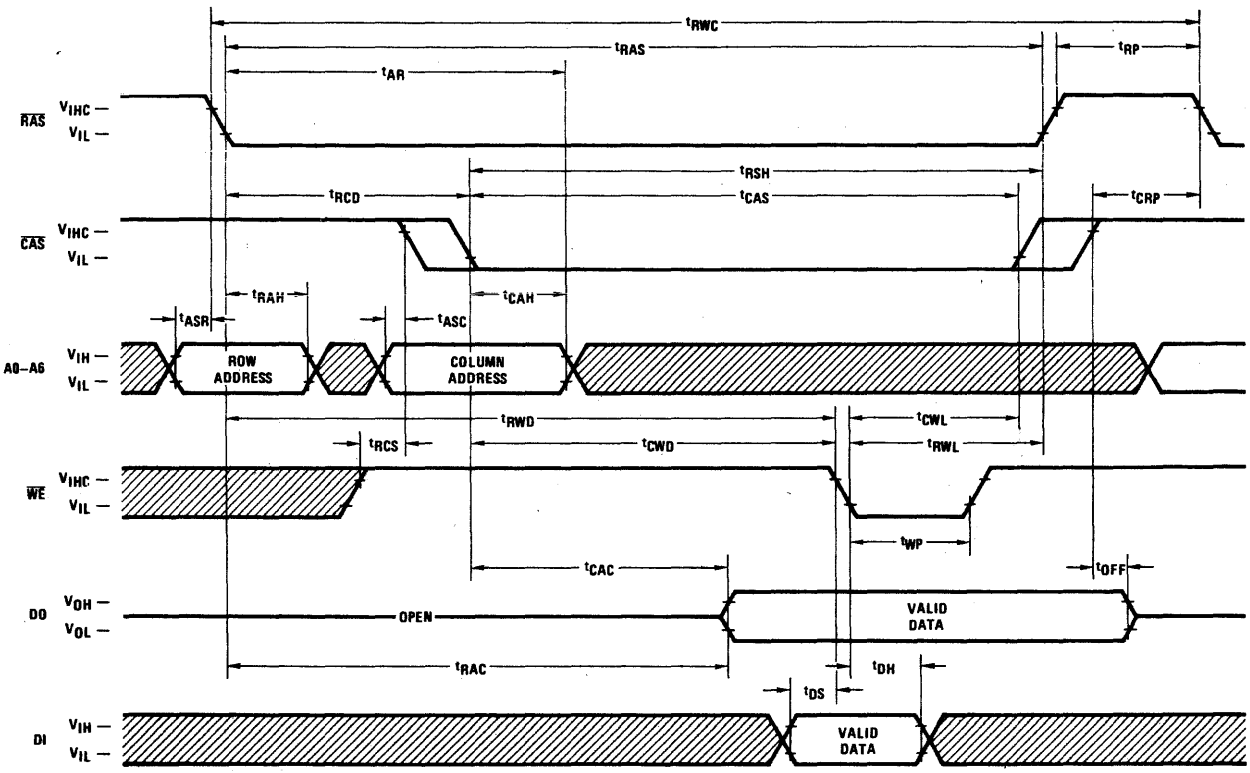
Write Cycle (Early Write)



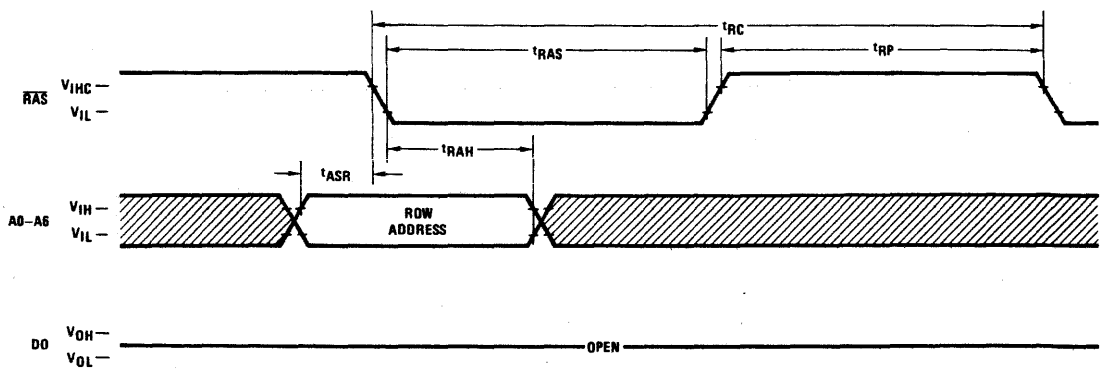
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Switching Time Waveforms (Continued)

Read-Write Cycle, Read-Modify-Write Cycle



$\overline{RAS}$-Only Refresh Cycle

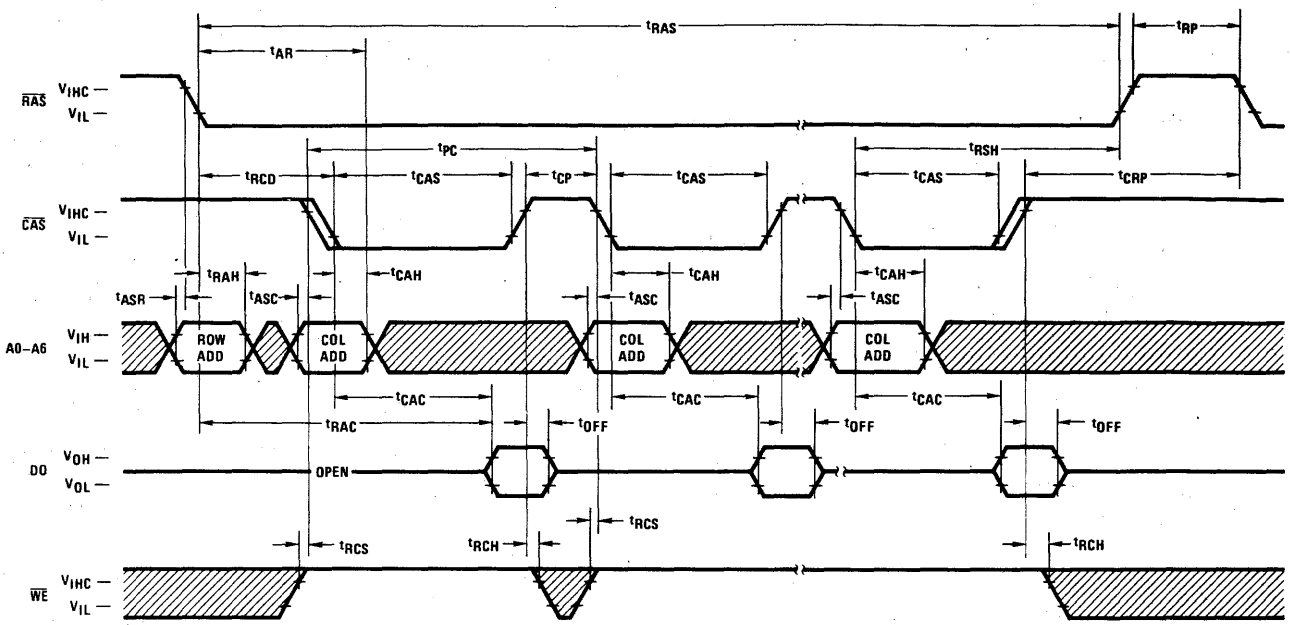


Note. $\overline{CAS}$ = V_{IHC}, $\overline{WE}$ = don't care

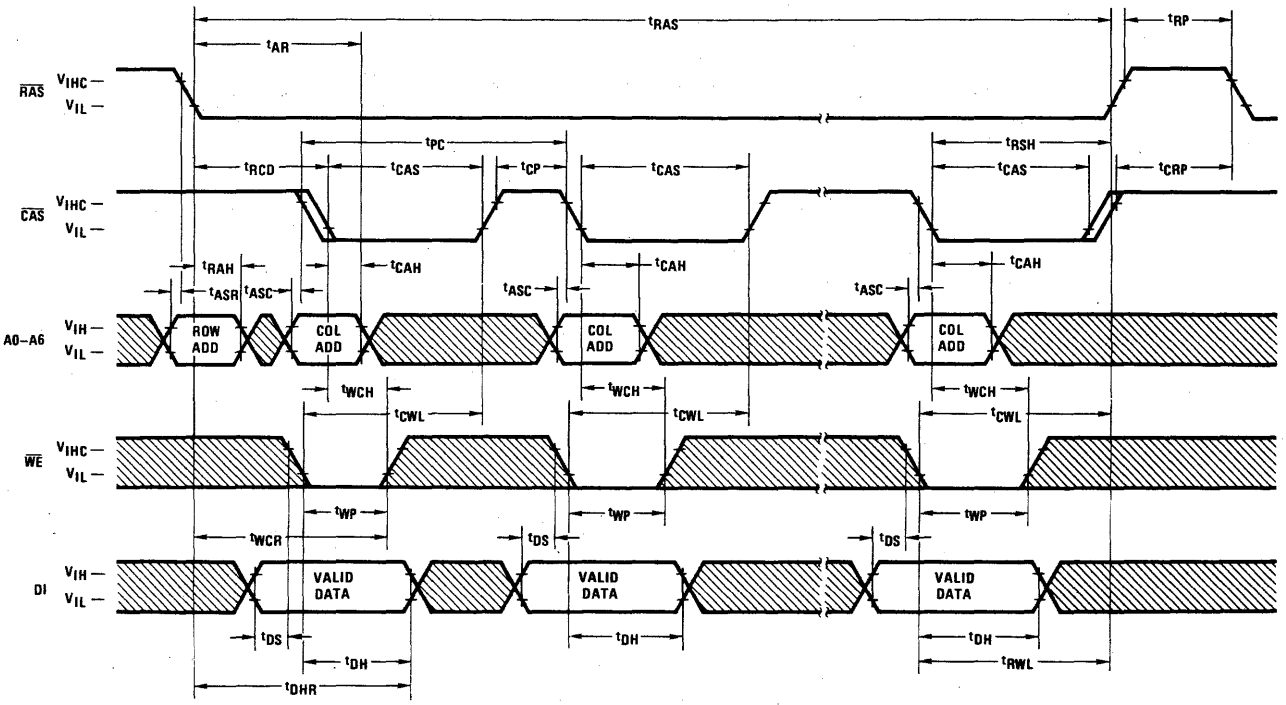
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Switching Time Waveforms (Continued)

Page Mode Read Cycle



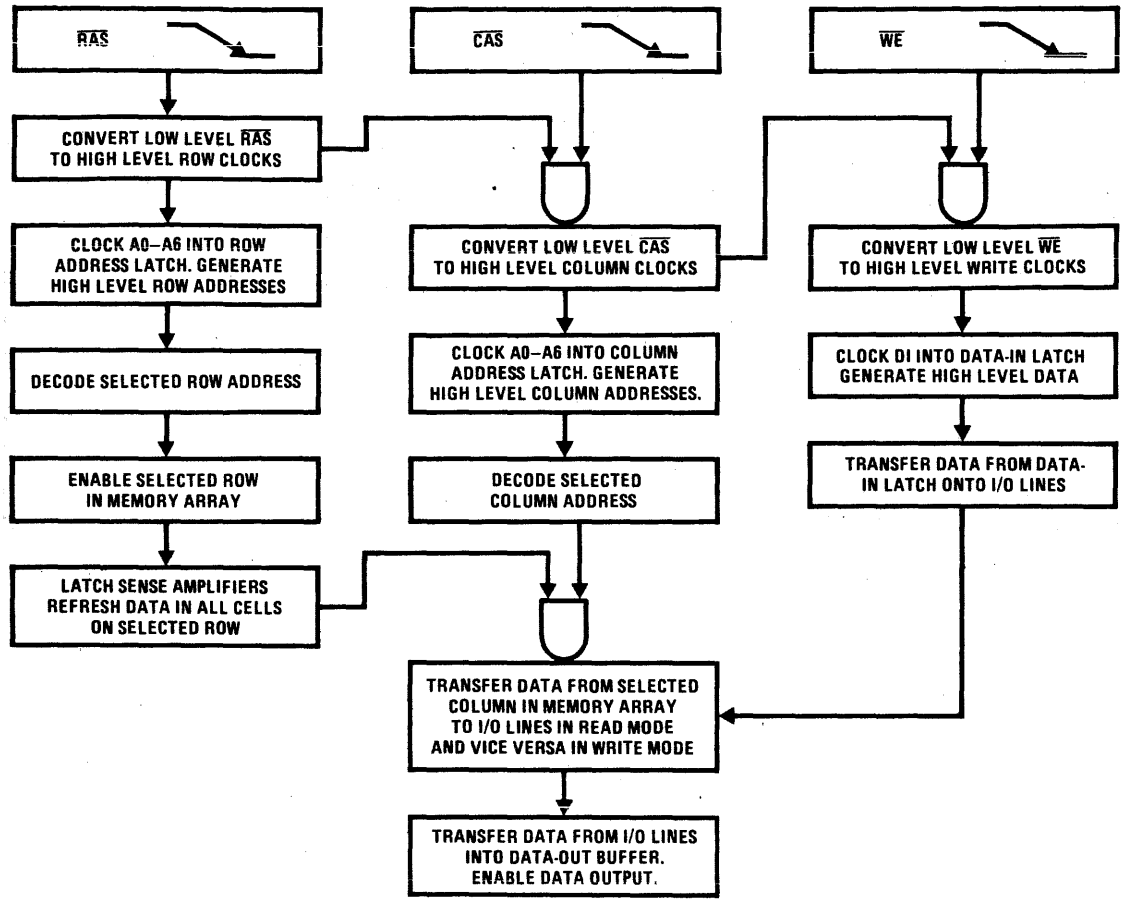
Page Mode Write Cycle



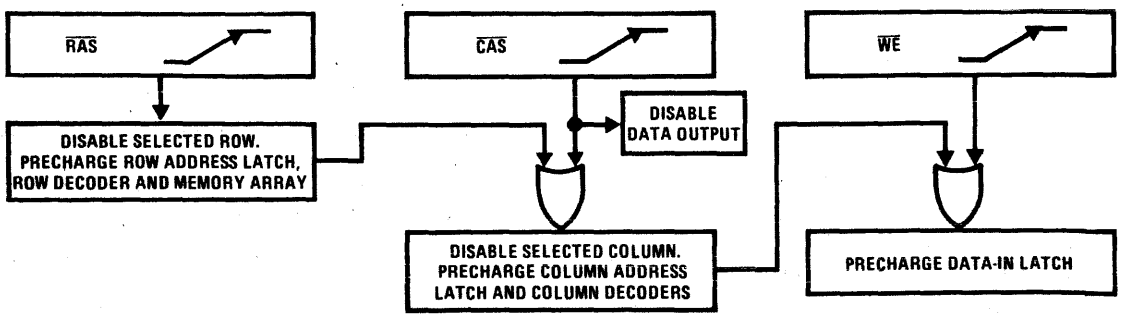
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Timing Flow Chart

ACTIVE

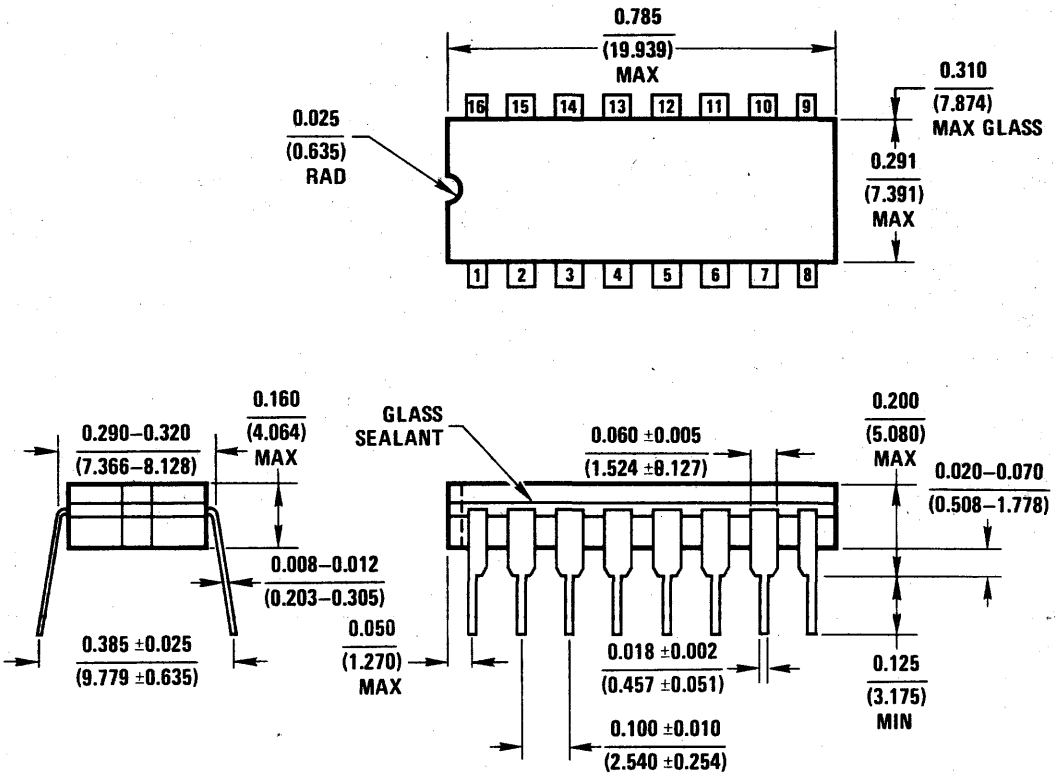


PRECHARGE



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Physical Dimensions inches (millimeters)



Cavity Dual-In-Line Package (J)
Order Number MM5290J
NS Package Number J16A

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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MM54C89/MM74C89 64-bit TRI-STATE® random access read/write memory

general description

The MM54C89/MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register, latches the address information on the positive to negative transition of the memory enable input. The four TRI-STATE® data output lines working in conjunction with the memory enable input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note: The timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

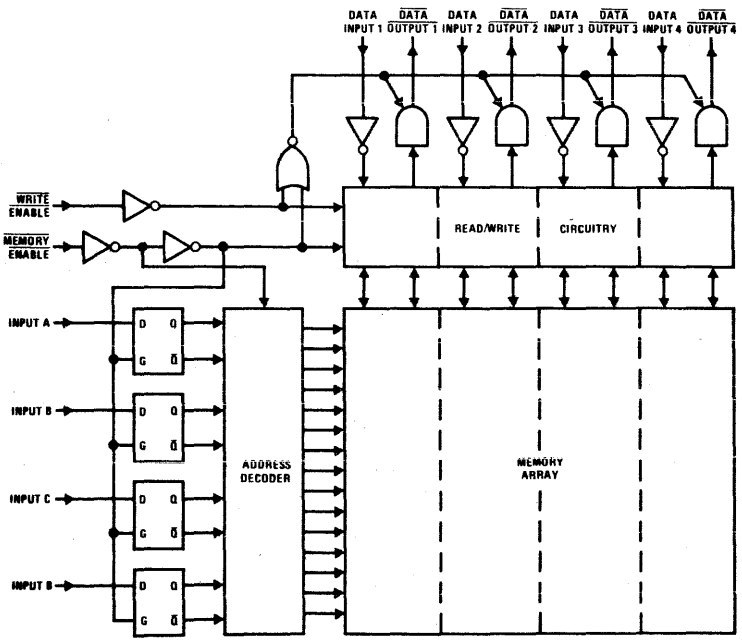
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

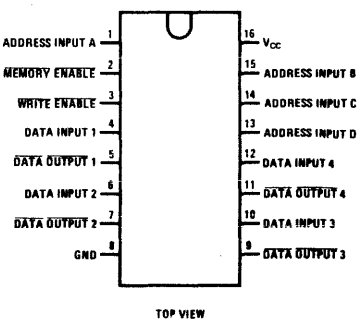
When the device is writing or disabled the output assumes a TRI-STATE (Hi-z) condition.

features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- Low power TTL compatibility — fan out of 2 driving 74L
- Input address register
- Low power consumption — 100 nW/package typ @ V_{CC} = 5V
- Fast access time — 130 ns typ at V_{CC} = 10V
- TRI-STATE output

logic and connection diagrams





TOP VIEW

Order Number MM54C89D or MM74C89D
See Package 3
Order Number MM74C89N
See Package 15

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absolute maximum ratings

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C89	−55°C to +125°C
MM74C89	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9.0			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0.5 1.0	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Output Current in High Impedance State	V_{CC} = 15V, V_O = 15V V_{CC} = 15V, V_O = 0V	 −1.0	0.005 −0.005	1.0	μA μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA 74C, V_{CC} = 4.75V, I_O = −360μA	2.4 2.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = +360μA 74C, V_{CC} = 4.75V, I_O = +360μA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	8.0	16		mA

ac electrical characteristics (T_A = 25°C, C_L = 50 pF, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from $\overline{\text{Memory Enable}}$ (t_{pd})	V_{CC} = 5.0V V_{CC} = 10V		270 100	500 220	ns ns
Access Time from Address Input (t_{acc})	V_{CC} = 5.0V V_{CC} = 10V		350 130	650 280	ns ns
Address Input Setup Time (t_{SA})	V_{CC} = 5.0V V_{CC} = 10V	150 60			ns ns
Address Input Hold Time (t_{HA})	V_{CC} = 5.0V V_{CC} = 10V	60 40			ns ns
$\overline{\text{Memory Enable}}$ Pulse Width (t_{ME})	V_{CC} = 5.0V V_{CC} = 10V	400 150	250 90		ns ns
$\overline{\text{Memory Enable}}$ Pulse Width ($t_{\overline{ME}}$)	V_{CC} = 5.0V V_{CC} = 10V	400 150	200 70		ns ns

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ac electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Setup Time for a Read (t_{SR})	V_{CC} = 5.0V	0			ns
	V_{CC} = 10V	0			ns
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Setup Time for a Write (t_{WS})	V_{CC} = 5.0V			t_{ME}	ns
	V_{CC} = 10V			t_{ME}	ns
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Pulse Width ($t_{\overline{WE}}$)	V_{CC} = 5.0V, t_{WS} = 0	300	160		ns
	V_{CC} = 10V, t_{WS} = 0	100	60		ns
Data Input Hold Time (t_{HD})	V_{CC} = 5.0V	50			ns
	V_{CC} = 10V	25			ns
Data Input Setup (t_{SD})	V_{CC} = 5.0V	50			ns
	V_{CC} = 10V	25			ns
Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from $\overline{\text{Memory}}$ $\overline{\text{Enable}}$ (t_{1H}, t_{0H})	V_{CC} = 5.0V, C_L = 5.0 pF, R_L = 10k		180	300	ns
	V_{CC} = 10V, C_L = 5.0 pF, R_L = 10k		85	120	ns
Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from $\overline{\text{Write}}$ $\overline{\text{Enable}}$ (t_{1H}, t_{0H})	V_{CC} = 5.0V, C_L = 5.0 pF, R_L = 10k		180	300	ns
	V_{CC} = 10V, C_L = 5.0 pF, R_L = 10k		85	120	ns
Input Capacity (C_{IN})	Any Input (Note 2)		5.0		pF
Output Capacity (C_{OUT})	Any Output (Note 2)		6.5		pF
Power Dissipation Capacity (C_{pd})	(Note 3)		230		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

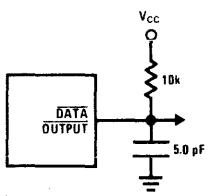
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

truth table

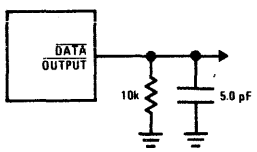
ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE
H	H	Inhibit, Storage	TRI-STATE

ac test circuits

t_{0H}

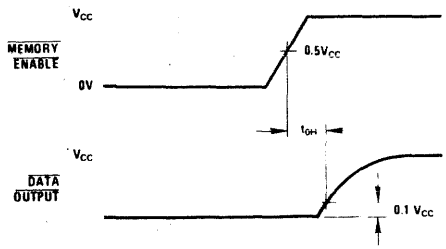


t_{1H}

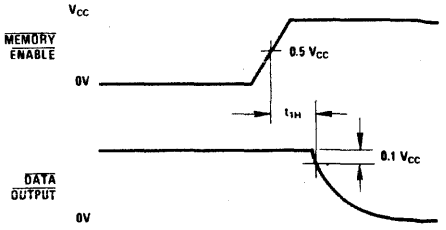


switching time waveforms

t_{0H}



t_{1H}



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CMOS RAMs

MM54C200/MM74C200 256-bit TRI-STATE® random access read/write memory

general description

The MM54C200/MM74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines, a data input line, a write enable line, and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. An internal address register, latches and address information on the positive to negative edge of $\overline{CE}_3$. The TRI-STATE data output line working in conjunction with $\overline{CE}_1$ or $\overline{CE}_2$ inputs provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of $\overline{CE}_3$. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition).

Note: The timing is different than the DM74200 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

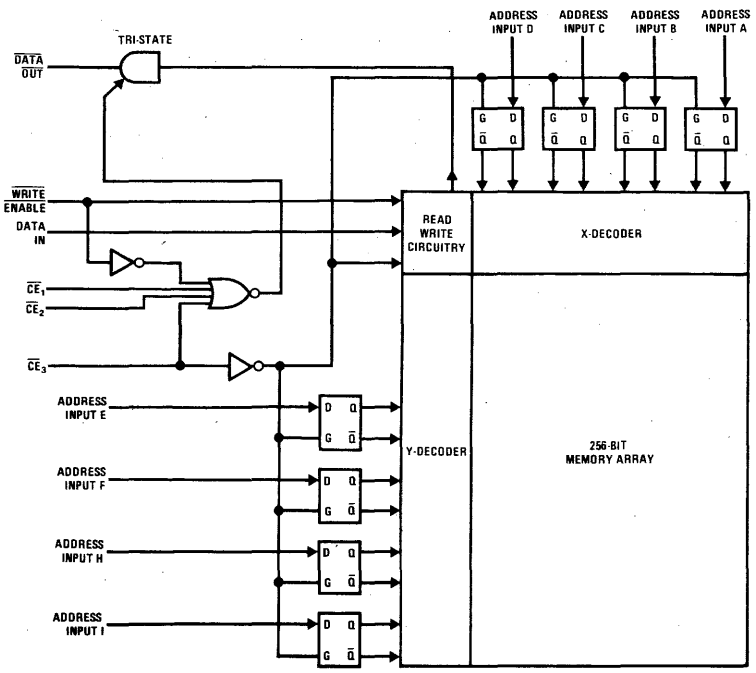
Read Operation: The data is read out by selecting the proper address and bringing $\overline{CE}_3$ low and write enable high. Holding $\overline{CE}_1$ or $\overline{CE}_2$ or $\overline{CE}_3$ at a high level forces the output into TRI-STATE. When used in bus organized systems, $\overline{CE}_1$, or $\overline{CE}_2$, a TRI-STATE control, provides for fast access times by not totally disabling the chip.

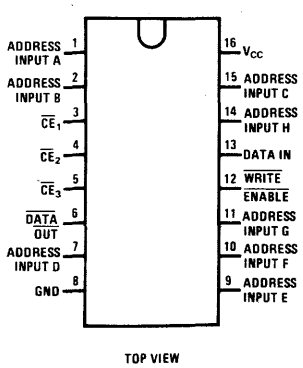
Write Operation: Data is written into the memory with $\overline{CE}_3$ low and write enable low. The state of $\overline{CE}_1$ or $\overline{CE}_2$ has no effect on the write cycle. The output assumes TRI-STATE with write enable low.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ TTL compatibility	fan out of 1 driving standard TTL
■ Low power	500 nW typ
■ Internal address register	

logic and connection diagrams





TOP VIEW

Order Number MM54C200D or MM74C200D
See Package 3
Order Number MM74C200N
See Package 15

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absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C200	−55°C to +125°C
MM74C200	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V V_{IN} = 0V	1.0	-0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.10		μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −1.6 mA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −1.6 mA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 1.6 mA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 1.6 mA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−4.0	−6.0		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−16.0	−25		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	5.0	8.0		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	20.0	30		mA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Access Time From Address (t_{ACC})	V_{CC} = 5.0V		450	900	ns
	V_{CC} = 10V		200	400	ns
Propagation Delay From $\overline{CE}_3$ (t_{pd})	V_{CC} = 5.0V		360	700	ns
	V_{CC} = 10V		120	300	ns
Propagation Delay From $\overline{CE}_1$ or $\overline{CE}_2$ ($t_{p\overline{CE}1}$)	V_{CC} = 5.0V		250	500	ns
	V_{CC} = 10V		85	200	ns
Address Setup Time (t_{SA})	V_{CC} = 5.0V	200	80		ns
	V_{CC} = 10V	100	30		ns
Address Hold Time (t_{HA})	V_{CC} = 5.0V	50	15		ns
	V_{CC} = 10V	25	5		ns

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ac electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Pulse Width ($t_{\overline{WE}}$)	V_{CC} = 5.0V	300	160		ns
	V_{CC} = 10V	150	70		ns
$\overline{CE}_3$ Pulse Widths (t_{CE})	V_{CC} = 5.0V	400	200		ns
	V_{CC} = 10V	160	80		ns
Input Capacity (C_{IN})	Any Input (Note 2)		5.0		pF
Output Capacity in TRI-STATE (C_{OUT})	(Note 2)		9.0		pF
Power Dissipation Capacity (C_{pd})	(Note 3)		400		pF

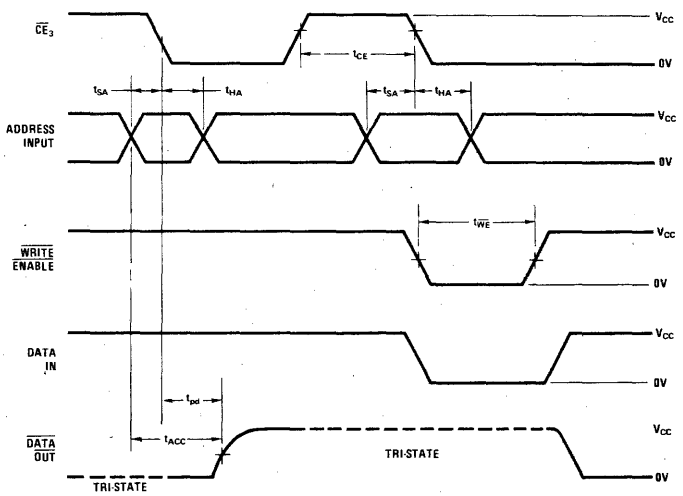
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

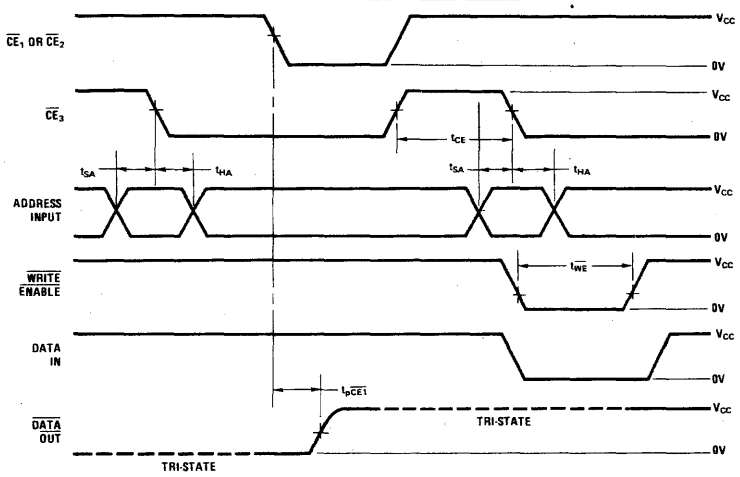
Note 3: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

switching time waveforms

Read and Write Cycles Using $\overline{CE}_3$ ($\overline{CE}_1$ = $\overline{CE}_2$ = logic 0)



Read and Write Cycles Using $\overline{CE}_3$ and $\overline{CE}_1$ (or $\overline{CE}_2$)



Note: Used for fast access time in bused systems.

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MM54C910/MM74C910 256-bit TRI-STATE® random access read/write memory

general description

The MM54C910/MM74C910 is a 64 word by 4 bit random access memory. Inputs consist of six address lines, four data input lines, a write enable, and a memory enable line. The six address lines are internally decoded to select one of 64 word locations. An internal address register, latches the address information on the positive to negative transition of memory enable. The TRI-STATE outputs allow for easy memory expansion.

Address Operation: Address inputs must be stable (t_{SA}) prior to the positive to negative transition of memory enable, and (t_{HA}) after the positive to negative transition of memory enable. The address register holds the information and stable address inputs are not needed at any other time.

Write Operation: Data is written into memory at the selected address if write enable goes low while memory enable is low. Write enable must be held low for t_{WE} and data must remain stable t_{HD} after write enable returns high.

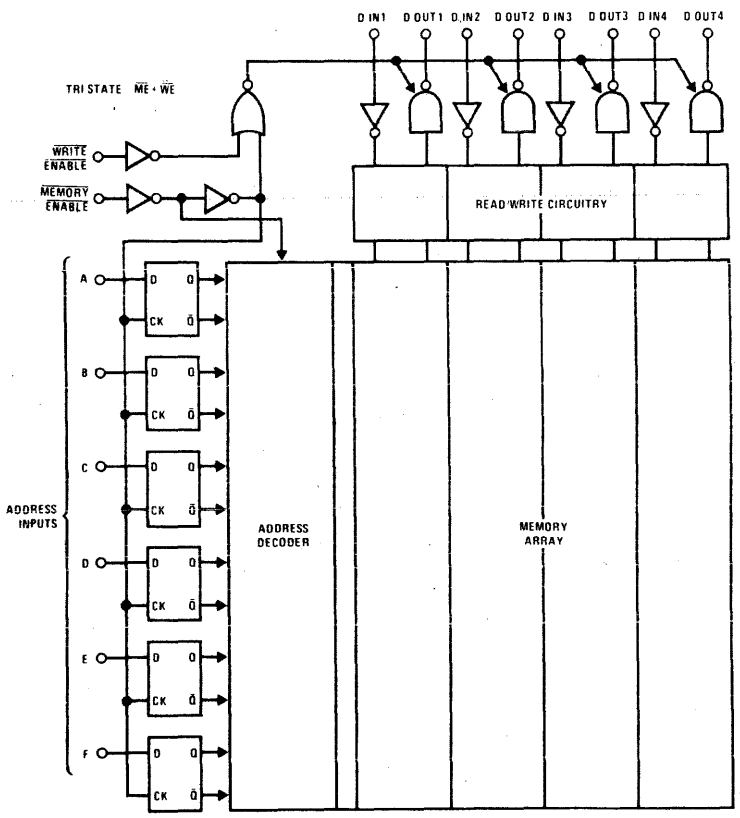
Read Operation: Data is nondestructively read from a memory location by an address operation with write enable held high.

Outputs are in the TRI-STATE (Hi-Z) condition when the device is writing or disabled.

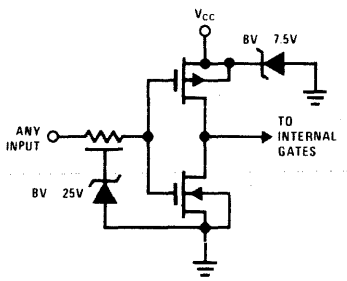
features

- Supply voltage range — 3V to 5.5V
- High noise immunity — 0.45 V_{CC} typ
- TTL compatible fan out — 1 TTL load
- Input address register
- Low power consumption — 250 nW/package typ (chip enabled or disabled)
- Fast access time — 250 ns typ at 5V
- TRI-STATE outputs
- High voltage inputs

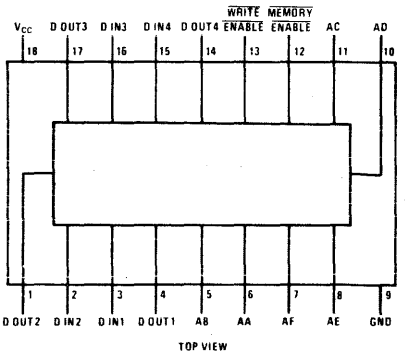
logic and connection diagrams



Input Protection



Dual-In-Line Package



Order Number MM54C910D or MM74C910D
See Package 4
Order Number MM74C910N
See Package 16

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absolute maximum ratings (Note 1)

Voltage At Any Output Pin	−0.3V to V_{CC} +0.3V
Voltage At Any Input Pin	−0.3V to +15V
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 5.5V
Standby V_{CC} Range	1.5V to 5.5V
Absolute Maximum V_{CC}	6.0V
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
MM54C910	4.5	5.5	V
MM74C910	4.75	5.25	V
Temperature (T_A)			
MM54C910	−55	+125	°C
MM74C910	−40	+85	°C

dc electrical characteristics MM54C910/MM74C910

(Min/max limits apply across the temperature and power supply range indicated).

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	Full Range	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	Full Range			0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 15V		0.005	2	μA
		V_{IN} = 5V		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0V	−1	−0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −150μA	V_{CC}−0.5			V
		I_O = −400μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.4	V
	Output Current in High	V_O = 5V		0.005	1	μA
	Impedence State	V_O = 0V	−1	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 5V		0.05	300	μA

ac electrical characteristics MM54C910/MM74C910

T_A = 25°C, V_{CC} = 5V, C_L = 50 pF

	PARAMETER	MIN	TYP	MAX	UNITS
t_{ACC}	Access Time from Address		250	500	ns
t_{PD}	Propagation Delay from $\overline{ME}$		180	360	ns
t_{SA}	Address Input Set-Up Time	140	70		ns
t_{HA}	Address Input Hold Time	20	10		ns
t_{ME}	$\overline{\text{Memory Enable}}$ Pulse Width	200	100		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	400	200		ns
t_{SD}	Data Input Set-Up Time	0			ns
t_{HD}	Data Input Hold Time	30	15		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	140	70		ns
t_{1H}, t_{OH}	Delay to TRI-STATE (Note 4)		100	200	ns
CAPACITANCE					
C_{IN}	Input Capacity				
	Any Input (Note 2)		5		pF
C_{OUT}	Output Capacity				
	Any Output (Note 2)		9		pF
C_{PD}	Power Dissipation Capacity (Note 3)		350		pF

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ac electrical characteristics (con't)

C_L = 50 pF

PARAMETER		MM54C910 T_A = −55°C to +125°C V_{CC} = 4.5V to 5.5V		MM74C910 T_A = −40°C to +85°C V_{CC} = 4.75V to 5.25V		UNITS
		MIN	MAX	MIN	MAX	
t_{ACC}	Access Time from Address		860		700	ns
t_{PD1}, t_{PD0}	Propagation Delay from $\overline{ME}$		660		540	ns
t_{SA}	Address Input Set-Up Time	200		160		ns
t_{HA}	Address Input Hold Time	20		20		ns
t_{ME}	$\overline{Memory\ Enable}$ Pulse Width	280		260		ns
$t_{\overline{ME}}$	$\overline{Memory\ Enable}$ Pulse Width	750		600		ns
t_{SD}	Data Input Set-Up Time	0		0		ns
t_{HD}	Data Input Hold Time	50		50		ns
$t_{\overline{WE}}$	$\overline{Write\ Enable}$ Pulse Width	200		180		ns
t_{1H}, t_{0H}	Delay to TRI-STATE (Note 4)		200		200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

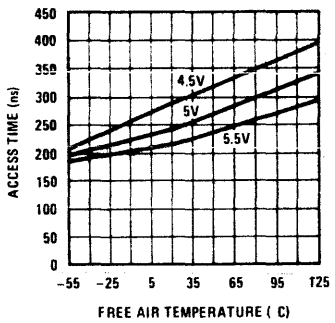
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{pd} determines the no load ac power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Note 4: See ac test circuit for t_{1H}, t_{0H}.

typical performance characteristics

Typical Access Time vs Ambient Temperature

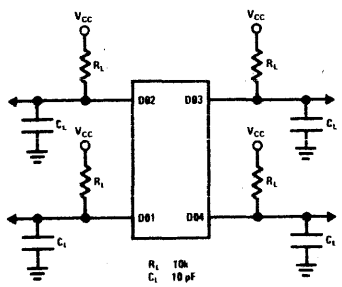


truth table

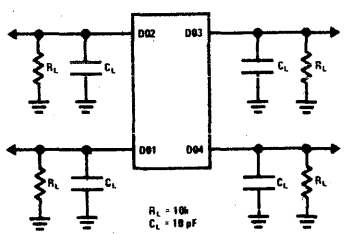
$\overline{ME}$	$\overline{WE}$	OPERATION	OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Data
H	L	Inhibit, Store	TRI-STATE
H	H	Inhibit, Store	TRI-STATE

ac test circuits

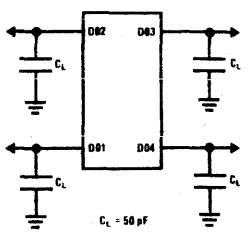
t_{0H}



t_{1H}



All Other AC Tests



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MM54C920/MM74C920, MM54C921/MM74C921
1024-bit static silicon gate CMOS RAMs

general description

The MM54C920/MM74C920 256 x 4 random access read/write memory is manufactured using silicon gate CMOS technology. Data output is the same polarity as data input. Internal latches store address inputs, $\overline{CES}$ and data output. This RAM is specifically designed to operate from standard 54/74 TTL power supplies. All inputs and outputs are TTL compatible.

The MM54C921/MM74C921 is identical to the MM54C920/MM74C920, except data inputs are internally connected to data outputs; the number of package leads thereby is reduced to 18.

Complete address decoding as well as two chip select functions, $\overline{CEL}$ and $\overline{CES}$, and TRI-STATE® outputs allow easy expansion with a minimum of external components. Versatility plus high speed and low power make these RAMs ideal elements for use in microprocessor, minicomputer as well as main frame memory applications.

features

- Fast access—250 ns max
- TRI-STATE outputs
- Low power
- On-chip registers
- Single +5V supply
- Data retained with V_{CC} as low as 2V

functional description

The functional description will reference the logic diagram of the MM54C920/MM74C920 shown in *Figure 1.* Input addresses and $\overline{CES}$ are clocked into the input latches by the falling edge of $\overline{STROBE}$. Input setup and hold times must be observed on these signals (see timing diagrams). The true and complement address information is fed to the row and column decoders which access the selected 4-bit memory word.

logic and connection diagrams

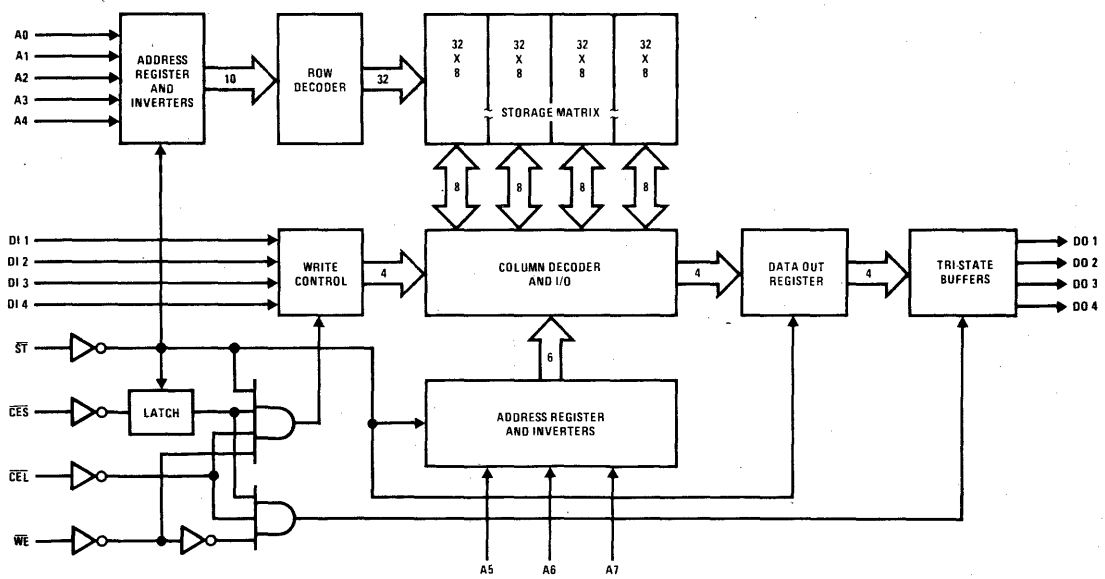
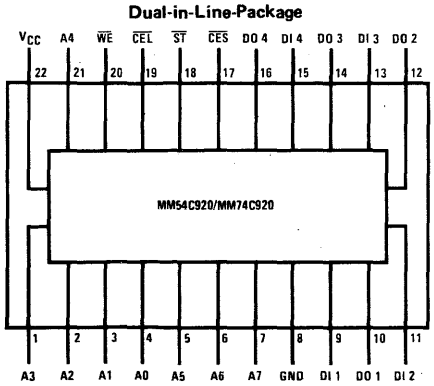
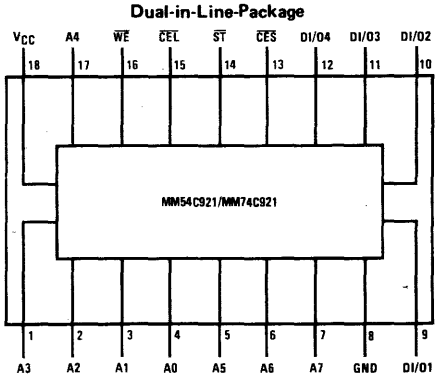


FIGURE 1. MM54C920/MM74C920 Logic Diagram

Dual-in-Line-Package



Dual-in-Line-Package



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functional description (con't)

The addressed word (4 bits) is fed to four sense amplifiers through the column decoders. The information from the sense amplifiers is retained in the output register when $\overline{STROBE}$ rises. The register drives the TRI-STATE output buffers.

Chip select inputs, $\overline{CEL}$ and $\overline{CES}$, have identical functions except that $\overline{CES}$ (Chip Enable Stored) is clocked into a latch on the falling edge of $\overline{STROBE}$; $\overline{CEL}$ (Chip Enable Level) is not.

Note that setup and hold times must be observed on $\overline{CES}$. Because $\overline{CEL}$ is not clocked by $\overline{STROBE}$, it may fall after $\overline{STROBE}$ has fallen without affecting access time.

The outputs are in a high impedance state when the chip is not selected ($\overline{CES}$ or $\overline{CEL}$ high) or when writing ($\overline{WE}$ low). Note that the information stored in the output latches will be changed whenever $\overline{STROBE}$ falls, regardless of the logic states of $\overline{WE}$, $\overline{CEL}$ or $\overline{CES}$.

The timing diagrams in *Figures 2, 3, and 4* define the read, write, and output enable/disable parameters respectively.

absolute maximum ratings

Supply Voltage, V_{CC}	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C920, MM54C921	−55°C to +125°C
MM74C920, MM74C921	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

dc electrical characteristics V_{CC} = 5.0V ±10%, T_A = Operating Range

PARAMETER		CONDITIONS	MM54C920, MM54C921			MM74C920, MM74C921			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	Logical "1" Input Voltage		V_{CC}−2.0		V_{CC}	V_{CC}−2.0		V_{CC}	V
V_{IL}	Logical "0" Input Voltage		0		0.8	0		0.8	V
V_{OH1}	Logical "1" Output Voltage	I_{OH} = −1.0 mA	2.4			2.4			V
V_{OH2}	Logical "1" Output Voltage	I_{OUT} = 0	V_{CC}−0.01			V_{CC}−0.01			V
V_{OL1}	Logical "0" Output Voltage	I_{OL} = 2.0 mA			0.4			0.4	V
V_{OL2}	Logical "0" Output Voltage	I_{OUT} = 0			0.01			0.01	V
I_{IL}	Input Leakage	$0V \le V_{IN} \le V_{CC}$	−1.0	0.001	1.0	−1.0	0.001	1.0	μA
I_Q	Output Leakage	$0V \le V_O \le V_{CC}$, $\overline{CEL}$ = V_{CC}	−1.0	0.001	1.0	−1.0	0.001	1.0	μA
I_{CC}	Supply Current	V_{IN} = V_{CC}, V_O = 0V		0.1	10		0.1	10	μA
C_{IN}	Input Capacitance	(Note 1)		4	7		4	7	pF
C_O	Output Capacitance	(Note 1)		6	9		6	9	pF
$C_{I/O}$	Data Input/Output Capacitance	MM54C921/MM74C921 Only		8	12		8	12	pF
V_{DR}	V_{CC} for Data Retention	$\overline{CEL}$ = V_{CC}	2.0			2.0			V

Note 1: Capacitance is guaranteed by periodic testing.

ac electrical characteristics V_{CC} = 5.0V ±10%, T_A = Operating Range

PARAMETER		MM54C920, MM54C921			MM74C920, MM74C921			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TTL Interface (V_{IH} = V_{CC} − 2.0V, V_{IL} = 0.8V, Input t_{RISE} = t_{FALL} = 5 ns, Load = 1 TTL Gate + 50 pF)								
t_C	Cycle Time	290	120		255	120		ns
t_{ACC}	Access Time From Address		120	275		120	250	ns
t_{ACS}	Access Time From Strobe		110	250		110	225	ns
t_{AS}	Address Setup Time	25	10		25	10		ns
t_{AH}	Address Hold Time	25	15		25	15		ns
t_{OE}	Output Enable Time		60	150		60	130	ns
t_{OD}	Output Disable Time		60	150		60	130	ns
$t_{\overline{ST}}$	$\overline{ST}$ Pulse Width (Negative)	150	60		130	60		ns
t_{ST}	ST Pulse Width (Positive)	140	60		125	60		ns
t_{WP}	Write Pulse Width (Negative)	150	80		130	80		ns
t_{DS}	Data Setup Time	100	40		90	40		ns
t_{DH}	Data Hold Time	60	25		60	25		ns

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MM54C929/MM74C929, MM54C930/MM74C930
1024-bit static silicon gate CMOS RAMs

general description

The MM54C929/MM74C929 and the MM54C930/MM74C930 1024 x 1 random access read/write memories are manufactured using silicon gate CMOS technology. These RAMS are specifically designed to operate from standard 54/74 TTL power supplies; all inputs and outputs are TTL compatible. Data output is the same polarity as data input. Internal latches store the address inputs and data output. Chip select input $\overline{CS1}$ serves as a chip strobe, controlling address and data latching. The Data-In and Data-Out terminals can be tied together for common I/O applications. Complete address decoding, three chip select functions (MM54C930/MM74C930) and TRI-STATE® output allow easy memory expansion and organization. The MM54C929/MM74C929 differs from the MM54C930/MM74C930 only in that $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ are internally connected together, providing a single chip-select input.

Versatility, high speed, and low power make these RAMs ideal elements for use in many microprocessor minicomputer and main frame memory applications.

features

- Fast access—250 ns max
- TRI-STATE outputs
- Low power—10μA max standby
- On-chip registers
- Single 5V supply
- Inputs and output TTL compatible
- Data retained with V_{CC} as low as 2V
- Can be operated common I/O

block and connection diagrams

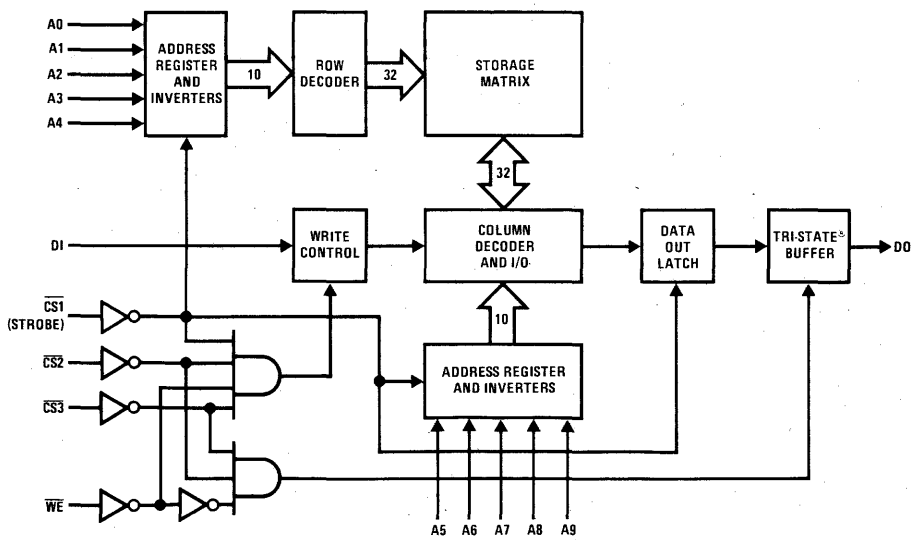
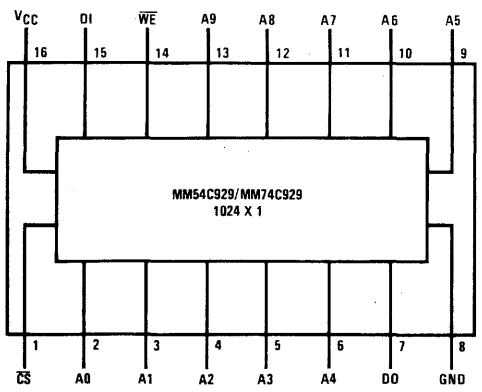
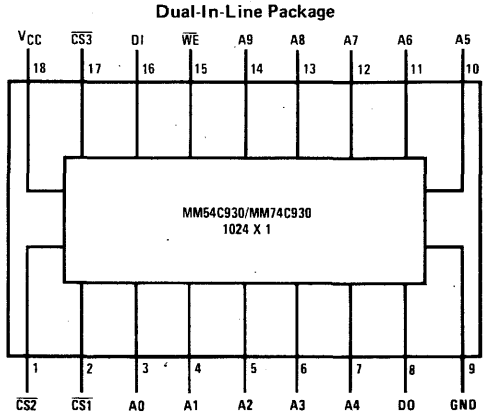


FIGURE 1. Block Diagram

Dual-In-Line Package



Dual-In-Line Package



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absolute maximum ratings

Supply Voltage, V_{CC}	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C929, MM54C930	−55°C to +125°C
MM74C929, MM74C930	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

dc electrical characteristics V_{CC} = 5V ±10%, T_A = Operating Range

PARAMETER		CONDITIONS	MM54C929, MM54C930			MM74C929, MM74C930			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	Logical "1" Input Voltage		V_{CC}−2.0		V_{CC}	V_{CC}−2.0		V_{CC}	V
V_{IL}	Logical "0 ' Input Voltage		0		0.8	0		0.8	V
V_{OH1}	Logical "1" Output Voltage	I_{OH} = −1 mA	2.4			2.4			V
V_{OH2}	Logical "1" Output Voltage	I_{OUT} = 0	V_{CC}−0.01			V_{CC}−0.01			V
V_{OL1}	Logical "0" Output Voltage	I_{OL} = 2 mA			0.4			0.4	V
V_{OL2}	Logical "0 ' Output Voltage	I_{OUT} = 0			0.01			0.01	V
I_{IL}	Input Leakage	$0V \leq V_{IN} \leq V_{CC}$	−1.0	0.001	1.0	−1.0	0.001	1.0	μA
I_O	Output Leakage	$0V \leq V_O \leq V_{CC}$, $\overline{CS2}$ or $\overline{CS3}$ = V_{CC}	−1.0	0.001	1.0	−1.0	0.001	1.0	μA
I_{CC}	Supply Current	$V_{IN} = V_{CC}$, V_O = 0V		0.1	10		0.1	10	μA
C_{IN}	Input Capacitance	(Note 1)		5			5		pF
C_O	Output Capacitance	(Note 1)		5			5		pF
V_{DR}	V_{CC} for Data Retention	$\overline{CS2}$ or $\overline{CS3}$ = V_{CC}	2.0			2.0			V

Note 1: Capacitance maximum is guaranteed by periodic testing.

ac electrical characteristics V_{CC} = 5V ±10%, T_A = Operating Range

PARAMETER		MM54C929, MM54C930			MM74C929, MM74C930			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TTL Interface ($V_{IH} = V_{CC} - 2V$, V_{IL} = 0.8V, Input $t_{RISE} = t_{FALL}$ = 5 ns, Load = 1 TTL Gate + 50 pF)								
t_C	Cycle Time		140			140		ns
t_{ACC}	Access Time From Address		100			100		ns
t_{ACS1}	Access Time From $\overline{CS1}$		100			100		ns
t_{AS}	Address Setup Time		0			0		ns
t_{AH}	Address Hold Time		15			15		ns
t_{OE}	Output Enable Time		60			60		ns
t_{OD}	Output Disable Time		60			60		ns
$t_{\overline{CS1}}$	$\overline{CS1}$ Pulse Width (Negative)		60			60		ns
t_{CS1}	$\overline{CS1}$ Pulse Width (Positive)		60			60		ns
t_{WP}	Write Pulse Width (Negative)		80			80		ns
t_{DS}	Data Setup Time		100			100		ns
t_{DH}	Data Hold Time		0			0		ns

truth tables

MM54C929/MM74C929

$\overline{CS}$	$\overline{WE}$	DI	FUNCTION
1	X	X	Output in Hi-Z State
X	0	X	Output in Hi-Z State
0	0	0	Write "0," Output in Hi-Z State
0	0	1	Write "1," Output in Hi-Z State
0	1	X	Read Data, Output Enabled

X = Don't care

MM54C930/MM74C930

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{WE}$	DI	FUNCTION
X	1	X	X	X	Output in Hi-Z State
X	X	1	X	X	Output in Hi-Z State
X	X	X	0	X	Output in Hi-Z State
0	0	0	0	0	Write "0," Output in Hi-Z State
0	0	0	0	1	Write "1," Output in Hi-Z State
0	0	0	1	X	Read Data, Output Enabled

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MOS EPROMs

MM1702A 2048-bit electrically programmable ROM

general description

The MM1702A is a 256 word by 8-bit electrically programmable ROM ideally suited for uses where fast turn-around and pattern experimentation are important. The MM1702A undergoes complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.

The MM1702AQ is packaged in a 24-pin dual-in-line package with a transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. The MM1702AD is packaged in a 24-pin dual-in-line package with a metal lid and is not erasable.

The circuitry of the MM1702A is entirely static; no clocks are required.

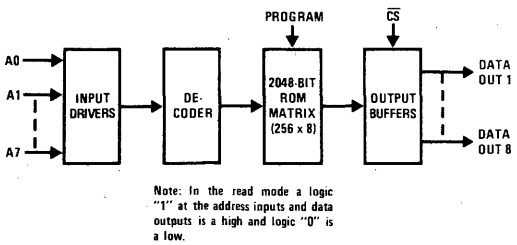
A pin-for-pin metal mask programmed ROM, the MM1302 is ideal for large volume production runs of systems initially using the MM1702A.

The MM1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

features

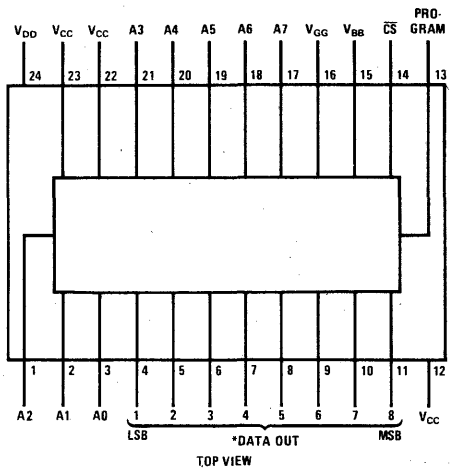
- Fast programming—30 seconds for all 2048 bits
- All 2048 bits guaranteed programmable—100% factory tested
- Fully decoded, 256 x 8 organization
- Static MOS—no clocks required
- Inputs and outputs DTL and TTL compatible
- TRI-STATE® output—OR-tie capability
- Simple memory expansion—chip select input lead
- Direct replacement for the Intel 1702A

block and connection diagrams



Note: In the read mode a logic "1" at the address inputs and data outputs is a high and logic "0" is a low.

Dual-In-Line Package



*This pin is the data input lead during programming.

Order Number MM1702AD
See Package 6
Order Number MM1702AQ
See Package 21

Pin Names

A0–A7	Address Inputs
$\overline{CS}$	Chip Select Input
$D_{OUT\,1} - D_{OUT\,8}$	Data Outputs

Pin Connections*

MODE/PIN	12 (V_{CC})	13 (PROGRAM)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

*The external lead connections to the MM1702A differ, depending on whether the device is being programmed or used in read mode. (See following table.) In the programming mode, the data inputs 1–8 are pins 4–11 respectively.

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absolute maximum ratings (Note 1)

Ambient Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C
Power Dissipation	2W
Read Operation	
Input Voltages and Supply Voltages with Respect to V_{CC}	+0.5V to −20V
Program Operation	
Input Voltages and Supply Voltages with Respect to V_{CC}	−48V
Lead Temperature (Soldering, 10 seconds)	300°C

read operation dc characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5%, unless otherwise noted. Typical values are at nominal voltages and T_A = 25°C. (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Address and Chip Select Input Load Current	V_{IN} = 0.0V			1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} −2			1	μA
I_{DDO}	Power Supply Current	V_{GG} = V_{CC}, $\overline{CS}$ = V_{CC} −2 I_{OL} = 0.0 mA, T_A = 25°C, (Note 2)		5	10	mA
I_{DD1}	Power Supply Current	$\overline{CS}$ = V_{CC} −2, I_{OL} = 0.0 mA, T_A = 25°C		35	50	mA
I_{DD2}	Power Supply Current	$\overline{CS}$ = 0.0, I_{OL} = 0.0 mA, T_A = 25°C		32	46	mA
I_{DD3}	Power Supply Current	$\overline{CS}$ = V_{CC} −2, I_{OL} = 0.0 mA, T_A = 0°C		38.5	60	mA
I_{CF1}	Output Clamp Current	V_{OUT} = −1.0V, T_A = 0°C		8	14	mA
I_{CF2}	Output Clamp Current	V_{OUT} = −1.0, T_A = 25°C			13	mA
I_{GG}	Gate Supply Current				1	μA
V_{IL1}	Input Low Voltage for TTL Interface		−1.0		V_{CC}−4.1	V
V_{IL2}	Input Low Voltage for MOS Interface		V_{DD}		V_{CC}−6	V
V_{IH}	Address and Chip Select Input High Voltage		V_{CC}−2		V_{CC}+0.3	V
I_{OL}	Output Sink Current	V_{OUT} = 0.45V	1.6	4		mA
I_{OH}	Output Source Current	V_{OUT} = 0.0V	−2.0			mA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		−0.7	0.45	V
V_{OH}	Output High Voltage	I_{OH} = −100μA	3.5	4.5		V

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Note 2: Power-Down Option: V_{GG} may be clocked to reduce power dissipation. The average I_{DD} will vary between I_{DD0} and I_{DD1} depending on the V_{GG} duty cycle (see typical characteristics). For this option, please specify MM1702AL.

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read operation ac characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5%, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNITS
Freq.	Repetition Rate			1	MHz
t_{0H}	Previous Read Data Valid			100	ns
t_{ACC}	Address to Output Delay		0.7	1	μs
t_{DVGG}	Clocked V_{GG} Set-Up (Note 1)	1			μs
t_{CS}	Chip Select Delay			100	ns
t_{CO}	Output Delay From $\overline{CS}$			900	ns
t_{0D}	Output Deselect			300	ns
t_{0HC}	Data Out Hold in Clocked V_{GG} Mode (Note 1)			5	μs

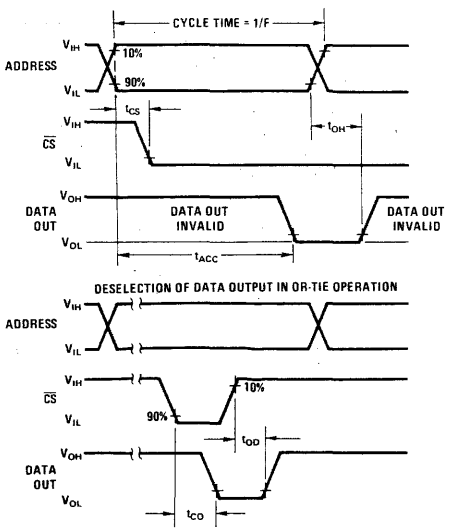
capacitance characteristics T_A = 25°C (Note 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	All Unused	$V_{IN} = V_{CC}$		8	15	pF
C_{OUT}	Output Capacitance	Pins Are	$\overline{CS} = V_{CC}$		10	15	pF
C_{VGG}	V_{GG} Capacitance (Note 1)	At ac Ground	$V_{OUT} = V_{CC}$ $V_{GG} = V_{CC}$			30	pF

Note 3: This parameter is periodically sampled and is not 100% tested.

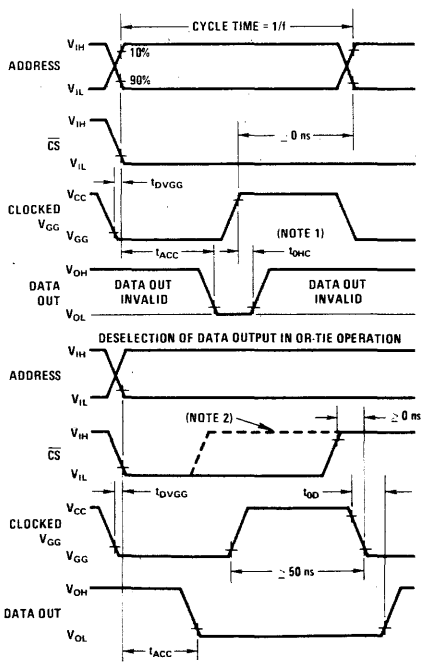
read operation switching time waveforms

(a) Constant V_{GG} Operation



Conditions of Test:
Input pulse amplitudes: 0–4V, t_r, $t_f \leq$ 50 ns. Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{PD} \leq$ 15 ns), C_L = 15 pF.

(b) Power-Down Option (Note 1)



Note 1: The output will remain valid for t_{0HC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

Note 2: If $\overline{CS}$ makes a transition from V_{IL} to V_{IH} while clocked V_{GG} is at V_{GG}, then deselection of output occurs at t_{0D} as shown in static operation with constant V_{GG}.

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programming operation dc characteristics

$T_A = 25°C$, $V_{CC} = 0V$, $V_{BB} = 12V \pm 10\%$, $\overline{CS} = 0V$ unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI1P}	Address and Data Input Load Current	$V_{IN} = -48V$			10	mA
I_{LI2P}	Program and V_{GG} Load Current	$V_{IN} = -48V$			10	mA
I_{BB}	V_{BB} Supply Load Current	(Note 5)		10	100	mA
I_{DDP}	Peak I_{DD} Supply Load Current	$V_{DD} = V_{PROG} = -48V$ $V_{GG} = -35V$ (Note 4)		200	300	mA
V_{IHP}	Input High Voltage				0.3	V
V_{IL1P}	Pulsed Data Input Low Voltage		−46		−48	V
V_{IL2P}	Address Input Low Voltage		−40		−48	V
V_{IL3P}	Pulsed Input Low V_{DD} and Program Voltage		−46		−48	V
V_{IL4P}	Pulsed Input Low V_{GG} Voltage		−35		−40	V

Note 4: I_{DDP} flows only during V_{DD}, V_{GG} on time. I_{DDP} should not be allowed to exceed 300 mA for greater than 100μs. Average power supply current I_{DDP} is typically 40 mA at 20% duty cycle.

Note 5: The V_{BB} supply must be limited to 100 mA max current to prevent damage to the device.

programming operation ac characteristics

$T_A = 25°C$, $V_{CC} = 0V$, $V_{BB} = 12V \pm 10\%$, $\overline{CS} = 0V$ unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
	Duty Cycle (V_{DD}, V_{GG})				20	%
$t_{\phi PW}$	Program Pulse Width	$V_{GG} = -35V$, $V_{DD} = V_{PROG} = -48V$			3	ms
t_{DW}	Data Set-Up Time		25			μs
t_{DH}	Data Hold Time		10			μs
t_{VW}	V_{DD}, V_{GG} Set-Up		100			μs
t_{VD}	V_{DD}, V_{GG} Hold		10		100	μs
t_{ACW}	Address Complement Set-Up	(Note 6)	25			μs
t_{ACH}	Address Complement Hold	(Note 6)	25			μs
t_{ATW}	Address True Set-Up		10			μs
t_{ATH}	Address True Hold		10			μs

Note 6: All 8 address bits must be in the complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses (0–255) must be programmed as shown in the timing diagram until data reads true, then over-programmed 4 times that amount. (Symbolized by x + 4x.)

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MOS EPROMs

MM4204/MM5204
electrically programmable 4096-bit read only memory (EROM)

general description

The MM4204/MM5204 is a 4096-bit static Read Only Memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatiblity. The device is a non-volatile memory organized as 512 words by 8 bits per word. Programming of the memory is accomplished by storing a charge in a cell location by applying a −50V pulse. A logic input, "Power Saver," is provided which gives a 5:1 decrease in power when the memory is not being accessed.

- Standard power supplies 5.0V, −12V
- Static operation—no clock required
- Easy memory expansion—TRI-STATE® output Chip Select input ($\overline{CS}$)
- "Q" quartz lid version erasable with short wave ultraviolet light (i.e., 253.7 nm)
- Low power dissipation
- "Power Saver" control for low power applications

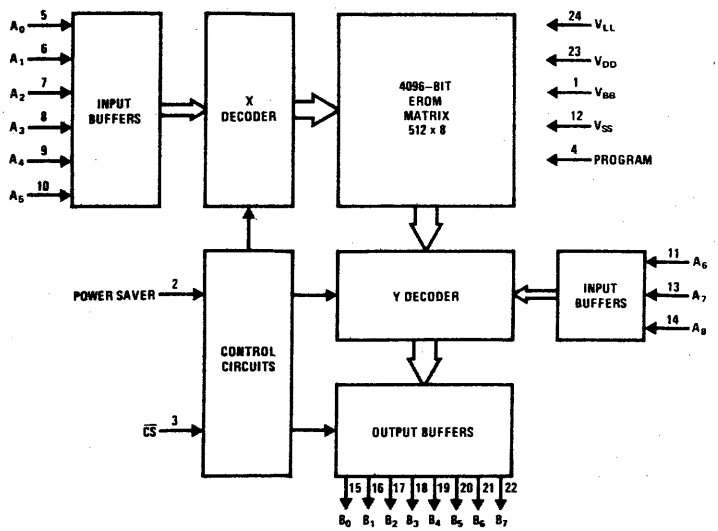
features

- Field programmable
- Fast program time: ten seconds typical for 4096-bits
- Fast access time
  - MM4204 1.25μs
  - MM5204 1μs
- DTL/TTL compatibility

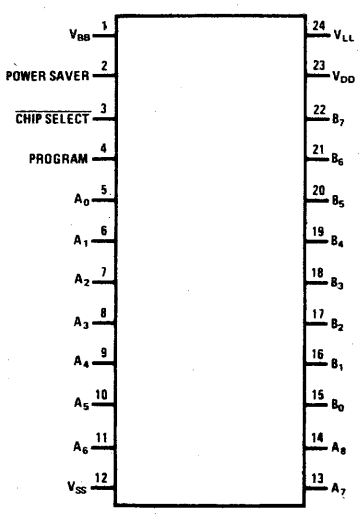
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming
- Electronic keyboards

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM4204D or MM5204D
See Package 6

Order Number MM4204Q or MM5204Q
See Package 21

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absolute maximum ratings (Note 1)

All Input or Output Voltages with Respect to V_{BB} Except During Programming	+0.3V to −20V
Power Dissipation	750 mW
Operating Temperature Range	
MM5204	0°C to +70°C
MM4204	−55°C to +85°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

T_A within operating temperature range, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, MM4204: V_{SS} = 5.0V ±10%, V_{DD} = −12V ±10%, MM5204: V_{SS} = 5.0V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
V_{IL}	Input Low Voltage		V_{SS}−14		V_{SS}−4.2	V
V_{IH}	Input High Voltage		V_{SS}−1.5		V_{SS}+0.3	V
I_{LI}	Input Current	V_{IN} = 0V			1.0	μA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	V_{LL}		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −0.8 mA	2.4		V_{SS}	V
I_{LO}	Output Leakage Current	V_{OUT} = 0V, $\overline{CS}$ = V_{IH}			1.0	μA
I_{DD}	Power Supply Current	MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}		28	40.0	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			50.0	mA
		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}		6.0	8.0	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			10.0	mA
I_{SS}		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			42	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			52	mA
		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			10	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			12	mA

ac electrical characteristics

T_A within operating temperature range, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, MM4204: V_{SS} = 5.0V ±10%, V_{DD} = −12V ±10%, MM5204: V_{SS} = 5.0V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
t_{ACC}	Access Time					
	MM5204	T_A = 70°C, (Note 4)		0.75	1.0	μs
	MM4204	T_A = 85°C, (Note 4)			1.25	μs
t_{PO}	Power Saver Set-Up Time					
	MM5204				1.8	μs
	MM4204				2.0	μs
t_{CO}	Chip Select Delay					
	MM5204				500	ns
	MM4204				600	ns
t_{OH}	Data Hold Time		30	50		ns
t_{ODC}	Chip Select Deselect Time					
	MM5204		30	300	500	ns
	MM4204		30	300	600	ns
t_{ODP}	Power Saver Deselect Time					
	MM5204		30	300	500	ns
	MM4204		30	300	600	ns
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = V_{SS}, f = 1.0 MHz, (Note 2)		5.0	8.0	pF
C_{OUT}	Output Capacitance (All Outputs)	V_{OUT} = V_{SS}, $\overline{CS}$ = V_{IH}, f = 1.0 MHz, (Note 2)		8.0	15	pF

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programmer electrical characteristics

$T_A = 25°C$, $V_{SS} = \overline{CS}$ = Power Saver = 0V, V_{LL} = 0V to −14V, unless otherwise specified, (Note 5).

PARAMETER		CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
I_{LD}	Data Input Load Current	V_{IN} = −18V			−10	mA
I_{ALD}	Address Input Load Current	V_{IN} = −50V			−10	mA
I_{LP}	Program Load Current	V_{IN} = −50V			−10	mA
I_{LBB}	V_{BB} Load Current				50	mA
I_{LDD}	V_{DD} Load Current	V_{DD} = PROGRAM = −50V			−200	mA
V_{IHP}	Address Data and Power Saver Input High Voltage		−2.0		0.3	V
V_{ILP}	Address Input Low Voltage		−50		−11	V
	Data Input Low Voltage		−18		−11	V
V_{DHP}	V_{DD} and Program High Voltage		−2.0		0.5	V
V_{DLP}	V_{DD} and Program Low Voltage		−50		−48	V
V_{BLP}	V_{BB} Low Voltage		0		0.4	V
V_{BHP}	V_{BB} High Voltage		11.4		12.6	V
V_{DD}	Pulse Duty Cycle				25	%
t_{PW}	Program Pulse Width		0.5		5.0	ms
t_{DS}	Data and Address Set-Up Time		40			μs
t_{DH}	Data and Address Hold Time		0			μs
t_{SS}	Pulsed V_{DD} Set-Up Time		40		100	μs
t_{SH}	Pulsed V_{DD} Hold Time		1.0			μs
t_{BS}	Pulsed V_{BB} Set-Up Time		1.0			μs
t_{BH}	Pulsed V_{BB} Hold Time		1.0			μs
t_{PSS}	Power Saver Set-Up Time		1.0			μs
t_{PSH}	Power Saver Hold Time		1.0			μs
t_R, t_F	V_{DD}, Program, Address and Data Rise and Fall Time				1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used except on data inputs during programming
Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: t_{ACC} = 1000 ns + 25 (N-1) where N is the number of devices wire—OR'd together.

Note 5: The program cycle should be repeated until the data reads true, then over-programmed 5 times that number of cycles. (Symbolized as X + 5X programming).

Note 6: The EROM is initially programmed with all "0's." A V_{IHP} on any data input B0—B7 will leave the stored "0's" undisturbed, and a V_{ILP} on any data input B0—B7 will write a logic "1" into that location.

Note 7: Typical values are for nominal voltages and $T_A = 25°C$, unless otherwise specified.

erase specification

The recommended dosage of ultraviolet light exposure is 6W sec/cm².

programming

The MM4204/MM5204 is normally shipped in the unprogrammed state. All 4096-bits are at logic "0" state. The table of electrical programming characteristics and *Figure 2* give the conditions for programming of the device. In the program mode the device effectively becomes a RAM with the 512 word locations selected by address inputs A0—A8. Data inputs are B0—B7 and write operation is controlled by pulsing the Program input. Since the EROM is initially shipped with all "0's," a V_{IHP} on any data input B0—B7 will leave the stored "0's" undisturbed and a V_{ILP} on any data input B0—B7 will write a logic "1" into that location.

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MM2316A 16,384-bit read only memory

general description

The MM2316A is a static MOS 16,384-bit read-only memory organized in a 2048-word-by-8-bit format. It is fabricated using N-channel enhancement and depletion-mode silicon-gate technology which provides complete DTL/TTL compatibility and single power-supply operation.

Three programmable chip selects controlling the TRI-STATE® outputs allow for memory expansion.

Programming of the memory array and chip-select active levels is accomplished by changing one mask during fabrication.

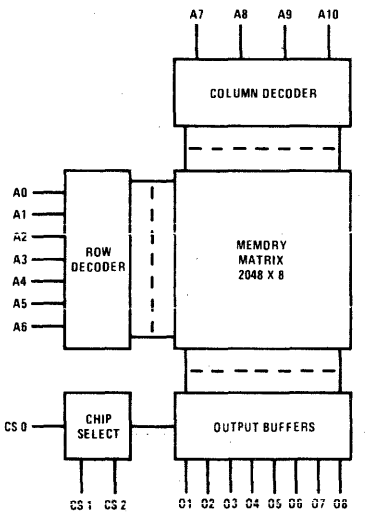
features

- Fully decoded
- Single 5V power supply
- Inputs and outputs TTL compatible
- Static operation
- TRI-STATE outputs for bus interface
- Programmable chip selects
- 2048 word by 8-bit organization
- Maximum access time—450 ns

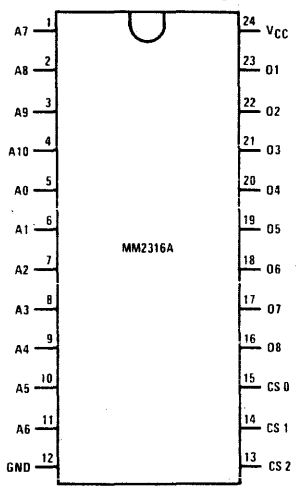
applications

- Microprogramming
- Control logic
- Table look-up

block and connection diagrams

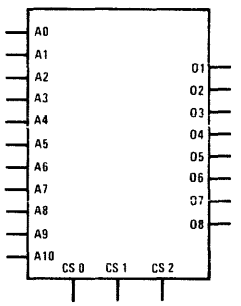


Dual-In-Line Package

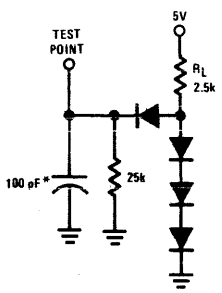


TOP VIEW

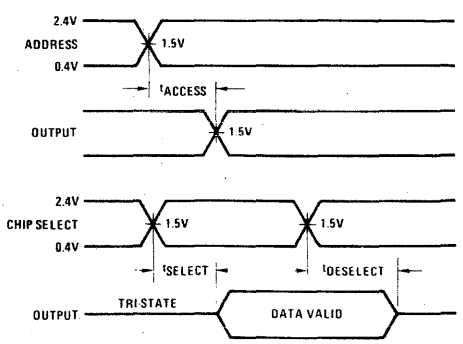
logic symbol



ac test circuit and switching time waveforms



*Includes jig capacitance



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absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.5V to +7V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics (T_A within operating temperature range, V_{CC} = 5V ±5%, unless otherwise noted).

PARAMETER (Note 3)	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Input Current (I_{LI})	V_{IN} = 0 to V_{CC}			10	μA
Logical "1" Input Voltage (V_{IH})		2.0		V_{CC}+1.0	V
Logical "0" Input Voltage (V_{IL})		−0.5		0.8	V
Logical "1" Output Voltage (V_{OH})	I_{OH} = −100 μA	2.2			V
Logical "0" Output Voltage (V_{OL})	I_{OL} = 2 mA			0.45	V
Output Leakage Current (I_{LOH})	V_{OUT} = 4V, CS = 2.2V			10	μA
Output Leakage Current (I_{LOL})	V_{OUT} = 0.45V, CS = 2.2V			−20	μA
Power Supply Current (I_{CC1}) (Note 4)	All Inputs = 5.25V, Data Output Open		40	98	mA

capacitance

PARAMETER (Note 3)	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Input Capacitance (All Inputs) (C_{IN}), (Note 4)	V_{IN} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			7.5	pF
* Output Capacitance (C_{OUT}), (Note 4)	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			15.0	pF

ac electrical characteristics

(T_A within operating temperature range, V_{CC} = 5V ±5%, unless otherwise specified).
See ac test circuit and switching time waveforms.

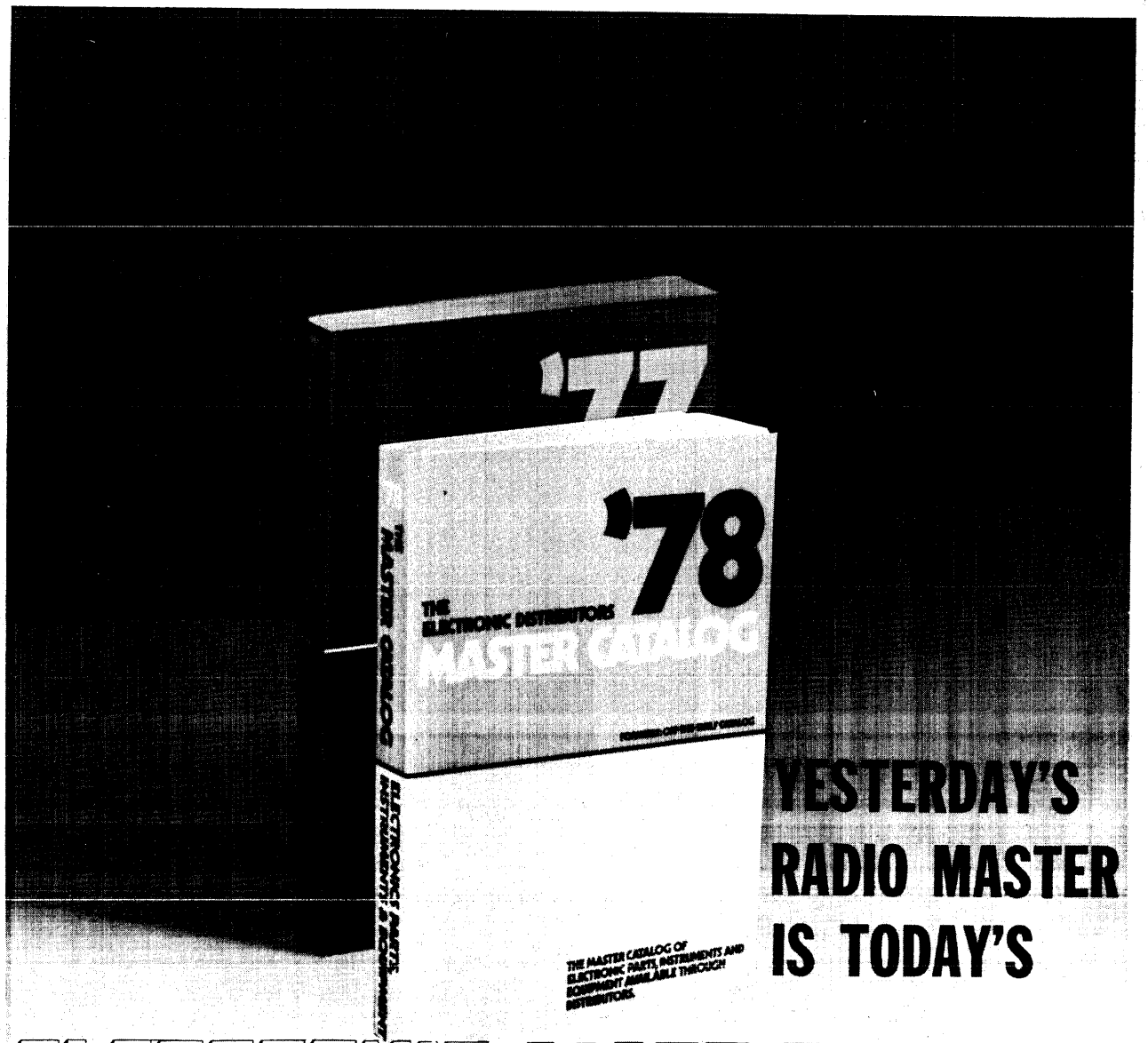
PARAMETER (Note 3)	CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
t_{ACCESS}	See ac Load Circuit. All Times Measured to 1.5V Level with t_r and t_f of Input < 20 ns			450	ns
t_{SELECT}	See ac Load Circuit. All Times Measured to 1.5V Level with t_r and t_f of Input < 20 ns			300	ns
$t_{DESELECT}$	See ac Load Circuit. All Times Measured to 1.5V Level with t_r and t_f of Input < 20 ns			300	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: logical "1" = most positive voltage level, logical "0" = most negative voltage level.

Note 4: Typical values are for T_A = 25°C and nominal supply voltage.



ELECTRONIC DISTRIBUTORS MASTER CATALOG

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The **MANUFACTURERS' CATALOG SECTION** is a collection of their respective product pages, alphabetically by manufacturer, again including addresses and phone numbers.

The **MANUFACTURERS DIRECTORY** is an alphabetical listing of all manufacturers whose products information is shown. Page numbers are referenced. Sales offices, representatives and distributors are included for many manufacturers.

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μPD411-E
μPD411
μPD411-1
μPD411-2
μPD411-3
μPD411-4

FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION

The μPD411 Family consists of six 4096 words by 1 bit dynamic N-channel MOS RAMs. They are designed for memory applications where very low cost and large bit storage are important design objectives. The μPD411 Family is designed using dynamic circuitry which reduces the standby power dissipation.

Reading information from the memory is a non-destructive. Refreshing is easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic high or a logic low.

FEATURES

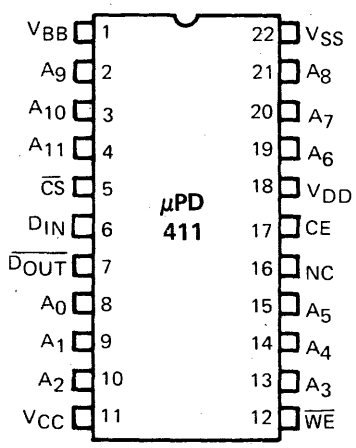
All of these products are guaranteed for operation over the 0 to 70°C temperature range.

Important features of the μPD411 family are:

- Low Standby Power
- 4096 words x 1 bit Organization
- A single low-capacitance high level clock input with solid ±1 volt margins.
- Inactive Power/0.3 mW (Typ.)
- Power Supply: +12, +5, -5V
- Easy System Interface
- TTL Compatible (Except CE)
- Address Registers on the Chip
- Simple Memory Expansion by Chip Select
- Three State Output and TTL Compatible
- 22 pin Ceramic Dual-in-Line Package
- Replacement for INTEL'S 2107B, TI'S 4060 and Equivalent Devices.
- 4 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE	REFRESH TIME
μPD411-E	350 ns	800 ns	960 ns	1 ms
μPD411	300 ns	470 ns	650 ns	2 ms
μPD411-1	250 ns	470 ns	640 ns	2 ms
μPD411-2	200 ns	400 ns	520 ns	2 ms
μPD411-3	150 ns	380 ns	470 ns	2 ms
μPD411-4	135 ns	320 ns	320 ns	2 ms

PIN CONFIGURATION



PIN NAMES

$A_0 - A_{11}$	Address Inputs
$A_0 - A_5$	Refresh Addresses
CE	Chip Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
$\overline{D_{OUT}}$	Data Output
$\overline{WE}$	Write Enable
V_{DD}	Power (+12V)
V_{CC}	Power (+5V)
V_{SS}	Ground
V_{BB}	Power (-5V)
NC	No Connection

Rev/2

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FUNCTIONAL DESCRIPTION

CE Chip Enable

A single external clock input is required. All read, write, refresh and read-modify-write operations take place when chip enable input is high. When the chip enable is low, the memory is in the low power standby mode. No read/write operations can take place because the chip is automatically precharging.

$\overline{CS}$ Chip Select

The chip select terminal affects the data in, data out and read/write inputs. The data input and data output terminals are enabled when chip select is low. The chip select input must be low on or before the rising edge of the chip enable and can be driven from standard TTL circuits. A register for the chip select input is provided on the chip to reduce overhead and simplify system design.

$\overline{WE}$ Write Enable

The read or write mode is selected through the write enable input. A logic high on the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The $\overline{WE}$ terminal can be driven from standard TTL circuits. The data input is disabled when the read mode is selected.

A_0–A_{11} Addresses

All addresses must be stable on or before the rising edge of the chip enable pulse. All address inputs can be driven from standard TTL circuits. Address registers are provided on the chip to reduce overhead and simplify system design.

D_{IN} Data Input

Data is written during a write or read-modify-write cycle while the chip enable is high. The data in terminal can be driven from standard TTL circuits. There is no register on the data in terminal.

$\overline{D_{OUT}}$ Data Output

The three state output buffer provides direct TTL compatibility with a fan-out of two TTL gates. The output is in the high-impedance (floating) state when the chip enable is low or when the Chip Select input is high. Data output is inverted from data in.

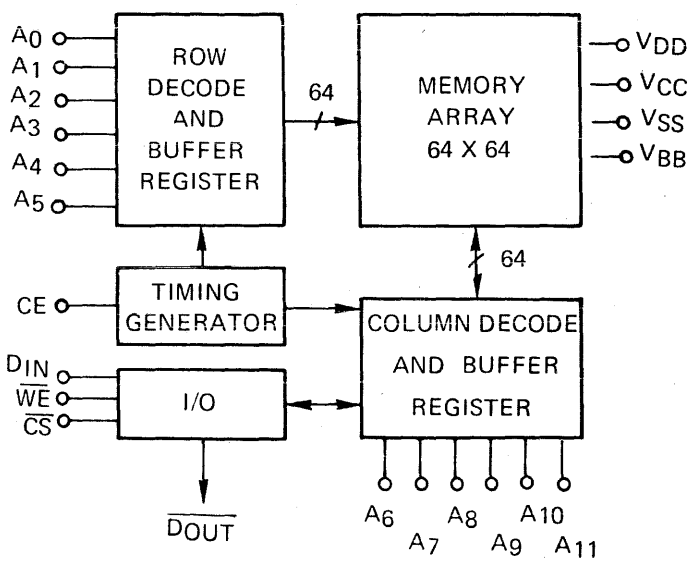
Refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs A_0 through A_5 or by addressing every row within any 2*-millisecond period. Addressing any row refreshes all 64 bits in that row.

The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, the chip select must be high.

*μPD411-E = 1 millisecond refresh period.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS*

	μPD411 FAMILY (EXCEPT 411-4)	μPD411-4
Operating Temperature	0°C to +70°C	+10°C to +55°C
Storage Temperature	−55°C to +150°C	−55°C to +150°C
All Output Voltages	−0.3 to +20 Volts	−0.3 to +25 Volts ①
All Input Voltages	−0.3 to +20 Volts	−0.3 to +25 Volts ①
Supply Voltage V_{DD}	−0.3 to +20 Volts	−0.3 to +25 Volts ①
Supply Voltage V_{CC}	−0.3 to +20 Volts	−0.3 to +25 Volts ①
Power Dissipation	1.0W	1.5W

Note: ① Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V,
Except V_{DD} = +15V ±5% for 411-4.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current	I_{LI}		0.01	10	μA	V_{IN} = V_{IL} MIN to V_{IH} MAX
CE Input Load Current	I_{LC}		0.01	10	μA	V_{IN} = V_{ILC} MIN to V_{IHC} MAX
Output Leakage Current for High Impedance State	I_{LO}		0.01	±10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
V_{DD} Supply Current during CE off	I_{DD} OFF		20	200	μA	CE = 1.0V to 0.6V
V_{DD} Supply Current during CE on	I_{DD} ON		35*	60⑤	mA	CE = V_{IHC}, T_a = 25°C
Average V_{DD} Current						T_a = 25°C
μPD411-E	I_{DD} AV		29	60	mA	Cycle Time = 800 ns
μPD411	I_{DD} AV		37	60	mA	Cycle Time = 470 ns
μPD411-1	I_{DD} AV		37	60	mA	Cycle Time = 470 ns
μPD411-2	I_{DD} AV		37	60	mA	Cycle Time = 400 ns
μPD411-3	I_{DD} AV		41	65	mA	Cycle Time = 380 ns
μPD411-4	I_{DD} AV		55	80	mA	Cycle Time = 320 ns
V_{BB} Supply Current ②	I_{BB}		5	100	μA	
V_{CC} Supply Current during CE off ③	I_{CC} OFF		0.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
Input Low Voltage	V_{IL}	-1.0		0.6	V	
Input High Voltage	V_{IH}	2.4 ④		V_{CC}+1	V	
CE Input Low Voltage	V_{ILC}	-1.0		0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD}−1	V_{DD}	V_{DD}+1	V	
Output Low Voltage	V_{OL}	0		0.40	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −2.0 mA

Notes: ① Typical values are for T_a = 25°C and nominal power supply voltages.
② The I_{BB} current is the sum of all leakage currents.
③ During CE on V_{CC} supply current is dependent on output loading.
V_{CC} is connected to output buffer only.
④ 3.5V for μPD411-E
⑤ 65 mA for μPD411-3
80 mA for μPD411-4
⑥ 41 mA for μPD411-3
55 mA for μPD411-4

CAPACITANCE

T_a = 0° − 70°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address Capacitance, $\overline{CS}$	C_{AD}		4	6	pF	V_{IN} = V_{SS}
CE Capacitance	C_{CE}		18	27	pF	V_{IN} = V_{SS}
Data Output Capacitance	C_{OUT}		5	7	pF	V_{OUT} = 0V
D_{IN} and $\overline{WE}$ Capacitance	C_{IN}		8	10	pF	V_{IN} = V_{SS}

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READ CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise noted,
Except V_{DD} = +15V ± 5% for 411-4

PARAMETER	SYMBOL	LIMITS												UNIT
		μPD411-E		μPD411		μPD411-1		μPD411-2		μPD411-3		μPD411-4		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Time Between Refresh	t_{REF}		1		2		2		2		2		2	ms
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		0		ns
Address Hold Time	t_{AH}	150		150		150		150		150		100		ns
CE Off Time	t_{CC}	380		130		170		130		130		80		ns
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	0	40	ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	0	130	0	130	ns
Cycle Time	t_{CY}	800		470		470		400		380		320		ns
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	210	3000	200	3000	ns
CE Output Delay	t_{CO}		330		280		230		180		130		115	ns
Access Time	t_{ACC}		350		300		250		200		150		135	ns
CE to $\overline{WE}$	t_{WL}	40		40		40		40		40		40		ns
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		0		0		ns

WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise noted,
Except V_{DD} = +15V ± 5% for 411-4

PARAMETER	SYMBOL	LIMITS												UNIT
		μPD411-E		μPD411		μPD411-1		μPD411-2		μPD411-3		μPD411-4		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	t_{CY}	800		470		470		400		380		320		ns
Time Between Refresh	t_{REF}		1		2		2		2		2		2	ms
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		0		ns
Address Hold Time	t_{AH}	150		150		150		150		150		100		ns
CE Off Time	t_{CC}	380		130		170		130		130		80		ns
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	0	40	ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	0	130	0	130	ns
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	210	3000	200	3000	ns
$\overline{WE}$ to CE off	t_W	200		180		180		150		150		65		ns
CE to $\overline{WE}$	t_{CW}	380		300		260		230		210		200		ns
D_{IN} to $\overline{WE}$ Set Up ①	t_{DW}	0		0		0		0		0		0		ns
D_{IN} Hold Time	t_{DH}	40		40		40		40		40		40		ns
$\overline{WE}$ Pulse Width	t_{WP}	200		180		180		150		100		65		ns

Note: ① If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.

READ-MODIFY-WRITE CYCLE

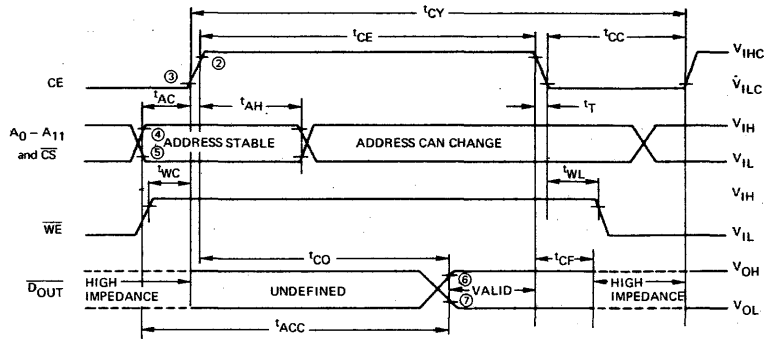
T_a = 0 C to 70 C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, unless otherwise noted,
Except V_{DD} = +15V ± 5% for 411-4

PARAMETER	SYMBOL	LIMITS												UNIT
		μPD411-E		μPD411		μPD411-1		μPD411-2		μPD411-3		μPD411-4		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read–Modify–Write (RMW) Cycle Time	t_{RWC}	960		650		640		520		470		320		ns
Time Between Refresh	t_{REF}		1		2		2		2		2		2	ms
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		0		ns
Address Hold Time	t_{AH}	150		150		150		150		150		100		ns
CE Off Time	t_{CC}	380		130		170		130		130		80		ns
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	0	40	ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	0	130	0	130	ns
CE Width During RMW	t_{CRW}	540	3000	480	3000	430	3000	350	3000	300	3000	200	3000	ns
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		0		0		ns
$\overline{WE}$ to CE off	t_W	200		180		180		150		150		65		ns
$\overline{WE}$ Pulse Width	t_{WP}	200		180		180		150		100		65		ns
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		0		0		0		ns
D_{IN} Hold Time	t_{DH}	40		40		40		40		40		40		ns
CE to Output Display	t_{CO}		330		280		230		180		130		115	ns
Access Time	t_{ACC}		350		300		250		200		150		135	ns

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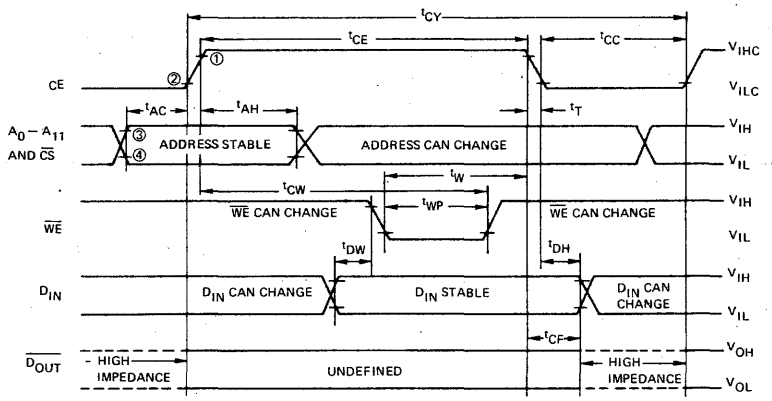
TIMING WAVEFORMS

READ CYCLE ①



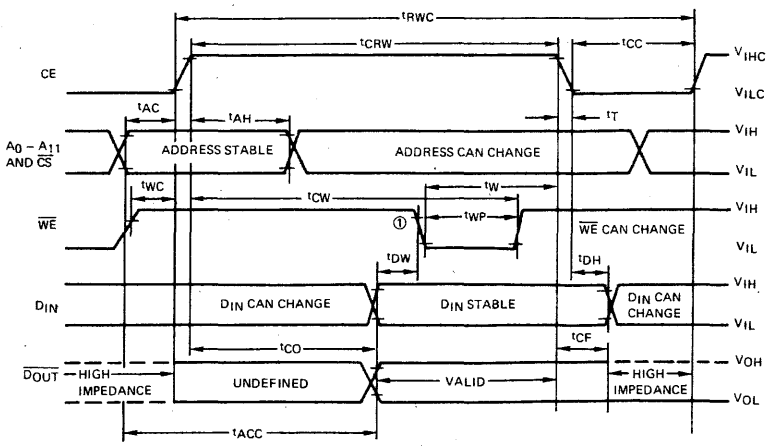
Notes: ① For refresh cycle row and column addresses must be stable t_{AC} and remain stable for entire t_{AH} period.
② V_{DD} -2V is the reference level for measuring timing of CE.
③ V_{SS} +2V is the reference level for measuring timing of CE.
④ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
⑤ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
⑥ V_{SS} +2.0V is the reference level for measuring timing of $\overline{D_{OUT}}$.
⑦ V_{SS} +0.8V is the reference level for measuring timing of $\overline{D_{OUT}}$.

WRITE CYCLE



Notes: ① V_{DD} -2V is the reference level for measuring timing of CE.
② V_{SS} +2V is the reference level for measuring timing of CE.
③ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
④ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

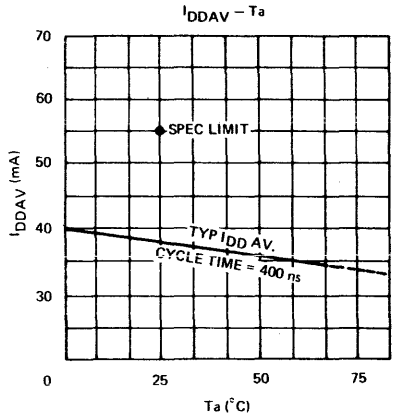
READ-MODIFY-WRITE CYCLE

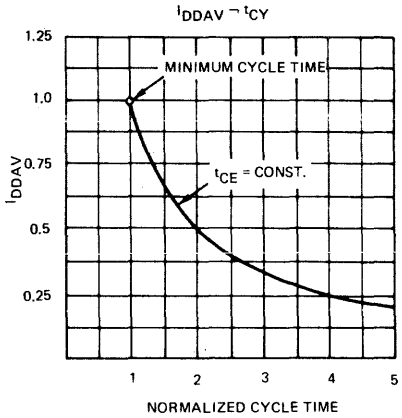


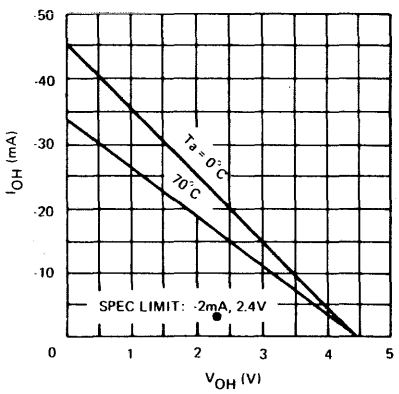
Note: ① $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

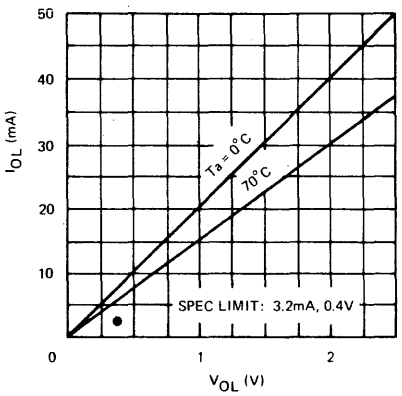
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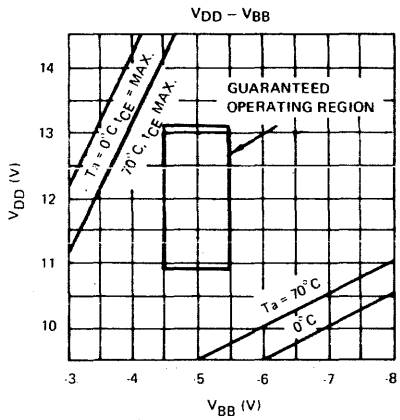
TYPICAL OPERATING CHARACTERISTICS (Except 411-4)

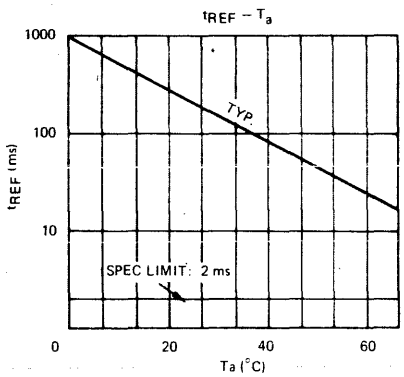












POWER CONSUMPTION

Power consumption = $V_{DD} \times I_{DDAV} + V_{BB} \times I_{BB}$.

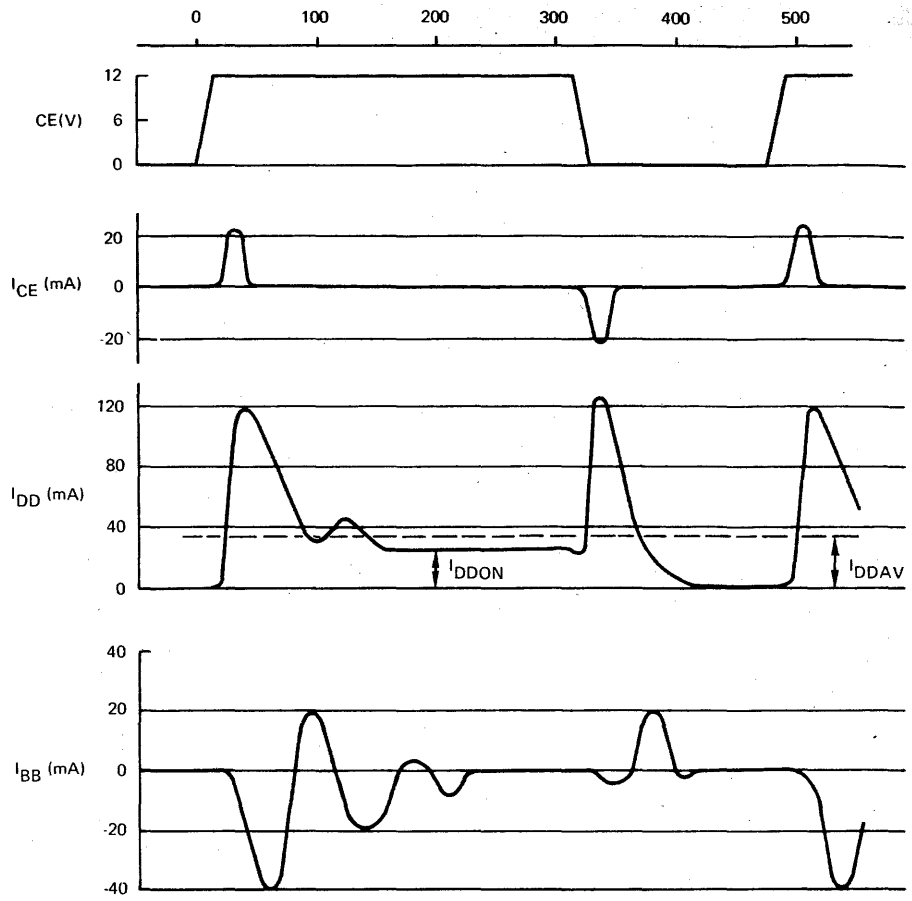
Typical power dissiption for each product is shown below.

	mW (TYP.)	CONDITIONS
μPD411-E	350	Ta = 25° C, t_{cy} = 800ns, t_{CE} = 380ns
μPD411	450	Ta = 25° C, t_{cy} = 470ns, t_{CE} = 300ns
μPD411-1	450	Ta = 25° C, t_{cy} = 470ns, t_{CE} = 260ns
μPD411-2	450	Ta = 25° C, t_{cy} = 400ns, t_{CE} = 230ns
μPD411-3	550	Ta = 25° C, t_{cy} = 380ns, t_{CE} = 210ns
μPD411-4	660	Ta = 25° C, t_{cy} = 320ns, t_{CE} = 200ns

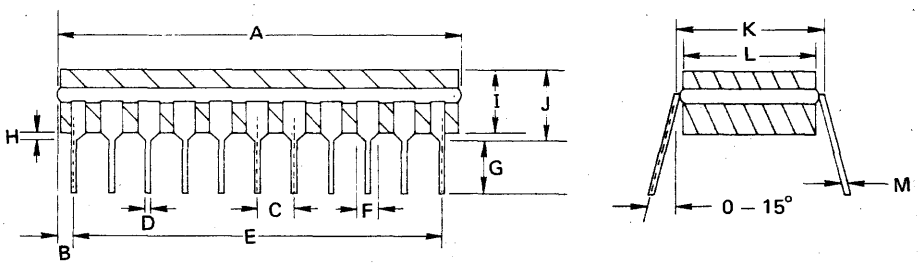
See above curves for power dissipation versus cycle time.

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CURRENT WAVEFORMS



PACKAGE OUTLINE μPD411D



ITEM	MILLIMETERS	INCHES
A	27.43 MAX	1.079 MAX
B	1.27 MAX	0.05 MAX
C	2.54 ± 0.1	0.10
D	0.42 ± 0.1	0.016
E	25.4 ± 0.3	1.0
F	1.5 ± 0.2	0.059
G	3.5 ± 0.3	0.138
H	3.7 ± 0.3	0.145
I	4.2 MAX	0.165 MAX
J	5.08 MAX	0.200 MAX
K	10.16 ± 0.15	0.400
L	9.1 ± 0.2	0.358
M	0.25 ± 0.05	0.009

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μPD411A-E
μPD411A
μPD411A-1
μPD411A-2

4096 BIT DYNAMIC RAMS

DESCRIPTION

The μPD411A Family consists of four 4096 words by 1 bit dynamic N-channel MOS RAMs. They are designed for memory applications where very low cost and large bit storage are important design objectives. The μPD411A Family is designed using dynamic circuitry which reduces the standby power dissipation.

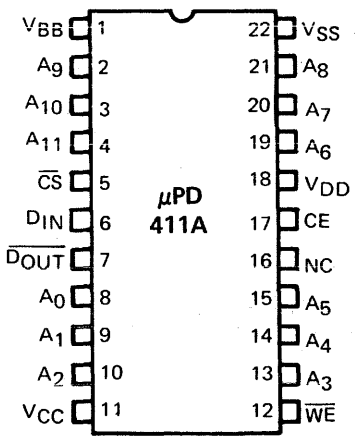
Reading information from the memory is non-destructive. Refreshing is easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic high or a logic low.

FEATURES

- Low Standby Power
- 4096 words x 1 bit Organization
- A single low-capacitance high level clock input with solid ±1 volt margins.
- Inactive Power 0.7 mW (Typ.)
- Power Supply +12, +5, −5V
- Easy System Interface
- TTL Compatible (Except CE)
- Address Registers on the Chip
- Simple Memory Expansion by Chip Select
- Three State Output and TTL Compatible
- 22 pin Plastic Dual-in-Line Package
- Replacement for INTEL's 2107B, TI's 4060 and Equivalent Devices.
- 4 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE	REFRESH TIME
μPD411A-E	350 ns	800 ns	960 ns	1 ms
μPD411A	300 ns	470 ns	650 ns	2 ms
μPD411A-1	250 ns	430 ns	600 ns	2 ms
μPD411A-2	200 ns	400 ns	520 ns	2 ms

PIN CONFIGURATION



PIN NAMES

$A_0 - A_{11}$	Address Inputs
$A_0 - A_5$	Refresh Addresses
CE	Chip Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
$\overline{D_{OUT}}$	Data Output
$\overline{WE}$	Write Enable
V_{DD}	Power (+12V)
V_{CC}	Power (+5V)
V_{SS}	Ground
V_{BB}	(Power −5V)
NC	No Connection

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FUNCTIONAL DESCRIPTION

CE Chip Enable

A single external clock input is required. All read, write, refresh and read-modify-write operations take place when chip enable input is high. When the chip enable is low, the memory is in the low power standby mode. No read/write operations can take place because the chip is automatically precharging.

$\overline{CS}$ Chip Select

The chip select terminal affects the data in, data out and read/write inputs. The data input and data output terminals are enabled when chip select is low. The chip select input must be low on or before the rising edge of the chip enable and can be driven from standard TTL circuits. A register for the chip select input is provided on the chip to reduce overhead and simplify system design.

$\overline{WE}$ Write Enable

The read or write mode is selected through the write enable input. A logic high on the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The $\overline{WE}$ terminal can be driven from standard TTL circuits. The data input is disabled when the read mode is selected.

A_0–A_{11} Addresses

All addresses must be stable on or before the rising edge of the chip enable pulse. All address inputs can be driven from standard TTL circuits. Address registers are provided on the chip to reduce overhead and simplify system design.

D_{IN} Data Input

Data is written during a write or read-modify-write cycle while the chip enable is high. The data in terminal can be driven from standard TTL circuits. There is no register on the data in terminal.

$\overline{D_{OUT}}$ Data Output

The three state output buffer provides direct TTL compatibility with a fan-out of two TTL gates. The output is in the high-impedance (floating) state when the chip enable is low or when the Chip Select input is high. Data output is inverted from data in.

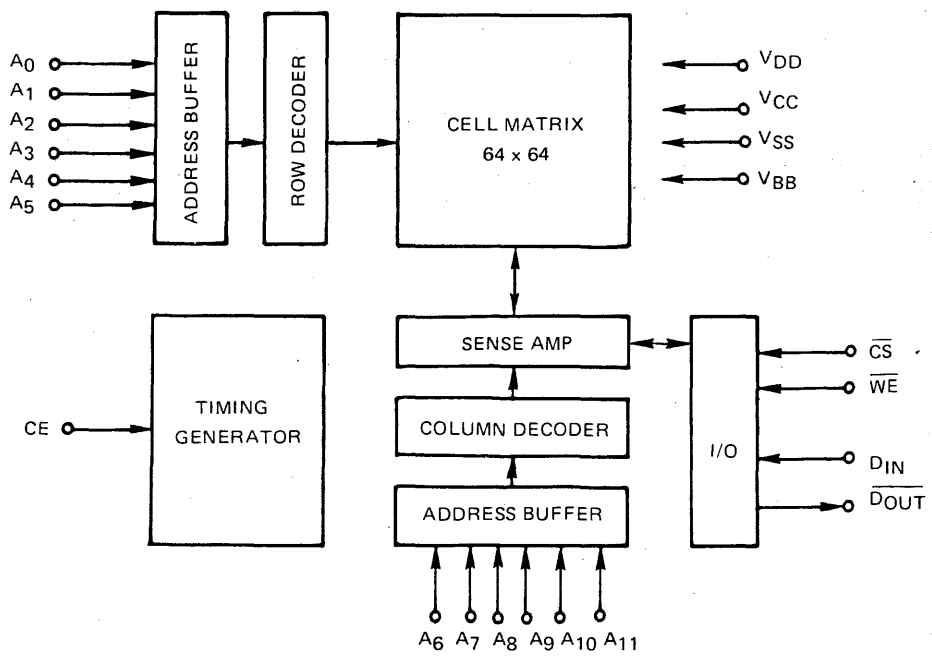
Refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs A_0 through A_5 or by addressing every row within any 2*-millisecond period. Addressing any row refreshes all 64 bits in that row.

The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, the chip select must be high.

*μPD411A-E = 1 millisecond refresh period.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
Output Voltage ①	+20 to −0.3 Volts
All Input Voltages ①	+20 to −0.3 Volts
Supply Voltage V_{DD} ①	+20 to −0.3 Volts
Supply Voltage V_{CC} ①	+20 to −0.3 Volts
Supply Voltage V_{SS} ①	+20 to −0.3 Volts
Power Dissipation	1.0W

Note: ① Relative to V_{BB}.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

*T_a = 25°C

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP. ①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Load Current	I_{LI}		0.01	10	μA	V_{IN} = V_{IL} MIN to V_{IH} MAX
CE Input Load Current	I_{LC}		0.01	10	μA	V_{IN} = V_{ILC} MIN to V_{IHC} MAX
Output Leakage Current for High Impedance State	I_{LO}		0.01	±10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
V_{DD} Supply Current during CE off	I_{DD} OFF		50	200	μA	CE = −1.0V to 0.6V
V_{DD} Supply Current during CE on	I_{DD} ON		35	50	mA	CE = V_{IHC}, T_a = 25°C
Average V_{DD} Current						T_a = 25°C
μPD411A-E	I_{DD} AV		25	40	mA	Cycle Time = 800 ns
μPD411A	I_{DD} AV		38	55	mA	Cycle Time = 470 ns
μPD411A-1	I_{DD} AV		38	55	mA	Cycle Time = 430 ns
μPD411A-2	I_{DD} AV		38	55	mA	Cycle Time = 400 ns
V_{BB} Supply Current ②	I_{BB}		5	100	μA	
V_{CC} Supply Current during CE off ③	I_{CC} OFF		0.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
Input Low Voltage	V_{IL}	−1.0		0.6	V	
Input High Voltage	V_{IH}	2.4		V_{CC} + 1	V	
CE Input Low Voltage	V_{ILC}	−1.0		0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD} − 1	V_{DD}	V_{DD} + 1	V	
Output Low Voltage	V_{OL}	0		0.40	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −2.0 mA

Notes: ① Typical values are for T_a = 25°C and nominal power supply voltages.
② The I_{BB} current is the sum of all leakage currents.
③ During CE on V_{CC} supply current is dependent on output loading.

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Address Capacitance	C_{AD}			6	pF	V_{IN} = V_{SS}
$\overline{CS}$ Capacitance	C_{CS}			6	pF	V_{IN} = V_{SS}
D_{IN} Capacitance	C_{IN}			6	pF	V_{IN} = V_{SS}
$\overline{D_{OUT}}$ Capacitance	C_{OUT}			7	pF	V_{OUT} = V_{SS}
$\overline{WE}$ Capacitance	C_{WE}			7	pF	V_{IN} = V_{SS}
CE Capacitance	C_{CE1}			27	pF	V_{IN} = V_{SS}
	C_{CE2}			22	pF	V_{IN} = V_{DD}

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AC CHARACTERISTICS

READ CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD411A-E MIN	μPD411A-E MAX	μPD411A MIN	μPD411A MAX	μPD411A-1 MIN	μPD411A-1 MAX	μPD411A-2 MIN	μPD411A-2 MAX	UNIT	TEST CONDITIONS
Time Between Refresh	t_{REF}		1		2		2		2	ms	$t_T = t_r = t_f$ = 20 ns C_L = 50 pF Load = 1TTL Gate V_{ref} = 2.0 or 0.8 Volts
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		150		ns	
CE Off Time	t_{CC}	380		130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	ns	
Cycle Time	t_{CY}	800		470		430		400		ns	
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	ns	
CE Output Delay	t_{CO}		330		280		230		180	ns	
Access Time	t_{ACC}		350		300		250		200	ns	
CE to $\overline{WE}$	t_{WL}	40		40		40		40		ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		ns	

WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD411A-E MIN	μPD411A-E MAX	μPD411A MIN	μPD411A MAX	μPD411A-1 MIN	μPD411A-1 MAX	μPD411A-2 MIN	μPD411A-2 MAX	UNIT	TEST CONDITIONS
Cycle Time	t_{CY}	800		470		430		400		ns	$t_T = t_r = t_f$ = 20 ns C_L = 50 pF Load = 1TTL Gate V_{ref} = 2.0 or 0.8 Volts
Time Between Refresh	t_{REF}		1		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		150		ns	
CE Off Time	t_{CC}	380		130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	ns	
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	ns	
$\overline{WE}$ to CE off	t_W	200		180		180		150		ns	
CE to $\overline{WE}$	t_{CW}	380		300		260		230		ns	
D_{IN} to $\overline{WE}$ Set Up ①	t_{DW}	0		0		0		0		ns	
D_{IN} Hold Time	t_{DH}	40		40		40		40		ns	
$\overline{WE}$ Pulse Width	t_{WP}	200		180		180		150		ns	

Note: ① If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.

READ-MODIFY-WRITE CYCLE

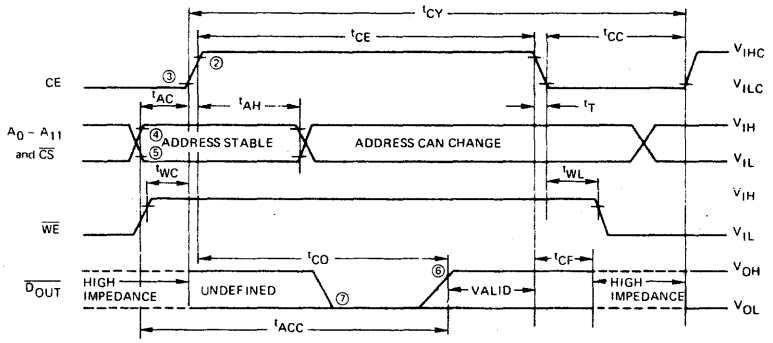
T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD411A-E MIN	μPD411A-E MAX	μPD411A MIN	μPD411A MAX	μPD411A-1 MIN	μPD411A-1 MAX	μPD411A-2 MIN	μPD411A-2 MAX	UNIT	TEST CONDITIONS
Read-Modify-Write (RMW) Cycle Time	t_{RWC}	960		650		600		520		ns	$t_T = t_r = t_f$ = 20 ns C_L = 50 pF Load = 1TTL Gate V_{ref} = 2.0 or 0.8 Volts
Time Between Refresh	t_{REF}		1		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		150		ns	
CE Off Time	t_{CC}	380		130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	ns	
CE Width During RMW	t_{CRW}	540	3000	480	3000	430	3000	350	3000	ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		ns	
$\overline{WE}$ to CE off	t_W	200		180		180		150		ns	
$\overline{WE}$ Pulse Width	t_{WP}	200		180		180		150		ns	
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		0		ns	
D_{IN} Hold Time	t_{DH}	40		40		40		40		ns	
CE to Output Delay	t_{CO}		330		280		230		180	ns	
Access Time	t_{ACC}		350		300		250		200	ns	

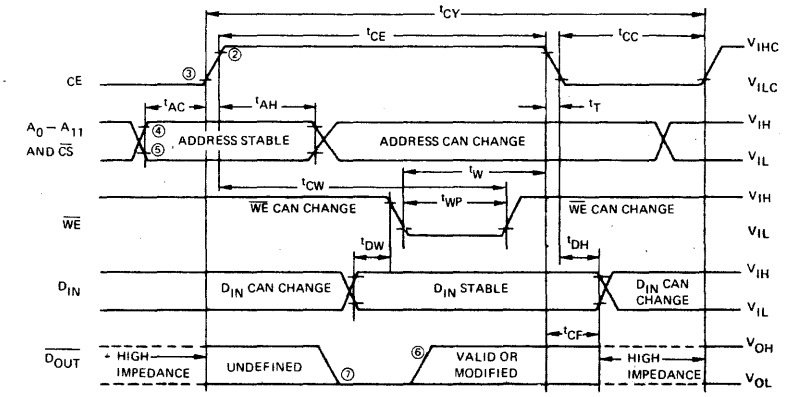
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TIMING WAVEFORMS

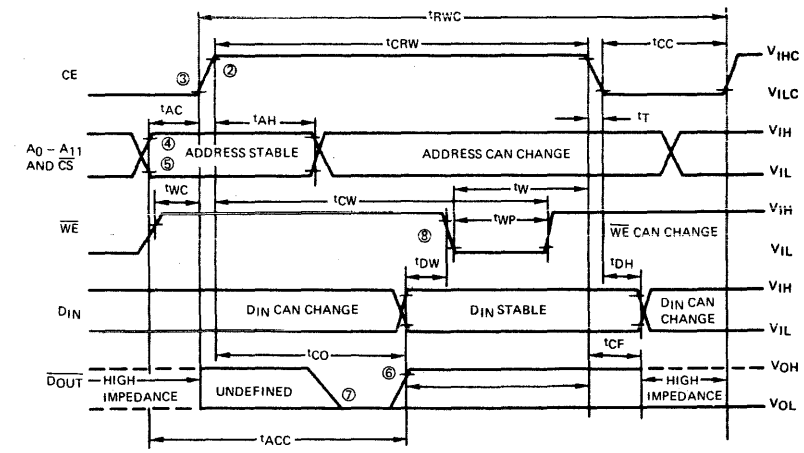
READ AND REFRESH CYCLE ①



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



Notes:

① For refresh cycle, row and column addresses must be stable t_{AC} and remain stable for entire t_{AH} period.

② V_{DD} – 2V is the reference level for measuring timing of CE.

③ V_{SS} + 2V is the reference level for measuring timing of CE.

④ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

⑤ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

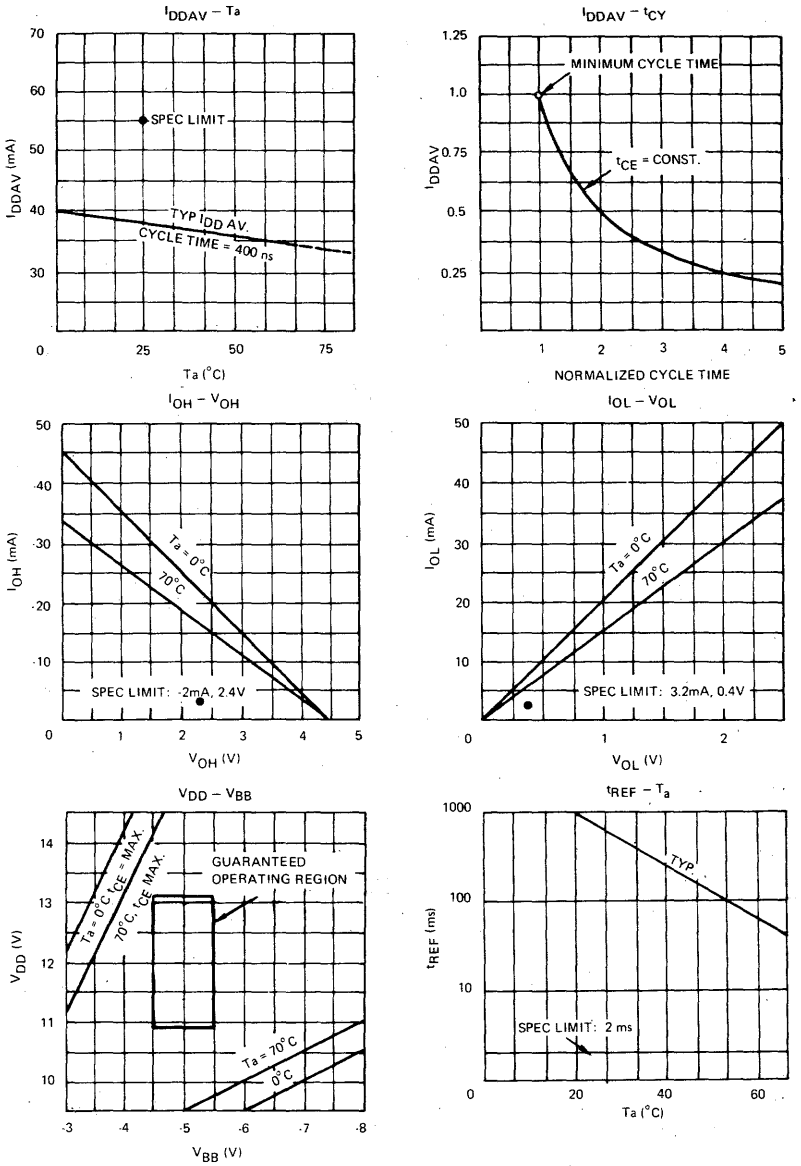
⑥ V_{SS} + 2.0V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑦ V_{SS} + 0.8V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑧ $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

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TYPICAL OPERATING CHARACTERISTICS



POWER CONSUMPTION

Power consumption = $V_{DD} \times I_{DDAV} + V_{BB} \times I_{BB}$

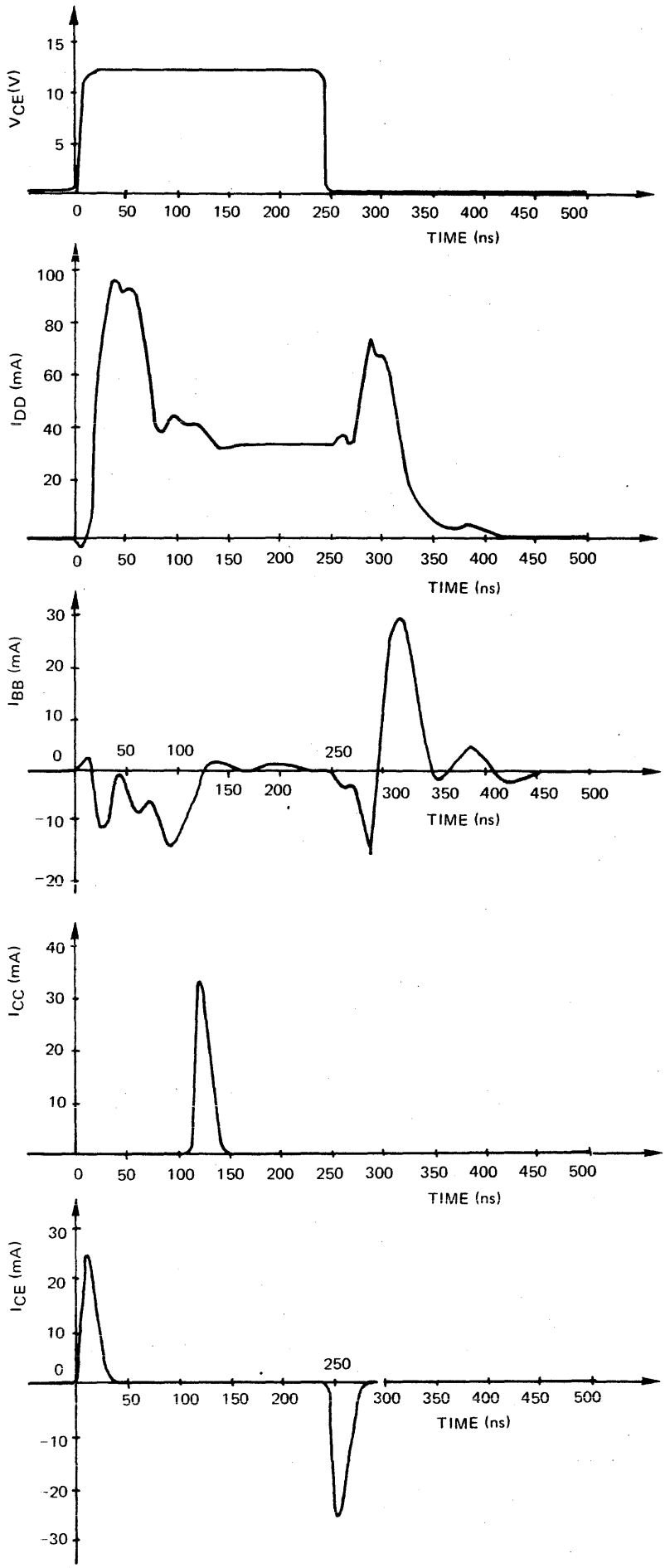
Typical power dissipation for each product is shown below.

	mW (TYP.)	CONDITIONS
μPD411A-E	300 mW	$T_a = 25°C$, $t_{cy} = 800$ ns, $t_{CE} = 380$ ns
μPD411A	460 mW	$T_a = 25°C$, $t_{cy} = 470$ ns, $t_{CE} = 300$ ns
μPD411A-1	460 mW	$T_a = 25°C$, $t_{cy} = 430$ ns, $t_{CE} = 260$ ns
μPD411A-2	460 mW	$T_a = 25°C$, $t_{cy} = 400$ ns, $t_{CE} = 230$ ns

See curve above for power dissipation versus cycle time.

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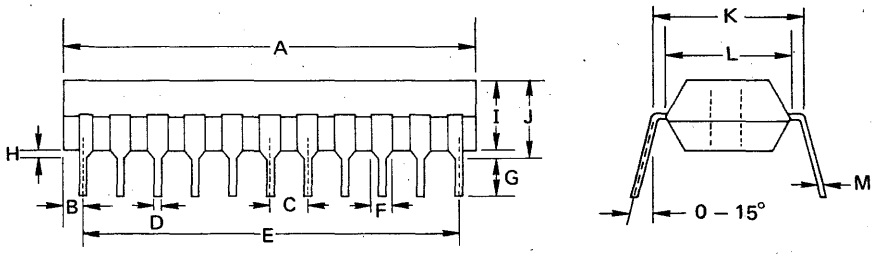
CURRENT WAVEFORMS ①



Note: ① V_{DD} = 12V, V_{BB} = −5.0V, V_{CC} = 5.0V

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PACKAGE OUTLINE
μPD411AC



μPD411AC (Plastic)

ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50	0.02
E	25.4	1.00
F	1.40	0.055
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

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4096 BIT DYNAMIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The μPD411-M Family consists of three 4096 words by 1 bit dynamic N-channel MOS RAMs. They are designed for memory applications where wide operating environmental temperatures are important design considerations. The μPD411-M Family is designed using dynamic circuitry which reduces the standby power dissipation.

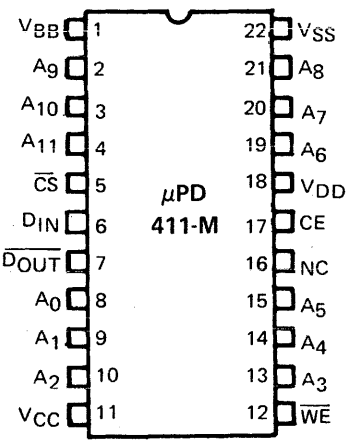
Reading information from the memory is non-destructive. Refreshing is easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic high or a logic low.*

FEATURES

- 4096 Words x 1 Bit Organization.
- Wide Operating Temperature Range (T_a = −40 to +85°C).
- TTL Compatibility on All Inputs (except CE).
- Three-State Output Providing TTL Compatibility.
- 22 Pin Dual-In-Line Ceramic Package.
- 3 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE	REFRESH TIME	POWER DISSIPATION
μPD411-M	300 ns	470 ns	650 ns	2 ms	65 mA
μPD411-1M	250 ns	430 ns	600 ns	2 ms	65 mA
μPD411-2M	200 ns	400 ns	520 ns	2 ms	65 mA

PIN CONFIGURATION

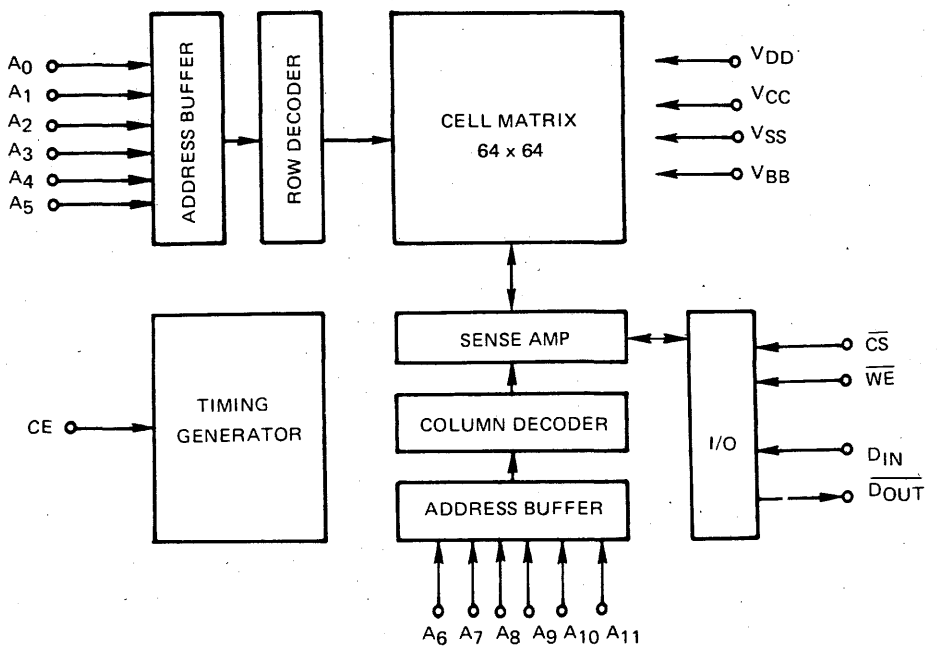


PIN NAMES

$A_0 - A_{11}$	Address Inputs
$A_0 - A_5$	Refresh Addresses
CE	Chip Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
$\overline{D_{OUT}}$	Data Output
$\overline{WE}$	Write Enable
V_{DD}	Power (+12V)
V_{CC}	Power (+5V)
V_{SS}	Ground
V_{BB}	Power (-5V)
NC	No Connection

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−40°C to +85°C ①
Storage Temperature	−55°C to +150°C
All Output Voltages	−0.3 to +20 Volts ②
All Input Voltages	−0.3 to +20 Volts ②
Supply Voltage V_{DD}	−0.3 to +20 Volts ②
Supply Voltage V_{CC}	−0.3 to +20 Volts ②
Supply Voltage V_{SS}	−0.3 to +20 Volts ②
CE Input Voltage	−0.3 to +20 Volts
Power Dissipation	1.0W

Notes: ① Still Air
② Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C.

CAPACITANCE

V_{CC} = +5V ± 5%, V_{DD} = +12V ± 5%, V_{SS} = 0V, V_{BB} = −5V ± 5%, T_a = −40 to +85°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address Capacitance	C_{AD}			7	pF	V_{IN} = V_{SS}
$\overline{CS}$ Capacitance	C_{CS}			6	pF	V_{IN} = V_{SS}
D_{IN} Capacitance	C_{IN}			6	pF	V_{IN} = V_{SS}
$\overline{D_{OUT}}$ Capacitance	C_{OUT}			7	pF	V_{OUT} = V_{SS}
$\overline{WE}$ Capacitance	C_{WE}			7	pF	V_{IN} = V_{SS}
CE Capacitance	C_{CE1}			27	pF	V_{IN} = V_{SS}
	C_{CE2}			22	pF	V_{IN} = V_{DD}

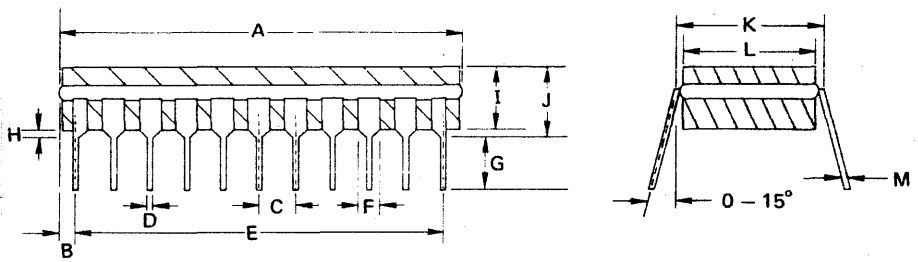
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DC CHARACTERISTICS

T_a = −40°C to +85°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP ①	MAX		
Input Load Current	I_{LI}			10	μA	V_{IN} = V_{IL} MIN to V_{IH} MAX
CE Input Load Current	I_{LC}			10	μA	V_{IN} = V_{ILC} MIN to V_{IHC} MAX
Output Leakage Current for High Impedance State	I_{LO}			10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
V_{DD} Supply Current during CE off	I_{DD} OFF			200	μA	CE = −1.0V to 0.6V
V_{DD} Supply Current during CE on	I_{DD} ON			65	mA	CE = V_{IHC}, T_a = 25°C
Average V_{DD} Current μPD411-M μPD411-1M μPD411-2M	 I_{DD} AV I_{DD} AV I_{DD} AV			 65 65 65	 mA mA mA	T_a = 25°C Cycle Time = 470 ns Cycle Time = 430 ns Cycle Time = 400 ns
V_{BB} Supply Current ②	I_{BB}		5	100	μA	
V_{CC} Supply Current during CE off ③	I_{CC} OFF			10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
Input Low Voltage	V_{IL}	−1.0		0.6	V	
Input High Voltage	V_{IH}	2.6		V_{CC} + 1	V	
CE Input Low Voltage	V_{ILC}	−1.0		0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD} − 1	V_{DD}	V_{DD} + 1	V	
Output Low Voltage	V_{OL}	0		0.40	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −2.0 mA
Time Between Refresh	t_{REF}			2	ms	

Notes: ① Typical values are for T_a = 25°C and nominal power supply voltages.
② The I_{BB} current is the sum of all leakage currents.
③ During CE on V_{CC} supply current is dependent on output loading.



PACKAGE OUTLINE
μPD411-MD

ITEM	MILLIMETERS	INCHES
A	27.43 Max.	1.079 Max.
B	1.27 Max.	0.05 Max.
C	2.54 ± 0.1	0.10
D	0.42 ± 0.1	0.016
E	25.4 ± 0.3	1.0
F	1.5 ± 0.2	0.059
G	3.5 ± 0.3	0.138
H	3.7 ± 0.3	0.145
I	4.2 Max.	0.165 Max.
J	5.08 Max.	0.200 Max.
K	10.16 ± 0.15	0.400
L	9.1 ± 0.2	0.358
M	0.25 ± 0.05	0.009

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AC CHARACTERISTICS

READ CYCLE

T_a = –40°C to +85°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = –5V ± 5%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		μPD411-M		μPD411-1M		μPD411-2M			
		MIN	MAX	MIN	MAX	MIN	MAX		
Time Between Refresh	t_{REF}		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		ns	
CE Off Time	t_{CC}	130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	ns	$t_T = t_r = t_f$ = 20 ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	ns	C_L = 50 pF
Cycle Time	t_{CY}	470		430		400		ns	Load = 1_{TTL} Gate
CE on Time	t_{CE}	300	3000	260	3000	230	3000	ns	V_{ref} = 2.0 or 0.8 Volts
CE Output Delay	t_{CO}		280		230		180	ns	
Access Time	t_{ACC}		300		250		200	ns	
CE to $\overline{WE}$	t_{WL}	40		40		40		ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		ns	
$\overline{CS}$ Hold Time	t_{CSH}	150		150		150		ns	
$\overline{CS}$ Set Up Time	t_{CSC}	0		0		0		ns	

WRITE CYCLE

T_a = –40°C to +85°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = –5V ± 5%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		μPD411-M		μPD411-1M		μPD411-2M			
		MIN	MAX	MIN	MAX	MIN	MAX		
Cycle Time	t_{CY}	470		430		400		ns	
Time Between Refresh	t_{REF}		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		ns	
CE Off Time	t_{CC}	130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	ns	$t_T = t_r = t_f$ = 20 ns
CE on Time	t_{CE}	300	3000	260	3000	230	3000	ns	C_L = 50 pF
$\overline{WE}$ to CE off	t_W	180		180		150		ns	Load = 1_{TTL} Gate
CE to $\overline{WE}$	t_{CW}	300		260		230		ns	V_{ref} = 2.0 or 0.8 Volts
D_{IN} to $\overline{WE}$ Set Up ①	t_{DW}	0		0		0		ns	
D_{IN} Hold Time	t_{DH}	40		40		40		ns	
$\overline{WE}$ Pulse Width	t_{WP}	180		180		150		ns	
$\overline{CS}$ Set Up Time	t_{CSC}	0		0		0		ns	
$\overline{CS}$ Hold Time	t_{CSH}	150		150		150		ns	

Note: ① If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.

READ-MODIFY-WRITE CYCLE

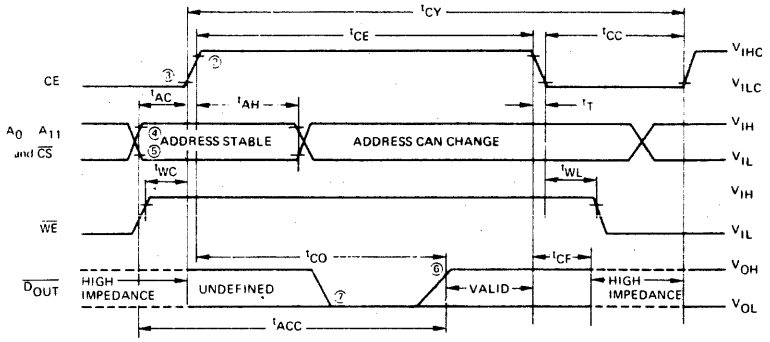
T_a = –40°C to +85°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = –5V ± 5%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		μPD411-M		μPD411-1M		μPD411-2M			
		MIN	MAX	MIN	MAX	MIN	MAX		
Read-Modify-Write (RMW) Cycle Time	t_{RWC}	650		600		520		ns	
Time Between Refresh	t_{REF}		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		ns	
CE Off Time	t_{CC}	130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	ns	
CE Width During RMW	t_{CRW}	480	3000	430	3000	350	3000	ns	$t_T = t_r = t_f$ = 20 ns
$\overline{WE}$ to CE on	t_{WC}	0		0		0		ns	C_L = 50 pF
$\overline{WE}$ to CE off	t_W	180		180		150		ns	Load = 1_{TTL} Gate
$\overline{WE}$ Pulse Width	t_{WP}	180		180		150		ns	V_{ref} = 2.0 or 0.8 Volts
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		ns	
D_{IN} Hold Time	t_{DH}	40		40		40		ns	
CE to Output Delay	t_{CO}		280		230		180	ns	
Access Time	t_{ACC}		300		250		200	ns	
CE on Time	t_{CE}	480	3000	430	3000	350	3000	ns	
$\overline{CS}$ Set Up Time	t_{CSC}	0		0		0		ns	
$\overline{CS}$ Hold Time	t_{CSH}	150		150		150		ns	
CE to $\overline{WE}$	t_{CW}	480		430		350		ns	

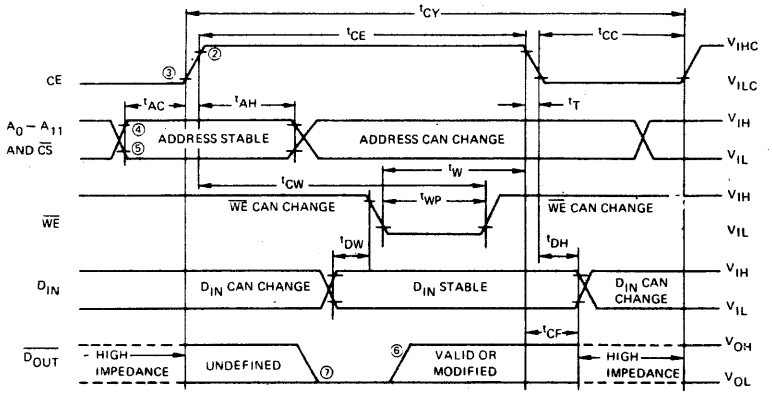
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TIMING WAVEFORMS

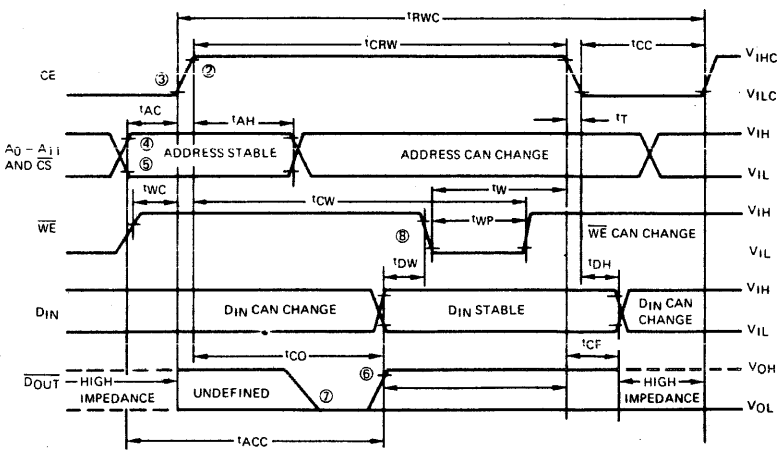
READ AND REFRESH CYCLE ①



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



Notes:

① For refresh cycle, row and column addresses must be stable t_{AC} and remain stable for entire t_{AH} period.

② V_{DD} – 2V is the reference level for measuring timing of CE.

③ V_{SS} + 2V is the reference level for measuring timing of CE.

④ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

⑤ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

⑥ V_{SS} + 2.0V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑦ V_{SS} + 0.8V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑧ $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

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FULLY DECODED RANDOM ACCESS 4096 BIT DYNAMIC MEMORY

DESCRIPTION

The NEC μPD414 is a 4096 words by 1 bit Dynamic N channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. The μPD414 uses a single transistor dynamic storage cell and dynamic circuitry to achieve high speed and low power dissipation.

The μPD414 is packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is available in either cerdip or plastic.

The use of the 16 pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the μPD414 on 6 address input pins. The two 6 bit address words are latched into the μPD414 by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Noncritical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

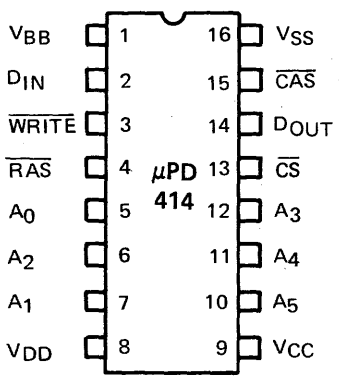
The single transistor dynamic storage cell provides high speed along with low power dissipation. The memory cell requires refreshing for data retention. Refreshing is most easily accomplished by performing a read cycle at each of the 64 row addresses every 2 milliseconds.

FEATURES

- 4096 Words x 1 Bit Organization
- Refresh Period 2 ms
- Standard 16 Pin Cerdip and Plastic Packages
- Low Standby Power
- All Inputs Including Clocks TTL Compatible
- Standard Power Supplies +12V, +5V, -5V
- Gated $\overline{CAS}$ Characteristic
- On-Chip Latches for Addresses, Chip Select and Data In
- Simple Memory Expansion Chip Select
- Output is Three State, TTL Compatible; Data is Latched and Valid into Next Cycle
- 4 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE
μPD414-E	350 ns	500 ns	700 ns
μPD414	300 ns	425 ns	590 ns
μPD414-1	250 ns	375 ns	480 ns
μPD414-2	200 ns	375 ns	420 ns

PIN CONFIGURATION

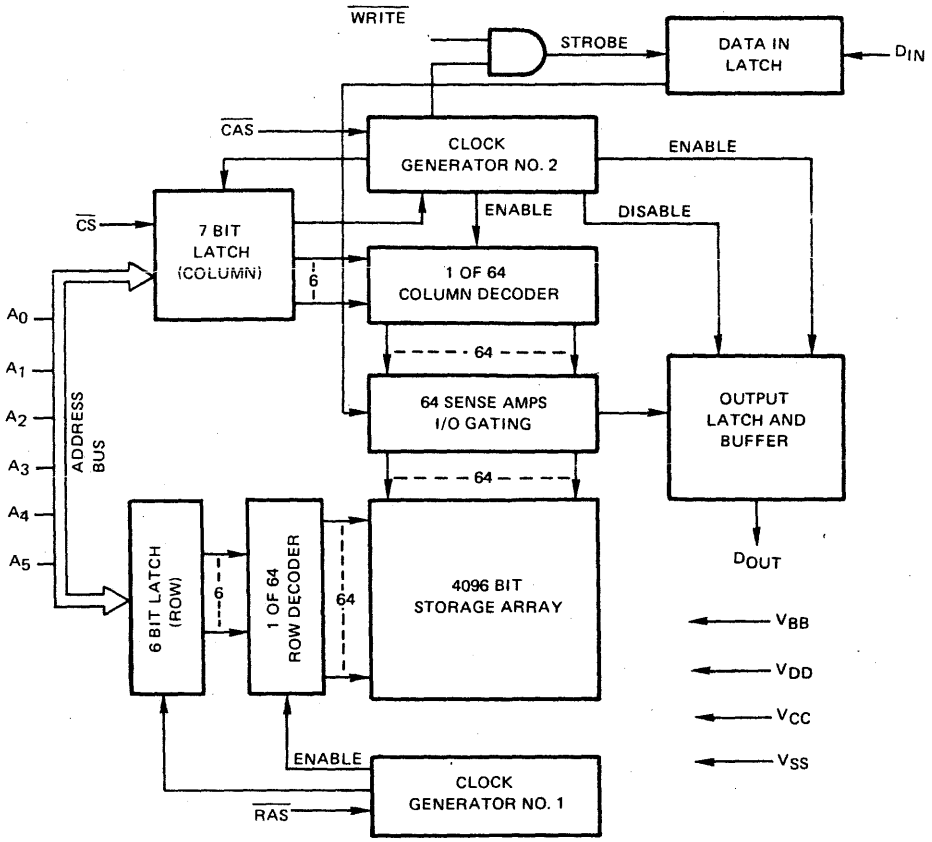


PIN NAMES

A_0-A_5	Address Inputs
$\overline{CAS}$	Column Address Strobe
$\overline{CS}$	Chip Select
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write
V_{BB}	Power (-5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
V_{SS}	Ground

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
All Output Voltages ①	−0.5 to +25 Volts
All Input Voltages ①	−0.5 to +25 Volts
Supply Voltages V_{DD}, V_{CC}, V_{SS} ①	−0.5 to +25 Volts
Power Dissipation	1.0W

Note: ① Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V, unless otherwise noted. ①②

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Address Capacitance	C_{AD}			10	pF	V_{IN} = V_{SS}
$\overline{CAS}$, $\overline{RAS}$, $\overline{CS}$ Capacitance	C_C			7	pF	V_{IN} = V_{SS}
Data Output Capacitance	C_{OUT}			8	pF	V_{OUT} = 0V
D_{IN} and $\overline{WRITE}$ Capacitance	C_{IN}			7	pF	V_{IN} = V_{SS}

Notes: ① All voltages referenced to V_{SS}. The only requirement for the sequence of applying voltages to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.5V or more negative than V_{BB}.

② Capacitance measured with Boonton Meter.

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DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, ① V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP ②	MAX		
Input Load Current (any input)	I_{LI}			10	μA	⑤
Output Leakage Current for High Impedance State	I_{LO}			10	μA	Chip deselected ⑥⑦
V_{DD} Supply Current	$I_{DD}OFF$ ③			2.0	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}. Chip deselected. ⑥
Average V_{DD} Current	$I_{DD}AV$ ③			35	mA	Cycle time = Min ④ t_{RP} = 150 ns, T_a = 25°C
V_{CC} Supply Current when deselected	$I_{CC}OFF$			10	μA	⑧
Average V_{BB} Current	I_{BB} ③			75	μA	
Average V_{DD} Power Supply Current During "$\overline{RAS}$ only" cycles	I_{DD3}			28	mA	④
Input Low Voltage (any input)	V_{IL}	−1.0		0.8	V	①⑨
Input High Voltage except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.4		7.0	V	①⑨
Output Low Voltage	V_{OL}	0		0.4	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4		7.0	V	I_{OH} = −5.0 mA
Supply Voltage	V_{DD}	10.8	12.0	13.2	V	①
Supply Voltage	V_{CC}	V_{SS}	5.0	V_{DD}	V	① ⑩
Supply Voltage	V_{SS}	0	0	0	V	①
Supply Voltage	V_{BB}	−4.5	−5.0	−5.5	V	①
Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7		7.0	V	⑨

Notes:
① All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
② Typical values are for T_a = 25°C and nominal power supply voltages.
③ The I_{DD} current flows to V_{SS}. The I_{BB} current is the sum of all leakage currents.
④ Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
⑤ All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.
⑥ Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
⑦ $0V \leqslant V_{OUT} \leqslant +10V$.
⑧ When chip is selected V_{CC} supply current is dependent on output loading; V_{CC} is connected to output buffer only.
⑨ Device speed is not guaranteed at input voltages greater than TTL levels (0 to +5V).
⑩ Output voltage will swing from V_{SS} to V_{CC} if $V_{CC} \leqslant V_{DD}$ −4 volts. If $V_{CC} \geqslant V_{DD}$ −4 volts, the output will swing from V_{SS} to a voltage somewhat less than V_{DD}.

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AC CHARACTERISTICS

T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V, unless otherwise noted.

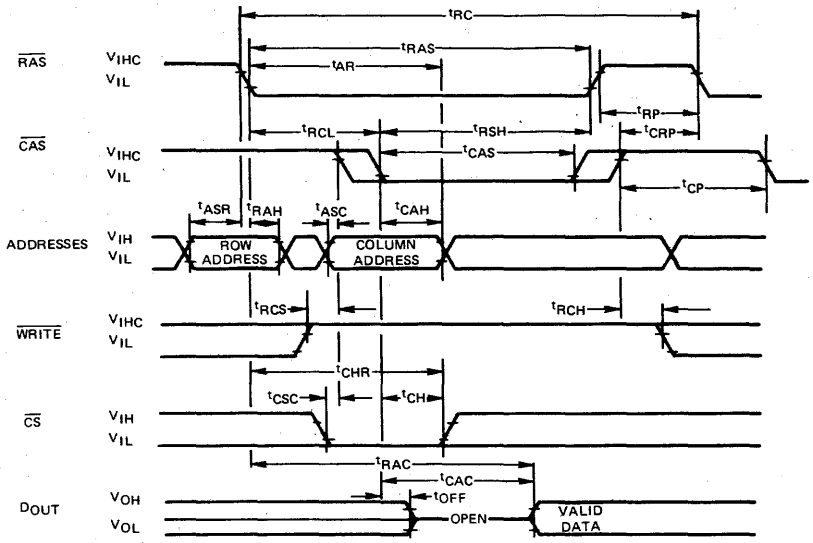
PARAMETER	SYMBOL	LIMITS												SYMBOL	TEST CONDITIONS
		414-E			414			414-1			414-2				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
Random read or write cycle time	t_{RC}	500			425			375			375			ns	②
Read write cycle time	t_{RWC}	700			590			480			420			ns	
Access time from row address strobe	t_{RAC}			350			300			250			200	ns	③ ⑤
Access time from column address strobe	t_{CAC}			200			165			140			135	ns	④ ⑤
Output buffer turn-off delay	t_{OFF}			100			80			60			50	ns	⑥
Row address strobe precharge time	t_{RP}	150			125			120			120			ns	
Row address strobe pulse width	t_{RAS}	350		32,000	300		32,000	250		32,000	200		32,000	ns	
Row address strobe hold time	t_{RSH}	200			165			140			135			ns	
Column address strobe pulse width	t_{CAS}	200		3,000	165		3,000	140		3,000	135		3,000	ns	
Row to column strobe lead time	t_{RCL}	110		150	90		135	35		110	25		65	ns	⑦
Row address set-up time	t_{ASR}	0			0			0			0			ns	
Row address hold time	t_{RAH}	100			80			35			25			ns	
Column address set-up time	t_{ASC}	0			0			0			0			ns	
Column address hold time	t_{CAH}	100			80			60			40			ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	210			170			160			120			ns	
Chip select set-up time	t_{CSC}	0			0			0			0			ns	
Chip select hold time	t_{CH}	100			80			60			40			ns	
Chip select hold time referenced to $\overline{RAS}$	t_{CHR}	210			170			160			120			ns	
Transition time (rise and fall)	t_T	5		50	5		50	3		50	3		50	ns	⑧
Read command set-up time	t_{RCS}	0			0			0			0			ns	
Read command hold time	t_{RCH}	0			0			0			0			ns	
Write command hold time	t_{WCH}	150			130			75			55			ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	260			220			160			120			ns	
Write command pulse width	t_{WP}	200			165			75			55			ns	
Write command to row strobe lead time	t_{RWL}	200			165			140			135			ns	
Write command to column strobe lead time	t_{CWL}	200			165			140			135			ns	
Data in set-up time	t_{DS}	0			0			0			0			ns	⑨
Data in hold time	t_{DH}	150			130			110			110			ns	⑨
Data in hold time referenced to $\overline{RAS}$	t_{DHR}	260			220			195			175			ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	0			0			0			0			ns	
Column precharge time	t_{CP}	150			125			120			120			ns	
Refresh period	t_{RFSH}			2			2			2			2	ms	
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	200			165			90			80			ns	⑩
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	350			300			175			145			ns	⑩

Notes:
① A.C. measurements assume t_T = 5 ns.
② Minimum cylce time (t_{RC}) is greater than $t_{RAS} + t_{RP} + 2t_T$ in order to limit power dissipation.
③ Assumes that $t_{RCL} + t_T \leq t_{RCL}$ (max).
④ Assumes that $t_{RCL} + t_T \geq t_{RCL}$ (max).
⑤ Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
⑥ Assumes that $t_{RCL} + t_T \geq t_{RCL}$ (max). If $t_{RCL} + t_T < t_{RCL}$ (max), $60 + t_{RCL}$ (max) − $t_{RCL} - t_T$ ns min.
⑦ Operation within the t_{RCL} (max) limit insures that t_{RAC} (max) can be met. t_{RCL} (max) is specified as a reference point only; if t_{RCL} is greater than the specified t_{RCL} (max) limit, then access time is controlled exclusively by t_{CAC}.
⑧ V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
⑨ These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
⑩ t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only:
If $t_{CWD} + t_T \leq t_{CWD}$ (min), the data out latch will contain high level data.
If $t_{CWD} \geq t_{CWD}$ (max) + t_T and $t_{RWD} \geq t_{RWD}$ (max) + t_T, the data out latch will contain the data read from the selected cell.
If t_{CWD} does not meet the above constraints, then data out latch will contain indeterminate data.

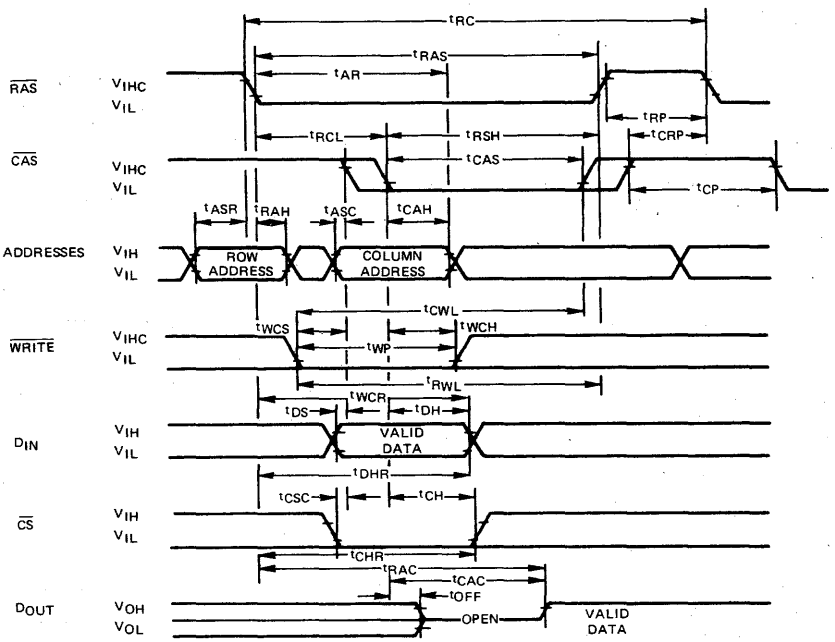
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TIMING WAVEFORMS

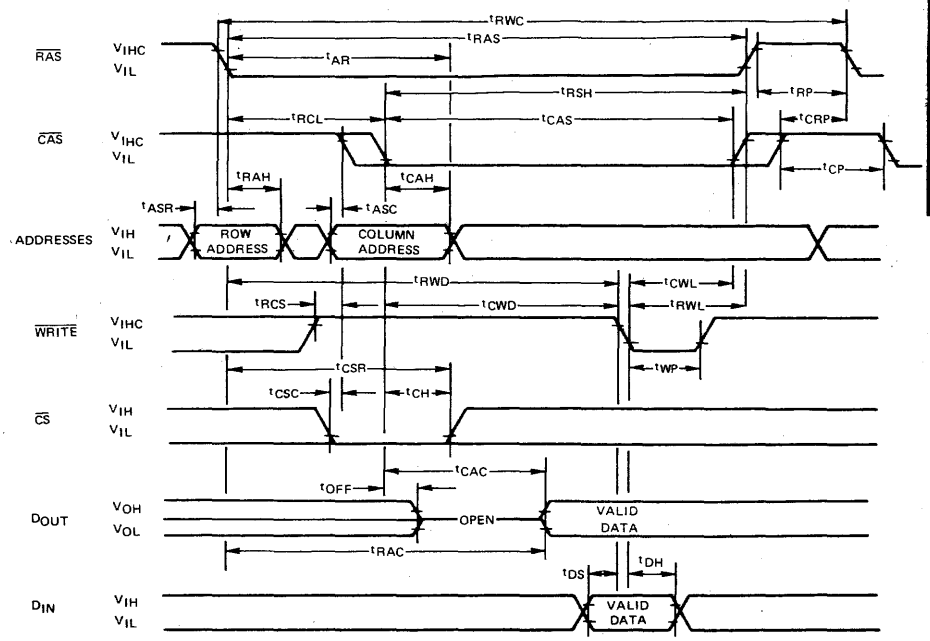
READ CYCLE



WRITE CYCLE



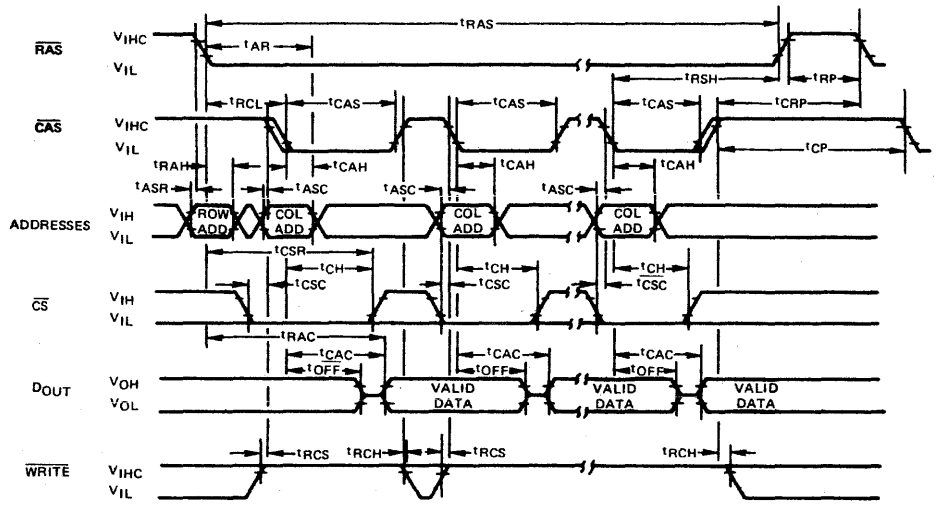
READ-MODIFY-WRITE CYCLE



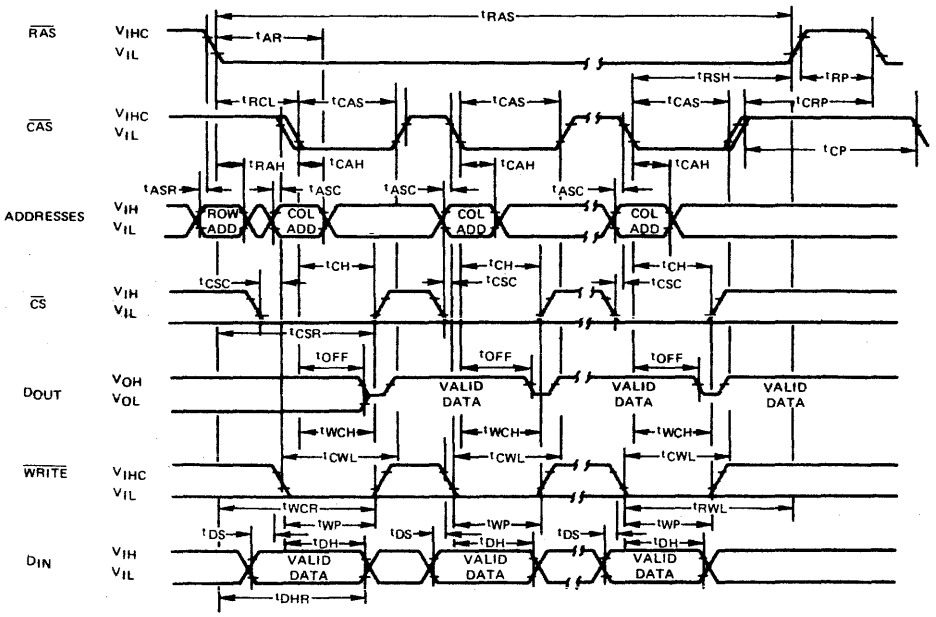
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TIMING WAVEFORMS (CONT.)

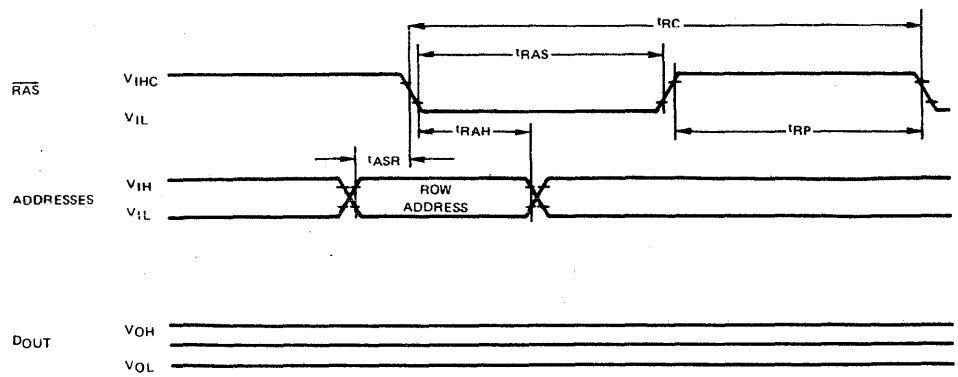
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



"RAS ONLY" REFRESH CYCLE



Note: D_{OUT} remains unchanged from previous cycle.

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ADDRESSING

The 12 address bits required to decode 1 of 4096 bit locations are multiplexed onto the 6 address pins and then latched on the chip with the use of the Row Address Strobe ($\overline{RAS}$), and the Column Address Strobe ($\overline{CAS}$). The 6 bit row address is first applied and $\overline{RAS}$ is then brought low. After the $\overline{RAS}$ hold time has elapsed, the column address and chip select signals are applied and $\overline{CAS}$ is brought low. Since the column address and chip select are not needed internally until a time of t_{RCL} MAX after the row address, this multiplexing operation imposes no penalty on access time as long as $\overline{CAS}$ is applied no later than t_{RCL} MAX. If this time is exceeded, access time will be defined from $\overline{CAS}$ instead of $\overline{RAS}$.

DATA I/O

For a write operation, the input data is latched on the chip by the negative going edge of $\overline{WRITE}$ or $\overline{CAS}$, whichever occurs later. If $\overline{WRITE}$ is active before $\overline{CAS}$, Data out will unconditionally assume a logic "1" state. If $\overline{WRITE}$ is mode active after the access time, as in a read/write cycle, the output will reflect the data read. The output data is latched and will remain in its proper state until the next negative transition of $\overline{CAS}$.

PAGE MODE

The μPD414 may also be operated in page mode for either reading or writing by keeping $\overline{RAS}$ low after strobing in the row address, and cycling $\overline{CAS}$ for each new column address.

REFRESH

Refresh of the memory matrix is accomplished by performing a memory cycle at each of the 64 row addresses every 2 milliseconds or less. Any memory cycle will refresh the chip regardless of the state of chip select although the chip must be deselected if a write cycle is used to avoid altering data. The data output will go to the high impedance state if chip select is high when $\overline{CAS}$ is brought low.

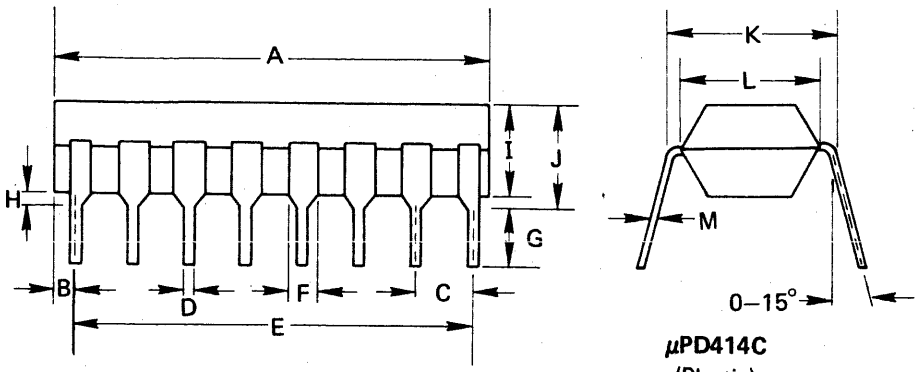
Refresh may also be achieved by cycling $\overline{RAS}$ only and strobing in each of the 64 row addresses. The data output will remain unaffected by this "$\overline{RAS}$-only" refresh.

$\overline{CAS}$ ONLY OPERATION

If $\overline{RAS}$ is decoded and applied only to the desired chips, the remaining chips will dissipate no power on the $\overline{CAS}$ edges. In addition, the outputs will assume the high impedance state regardless of chip select.

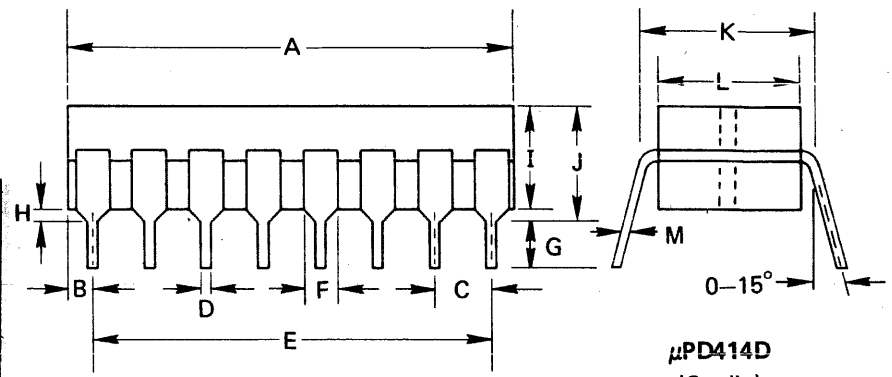
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PACKAGE OUTLINE
μPD414C/D



μPD414C
(Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01



μPD414D
(Cerdip)

ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	$0.0098^{+0.0039}_{-0.0019}$

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μPD416
μPD416-1
μPD416-2
μPD416-3

16384 x 1 BIT DYNAMIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The NEC μPD416 is a 16384 words by 1 bit Dynamic MOS RAM. It is designed for memory applications where very low cost and large bit storage are important design objectives.

The μPD416 is fabricated using a double-poly-layer N channel silicon gate process which affords high storage cell density and high performance. The use of dynamic circuitry throughout, including the sense amplifiers, assures minimal power dissipation.

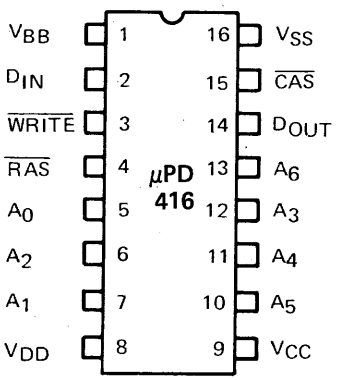
Multiplexed address inputs permit the μPD416 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is available in either ceramic or plastic. Noncritical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FEATURES

- 16384 Words x 1 Bit Organization
- High Memory Density – 16 Pin Ceramic and Plastic Packages
- Multiplexed Address Inputs
- Standard Power Supplies +12V, -5V, +5V
- Low Power Dissipation; 462 mW Active (MAX), 20 mW Standby (MAX)
- Output Data Controlled by $\overline{CAS}$ and Unlatched at End of Cycle
- Read-Modify-Write, $\overline{RAS}$-only Refresh, and Page Mode Capability
- All Inputs TTL Compatible, and Low Capacitance
- 128 Refresh Cycles
- 4 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE
μPD416	300 ns	510 ns	510 ns
μPD416-1	250 ns	430 ns	430 ns
μPD416-2	200 ns	375 ns	375 ns
μPD416-3	150 ns	375 ns	375 ns

PIN CONFIGURATION

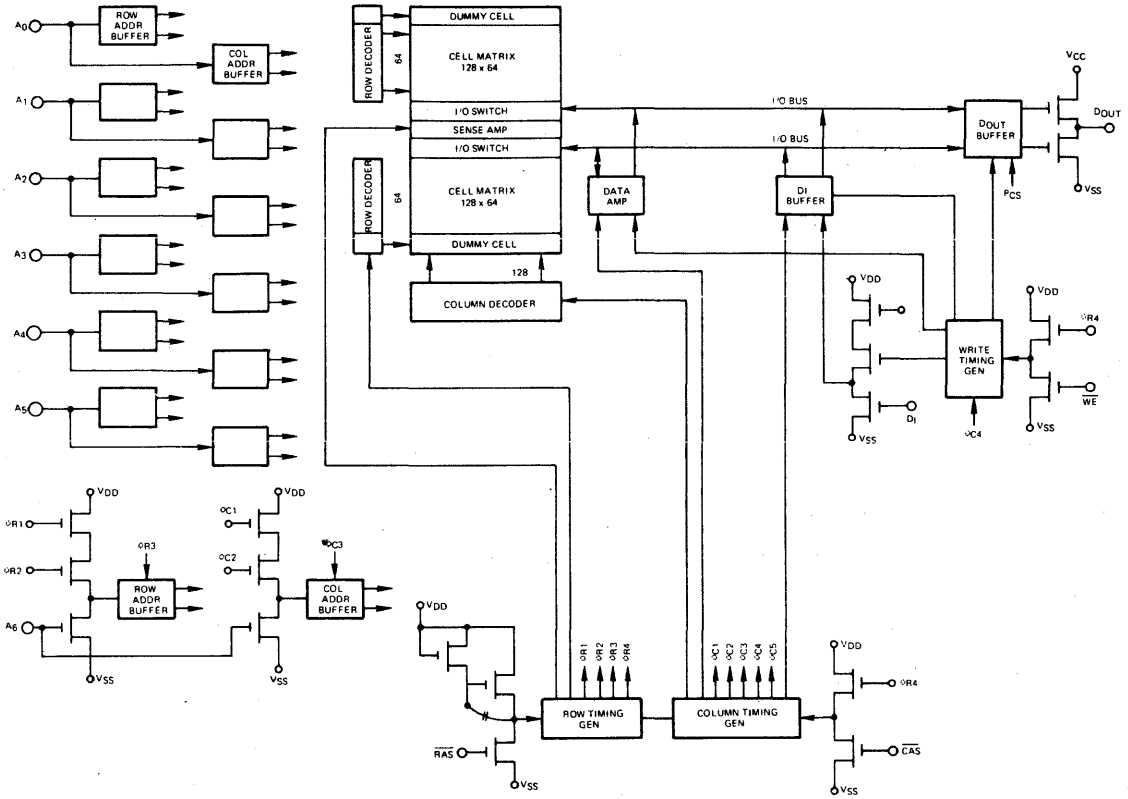


PIN NAMES

A_0-A_6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write
V_{BB}	Power (-5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
V_{SS}	Ground

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
All Output Voltages ①	−0.5 to +20 Volts
All Input Voltages ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC}, V_{SS} ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC} ②	−1.0 to +15 Volts
Short Circuit Output Current	50 mA
Power Dissipation	1 Watt

Notes: ① Relative to V_{BB}
② Relative to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V ± 10%, V_{CC} = +5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance (A_0-A_6), D_{IN}	C_{I1}		4	5	pF	
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}		8	10	pF	
Output Capacitance (D_{OUT})	C_O		5	7	pF	

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DC CHARACTERISTICS

T_a = 0°C to +70°C ①, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Supply Voltage	V_{DD}	10.8	12.0	13.2	V	②
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	② ③
Supply Voltage	V_{SS}	0	0	0	V	②
Supply Voltage	V_{BB}	−4.5	−5.0	−5.5	V	②
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7		7.0	V	②
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.4		7.0	V	②
Input Low (Logic 0) Voltage, all inputs	V_{IL}	−1.0		0.8	V	②
Operating V_{DD} Current	I_{DD1}			35	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ Min. ④
Standby V_{DD} Current	I_{DD2}			1.5	mA	$\overline{RAS} = V_{IHC}$, D_{OUT} = High Impedance
Refresh V_{DD} Current	I_{DD3}			25	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IHC}$; t_{RC} = 375 ns ④
Page Mode V_{DD} Current	I_{DD4}			27	mA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{PC} = 225 ns ④
Operating V_{CC} Current	I_{CC1}				μA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 375 ns ⑤
Standby V_{CC} Current	I_{CC2}	−10		10	μA	$\overline{RAS} = V_{IHC}$, D_{OUT} = High Impedance
Refresh V_{CC} Current	I_{CC3}	−10		10	μA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IHC}$, t_{RC} = 375 ns
Page Mode V_{CC} Current	I_{CC4}				μA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{PC} = 225 ns ⑤
Operating V_{BB} Current	I_{BB1}			200	μA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 375 ns
Standby V_{BB} Current	I_{BB2}			100	μA	$\overline{RAS} = V_{IHC}$, D_{OUT} = High Impedance
Refresh V_{BB} Current	I_{BB3}			200	μA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IHC}$; t_{RC} = 375 ns
Page Mode V_{BB} Current	I_{BB4}			200	μA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{PC} = 225 ns
Input Leakage (any input)	$I_{I(L)}$	−10		10	μA	V_{BB} = −5V, 0V ≤ V_{IN} ≤ +7V, all other pins not under test = 0V
Output Leakage	$I_{O(L)}$	−10		10	μA	D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V
Output High Voltage (Logic 1)	V_{OH}	2.4			V	I_{OUT} = -5 mA ③
Output Low Voltage (Logic 0)	V_{OL}			0.4	V	I_{OUT} = 4.2 mA

Notes: ① T_a is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met. See Figure 1 for derating curve.

② All voltages referenced to V_{SS}.

③ Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

④ I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See Figures 2, 3 and 4 for I_{DD} limits at other cycle rates.

⑤ I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

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DERATING CURVES

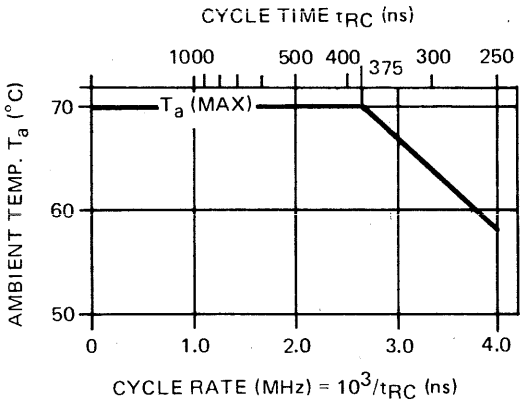


FIGURE 1

Maximum ambient temperature versus cycle rate for extended frequency operation. T_a (max) for operation at cycling rates greater than 2.66 MHz ($t_{CYC} < 375$ ns) is determined by T_a (max) [°C] = 70 - 9.0 x (cycle rate [MHz] -2.66).

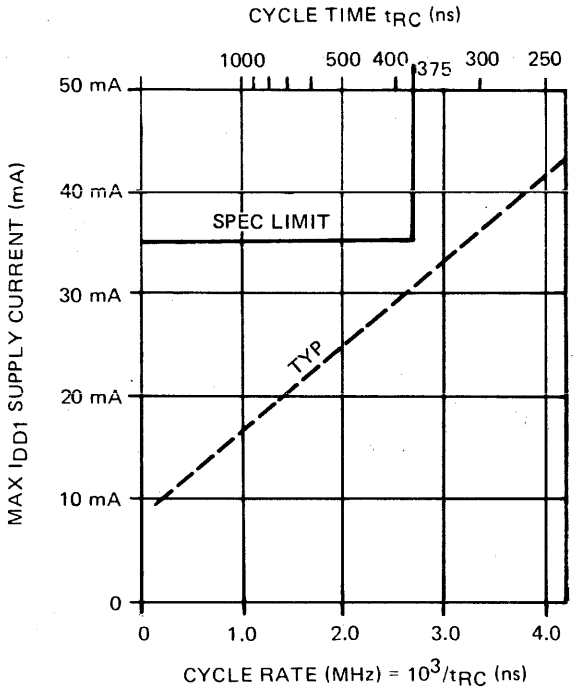


FIGURE 2

Maximum I_{DD1} versus cycle rate for device operation at extended frequencies.

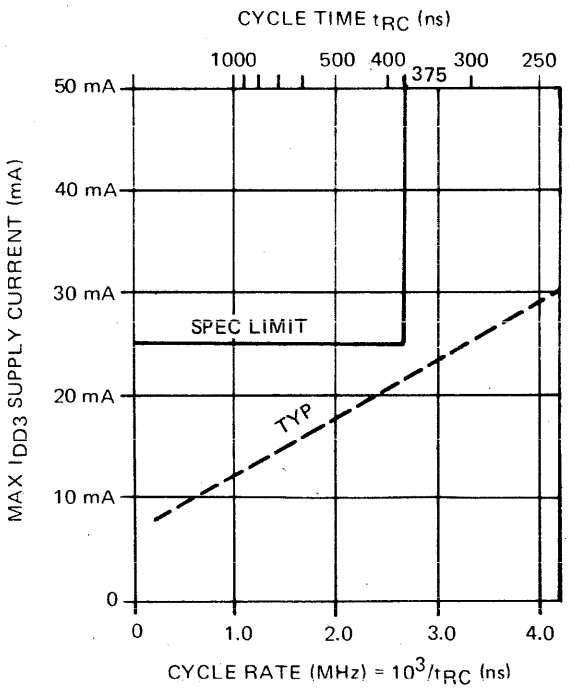


FIGURE 3

Maximum I_{DD3} versus cycle rate for device operation at extended frequencies.

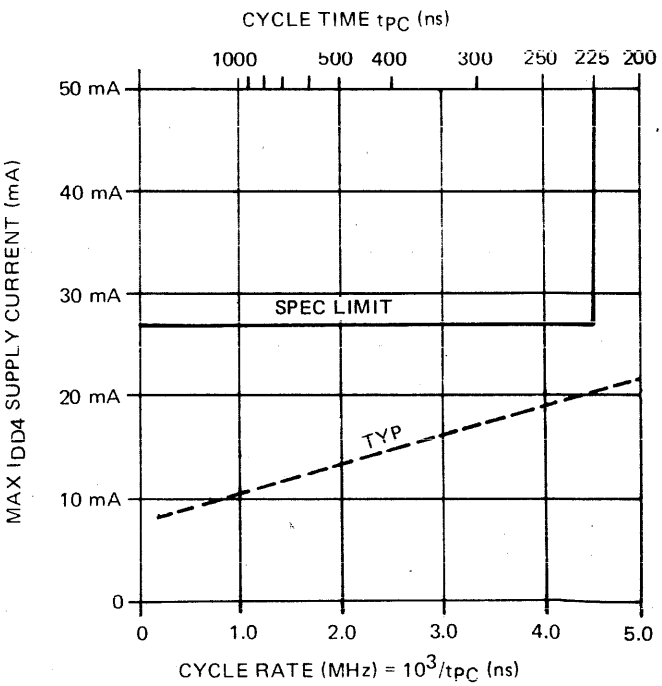


FIGURE 4

Maximum I_{DD4} versus cycle rate for device operation in page mode.

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AC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS								UNIT	TEST CONDITIONS
		μPD416		μPD416-1		μPD416-2		μPD416-3			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	510		430		375		375		ns	③
Read-write cycle time	t_{RWC}	510		430		375		375		ns	③
Page mode cycle time	t_{PC}	330		280		225		170		ns	
Access time from $\overline{RAS}$	t_{RAC}		300		250		200		150	ns	④ ⑥
Access time from $\overline{CAS}$	t_{CAC}		200		170		135		100	ns	⑤ ⑥
Output buffer turn-off delay	t_{OFF}	0	80	0	70	0	50	0	40	ns	⑦
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	35	ns	②
$\overline{RAS}$ precharge time	t_{RP}	200		170		120		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	300	32,000	250	32,000	200	32,000	150	32,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	200		170		135		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	200	10,000	170	10,000	135	10,000	100	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	40	100	35	85	25	65	20	50	ns	⑧
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	−20		−20		−20		−20		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row Address hold time	t_{RAH}	40		35		25		20		ns	
Column address set-up time	t_{ASC}	−10		−10		−10		−10		ns	
Column address hold time	t_{CAH}	90		75		55		45		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	190		160		120		95		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		0		ns	
Write command hold time	t_{WCH}	90		75		55		45		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	190		160		120		95		ns	
Write command pulse width	t_{WP}	90		75		55		45		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	120		100		80		60		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	120		100		80		60		ns	
Data-in set-up time	t_{DS}	0		0		0		0		ns	⑨
Data-in hold time	t_{DH}	90		75		55		45		ns	⑨
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	190		160		120		95		ns	
$\overline{CAS}$ precharge time (for page mode cycle only)	t_{CP}	120		100		80		60		ns	
Refresh period	t_{REF}		2		2		2		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	−10		−10		−10		−10		ns	
CAS to $\overline{WRITE}$ delay	t_{CWD}	140		120		95		70		ns	
RAS to $\overline{WRITE}$ delay	t_{RWD}	210		175		160		120		ns	

Notes:

① AC measurements assume t_T = 5 ns.

② V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

③ The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_a ≤ 70°C) is assured.

④ Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.

⑤ Assumes that $t_{RCD} \geq t_{RCD}$ (max).

⑥ Measured with a load equivalent to 2 TTL loads and 100 pF.

⑦ t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

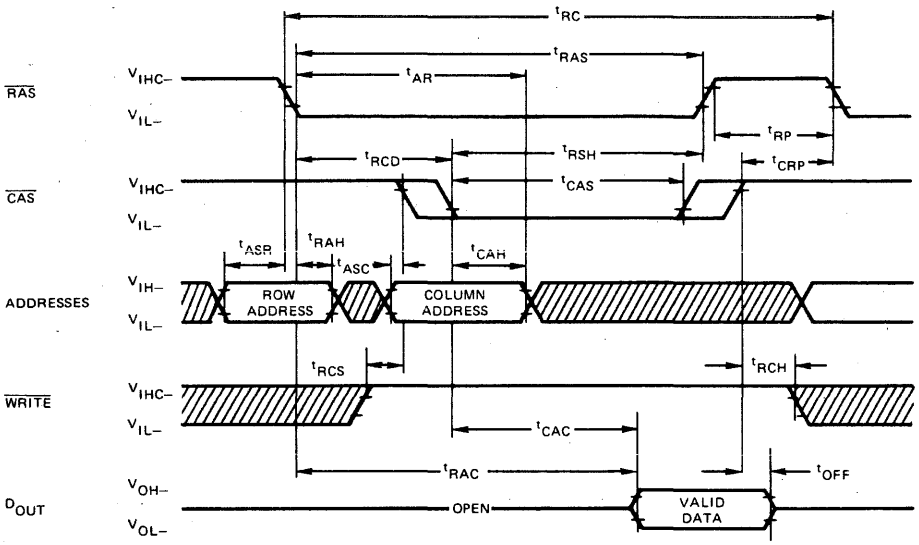
⑧ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

⑨ These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

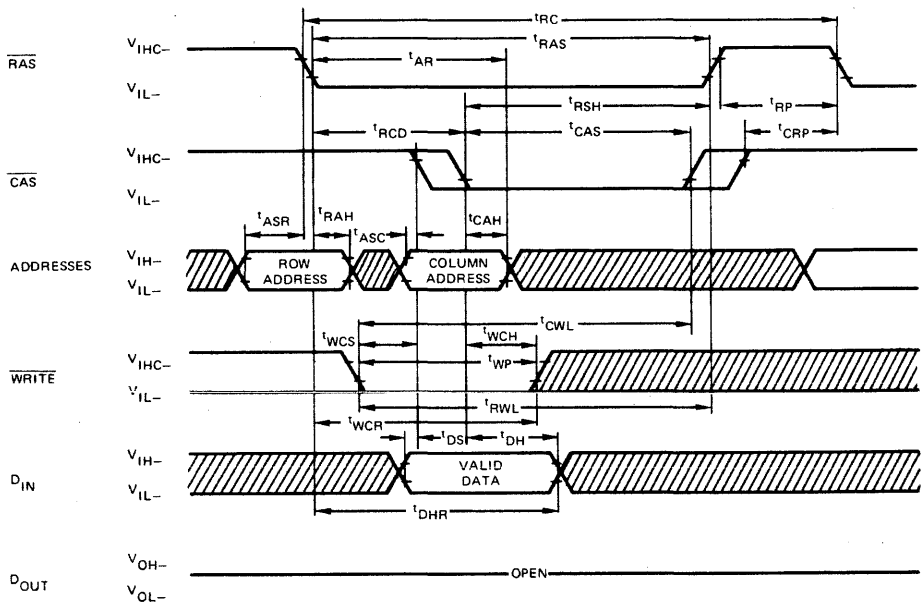
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TIMING WAVEFORMS

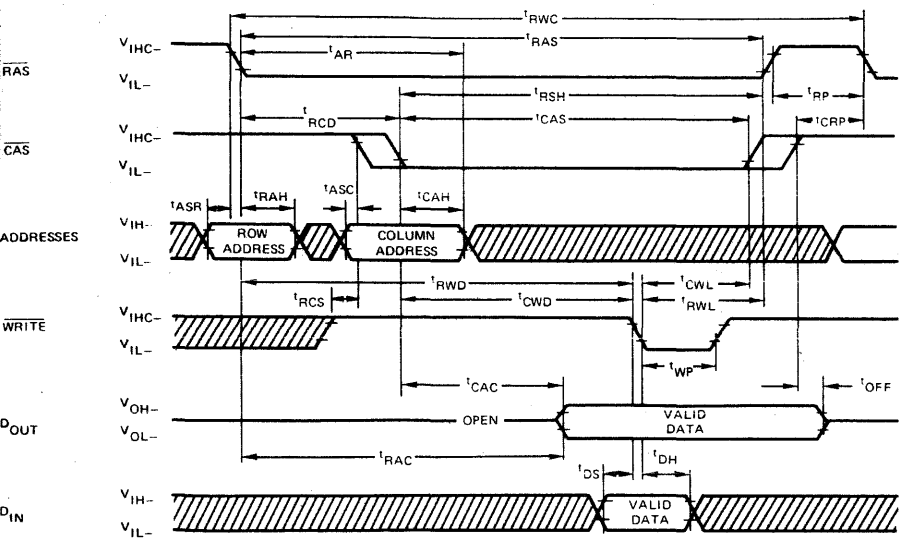
READ CYCLE



WRITE CYCLE



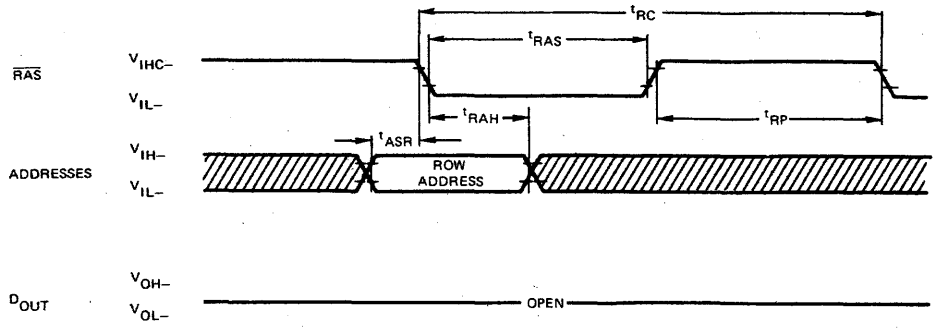
READ-WRITE/READ-MODIFY–WRITE CYCLE



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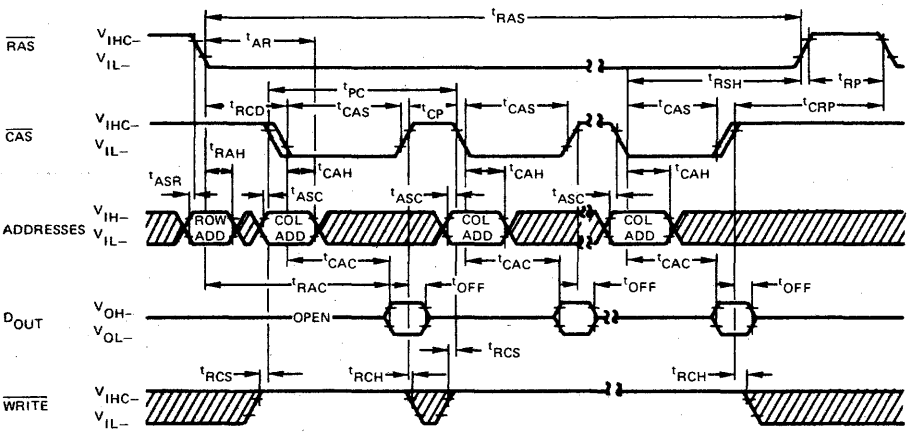
TIMING WAVEFORMS (CONT.)

"$\overline{RAS}$-ONLY" REFRESH CYCLE

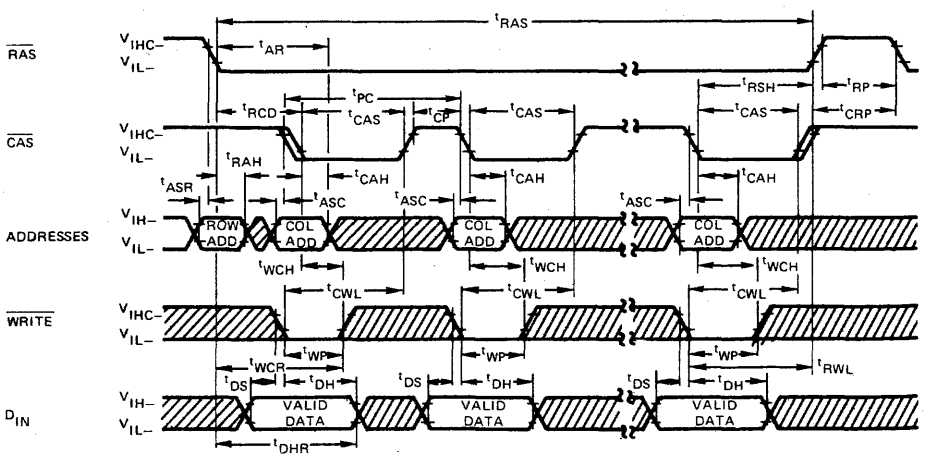


Note: $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't Care

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



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ADDRESSING

The 14 address bits required to decode 1 of 16,384 bit locations are multiplexed onto the 7 address pins and then latched on the chip with the use of the Row Address Strobe ($\overline{RAS}$), and the Column Address Strobe ($\overline{CAS}$). The 7 bit row address is first applied and $\overline{RAS}$ is then brought low. After the $\overline{RAS}$ hold time has elapsed, the 7 bit column address is applied and $\overline{CAS}$ is brought low. Since the column address is not needed internally until a time of t_{CRD} MAX after the row address, this multiplexing operation imposes no penalty on access time as long as $\overline{CAS}$ is applied no later than t_{CRD} MAX. If this time is exceeded, access time will be defined from $\overline{CAS}$ instead of $\overline{RAS}$.

DATA I/O

For a write operation, the input data is latched on the chip by the negative going edge of $\overline{WRITE}$ or $\overline{CAS}$, whichever occurs later. If $\overline{WRITE}$ is active before $\overline{CAS}$, this is an "early WRITE" cycle and data out will remain in the high impedance state throughout the cycle. For a READ, WRITE, OR READ-MODIFY-WRITE cycle, the data output will contain the data in the selected cell after the access time. Data out will assume the high impedance state anytime that $\overline{CAS}$ goes high.

PAGE MODE

The page mode feature allows the μPD416 to be read or written at multiple column addresses for the same row address. This is accomplished by maintaining a low on $\overline{RAS}$ and strobing the new column addresses with $\overline{CAS}$. This eliminates the setup and hold times for the row address resulting in faster operation.

REFRESH

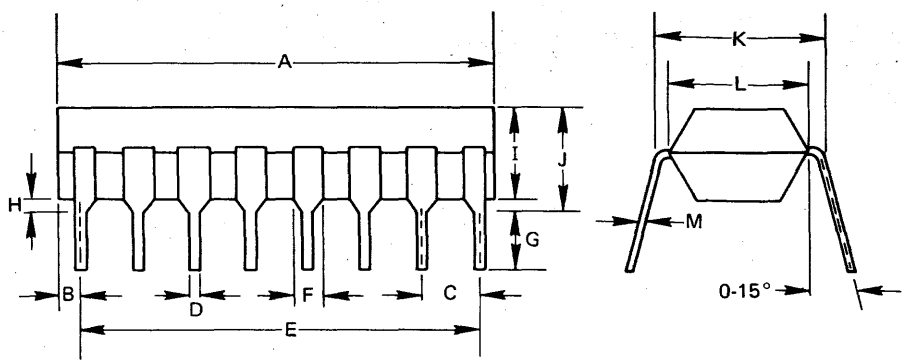
Refresh of the memory matrix is accomplished by performing a memory cycle at each of the 128 row addresses every 2 milliseconds or less. Because data out is not latched, "$\overline{RAS}$ only" cycles can be used for simple refreshing operation.

CHIP SELECTION

Either $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded for chip select function. Unselected chip outputs will remain in the high impedance state.

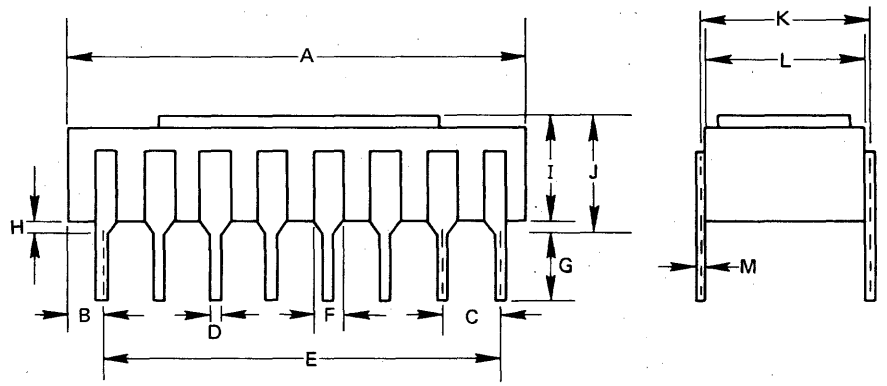
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PACKAGE OUTLINE
μPD416C/D



μPD416C
(Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01



μPD416D
(Ceramic)

ITEM	MILLIMETERS	INCHES
A	20.5 MAX.	0.81 MAX.
B	1.36	0.05
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	3.5 MIN.	0.14 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.20 MAX.
K	7.6	0.30
L	7.3	0.29
M	0.27	0.01

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4096 BIT DYNAMIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The μPD418 series is composed of high speed, dynamic, 4096 words x 1 bit, N channel, MOS, random access memories.

All inputs, except the clock (chip enable), are fully TTL compatible and require no pull-up resistors. The low capacitance of the address and control inputs precludes the need for specialized drivers. The data input and output are multiplexed to facilitate compatibility with a common bus system.

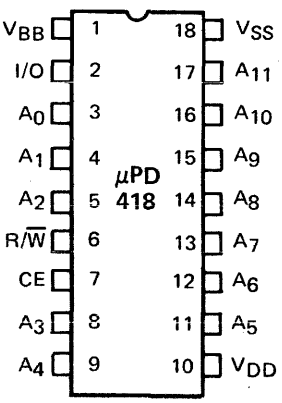
The μPD418 has only one clock (chip enable), to simplify system design. The low capacitance clock input requires a positive voltage (+12 volts) which can be driven by a variety of widely available drivers.

FEATURES

- 4096 words x 1 bit Organization
- High Memory Density – 18 Pin Cerdip and Plastic Package
- 10% Supply Margins
- Multiplexed Data Input/Output
- High Speed Access, Low Power Dissipation (370 mW Max)
- Full TTL Compatibility on All Inputs (except CE)
- Resistors for Address Inputs Provided on Chip
- Open Drain Output Buffer
- Single Low Capacitance Clock (CE)
- Power Supply +12V, –5V
- Replacement for TI's 4050 and Equivalent Devices
- 3 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE	POWER (TYP)
μPD418D	300 ns	470 ns	650 ns	200 mW
μPD418D-1	250 ns	430 ns	610 ns	200 mW
μPD418D-2	200 ns	400 ns	580 ns	200 mW

PIN CONFIGURATION

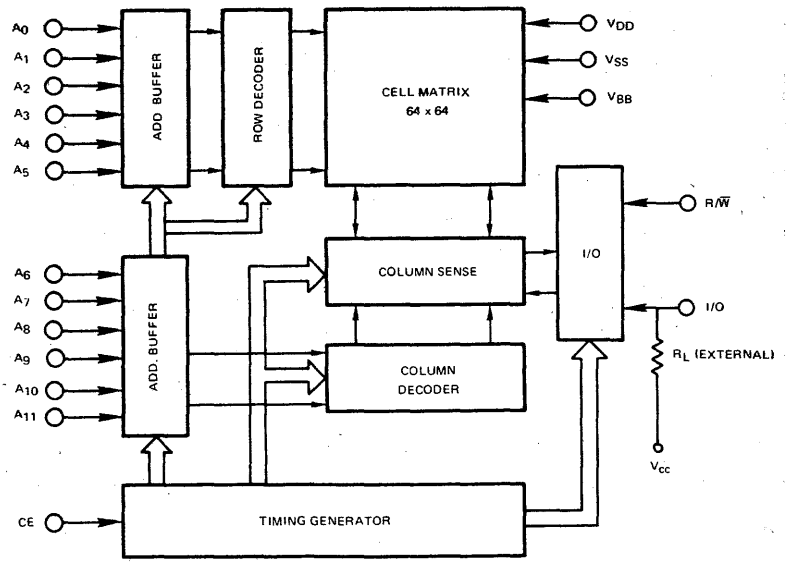


PIN NAMES

A_0-A_{11}	Address Input
A_0-A_5	Refresh Address
R/$\overline{W}$	Read/Write Control
I/O	Input/Output Terminal
CE	Chip Enable (Clock)
V_{DD}	Power Supply (+12V)
V_{BB}	Power Supply (–5V)
V_{SS}	Ground

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
All Output Voltages ①	−0.3 to +25 Volts
All Input Voltages ①	−0.3 to +25 Volts
Supply Voltage V_{DD} ①	−0.3 to +25 Volts
Supply Voltage V_{SS} ①	−0.3 to +25 Volts
Power Dissipation	1.0W

Note: ① Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V ± 10%,① V_{SS} = 0V unless otherwise noted.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ②	LIMITS MAX	UNIT	TEST CONDITIONS
Input Current (All Inputs Except CE)	I_I			10	μA	V_I = −0.3V to 5.5V
CE Input Current	I_I(CE)			10	μA	V_I = −0.3V to 13.6V
Supply Current From V_{DD} Standby	I_{DD}(OFF)			200	μA	V_I(CE) = 0.6V
Supply Current From V_{DD}	I_{DD}(ON)		6	15	mA	V_I(CE) = 13.6V
Average Supply Current From V_{DD} During Read or Write Cycle	I_{DD}(av)		16	28	mA	Minimum Cycle Timing μPD418
			16	28		Minimum Cycle Timing μPD418-1
			16	28		Minimum Cycle Timing μPD418-2
Average Supply Current From V_{DD} During Read-Modify-Write Cycle	I_{DD}(av)			28	mA	Minimum Cycle Timing μPD418
				28		Minimum Cycle Timing μPD418-1
				28		Minimum Cycle Timing μPD418-2
Supply Current From V_{BB}	I_{BB}			100	μA	V_{BB} = −5.5V, V_{DD} = 13.2V, V_{SS} = 0V
High Level Output Voltage	V_{OH}	2.4		V_{CC}	V	t_a = Guaranteed max access time, R_L = 2.2 kΩ to 5.5V, C_L = 50pF, Load = 1 TTL Gate
Low Level Output Voltage	V_{OL}	V_{SS}		0.4	V	
Low Level Output Current	I_{OL}	5			mA	t_a = Guaranteed max access time, C_L = 50pF, V_{OL} = 0.4V
High Level Input Voltage (Except CE)	V_{IH}	2.2		5.5	V	
High Level CE Voltage	V_{IH}(CE)	V_{DD} − 1		V_{DD} + 1	V	
Low Level Input Voltage (Except CE)	V_{IL}	−0.6		0.6	V	
Low Level CE Voltage	V_{IL}(CE)	−0.6		0.6	V	

Notes: ① All voltages referenced to V_{SS}.
② Typical values are for T_a = 25°C and nominal power supply voltages.

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AC CHARACTERISTICS

READ CYCLE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V + 10%, V_{SS} = 0V unless otherwise noted

PARAMETER	SYMBOL	LIMITS μPD418 MIN.	μPD418 MAX.	μPD418-1 MIN.	μPD418-1 MAX.	μPD418-2 MIN.	μPD418-2 MAX.	UNIT	TEST CONDITIONS
Refresh Time	t_{ref}		2		2		2	ms	
Read Cycle Time	t_c(rd)	470		430		400		ns	
Pulse Width, CE High	t_w(CEH)	300	4000	260	4000	230	4000	ns	
Pulse Width, CE Low	t_w(CEL)	130		130		130		ns	
CE Rise Time	t_r(CE)		40		40		40	ns	
CE Fall Time	t_f(CE)		40		40		40	ns	
Address Setup Time	t_{su}(ad)	0		0		0		ns	
Read Setup Time	t_{su}(rd)	0		0		0		ns	
Address Hold Time	t_h(ad)	150		150		150		ns	
Read Hold Time	t_h(rd)	40		40		40		ns	
Access Time From Address	t_a(ad)		300		250		200	ns	C_L = 50pF, R_L = 2.2 kΩ to 5.5V Load = 1 TTL Gate, t_r(CE) = 20 ns
Access Time From CE	t_a(CE)		280		230		180	ns	
Propagation Delay Time, Low to High Level Output From CE	t_{PLH}	40		40		40		ns	C_L = 50pF, R_L = 2.2 kΩ to 5.5V Load = 1 TTL Gate

WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD418 MIN.	μPD418 MAX.	μPD418-1 MIN.	μPD418-1 MAX.	μPD418-2 MIN.	μPD418-2 MAX.	UNIT	TEST CONDITIONS
Refresh Time	t_{ref}		2		2		2	ms	
Write Cycle Time	t_c(wr)	470		430		400		ns	
Pulse Width, CE High	t_w(CEH)	300	4000	260	4000	230	4000	ns	
Pulse Width, CE Low	t_w(CEL)	130		130		130		ns	
Write Pulse Width	t_w(wr)	180		180		180		ns	
CE Rise Time	t_r(CE)		40		40		40	ns	
CE Fall Time	t_f(CE)		40		40		40	ns	
Address Setup Time	t_{su}(ad)	0		0		0		ns	
Data Setup Time	t_{su}(da)	150		150		150		ns	
Write Pulse Setup Time	t_{su}(wr)	200		200		200		ns	
CE High to Write Delay Time ⑦ ⑧	t_d(CEH-wr)		40		40		40	ns	
Data Hold Time	t_h(da)	40		40		40		ns	
Address Hold Time	t_h(ad)	150		150		150		ns	
Write Hold Time ⑦ ⑧	t_h(wr)		40		40		40	ns	

READ-MODIFY-WRITE CYCLE

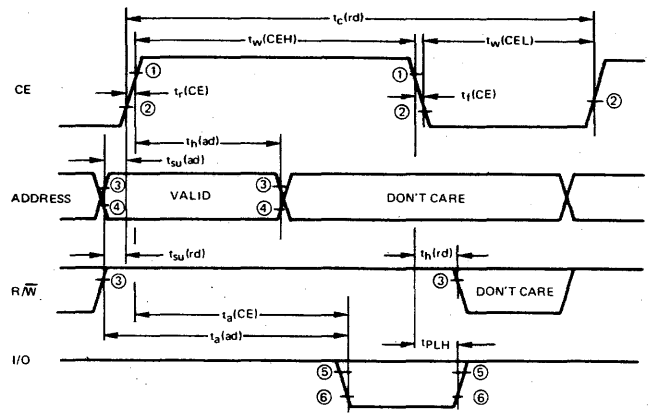
T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD418 MIN.	μPD418 MAX.	μPD418-1 MIN.	μPD418-1 MAX.	μPD418-2 MIN.	μPD418-2 MAX.	UNIT	TEST CONDITIONS
Refresh Time	t_{ref}		2		2		2	ms	
Read Modify Write Cycle Time	t_c(RMW)	650		610		580		ns	
Pulse Width, CE High	t_w(CEH)	480	4000	440	4000	410	4000	ns	
Pulse Width, CE Low	t_w(CEL)	130		130		130		ns	
Write Pulse Width	t_w(wr)	180		180		180		ns	
CE Rise Time	t_r(CE)		40		40		40	ns	
CE Fall Time	t_f(CE)		40		40		40	ns	
Write Pulse Setup Time	t_{su}(wr)	200		200		200		ns	
Address Setup Time	t_{su}(ad)	0		0		0		ns	
Read Pulse Setup Time	t_{su}(rd)	0		0		0		ns	
Data Setup Time	t_{su}(da)	150		150		150		ns	
Data Hold Time	t_h(da)	40		40		40		ns	
Address Hold Time	t_h(ad)	150		150		150		ns	
Access Time From Address	t_a(ad)		300		250		200	ns	C_L = 50pF, R_L = 2.2 kΩ to 5.5V Load = 1 TTL Gate, t_r(CE) = 20 ns
Access Time From CE	t_a(CE)		280		230		180	ns	C_L = 50pF, R_L = 2.2 kΩ to 5.5V Load = 1 TTL Gate

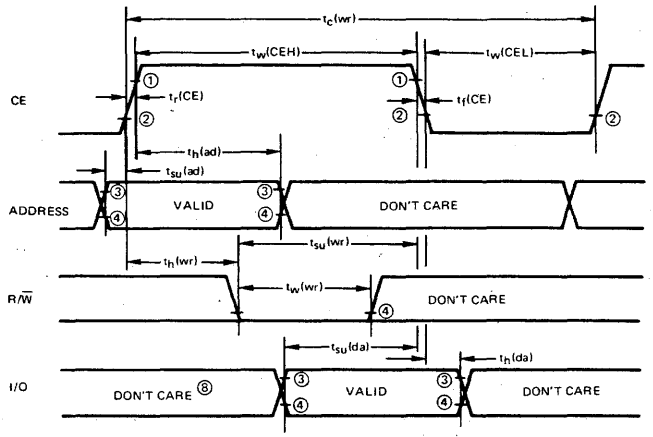
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TIMING WAVEFORMS

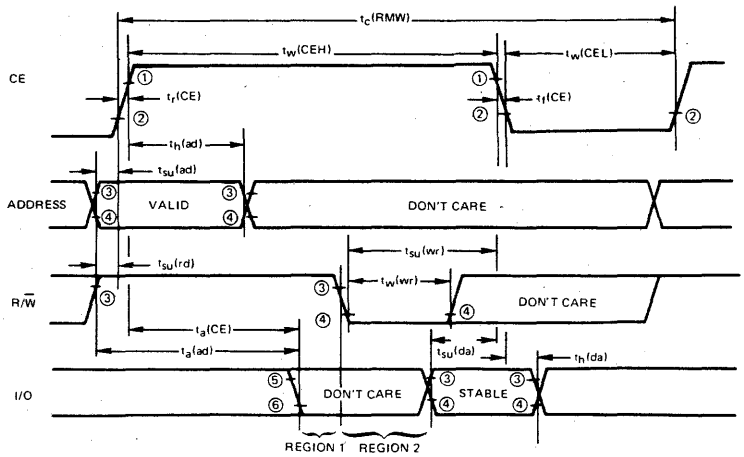
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



Notes:
① V_{DD} – 2V is the reference level for measuring timing of CE.
② V_{SS} + 2V is the reference level for measuring timing of CE.
③ V_{IH} MIN. is the reference level for measuring timing of addresses, R/$\overline{W}$, I/O (Write cycle).
④ V_{IL} MAX. is the reference level for measuring timing of addresses, R/$\overline{W}$, I/O (Write cycle).
⑤ V_{OH} MIN. is the reference level for measuring timing of I/O (Read cycle).
⑥ V_{OL} MAX. is the reference level for measuring timing of I/O (Read cycle).
⑦ During the time from the rise of CE to the fall of R/$\overline{W}$, R/$\overline{W}$ is permitted to change from high to low only.
⑧ If R/$\overline{W}$ remains high more than t_h(wr) from CE goes to high, the Data in driver must be disabled until R/$\overline{W}$ goes to low. (See Note 9.)
⑨ In region 1, Data out is valid until the I/O terminal is forced high or low by the data in driver. A transition from low to high is permissible but additional power to overcome the output buffer will be required. A transition from high to low is permitted without power penalty. In region 2, during the time from the fall of R/$\overline{W}$ to (t_f(R/$\overline{W}$) + 50 ns, MAX.), a transition from low to high permissible but additional power to overcome the output buffer will be required.

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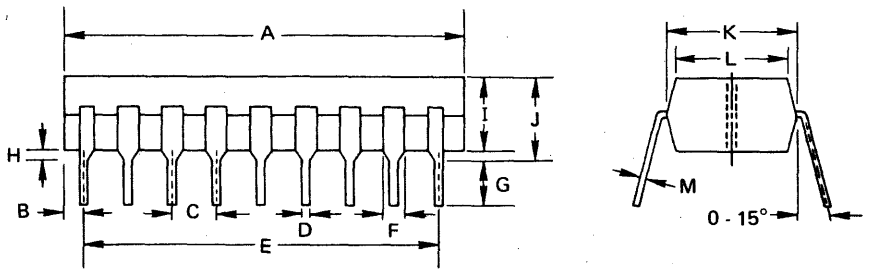
CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V ± 10%①
V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Capacitance Address Inputs	C_I(ad)		3.5	6	pF	V_I = 0V
Input Capacitance CE Input	C_I(CE)		13	18	pF	V_I(CE) = 12V
			13	18		V_I(CE) = 0V
Input Capacitance R/$\overline{W}$ Input	C_I(R/$\overline{W}$)		4.5	6	pF	V_I = 0V
I/O Terminal Capacitance	C_I(I/O)		5	7	pF	V_I = 0V

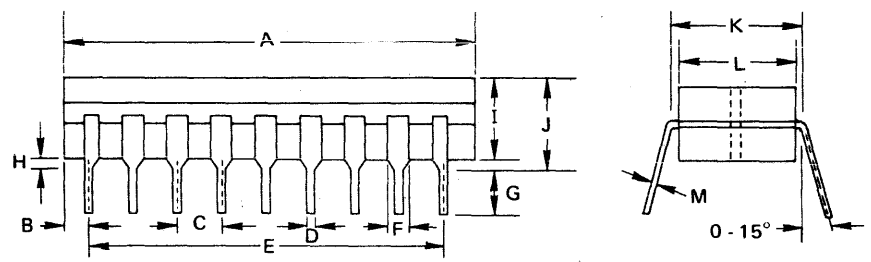
Note: ① All voltages referenced to V_{SS}.

PACKAGE OUTLINE μPD418C/D



μPD418C (Plastic)

ITEM	MILLIMETERS	INCHES
A	22.5 MAX.	0.89
B	1.09	0.04
C	2.54	0.10
D	0.50 ± 0.10	0.02
E	20.32	0.80
F	1.2 MIN.	0.05
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01



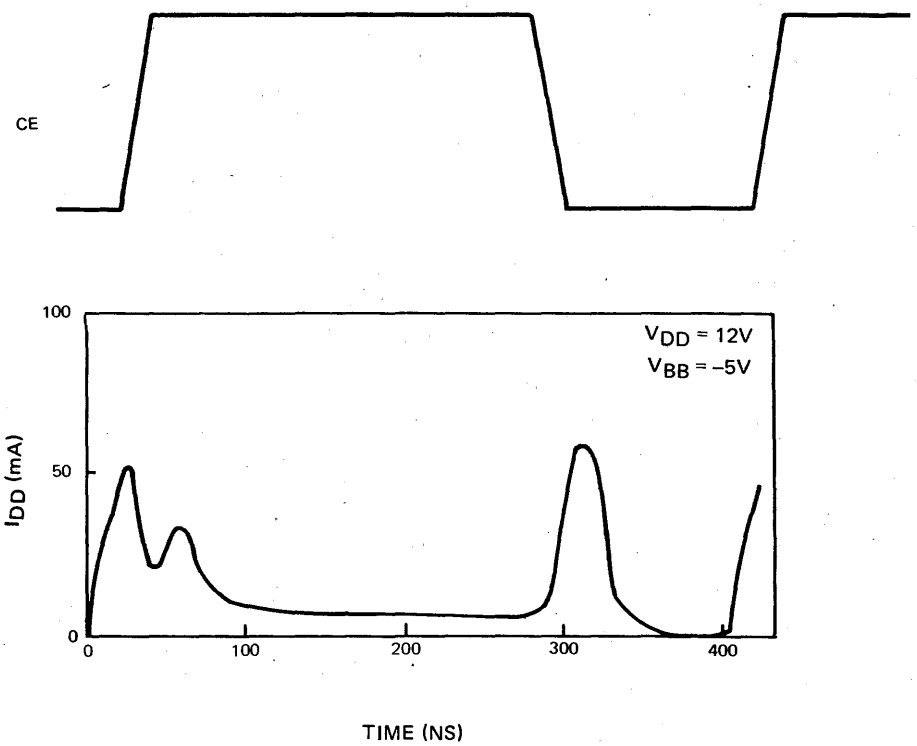
μPD418D (Cerdip)

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

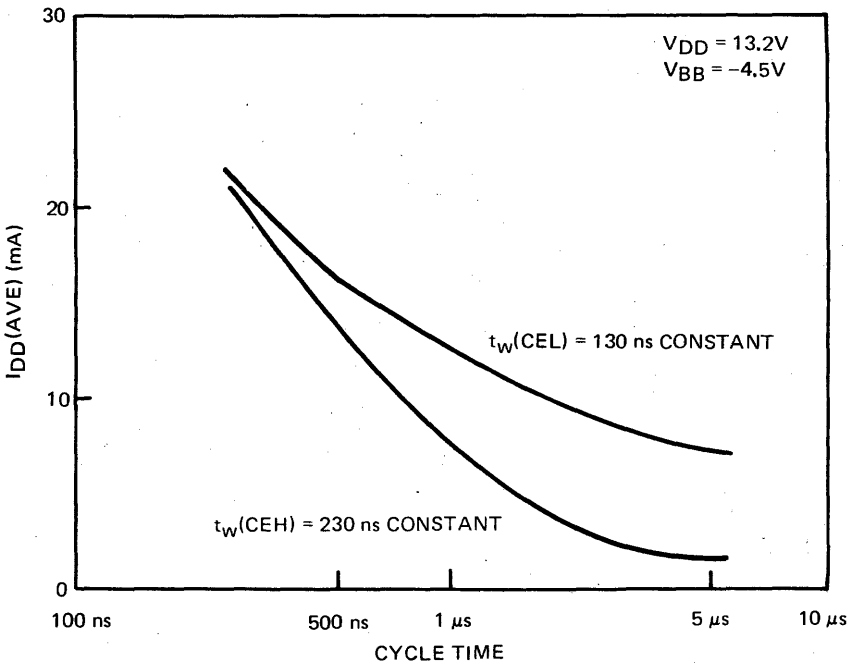
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I_{DD} CHARACTERISTICS

I_{DD} WAVEFORM



I_{DD}(AVE) VS CYCLE TIME



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1024-BIT BIPOLAR TTL RAM

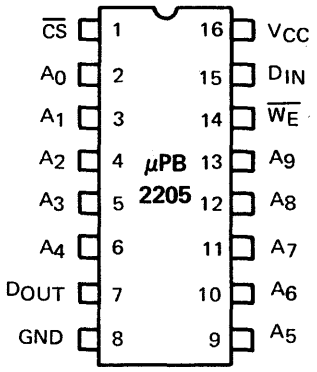
DESCRIPTION

The NEC μPB2205 integrated circuits are high-speed Open-Collector TTL interface, 1024-bit Random Access Memories.

FEATURES

- 1024 Words x 1 Bit Organization (Fully Decoded)
- TTL Interface
- Fast Access Time – 50 ns max.
- Power Consumption – 500 mW typ.
- A Chip Select Input for Memory Expansion
- Open-Collector Output
- Ceramic 16-Lead Dual-In-Line Package
- Compatibility with Fairchild's "93415" and Equivalent Devices

PIN CONFIGURATION

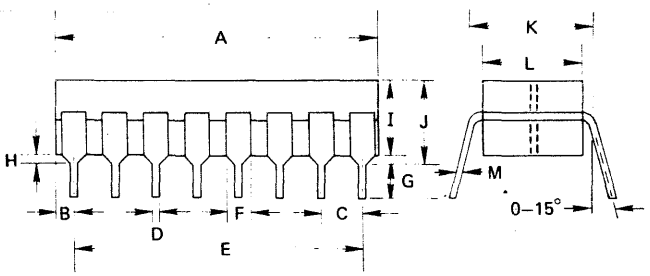


FUNCTION TABLE

CHIP SELECT	WRITE ENABLE	OPERATION	OUTPUT
0	0	WRITE	1
0	1	READ	Non-Inverted Data Written in Memory
1	X	HOLD	1

X – High or Low.

PACKAGE OUTLINE μPB2205D



ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	$0.0098^{+0.0039}_{-0.0019}$

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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . -25°C to +75°C
Storage Temperature . . . . . -65°C to +150°C
Output Voltage . . . . . -0.5 to +5.5 Volts
Input Voltage . . . . . -0.5 to +5.5 Volts
Supply Voltage V_{CC} . . . . . -0.5 to +7 Volts
Output Current . . . . . 50 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 75°C; V_{CC} = 4.75 to 5.25V ①

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High Current	I_{IH}			40	μA	V_I = 2.7V
Input Low Current	$-I_{IL}$			0.40	mA	V_I = 0.4V
Output Low Voltage	V_{OL}			0.50	V	I_{OL} = 16 mA
Output High Current	I_{OH}			100	μA	V_{OH} = 5.25V
Input Clamp Voltage	$-V_{IC}$			1.3	V	$-I_I$ = 12 mA
Power Supply Current	I_{CC}		100	155	mA	All input except W_E grounded.

Note: ① Guaranteed with transverse airflow exceeding 400 linear F.P.M. and two minute warm-up.
Typical thermal resistance values of the package are:
θ_{JA} (Junction to Ambient) = 50° C/W (at 400 F.P.M. airflow)
θ_{JA} (Junction to Ambient) = 70° C/W (Free Air)
Under free air condition, ambient temperature is guaranteed 0°C to 65°C.

AC CHARACTERISTICS

T_a = 0°C to 75°C; V_{CC} = 4.75 to 5.25V

PARAMETER		SYMBOL	LIMITS			UNIT
			MIN	TYP	MAX	
Read Access Time	Address Access	t_{AA}	10		50	ns
	$\overline{CS}$ Access	t_{ACS}	5		30	ns
	$\overline{CS}$ Recovery	t_{RCS}			30	ns
Write Pulse Width Time		t_W			60	ns
Write Set-Up Time	Address Set-Up	t_{WSA}	25			ns
	Data-In Set-Up	t_{WSD}	5			ns
	$\overline{CS}$ Set-Up	t_{WSCS}	5			ns
Write Hold Time	Address Hold	t_{WHA}	5			ns
	Data-In Hold	t_{WHD}	5			ns
	$\overline{CS}$ Hold	t_{WHCS}	5			ns
Write Disable Time		t_{WD}			40	ns
Write Recovery Time		t_{WR}			40	ns

Notes: ① Output Load — Fig. 1. Capacitances C_L in Fig. 1 including jig and scope.
② Input Waveform — 0V for "0" level and 3.0V for "1" level, less than 10 ns for both rise and fall time.
③ Measurement Reference — 1.5V for both inputs and output.

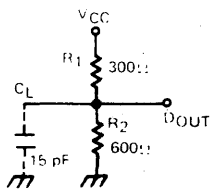
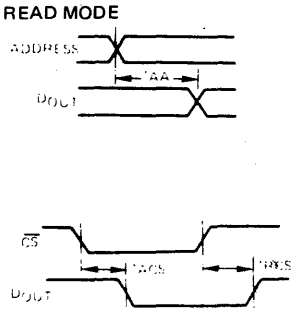


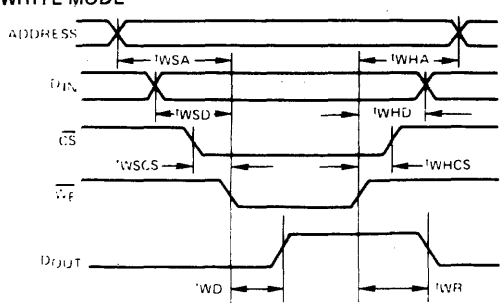
Figure 1

TIMING WAVEFORMS

READ MODE



WRITE MODE



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4096 BIT HIGH SPEED STATIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The μPD410 is a very high speed 4K bit static random access memory. It is organized as 4096 words by 1 bit per word and fabricated using N channel silicon gate MOS technology.

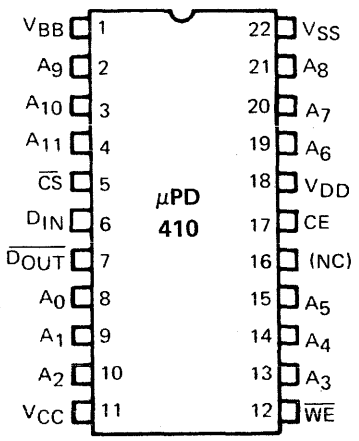
All signals to the device are TTL compatible except for Chip Enable which is standard +12 Volt MOS level.

Circuit operation starts with the rising edge of CE. Data is latched and valid until falling edge of CE. Address and Chip Select signals are latched on-chip to simplify system timing requirements.

FEATURES

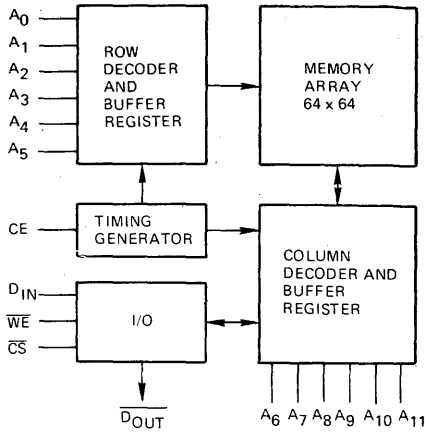
- 4096 Words x 1 Bit Organization
- Fully Decoded
- TTL Compatible (except CE)
- High Speed-Access Time: 100 ns max.
- Cycle Time: 220 ns min.
- Static Operation — No Refresh Required
- Standby Power: 75 mW max.
- Active Power: 470 mW typ.
- Supply Voltages: V_{DD} = +12V, V_{CC} = +5V, V_{BB} = -5V
- Address Registers on the Chip
- Three State Output
- Standard 22 Pin Ceramic Dual-in-Line Package
- Pin Compatible with μPD411 and Other 4K Dynamic RAMs

PIN CONFIGURATION



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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Output Voltages	-0.3 to +20 Volts①
All Input Voltages	-0.3 to +20 Volts①
Supply Voltage V_{DD}	-0.3 to +20 Volts①
Supply Voltage V_{CC}	-0.3 to +20 Volts①
Supply Voltage V_{SS}	-0.3 to +20 Volts①
Power Dissipation	1.0W

Note: ① Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

*T_a = 25°C

T_a = 0°C to 70°C; V_{DD} = 12V ± 5%; V_{CC} = 5V ±5%; V_{BB} = -5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Leakage Current	I_{LI}			10	μA	V_{IN} = V_{IL}MIN to V_{IH} MAX
CE Input Leakage Current	I_{LC}			10	μA	V_{IN} = V_{ILC} MIN to V_{IHC} MAX
Output Leakage Current	I_{LO}			10	μA	$\overline{CE}$ = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
V_{DD} Supply Current during CE off	I_{DDOFF}			200	μA	CE = -1.0V to 0.6V
V_{DD} Supply Current during CE on	I_{DDON}			60	mA	CE = V_{IHC}
Average V_{DD} Current	I_{DDAV}			60	mA	Cycle Time = min
V_{BB} Supply Current	I_{BB}			100	μA	
V_{CC} Supply Current during CE off	I_{CCOFF}			15	mA	$\overline{CE}$ = V_{ILC} or $\overline{CS}$ = V_{IH}
Average V_{CC} Current	I_{CCAV}			21	mA	D_{OUT} = No load
Input Low Voltage	V_{IL}	-1.0		0.6	V	
Input High Voltage	V_{IH}	2.4		V_{CC}+1	V	
CE Input Low Voltage	V_{ILC}	-1.0		0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD}-1		V_{DD}+1	V	
Output Low Voltage	V_{OL}	0		0.4	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = 2.0 mA

Note: ① Typical values are for T_a = 25°C and nominal supply voltages.

CAPACITANCE

T_a = 0°C to 70°C; V_{DD} = 12V ± 5%; V_{CC} = 5V ± 5%; V_{BB} = -5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address Capacitance	C_{AD}		4	6	pF	V_{IN} = V_{SS}
$\overline{CS}$ Capacitance	C_{CS}		4	6	pF	V_{IN} = V_{SS}
D_{IN} Capacitance	C_{IN}		8	10	pF	V_{IN} = V_{SS}
$\overline{D_{OUT}}$ Capacitance	C_{OUT}		5	7	pF	V_{OUT} = V_{SS}
$\overline{WE}$ Capacitance	C_{WE}		8	10	pf	V_{IN} = V_{SS}
CE Capacitance	C_{CE}		18	27	pf	V_{IN} = V_{SS}

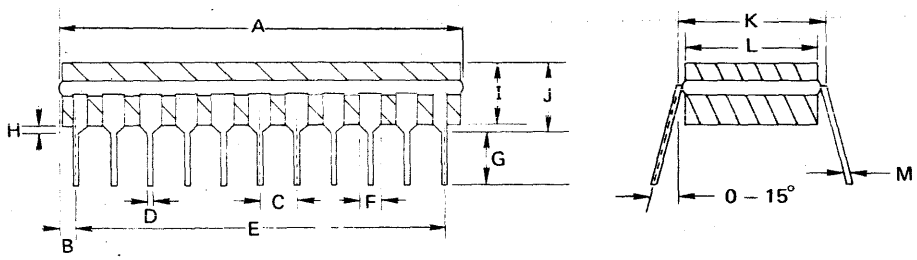
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AC CHARACTERISTICS

T_a = 0°C to 70°C; V_{DD} = 12V ± 5%; V_{CC} = 5V ± 5%; V_{BB} = -5V ± 5%; V_{SS} = 0V (410-2: T_a = 0°C to 55°C)

PARAMETER	SYMBOL	LIMITS									UNIT	TEST CONDITIONS
		410			410-1			410-2				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
READ, WRITE AND READ-MODIFY-WRITE												
Address to CE Set Up Time	t_{AC}	0			0			0			ns	
Address Hold Time	t_{AH}	90			70			50			ns	
CE Off Time	t_{CC}	100			140			90			ns	
CE Transition Time	t_T	0		40	0		40	0		40	ns	
CE off to Output High Impedance State	t_{CF}	0		90	0		90	0		90	ns	
READ												
Cycle Time	t_{CY}	440			330			220			ns	t_T = 10 ns
CE on Time	t_{CE}	230		2000	170		2000	110		2000	ns	
CE Output Delay	t_{CO}			190			140			90	ns	Load = 50 pF + 1TTL, Ref = 2.0 or 0.8V
Access Time	t_{ACC}			200			150			100	ns	$t_{ACC} = t_{AC} + t_{CO} + t_T$
CE to $\overline{WE}$	t_{WL}	20			20			20			ns	
$\overline{WE}$ to CE on	t_{WC}	0			0			0			ns	
WRITE												
Cycle Time	t_{CY}	440			330			220			ns	t_T = 10 ns
CE on Time	t_{CE}	230		2000	170		2000	110		2000	ns	
$\overline{WE}$ to CE off	t_W	130			100			70			ns	
CE to $\overline{WE}$	t_{CW}	130			100			70			ns	
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0			0			0			ns	
D_{IN} Hold Time	t_{DH}	60			40			20			ns	
$\overline{WE}$ Pulse Width	t_{WP}	130			100			70			ns	
READ-MODIFY-WRITE												
Read-Modify-Write (RMW) Cycle Time	t_{RWC}	560			420			280			ns	t_T = 10 ns
CE Width During RMW	t_{CRW}	350		2000	260		2000	170		2000	ns	
$\overline{WE}$ to CE on	t_{WC}	0			0			0			ns	
$\overline{WE}$ to CE off	t_W	130			100			70			ns	
$\overline{WE}$ Pulse Width	t_{WP}	130			100			70			ns	
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0			0			0			ns	
D_{IN} Hold Time	t_{DH}	60			40			20			ns	
CE to Output Delay	t_{CO}			190			140			90	ns	Load = 50 pF + 1TTL, Ref = 2.0 or 0.8V
Access Time	t_{ACC}			200			150			100	ns	$t_{ACC} = t_{AC} + t_{CO} + t_T$

PACKAGE OUTLINE μPD410D

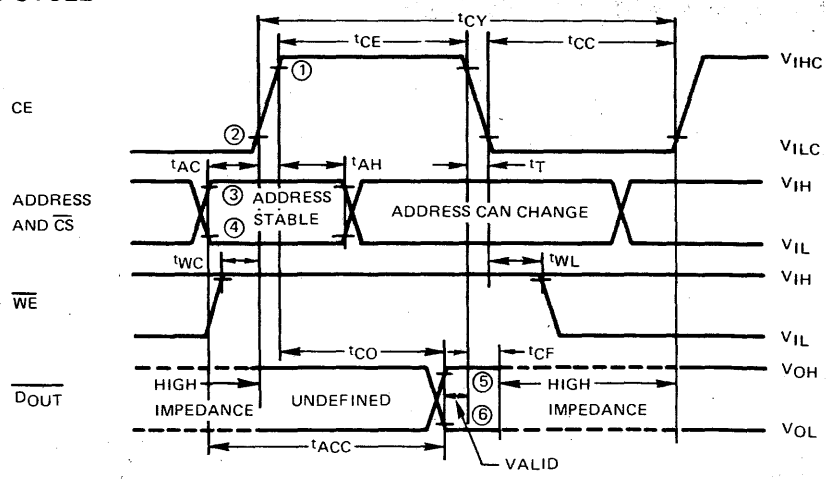


ITEM	MILLIMETERS	INCHES
A	27.43 Max.	1.079 Max.
B	1.27 Max.	0.05 Max.
C	2.54 ± 0.1	0.10
D	0.42 ± 0.1	0.016
E	25.4 ± 0.3	1.0
F	1.5 ± 0.2	0.059
G	3.5 ± 0.3	0.138
H	3.7 ± 0.3	0.145
I	4.2 Max.	0.165 Max.
J	5.08 Max.	0.200 Max.
K	10.16 ± 0.15	0.400
L	9.1 ± 0.2	0.358
M	0.25 ± 0.05	0.009

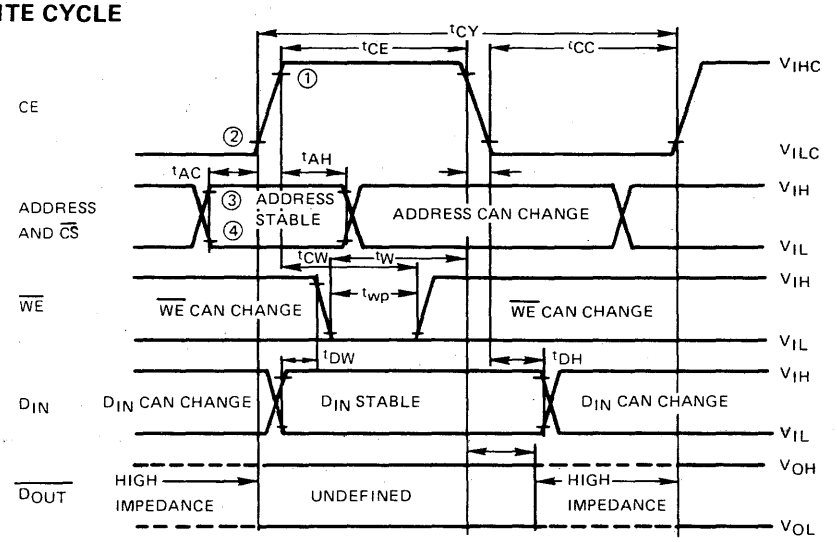
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TIMING WAVEFORMS

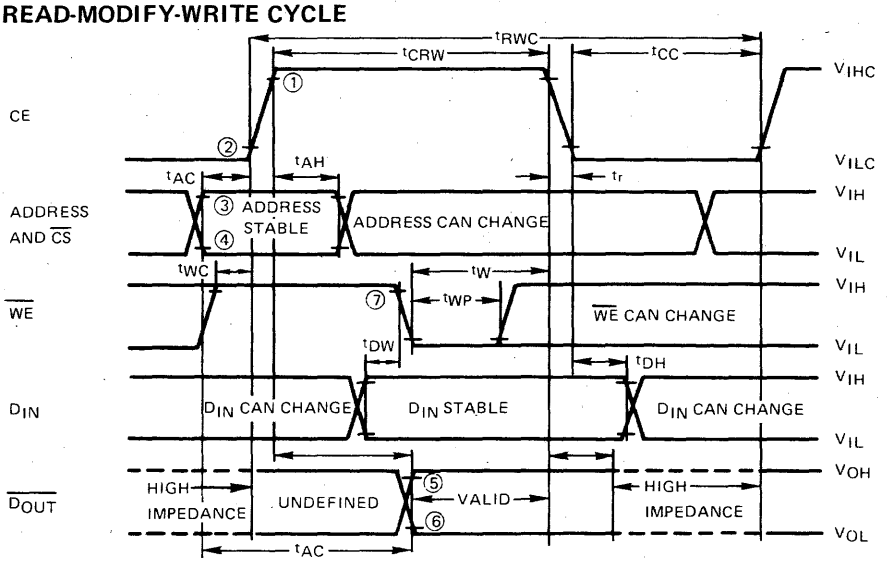
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



Notes:
① V_{DD} − 2V is the reference level for measuring timing of CE.
② V_{SS} + 2V is the reference level for measuring timing of CE.
③ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
④ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
⑤ V_{SS} + 2.0V is the reference level for measuring timing of $\overline{D_{OUT}}$.
⑥ V_{SS} + 0.8V is the reference level for measuring timing of $\overline{D_{OUT}}$.
⑦ $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

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μPD2101AL
μPD2101AL-2
μPD2101AL-4

1024 BIT (256 X 4) STATIC MOS RAM WITH SEPARATE I/O

DESCRIPTION

The μPD2101ALC is a 256 word by 4 bit static random access memory requiring no clocks or refreshing. It features high speed, low cost, and simplicity of interfacing.

It is directly TTL compatible in all respects; inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The output disable function eliminates the need for bidirectional logic in a common I/O system. Output data is the same polarity as input data, and readout is non-destructive.

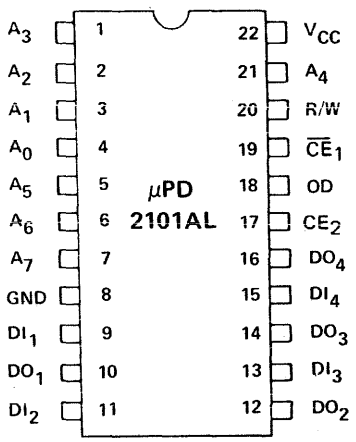
The μPD2101ALC family of devices offers access times from 450 ns to 250 ns with a typical standby mode power dissipation of only 36 mW.

The use of NEC's N-channel silicon gate MOS process, with its excellent protection from contamination, permits the use of a low cost 22 pin plastic package in providing a high performance, high reliability MOS circuit at a most cost effective price level. The μPD2101ALC is pin-compatible with the μPD5101C CMOS static RAM.

FEATURES

- 256 x 4 Organizations to Meet Needs for Small System Memories
- Access Time – 250 to 450 nsec max
- Directly TTL Compatible – All Inputs and Output
- Static MOS – No Clocks or Refreshing Required
- Simple Memory Expansion – Chip Enable Input
- Low Standby Power – 36 mW typ.
- Low Cost Packaging – 22 Pin Plastic Dual-in-Line Configuration
- Low Operating Power
- Three-State Output – OR-Tie Capability
- Output Disable Provided for Ease of Use in Common Data Bus Systems

PIN CONFIGURATION



PIN NAMES

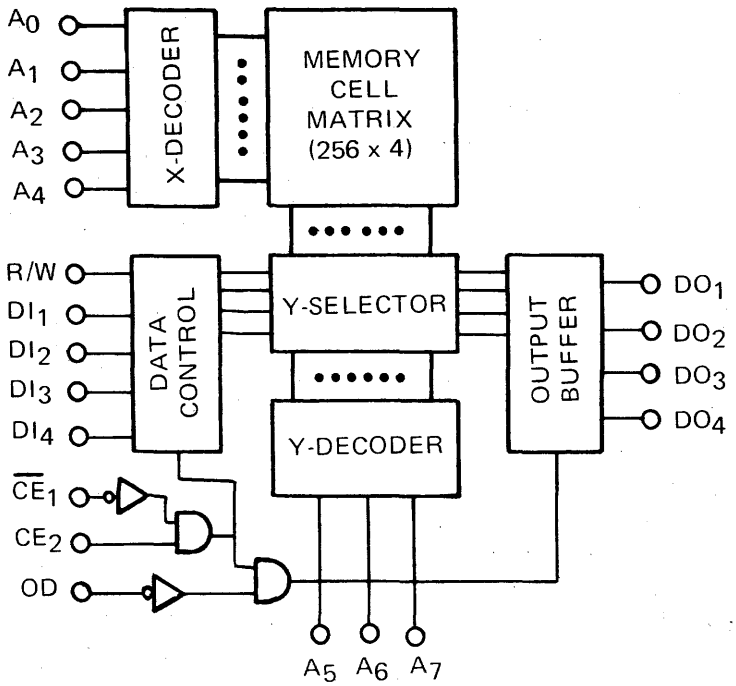
DI_1–DI_4	DATA INPUT	CE_2	CHIP ENABLE 2
A_0–A_7	ADDRESS INPUTS	OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT	DO_1–DO_4	DATA OUTPUT
$\overline{CE}_1$	CHIP ENABLE 1	V_{CC}	POWER (+5V)

OPERATION MODES

$\overline{CE}_1$	CE_2	OD	CHIP	OUTPUT MODE
0	1	0	Selected	Data Out
0	1	1		High Impedance
Others			No-Selected	

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-10°C to +70°C
Storage Temperature	-65°C to +125°C
All Output Voltages	-0.5 to +7 Volts
All Input Voltages	-0.5 to +7 Volts
Supply Voltage V_{CC}	-0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = -10°C to +70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	+2.0		V_{CC}	V	
Input Low Voltage	V_{IL}	-0.5		+0.8	V	
Output High Voltage	V_{OH}	+2.4			V	I_{OH} = -100 μA
Output Low Voltage	V_{OL}			+0.4	V	I_{OL} = +2.1 mA
Input Leakage Current High	I_{LIH}			+10	μA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			-10	μA	V_I = 0V
Output Leakage Current High	I_{LOH}			+10	μA	V_O = +2.4V to V_{CC} $\overline{CE}_1$ = +2.0V
Output Leakage Current Low	I_{LOL}			-10	μA	V_O = +0.4V $\overline{CE}_1$ = +2.0V
Power Supply Current	I_{CC1}			+60	mA	V_I = +5.25V I_O = 0 mA T_a = +25°C
Power Supply Current	I_{CC2}			+70	mA	V_I = +5.25V I_O = 0 mA T_a = -10°C to +70°C

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READ CYCLE

AC CHARACTERISTICS

T_a = −10°C to +70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS									UNIT
		2101AL-4			2101AL			2101AL-2			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Read Cycle Time	t_{RC}	450			350			250			ns
Access Time	t_A			450			350			250	ns
Chip Enable to Output	t_{CO}			180			150			130	ns
Output Disable to Output	t_{OD}			150			130			120	ns
Data Output to High Z State	t_{DF}*	0		130	0		115	0		100	ns
Previous Read Data Valid After Change of Address	t_{OH}	40			40			40			ns

*t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, CE_2, or OD, whichever occurs first.

WRITE CYCLE

T_a = −10°C to +70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS									UNIT
		2101AL-4			2101AL			2101AL-2			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Write Cycle Time	t_{WC}	450			350			250			ns
Write Delay	t_{AW}	20			20			20			ns
Chip Enable to Write	t_{CW}	180			150			130			ns
Data Setup Time	t_{DW}	180			150			130			ns
Data Hold Time	t_{DH}	0			0			0			ns
Write Pulse Width	t_{WP}	160			130			120			ns
Write Recovery	t_{WR}	0			0			0			ns
Output Disable Setup	t_{DS}	20			20			10			ns

Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

STANDBY CHARACTERISTICS

T_a = −10°C to +70°C

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.①	MAX.		
V_{CC} in Standby	V_{PD}	1.5			V	
$\overline{CE}_1$ Bias in Standby	V_{CES}	2.0			V	$2.0V \leq V_{PD} \leq 5.25V$
		V_{PD}			V	$1.5V \leq V_{PD} < 2.0V$
Standby Current Drain	I_{PD1}		24	36	mA	All Inputs = V_{PD1} = 1.5V
Standby Current Drain	I_{PD2}		30	45	mA	All Inputs = V_{PD2} = 2.0V
Chip Deselect to Standby Time	t_{CP}	0			ns	
Standby Recovery Time	t_R	t_{RC}②			ns	

Notes: ① Typical values are for T_a = 25°C and nominal supply voltage.
② $t_R = t_{RC}$ (Read Cycle Time).

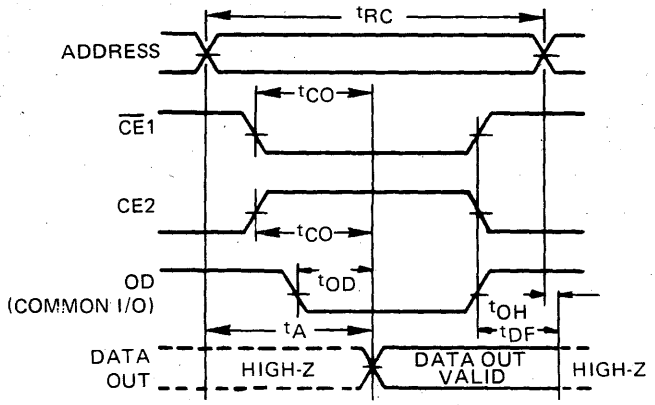
CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Capacitance	C_{IN}			8	pf	V_I = 0V
Output Capacitance	C_{OUT}			12	pf	V_O = 0V

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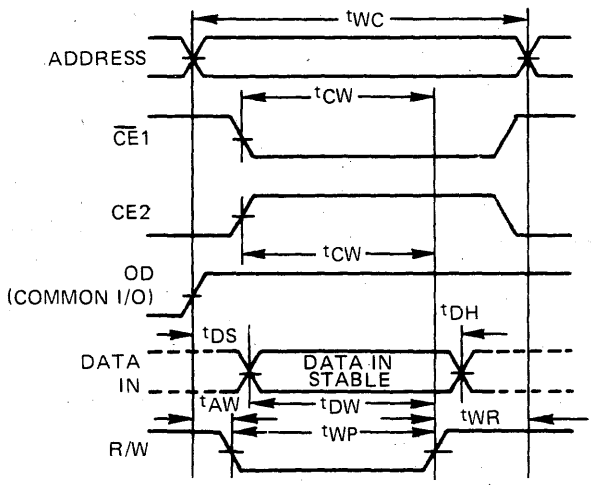
TIMING WAVEFORMS

READ CYCLE



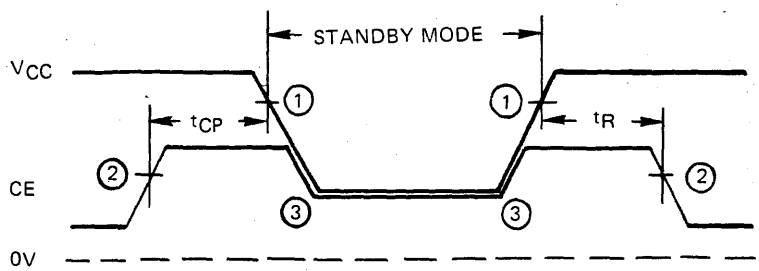
Notes: (1) OD should be tied low for separate I/O operation.
(2) R/W is high for read operation.

WRITE CYCLE



Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

STANDBY WAVEFORMS



Notes: (1) 4.75V
(2) 2.0V
(3) 1.5V

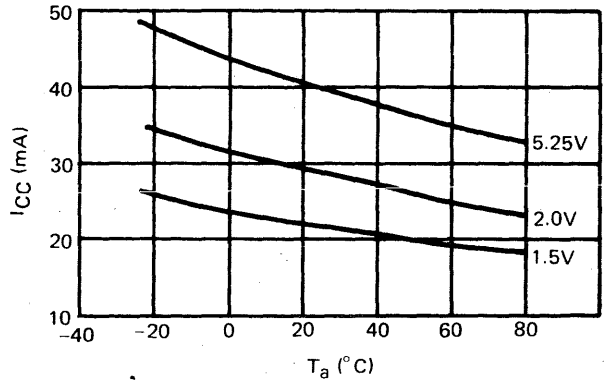
AC CONDITIONS OF TEST

Input Pulse Levels	+0.8V to +2.0V
Input Pulse Rise and Fall Times	20 ns
Timing Measurement Reference Level	1.5V
Output Load	1 TTL + 100 pF

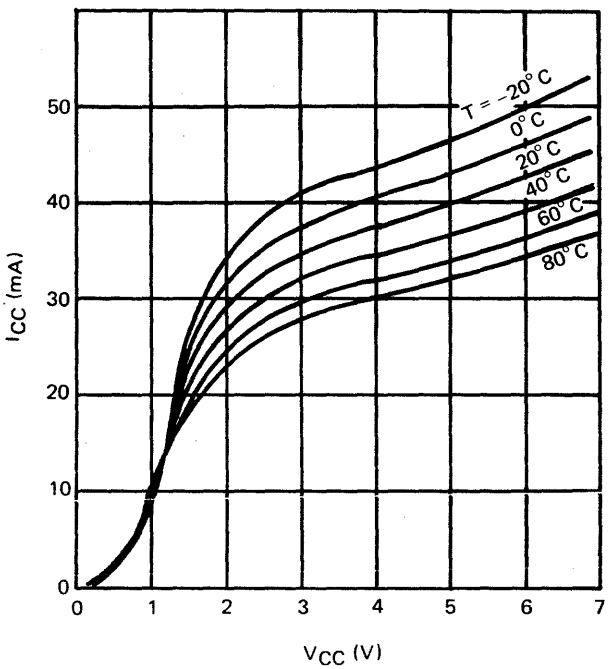
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TYPICAL OPERATING CHARACTERISTICS

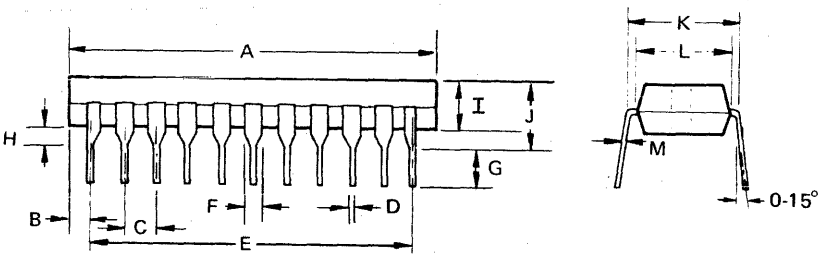
I_{CC} VS T_a



I_{CC} VS V_{CC}



PACKAGE OUTLINE μPD2101ALC



ITEM	MILLIMETERS	INCHES
A	28.0 MAX.	1.10 MAX.
B	1.4 MAX.	0.025
C	2.54	0.10
D	0.50	0.02
E	25.4	1.00
F	1.40	0.055
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.7 MAX.	0.18 MAX.
J	5.2 MAX.	0.20 MAX.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{0.05}$	$0.01^{+0.004}_{0.002}$

SP2101-8-77-GY-CAT

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1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The μPD2102AL is a 1024 words by one bit static Random Access Memory requiring no clocks or refreshing. A family of devices with maximum access times ranging from 250 ns to 450 ns meet the requirements of microcomputer memory applications where speed, low cost and easy interfacing are prime design objectives.

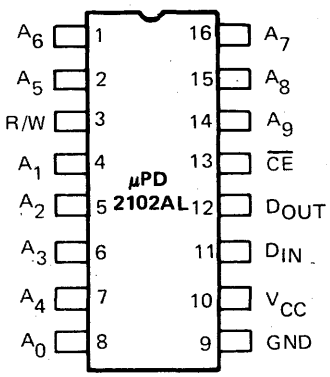
All μPD2102AL inputs and outputs are TTL compatible. A single chip-enable ($\overline{CE}$) pin is provided for selection of an individual device in systems with OR-tied outputs. Output data is the same polarity as input data and is nondestructively read out. Only a single +5 volt supply is required. In standby mode, with the supply lowered to 1.5 volts, power dissipation is reduced to 42 mW max.

The μPD2102AL family is fabricated using NEC's N-channel MOS silicon gate process, providing excellent contamination protection. This process permits the use of a low cost plastic package (16 pin) and enables high performance, highly reliable MOS circuits to be produced.

FEATURES

- Access Time – μPD2102AL-2 – 250 ns Max
  μPD2102AL – 350 ns Max
  μPD2102AL-4 – 450 ns Max
- Single +5 Volts Supply Voltage
- Directly TTL Compatible – All Inputs and Output
- Static MOS – No Clocks or Refreshing Required
- Low Power – Typically 150 mW
- Low Standby Power – 42 mW max
- Three-State Output – OR-TIE Capability
- Simple Memory Expansion – Chip Enable Input
- Fully Decoded – On Chip Address Decode
- Inputs Protected – All Inputs have Protection against Static Charge
- Low Cost Packaging – 16 Pin Plastic Dual-In-Line Configuration

PIN CONFIGURATION

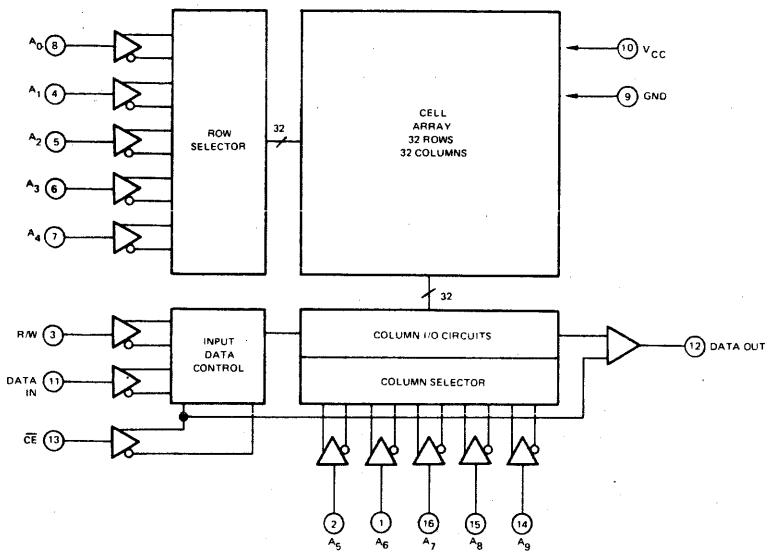


PIN NAMES

$A_0 - A_9$	Address Inputs
R/W	Read/Write
$\overline{CE}$	Chip Enable
V_{CC}	Power (+5V)

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . -10°C to 70°C
Storage Temperature . . . . . -65°C to +125°C
Voltage On Any Pin . . . . . -0.5 to +7 Volts ①

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

*T_a = 25°C

DC CHARACTERISTICS

T_a = -10°C to +70°C; V_{CC} = 5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Leakage Current	I_{LI}			±10	μA	V_{IN} = 0 to 5.25V
I/O Leakage Current	I_{LOH}			+5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = +2.4V to V_{CC}
I/O Leakage Current	I_{LOL}			-10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
Power Supply Current	I_{CC1}		30	70	mA	All Inputs = 5.25V, Data Out Open
Input "Low" Voltage	V_{IL}	-0.5		+0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC}	V	
Output "Low" Voltage	V_{OL}			+0.4	V	I_{OL} = 2.1 mA
Output "High"	V_{OH}	2.4			V	I_{OH} = -100 μA

Note: ① Typical values are for T_a = 25°C and nominal supply voltage

CAPACITANCE

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		3	5	pf	V_{IN} = 0V
Output Capacitance	C_{OUT}		7	10	pf	V_{OUT} = 0V

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AC CHARACTERISTICS

READ CYCLE

$T_a = -10°C$ to $+70°C$; $V_{CC} = +5V$ ±5% unless otherwise noted

PARAMETER	SYMBOL	LIMITS 2102AL-4 MIN	2102AL-4 MAX	2102AL MIN	2102AL MAX	2102AL-2 MIN	2102AL-2 MAX	UNIT	TEST CONDITIONS
Read Cycle	t_{RC}	450		350		250		ns	$t_T = t_r = t_f = 100$ ns $C_L = 100$ pF Load = 1 TTL Gate $V_{ref} = 2.0$ or 0.8V
Access Time	t_A		450		350		250	ns	
Chip Enable to Output Time	t_{CO}		230		180		130	ns	
Previous Read Data Valid in Respect to Address	t_{OH1}	40		40		40		ns	
Previous Read Data Valid in Respect to Chip Enable	t_{OH2}	0		0		0		ns	

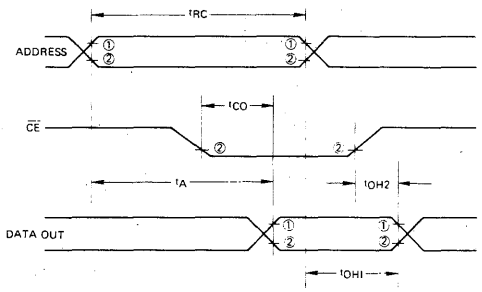
WRITE CYCLE

$T_a = -10°C$ to $+70°C$; $V_{CC} = +5V$ ± 5% unless otherwise noted

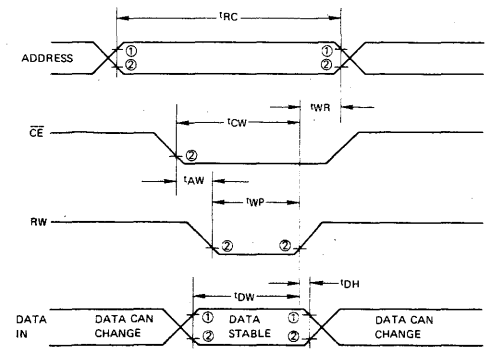
PARAMETER	SYMBOL	LIMITS 2102AL-4 MIN	2102AL-4 MAX	2102AL MIN	2102AL MAX	2102AL-2 MIN	2102AL-2 MAX	UNIT	TEST CONDITIONS
Write Cycle	t_{WC}	450		350		250		ns	$t_T = t_r = t_f = 100$ ns $C_L = 100$ pF Load = 1 TTL Gate $V_{ref} = 2.0$ or 0.8V
Address to Write Setup Time	t_{AW}	20		20		20		ns	
Write Pulse Width	t_{WP}	300		250		180		ns	
Write Recovery Time	t_{WR}	0		0		0		ns	
Data Setup Time	t_{DW}	300		250		180		ns	
Data Hold Time	t_{DH}	0		0		0		ns	
Chip Enable to Write Setup Time	t_{CW}	300		250		180		ns	

TIMING WAVEFORMS

READ CYCLE



WRITE CYCLE



Notes: ① 2.0 Volts
② 0.8 Volts

STANDBY CHARACTERISTICS

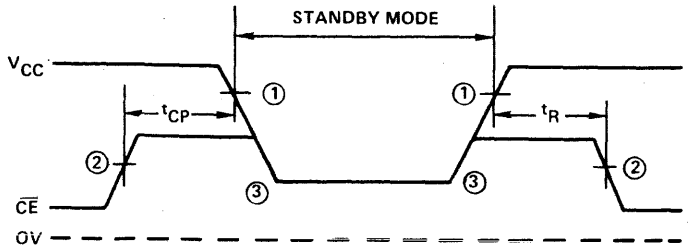
$T_a = 0$ to $+70°C$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{CC} in Standby	V_{PD}	1.5			V	
$\overline{CE}$ Bias in Standby	V_{CES}	2.0			V	$+2.0V \leq V_{PD} \leq +5.25V$
	V_{PD}				V	$+1.5V \leq V_{PD} < +2.0V$
Standby Current Drain	I_{PD1}		14	28	mA	All Inputs, $V_{PD1} = +1.5$
Standby Current Drain	I_{PD2}		18	38	mA	All Inputs, $V_{PD2} = +2.0V$
Chip Deselect to Standby Time	t_{CP}	0			ns	
Standby Recovery Time	t_R	t_{RC} ①			ns	

① t_{RC} = Read Cycle Time

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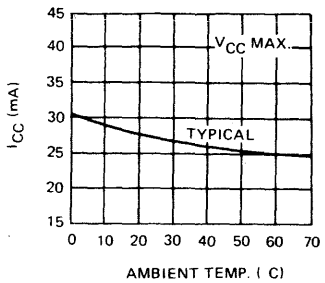
STANDBY MODE TIMING WAVEFORM



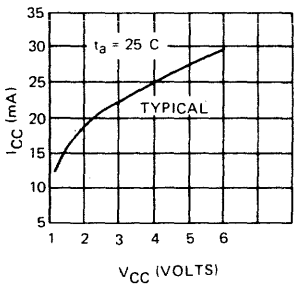
① 4.75V
② 2.0V
③ 1.5V

TYPICAL CHARACTERISTICS

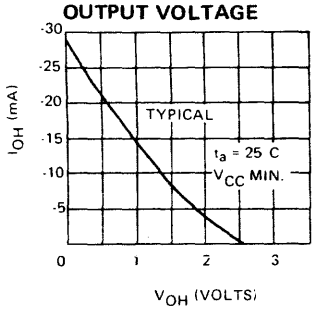
POWER SUPPLY CURRENT VS AMBIENT TEMPERATURE



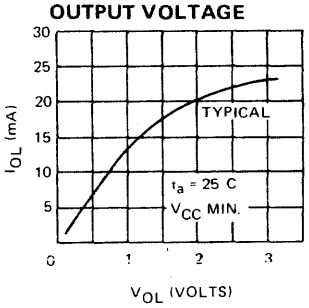
POWER SUPPLY CURRENT VS SUPPLY VOLTAGE



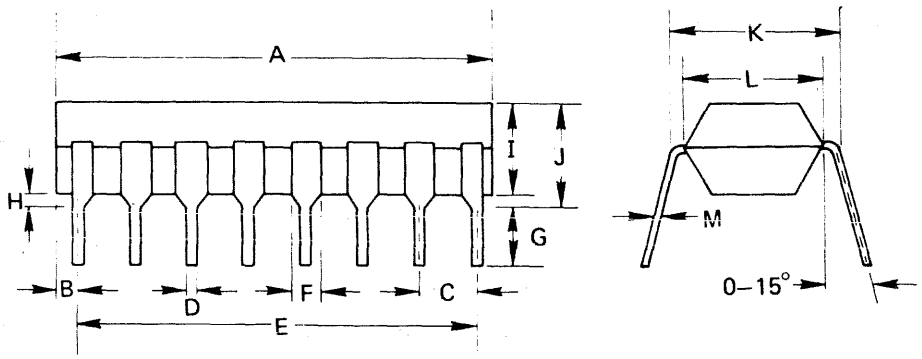
OUTPUT SOURCE CURRENT VS OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS OUTPUT VOLTAGE



PACKAGE OUTLINE μPD2102ALC



ITEM	MILLIMETERS	INCHES
A	19.4 MAX	0.76 MAX
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	4.05 MAX	0.16 MAX
J	4.55 MAX	0.18 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

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μPD2111AL
μPD2111AL-2
μPD2111AL-4

1024 BIT (256 x 4) STATIC MOS RAM WITH COMMON I/O AND OUTPUT DISABLE

DESCRIPTION

The μPD2111AL is a 256 words by 4 bits static random access memory fabricated with N-channel MOS technology. It uses fully static circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

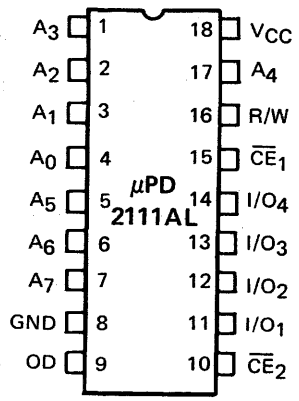
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate chip enable ($\overline{CE}$) leads allow easy selection of an individual package when outputs are OR-tied.

All members in the μPD2111AL family feature a low standby power mode with the supply voltage being reduced to +1.5V.

FEATURES

- 256 Words x 4 Bits Organization
- Common Data Input and Output
- Single +5V Supply Voltage
- Directly TTL Compatible — All Inputs and Outputs
- Static MOS — No Clocks or Refreshing Required
- Access Time — 250 ns to 450 ns max.
- Simple Memory Expansion — Chip Enable Inputs
- Fully Decoded — On Chip Address Decode
- Inputs Protected — All Inputs have Protection Against Static Charge
- Low Cost Packaging — 18 Pin Plastic Dual-In-Line Configuration
- Three-State Output — OR-Tie Capability
- Low Standby Power

PIN CONFIGURATION



PIN NAMES

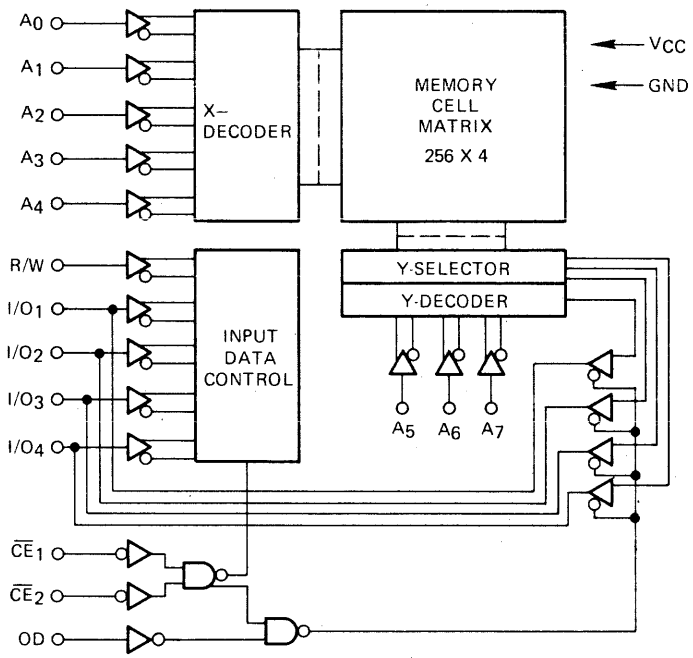
A_0 - A_7	Address Inputs
OD	Output Disable
R/W	Read/Write Input
$\overline{CE}_1$	Chip Enable 1
$\overline{CE}_2$	Chip Enable 2
I/O_1 - I/O_4	Data Input/Output

OPERATION MODES

$\overline{CE}_1$	$\overline{CE}_2$	OD	Chip Output Status	
0	0	0	Selected	Data Output
0	0	1		High Z
Others			Unselected	State

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +125°C
All Output Voltages	−0.5 to +7 Volts
All Input Voltages	−0.5 to +7 Volts
Supply Voltage V_{CC}	−0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = -10 to +70°C; V_{CC} = +5V ± 5%

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage		V_{IH}	+2.0		V_{CC}	V	
Input Low Voltage		V_{IL}	−0.5		+0.8	V	
Output High Voltage	2111AL-4	V_{OH}	+2.4			V	I_{OH} = −150 μA
	2111AL 2111AL-2		+2.4			V	I_{OH} = −200 μA
Output Low Voltage		V_{OL}			+0.4	V	I_{OL} = +2.1 mA
Input Leakage Current High		I_{LIH}			+10	μA	$V_I = V_{CC}$
Input Leakage Current Low		I_{LIL}			−10	μA	V_I = 0V
Output Leakage Current High		I_{LOH}			+5	μA	V_O = +2.4V to V_{CC} $\overline{CE}$ = +2.0V
Output Leakage Current Low		I_{LOL}			−10	μA	V_O = +0.4V $\overline{CE}$ = +2.0V
Power Supply Current	2111AL-4	I_{CC1}			50	mA	V_I = +5.25V
	2111AL 2111AL-2				55	mA	I_O = 0 mA T_a = +25°C
Power Supply Current	2111AL-4	I_{CC2}			60	mA	V_I = +5.25V
	2111AL 2111AL-2				65	mA	I_O = 0 mA T_a = −10 to +70°C

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AC CHARACTERISTICS

READ CYCLE

T_a = −10°C to +70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS									UNIT
		2111AL-4			2111AL			2111AL-2			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Read Cycle Time	t_{RC}	450			350			250			ns
Access Time	t_A			450			350			250	ns
Chip Enable to Output	t_{CO}			310			240			180	ns
Output Disable to Output	t_{OD}			250			180			130	ns
Data Output to High Z State	t_{DF} ①	0		200	0		150	0		130	ns
Previous Read Data Valid After Change of Address	t_{OH}	40			40			40			ns

Note: ① t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, $\overline{CE}_2$, or OD, whichever occurs first.

WRITE CYCLE

T_a = −10°C to +70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS									UNIT
		2111AL-4			2111AL			2111AL-2			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Write Cycle Time	t_{WC}	270			220			170			ns
Write Delay	t_{AW}	20			20			20			ns
Chip Enable to Write	t_{CW}	250			200			150			ns
Data Setup Time	t_{DW}	250			200			150			ns
Data Hold Time	t_{DH}	0			0			0			ns
Write Pulse Width	t_{WP}	250			200			150			ns
Write Recovery	t_{WR}	0			0			0			ns
Output Disable Setup	t_{DS}	20			20			20			ns

Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

AC CONDITIONS OF TEST

Input Pulse Levels	+0.8V to +2.0V
Input Pulse Rise and Fall Times	20 ns
Timing Measurement Reference Level	1.5V
Output Load	1 TTL + 100 pF

STANDBY CHARACTERISTICS

T_a = −10°C to +70°C

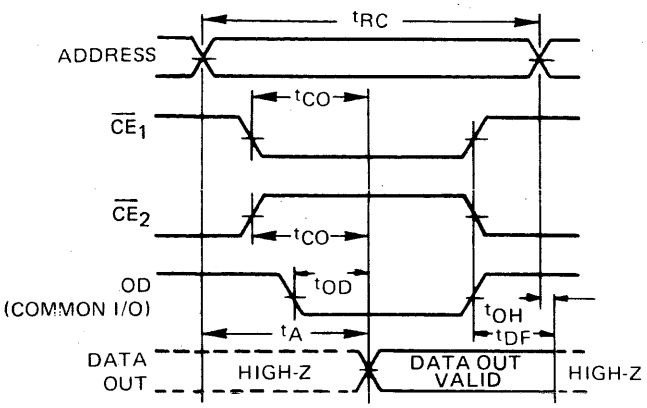
PARAMETER		SYMBOL	LIMITS			UNIT	TEST CONDITIONS
			MIN	TYP ①	MAX		
V_{CC} in Standby		V_{PD}	1.5			V	
$\overline{CE}_1$ Bias in Standby		V_{CES}	2.0			V	2.0V ≤ V_{PD} ≤ 5.25V
			V_{PD}			V	1.5V ≤ V_{PD} < 2.0V
Standby Current Drain	2111AL-4	I_{PD_1}			36	mA	All Inputs = V_{PD_1} = 1.5V
	2111AL/AL-2				38		
Standby Current Drain	2111AL-4	I_{PD_2}			45	mA	All Inputs = V_{PD_2} = 2.0V
	2111AL/AL-2				48		
Chip Deselect to Standby Time		t_{CP}	0			ns	
Standby Recovery		t_R	t_{RC} ②			ns	

Notes: ① Typical values are for T_a = 25°C and nominal supply voltage
② t_R = t_{RC} (Read Cycle Time)

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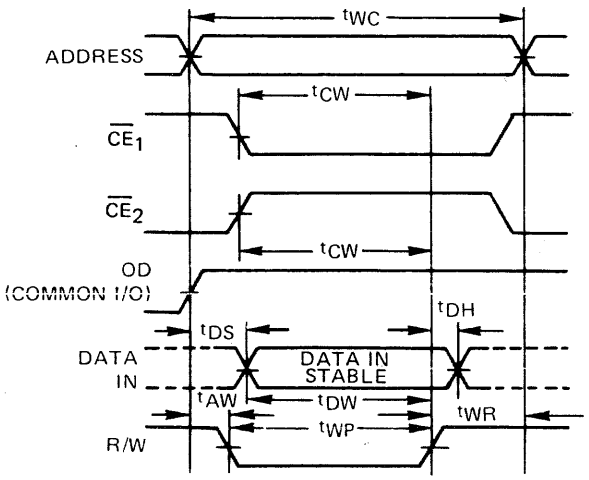
TIMING WAVEFORMS

READ CYCLE



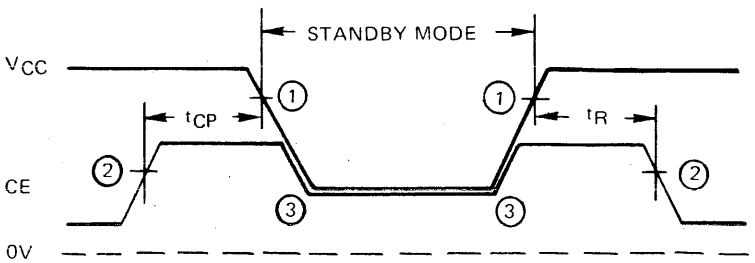
Notes: ① OD should be tied low for separate I/O operation.
② R/W is high for read operation.

WRITE CYCLE



Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

STANDBY WAVEFORMS



Notes: ① 4.75V
② 2.0V
③ 1.5V
④ If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max) and 2.0V, then $\overline{CE}$ must be held at 2.0V Min (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD} Min), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the two. $\overline{CE}$ may be either of $\overline{CE}_1$ or $\overline{CE}_2$.

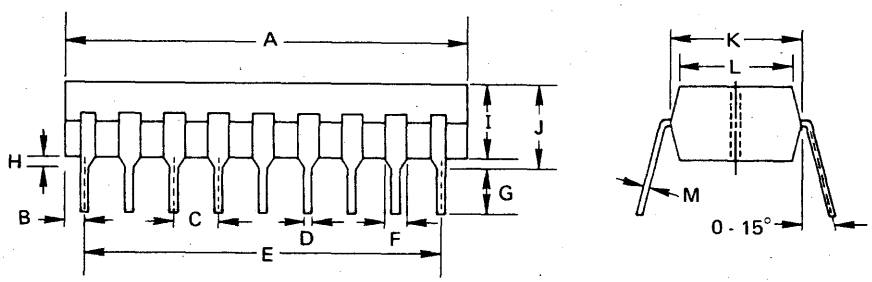
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CAPACITANCE

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			8	pf	V_I = 0V
Output Capacitance	C_{OUT}			12	pf	V_O = 0V

PACKAGE OUTLINE μPD2111ALC



ITEM	MILLIMETERS	INCHES
A	22.5 MAX.	0.89
B	1.09	0.04
C	2.54	0.10
D	0.50 ± 0.10	0.02
E	20.32	0.80
F	1.2 MIN.	0.05
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

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1024 BIT (256x4) STATIC CMOS RAM

DESCRIPTION

The μPD5101-E is a very low power 1024 bit (256 words by 4 bits) static CMOS Random Access Memory. It meets the low power requirements of battery operated systems and can be used to ensure non-volatility of data in systems using battery backup power.

All inputs and outputs of the μPD5101-E are TTL compatible. Two chip enables ($\overline{CE}_1$, CE_2) are provided, with the device being selected when $\overline{CE}_1$ is low and CE_2 is high. The μPD5101-E can be placed in standby mode, drawing 15 μA maximum, by driving $\overline{CE}_1$ high and inhibiting all address and control line transitions. The standby mode can also be selected unconditionally by driving CE_2 low.

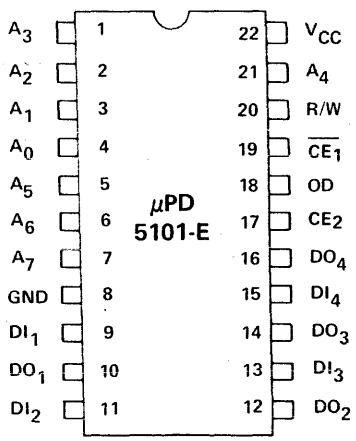
The μPD5101-E has separate input and output lines. It can be used in common I/O bus systems through the use of the OD (Output Disable) pin and OR-tying the input/output pins. Output data is the same polarity as input data and is non-destructively read out. Read mode is selected by placing a high on the R/W pin. The μPD5101-E is guaranteed to retain data with the power supply voltage as low as 2.0 volts. Normal operation requires a single +5 volt supply.

The μPD5101-E is fabricated using NEC's complementary MOS (CMOS) process and is packaged in a 22-pin dual-in-line package.

FEATURES

- Directly TTL Compatible – All Inputs and Outputs
- Three-State Output
- Access Time – 800 ns
- Single +5V Power Supply
- CE_2 Controls Unconditional Standby Mode

PIN CONFIGURATION

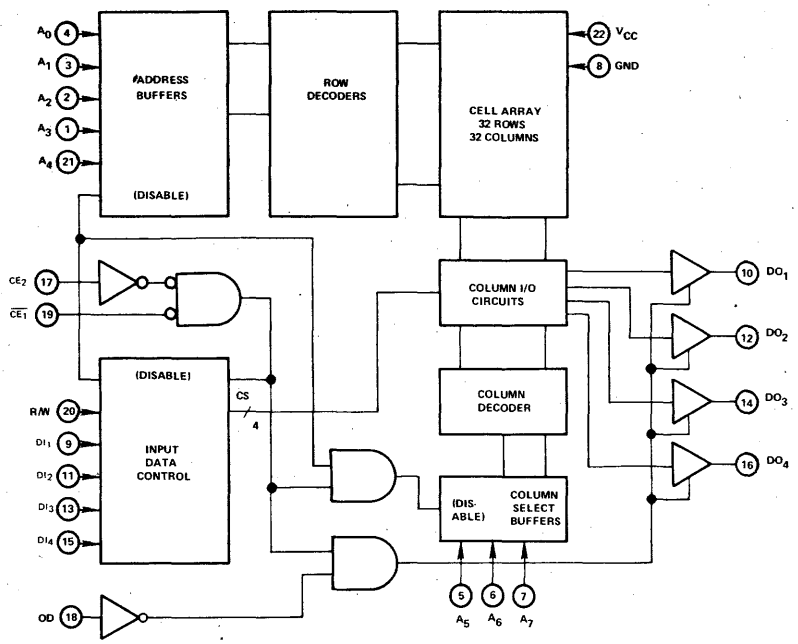


PIN NAMES

$DI_1 - DI_4$	Data Input
$A_0 - A_7$	Address Inputs
R/W	Read/Write Input
$\overline{CE}_1$, CE_2	Chip Enables
OD	Output Disable
$DO_1 - DO_4$	Data Output
V_{CC}	Power (+5V)

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -40°C to +125°C
Voltage On Any Pin With Respect to Ground . . . . . -0.3 Volts to V_{CC} +0.3 Volts
Power Supply Voltage . . . . . -0.3 to +7.0 Volts

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = +5V ± 5%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Leakage	I_{LIH} ②			1	μA	$V_{IN} = V_{CC}$
Input Low Leakage	I_{LIL} ②			-1	μA	V_{IN} = 0V
Output High Leakage	I_{LOH} ②			1	μA	$\overline{CE_1}$ = 2.2V, $V_{OUT} = V_{CC}$
Output Low Leakage	I_{LOL} ②			-1	μA	$\overline{CE_1}$ = 2.2V, V_{OUT} = 0.0V
Operating Current	I_{CC1}		9	22	mA	$V_{IN} = V_{CC}$ Except $\overline{CE_1}$ ≤0.01V, Outputs Open
Operating Current	I_{CC2}		13	27	mA	V_{IN} = 2.2V Except $\overline{CE_1}$ ≤0.65V, Outputs Open
Standby Current	I_{CCL} ②			15	μA	V_{IN} = 0 to 5.25V $CE_2 \leq$ 0.2V
Input Low Voltage	V_{IL}	-0.3		0.65	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = -1.0 mA
Output High Voltage	V_{OH2}	3.5			V	I_{OH} = -100 μA

Notes: ① Typical values at T_a = 25°C and nominal supply voltage.
② Current through all inputs and outputs included in I_{CCL}.

CAPACITANCE

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance (All Input Pins)	C_{IN}		4	8	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		12	20	pF	V_{OUT} = 0V

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AC CHARACTERISTICS

READ CYCLE

T_a = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Read Cycle	t_{RC}	800			ns	Input pulse amplitude: 0.65 to 2.2 Volts
Access Time	t_A		415	800	ns	Input rise and fall times: 20 ns
Chip Enable ($\overline{CE_1}$) to Output	t_{CO1}		400	800	ns	Timing measurement reference level: 1.5 Volt
Chip Enable (CE_2) to Output	t_{CO2}		440	850	ns	Output load: I_{TTL}
Output Disable to Output	t_{OD}		145	350	ns	Gate and C_L = 100 pF
Data Output to High Z State	t_{DF}	0		200	ns	
Previous Read Data Valid with Respect to Address Change	t_{OH1}	0	100		ns	
Previous Read Data Valid with Respect to Chip Enable	t_{OH2}	0	250		ns	

WRITE CYCLE

T_a = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Write Cycle	t_{WC}	800			ns	Input pulse amplitude: 0.65 to 2.2 Volts
Write Delay	t_{AW}	200	-120		ns	Input rise and fall times: 20 ns
Chip Enable ($\overline{CE_1}$) to Write	t_{CW1}	600	275		ns	Timing measurement reference level: 1.5 Volt
Chip Enable (CE_2) to Write	t_{CW2}	600	295		ns	Output load: I_{TTL}
Data Setup	t_{DW}	400			ns	Gate and C_L = 100 pF
Data Hold	t_{DH}	100	-160		ns	
Write Pulse	t_{WP}	400	190		ns	
Write Recovery	t_{WR}	50	-130		ns	
Output Disable Setup	t_{DS}	200			ns	

LOW V_{CC} DATA RETENTION CHARACTERISTICS

T_a = 0°C to 70°C

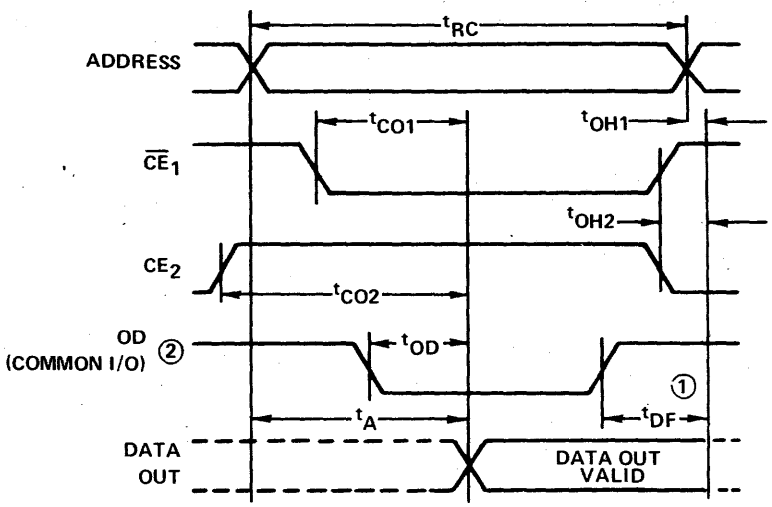
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
V_{CC} for Data Retention	V_{CCDR}	+2.0			V	$CE_2 \leq +0.2V$
Data Retention Current	I_{CCDR}			+10	μA	V_{CCDR} = +2.0 to +3.0V; $CE_2 \leq +0.2V$
Chip Deselect Setup Time	t_{CDR}	0			ns	
Chip Deselect Hold Time	t_R	t_{RC} ①			ns	

Note: ① t_{RC} = Read Cycle Time

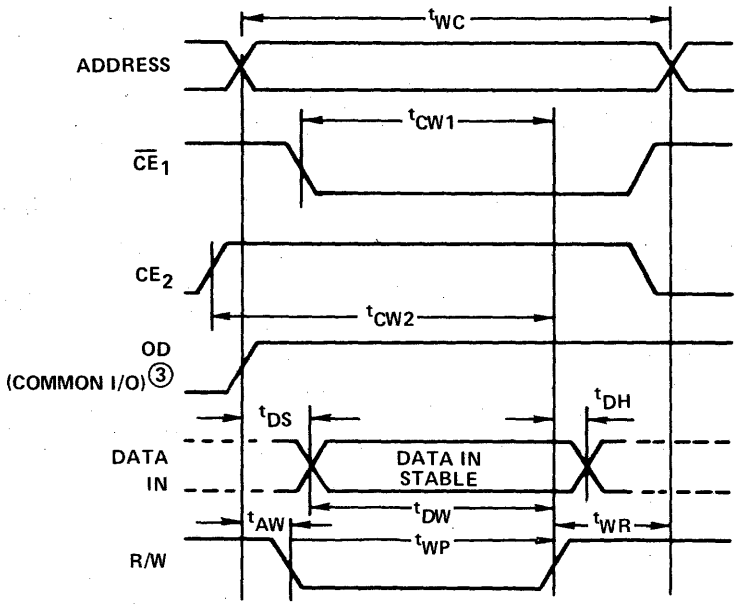
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TIMING WAVEFORMS

READ CYCLE

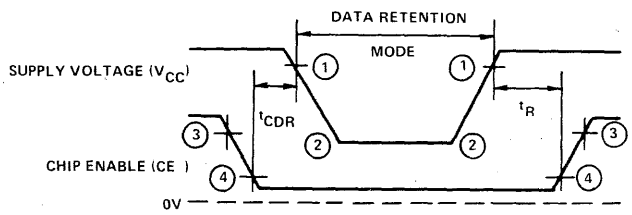


WRITE CYCLE



Notes: ① Typical values are for $T_a = 25°C$ and nominal supply voltage.
② OD may be tied low for separate I/O operation.
③ During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

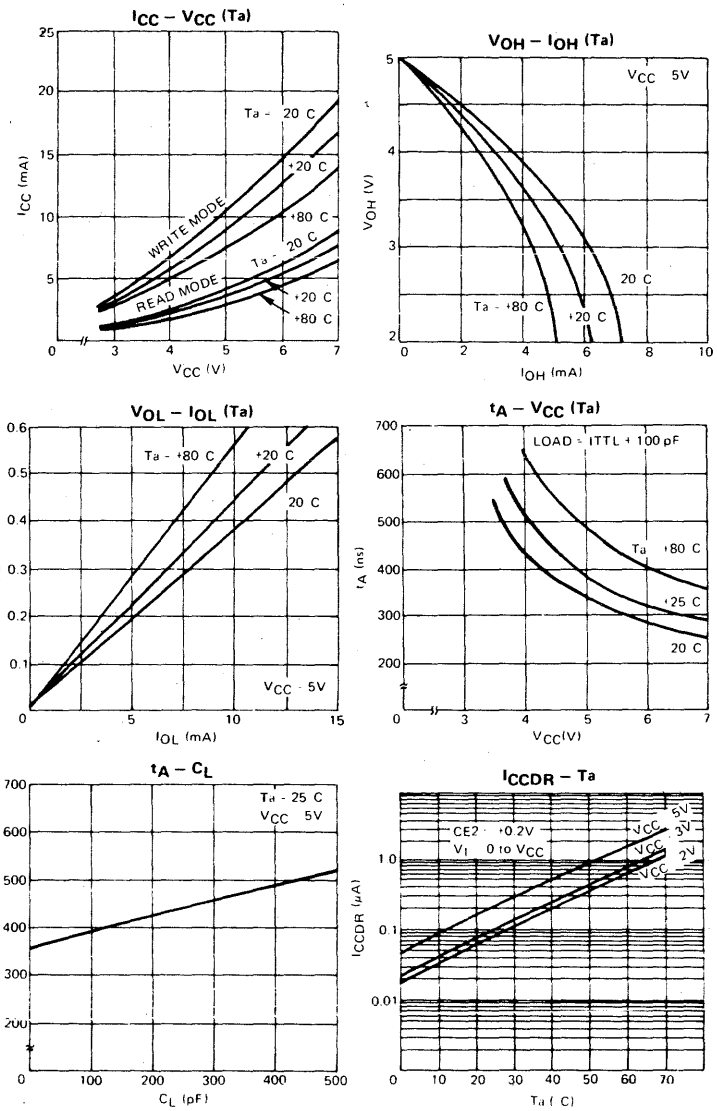
LOW V_{CC} DATA RETENTION



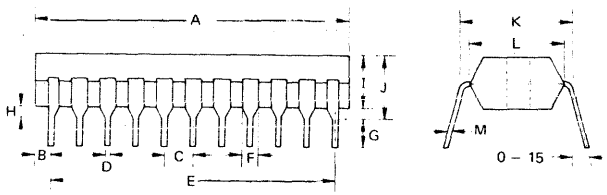
Notes: ① 4.75V
② V_{CCDR}
③ V_{IH}
④ 0.2V

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TYPICAL OPERATING CHARACTERISTICS



PACKAGE OUTLINE μPD5101C-E



ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50 0.10	0.02 0.004
E	25.4	1.0
F	1.40	0.055
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	0.25 +0.10 0.05	0.01 +0.004 0.002

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NEC Microcomputers

1024 BIT (256x4) STATIC CMOS RAM

DESCRIPTION

The μPD5101L and μPD5101L-1 are very low power 1024 bit (256 words by 4 bits) static CMOS Random Access Memories. They meet the low power requirements of battery operated systems and can be used to ensure non-volatility of data in systems using battery backup power.

All inputs and outputs of the μPD5101L and μPD5101L-1 are TTL compatible. Two chip enables ($\overline{CE}_1$, CE_2) are provided, with the devices being selected when $\overline{CE}_1$ is low and CE_2 is high. The devices can be placed in standby mode, drawing 10 μA maximum, by driving $\overline{CE}_1$ high and inhibiting all address and control line transitions. The standby mode can also be selected unconditionally by driving CE_2 low.

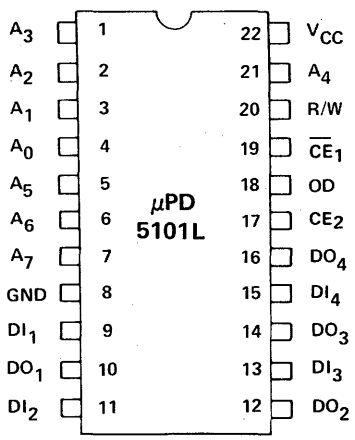
The μPD5101L and μPD5101L-1 have separate input and output lines. They can be used in common I/O bus systems through the use of the OD (Output Disable) pin and OR-tying the input/output pins. Output data is the same polarity as input data and is nondestructively read out. Read mode is selected by placing a high on the R/W pin. Either device is guaranteed to retain data with the power supply voltage as low as 2.0 volts. Normal operation requires a single +5 volt supply.

The μPD5101L and μPD5101L-1 are fabricated using NEC's silicon gate complementary MOS (CMOS) process.

FEATURES

- Directly TTL Compatible – All Inputs and Outputs
- Three-State Output
- Access Time – 650 ns (μPD5101L); 450 ns (μPD5101L-1)
- Single +5V Power Supply
- CE_2 Controls Unconditional Standby Mode
- Available in a 22-pin Dual-in-Line Package

PIN CONFIGURATION

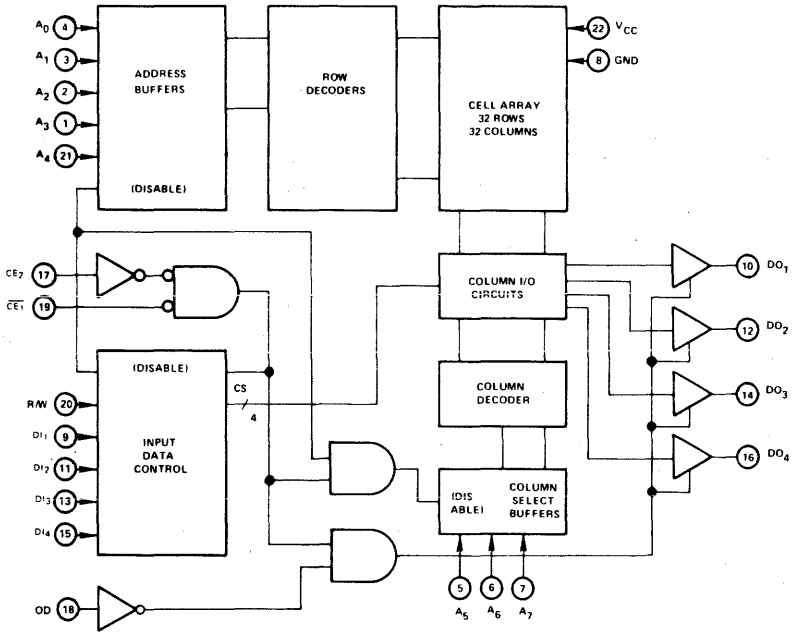


PIN NAMES

$DI_1 - DI_4$	Data Input
$A_0 - A_7$	Address Inputs
R/W	Read/Write Input
$\overline{CE}_1$, CE_2	Chip Enables
OD	Output Disable
$DO_1 - DO_4$	Data Output
V_{CC}	Power (+5V)

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -40°C to +125°C
Voltage On Any Pin With Respect to Ground . . . . . -0.3 Volts to V_{CC} +0.3 Volts
Power Supply Voltage . . . . . -0.3 to +7.0 Volts

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = +5V ± 5%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP (1)	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Leakage	I_{LIH} (2)			1	μA	$V_{IN} = V_{CC}$
Input Low Leakage	I_{LIL} (2)			-1	μA	V_{IN} = 0V
Output High Leakage	I_{LOH} (2)			1	μA	$\overline{CE}_1$ = 2.2V, $V_{OUT} = V_{CC}$
Output Low Leakage	I_{LOL} (2)			-1	μA	$\overline{CE}_1$ = 2.2V, V_{OUT} = 0.0V
Operating Current	I_{CC1}			22	mA	$V_{IN} = V_{CC}$ Except $\overline{CE}_1$ ≤0.65V, Outputs Open
Operating Current	I_{CC2}			27	mA	V_{IN} = 2.2V Except $\overline{CE}_1$ ≤0.65V, Outputs Open
Standby Current	I_{CCL} (2)			10	μA	V_{IN} = 0 to 5.25V $CE_2 \leq 0.2V$
Input Low Voltage	V_{IL}	-0.3		0.65	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = -1.0 mA
Output High Voltage	V_{OH2}	3.5			V	I_{OH} = -100 μA

Notes: (1) Typical values at T_a = 25°C and nominal supply voltage.
(2) Current through all inputs and outputs included in I_{CCL}.

CAPACITANCE

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance (All Input Pins)	C_{IN}		4	8	pF	V_{IN} 0V
Output Capacitance	C_{OUT}		8	12	pF	V_{OUT} 0V

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AC CHARACTERISTICS

READ CYCLE

T_a = 0°C to 70°C; V_{CC} = 5V±5%, unless otherwise specified

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		5101L			5101L-1				
		MIN	TYP	MAX	MIN	TYP	MAX		
Read Cycle	t_{RC}	650			450			ns	Input pulse amplitude: 0.65 to 2.2 Volts
Access Time	t_A			650			450	ns	Input rise and fall times: 20 ns
Chip Enable ($\overline{CE_1}$) to Output	t_{CO1}			600			400	ns	Timing measurement reference level: 1.5 Volt
Chip Enable (CE_2) to Output	t_{CO2}			700			500	ns	Output load: I_{TTL}
Output Disable to Output	t_{OD}			350			250	ns	Gate and C_L = 100 pF
Data Output to High Z State	t_{DF}	0		150	0		130	ns	
Previous Read Data Valid with Respect to Address Change	t_{OH1}	0			0			ns	
Previous Read Data Valid with Respect to Chip Enable	t_{OH2}	0			0			ns	

WRITE CYCLE

T_a = 0°C to 70°C; V_{CC} = 5V±5%, unless otherwise specified

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		5101L			5101L-1				
		MIN	TYP	MAX	MIN	TYP	MAX		
Write Cycle	t_{WC}	650			450			ns	Input pulse amplitude: 0.65 to 2.2 Volts
Write Delay	t_{AW}	150			130			ns	Input rise and fall times: 20 ns
Chip Enable ($\overline{CE_1}$) to Write	t_{CW1}	550			350			ns	Timing measurement reference level: 1.5 Volt
Chip Enable (CE_2) to Write	t_{CW2}	550			350			ns	Output load: I_{TTL}
Data Setup	t_{DW}	400			250			ns	Gate and C_L = 100 pF
Data Hold	t_{DH}	100			50			ns	
Write Pulse	t_{WP}	400			250			ns	
Write Recovery	t_{WR}	50			50			ns	
Output Disable Setup	t_{DS}	150			130				

LOW V_{CC} DATA RETENTION CHARACTERISTICS

T_a = 0°C to 70°C

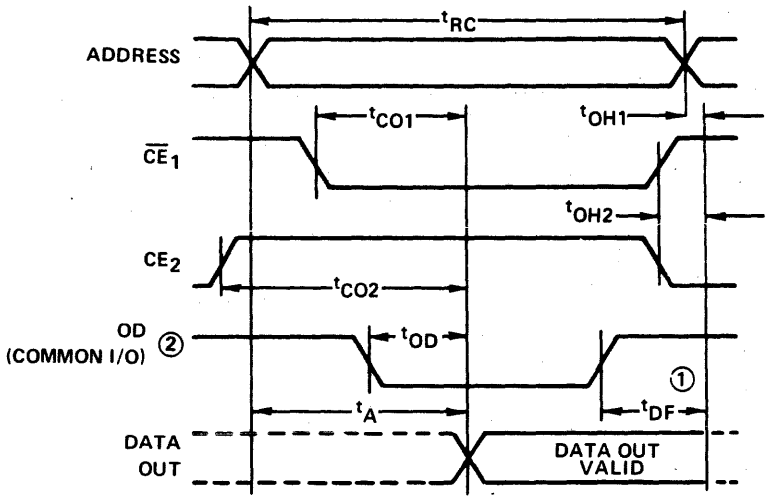
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
V_{CC} for Data Retention	V_{CCDR}	+2.0			V	$CE_2 \leq +0.2V$
Data Retention Current	I_{CCDR}			+10	μA	V_{CCDR} = +2.0V $CE_2 \leq +0.2V$
Chip Deselect Setup Time	t_{CDR}	0			ns	
Chip Deselect Hold Time	t_R	t_{RC} ①			ns	

Note: ① t_{RC} = Read Cycle Time

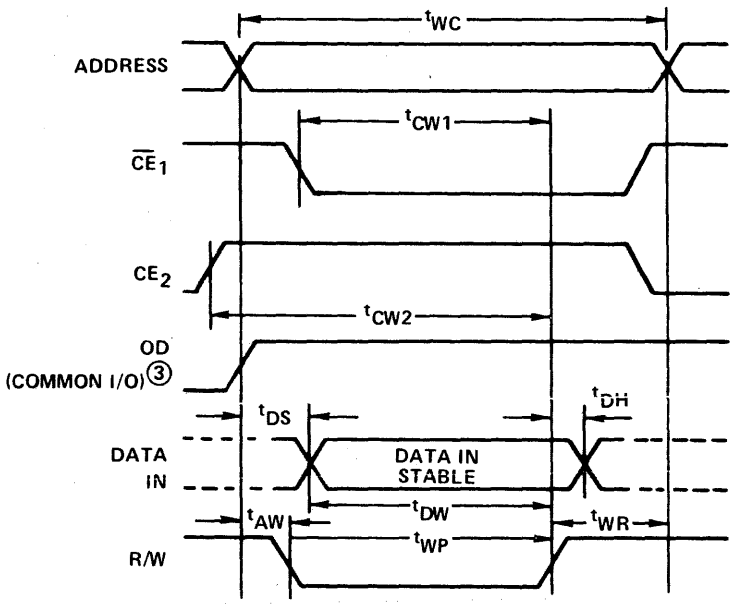
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TIMING WAVEFORMS

READ CYCLE

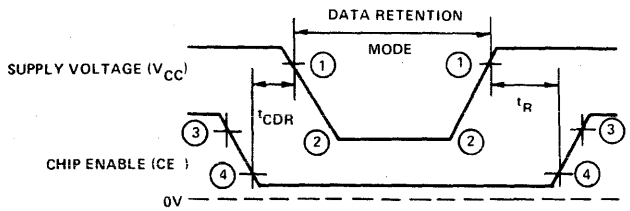


WRITE CYCLE



Notes: ① Typical values are for T_a = 25°C and nominal supply voltage.
② OD may be tied low for separate I/O operation.
③ During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

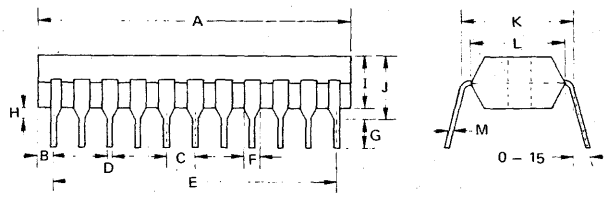
LOW V_{CC} DATA RETENTION



Notes: ① 4.75V
② V_{CCDR}
③ V_{IH}
④ 0.2V

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PACKAGE OUTLINE
μPD5101LC



ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50 ± 0.10	0.02 ± 0.004
E	25.4	1.0
F	1.40	0.055
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

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FULLY DECODED 2048 BIT ELECTRICALLY ERASABLE AND PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

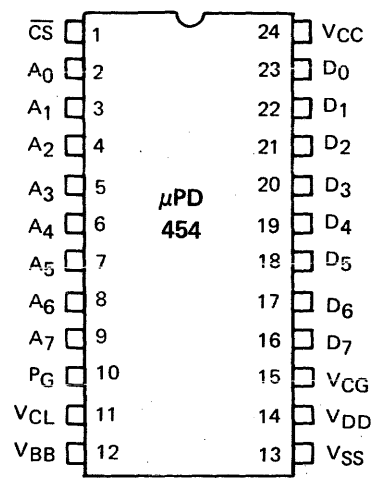
The μPD454 EEPROM, a 256 Words x 8 Bits Read Only Memory, is designed for rapid development of microcomputer systems. The ability to electrically program, erase, and reprogram the μPD454 provides a fast and convenient means of debugging both hardware and software designs.

The μPD454 is pin for pin compatible with NEC's μPD464 mask programmed ROM.

FEATURES

- Electrically Erasable and Programmable
- Fully Decoded, 256 Words x 8 Bits Organization
- Access Time 800 ns Max
- Low Power: 245 mW (Typ.) in Read Operation
  670 mW (Typ.) in Programming Operation
- Fast Programming and Erasure Speed
- Low Power for Programming and Erasure
- Static, No Clock Required
- Input/Output TTL Compatible for Read and Programming Operation
- Three-State Output, OR-Tie Capability
- N-Channel MOS Fabrication
- Two Power Supplies, +12V and +5V for Read Operation
- 24 Pin Ceramic DIP

PIN CONFIGURATION

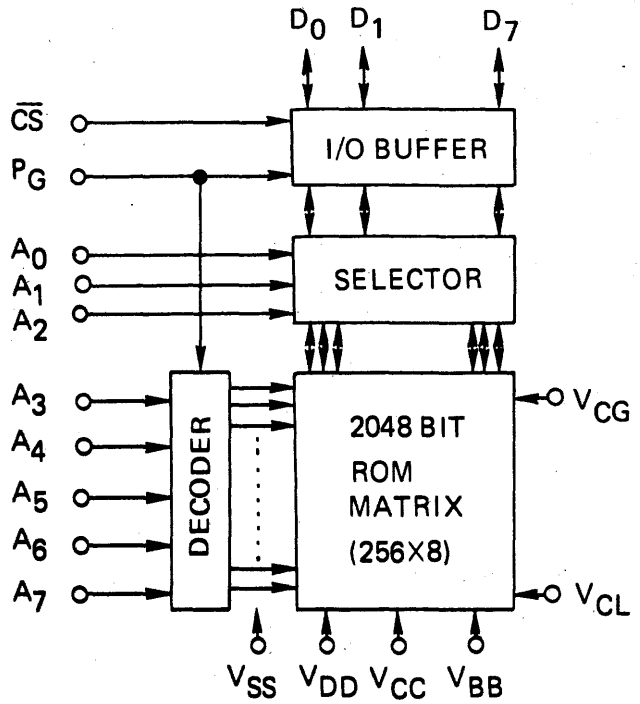


Rev/1

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NEC Microcomputers

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
All Output Voltages	−0.3 to +11 Volts①
All Input Voltages	−0.3 to +11 Volts①
Supply Voltage V_{DD}	−0.3 to +15 Volts①
Supply Voltage V_{CC}	−0.3 to +7 Volts①
Supply Voltage V_{BB}	V_{SS} to −7 Volts②
Supply Voltage P_G	−0.3 to +30 Volts①②
Supply Voltage V_{CL}	−0.3 to +43 Volts①②
Supply Voltage V_{CG}	−44 to +30 Volts①②

Notes: ① Relative to V_{BB}.
② Data in the memory cell is not guaranteed to be preserved.
Specifies ratings which will not cause permanent damage to the device.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			10	pF	f = 1 MHz
Output Capacitance	C_{OUT}			15	pF	f = 1 MHz

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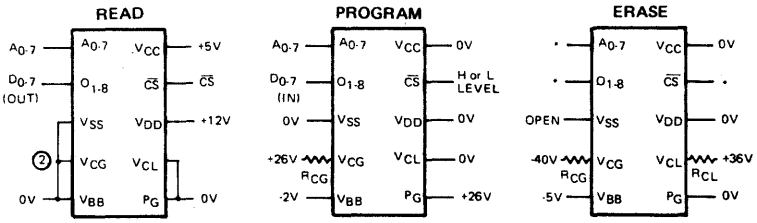
PIN DEFINITION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1	$\overline{CS}$	CHIP SELECT	Chip selection, active low
2-9	A_0–A_7	ADDRESS BUS	Memory address
10	P_G	+26V (TYP) Power Supply	Power supply for programming operation
11	V_{CL}	+36V (TYP) Power Supply	Power supply for erasing operations
12	V_{BB}	Substrate Power Supply	Power supply
13	V_{SS}	GROUND	Ground Reference
14	V_{DD}	+12V Power Supply	Power supply for read operations
15	V_{CG}	−44 to +30 Power Supply	Power supply for control of programming and erasure operations
16-23	D_7–D_0	Data Input/Output	Data In for programming operations. Data Output for read operations.
24	V_{CC}	+5V Power Supply	Power supply for read operations

SUPPLY VOLTAGES

Typical values. Unit – Voltage.

MODE \ PIN	V_{DD}(14)	V_{CC}(24)	V_{BB}(14)	P_G(10)	V_{CL}(11)	V_{CG}(15)	V_{SS}(13)
Read	+12	+5	0	0	0	0	0
Program	0	0	-2	+26	0	+26	0
Erase	0	0	-5	0	+36	-40	Open
Verify "0"	+12	+5		0	0	+3	0
Verify "1"	+12	+5		0	0	-3	0

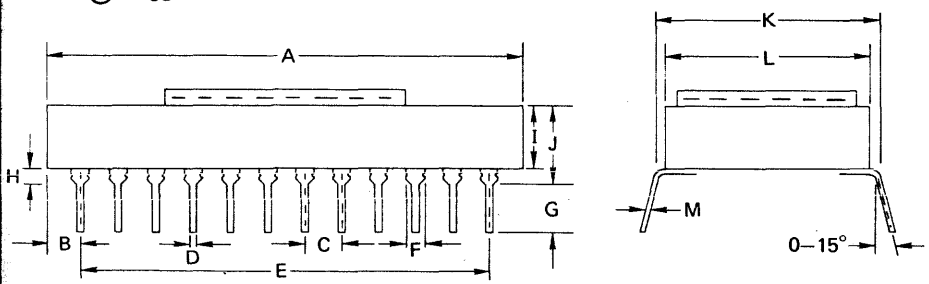


Notes: * = Either High or Low Level, or Open.

① R_{CG} and R_{CL} are Protection Resistors
R_{CG} = 10 kΩ ± 10%, 1/4W
R_{CL} = 200Ω ± 10%, 10W

② R_{CG} may be left connected in Read Mode

PACKAGE OUTLINE μPD454D



ITEM	MILLIMETERS	INCHES
A	32.5 MAX	1.28 MAX
B	2.28	0.09
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.20 MIN	0.047 MIN
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.165 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

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READ OPERATION

DC CHARACTERISTICS

$T_a = -10$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$,
$V_{BB} = P_G = V_{CL} = V_{CG} = V_{SS} = 0V$

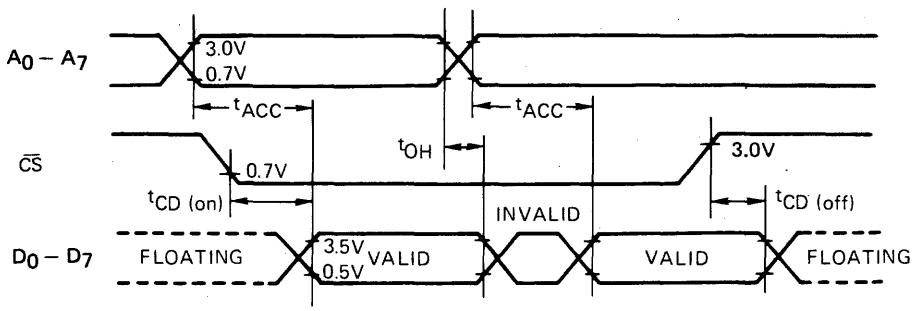
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	3.0		V_{CC}	V	
Input Low Voltage	V_{IL}	0		0.7	V	
Output High Voltage	V_{OH}	3.5			V	$I_{OH} = -2.0$ mA
Output Low Voltage	V_{OL}			0.5	V	$I_{OL} = 1.7$ mA
Input Leakage Current High	I_{LIH}			+10	μA	$V_I = +3.0V$
Input Leakage Current Low	I_{LIL}			-10	μA	$V_I = +0.7V$
Output Leakage Current High	I_{LOH}			+100	μA	$\overline{CS}$ = "1" $V_O = 3.5V$
Output Leakage Current Low	I_{LOL}			-10	μA	$\overline{CS}$ = "1" $V_O = 0.4V$
V_{DD} Supply Current	I_{DD}		20		mA	
V_{CC} Supply Current	I_{CC}			0.3	mA	with no load

AC CHARACTERISTICS

$T_a = -10$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$,
$V_{BB} = P_G = V_{CL} = V_{CG} = V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Access Time	t_{ACC}			800	ns	1 TTL + 100 pF
$\overline{CS}$ to Output On Delay	$t_{CD(on)}$			200	ns	
$\overline{CS}$ to Output Off Delay	$t_{CD(off)}$	0		200	ns	
Output Hold Time	t_{OH}	0			ns	

TIMING WAVEFORMS



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PROGRAMMING OPERATION

Before the μPD454 is programmed the device must be erased. All bit locations must contain a zero (0). The μPD454 programming procedure is word by word one word at a time.

DC CHARACTERISTICS

T_a = 25°C ± 2°C, V_{DD} = V_{CC} = V_{SS} = V_{CL} = 0V. $\overline{CS}$ = Either HIGH or LOW level.

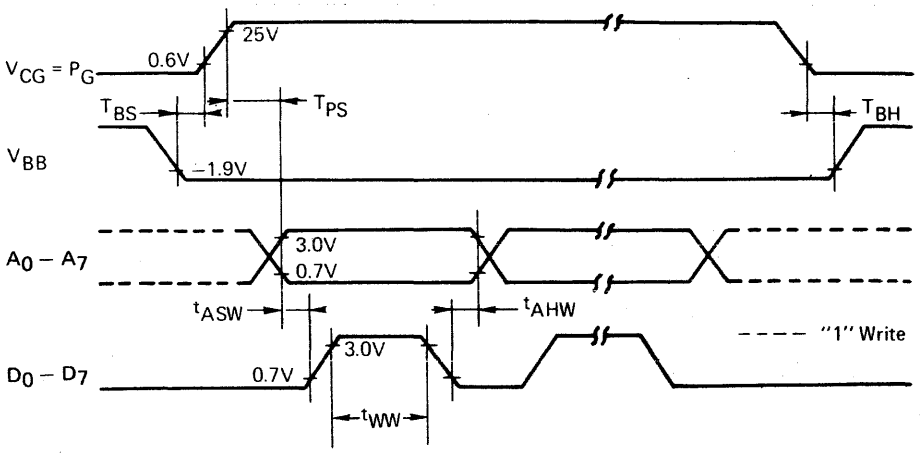
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	3.0		V_{CC}	V	
Input Low Voltage	V_{IL}	0		0.7	V	
Supply Voltage	V_{BB}	-1.9	-2.0	-2.1	V	
Supply Voltage	P_G	25	26	27	V	
Supply Voltage	V_{CG}	25	26	27	V	through R_{CG}
Supply Current (V_{BB})	I_{BB}		-8		mA	
Supply Current (P_G)	I_G		+25		mA	
Supply Current (V_{CG})	I_{CG}			+10	μA	

AC CHARACTERISTICS

T_a = 25°C ± 2°C, V_{DD} = V_{CC} = V_{SS} = V_{CL} = 0V. $\overline{CS}$ = Either HIGH or LOW level.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Address Setup Time	t_{ASW}	10			μs	
Address Hold Time	t_{AHW}	10			μs	
Write Data Width	t_{WW}	20		100	ms	per one word
V_{BB} Setup Time	T_{BS}	1.0			μs	
V_{BB} Hold Time	T_{BH}	1.0			μs	
P_G, V_{CG} Setup Time	T_{PS}	10			μs	

TIMING WAVEFORMS



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ERASURE OPERATION*

DC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = P_G = 0V$, $V_{SS} = 0V$
$\overline{CS}$, $A_0 - A_7$ and $D_0 - D_7$ = Either HIGH or LOW level, or non-connected

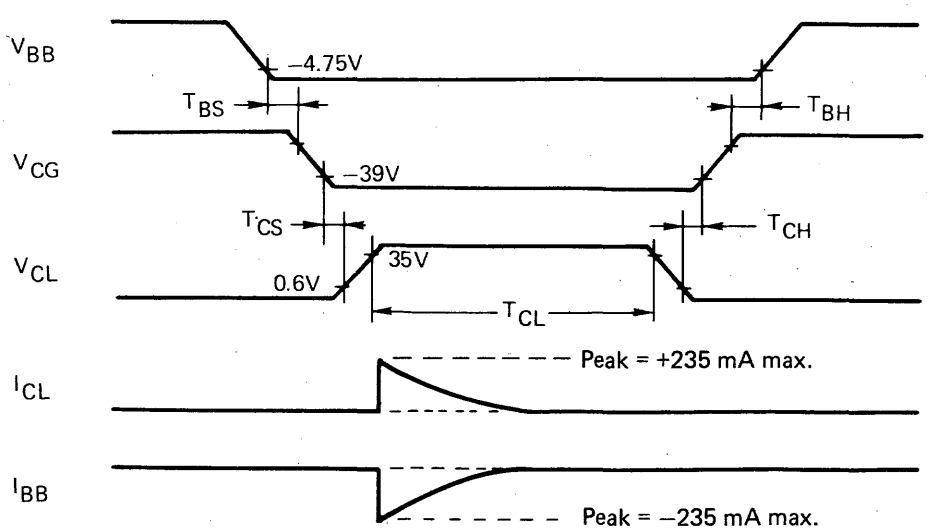
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Supply Voltage	V_{BB}	-4.75	-5.0	-5.25	V	
Supply Voltage	V_{CL}	+35	+36	+37	V	through R_{CL}
Supply Voltage	V_{CG}	-39	-40	-41	V	through R_{CG}
Supply Current (V_{BB})	I_{BB}			-235	mA	Initial peak current. See timing chart.
Supply Current (V_{CL})	I_{CL}			-235	mA	
Supply Current (V_{CG})	I_{CG}			-20	μA	

AC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = P_G = 0V$, $V_{SS} = 0V$
$\overline{CS}$, $A_0 - A_7$ and $D_0 - D_7$ = Either HIGH or LOW level, or non-connected

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Clear Time	T_{CL}			60	sec	
V_{BB} Setup Time	T_{BS}	0			μs	
V_{BB} Hold Time	T_{BH}	0			μs	
V_{CG} Setup Time	T_{CS}	1.0			μs	
V_{CG} Hold Time	T_{CH}	1.0			μs	

TIMING WAVEFORMS



Note: The supply currents I_{BB} and I_{CL} diminish to almost zero within T_{CL}.

*Erasure operation clears all 2048 bits to Logic "0" simultaneously.

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FULLY DECODED 8192 BIT ELECTRICALLY ERASABLE AND PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

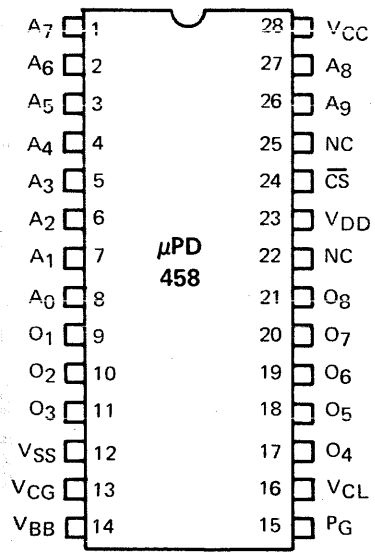
The μPD458 is an Electrically Erasable and Reprogrammable Read Only Memory (EEPROM), organized as 1024 words by 8 bits.

The μPD458 is fabricated with N-channel MOS technology and is packaged in a 28 pin ceramic DIP.

FEATURES

- Electrically Erasable and Reprogrammable
- Fully Decoded, 1024 Words x 8 Bits Organization
- Access Time – 450 ns max.
- Fast Programming and Erasure Speed
- Simple Worst-case Verification of Programmed Data and Erasure
- Static, No Clock Required
- Input/Output TTL Compatible for Read and Programming Operation
- Three-State Output, OR-Tie Capability
- N-Channel MOS
- Two Power Supplies, +12V and +5V for Read
- 28 Pin Ceramic DIP

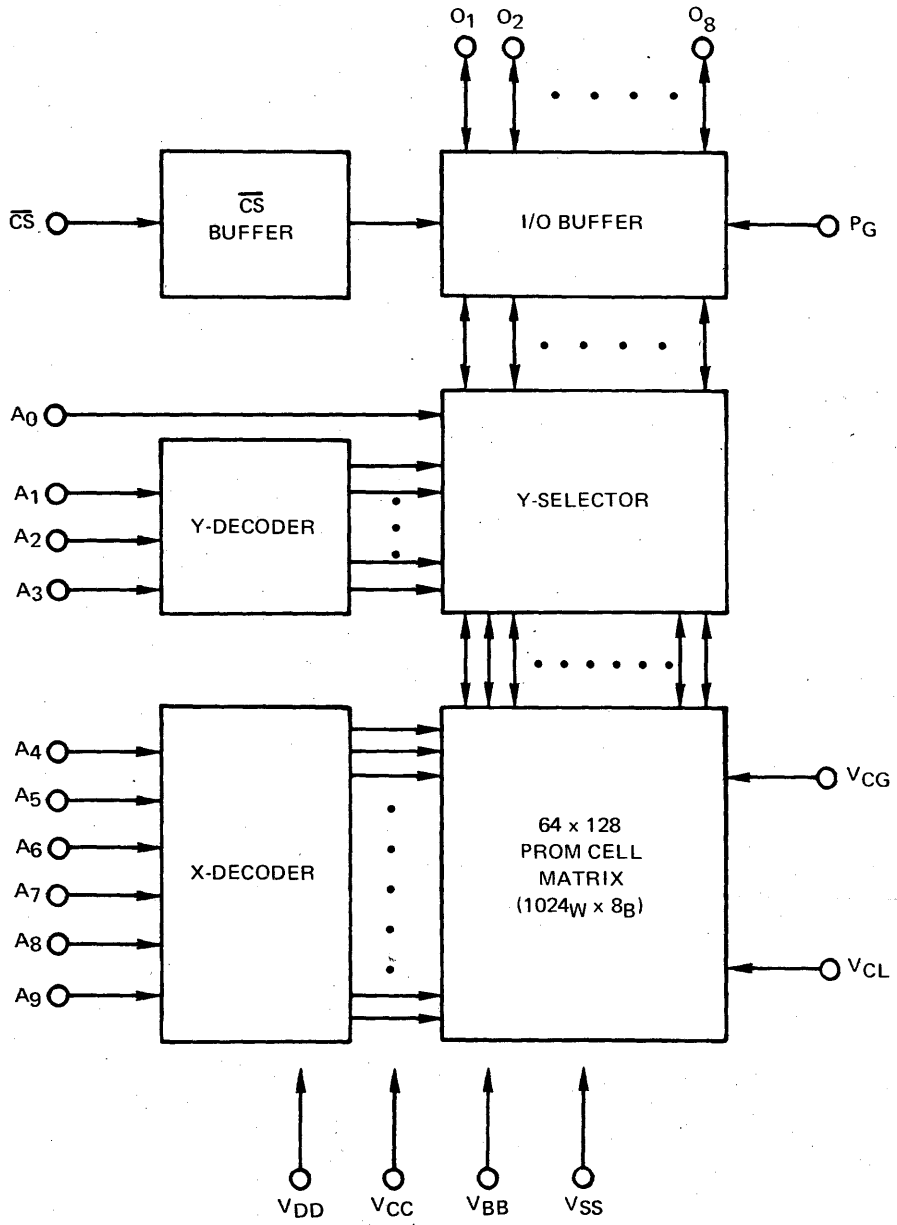
PIN CONFIGURATION



NC: No Connection

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
All Output Voltages	−0.3 to +11 Volts①
All Input Voltages	−0.3 to +11 Volts①
Supply Voltage V_{DD}	−0.3 to +15 Volts①
Supply Voltage V_{CC}	−0.3 to +7 Volts①
Supply Voltage V_{BB}	V_{SS} to −7 Volts②
Supply Voltage P_G	−0.3 to +30 Volts①②
Supply Voltage V_{CL}	−0.3 to +43 Volts①②
Supply Voltage V_{CG}	−44 to +30 Volts①②

Notes: ① Relative to V_{BB}.
② Data in the memory cell is not guaranteed to be preserved.
Specifies ratings which will not cause permanent damage to the device.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

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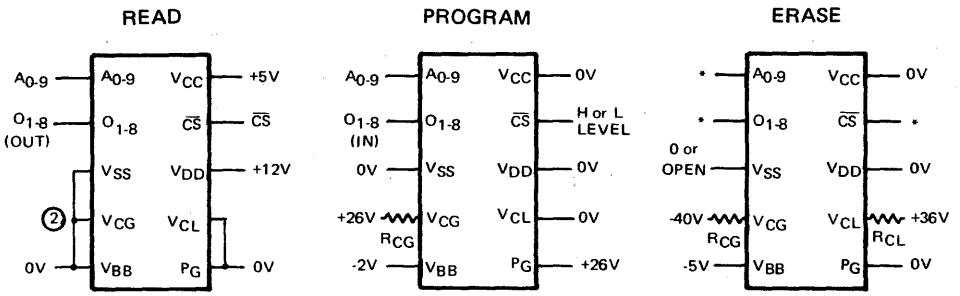
CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			10	pF	f = 1 MHz
Output Capacitance	C_{OUT}			15	pF	f = 1 MHz

SUPPLY VOLTAGES

Typical values. Unit — Voltage.

MODE \ PIN	V_{DD}(23)	V_{CC}(28)	V_{BB}(14)	P_G(15)	V_{CL}(16)	V_{CG}(13)	V_{SS}(12)
Read	+12	+5	0	0	0	0	0
Program	0	0	−2	+26	0	+26	0
Erase	0	0	−5	0	+36	−40	0 or Open
Verify "0"	+12	+5		0	0	+3	0
Verify "1"	+12	+5		0	0		0



Notes: * = Either High or Low Level, or Open.

① R_{CG} and R_{CL} are Protection Resistors
R_{CG} = 10 kΩ ± 10%, 1/4W
R_{CL} = 200Ω ± 10%, 10W

② R_{CG} may be left connected in Read Mode.

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	INPUT/ OUTPUT	FUNCTION
1 – 8, 26, 27	$A_0 - A_9$	Input	Address Input
24	$\overline{CS}$	Input	Chip Select Input (Active Low)
9 – 11, 17 – 21	$O_1 - O_8$	Output	Data Out for Read Operation
		Input	Data Input for Programming Operation
15	P_G	Power Supply	Power Supply for Programming Operation
16	V_{CL}	Power Supply	Power Supply for Erasure Operation
13	V_{CG}	Power Supply	Power Supply for Control Gate for Programming and Erasure Operation
14	V_{BB}	Power Supply	Power Supply for Substrate Bias
23	V_{DD}	Power Supply	+12V Power Supply for Read Operation
28	V_{CC}	Power Supply	+5V Power Supply for Read Operation
12	V_{SS}	GND	Ground Reference

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READ OPERATION

DC CHARACTERISTICS

$T_a = -10$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$,
$V_{BB} = P_G = V_{CL} = V_{CG} = V_{SS} = 0V$

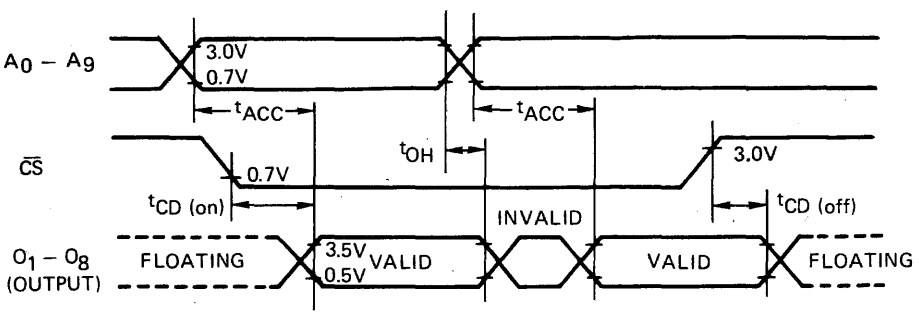
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	3.0		V_{CC}	V	
Input Low Voltage	V_{IL}	0		0.7	V	
Output High Voltage	V_{OH}	3.5			V	$I_{OH} = -2.0$ mA
Output Low Voltage	V_{OL}			0.5	V	$I_{OL} = 1.7$ mA
Input Leakage Current High	I_{LIH}			+10	μA	$V_I = +3.0V$
Input Leakage Current Low	I_{LIL}			-10	μA	$V_I = +0.7V$
Output Leakage Current High	I_{LOH}			+20	μA	$\overline{CS}$ = "1" $V_O = 3.5V$
Output Leakage Current Low	I_{LOL}			-10	μA	$\overline{CS}$ = "1" $V_O = 0.4V$
V_{DD} Supply Current	I_{DD}		55	80	mA	
V_{CC} Supply Current	I_{CC}		20	30	mA	with no load

AC CHARACTERISTICS

$T_a = -10$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$,
$V_{BB} = P_G = V_{CL} = V_{CG} = V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Access Time	t_{ACC}			450	ns	1 TTL + 100 pF
$\overline{CS}$ to Output On Delay	$t_{CD(on)}$			200	ns	
$\overline{CS}$ to Output Off Delay	$t_{CD(off)}$	0		200	ns	
Output Hold Time	t_{OH}	0			ns	

TIMING WAVEFORMS



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PROGRAMMING OPERATION

Programming is performed word by word and one word at a time. Address and an 8 bit programming word for that address should be input at the same time. High level data "1" given through one of Data Input terminals ($O_1 - O_8$) writes a high level data "1" into the memory cell specified with the address input and its bit position.

After erasure, all memory cells of the μPD458 contain cleared data "0" By this programming operation, only the memory cells which contain data "0" are programmed to high level data "1" by high level input. Thus before normal programming operation, the μPD458 should undergo erasure operation to clear all bits to "0".

DC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = V_{SS} = V_{CL} = 0V$. $\overline{CS}$ = Either HIGH or LOW level.

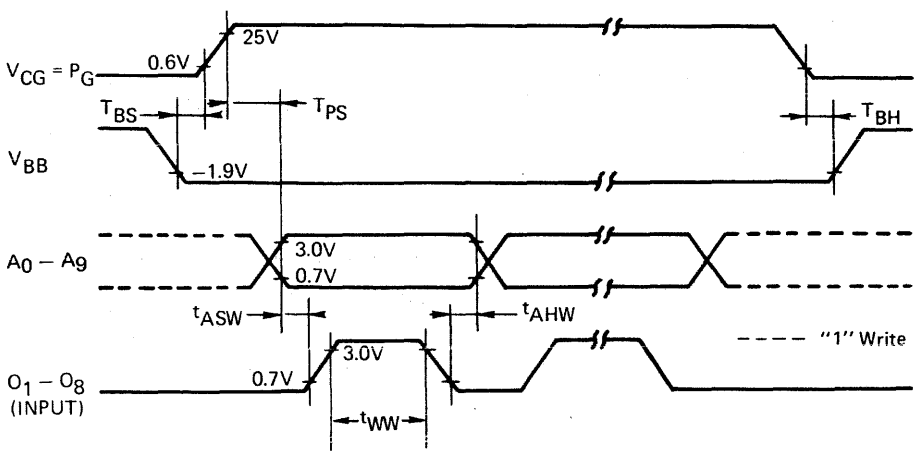
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	3.0		5.25	V	
Input Low Voltage	V_{IL}	0		0.7	V	
Supply Voltage	V_{BB}	-1.9	-2.0	-2.1	V	
Supply Voltage	P_G	25	26	27	V	
Supply Voltage	V_{CG}	25	26	27	V	through R_{CG}
Supply Current (V_{BB})	I_{BB}		-8	-15	mA	
Supply Current (P_G)	I_G		+30	+50	mA	
Supply Current (V_{CG})	I_{CG}			+20	μA	

AC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = V_{SS} = V_{CL} = 0V$. $\overline{CS}$ = Either HIGH or LOW level.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Address Setup Time	t_{ASW}	10			μs	
Address Hold Time	t_{AHW}	10			μs	
Write Data Width	t_{WW}	40		100	ms	per one word
V_{BB} Setup Time	T_{BS}	1.0			μs	
V_{BB} Hold Time	T_{BH}	1.0			μs	
P_G, V_{CG} Setup Time	T_{PS}	10			μs	

TIMING WAVEFORMS



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ERASURE OPERATION*

DC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = P_G = 0V$, $V_{SS} = 0V$ or Open
$\overline{CS}$, $A_0 - A_9$ and $O_1 - O_8$ = Either HIGH or LOW level, or non-connected

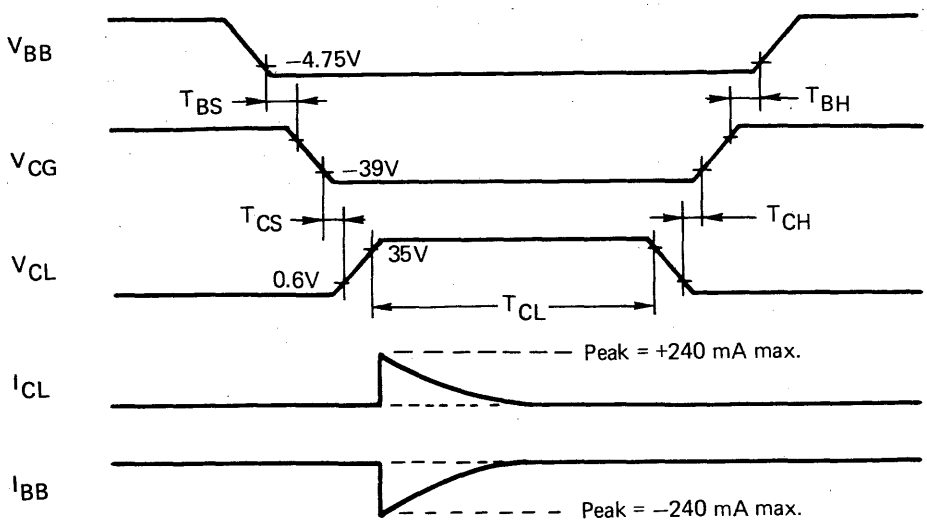
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Supply Voltage	V_{BB}	-4.75	-5.0	-5.25	V	
Supply Voltage	V_{CL}	+35	+36	+37	V	through R_{CL}
Supply Voltage	V_{CG}	-39	-40	-41	V	through R_{CG}
Supply Current (V_{BB})	I_{BB}			-240	mA	Initial peak current. See timing chart.
Supply Current (V_{CL})	I_{CL}			+240	mA	
Supply Current (V_{CG})	I_{CG}			-20	μA	

AC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = P_G = 0V$, $V_{SS} = 0V$ or Open
$\overline{CS}$, $A_0 - A_9$ and $O_1 - O_8$ = Either HIGH or LOW level, or non-connected

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Clear Time	T_{CL}		60		sec	
V_{BB} Setup Time	T_{BS}	0			μs	
V_{BB} Hold Time	T_{BH}	0			μs	
V_{CG} Setup Time	T_{CS}	1.0			μs	
V_{CG} Hold Time	T_{CH}	1.0			μs	

TIMING WAVEFORMS



Note: The supply currents I_{BB} and I_{CL} diminish to almost zero within T_{CL}.

*Erasure operation clears all 8192 bits to Logic "0" simultaneously.

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APPENDIX
PROM PROGRAMMER
DESIGN

To insure integrity and retention of data programmed in the μPD458, the following requirements are specified for the μPD458 supply voltage and current levels. The PROM PROGRAMMER should be designed such that voltages provided to the PROM socket be within the range specified on any occasion including power on/off to the programmer, power on/off to the μPD458, and in READ, WRITE or ERASE operation. Surge or noise voltages beyond the specified range are to be avoided.

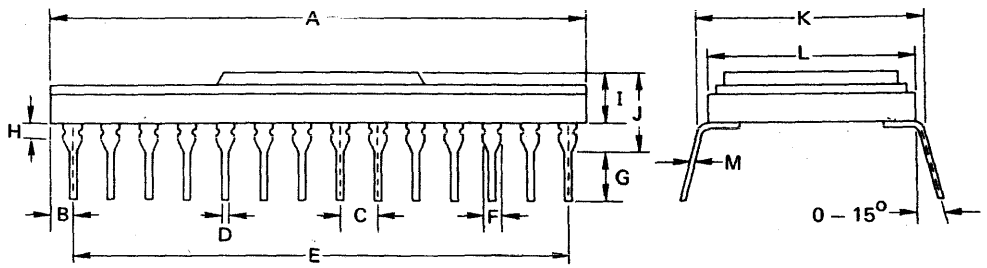
Setting V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5% and V_{CG} = +3V ± 0.1V after erasure and comparing data read from the μPD458 with zero effectively tests for proper erasure.

Setting V_{DD}= +12V ± 5%, V_{CC} = +5V ± 5% and V_{CG} = -3V ± 0.1V after programming and comparing data read from the μPD458 with the desired data coupled with erase verification, provides a simple test of worst-case temperature and long-term data retention.

Under normal Read Mode conditions, V_{CG} should either be grounded directly or held at 0V ± 0.1V through R_{CG}. R_{CG} is required when any non-zero voltage is applied to V_{CG}.

SYMBOL	LIMITS② READ MIN	READ TYP	READ MAX	PROGRAM MIN	PROGRAM TYP	PROGRAM MAX	ERASE MIN	ERASE TYP	ERASE MAX	UNIT	TEST CONDITIONS
V_{DD}	+11.4	+12	+12.6	-0.3	0	+0.3	-0.3	0	+0.3	V	
V_{CC}	+4.75	+5	+5.25	-0.3	0	+0.3	-0.3	0	+0.3	V	
V_{CG}	-0.1	0	+0.1	+25	+26	+27	-39	-40	-41	V	
V_{BB}	-0.1	0	+0.1	-1.9	-2	-2.1	-4.75	-5	-5.25	V	
P_G	-0.3	0	+0.3	+25	+26	+27	-0.3	0	+0.3	V	
V_{CL}	-0.1	0	+0.1	-0.1	0	+0.1	+35	+36	+37	V	
I_{CC}		+20	+30			-0.2			-0.2	mA	①
I_{DD}		+55	+80			-0.2			-0.2	mA	①
I_{CG}			+10			+20			-20	μA	①
I_{BB}			-0.2		-8	-15			-240	mA	①
I_{PG}			-0.2		+30	+50			-0.2	mA	①
I_{CL}			-0.5			-10			+240	mA	①

Notes: ① At typical supply voltage
② All voltages relative to VSS = 0V.



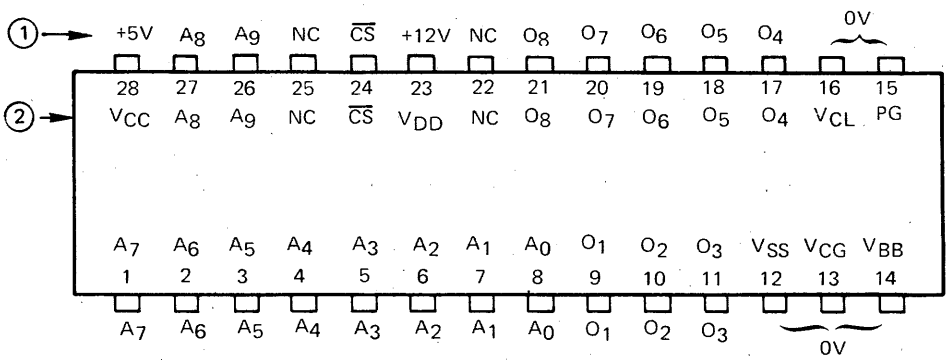
PACKAGE OUTLINE
μPD458D

ITEM	MILLIMETERS	INCHES
A	36.0 MAX.	1.41 MAX.
B	1.5 MAX.	0.059 MAX
C	2.54	0.1
D	0.50 ± 0.1	0.02 ± 0.004
E	33.0	1.299
F	1.27	0.05
G	3.2 MIN.	0.126 MIN
H	1.0 MIN	0.04 MIN
I	3.3 MAX.	0.13 MAX.
J	5.2 MAX.	0.20 MAX.
K	15.3	0.60
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

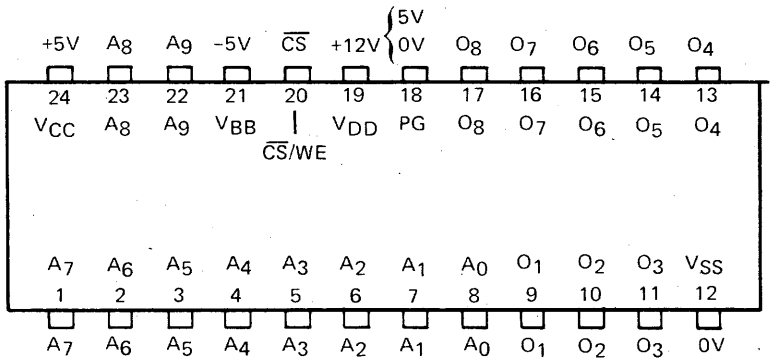
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μPD458

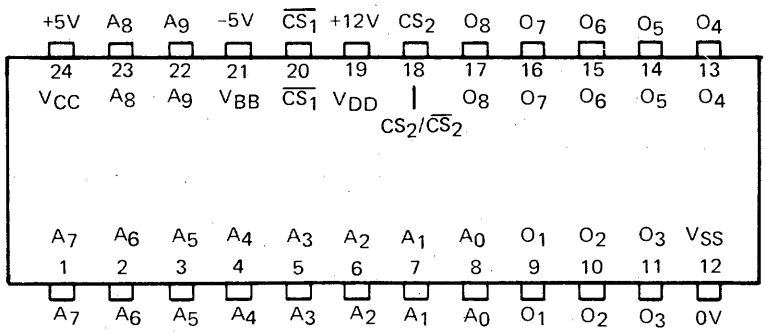
μPD458D (EEPROM)



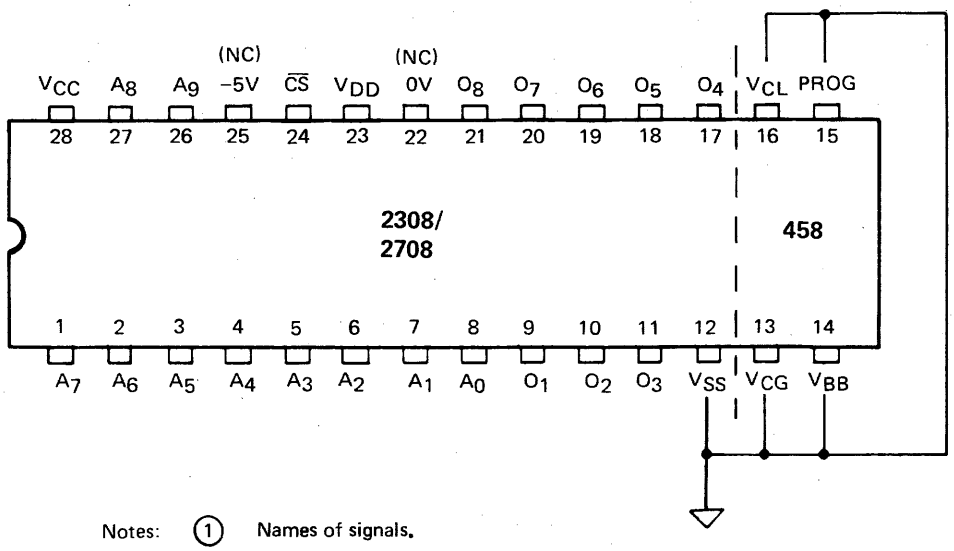
2708 (PROM ERASABLE WITH ULTRAVIOLET)



μPD2308C/D – 2308 (MASK ROM)



COMMON PIN CONFIGURATION



Notes: ① Names of signals.
② Names of the terminal.

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1024-BIT BIPOLAR TTL PROGRAMMABLE READ ONLY MEMORY

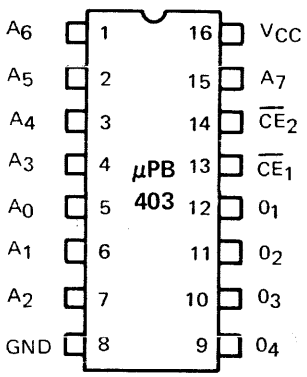
DESCRIPTION

The μPB403 is a high speed electrically programmable fully decoded 1024 bit TTL read only memory. On-chip address decoding, two chip enable inputs and open-collector outputs allow easy expansion of memory capacity. The μPB403 is fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

FEATURES

- 256 Words x 4 Bits Organization (Fully Decoded)
- TTL Interface
- Fast Read Access Time: 30 ns TYP.
- Medium Power Consumption: 450 mW TYP.
- AIM (Avalanche Induced Migration) Technology
- Two Chip Enable Inputs for Memory Expansion
- Open-Collector Outputs
- Ceramic 16-Pin Dual-In-Line Package
- Fast Programming Time: 200 μs/bit TYP.
- Compatibility with: Intersil's IM5603A (both in programming and as a ROM), Harris HPROM1024A and Equivalent Devices (as a ROM)

PIN CONFIGURATION



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OPERATION

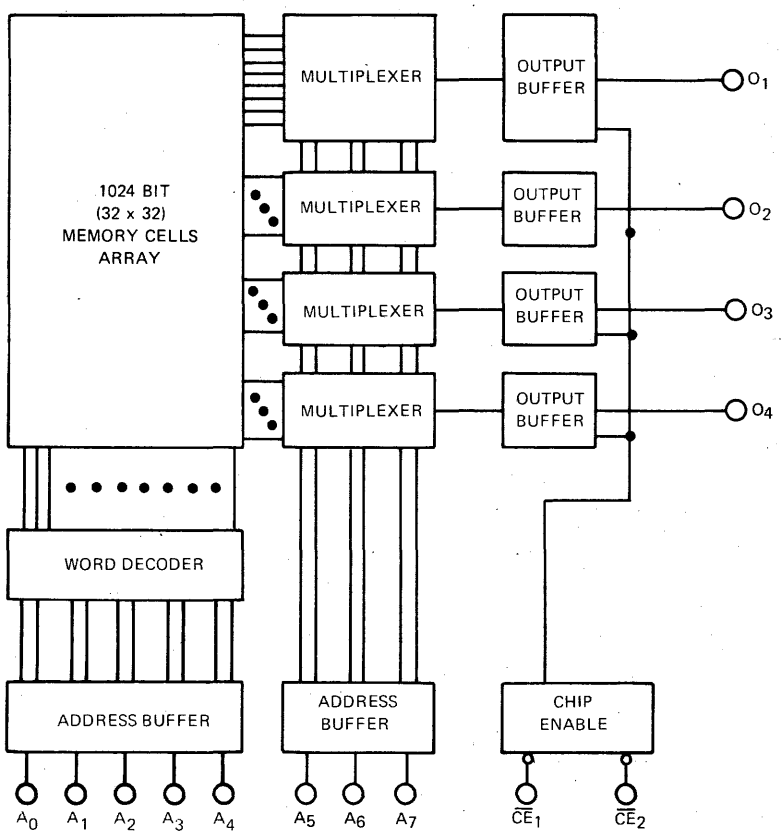
Programming

A logic one can be permanently programmed into a selected bit location in accordance with the programming procedures specified. First, the desired word is selected by the eight TTL address inputs. Either or both of the two chip enable inputs should be at a logic one (high). Secondly, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, and programming is complete.

Reading

To read the memory, both of the two chip enable inputs should be held at logic zero (low). The outputs then correspond to the data programmed in the selected words. When either or both of the two chip enable inputs are at logic one (high), all the outputs will be high (floating).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-25°C to +75°C
Storage Temperature	-65°C to +150°C
All Output Voltages	-0.5 to +5.5 Volts
All Input Voltages	-0.5 to +5.5 Volts
Supply Voltage V_{CC}	-0.5 to +7.0 Volts
Output Currents	50 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

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DC CHARACTERISTICS

T_a = 0°C to +65°C, V_{CC} = 4.75V to 5.25V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High Current	I_{IH}			40	μA	V_I = 2.7V
Input Low Current	$-I_{IL}$			1.0	mA	V_I = 0.4V
Output Low Voltage	V_{OL}			0.45	V	I_O = 16 mA
Output Leakage Current	I_{OFF1}			40	μA	V_O = 5.25V
Output Leakage Current	$-I_{OFF2}$				μA	V_O = 0.4V
Input Clamp Voltage	$-V_{IC}$			1.3	V	I_I = −12 mA
Power Supply Current	I_{CC}		90	130	mA	All Inputs Grounded

AC CHARACTERISTICS

T_a = 25°C, V_{CC} = 5.0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Address Access Time	t_{AA}		30	60	ns	See Notes
Chip Enable Access Time	t_{ACE}			30	ns	
Chip Enable Disable Time	t_{DCE}			30	ns	

Notes:
① Output Load: See Figure 1.
② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10 ns for both rise and fall times.
③ Measurement References: 1.5V for both inputs and outputs.
④ C_L in Figure 1 includes jig and probe stray capacitances.

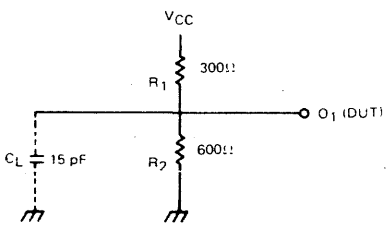
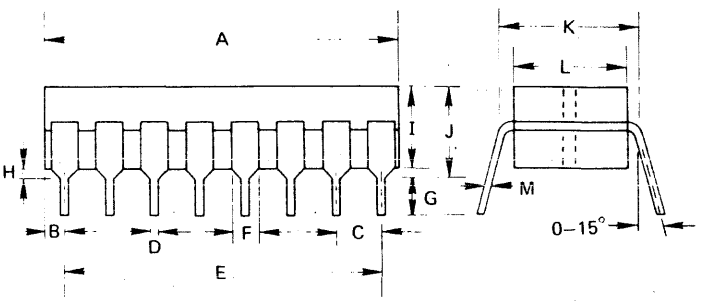


Figure 1

PACKAGE OUTLINE μPB403D



ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{0.05}$	$0.0098^{+0.0039}_{0.0019}$

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PROGRAMMING SPECIFICATION

It is imperative that this specification be rigorously observed in order to correctly program the μPB403. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

A typical programming operation is performed by first sensing, then programming, then sensing again to see if the word to be programmed has reached the desired state.

Sensing is accomplished by forcing a 20 mA current into the selected location via the output. The μPB403 is disabled by forcing 2 mA into one of the chip enables. The sense measurement is to ensure that the voltage required to force this 20 mA current is less than the reference voltage. If this condition is satisfied, then that bit location is in the logic "1" (high) state.

Programming is accomplished by forcing a 200 mA current into the selected bit via the output. This operation is also executed with 2 mA being forced into a chip enable. This current pulse is applied for 7.5 μs and then the location is sensed before a second programming current pulse is applied. This process is continued until that location is altered to the "1" state. A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ± 5	°C	
Programming Pulse			
Amplitude	200 ± 5%	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate (both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ± 5%	μs	15V point/ 150Ω load.
Duty Cycle	70% MIN.		
Sense Current			
Amplitude	20 ± 0.5	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate	70 MAX.	V/μs	15V point/ 150Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 + 5% − 0%	V	
Maximum Sensed Voltage for programmed "1"	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

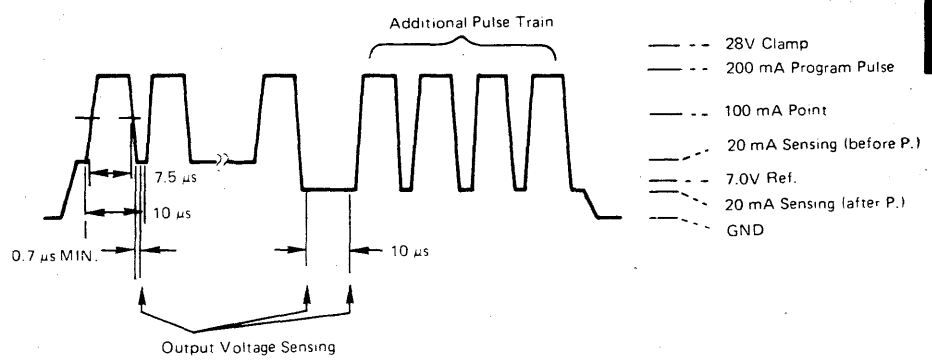


Figure 2. Typical Output Voltage Waveform

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4096-BIT BIPOLAR TTL PROGRAMMABLE READ ONLY MEMORY

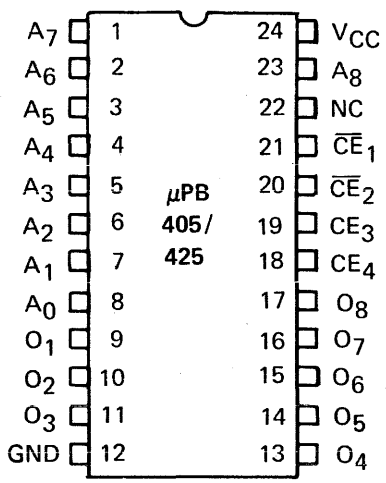
DESCRIPTION

The μPB405 and μPB425 are high speed, electrically programmable, fully decoded 4096-bit TTL read only memories. On-chip address decoding, four chip enable inputs and open-collector outputs allow easy expansion of memory capacity. The μPB405 and μPB425 are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

FEATURES

- 512 WORDS X 8 BITS Organization (Fully Decoded)
- TTL Interface
- Fast Read Access Time: 70 ns max. (μPB425)
- Medium Power Consumption: 600 mW TYP.
- Four Chip Enable Inputs for Memory Expansion
- Open-Collector Outputs (μPB405)/Three-State Outputs (μPB425)
- Ceramic 24-Lead Dual In-Line Package
- Fast Programming Time: 200 μs/bit TYP.
- Compatibility with: Intersil's IM5605/5625 (both in programming and as a ROM), Harris' HPROM HM-7640/7641 and Equivalent Devices (as a ROM).
- A.I.M. (Avalanche Induced Migration) Technology

PIN CONFIGURATION



NC: No Connection

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OPERATION

Chip Enable logic is defined by:

$\overline{CE}_1$	$\overline{CE}_2$	CE_3	CE_4	CE'
0	0	1	1	0
All other combinations				1

Where: CE' = 0 denotes chip selected
CE' = 1 denotes chip deselected

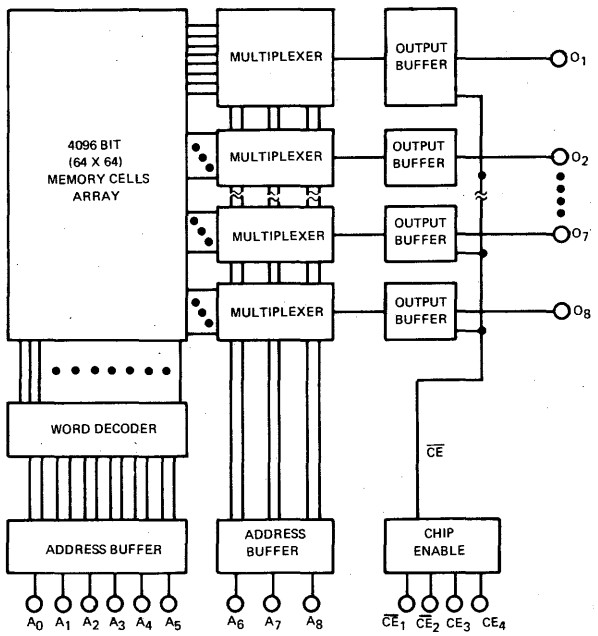
Programming

A logic one can be permanently programmed into a selected bit location in accordance with the programming procedures specified. First, the desired word is selected by the eight TTL address inputs. The four Chip Enable inputs must be set so that CE' is a logical one. Secondly, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, and programming is complete.

Reading

To read the memory, the four Chip Enable inputs must be set so that CE' is a logical zero. The outputs then correspond to the data programmed in the selected words. When the four Chip Enable inputs are set so that CE' becomes a logical one, all the outputs will be high (floating).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−25°C to +75°C
Storage Temperature	−65°C to +150°C
All Output Voltages	−0.5 to +5.5 Volts
All Input Voltages	−0.5 to +5.5 Volts
Supply Voltage V_{CC}	−0.5 to +7.0 Volts
Output Currents	50 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

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DC CHARACTERISTICS

T_a = 0°C to +65°C, V_{CC} = 4.75V to 5.25V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High Current	I_{IH}			40	μA	V_I = 2.7V
Input Low Current	$-I_{IL}$			0.5	mA	V_I = 0.4V
Output Low Voltage	V_{OL}			0.45	V	I_O = 16 mA
Output Leakage Current	I_{OFF1}			40	μA	V_O = 5.25V
Output Leakage Current	$-I_{OFF2}$	40			μA	V_O = 0.4V
Input Clamp Voltage	$-V_{IC}$			1.3	V	I_I = −12 mA
Power Supply Current	I_{CC}		120	160	mA	All Inputs Grounded
Output High Voltage①	V_{OH}	2.4			V	I_O = −2.4 mA
Output Short Circuit Current①	$-i_{SC}$	15		60	mA	V_O = 0V

NOTE: ① Applicable to μPB425D only.

AC CHARACTERISTICS

T_a = 25°C, V_{CC} = 5.0V

PARAMETER	SYMBOL	LIMITS 405-E/425-E			LIMITS 425			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Address Access Time	t_{AA}			100		40	70	ns	
Chip Enable Access Time	t_{ACE}			70			35	ns	
Chip Enable Disable Time	t_{DCE}			70			35	ns	

Notes: ① Output Load: See Figure 1.
② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10 ns for both rise and fall times.
③ Measurement References: 1.5V for both inputs and outputs.
④ C_L in Figure 1 includes jig and probe stray capacitances.

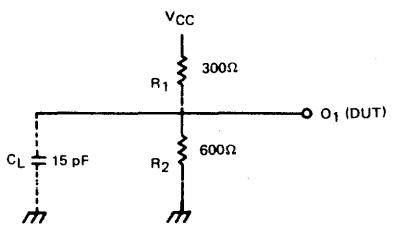
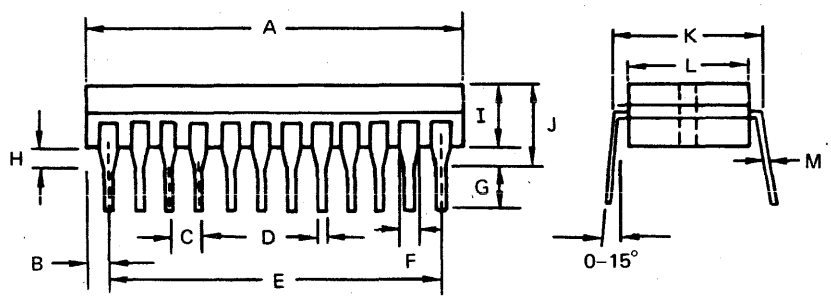


Figure 1

PACKAGE OUTLINE μPB405/425D



ITEM	MILLIMETERS	INCHES
A	33.5 MAX.	1.32 MAX.
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.019 MIN.
I	4.58 MAX.	0.181 MAX.
J	5.08 MAX.	0.2 MAX.
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

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PROGRAMMING SPECIFICATION

It is imperative that this specification be rigorously observed in order to correctly program the μPB405 and μPB425. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

A typical programming operation is performed by first sensing, then programming, then sensing again to see if the word to be programmed has reached the desired state.

Sensing is accomplished by forcing a 20 mA current into the selected location via the output. The μPB405 and μPB425 are disabled in accordance with the truth table on page 2. The sense measurement is to ensure that the voltage required to force this 20 mA current is less than the reference voltage. If this condition is satisfied, then that bit location is in the logic "1" (high) state.

Programming is accomplished by forcing a 200 mA current into the selected bit via the output. This current pulse is applied for 7.5 μs and then the location is sensed before a second programming current pulse is applied. This process is continued until that location is altered to the "1" state. A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ± 5	°C	
Programming Pulse			
Amplitude	200 ± 5%	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate (both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ± 5%	μs	15V point/ 150Ω load.
Duty Cycle	70% MIN.		
Sense Current			
Amplitude	20 ± 0.5	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate	70 MAX.	V/μs	15V point/ 150Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 + 5% − 0%	V	
Maximum Sensed Voltage for programmed "1"	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

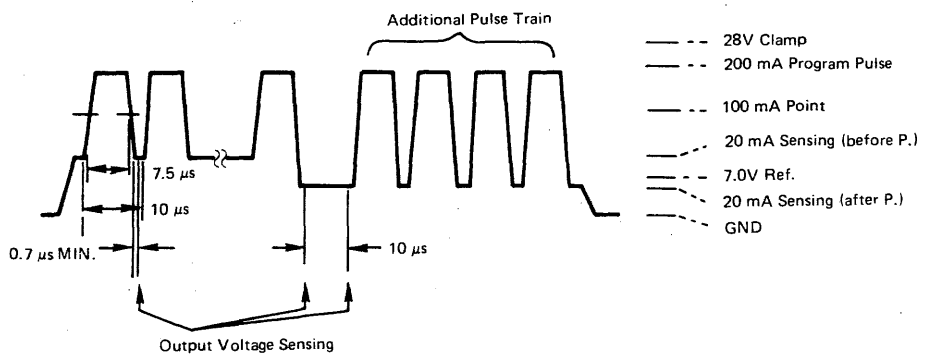


Figure 2. Typical Output Voltage Waveform

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μPB406
μPB406-E
μPB426
μPB426-E

4096-BIT BIPOLAR TTL PROGRAMMABLE READ ONLY MEMORY

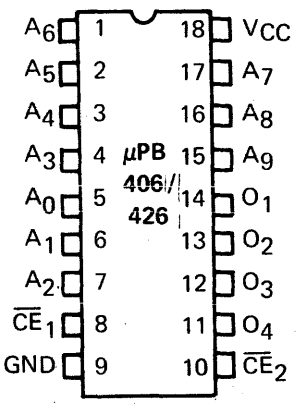
DESCRIPTION

The μPB406 and μPB426 are high speed electrically programmable fully decoded 4096-bit TTL read only memories. On-chip address decoding, two chip enable inputs and open-collector/three-state outputs allow easy expansion of memory capacity. The μPB406 and μPB426 are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

FEATURES

- 1024 WORDS X 4 BITS Organization (Fully Decoded)
- TTL Interface
- Fast Read Access Time: 70 ns MAX. (406/426)
- Medium Power Consumption: 500 mW TYP.
- Two Chip Enable Inputs for Memory Expansion
- Open-Collector Output (μPB406, μPB406 E)/Three-State Outputs (μPB426, μPB426-E)
- Ceramic 18-Lead Dual In-Line Package
- Fast Programming Time: 200 μs/bit TYP.
- Compatibility with: Intersil's IM56S06/56S26 (both in programming and as a ROM), Harris' HPROM HM-7642/7643 and Equivalent Devices (as a ROM)
- A.I.M. (Avalanche Induced Migration) Technology

PIN CONFIGURATION



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OPERATION

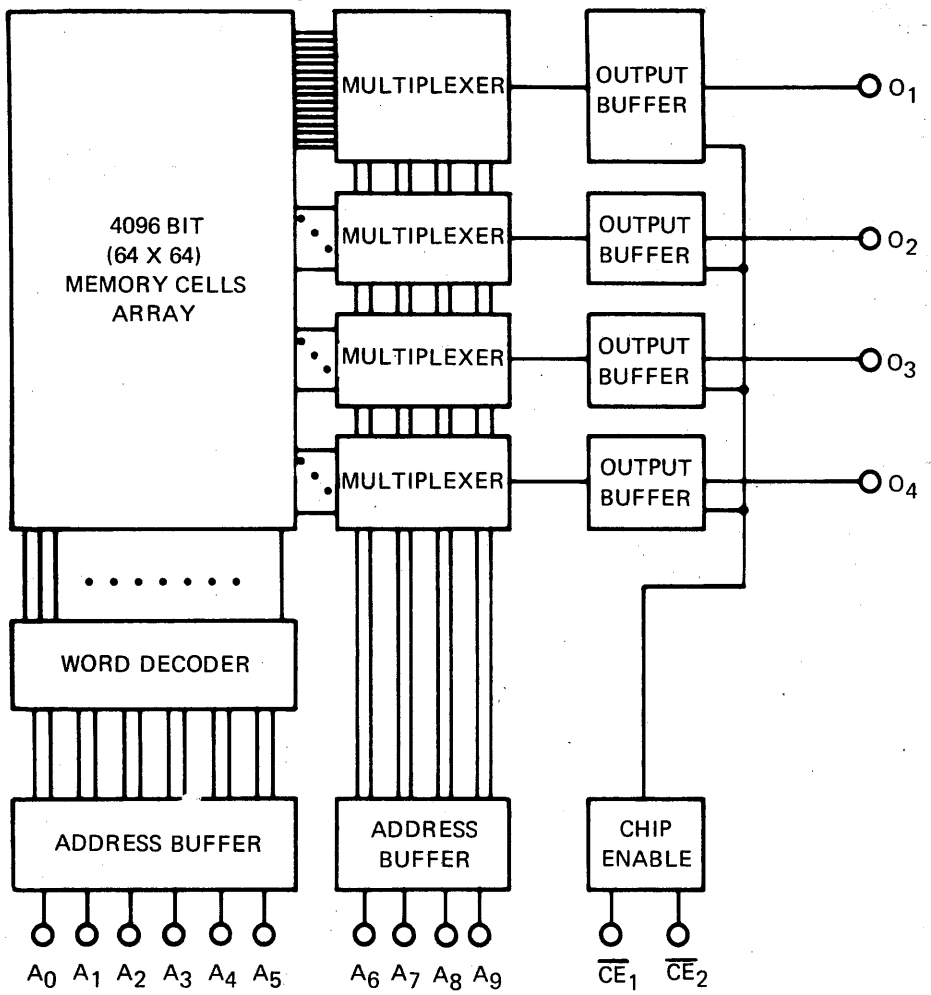
Programming

A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First, the desired word is selected by the ten address inputs in TTL levels. Either or both of the two chip enable inputs must be at a logic one (high). Secondly, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

Reading

To read the memory, both of the two chip enable inputs should be held at logic zero (low). The outputs then correspond to the data programmed in the selected words. When either or both of the two chip enable inputs are at logic one (high), all the outputs will be high (floating).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-25°C to +75°C
Storage Temperature	-65°C to +150°C
All Output Voltages	-0.5 to +5.5 Volts
All Input Voltages	-0.5 to +5.5 Volts
Supply Voltage V_{CC}	-0.5 to +7.0 Volts
Output Currents	50 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

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DC CHARACTERISTICS

T_a = 0°C to +65°C, V_{CC} = 4.75V to 5.25V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High Current	I_{IL}			40	μA	V_I = 2.7V
Input Low Current	$-I_{IL}$			0.5	mA	V_I = 0.4V
Output Low Voltage	V_{OL}			0.45	V	I_O = 16 mA
Output Leakage Current	I_{OFF1}			40	μA	V_O = 5.25V
Output Leakage Current	$-I_{OFF2}$	40			μA	V_O = 0.4V
Input Clamp Voltage	$-V_{IC}$			1.3	V	I_I = −12 mA
Power Supply Current	I_{CC}		100	150	mA	All Inputs Grounded
Output High Voltage①	V_{OH}	2.4			V	I_O = −2.4 mA
Output Short Circuit Current①	$-I_{SC}$	15		60	mA	V_O = 0V

NOTE: ① Applicable to μPB426D only.

AC CHARACTERISTICS

T_a = 25°C, V_{CC} = 5.0V

PARAMETER	SYMBOL	LIMITS 406-E/426-E			LIMITS 406/426			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Address Access Time	t_{AA}			100		40	70	ns	
Chip Enable Access Time	t_{ACE}			70			40	ns	
Chip Enable Disable Time	t_{DCE}			70			40	ns	

Notes: ① Output Load: See Figure 1.
② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10 ns for both rise and fall times.
③ Measurement References: 1.5V for both inputs and outputs.
④ C_L in Figure 1 includes jig and probe stray capacitances.

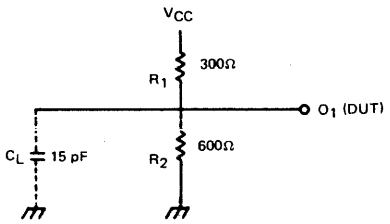
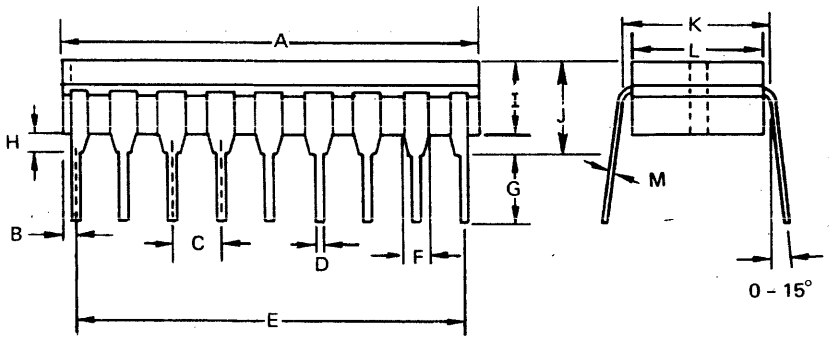


Figure 1

PACKAGE OUTLINE μPB406/426D



ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.05
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

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PROGRAMMING SPECIFICATION

It is imperative that this specification be rigorously observed in order to correctly program the μPB406 and μPB426. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

A typical programming operation is performed by first sensing, then programming, then sensing again to see if the word to be programmed has reached the desired state. Either or both of the two chip enable inputs must be at a logic one (high).

Sensing is accomplished by forcing a 20 mA current into the selected location via the output. The sense measurement is to ensure that the voltage required to force this 20 mA current is less than the reference voltage. If this condition is satisfied, then that bit location is in the logic "1" (high) state.

Programming is accomplished by forcing a 200 mA current into the selected bit via the output. This current pulse is applied for 7.5 μs and then the location is sensed before a second programming current pulse is applied. This process is continued until that location is altered to the "1" state. A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ± 5	°C	
Programming Pulse			
Amplitude	200 ± 5%	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate (both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ± 5%	μs	15V point/ 150Ω load.
Duty Cycle	70% MIN.		
Sense Current			
Amplitude	20 ± 0.5	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate	70 MAX.	V/μs	15V point/ 150Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 + 5% − 0%	V	
Maximum Sensed Voltage for programmed "1"	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

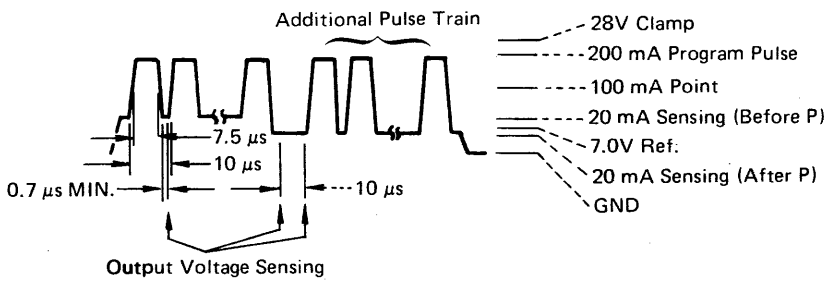


Figure 2 — Typical Output Voltage Waveform

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FULLY DECODED 2048 BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The μPD464 is a 2048 bit (256 x 8) mask programmable Read Only Memory. It is pin-for-pin compatible with NEC's Electrically Eraseable Programmable ROM (EEPROM), the μPD454. The μPD464 features high speed operation, making it suitable for large volume microcomputer memory applications that used the μPD464 for initial prototyping.

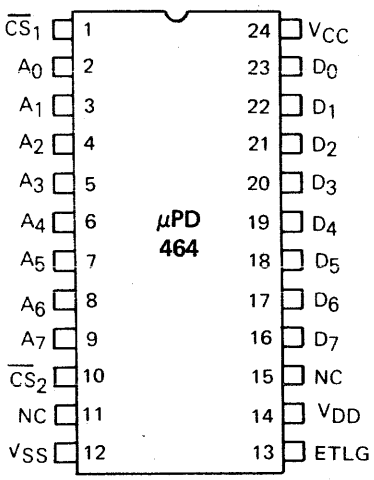
All inputs and outputs of the μPD464 are TTL compatible. Two chip select pins ($\overline{CS}_1$, $\overline{CS}_2$) are provided for selection of an individual device in systems with OR-tied outputs. Two power supplies, +12 volts and +5 volts, are required.

The μPD464 is fabricated using NEC's N-channel MOS silicon gate process, providing excellent contamination protection. This process enables high performance, highly reliable MOS circuits to be produced. The μPD464 is packaged in a 24-pin ceramic or plastic dual-in-line package.

FEATURES

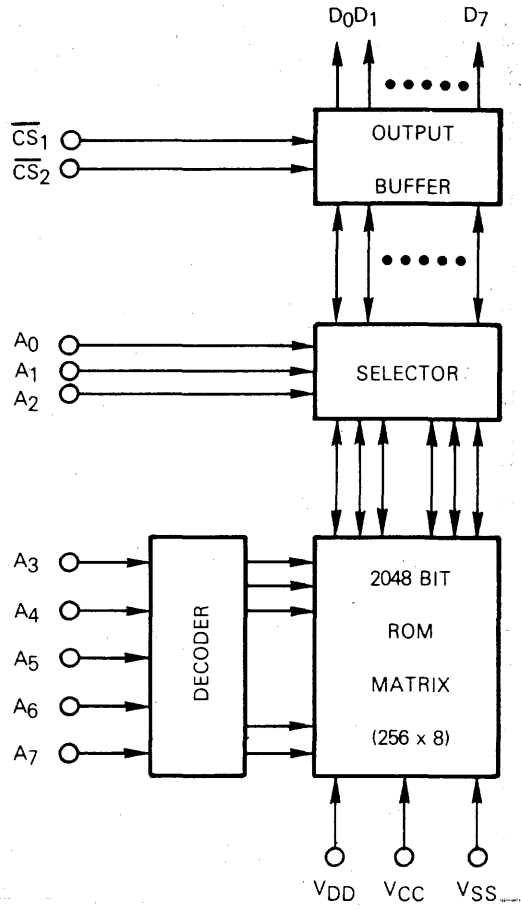
- Fully Decoded, 256 Words x 8 Bits Organization
- Access Time 450 ns Max.
- Static, No Clock Required
- Input/Output TTL Compatible
- Three-State Output, OR-Tie Capability
- N-Channel MOS Fabrication
- Two Power Supplies, +12V and +5V
- 24 Pin Ceramic or Plastic DIP

PIN CONFIGURATION



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BLOCK DIAGRAM



PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1	$\overline{CS_1}$ ①	CHIP SELECT 1	Chip selection, active low
2–9	A_0–A_7	ADDRESS BUS	Memory address
10	$\overline{CS_2}$ ①	CHIP SELECT 2	Chip selection, active low
11	NC		No connection
12–13	V_{SS}	GROUND	Ground Reference
14	V_{DD}	+12V Power Supply	Power Supply
15	NC		No connection
16–23	D_7–D_0	Data output	Data Output
24	V_{CC}	+5V Power Supply	Power Supply

Note: ① Chip is selected only when both $\overline{CS_1}$ and $\overline{CS_2}$ are low.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
All Output Voltages	−0.3 to +7 Volts
All Input Voltages	−0.3 to +7 Volts
Supply Voltage V_{DD}	−0.3 to +15 Volts
Supply Voltage V_{CC}	−0.3 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

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DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{DD} = +12V \pm 5\%$; $V_{CC} = +5V \pm 5\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input High Voltage	V_{IH}	+2.4		V_{CC}	V	
Input Low Voltage	V_{IL}	-0.3		+ 0.7	V	
Output High Voltage	V_{OH}	+3.5			V	$I_{OH} = -1.0$ mA
Output Low Voltage	V_{OL}			0.5	V	$I_{OL} = +1.7$ mA
Input Leakage Current High	I_{LIH}			+10	μA	$V_I = +2.4V$
Input Leakage Current Low	I_{LIL}			-10	μA	$V_I = +0.7V$
Output Leakage Current High	I_{LOH}			+10	μA	$V_O = +3.5V$
Output Leakage Current Low	I_{LOL}			-10	μA	$V_O = +0.4V$
V_{DD} Supply Current	I_{DD}		35	55	mA	
V_{CC} Supply Current	I_{CC}		20	30	mA	

CAPACITANCE

$T_a = -10°C$ to $+70°C$; $V_{DD} = +12V \pm 5\%$; $V_{CC} = +5V \pm 5\%$; $V_{SS} = 0V$

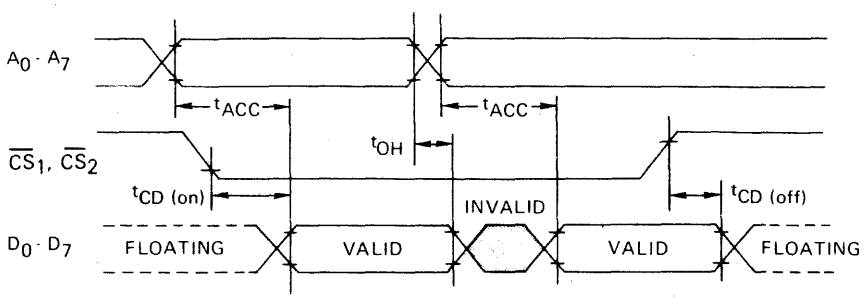
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Capacitance	C_{IN}		6	15	pF	f = 1 MHz
Output Capacitance	C_{OUT}		8	15	pF	f = 1 MHz

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{DD} = +12V \pm 5\%$; $V_{CC} = +5V \pm 5\%$; $V_{SS} = 0V$

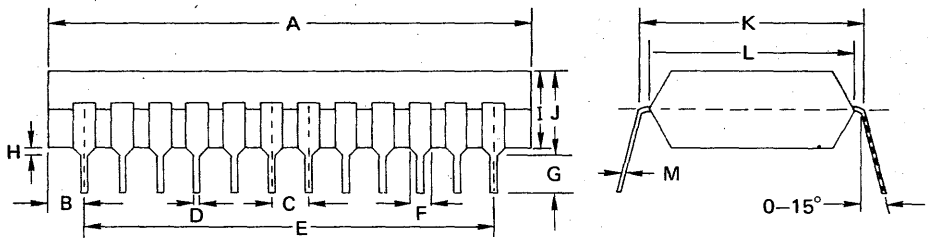
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Access Time	t_{ACC}			450	ns	1 TTL + 100 pF
$\overline{CS}$ to Output On Delay	t_{CD} (on)			250	ns	
$\overline{CS}$ to Output Off Delay	t_{CD} (off)	0		250	ns	
Output Hold Time	t_{OH}	20			ns	

TIMING WAVEFORM



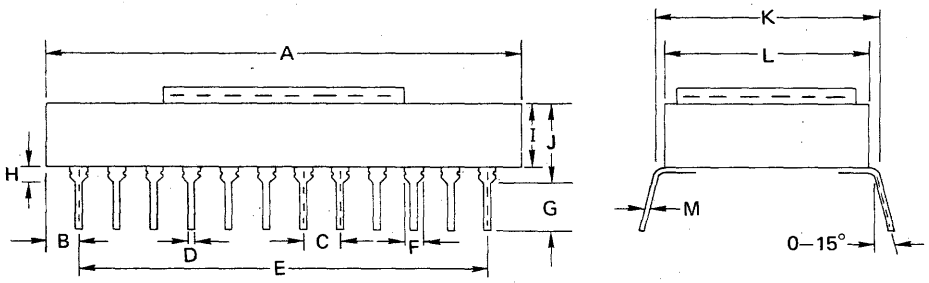
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PACKAGE OUTLINE μPD464C/D



μPD464C (Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



μPD464D (Ceramic)

ITEM	MILLIMETERS	INCHES
A	32.5 MAX	1.28 MAX
B	2.28	0.09
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.20 MIN	0.047 MIN
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.165 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

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FULLY DECODED 8192 BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

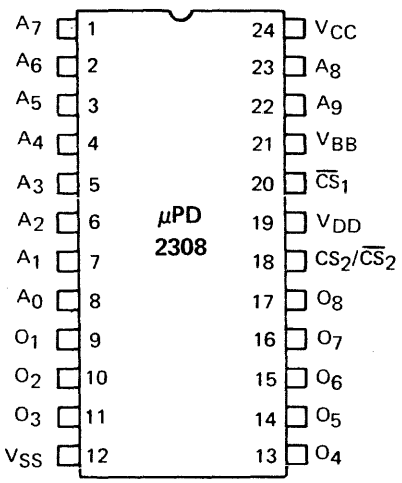
The NEC μPD2308 is a high speed 8,192 bit mask programmable Read Only Memory organized as 1024 words by 8 bits. The μPD2308 is fabricated with N-channel MOS technology.

Two Chip Selects are provided – $\overline{CS}_1$ which is negative true, and $CS_2/\overline{CS}_2$ which may be programmed either negative or positive true at the mask level.

FEATURES

- 1024 Words by 8 bits Organization
- Fast Access – 450 ns max
- Two Chip Select Inputs for Easy Memory Expansion
- TTL Compatible – All Inputs and Outputs
- Three State Output – OR-Tie Capability
- Fully Decoded
- Standard Power Supplies – +12V, ±5V
- 24 Pin Plastic or Ceramic Dual-in-Line Package
- Pin Compatible with INTEL 8308

PIN CONFIGURATION

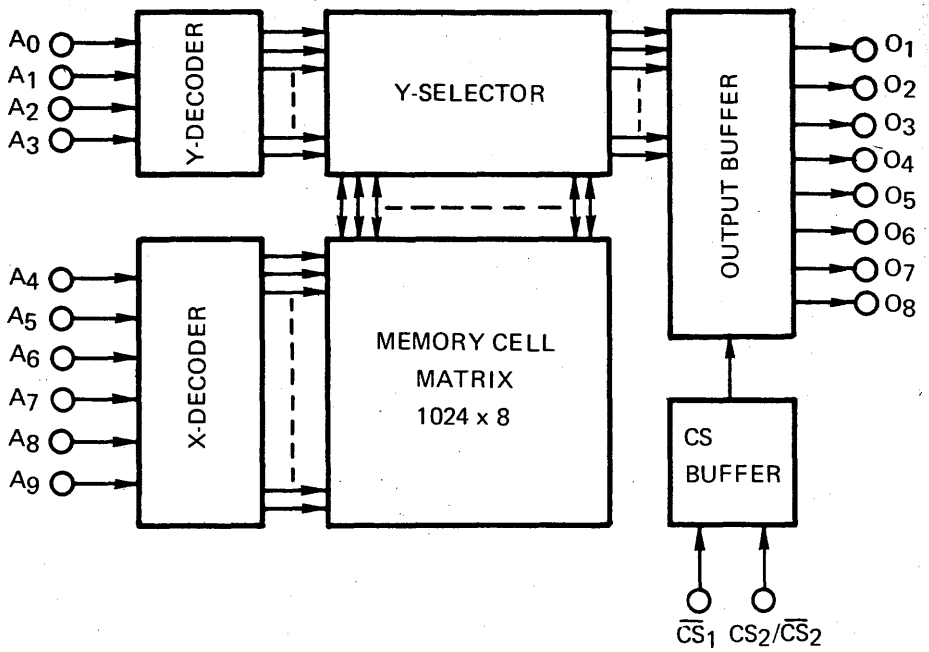


PIN NAMES

$A_0 - A_9$	Address Inputs
$\overline{CS}_1$	Chip Select 1
$CS_2/\overline{CS}_2$	Chip Select 2
$O_1 - O_8$	Data Outputs

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +125°C
All Input Voltages	−1 to +7 Volts ①
All Output Voltages	−1 to +7 Volts ①
Supply Voltage V_{DD}	−1 to +15 Volts ①
Supply Voltage V_{CC}	−1 to +7 Volts ①
Supply Voltage V_{BB}	−2 to −8 Volts

Note: ① V_{BB} = −5.25 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C, V_{DD} = +12V±5%, V_{CC} = +5V±5%, V_{BB} = −5V±5%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Leakage Current (All Input Pins)	I_{LI}			±10	μA	V_I = 0 to 5.25V
Output Leakage Current	I_{LO}			±10	μA	V_O = 0-5.25V Chip Deselected
Input Low Voltage	V_{IL}	V_{SS}-1		0.8	V	
Input High Voltage	V_{IH}	2.4		V_{CC} + 1.0	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −4 mA
Output High Voltage	V_{OH2}	3.7			V	I_{OH} = −1 mA
Power Supply Current V_{CC}	I_{CC}		14	30	mA	
Power Supply Current V_{DD}	I_{DD}		15	30	mA	
Power Supply Current V_{BB}	I_{BB}			−1	mA	
Power Dissipation	P_D			545	mW	

Note: Typical values are for T_a = 25°C and nominal supply voltage.

CAPACITANCE

T_a = 25°C; V_{BB} = −5V; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			6	pF	V_{DD}, V_{CC} and all other pins tied to V_{SS}
Output Capacitance	C_{OUT}			12	pF	

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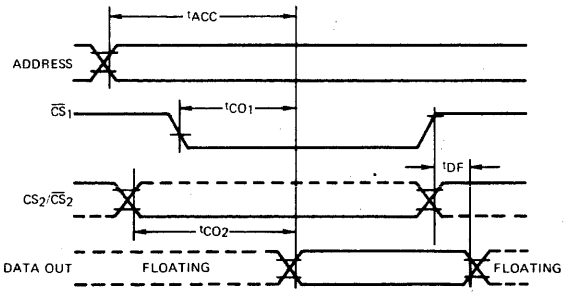
AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$

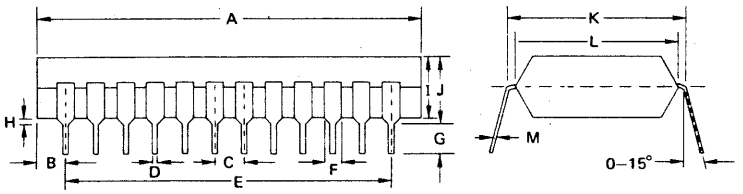
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Address to Output Delay Time	t_{ACC}		250	450	ns	$t_T = t_R = t_F = 20$ ns $V_{REF} = 2.4V, 0.8V$ $V_{IN} = 0.65V, 3.3V$ LOAD = 1 TTL GATE $C_L = 100$ pF
Chip Select 1 to Output Delay Time	t_{CO1}		125	200	ns	
Chip Select 2 to Output Delay Time	t_{CO2}		140	220	ns	
Chip Deselect to Output Float Time	t_{DF}		140	220	ns	

Note: Typical values are for $T_a = 25°C$ and nominal supply voltage.

TIMING WAVEFORMS

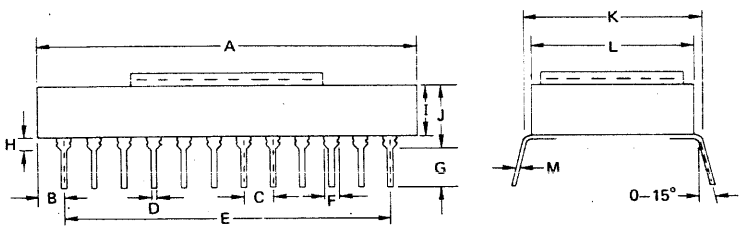


PACKAGE OUTLINE μPD2308C/D



μPD2308C (Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	0.25 $^{+0.10}_{-0.05}$	0.01 $^{+0.004}_{-0.0019}$



μPD2308D (Ceramic)

ITEM	MILLIMETERS	INCHES
A	32.5 MAX	1.28 MAX
B	2.28	0.09
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.20 MIN	0.047 MIN
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.165 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

SP2308-8-77-GY-CAT
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FULLY DECODED 16,384 BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

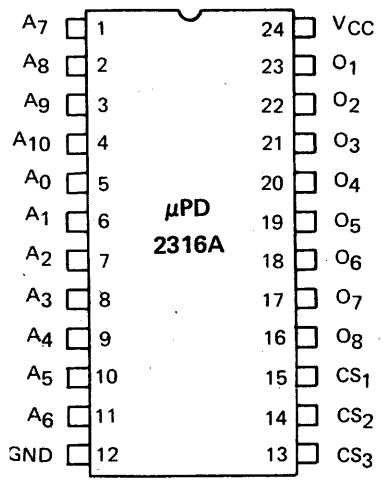
The NEC μPD2316A is a high speed 16,384 bit mask programmable Read Only Memory organized as 2048 words by 8 bits. The μPD2316A is fabricated with N-channel MOS technology.

The inputs and outputs are fully TTL compatible. The device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined and desired chip select code is fixed during the masking process.

FEATURES

- Access Time 450 ns Max
- 2048 Words x 8 Bits Organization
- Single +5V Power Supply Voltage
- Directly TTL Compatible – All Inputs and Outputs
- Three Programmable Chip Select Inputs for Easy Memory Expansion
- Three-State Output – OR-Tie Capability
- On Chip Address Fully Decoded
- All Inputs Protected Against Static Charge
- Direct Replacement for Intel 2316A/8316A
- Available in 24-pin plastic or ceramic package.

PIN CONFIGURATION

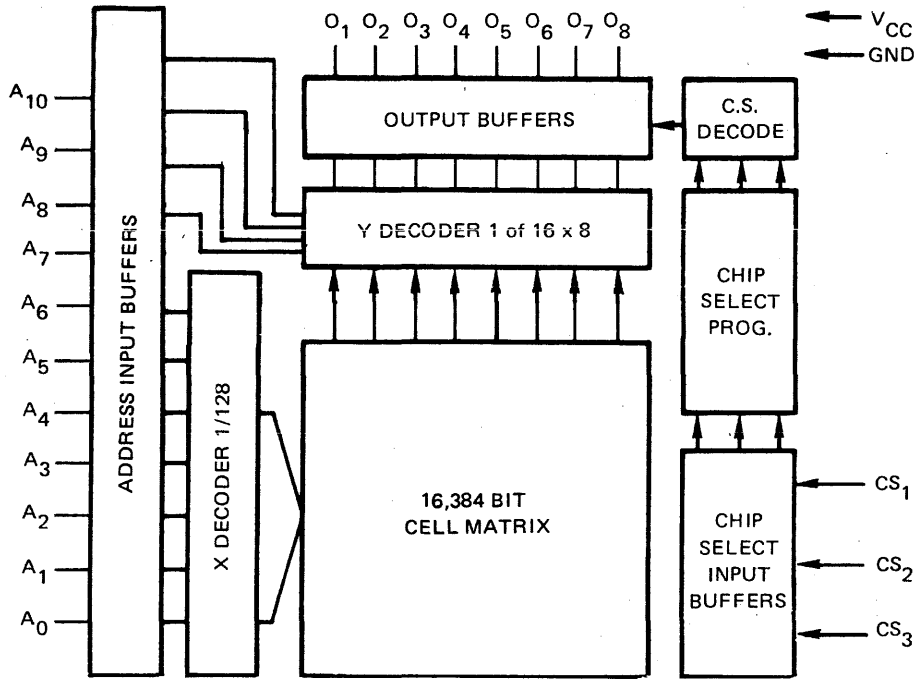


PIN NAMES

$A_0 - A_{10}$	Address Inputs
$O_1 - O_8$	Data Outputs
$CS_1 - CS_2$	Programmable Chip Select Inputs

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Voltage on Any Pin . . . . . −0.5 to +7.0 Volts ①

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{CC} = +5 ± 5% unless otherwise noted.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP ①	MAX		
Input Load Current (All Input Pins)	I_{LI}		1	10	μA	V_{IN} = 0 to 5.25V
Output Leakage Current	I_{LOH}			10	μA	CS = 2.2V (Deselected) V_{OUT} = V_{CC}
Output Leakage Current	I_{LOL}			−10	μA	CS = 2.2V (Deselected) V_{OUT} = 0V
Power Supply Current	I_{CC}			104	mA	All inputs 5.25V Data Out Open
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC} + 1.0V	V	
Output "Low" Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output "High" Voltage	V_{OH}	2.2			V	I_{OH} = 200μA

Note: ① Typical values for T_a = 25°C and nominal supply voltage.

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CAPACITANCE

$T_a = 25°C$; f = 1 MHz

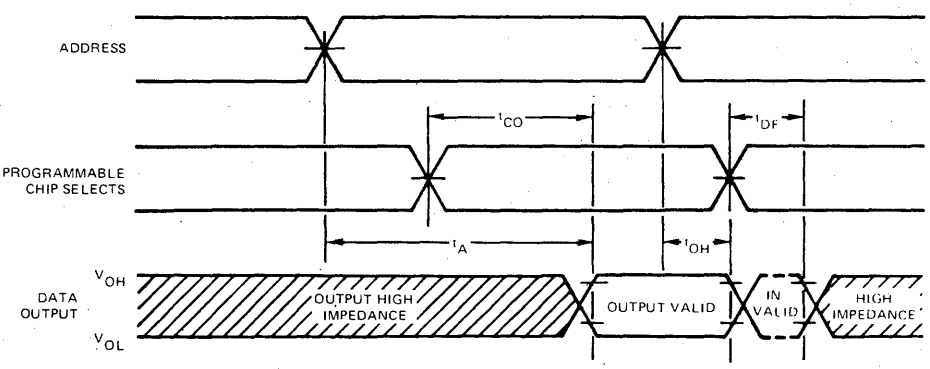
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pf	All Pins Except Pin Under Test Tied to AC Ground
Output Capacitance	C_{OUT}			15	pf	All Pins Except Pin Under Test Tied to AC Ground

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$ unless otherwise specified.

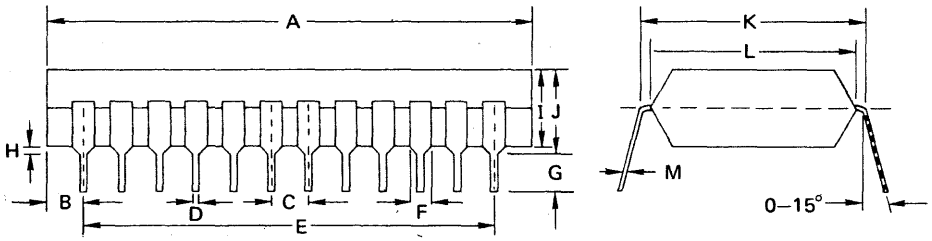
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address to Output Delay Time	t_A			450	ns	$t_T = t_r = t_f = 20$ ns $V_{ref\ in} = 1.5V$ $V_{ref\ out} = .45, 2.2V$ Output LOAD = 1 TTL GATE $C_L = 100$ pf
Chip Select to Output Enable Delay Time	t_{CO}			150	ns	
Chip Deselect to Output Data Float Delay Time	t_{DF}	0		150	ns	
Output Hold Time	t_{OH}	20			ns	

TIMING WAVEFORMS



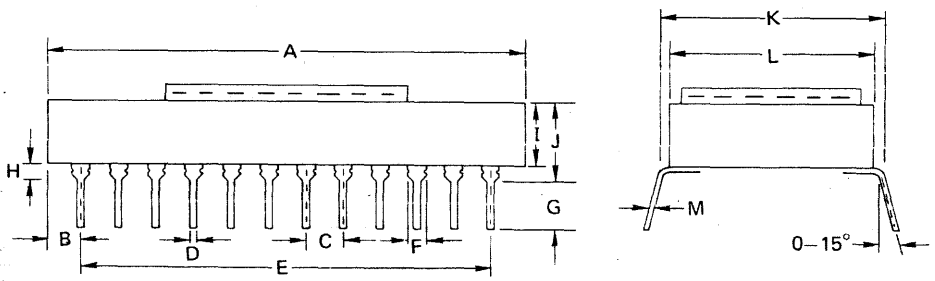
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PACKAGE OUTLINE
μPD2316AC/D



μPD2316AC (Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



μPD2316AD (Ceramic)

ITEM	MILLIMETERS	INCHES
A	32.5 MAX	1.28 MAX
B	2.28	0.09
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.20 MIN	0.047 MIN
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.165 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

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FULLY DECODED 32,768 BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

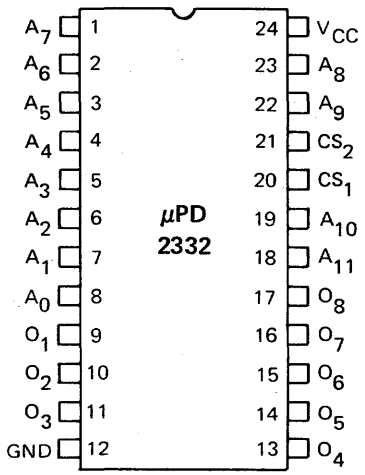
The NEC μPD2332 is a Fully Decoded 32,768 Bit Mask Programmable Read-Only Memory organized as 4,096 Words by 8 Bits. The μPD2332 has two chip select inputs and the combination of "High"/"Low" levels of these inputs is mask-programmable.

The μPD2332 is fabricated with sophisticated N-channel MOS technology and features high speed and TTL compatibility for simple interface with bipolar circuits.

FEATURES

- 4096 Words x 8 Bits Organization
- Directly TTL Compatible – All Inputs and Outputs
- Fully Static (No Clock or Refresh Required)
- Single +5V Power Supply
- High Speed – Access Time 450 ns Max.
- Three-State Output – OR-Tie Capability
- Two Programmable Chip Select Inputs for Easy Memory Expansion
- N-Channel MOS Technology
- Pin Compatible with TI TMS4732
- 24 Pin Plastic or Ceramic Dual-in-Line Package

PIN CONFIGURATION



PIN NAMES

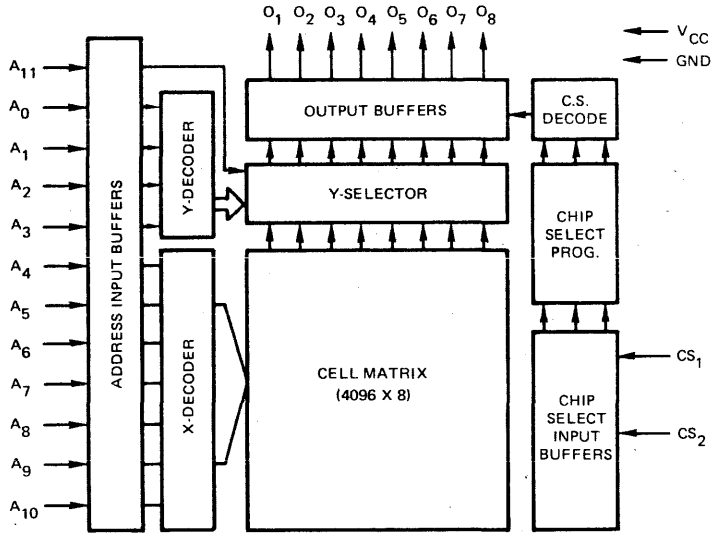
$A_0 - A_{11}$	Address Inputs
$O_1 - O_8$	Data Outputs
$CS_1 - CS_2$	Programmable Chip Select Inputs

When ordering the μPD2332, specify a chip select combination of CS_1 and CS_2 from the following.

CS_2	CS_1
0	0
0	1
1	0
1	1

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Supply Voltage On Any Pin . . . . . −0.5 to +7.0 Volts①

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}			10	μA	
Output Leakage Current	I_{LOH}			+10	μA	CS = 2.2V (Deselected) V_{OUT} = V_{CC}
Output Leakage Current	I_{LOL}			−10	μA	CS = 2.2V (Deselected) V_{OUT} = 0V
Power Supply Current	I_{CC}		55	110	mA	All inputs 5.25V Data Out Open
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC} + 1.0V	V	
Output "Low" Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output "High" Voltage	V_{OH}	2.2			V	I_{OH} = −100 μA

Note: ① Typical Values for T_a = 25°C and nominal supply voltages.

CAPACITANCE

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	All Pins Except Pin Under Test Tied to AC Ground
Output Capacitance	C_{OUT}			15	pF	All Pins Except Pin Under Test Tied to AC Ground

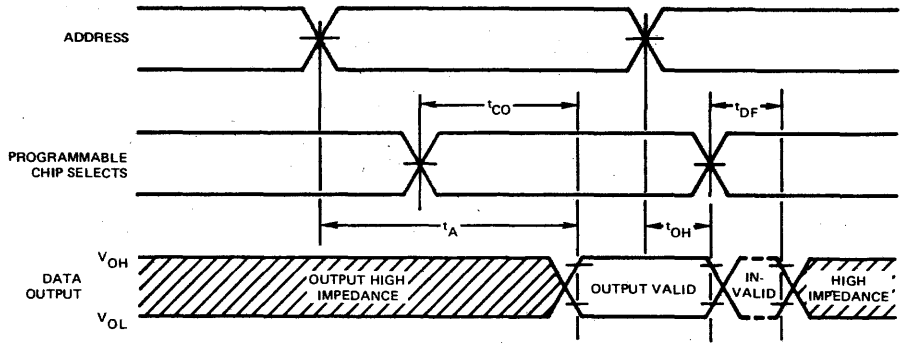
AC CHARACTERISTICS

T_a = −10°C to +70°C, V_{CC} = +5V ± 5% unless otherwise specified.

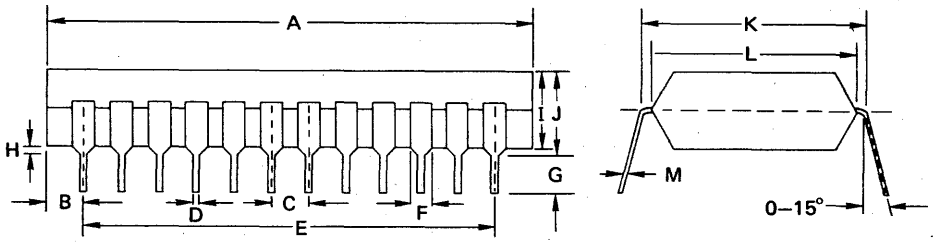
PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Address to Output Delay Time	t_A			450	ns	t_T = t_r = t_f = 20 ns
Chip Select to Output Enable Delay Time	t_{CO}			150	ns	C_L = 100 pF
Chip Deselect to Output Data Float Delay Time	t_{DF}	0		150	ns	Load = ITTL gate
Output Hold Time	t_{OH}	20			ns	V_{IN} = 0.8 to 2V V_{ref} Input = 1.5V V_{ref} Output = 0.45/2.2V

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TIMING WAVEFORMS

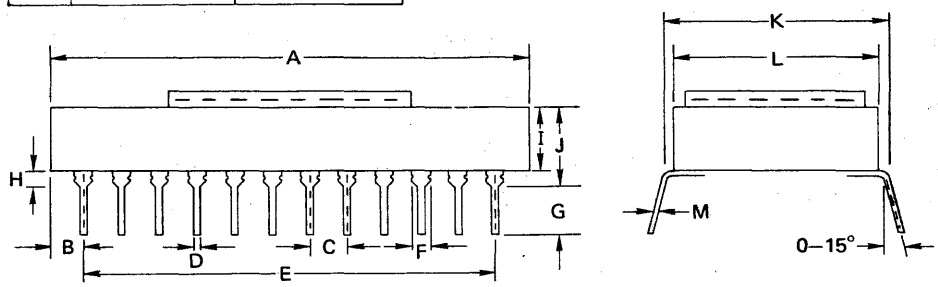


PACKAGE OUTLINE μPD2332C/D



μPD2332C (Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



μPD2332D (Ceramic)

ITEM	MILLIMETERS	INCHES
A	32.5 MAX	1.28 MAX
B	2.28	0.09
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.20 MIN	0.047 MIN
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.165 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

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NEC microcomputers, inc.

PRELIMINARY

μPD414A
μPD414A-1
μPD414A-2
μPD414A-3

4K BIT DYNAMIC RAM

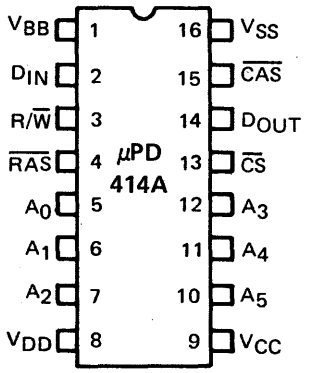
DESCRIPTION

The NEC μPD414A is a 4096 words by 1 bit dynamic Random Access Memory fabricated with N-channel MOS technology. It features high performance, low power, and 16 pin packaging for high system bit density. The 12 bit address is multiplexed into the chip in two 6 bit halves. Flexible I/O control allows common or separate I/O data busses.

FEATURES

- Four speeds: 300 ns (μPD414A)
  250 ns (μPD414A-1)
  200 ns (μPD414A-2)
  150 ns (μPD414A-3)
- ±10% Supply Tolerance
- Gated $\overline{CAS}$ Operation
- Latched Output
- Three State Output
- Fully TTL Compatible
- Replacement for 4027 Type Devices

PIN CONFIGURATION



NEC microcomputers, inc.

PRELIMINARY

μPD6508
μPD6508-1

1K (1024x1) STATIC CMOS RAM

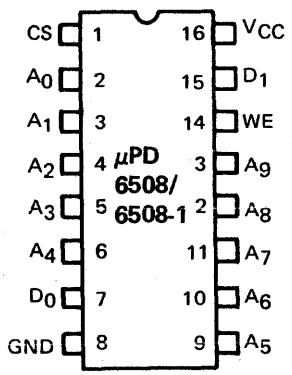
DESCRIPTION

The NEC μPD6508/6508-1 are high speed, low power, silicon gate CMOS RAMs organized as 1024 words by 1 bit. It features extremely low power requirements and data retention to +3 volts V_{CC}.

FEATURES

- Extremely Low Power Operation
- High Speed – 250 ns Max (μPD6508-1)
- TTL Compatible, All Inputs and Outputs
- Static Operation
- On Chip Register Address
- Replacement for 5608 Type Devices

PIN CONFIGURATION



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PRELIMINARY

NEC microcomputers, inc.

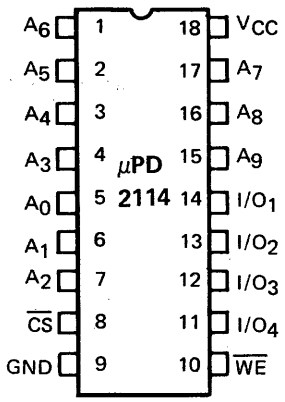
μPD2114

4K (1024x4) STATIC RAM

DESCRIPTION

The NEC μPD2114 is a 4096 bit, fully static Random Access Memory, organized as 1024 words by 4 bits. It is fabricated with N-channel silicon gate technology and is housed in an 18 pin package for high system bit densities.

PIN CONFIGURATION



FEATURES

- High Density 18 Pin Package
- Completely Static
- Directly TTL Compatible — All Inputs and Outputs
- Single +5V Supply
- Low Operating Power — 0.06 mW/Bit Typ
- Access Time — 250 ns Typical

NEC microcomputers, inc.

PRELIMINARY

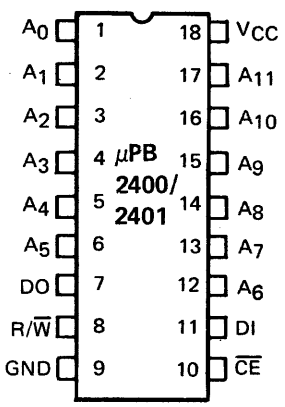
μPB2400
μPB2401

4096 BIT STATIC BIPOLAR RAM

DESCRIPTION

The NEC μPB2400 and μPB2401 are static, Random Access Memories organized as 4096 words by 1 bit. The devices feature operation from a single +5 volt supply, and are fully TTL compatible. Fast data out disable time allows a common I/O data bus structure.

PIN CONFIGURATION



FEATURES

- 4096 Words x 1 Bit Organization
- Fast Read and Write Cycle — 75 ns Typ
- Low Power Operation — 500 mW Typ
- Single +5 Volt Supply
- 18 Pin Cerdip Package
- Latched Data Outputs
- Three State (μPB2401) or Open Collector (μPB2400) Output
- Replacement for 74S400/401

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4096 × 1 STATIC NMOS RAM

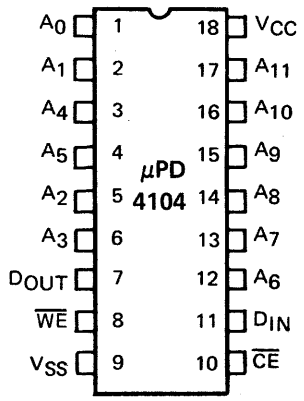
DESCRIPTION

The NEC μPD4104 is a high speed 4096 bit Static RAM organized as 4096 words by 1 bit. The use of static storage circuitry eliminates the need for refresh while the dynamic control circuitry provides substantially lower power dissipation than fully static types.

FEATURES

- Fast Access Time – 200 ns
- High System Density – 18 Pin Package
- Fully TTL Compatible – All Inputs and Outputs
- Single +5V Supply

PIN CONFIGURATION



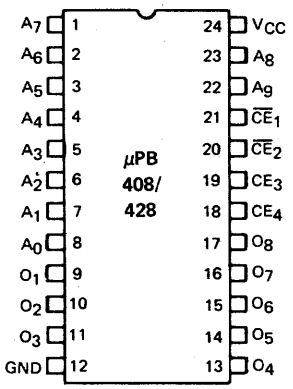
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8192 BIT BIPOLAR TTL PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The NEC μPB408 and μPB428 are high speed, electrically programmable, 8192 bit, TTL, Read Only Memories. Three chip enable inputs and three state (μPB428) or open collector (μPB408) outputs allow OR-tying outputs for ease of memory expansion. The devices are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the desired bit locations.

PIN CONFIGURATION



FEATURES

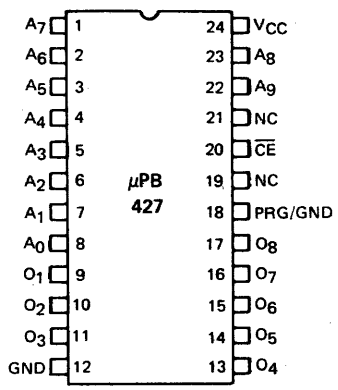
- 1024 Words x 8 Bits Organization
- Fast Access Time - 85 ns Max
- Three State (μPB428) or Open Collector (μPB408) Outputs
- Replacement for 6380/6381 Type Devices

8192 BIT BIPOLAR TTL PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The NEC μPB427 is a high speed, electrically programmable, 8192 bit, TTL, Read Only Memory. Three-state outputs and a chip enable input allow easy expansion of memory capacity. The μPB427 is fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the desired bit locations.

PIN CONFIGURATION



FEATURES

- 1024 Words x 8 Bits Organization
- Fast Read Access Time - 120 ns Max
- Power Switching - 750 mW Max Selected
  - 350 mW Max Unselected
- Three State Outputs
- Replacement for 2708 Type Devices as a ROM

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PRELIMINARY

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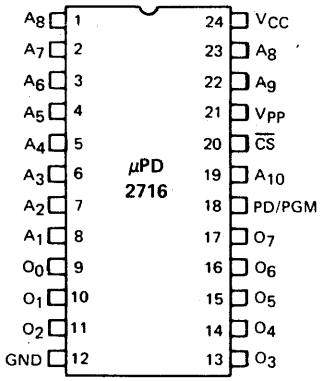
μPD2716

16K ULTRAVIOLET ERASABLE PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The NEC μPD2716 is a 16,384 bit ultraviolet erasable and electrically programmable Read Only Memory organized as 2048 words by 8 bits. Its 450 ns access time and single +5 volt supply make it ideal for microprocessor applications.

PIN CONFIGURATION



FEATURES

- Single +5 Volt Supply (Read Mode)
- Simple Programming
- Inputs and Outputs TTL Compatible in Read and Program Mode
- Low Power - 525 mW Max Active
  - 132 mW Max Standby

PRELIMINARY

NEC microcomputers, inc.

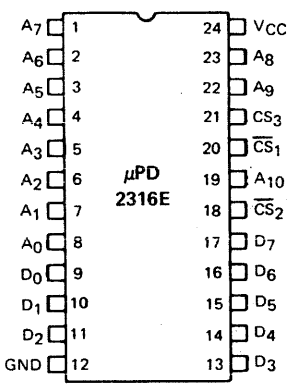
μPD2316E

16K (2048x8) MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The NEC μPD2316E is a high speed 16,384 bit mask programmable Read Only Memory organized as 2148 words by 8 bits. All inputs and outputs are fully TTL compatible. These devices operate with a single +5V supply. The three chip select inputs are programmable; any combination of active high or low level chip select inputs can be defined and fixed during the masking process.

PIN CONFIGURATION



FEATURES

- Access Time - 450 ns Max
- 2048 Words x 8 Bits Organization
- Single +5V Supply
- Directly TTL Compatible
- Three Programmable Chip Selects
- Three State Outputs — OR-Tie Capabilities
- Direct Replacement for 2316E Type Devices

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RAYTHEON THE NEW INNOVATOR IN PROGRAMMABLE MEMORY COMPONENTS

RAYTHEON

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POWER SWITCHED PROMS (SPROMS)

In June of 1977, Raytheon announced the first performance compatible PROMS with on-chip power switching. By simply de-selecting the SPROM, the typical power requirements are reduced from 70-80% depending on whether the device is an open-collector or tri-state version. In large PROM arrays, the direct substitution of the SPROM for the standard PROM can reduce the overall power consumption by more than 50%.

FEATURES

- Highly reliable nichrome fuses
- Three-state and open collector versions
- Standard PROM and SPROM (power switched) versions
- Standard pin outs
- Readily available programming equipment
- Available in both military and commercial temperature ranges
- Low current PNP inputs

AVAILABLE TYPES/ORDERING INFORMATION

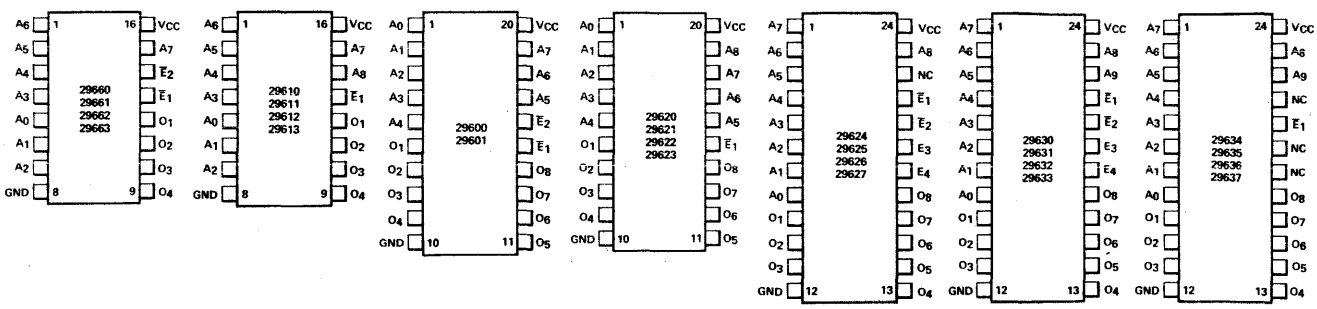
Total Bits	Configuration	Output	Part Number				Package (# of pins)
			Standard		Power Switched		
			Commercial (0 to +70°C)	Military[1] (-55 to +125°C)	Commercial (0 to +70°C)	Military[1] (-55 to +125°C)	
1024	256 x 4	OC	29660DC	29660DM	29662DC	29662DM	16
		TS	29661DC	29661DM	29663DC	29663DM	16
2048	512 x 4	OC	29610DC	29610DM	29612DC	29612DM	16
		TS	29611DC	29611DM	29613DC	29613DM	16
	256 x 8	OC	29600DC	29600DM			20
		TS	29601DC	29601DM			20
4096	512 x 8	OC	29620DC	29620DM	29622DC	29622DM	20
			29624DC	29624DM	29626DC	29626DM	24
		TS	29621DC	29621DM	29623DC	29623DM	20
			29625DC	29625DM	29627DC	29627DM	24
8192	1024 x 8	OC	29630DC	29630DM	29632DC	29632DM	24
		TS	29634DC	29634DM	29635DC	29635DM	24
			29631DC	29631DM	29633DC	29633DM	24
			29636DC	29636DM	29637DC	29637DM	24

Notes: 1. Also available in flat pack. Substitute FM for DM.

2. For 883B processing, add the letter "B" to the suffix, e.g., 29660DMB.

PIN ASSIGNMENTS

1024 Bits 256 x 4 | 2048 Bits 512 x 4 | 2048 Bits 256 x 8 | 4096 Bits 512 x 8 | 4096 Bits 512 x 8 | 8192 Bits 1024 x 8 | 8192 Bits 1024 x 8



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ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage temperature	-65 to +150° C
Temperature (ambient) under bias	-55 to +125° C
Supply voltage to ground potential continuous	-0.5 to +7V
DC voltage applied to outputs (except during programming)	-0.5V to +V_{CC} max.
DC input voltage (address inputs)	-0.5 to +5.5V
DC voltage applied to outputs during programming	26V
Output current into outputs during programming	125 mA
DC input voltage (chip select input)	-0.5 to +33V
DC input current	-30 to +5 mA

OPERATING RANGE

296XXDC	T_A = 0 to +75° C	V_{CC} = 5.0V ±5%	Commercial
296XXDM, 296XXFM	T_A =-55 to +125° C	V_{CC} = 5.0V ±10%	Military

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (unless otherwise noted)

PARAMETERS	DESCRIPTION	TEST CONDITIONS		MIN.	TYP[1]	MAX.	UNITS
V_{OH} (tri-state version)	Output HIGH voltage	V_{CC} = MIN., I_{OH} = -2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8 mA			0.4	Volts
			I_{OL} = 16 mA			0.5	
V_{IH}	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW current	V_{CC} = MAX., V_{IN} = 0.4V			-60	-250	μA
I_{IH}	Input HIGH current	V_{CC} = MAX.	V_{IN} = 2.7V			10	μA
		V_{CC} = MAX.	V_{IN} = 5.5V			1.0	mA
		Pin 13 only	V_{IN} = 4.5V			1.0	mA
I_{SC} (tri-state version)	Output short circuit current	V_{CC} = MAX., V_{OUT} = 0.0V		-12	-35	-85	mA
V_I	Input clamp voltage	V_{CC} = MIN., I_{IN} = 18 mA				-1.5	V
I_{CEX}	Output leakage current	V_{CC} = MAX.	V_O = 4.5V			100	μA
			V_O = 2.4V			40	
		V_{CS} = 2.4V	V_O = 0.4V			-40	

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25° C.

2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

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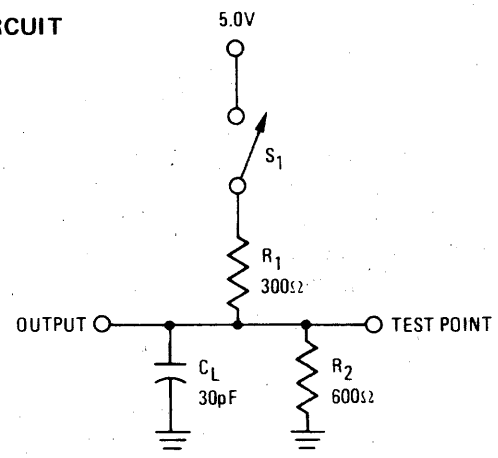
SWITCHING AND POWER CHARACTERISTICS

Part Type	AC Characteristics												Power Supply Current			
	Commercial						Military						Selected		Unselected	
	Address Access		Enable Access		Enable Recovery		Address Access		Enable Access		Enable Recovery					
	Typ (ns)	Max (ns)	Typ (ns)	Max (ns)	Typ (ns)	Max (ns)	Typ (ns)	Max (ns)	Typ (ns)	Max (ns)	Typ (ns)	Max (ns)	Typ (mA)	Max (mA)	Typ (mA)	Max (mA)
29600	50	70	20	40	20	40	50	90	20	50	20	50	90	130	N/A	N/A
29601	50	70	20	40	20	40	50	90	20	50	20	50	90	130	N/A	N/A
29610	30	55	20	30	20	30	30	70	20	40	20	40	90	130	N/A	N/A
29611	30	55	20	30	20	30	30	70	20	40	20	40	90	130	N/A	N/A
29612	35	60	40	60	15	30	35	75	40	75	15	40	90	130	20	30
29613	35	60	40	60	15	30	35	75	40	75	15	40	90	130	30	45
29620	40	65	20	40	20	40	40	80	20	50	20	50	100	140	N/A	N/A
29621	40	65	20	40	20	40	40	80	20	50	20	50	100	140	N/A	N/A
29622	45	70	45	70	20	40	45	85	45	85	20	55	100	140	30	40
29623	45	70	45	70	20	40	45	85	45	85	20	55	100	140	40	50
29624	40	65	20	40	20	40	40	80	20	50	20	50	100	140	N/A	N/A
29625	40	65	20	40	20	40	40	80	20	50	20	50	100	140	N/A	N/A
29626	45	70	45	70	20	40	45	85	45	85	20	55	100	140	30	40
29627	45	70	45	70	20	40	45	85	45	85	20	55	100	140	40	50
29630 *	45	70	20	40	20	40	40	85	20	50	20	50	110	150	N/A	N/A
29631 *	45	70	20	40	20	40	40	85	20	50	20	50	110	150	N/A	N/A
29632 *	50	80	50	80	20	40	50	90	50	90	20	50	110	150	35	45
29633 *	50	80	50	80	20	40	50	90	50	90	20	50	110	150	45	55
29634 *	45	70	20	40	20	40	40	85	20	50	20	50	110	150	N/A	N/A
29635 *	45	70	20	40	20	40	40	85	20	50	20	50	110	150	N/A	N/A
29636 *	50	80	50	80	20	40	50	90	50	90	20	50	110	150	35	45
29637 *	50	80	50	80	20	40	50	90	50	90	20	50	110	150	45	55
29660	45	70	20	35	20	35	45	80	20	40	20	40	90	130	N/A	N/A
29661	45	70	20	35	20	35	45	80	20	40	20	40	90	130	N/A	N/A
29662	35	60	40	60	15	30	35	75	40	75	15	40	90	130	20	30
29663	35	60	40	60	15	30	35	75	40	75	15	40	90	130	30	45

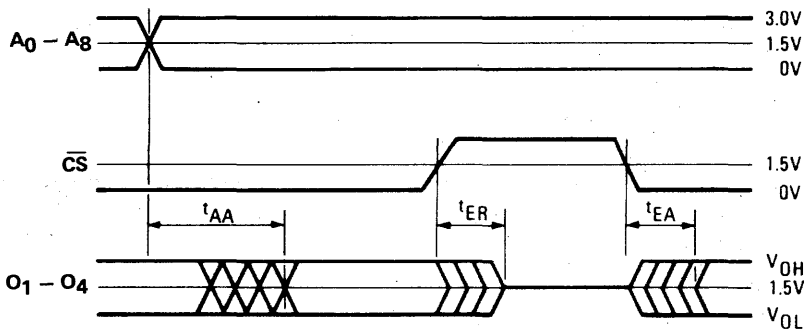
* Objective

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AC TEST CIRCUIT



SWITCHING WAVEFORMS



NOTE: LEVEL ON OUTPUT WHILE $\overline{CS}$ IS HIGH IS DETERMINED EXTERNALLY.

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▨	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
⋈	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

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PROGRAMMING INSTRUCTIONS

DEVICE DESCRIPTION

Raytheon PROMS are manufactured with all outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be changed from a low resistance to a high resistance. This procedure is called programming. Programming equipment can be obtained from Data I/O, Inc., and other manufacturers of P/ROM programming equipment.

PROGRAMMING DESCRIPTION

To select a particular fusible link for programming, the word address is presented with TTL levels on the address pins, a V_{CC} of 5.50V is applied or left applied, and the program pin (CS) and the output to be programmed are taken to an elevated voltage to supply the required current to program the fuse. The outputs must be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming at a time.

TIMING

The programming procedure involves the use of the program pin (CS) and the output pin. In order to guarantee that the output transistor is off before increasing the voltage on the output pin, the program pin's voltage pulse must come before the output pin's programming pulse and leave after the output pin's programming pulse. 100 ns delay is adequate. The programming pulse applied to the output pin and program pin must have a 50 to 70 microseconds rise time. See Figure 1.

PROGRAMMING SPEED

Typically fuses will blow on the rise time of the pulse.

In automated programmers which must copy devices in a short time because of production requirements, the following pulse and voltage sequences have been found to maximize reliability, programming yield, and thruput. The device should be verified after each programming attempt and is advanced to the next bit if the device has programmed.

PULSE NUMBER	PROGRAM PIN VOLTAGE	OUTPUT VOLTAGE
1 to 3	27V	20V
4 to 6	30V	23V
7 to 9	33V	26V

VERIFICATION

After programming either device, it can be checked for a low output by taking CS low. Since we must guarantee operation at minimum and maximum V_{CC}, current and temperature, the device must be required to sink 12 mA at 4.20V V_{CC} and 0.2 mA at 6.0V V_{CC} at room temperature.

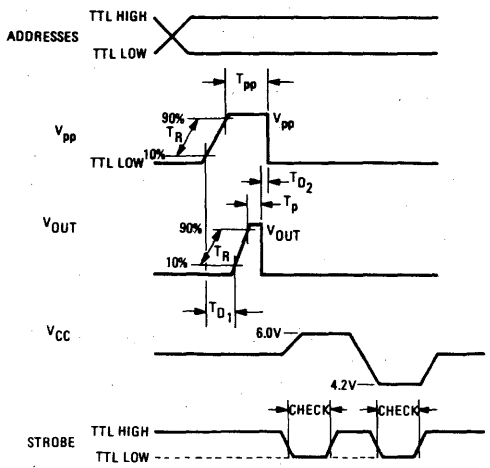
BOARD PROGRAMMING

Units may be programmed at the board level by bringing the program pin of each package to the card connector. To program a particular package "A", the program pin of package A and one output of package A, which may or may not be "OR" tied to other packages, are taken to the required programming voltage. An alternate procedure is to tie the CS and outputs together as required by the system function and only apply V_{CC} to the device to be programmed. The number of units soldered on a board should be consistent with expected programming yields to avoid rework.

UNPROGRAMMABLE UNITS

Visual inspection at 200X prior to encapsulation, test fuses and decoding circuitry tests are used to guarantee a high programming yield of the devices in the field. However, because of random defects, it is impossible to guarantee that a link will open without actually programming it. **UNITS RETURNED TO RAYTHEON AS UNPROGRAMMABLE MUST BE ACCOMPANIED BY A COMPLETE DEVICE TRUTH TABLE WITH THE LOCATION WHICH CANNOT BE PROGRAMMED, OR WHICH FALSELY PROGRAMMED, CLEARLY INDICATED.**

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T_R 0.4 V/μs ±15%
T_{pp} 95 ±15 μs
T_p 1 μs min., 8 μs max.
T_{D_1} 80 ±10 μs
T_{D_2} 100 ns min.

NOTE: Output Load = 0.2 mA during 6.0V check
Output Load = 12 mA during 4.2V check

Figure 1. Program Timing

TRUTH TABLES

Raytheon can program devices at our facility from Raytheon truth table forms (available on request). For customers desiring to make their own forms, an example is shown below for a 256 x 4 device.

		OUTPUTS			
WORD NUMBER	PIN ⟶	9 O_4	10 O_3	11 O_2	12 O_1
0		H	H	H	L
1		L	H	L	H
.		.	.	.	.
.		.	.	.	.
255		L	H	H	H

Note: A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pins, so for example, word 255 = HHHHHHHH.

PAPER TAPE FORMAT

Truth tables can also be sent to Raytheon in an ASCII tape format. Information can be sent to us by air mail or TWX 910-379-6481. The tape reading equipment at Raytheon only recognizes ASCII characters S, B, P, N, F, and E and interprets them as:

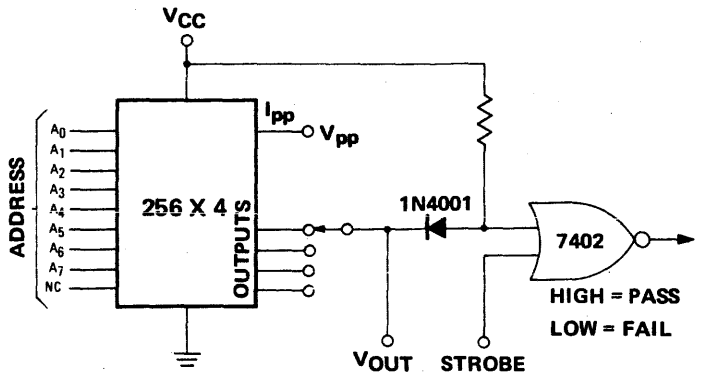
S	Start
B	Begin a word
P	High data
N	Low data
F	Finish a word
E	End of tape

All other characters such as carriage returns, line feeds, etc. are ignored so that comments and spaces may be sent in the data field to improve readability. Comments, however, should not use the characters S, B, P, N, F, and E. Word addresses must begin with zero and count sequentially to word the maximum number of words.

In order to assist the machine operator in determining where the heading information stops and the data field begins, 25 bell characters or rubout characters should precede the start of the truth table. Any type of 8 level paper tape (mylar, fanfold, etc.) is acceptable. Channel 1 is the most significant bit and channel 8 (parity) is ignored. Sprocket holes are located between channels 3 and 4. Note that the output between characters B and F starts with the most significant bit and ends with the least significant bit.

A typical list of characters and their machine interpretations are shown on the next page.

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Suggested Implementation of the Verification Circuitry

Notes:

1. For proper threshold adjustment, insert a 2N404 germanium transistor with collector and emitter shorted so that it looks like a diode in series with pin 7 of the 7402 to ground.
2. The 1N4001 diode protects the input of the 7402 from the high programming voltages.

X 4 Example

BEGIN DATA FIELD
DATA FIELD (H = HIGH VOLTAGE, L = LOW)
FINISHED DATA FIELD

B P P N P F B P P P P F B P N N P F – – – B P N N N F (etc)

O_4 O_3 O_2 O_1

WORD 0 WORD 1 WORD 2 WORD 511

X 8 Example

BEGIN DATA FIELD
DATA FIELD (H = HIGH VOLTAGE, L = LOW VOLTAGE)
FINISHED DATA FIELD

B P P P N P P N P F BPPPPPPPPF BPNPPPNNPF – – – BPPNPPNNNF (etc)

O_8 O_7 O_6 O_5 O_4 O_3 O_2 O_1

WORD 0 WORD 1 WORD 2 WORD 255

The required heading information at the beginning of the tape is as follows:

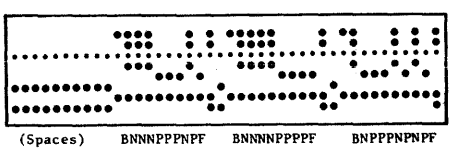
Customer name and phone_____ Truth table number_____
Customer TWX number_____ Number of truth tables_____
Purchase order number_____ Total number of parts_____
Raytheon part number_____ Number of parts of each truth table_____
Customer symbolized part number_____ 25 bell or rubout characters_____

An example is shown below:

BLARNEY ELECTRONICS 408-735-8140
TWX 911-338-9225
P0142
29601

BNNNPPPNPF BNNNNPPPPF BNPPPNPNPF BNNNNNNNNF BNNNNNNNNF BNNNNNNNNF BNNNNNNNNF BNNNNNNNNF
BNNNNNNNNF BNNNPPPNPF BPPPPPPPPF BNPPNPNNNF BNPPPNNNPF BNNNNNNNNF BPPPPPPPPF BNNNNNPPF

8 LEVEL TWX



Interpretation: (Spaces) BNNNPPPNPF BNNNNPPPPF BNPPPNPNPF

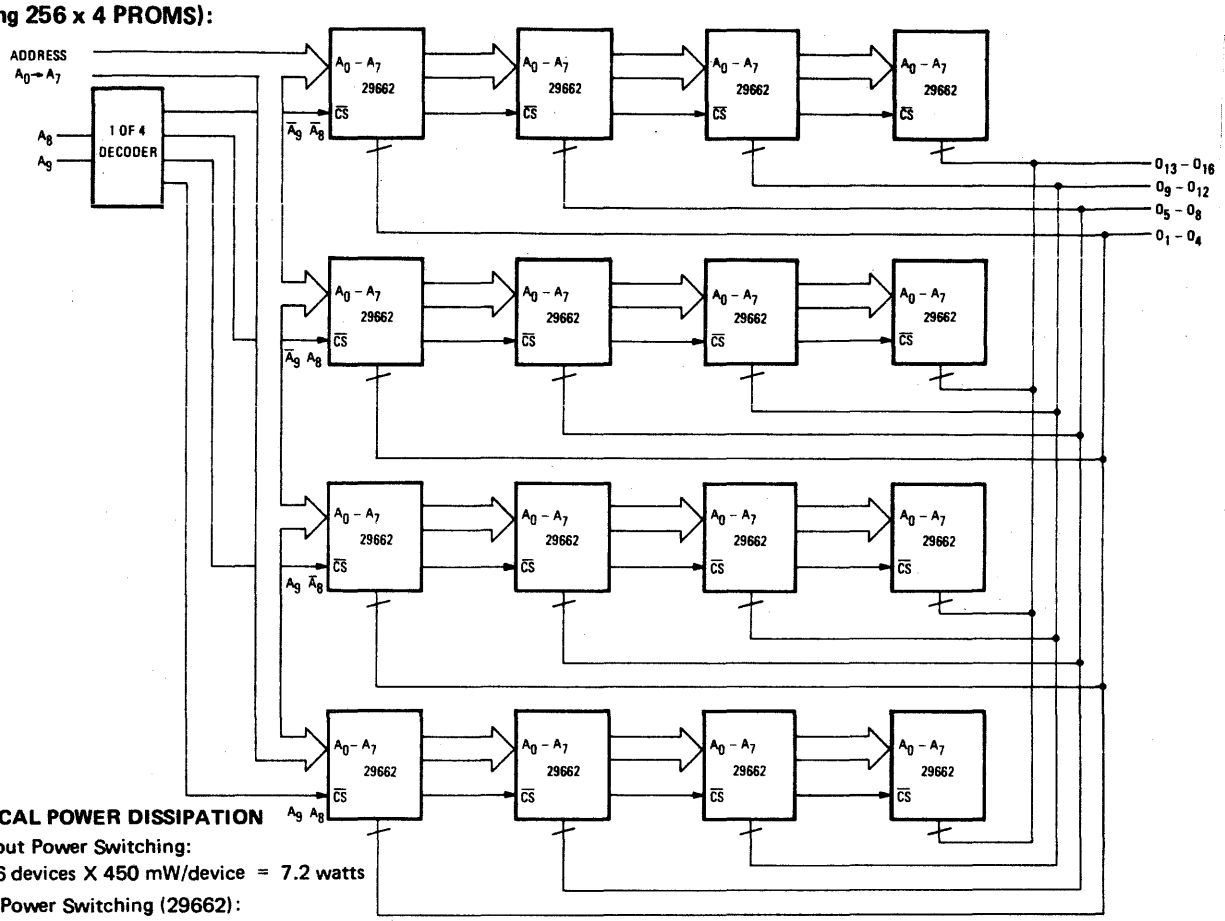
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PROGRAMMING PARAMETERS — Do not test these limits or you may program the device.

SYMBOL	PARAMETER	TEST CONDITIONS (See Figure 4)	LIMITS MIN.	LIMITS TYPICAL OR OPTIMUM	LIMITS MAX.	UNITS
I_{pp}	Current program pin during programming. Before and after fuse has blown	V_{CC} = 5.50V V_{out} = 5.0 to 25V V_{pp} = 4.50V		0		mA
		V_{pp} = 27V		77		mA
I_{out}	Current into output during programming before the fuse has programmed	V_{pp} = 27V, V_{CC} = 5.50V V_{out} = 9.0V		0.1		mA
		V_{out} = 20V		16		mA
I_{out}	Current into output during programming after the fuse has programmed.	V_{pp} = 27V, V_{out} = 20V V_{CC} = 5.50V		0.1		mA
T_R	Rise time of program pulse applied to the data out or program pin.		0.34	0.4	0.46	V/μs
V_{CCP}	V_{CC} required during programming.		5.40	5.50	5.60	V
I_{OLV1}	Output current required during verification.	Both chip enables low T_A = 25°C, V_{CC} = 4.2V	11	12	13	mA
I_{OLV2}	Output current required during verification.	Both chip enables low T_A = 25°C, V_{CC} = 6.0V	0.19	0.2	0.21	mA
MDC	Maximum duty cycle during automatic programming of program pin and output pin.	$\frac{T_P}{T_C}$			25	%
V_{pp}	Required programming voltage on program pin.		27	27	33	V
V_{out}	Required programming voltage on the output pin		20	20	26	V
I_L	Required current limit of the power supply feeding the program pin and and the output during programming.	V_{pp} = 33V V_{out} = 26V V_{CC} = 5.50V	150			mA
T_{pp}	Required coincidence among the program pin, output, address and V_{CC} for programming.		80	95	110	μs
T_{D1}	Required time delay between disabling the memory output and application of the output programming pulse.	Measure at 10% levels	70	80	90	μs
T_{D2}	Required time delay between removal of programming pulse and enabling the memory output.	Measure at 10% levels	100			nS

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1024 X 16 BIT PROM ARRAY APPLICATION:
(Using 256 x 4 PROMS):



TYPICAL POWER DISSIPATION

Without Power Switching:

16 devices X 450 mW/device = 7.2 watts

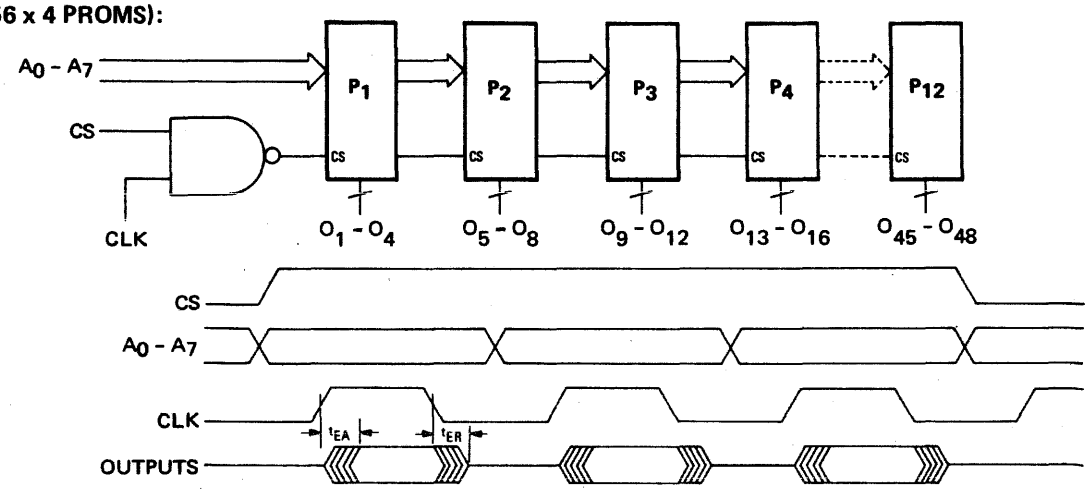
With Power Switching (29662):

4 devices X 450 mW/device = 1.8 watts

12 devices X 100 mW/device = 1.2 watts

Total Power = 3.0 watts

256 X 48 BIT CLOCKED PROM APPLICATION:
(Using 256 x 4 PROMS):



TYPICAL POWER DISSIPATION

Without Power Switching:

12 devices X 450 mW/device = 5.4 watts

With Power Switching (29662 and 50% duty cycle clock):

(0.5 X 12 devices X 450 mW/device) + (0.5 X 12 devices X 100 mW/device) = 3.3 watts

With Power Switching (29662 and 20% duty cycle clock):

(0.2 X 12 devices X 450 mW/device) + (0.8 X 12 devices X 100 mW/device) = 2.04 watts

RAYTHEON

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INTRODUCTION TO MICROPROCESSORS

This section briefly describes microprocessors from 26 manufacturers. It gives you a list of system components (pages 1504-1513) followed by detailed information from the manufacturers on key products (pages 1537-1927).

The extent of information, support, and applications assistance available from manufacturers is an important factor in selecting microprocessors. Therefore, the detailed facts presented in the system descriptions include hardware and software items. The descriptions indicate whether complete operating cards are offered and indicate if "prototyping systems" or developmental operating systems are available. The listings also cover the availability of "in-system emulators." These units are usually black boxes that look to the system like a real time IC device. But by using them the designer can modify the program and can effectively gain access to what would be interior portions of the integrated circuit to test, analyze, and debug the microprocessor while it is connected to the system.

INDEX TO MICROPROCESSOR SYSTEMS SECTION

Manufacturers	Pages Start On:	Manufacturers	Pages Start On:
AMD	1514	Motorola	1523
AMI	1514, **1537**	**National Semiconductor**	1524, **1656**
Data General	1515	NEC	1526, **1727**
Essex	1515	Panasonic	1528
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MICROPROCESSOR–System Components

This section presents the major microprocessor system devices organized into system groups, ie F8, 6800, 8080, etc. It includes those RAM's, ROM's and PROM's which are unique to a system. It omits most general purpose memories as they are listed in the Memory section. Similarly, buffers, line drivers, transceivers, UART's, etc. are covered briefly here as they are presented in depth in the Digital and Interface sections.

μCOM-4

Function	Device	Source		Line
Microcomputer				
	μCOM-42	**NEC Micro**	**(1727)**	10
	μPD548	**NEC Micro**	**(1727)**	
	μCOM-43	**NEC Micro**	**(1727)**	
	μPD546	**NEC Micro**	**(1727)**	
	μCOM-44	**NEC Micro**	**(1727)**	
	μPD547	**NEC Micro**	**(1727)**	
	μCOM-45	**NEC Micro**	**(1727)**	
	μPD550	**NEC Micro**	**(1727)**	
Evaluation Devices				
	μPD555	**NEC Micro**	**(1727)**	20
	μPD556	**NEC Micro**	**(1727)**	

F8

Function	Device	Source		Line
Central Processing Unit				
	3850	**Fairchild**	**(1606)**	
	3850M	**† Fairchild**	**(1606)**	
	F8	Fairchild		
	MK3850	Mostek		
	3850	SGS		
Program Storage Unit				
	3851	**Fairchild**	**(1606)**	
	3851M	**† Fairchild**	**(1606)**	30
	3856	**Fairchild**	**(1608)**	
	3857	**Fairchild**	**(1608)**	
	MK3851	Mostek		
	3851	SGS		
Microcomputer (1 chip)				
	3870	Fairchild		
	MC3870	Motorola		
	MK3870	Mostek		
Direct Memory Access				
	3854	**Fairchild**	**(1607)**	40
	MK3854	Mostek		
Peripheral Input/Output Interface				
	3861	**Fairchild**	**(1609)**	
	3861M	† Fairchild		
	3871	**Fairchild**	**(1609)**	
	MK3861	Mostek		
	MK3871	Mostek		
Analog input, MUX, A/D converter				
	MP21	Burr-Brown		
Dynamic Memory Interface				50
	3852	**Fairchild**	**(1607)**	
	MK3852	Mostek		
Static Memory Interface				
	3853	**Fairchild**	**(1607)**	
	3853M	† Fairchild		
	MK3853	Mostek		
Development System				
	Formulator	**Fairchild**	**(1594)**	

IMP

Function	Device	Source		Line
Control Read Only Memory (CROM)				
	IMP-8A/520	National		60
	(Continued)			

IMP (Cont'd)

Function	Device	Source		Line
Control Read Only Memory (CROM) (Cont'd.)				
	IMP-16	**National**	**(1656)**	
	IMP-16A/521	National		
	IMP-16A/522	National		
	IMP-16A/523	National		
	IMP-16A/524	National		
Register, Arithmetic and Logic Unit (RALU)				
	IMP-00A/520	**National**	**(1656)**	
Development System				
	LCDS	**National**	**(1656)**	70

Macrologic Bipolar

Function	Device	Source		Line
Microprogram Sequencer				
	9408C	**Fairchild**	**(1625)**	
	9408AC	Fairchild		
	9408M	**† Fairchild**	**(1625)**	
	9408AM	† Fairchild		
Arithmetic Logic Register Stack				
	9405C	Fairchild		
	9405AC	**Fairchild**	**(1620)**	
	9405M	† Fairchild		
	9405AM	**† Fairchild**	**(1620)**	80
Data Path Switch (for closing data path loops around arithmetic/logic networks such as 9405)				
	9404C	Fairchild		
	9404M	† Fairchild		
Data Access Register (performs memory address arithmetic)				
	9407C	Fairchild		
	9407M	† Fairchild		
Buffer (16x4 First In First Out Memory. See also Memory FIFO's)				
	9403C	**Fairchild**	**(1613)**	90
	9403M	**† Fairchild**	**(1613)**	
Buffer (64x4 First In First Out Memory. See also Memory FIFO's)				
	9423C	Fairchild		
	9423M	† Fairchild		
Data Encryption, 4 device set				
	9414	Fairchild		
	9415	Fairchild		
	9416	Fairchild		100
	9417	Fairchild		
Display Controller				
	9412C	Fairchild		
	9412M	† Fairchild		
Program Stack (16x4 LIFO memory)				
	9406C	Fairchild		
	9406M	† Fairchild		
CRC Generator/Checker (See also Interface Error Checking Circuits)				
	9401C	Fairchild		110
	9401M	† Fairchild		
	9411C	Fairchild		
	9411M	† Fairchild		
RAM (16x4) Write while Read (See also Digital TTL Memories)				
	9410C	Fairchild		
	9410M	† Fairchild		

Macrologic CMOS

Function	Device	Source		Line
Arithmetic Logic Register Stack				
	F4705BC	Fairchild		
	F4705BM	† Fairchild		120
Data Path Switch (for closing data path loops around arithmetic/logic networks such as the F4705)				
	F4704BC	Fairchild		
	F4704BM	† Fairchild		
Data Access Register (performs memory address arithmetic)				
	F4707BC	Fairchild		
	F4707BM	† Fairchild		130
Microprogram Sequencer				
	F4708C	Fairchild		
	F4708M	† Fairchild		
Parallel/Serial First In First Out Memory (FIFO) (See also Memory FIFO's)				
	F4703BC	Fairchild		
	F4703BM	† Fairchild		
Program Stack (16x4 LIFO Memory)				
	F4706BC	Fairchild		
	F4706BM	† Fairchild		
Programmable Bit Rate Generator (See also Digital CMOS Miscellaneous Bit Rate Generator)				140
	F4702BC	Fairchild		
	F4702BM	† Fairchild		
	HD4702-2	**Harris**	**(1634)**	
	HD4702-9	**† Harris**	**(1634)**	
RAM (16x4, clocked) Write while Read (See also Digital CMOS Memories)				
	F4710BC	Fairchild		
	F4710BM	† Fairchild		
RAM (16x4) (See also Memory RAM's)				
	F4725BC	Fairchild		150
	F4725BM	† Fairchild		
RAM (256x1) (See also Memory RAM's)				
	F4720C	Fairchild		
	F4720M	† Fairchild		
RAM (256X4) (See also Memory RAMS)				
	F4726BC	Fairchild		
	F4726BM	† Fairchild		
ROM (256X8) (See also Memory ROMS)				
	F4735BC	Fairchild		
	F4735BM	† Fairchild		160

MicroNOVA

Function	Device	Source	Line
CPU			
	MN601	Data General	
	MICRONOVA	Data General	
I/O Transceiver			
	MN629	Data General	
I/O Transceiver Buffer			
	MN636	Data General	
Memory Bus Transceiver, Octal			
	MN634	Data General	
Intelligent I/O Controller			170
	MN603	Data General	
Memory Address Driver			
	MN633	Data General	
RAM (4096x1)			
	MN606	Data General	
Sense Amplifier (for MN606)			
	MN506	Data General	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

MICROPROCESSOR–System Components (Cont'd)

M380

Function	Device	Source
CPU		
	M38	SGS
	M380	SGS
RAM/ROM/I/O		
	M381	SGS
RAM/I/O		
	M383	SGS
ROM/I/O		
	M382	SGS

PACE/INS8900

Function	Device	Source	
CPU			
	INS8900	**National**	**(1702)**
Processing and Control Element (CPU)			
	PACE	**National**	**(1656)**
	IPC-16A/500	National	
	IPC-16A/520	**National**	**(1656)**
Bidirectional Transceiver Element (BTE)			
	DP8300	**National**	**(488)**
Bidirectional Bus Transceiver			
	DP8304	**National**	**(501)**
Octal Bus Transceiver			
	IDM8208	National	
Interface Latch Elements (ILE)			
	DP8301	National	
System Timing Element (STE)			
	DP8302	**National**	**(496)**
	DP8305	National	
CMOS Clock			
	MM74C04	National	
Erasable PROM (See also Memory PROM's MM5204)			
	IPC-16A/506	National	
RAM (256x4) (See also Memory RAM's, MM5269)			
	IPC-16A/504	National	
Development System			
	LCDS	**National**	**(1656)**

PPS-4, PPS-8

Function	Device	Source
CPU (for PPS 4)		
	12660	Rockwell
ROM RAM (for PPS 4)		
	A07XX	Rockwell
	A08XX	Rockwell
	A20XX	Rockwell
CPU (for PPS 4/1)		
	75XX	Rockwell
	76XX	Rockwell
	77XX	Rockwell
CPU Evaluation Circuit (for PPS 4/1)		
	6799	Rockwell
CPU (for PPS 4/2)		
	11600	Rockwell
ROM RAM (for PPS 4/2)		
	A17XX	Rockwell
CPU (for PPS 8)		
	11806	Rockwell
CPU (for PPS 8/2)		
	12806	Rockwell
ROM RAM (for PPS 8/2)		
	A21XX	Rockwell

PPS-4, PPS-8 (Cont'd)

Function	Device	Source
Bus Interface Circuit (BIC)		
	10738	Rockwell
Clock Generator (CLK) (for PPS 4, PPS 8)		
	10706	Rockwell
Direct Memory Access Controller (DMA) (for PPS 8)		
	10817	Rockwell
Display Controller (DC)		
	10814	Rockwell
Floppy Disk Controller (FDC) (for PPS 8)		
	10936	Rockwell
General Purpose Keyboard and Display Control (GPKD)		
	10788	Rockwell
General Purpose Input/Output (GPI/O)		
	10696	Rockwell
Interval Timer		
	11049	Rockwell
Keyboard/Printer Controller (KPC)		
	10815	Rockwell
Printer Controller (PC)		
	10789	Rockwell
Victor Dot Matrix Printer Controller (VPC)		
	10736	Rockwell
	15380	Rockwell
Parallel Data Controller (PDC) (for PPS 8, PPS 8/12)		
	10453	Rockwell
Serial Data Controller (SDC)		
	10930	Rockwell
Telecommunications Data Interface (includes modem)		
	10371	Rockwell
RAM (256x4) (for PPS 4, PPS 4/2)		
	10432	Rockwell
RAM (512x4) (for PPS 4, PPS 4/2)		
	10932	Rockwell
RAM (256x8) (for PPS 8, PPS 8/2)		
	10809	Rockwell
4K RAM Interface		
	10929	Rockwell
RAM (4096x1) (See also Memory RAM's)		
	1604-8	Rockwell
ROM (1024x8)		
	A05XX	Rockwell
ROM (2048x8)		
	A52XX	Rockwell
ROM (4096x8)		
	A66XX	Rockwell

SBA

Function	Device	Source
Sequential Boolean Analyzer		
	SBA	GI

SBP0400

Function	Device	Source
CPU, 4 Bit Slice		
	SBP0400AC	TI
	SBP0400AM	†TI
	SBP0401AC	TI
	SBP0401AM	†TI
4 Bit Slice Control Element		
	SN54S482	†TI

(Continued)

SBP0400 (Cont'd)

Function	Device	Source
4 Bit Slice Control Element (Cont'd.)		
	SN74S482	TI

SC/MP

Function	Device	Source	
Microprocessor			
	SC/MP	**National**	**(1656)**
	ISP-8A/500	National	
	ISP-8A/600	**National**	**(1692)**
	SC/MP	Signetics	
	ISP-8A/600	Signetics	
8 Bit I/O Port			
	INS8212	**National**	**(469)**
Analog Input, Multiplexer, A/D Converter			
	MP20	Burr-Brown	
Bit Programmable I/O			
	INS8254	National	
Programmable Communication Interface (USART. See also Interface Transmitters Receivers)			
	INS8251	National	
Programmable Peripheral Interface			
	INS8255	National	
ROM/RAM and I/O			
	INS2656	National	
RAM(128x8) and I/O			
	INS8154	National	
	ISP-8A/650	National	
Development System			
	LCDS	**National**	**(1656)**

SX200

Function	Device	Source
Microcomputer		
	SX200	Essex

TLCS-12

Function	Device	Source
CPU		
	T3190	Toshiba
Input/Output Control Unit		
	T3218	Toshiba
General Purpose Input/Output Register		
	T3320	Toshiba
Memory Control Unit		
	T3216	Toshiba
Erasable PROM		
	T3181	Toshiba
RAM (128x4)		
	T3151	Toshiba

W40

Function	Device	Source
Microcontroller		
	CR1872	Western
	CR2872	Western

Z80

Note: the 6500, 6800 and 8080 peripheral circuits are compatible with the Z80 series.

Function	Device	Source	
CPU			
	MK3880	Mostek	
	μPDZ-80	**NEC Micro**	**(1850)**

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

MICROPROCESSOR–System Components (Cont'd)

Z80 (Cont'd)

Function	Device	Source
CPU (Cont'd.)		
	Z80-CPU	Zilog
Counter Timer Circuit		
	MK3882	Mostek
	Z80-CTC	Zilog
Direct Memory Access Controller		
	MK3883	Mostek
	Z80-DMA	Zilog
Parallel Input/Output Controller		
	MK3881	Mostek
	Z80-PIO	Zilog
Serial Input/Output Controller		
	MK3884	Mostek
	Z80-SIO	Zilog
Analog Input, Multiplexer, A/D Converter		
	MP20	Burr-Brown
Development System		
	8001	**Tektronix (1916)**
	8002	**Tektronix (1916)**

1000

Microcomputer		
	TMS1000	TI
	TMS1070	TI
	TMS1100	TI
	TMS1200	TI
	TMS1270	TI
	TMS1300	TI
Program Development Device (uses external memory)		
	TMS1098	TI
	TMS1099	TI

1400

Microcomputer		
	MN1400	Panasonic
	MN1402	Panasonic
Microcomputer, external memory		
	MN1498	Panasonic
Microcomputer, evaluator		
	MN1499	Panasonic

1600

See also 1600 below.		
Microcomputer		
	CP-1600	GI
	CP-1610	GI
	PIC1650	GI
Microcomputer Development Device		
	PIC1664	GI
Dual D/A Converter (two 10 bit pulse width modulated outputs)		
	DAC1600	GI
18 Channel Analog Multiplexer		
	MUX1600	GI
Input/Output Buffer		
	IOB1680	GI

1600

See also 1600 above.		
CPU, 8 Bit		
	CP1651	Western
	CP1661	Western
CPU, 16 Bit		
	MP1651	Western
	MP1661	Western
General Purpose Input/Output		
	CP1851	Western
Microm		
	CP1631	Western
Direct Memory Access Controller		
	DM1881	Western
	DM1883	Western
Floppy Disc Controller/Transmitter		
	INS1771	National
	FD1771	Western
	FD1781	Western
Asynchronous/Synchronous Transmitter/Receiver (ASTRO) (See also Interface Serial Transmitters Receivers)		
	INS1671	National
	COM1671	SMC
	UC1671	Western
	UC1971	Western

1800

CPU		
	HCMP1802	†Hughes
	HCMP1802C	†Hughes
	CDP1802	†RCA
	CDP1802C	†RCA
8 Bit Input/Output Port		
	HCMP1852	†Hughes
	CDP1852	†RCA
4 Bit Buffer/Separator (for memory interface)		
	HCMP1856	†Hughes
	CDP1856	†RCA
4 Bit Bus Buffer/Separator (for I/O interface)		
	HCMP1857	†Hughes
	CDP1857	†RCA
N Bit Decoder (for I/O interface)		
	HCMP1853	†Hughes
	CDP1853	†RCA
4 Bit Latch with 1 of 4 Decoder		
	HCMP1858	†Hughes
	CDP1858	†RCA
4 Bit Latch with dual 1 of 4 Decoders		
	HCMP1859	†Hughes
	CDP1859	†RCA
UART		
	HCMP1854	†Hughes
	CDP1854	RCA
	CDP1854A	†RCA
Video Display Controller		
	CDP1861	†RCA
RAM (32x8) (See also Memory RAM's)		
	HCMP1824	†Hughes
	CDP1824	†RCA
RAM (128x8) (See also Memory RAM's)		
	CDP1823S	RCA

1800 (Cont'd)

RAM (256x4) (See also Memory RAM's)		
	CDP1822S	RCA
RAM (1024x1) (See also Memory RAM's)		
	CDP1821S	RCA
ROM (512x8) (See also Memory ROM's)		
	HCMP1831	†Hughes
	HCMP1832	†Hughes
	CDP1831	†RCA
	CDP1832	†RCA
ROM (1024x8) (See also Memory ROM's)		
	HCMP1833	†Hughes
	HCMP1834	†Hughes
	CDP1833	†RCA
	CDP1834	†RCA

2000

Microcomputer		
	S2000	**AMI (1571)**
Development System		
	MDC-140	**AMI (1540)**

2650

Microprocessor		
	INS2650A	**National (1656)**
	2650	Signetics
	2650A	Signetics
Hex Buffers/Inverters (See also Digital TTL Buffers/Inverters 8T95, 8T96, 8T97, 8T98)		
	MC8T95	Motorola
	MC8T96	Motorola
	MC8T97	Motorola
	MC8T98	Motorola
	N8T95	Signetics
	N8T96	Signetics
	N8T97	Signetics
	N8T98	Signetics
Bidirectional Port, Latched		
	N8T31	**Signetics (1898)**
Programmable Communication Interface		
	INS2651	National
	2651	Signetics
Multi Protocol Communications Circuit (includes SDLC, BiSync)		
	INS2652	National
	2652	Signetics
Programmable Peripheral Interface		
	INS2655	National
	2655	Signetics
System Memory Interface (RAM, ROM, I/O, Timer)		
	INS2656	National
	2656	Signetics
Quad Transceivers (See also Interface Line Transceivers)		
	N8T26	AMD
	MC8T26	Motorola
	MC8T28	Motorola
	N8T26	Signetics
	N8T28	Signetics
Field Programmable Logic Array (See also Memory PLA's)		
	N82S100	Signetics
	N82S101	Signetics

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

MICROPROCESSOR–System Components (Cont'd)

Function	Device	Source	Line
2900			
Microprocessor, 4 Bit Slice			
	AM2901C	AMD	
	AM2901M	† AMD	
	AM2901AC	AMD	
	AM2901AM	† AMD	
	AM2903C	AMD	
	AM2903M	† AMD	
	F2901AC	Fairchild	
	F2901AM	† Fairchild	
	9409	Fairchild	
	MC2901C	Motorola	10
	MC2901M	† Motorola	
	IDM2901AC	**National (1680)**	
	IDM2901AM	**† National (1680)**	
	μPB2901	**NEC Micro (1850)**	
	AM2901C	Raytheon	
	AM2901M	† Raytheon	
	AM2901AC	Raytheon	
	AM2901AM	† Raytheon	
	N2901-1	**Signetics (1851)**	
Look Ahead Carry Generator			20
	AM2902C	AMD	
	AM2902M	† AMD	
	MC2902C	Motorola	
	MC2902M	† Motorola	
	IDM2902C	National	
	IDM2902M	† National	
	μPB2902C	**NEC Micro (1850)**	
	AM2902C	Raytheon	
	AM2902M	† Raytheon	
Microprogram Sequencer			30
	AM2909C	AMD	
	AM2909M	† AMD	
	AM2911C	AMD	
	AM2911M	† AMD	
	MC2909C	Motorola	
	MC2909M	† Motorola	
	MC2911C	Motorola	
	MC2911M	† Motorola	
	IDM2909AC	National	
	IDM2909AM	† National	40
	IDM2911AC	National	
	IDM2911AM	† National	
	μPB2909	**NEC Micro (1850)**	
	μPB2911	**NEC Micro (1850)**	
	AM2909C	Raytheon	
	AM2909M	† Raytheon	
	AM2911C	Raytheon	
	AM2911M	† Raytheon	
Macroprogram Sequencer			
	AM2919C	AMD	50
	AM2919M	† AMD	
Control Store Sequencer			
	8X02	**Signetics (1877)**	
16 Way Branch Control Unit (use with 2909)			
	AM29803C	AMD	
	AM29803M	† AMD	
	IDM29803C	National	
	IDM29803M	† National	
Next Address Control Unit (use with 2911)			
	AM29811C	AMD	60
	AM29811M	† AMD	
	IDM29811C	National	
	IDM29811M	† National	
Priority Interrupt Encoder, Vectored			
	AM2914C	AMD	
	AM2914M	† AMD	

Function	Device	Source	Line
2900 (Cont'd)			
Priority Interrupt Expander (for 2914)			
	AM2913C	AMD	
	AM2913M	† AMD	
Priority Encoder			70
	IDM29902C	National	
	IDM29902M	† National	
Programmable Multiplexer, 10 inputs, four 10x8 field programmable arrays, four 8:1 addressable multiplexers, four outputs			
	29693C	**Raytheon (1494)**	
	29693M	**† Raytheon (1494)**	
Bus Transceivers (See also Interface Line Transceivers)			
	AM2905C	AMD	80
	AM2905M	† AMD	
	AM2906C	AMD	
	AM2906M	† AMD	
	AM2907C	AMD	
	AM2907M	† AMD	
	AM2915C	AMD	
	AM2915M	† AMD	
	AM2916C	AMD	
	AM2916M	† AMD	
	AM2917C	AMD	90
	AM2917M	† AMD	
	MC2905C	Motorola	
	MC2905M	† Motorola	
	MC2906C	Motorola	
	MC2906M	† Motorola	
	MC2907C	Motorola	
	MC2907M	† Motorola	
	MC2915C	Motorola	
	MC2915M	† Motorola	
	MC2916C	Motorola	100
	MC2916M	† Motorola	
	MC2917C	Motorola	
	MC2917M	† Motorola	
	μPB2905	**NEC Micro (1850)**	
	μPB2906	**NEC Micro (1850)**	
	μPB2907	**NEC Micro (1850)**	
	μPB2915	**NEC Micro (1850)**	
	μPB2916	**NEC Micro (1850)**	
	μPB2917	**NEC Micro (1850)**	
	AM2905C	Raytheon	110
	AM2905M	† Raytheon	
	AM2906C	Raytheon	
	AM2906M	† Raytheon	
	AM2907C	Raytheon	
	AM2907M	† Raytheon	
8 Input Multiplexer, with control storage			
	AM2922C	AMD	
	AM2922M	AMD	
Quad D Register with both Standard and Three State Outputs (See also Digital TTL Flip Flops)			120
	AM2918C	AMD	
	AM2918M	† AMD	
	MC2918C	Motorola	
	MC2918M	† Motorola	
	μPB2918	**NEC Micro (1850)**	
	AM2918C	Raytheon	
	AM2918M	† Raytheon	
Octal D type Flip Flop, three state			
	IDM29901C	National	
	IDM29901M	† National	130
PROM (32x8) (See also Memory PROM's)			
	AM29750C	AMD	
	AM29750M	† AMD	
	(Continued)		

Function	Device	Source	Line
2900 (Cont'd)			
PROM (32x8) (See also Memory PROM's) (Cont'd.)			
	AM29751C	AMD	
	AM29751M	† AMD	
	IDM29750C	National	
	IDM29750M	† National	
	IDM29751C	National	
	IDM29751M	† National	140
PROM(256x4) (See also Memory PROMs)			
	AM29760C	AMD	
	AM29760M	† AMD	
	AM29761C	AMD	
	AM29761M	† AMD	
	IDM29760C	National	
	IDM29760M	† National	
	IDM29761C	National	
	IDM29761M	† National	
RAM (16x4) Two output ports			150
	AM29704C	AMD	
	AM29704M	† AMD	
	AM29705C	AMD	
	AM29705M	† AMD	
RAM (16x4) (See also Memory RAM's)			
	AM29700C	AMD	
	AM29700M	† AMD	
	AM29701C	AMD	
	AM29701M	† AMD	
	AM29702C	AMD	160
	AM29702M	† AMD	
	AM29703C	AMD	
	AM29703M	† AMD	
	IDM29702C	National	
	IDM29702M	† National	
	IDM29703C	National	
	IDM29703M	† National	
	IDM29903C	National	
RAM (256x1) (See also Memory RAM's)			
	AM29720C	AMD	170
	AM29720M	† AMD	
	AM29721C	AMD	
	AM29721M	† AMD	
ROM(256x8)			
	IDM29904C	National	
	IDM29904M	† National	
	IDM29905C	National	
	IDM29905M	† National	
ROM(256x8), with latches			
	IDM29907C	National	180
	IDM29907M	† National	
ROM (1024x8) (See also Memory ROM's)			
	AM29882C	AMD	
	AM29883C	AMD	
3000			
Central Processing Element, 2 Bit slice			
	3002	Intel	
	M3002	† Intel	
	N3002	**Signetics (1868)**	
	S3002	**† Signetics (1868)**	
Microprogram Control Unit			190
	3001	Intel	
	M3001	† Intel	
	N3001	**Signetics (1860)**	
	S3001	**† Signetics (1860)**	
Parallel Bidirectional Bus Driver			
	3216	Intel	
	(Continued)		

† Military Temperature Range (−55° to 125°C)

* Typical Values

MICROPROCESSOR–System Components (Cont'd)

3000 (Cont'd)

Function	Device	Source	
Parallel Bidirectional Bus Driver (Cont'd.)			
	M3216	†Intel	
	3226	Intel	
	M3226	†Intel	
Interrupt Control Unit			
	3214	Intel	
	M3214	†Intel	
Look Ahead Carry Generator			
	3003	Intel	
	M3003	†Intel	
Multimode Latch Buffer			
	3212	Intel	
	M3212	†Intel	
Development System			
	Intellec MDS	**Intel**	**(1640)**

4004/4040

Function	Device	Source	
CPU			
	4004	Intel	
	4040	Intel	
	INS4004	**National**	**(1656)**
Clock Generator			
	4201	Intel	
	INS4201	**National**	**(465)**
Programmable General Purpose I/O			
	4265	Intel	
Programmable Keyboard/Display Device			
	4269	Intel	
Standard Memory and I/O Interface			
	4008	Intel	
	4009	Intel	
	4289	Intel	
	INS4008	National	
	INS4009	National	
10 Bit Shift Register/Output Expander			
	4003	Intel	
	INS4003	National	
Erasable PROM (256x8) (See also Memory PROM's, 1702A)			
	4702	AMD	
	4702A	Intel	
	INS4702	National	
320 Bit RAM and 4 Bit Output Port			
	4002	Intel	
	INS4002	National	
RAM (256x4) (See also Memory RAM's, 2101 series)			
	4101	Intel	
ROM (256x8) and 4 Bit I/O Port			
	4001	Intel	
	INS4001	National	
ROM (1024x8) and I/O Ports			
	4308	Intel	
ROM (2048x8) (See also Memory ROM's, 2316A)			
	4316A	Intel	

54/74LS481, 54/74S481

Function	Device	Source	
4 Bit Microprocessor Slice			
	SN54LS481	†TI	
	SN74LS481	TI	
	SN74S481	TI	

54/74LS481, 54/74S481 (Cont'd)

Function	Device	Source	
Control Element (for next address generators)			
	SN54S482	†TI	
	SN74S482	TI	
Field Programmable Logic Array			
	SN54S330	†TI	
	SN74S330	TI	
	SN54S331	†TI	
	SN74S331	TI	
FIFO (See also Memory FIFO's)			
	SN74S225	TI	
Erasable PROM (512x8) (See also Memory PROM's)			
	SN54S472	†TI	
	SN74S472	TI	
RAM (256x4) (See also Memory RAM's)			
	SN54S208	†TI	
	SN74S208	TI	

67000

Function	Device	Source	
Microcontroller			
	5701	†MMI	
	6701	MMI	
Microprogram Control Unit			
	57110	**†MMI**	**(1654)**
	67110	**MMI**	**(1654)**
FIFO Memory (64x4) (See also Memory FIFO's)			
	57401	**†MMI**	**(1654)**
	67401	**MMI**	**(1654)**
Multiplier (8x8)			
	57558	**†MMI**	**(1652)**
	67558	**MMI**	**(1652)**

5781/82

Function	Device	Source	
Microprocessor			
	MM5782	**National**	**(1656)**
Control ROM (2048x8)			
	MM5781	National	
ROM (Calculator ROM)			
	MM57135	National	
	MM57136	National	
Shift Register Memory (1024 Bit)			
	MM57126	National	
RAM Interface			
	MM5785	National	

5799

Function	Device	Source	
Microprocessor			
	MM5799	National	
	MM57109	National	
	MM57140	National	
Printer Interface			
	MM5788	National	
Oscillator, Decoder, Driver			
	DS8664	National	
RAM Interface			
	MM5785	National	
Shift Register Memory (1024 Bit)			
	MM57126	National	

6100

Function	Device	Source	
CPU, 12 bit			
	HM6100-2	**†Harris**	**(1631)**
	HM6100-9	**†Harris**	**(1631)**
	IM6100C	Intersil	
	IM6100M	†Intersil	
Parallel Interface Element			
	HD6101A-2	**†Harris**	**(1633)**
	HD6101A-9	**Harris**	**(1633)**
	IM6101A	Intersil	
	IM6101AM	†Intersil	
Universal Asynchronous Receiver Transmitter (UART) (See also Interface Serial Transmitters Receivers)			
	HD6402-2	**†Harris**	**(1632)**
	HD6402-9	**Harris**	**(1632)**
	HD6403-2	†Harris	
	HD6403-9	Harris	
	IM6402	Intersil	
	IM6402M	†Intersil	
	IM6403	Intersil	
	IM6403M	†Intersil	
Memory Extension, DMA, Interval Timer, Controller (MEDIC)			
	IM6102A	Intersil	
	IM6102AM	†Intersil	
20 Bit I/O Port			
	IM6103	Intersil	
Programmable Bit Rate Generator (See also Digital CMOS, Bit Rate Generator)			
	HD6405-2	**†Harris**	**(1634)**
	HD6405-9	**Harris**	**(1634)**

6500

Note: The 6500 series is bus compatable with 6800 series devices

Function	Device	Source
CPU		
	MCS6502	MOS
	MCS6503	MOS
	MCS6504	MOS
	MCS6505	MOS
	MCS6506	MOS
	MCS6512	MOS
	MCS6514	MOS
	MCS6515	MOS
	R6502	Rockwell
	R6503	Rockwell
	R6504	Rockwell
	R6505	Rockwell
	R6506	Rockwell
	R6507	Rockwell
	R6512	Rockwell
	R6513	Rockwell
	R6514	Rockwell
	R6515	Rockwell
	SY6502	Synertek
	SY6503	Synertek
	SY6504	Synertek
	SY6505	Synertek
	SY6506	Synertek
	SY6512	Synertek
	SY6513	Synertek
	SY6514	Synertek
	SY6515	Synertek
RAM, ROM, I/O and Interval Timer		
	MCS6530	MOS
	MCS6532	MOS
	R6530	Rockwell

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

MICROPROCESSOR–System Components (Cont'd)

Function	Device	Source	Line
6500 (Cont'd)			
RAM, ROM, I/O and Interval Timer (Cont'd.)			
	R6532	Rockwell	
	SY6530	Synertek	
	SY6532	Synertek	
RAM(128x8), I/O, and Timer			
	R6532	Rockwell	
Analog Input, Multiplexer, A/D Converter			
	MP21	Burr-Brown	
Peripheral Interface Adapter			
	MCS6520	MOS	10
	MCS6522	MOS	
	R6520	Rockwell	
	R6522	Rockwell	
	SY6520	Synertek	
	SY6522	Synertek	
ROM (2048x8) (See also Memory ROM's)			
	R2316A	Rockwell	
	R2316B	Rockwell	
	SY6540	Synertek	
	SY6541	Synertek	20
6800			
Note: The 6800 series is bus compatable with the 6500 series devices.			
CPU			
	S6800	**AMI** (1538,1548)	
	S68A00	**AMI** (1548)	
	S68B00	**AMI** (1548)	
	F6800	Fairchild	
	M6800	Hitachi	
	MC6800	Motorola	30
	MC6800M	†Motorola	
	MC68A00	Motorola	
	MC68B00	Motorola	
CPU (internal clock, 128x8 RAM)			
	F6802	Fairchild	
	MC6802	Motorola	
Priority Interrupt Controller			
	MC6828	Motorola	
	MC8507	Motorola	
Analog Input, Multiplexer, A/D Converter			40
	MP21	Burr-Brown	
Hex Buffers/Inverters (See also Digital TTL Buffers/Inverters 8T95, 8T96, 8T97, 8T98)			
	MC6885	Motorola	
	MC6886	Motorola	
	MC6887	Motorola	
	MC6888	Motorola	
Triple Bidirectional Bus Switch (also MC3449)			
	MC6881	Motorola	
Clock, 2 phase (MC6870/71 from Motorola Component Products Dept., Franklin Park, IL)			50
	MC6870	Motorola	
	MC6871	Motorola	
	MC6875	Motorola	
Clock Buffer			
	MPQ6842	Motorola	
CRT Controller			
	MC6845	Motorola	
Digital Modulator (for differential phase shift keying system)			60
	MC6862	Motorola	

Function	Device	Source	Line
6800 (Cont'd)			
DMA Controller			
	MC6844	Motorola	
Floppy Disc Controller			
	MC6843	Motorola	
Modem			
	F6860	Fairchild	
	MC6860	Motorola	
Programmable Timer			
	F6840	Fairchild	70
	MC6840	Motorola	
	MC6840-1	Motorola	
	MC68A40	Motorola	
	MC68B40	Motorola	
Synchronous Serial Data Adapter (SSDA)			
	MC6852	Motorola	
	MC6852M	†Motorola	
	MC68A52	Motorola	
Synchronous Receiver/Transmitter (UART. See also Interface Serial Transmitters Receivers)			80
	S2350	**AMI** (368,1589)	
Asynchronous Communications Interface Adapter (ACIA)			
	S6850	**AMI** (1567)	
	S68A50	**AMI** (1567)	
	S68B50	**AMI** (1567)	
	F6850	Fairchild	
	MC6850	Motorola	
	MC6850M	†Motorola	90
	MC68A50	Motorola	
	MC68B50	Motorola	
Advanced Data Link Controller			
	F6854	Fairchild	
	MC6854	Motorola	
	MC68A54	Motorola	
	MC68B54	Motorola	
General Purpose Interface Adapter (IEEE 488 bus)			
	F68448	Fairchild	
	MC68448	Motorola	100
	MC68A448	Motorola	
	MC68B448	Motorola	
Peripheral Interface Adapter, (PIA)			
	S6820	**AMI** (1556)	
	S68A21	**AMI** (1556)	
	S68B21	**AMI** (1556)	
	F6820	Fairchild	
	MK6820	Mostek	
	MC6820	Motorola	
	MC6821	Motorola	110
	MC6821M	†Motorola	
	MC68A21	Motorola	
	MC68B21	Motorola	
Bus Transceiver, (The 6880 is also called 8T26 and the 6889 the 8T28, See Interface Transceivers)			
	MC6880	Motorola	
	MC6889	Motorola	
Erasable PROM (512x8) (See also Memory PROM's)			
	S5204A	**AMI** (1057,1591)	120
	S6834	**AMI** (1067,1563)	
Erasable PROM (1024x8) (See also Memory PROM's)			
	MCM68708	Motorola	
	MCM68A708	Motorola	

Function	Device	Source	Line
6800 (Cont'd)			
Memory Controller, Microprocessor to 16K dynamic RAM			
	MC3480	Motorola	
RAM (128x8) (See also Memory RAM's)			
	S6810	**AMI** (1061)	130
	S68A10	**AMI** (1552)	
	S68B10	**AMI** (1552)	
	F6810	Fairchild	
	F68A10	Fairchild	
	MCM6810A	Motorola	
	MCM6810M	Motorola	
	MCM68A10	Motorola	
	MCM68B10	Motorola	
ROM, I/O, Timer			
	F6846	Fairchild	140
	MC6846	Motorola	
ROM (1024x8) (See also Memory ROM's)			
	MCM65308	Motorola	
	MCM6830A	Motorola	
	MCM68A30	Motorola	
	MCM68B30	Motorola	
	MCM68A308	Motorola	
ROM (2048x8) (See also Memory ROM's)			
	S6831	**AMI** (1062,1560)	150
	MC65317	Motorola	
	MC6832	Motorola	
	MCM68A316	Motorola	
Development System			
	MDC-100	**AMI** (1540)	
	MDC-140	**AMI** (1540)	
	8001	**Tektronix** (1916)	
	8002	**Tektronix** (1916)	
8X300			
Microprocessor			
	8X300	**Signetics** (1883)	160
I/O Port, Synchronous, Field Programmable Address			
	N8T32	**Signetics** (1898)	
	N8T33	**Signetics** (1898)	
I/O Port, Asynchronous, Field Programmable Address			
	N8T35	**Signetics** (1898)	
	N8T36	**Signetics** (1898)	
I/O Port, Latched Bidirectional			
	N8T31	**Signetics** (1898)	
Bus Expander, Addressable			
	N8T39	**Signetics** (1909)	170
8000			
Logic Processor			
	LP8000	GI	
Clock Generator			
	LP1030	GI	
Input/Output Buffer			
	LP1010	GI	
Memory Interface			
	LP1000	GI	
Program Memory (1024x8)			
	LP6000	GI	180

† Military Temperature Range (−55° to 125°C)

* Typical Values

MICROPROCESSOR–System Components (Cont'd)

8008

Function	Device	Source	Line
CPU	8008	Intel	
8 Bit I/O Port (See listing under 8080)	8212	Intel	
	μPB8212	**NEC Micro (1804)**	
Bidirectional Bus Driver (See listing under 8080)	8216	Intel	
	8226	Intel	
	μPB8216	**NEC Micro (1810)**	
	μPB8226	**NEC Micro (1810)**	
Analog input, MUX, A/D converter	MP20	Burr-Brown	10
Programmable Interval Timer (See listing under 8080)	8253	Intel	
	μPD8253	**NEC Micro (1845)**	
Programmable Peripheral Interface (See listing under 8080)	8255A	Intel	
	μPD8255	**NEC Micro (1830)**	
Keyboard Display Controller (See listing under 8080)	**8279**	**Intel (1651)**	20
Priority Interrupt Control. (See listing under 8080)	8214	Intel	
	μPB8214	**NEC Micro (1758)**	
Decoder, 1 of 8 (See listing under 8080)	8205	Intel	
Programmable Communication Interface (See listing under 8080)	8251	Intel	
	μPD8251	**NEC Micro (1814)**	

8048

Function	Device	Source	Line
8 Bit Microcomputer (Mask Programmed ROM)	8048	AMD	30
	8021	**Intel (1649)**	
	8048	**Intel (1648)**	
	8049	**Intel (1650)**	
	μPD8048	**NEC Micro (1849)**	
	8048	Signetics	
8 Bit Microcomputer (Erasable PROM)	**8748**	**Intel (1648)**	
	μPD8748	**NEC Micro (1849)**	
8 Bit Microcomputer (External ROM)	**8035**	**Intel (1648)**	40
	μPD8035	**NEC Micro (1849)**	
	8039	**Intel (1650)**	
I/O Expander	**8243**	**Intel (1651)**	
	μPD8243	NEC Micro	
PROM (Erasable), I/O	**8755**	**Intel (1646)**	
	μPD8755	**NEC Micro (1848)**	
RAM, I/O, Timer	8155	Intel	50
	μPD8155	**NEC Micro (1847)**	
ROM, I/O	**8355**	**Intel (1646)**	
	μPD8355	**NEC Micro (1848)**	
Universal Peripheral Interface (Slave Microprocessor)	**8041**	**Intel (1651)**	
	8741	**Intel (1651)**	

8048 (Cont'd)

Function	Device	Source	Line
I/O Expander for 8041/8741	**8243**	**Intel (1651)**	60
Analog Input, Multiplexer, A/D Converter	MP21	Burr-Brown	
Bidirectional Bus Driver. See 8216, 8226, etc. under 8080	8216	Intel	
	8226	Intel	
	μPB8216	**NEC Micro (1810)**	
	μPB8226	**NEC Micro (1810)**	
Programmable Communication Interface (USART) See 8251, etc. under 8080.	8251	Intel	70
	μPD8251	**NEC Micro (1814)**	
Decoder, 1 of 8. See 8205, etc. under 8080.	8205	Intel	
CRT Controller. See 8275, etc. under 8080.	**8275**	**Intel (1651)**	
Floppy Disc Controller. See 8271, etc. under 8080.	**8271**	**Intel (1651)**	
	μPD372	**NEC Micro (1781)**	
Keyboard Display Controller. See 8279, etc. under 8080.	**8279**	**Intel (1651)**	80
8 Bit I/O Port. See 8212, etc. under 8080.	8212	Intel	
	μPB8212	**NEC Micro (1804)**	
Priority Interrupt Control. See 8214, etc. under 8080.	8214	Intel	
	μPB8214	**NEC Micro (1758)**	
Programmable Interrupt Controller. See 8259, etc. under 8080.	8259	Intel	90
	μPD8259	**NEC Micro (1846)**	
Programmable Interval Timer. See 8253, etc. under 8080.	8253	Intel	
	μPD8253	**NEC Micro (1845)**	
Programmable Peripheral Interface. See 8255, etc. under 8080.	8255A	Intel	
	μPD8255A	**NEC Micro (1830,1845)**	100
SDLC Protocol Controller. See 8273, etc. under 8080.	**8273**	**Intel (1651)**	
	μPD379	**NEC Micro (1788)**	
Development System	**Intellec MDS**	**Intel (1640)**	

8080

Function	Device	Source	Line
See also Z80			
CPU	8080A	AMD	110
	9080AC	AMD	
	9080AM	†AMD	
	8080A	Intel	
	M8080A	†Intel	
	M58710S	Mitsubishi	
	INS8080A	**National (1656,1670)**	
	INS8080AM	**†National (1656,1670)**	
	μPD8080A	**NEC Micro (1750)**	

(Continued)

8080 (Cont'd)

Function	Device	Source	Line
CPU (Cont'd.)	**μPD8080AF**	**NEC Micro (1736)**	120
	MP8080A	Signetics	
	TMS8080A	TI	
Universal Peripheral Interface(Slave Microprocessor)	**8041**	**Intel (1651)**	
	8741	**Intel (1651)**	
I/O Expander for 8041/8741	**8243**	**Intel (1651)**	
Analog Input, 3¾ Digit DVM with multiplexed BCD Output	DP8294	National	130
Analog input, MUX, A/D converter	MP20	Burr-Brown	
	DP8292	National	
Arithmetic Processing Unit	AM9511C	AMD	
	AM9511M	†AMD	
Bus Driver (See also Digital Misc., Bus Drivers; Interface Line Drivers)	DP8202	National	140
	DP8203	National	
Bidirectional Bus Driver (See also Digital Miscellaneous Bus Drivers, Interface Line Transceivers.)	3216	AMD	
	M3216	†AMD	
	3226	AMD	
	M3226	†AMD	
	8216	AMD	
	M8216	†AMD	150
	8226	AMD	
	M8226	†AMD	
	MB425	Fujitsu	
	MB426	Fujitsu	
	8216	Intel	
	8226	Intel	
	M8216	†Intel	
	DP8208	National	
	DP8216	National	
	DP8226	National	160
	DS8833	National	
	DS8835	National	
	μPB8216	**NEC Micro (1810)**	
	μPB8226	**NEC Micro (1810)**	
Clock, Generator and Driver	8224C	AMD	
	8224M	†AMD	
	8224	Intel	
	M8224	†Intel	
	M54550	Mitsubishi	170
	DP8224	**National (477)**	
	μPB8224	**NEC Micro (1764)**	
	SN54LS424	†TI	
	SN74LS424	TI	
	TIM8224	TI	
Asynchronous Communication Element	INS8050	National	
	μPD369	NEC Micro	
	TR1983	Western	
Programmable Communication Interface (USART) (See also Interface Transmitters,Receivers)	9551C	AMD	180
	9551M	†AMD	
	8251	Intel	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

MICROPROCESSOR–System Components (Cont'd)

Function	Device	Source	Line
8080 (Cont'd)			
Programmable Communication Interface (USART) (See also Interface Transmitters,Receivers) (Cont'd.)			
	8251A	Intel	
	M8251	†Intel	
	INS8251	National	
	INS8252	National	
	INS8261	National	
	μPD8251	**NEC Micro (1814)**	
	TMS5501	TI	
Decoder, 1 of 8 (See also Digital TTL Decoders, 3222, 74LS138, etc.)			10
	AM25LS138C	AMD	
	AM25LS138M	†AMD	
	8205	Intel	
	DM74LS138	National	
	DP82LS05	National	
	SN74LS138	TI	
Display Controller			
	DP8247	National	
	DP8248	National	20
Programmable Direct Memory Access Controller			
	8257	AMD	
	AM9517C	AMD	
	AM9517M	†AMD	
	8257	Intel	
	INS8257	National	
	INS8258	National	
	μPD8257	**NEC Micro (1837)**	
Cassette Controller			
	μPD371	**NEC Micro (1774)**	30
CRT Controller			
	8275	**Intel (1651)**	
	INS8276	National	
Floppy Disc Controller			
	8271	**Intel (1651)**	
	INS8272	National	
	μPD372	**NEC Micro (1781)**	
Keyboard Encoder (See also Interface Keyboard Encoders)			
	DP8244	National	
	DP8245	National	
	DP8246	National	40
	μPD364	NEC Micro	
Keyboard Display Controller			
	8279	**Intel (1651)**	
Programmable I/O Circuit			
	EA9255	EA	
General Interface Circuit (for DMA or interrupt exchanges)			
	μPC6001	SMC	50
GPIB Talker/Listener Interface			
	8291	Intel	
8 Bit I/O Latch (see also Digital CMOS and TTL, Latches)			
	DP83C06	National	
8 Bit I/O Port			
	3212	AMD	
	M3212	†AMD	
	8212C	AMD	
	8212M	†AMD	60
	MB471	Fujitsu	
	8212	Intel	
	M8212	†Intel	
	M54552	Mitsubishi	
	DP8212	**National (469)**	
	(Continued)		

Function	Device	Source	Line
8080 (Cont'd)			
8 Bit I/O Port (Cont'd.)			
	μPB8212	**NEC Micro (1804)**	
	SN54S412	†TI	
	SN74S412	TI	
8 Bit I/O Port, Bidirectional			70
	DP8213	National	
Multifunction I/O Controller, (asynchronous communications interface, I/O buffers, interrupt control, interval timers)			
	TMS5501	TI	
Printer Controller (Seiko)			
	μPD758	**NEC Micro (1795)**	
Priority Interrupt Control			
	AM25LS2513C	AMD	
	AM2914C	AMD	80
	AM2914M	†AMD	
	8214	Intel	
	M8214	†Intel	
	μPB8214	**NEC Micro (1758)**	
Programmable Interrupt Controller			
	9519C	AMD	
	9519M	†AMD	
	8259	Intel	
	INS8259	National	
	μPD8259	**NEC Micro (1846)**	90
Programmable Interval Timer			
	8253	Intel	
	8253	AMD	
	INS8253	National	
	μPD8253	**NEC Micro (1845)**	
Programmable Peripheral Interface			
	9555C	AMD	
	9555M	†AMD	
	8255A	Intel	
	M8255A	†Intel	100
	M58740	Mitsubishi	
	INS8255	National	
	μPD8255	**NEC Micro (1830)**	
SDLC Protocol Controller			
	8273	**Intel (1651)**	
	μPD379	**NEC Micro (1788)**	
	SD1933	Western	
Multi Protocol Communications Controller (SDLC, ADDCP, BiSync, DDCMP)			
	INS8274	National	110
Advanced Protocol Controller (SDLC, ADCCP)			
	INS8283	National	
Synchronous Receiver/Transmitter (BiSync, SDLC)			
	μPD379	**NEC Micro (1788)**	
System Controller and Bus Driver			
	8228C	AMD	
	8228M	†AMD	
	8238C	AMD	
	8238M	†AMD	
	8228	Intel	120
	M8228	†Intel	
	8238	Intel	
	M54551	Mitsubishi	
	DP8228	**National (483)**	
	DP8238	**National (483)**	
	μPB8228	**NEC Micro (1769)**	
	μPB8238	**NEC Micro (1769)**	
	SN74S428	TI	
	SN74S438	TI	
	(Continued)		

Function	Device	Source	Line
8080 (Cont'd)			
System Controller and Bus Driver (Cont'd.)			130
	TIM8228	TI	
	TIM8238	TI	
RAM(128x8), ROM(2048x8), I/O			
	DP8356	National	
RAM (128x8) with 16 Bit I/O			
	INS8154	National	
Erasable PROM (256x8) (See also Memory PROM's, 1702A series)			
	8702A	AMD	
	8702A	Intel	140
	M8702A	†Intel	
	M58563	Mitsubishi	
	MM1702AQ	**National (1365)**	
	μPD454	**NEC Micro (1448)**	
Erasable PROM(512x8) (See also Memory PROMs, 2704)			
	2704	AMD	
	S2704A	AMI	
	MM2704	National	
	MM5204A	**National (1369)**	150
	2704	Signetics	
Erasable PROM (1024x8) (See also Memory PROM's 2708)			
	8708	Intel	
	2708	AMD	
	M8708	†Intel	
	MM2708	National	
	μPD458	**NEC Micro (1454)**	
	2708	Signetics	
	TMS2708	TI	160
RAM (256x4) (See also Memory RAM's 2101, 2111 series)			
	8101	AMD	
	8111	AMD	
	8101A-4	Intel	
	8111A-4	Intel	
	MM2101	National	
	MM2111	National	
	MM8101A-4	National	
	MM8111A-4	National	170
	μPD2101AL	**NEC Micro (1424)**	
RAM (1024x1) (See also Memory RAM's 2101A series)			
	8102A-4	AMD	
	8102A-4	Intel	
	M8102A	†Intel	
	M58751	Mitsubishi	
	MM2102A	**National (1300)**	
	μPD2102AL	**NEC Micro (1429)**	
RAM (4096x1) (See also Memory RAM's 2107, 5280 series)			180
	8107B-4	Intel	
	M58755	Mitsubishi	
	MM5270	**National (1325)**	
	μPD411	**NEC Micro (1375)**	
RAM(16384x1) (See also Memory RAMs			
	μPD416	National	
ROM (256x8) (See also Memory ROM's 1302)			
	8302	Intel	
	MM5213	National	190
	DP8302	**National (496)**	
ROM (1024x8) (See also Memory ROM's 2308)			
	9208	AMD	
	8308	Intel	
	(Continued)		

† Military Temperature Range (−55° to 125°C)

* Typical Values

MICROPROCESSOR–System Components (Cont'd)

8080 (Cont'd)

ROM (1024x8) (See also Memory ROM's 2308) (Cont'd.)

Device	Source	
M58730	Mitsubishi	
MM5242	National	
μPD2308	**NEC Micro**	**(1478)**

ROM (2048x8) (See also Memory ROM's 2316A)

Device	Source	
8316A	AMD	
8316E	AMD	
9216	AMD	
8316A	Intel	
M8316	†Intel	
M58731	Mitsubishi	
MM2316A	**National**	**(1307,1372)**
MM8316A	National	
MM8316E	National	
μPD2316A	**NEC Micro**	**(1481)**
μPD2316E	**NEC Micro**	**(1492)**

ROM(4096x8) (See also Memory ROMs)

Device	Source	
MM8332	National	
μPD2332	**NEC Micro**	**(1485)**

ROM(8192x8) (See also Memory ROM's)

Device	Source	
MM8364	National	
MM8364E	National	

ROM, BASIC Interpreter

Device	Source	
EA3280	EA	
INS8298	National	

Floating Point Arithmetic

Device	Source	
FP708	Novonics	
EA8380FP	EA	

Development System

Device	Source	
Intellec MDS	**Intel**	**(1640)**
PDA-80	**NEC Micro**	**(1727)**
8001	**Tektronix**	**(1916)**
8002	**Tektronix**	**(1916)**

8085

Many devices for the 8080 are also suitable for the 8085

CPU

Device	Source	
8085	AMD	
8085	**Intel**	**(1644)**
μPD8085	**NEC Micro**	**(1847)**

PROM (Erasable), I/O

Device	Source	
8755	**Intel**	**(1646)**
μPD8755	**NEC Micro**	**(1848)**

RAM, I/O, Timer

Device	Source	
8155	AMD	
8155	Intel	
8156	**Intel**	**(1645)**
μPD8155	**NEC Micro**	**(1847)**
μPD8156	**NEC Micro**	**(1847)**

ROM, I/O

Device	Source	
8355	AMD	
8355	**Intel**	**(1646)**
μPD8355	**NEC Micro**	**(1848)**

Analog Input, Multiplexer, A/D Converter

Device	Source
MP21	Burr-Brown

Bidirectional Bus Driver. See 8216, 8226, etc. under 8080.

Device	Source	
8216	Intel	
8226	Intel	
μPB8216	**NEC Micro**	**(1810)**
μPB8226	**NEC Micro**	**(1810)**

8085 (Cont'd)

Programmable Communication Interface (USART)

Device	Source	
8251A	Intel	
μPD8251	**NEC Micro**	**(1814)**

Decoder, 1 of 8. See 8205, etc. under 8080.

Device	Source
8205	Intel

Programmable Direct Memory Access Controller.

Device	Source	
8257	Intel	
μPD8257	**NEC Micro**	**(1837)**

Cassette Controller

Device	Source
μPB372	NEC Micro

CRT Controller. See 8275, etc. under 8080.

Device	Source	
8275-5	**Intel**	**(1651)**

Floppy Disc Controller. See 8271, etc. under 8080.

Device	Source	
8271	**Intel**	**(1651)**
μPD371	**NEC Micro**	**(1774)**

Keyboard Display Controller.

Device	Source	
8279-5	**Intel**	**(1651)**

8 Bit I/O Port. See 8212, etc. under 8080.

Device	Source	
8212	Intel	
μPB8212	**NEC Micro**	**(1804)**

Priority Interrupt Control. See 8214, etc. under 8080.

Device	Source	
8214	Intel	
μPB8214	**NEC Micro**	**(1758)**

Programmable Interrupt Controller.

Device	Source	
8259-5	Intel	
μPD8259	**NEC Micro**	**(1846)**

Programmable Interval Timer.

Device	Source	
8253-5	Intel	
μPD8253	**NEC Micro**	**(1845)**

Programmable Peripheral Interface.

Device	Source	
8255A-5	Intel	
μPD8255A	**NEC Micro**	**(1830,1845)**

SDLC Protocol Controller. See 8273, etc. under 8080.

Device	Source	
8273	**Intel**	**(1651)**
μPD379	**NEC Micro**	**(1788)**

GPIB Talker/Listener Interface

Device	Source
8291	Intel

ROM(2048x8) and I/O

Device	Source	
μPD8355	**NEC Micro**	**(1848)**

Erasable PROM, I/O

Device	Source	
μPD8755	**NEC Micro**	**(1848)**

Development System

Device	Source	
Intellec MDS	**Intel**	**(1640)**
8001	**Tektronix**	**(1916)**
8002	**Tektronix**	**(1916)**

Universal Peripheral Interface(slave microprocessor)

Device	Source	
8041	**Intel**	**(1651)**
8741	**Intel**	**(1651)**

I/O Expander, for 8041/8741

Device	Source	
8243	**Intel**	**(1651)**

9080

See 8080 series

9440

Microcomputer, 16 Bit (Mask programmed ROM)

Device	Source
9440	Fairchild

9900

Microprocessor

Device	Source	
S9900	**AMI**	**(1575)**
S9980	**AMI**	**(1585)**
SBP9900	†TI	
TMS9900	TI	
TMS9980	TI	

Microcomputer, 16 Bit

Device	Source	
S9940	**AMI**	**(1583)**
TMS9940	TI	

Microcomputer, 16 Bit(Erasable PROM)

Device	Source
TMS9940E	TI

Clock Generator and Driver (4 phase for 9900)

Device	Source
S9904	AMI
SN54LS362	†TI
SN74LS362	TI
TIM9904	TI

Data Selector/Multiplexer (See also Digital TTL Multiplexers 74LS251)

Device	Source
S9905	AMI
μPB74LS251	NEC America
SN54LS251	†TI
SN74LS251	TI
TIM9905	TI

Priority Encoder (See also Digital TTL Miscellaneous, Priority Encoder, 74LS148)

Device	Source
S9907	AMI
SN74LS148	TI
TIM9907	TI

Priority Encoder, 8 Line to 3 Line, three state

Device	Source
SN74LS348	TI
TIM9908	TI

Programmable Systems Interface (interrupt prioritization, I/O control and interval timing)

Device	Source	
S9901	**AMI**	**(1577)**
TMS9901	TI	

Synchronous Communication Controller (Bi Sync and SDLC)

Device	Source	
S9903	**AMI**	**(1581)**
TMS9903	TI	

Asynchronous Communication Controller (UART) (See also Interface Serial Transmitters Receivers)

Device	Source	
S9902	**AMI**	**(1579)**
TMS6011	TI	
TMS9902	TI	

8 Bit Addressable Latch

Device	Source
S9906	AMI
SN54LS259	†TI
SN74LS259	TI
TIM9906	TI

RAM (128x8)/ROM (1920x8)

Device	Source
TMS9972	TI

Development System

Device	Source	
8001	**Tektronix**	**(1916)**
8002	**Tektronix**	**(1916)**

10800

Arithmetic Logic Unit, 4 Bit Slice

Device	Source
MC10800	Motorola
MC10800M	†Motorola

Microprogram Control Function

Device	Source
MC10801	Motorola

Memory Interface

Device	Source
MC10803	Motorola

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

MICROPROCESSOR–System Components (Cont'd)

10800 (Cont'd)

Function	Device	Source	Line
Timing Function, 4 Phase	MC10802	Motorola	
4 Bit Bidirectional Translator with Latch	MC10804	Motorola	
5 Bit Bidirectional Translator with Latch	MC10805	Motorola	
5 Bit ECL Transceiver with Latch	MC10807	Motorola	
Dual Address Register(32x9 Stack)	MC10806	Motorola	
Multibit Shifter(16 Bit Programmable Shifter)	MC10808	Motorola	10
Memories (See Digital ECL Memories and Memory PROMs/ROMs)			

14500

Function	Device	Source	Line
CPU, 1 Bit, Industrial Control Unit	MC14500B	Motorola	
Latch, 8 Bit	MC14597B	Motorola	
	MC14598B	Motorola	
	MC14599B	Motorola	

General Purpose

Function	Device	Source	Line
Analog Input, Multiplexer, A/D Converter	MP20	Burr-Brown	20
	MP21	Burr-Brown	
Analog Output, D/A Converter, Latched Input	**NE5018**	**Signetics** (1913)	
Analog Output, Dual D/A Converter	MP10	Burr-Brown	
	MP11	Burr-Brown	
Arithmetic Processor	9511	AMD	
	9511-4	AMD	30
Arithmetic Processor, 4 function ASCII Floating Point Computations	CY-450	Cybernetic	
Sequence Controller	**57110**	**† MMI** (1654)	
	67110	**MMI** (1654)	
Deskew FIFO (to synchronize data from magnetic tape storage systems)	8X03	Signetics	
	8X04	Signetics	40
Control Sequencer (to control fetch sequence of microinstructions)	**8X02**	**Signetics** (1877)	
CRT Video Timer Controller, Programmable	CRT5027	SMC	
Direct Memory Access(16 Bit)	DM1883	Western	
Priority Interrupt Controller	MC6828	Motorola	
	MC8507	Motorola	50
Floppy Disc Controller/Transmitter (IBM 3740 compatible)	INS1771	National	
	FD1771	Western	
	FD1781	Western	

General Purpose (Cont'd)

Function	Device	Source	Line
Floppy Disc Controller	**μPD372**	**NEC Micro** (1781)	
Cassette Controller	**μPD371**	**NEC Micro** (1774)	
Printer Controller, for Seiko CR 330 or M310	**μPD764**	**NEC Micro** (1799)	60
Printer Controller, for 5x7 dot matrix printer	CY-480	Cybernetic	
Plasma Display Controller and ASCII Keyboard INterface	CY-300	Cybernetic	
Synchronous Serial Data Adapter	MC6852	Motorola	
Asynchronous Communication Interface Adapter	**S6850**	**AMI** (1567)	70
	MC6850	Motorola	
	MC68A50	Motorola	
	MC68B50	Motorola	
Peripheral Interface Adapter	**S6820**	**AMI** (1556)	
	MCS6520	MOS	
	MCS6522	MOS	
	MC6820	Motorola	
	MC6821	Motorola	
	MC68A21	Motorola	80
	MC68B21	Motorola	
	SY6520	Synertek	
	SY6522	Synertek	

See also Interface Error Checking Circuits, Keyboard Encoders, Line Circuits, Memory and Peripheral Drivers, Serial Transmitters/Receivers; Memory EAROM's, FIFO's, LIFO's, PLA's, PROM's, RAM's, ROM's.

† Military Temperature Range (−55° to 125°C)

* Typical Values

MICROPROCESSORS

Manufacturer Model For Detailed Data See:	AMD AM2901	AMD 9080A	AMI S2000/A Page 1571	AMI S6800 Pages 1538, 1548
General Structure	4-Bit Slice	8-Bit CPU	4-Bit Microcomputer	8-Bit CPU
Type	TTL	NMOS	NMOS	NMOS
No. of Devices per CPU		1	1	1
CPU Size (Pins)	40	40	40	40
Supply Voltage	5	±5, 12	9	5
CPU Power Dissipation (mw)	925	830	250	600
Architecture Data Word Size (bits)	Multiple of 4	8	4 (8-Bit I/O Bus)	8
Instruction Word Size (bits)	9	8, 16, 24	8	8, 16, 24
Directly Addressable Instruction Words (No.)		65K	8K	65K
Clock Frequency (Hz/ext. phases required)	to 10 MHz/1 phase	to 4 MHz/2 phase	1 MHz/0 phase	1 MHz/2 phase
Register to Register Add Time (μsec/data word)	0.125	2 (2 MHz clock)	4	2
No. of Registers Arithmetic	0	1	1	2
Index	0	0	2	1 (16-Bit)
General Purpose	17	6	1	0
Return Stack Size (No. x bits)	4x4 (2909)	External RAM	3x10	External RAM
Interrupts	Optional	Standard	None	Standard
Type		Vectored 8 Level		Vectored, Multilevel
Direct Memory Access	Optional (2914)	Standard	None	Optional
BCD Arithmetic (Hardware)	No	Yes	No	Yes
Microprogrammable	Yes	No	No	No
Extended Temp. Range Available	−55°C to 125°C	−55°C to 125°C	Yes	No
Devices See System Components:	2900	8080	2000	6800
Hardware Support Processor Cards (CPU system on a card)	No	No	Yes (Emulator)	Yes
Prototyping System (Hardware & software development system)	No	No	Yes	Yes
In-System Emulator (Tests system in place)	No	No	Yes	Yes
Software Support (from this manufacturer) Resident Assembler	No	No	No	Yes
Cross Assembler	No	No	Yes	Fortran IV
Simulator	No	No	Yes	Fortran IV
High Level Language	No	No	No	No
Programs Debug	No	No	Yes	Yes
Diagnostic	No	No	Yes	Yes
Edit	No	No	Yes	Yes
User Library (>25 programs from user)	No	No	Macro's	No
Delivery Start (Qtr.-Year)	3 Qtr. 75	3 Qtr. 75	3 Qtr. 77	1 Qtr. 75
Alternate Sources	Fairchild, Motorola, National, NEC, Raytheon, Signetics	Intel, Mitsubishi, National, NEC, Raytheon, Signetics	Future	Fairchild, Hitachi, Motorola
Comments		Priority interrupts with Intel 8214.	64x4 RAM, 1024x8 ROM, Timer, Touch Switch Input, Fluorescent Display Driver On-chip.	DMA through HALT and three state control.

Tinted column indicates additional data is provided on the page noted.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	AMI S9900 Page 1575	AMI S9980 Page 1585	Data General mN601	Essex SX200
General Structure	16-Bit CPU	8/16-Bit CPU	16-Bit CPU	4-Bit CPU
Type	NMOS	NMOS	NMOS	PMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	64	40	40	28
Supply Voltage	±5, 12	±5, 12	±5, 15	15
CPU Power Dissipation (mw)	1000	1000	1000	150
Architecture Data Word Size (bits)	16	8	16	4
Instruction Word Size (bits)	16, 32, 48	16, 32, 48	16	8
Directly Addressable Instruction Words (No.)	65K bytes, 32K words	16K bytes	32K	1K
Clock Frequency (Hz/ext. phases required)	3 MHz/4 phase	2-3 MHz/0 phase	8.3 MHz/2 phase	to 500/0 phase
Register to Register Add Time (μsec/data word)	4.67	8.8 (2 MHz)	2.4	16
No. of Registers Arithmetic	16	16		1
Index	15	15	2	1
General Purpose	16 (in memory)	16 (in memory)	4	0
Return Stack Size (No. x bits)	None	None	External RAM	1x10
Interrupts	Standard	Standard	Standard	None
Type	Vectored, 16 Levels	Vectored, 6 Levels	16 Levels	
Direct Memory Access	Standard	Standard	Standard	None
BCD Arithmetic (Hardware)	No	No	No	Yes
Microprogrammable	No	No	No	No
Extended Temp. Range Available	−25°C to 85°C		No	−40°C to 100°C Std.
Devices See System Components:	9900	9900	Micro Nova	SX200
Hardware Support Processor Cards (CPU system on a card)	No	No	Yes	No
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	No	No	No	Yes
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	Yes	No
Cross Assembler	Yes	Timesharing	Yes	Fortran
Simulator	Timesharing	Timesharing	Yes	Yes
High Level Language	Fortran, Cobol	Fortran, Cobol	Fortran	No
Programs Debug	Yes	Yes	Yes	No
Diagnostic	Yes	Yes	Yes	No
Edit	Yes	Yes	Yes	No
User Library (>25 programs from user)	No		Yes	No
Delivery Start (Qtr.-Year)	1 Qtr. 78	1 Qtr. 78	3 Qtr. 76	2 Qtr. 76
Alternate Sources	TI	TI	None	None
Comments	Software compatible with 990 minicomputer.	8-Bit data bus, 16-Bit internal operation. Software compatible with TMS9900.		

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Fairchild F8 Page 1606	Fairchild F3870	Fairchild F6800	Fairchild F9409/2901A
General Structure	8-Bit CPU	8-Bit CPU	8-Bit CPU	4-Bit Slice
Type	NMOS	NMOS	NMOS	TTL
No. of Devices per CPU	1	1	1	
CPU Size (Pins)	40	40	40	40
Supply Voltage	5, 12	5	5	5
CPU Power Dissipation (mw)	300	300	600	925
Architecture Data Word Size (bits)	8	8	8	Multiple of 4
Instruction Word Size (bits)	8, 16, 24	8, 16, 24	8, 16, 24	9
Directly Addressable Instruction Words (No.)	65K	2K	65K	
Clock Frequency (Hz/ext. phases required)	2 MHz/0 phase	4 MHz/0 phase	1 MHz/2 phase	to 10 MHz/1 phase
Register to Register Add Time (μsec/data word)	2	2	2	0.125
No. of Registers Arithmetic	1	1	2	0
Index	2	2	1 (16-Bit)	0
General Purpose	64	65	0	17
Return Stack Size (No. x bits)	33x16 or RAM	1x8 or RAM	External RAM	4x4 (2909)
Interrupts	Standard	Standard	Standard	Optional
Type	Vectored, 1 Level/PSU	Vectored, 1 Level	Vectored, Multilevel	
Direct Memory Access	Optional (3854)	None	Optional	Optional (2914)
BCD Arithmetic (Hardware)	Yes	Yes	Yes	No
Microprogrammable	No	No	No	Yes
Extended Temp. Range Available	−55°C to 125°C	Future	Future	−55°C to 125°C
Devices See System Components:	F8	F8	6800	2900
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes	Yes	No
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	No
In-System Emulator (Tests system in place)	Yes	Yes	Yes	No
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	Yes	No
Cross Assembler	Fortran IV	Fortran IV	Fortran IV	No
Simulator	Prototyping Sys, Fortran IV	No	Fortran IV	No
High Level Language	No	No	MPL	No
Programs Debug	Yes	Yes	Yes	No
Diagnostic	Yes	Yes	Yes	No
Edit	Yes	Yes	Yes	No
User Library (>25 programs from user)	Yes	No	No	No
Delivery Start (Qtr.-Year)	1 Qtr. 75	1 Qtr. 78	1 Qtr. 77	
Alternate Sources	Mostek, SGS	Mostek, Motorola	AMI, Hitachi, Motorola	AMD, Motorola, National, NEC, Raytheon, Signetics
Comments	64 bytes of RAM in CPU. 1024 or 2048 bytes of ROM in PSU. Programmable Timer.	One chip microcomputer. Programmable hardware, timer on-chip. Software compatible with F8.	DMA through HALT and three state control.	

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Fairchild Macrologic Bipolar Page 1613	Fairchild Macrologic CMOS	General Instrument CP-1600/A	General Instrument LP-8000
General Structure	4-Bit Slice	4-Bit Slice	16-Bit CPU	8-Bit CPU
Type	TTL	CMOS	NMOS	PMOS
No. of Devices per CPU			1	1
CPU Size (Pins)	24	24	40	40
Supply Voltage	5	3 to 15	−3, 5, 12	−12, 5
CPU Power Dissipation (mw)	800	to 5mw at 10V	750	500
Architecture Data Word Size (bits)	Multiple of 4	Multiple of 4	16	8
Instruction Word Size (bits)	3	4	10, 20, 30	8, 16, 24
Directly Addressable Instruction Words (No.)			65K	65K
Clock Frequency (Hz/ext. phases required)	to 14 MHz/1 phase	to 4.9 MHz (15V)/1 phase	5 MHz/2 phase	800 KHz/1 phase
Register to Register Add Time (μsec/data word)	0.10	0.086 (15V)	2.4	5.0
No. of Registers Arithmetic	0	1	0	1
Index	0	2	0	0
General Purpose	8	2	8	48
Return Stack Size (No. x bits)	10x4 (9408), 16x4 (9406)		Standard	1x8 or RAM
Interrupts	Optional		External RAM	Standard
Type			Vectored, Multilevel	Vectored, 1 Level
Direct Memory Access	Optional		Standard	No
BCD Arithmetic (Hardware)	No	No	No	Yes
Microprogrammable	Yes	Yes	No	No
Extended Temp. Range Available	−55°C to 125°C	−55°C to 125°C		
Devices See System Components:	Macrologic Bipolar	Macrologic CMOS	1600	8000
Hardware Support Processor Cards (CPU system on a card)	Yes	No	Yes	Yes
Prototyping System (Hardware & software development system)	Yes	No	Yes	Yes
In-System Emulator (Tests system in place)	No	No	Yes	No
Software Support (from this manufacturer) Resident Assembler	No	No	Yes	Yes
Cross Assembler	Timesharing	No	Fortran IV	Fortran IV
Simulator	No	No	Fortran IV	Fortran IV
High Level Language	No	No	No	No
Programs Debug	No	No	Yes	Yes
Diagnostic	No	No	Yes	Yes
Edit	No	No	Yes	Yes
User Library (>25 programs from user)	No	No	No	No
Delivery Start (Qtr.-Year)	4th Qtr. 75	2 Qtr. 75	3 Qtr. 74	2 Qtr. 75
Alternate Sources	None			None
Comments	Hardware stack with 9406, 10-Bit sequencer with 9408.		CP-1600 3.6 μsec add time with 3.3 MHz clock	

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	General Instrument PIC 1650	Harris HM6100 Page 1631	Harris HM6100A Page 1631	Hughes HCMP1802
General Structure	8-Bit Microcomputer	12-Bit CPU	12-Bit CPU	8-Bit CPU
Type	NMOS	CMOS	CMOS	CMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	40	40	40	40
Supply Voltage	5	5	4-11	4 to 6/3 to 12
CPU Power Dissipation (mw)	375	10	40	6 to 40
Architecture Data Word Size (bits)	8	12	12	8
Instruction Word Size (bits)	12	12	12	8, 16, 24
Directly Addressable Instruction Words (No.)	512	4K (Expandable to 32K)	4K (Expandable to 32K)	65K
Clock Frequency (Hz/ext. phases required)	1 MHz/0 phase	4 MHz/0 phase	8 MHz/0 phase	0-6.4 MHz/0 phase
Register to Register Add Time (μsec/data word)	4	5 (2.50 10V)	2.5	2.5 (6.4 MHz clock)
No. of Registers Arithmetic	0	2	2	1
Index	0	0	0	0
General Purpose	32	4	4	32
Return Stack Size (No. x bits)	2x9	None	None	External RAM
Interrupts	None	Standard	Standard	Standard
Type		Vectored, 1 Level	Vectored, 1 Level	1 Level
Direct Memory Access	None	Standard	Standard	Standard (on-chip)
BCD Arithmetic (Hardware)	No	No	No	No
Microprogrammable	Yes	No	No	No
Extended Temp. Range Available	Future	−55°C to 125°C	−55°C to 125°C	−55°C to 125°C Standard
Devices See System Components:	1600	6100	6100	1800
Hardware Support Processor Cards (CPU system on a card)	No	Yes	Yes	Yes
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	Yes	No	No	Yes
Software Support (from this manufacturer) Resident Assembler	No	Yes	Yes	Yes
Cross Assembler	Yes	Fortran IV	Fortran IV	Fortran IV, Timesharing
Simulator	Yes	Fopel III	Fopel	Yes
High Level Language	No	Focal, Basic, Fortran	Focal, Basic, Fortran	No
Programs Debug	Yes	Yes	Yes	Yes
Diagnostic	Yes	Yes	Yes	Yes
Edit	Yes	Yes	Yes	Yes
User Library (>25 programs from user)	No			No
Delivery Start (Qtr.-Year)	2 Qtr. 77	1 Qtr. 76	1 Qtr. 76	3 Qtr. 77
Alternate Sources	None	Intersil	Intersil	RCA
Comments	Stand alone controller.			

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Intel 3000	Intel 4004	Intel 4040	Intel 8008
General Structure	2-Bit Slice	4-Bit CPU	4-Bit CPU	8-Bit CPU
Type	TTL	PMOS	PMOS	PMOS
No. of Devices per CPU	≥2	1	1	1
CPU Size (Pins)	28 and 40	16	24	18
Supply Voltage	5	15 (or −10, 5)	15 (or −10, 5)	−9, 5
CPU Power Dissipation (mw)	800	450	1000	420
Architecture Data Word Size (bits)	Multiple of 2	4	4	8
Instruction Word Size (bits)		8, 16	8, 16	8, 16, 24
Directly Addressable Instruction Words (No.)	512 (Microinstructions)	4K	4K	16K
Clock Frequency (Hz/ext. phases required)	to 6 MHz/1 phase	500 to 740 kHz/2 phase	500 to 740 kHz/2 phase	800 kHz/2 phase
Register to Register Add Time (μsec/data word)	0.15 (16 bits)	10.8	10.8	12.5
No. of Registers Arithmetic	2	1	1	1
Index	0	0	0	0
General Purpose	11	16	24	6
Return Stack Size (No. x bits)	None	3x12	7x12	7x14
Interrupts	Optional	None	Standard	Standard
Type	8 Level Priority (3214)		Vectored, 1 Level	Vectored, 8 Level
Direct Memory Access	No	None	None	
BCD Arithmetic (Hardware)	No	Yes	Yes	No
Microprogrammable	Yes	No	No	No
Extended Temp. Range Available	−55°C to 125°C	−40°C to 85°C	−55°C to 85°C	−55°C to 85°C
Devices See System Components:	3000	4004/4040	4004/4040	8008
Hardware Support Processor Cards (CPU system on a card)	No	Yes	Yes	Yes
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	Yes	No	No	No
Software Support (from this manufacturer) Resident Assembler	No	Yes	Yes	Yes
Cross Assembler	CROMIS Microassembler	Fortran IV	Fortran IV	Fortran IV
Simulator	No	Fortran IV	Fortran IV	Fortran IV
High Level Language	No	No	No	PL/M (Fortran IV)
Programs Debug	No	Yes	Yes	Yes
Diagnostic	No	Yes	Yes	Yes
Edit	No	Yes	Yes	Yes
User Library (>25 programs from user)	No	Yes	Yes	Yes
Delivery Start (Qtr.-Year)	3 Qtr. 74	2 Qtr. 71	4 Qtr. 74	1 Qtr. 72
Alternate Sources	Signetics	National	None	None
Comments				8 level interrupts with 8214 Priority Interrupt IC.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Intel 8021 Page 1649	Intel 8048/8748 Page 1648	Intel 8049 Page 1650	Intel 8080A
General Structure	8-Bit Microcomputer	8-Bit Microcomputer	8-Bit Microcomputer	8-Bit CPU
Type	NMOS	NMOS	NMOS	NMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	28	40	40	40
Supply Voltage	5	5	5	±5, 12
CPU Power Dissipation (mw)	250	300	350	780
Architecture Data Word Size (bits)	8	8	8	8
Instruction Word Size (bits)	8, 16	8, 16	8, 16	8, 16, 24
Directly Addressable Instruction Words (No.)	1K	4K	4K	65K
Clock Frequency (Hz/ext. phases required)	3 MHz/0 phase	6 MHz/0 phase	6 MHz/0 phase	2 MHz/2 phase (2.6 and 3 MHz opt.)
Register to Register Add Time (μsec/data word)	10	2.5	2.5	2 (2 MHz clock)
No. of Registers Arithmetic	16	16	16	1
Index	0	0	0	0
General Purpose	64	64	128	6
Return Stack Size (No. x bits)	8x16	8x16	8x16	External RAM
Interrupts	None	Yes	Yes	Standard
Type		Dual, 1 Level, Vectored	Dual, 1 Level, Vectored	Vectored, Multilevel
Direct Memory Access	No	No	No	Standard
BCD Arithmetic (Hardware)	Yes	Yes	Yes	Yes
Microprogrammable	No	No	No	No
Extended Temp. Range Available		−55°C to 125°C		−55°C to 125°C
Devices See System Components:	8048	8048	8048	8080
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes	Yes	Yes
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	Yes	Yes	Yes	Yes
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	Yes	Yes
Cross Assembler	No	No	No	Fortran IV
Simulator	No	No	No	Fortran IV
High Level Language	No	No	No	PL/M (Fortran IV)
Programs Debug	Yes	Yes	Yes	Yes
Diagnostic	Yes	Yes	Yes	Yes
Edit	Yes	Yes	Yes	Yes
User Library (>25 programs from user)	Yes	Yes	Yes	Yes
Delivery Start (Qtr.-Year)	1 Qtr. 78	1 Qtr. 77	1 Qtr. 78	4 Qtr. 73
Alternate Sources	Signetics	AMD, NEC, Signetics, Siemens	None	AMD, Mitsubishi, National, NEC, Signetics, TI
Comments	Software subset of 8048.	8048 has ROM, 8748 U.V. PROM, 8035 external ROM.	8039 uses external ROM.	

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Intel 8085 Page 1644	Intersil IM6100	Mitsubushi MELPS 8	Monolithic Memories 67000 Page 1654
General Structure	8-Bit CPU	12-Bit CPU	8-Bit CPU	4-Bit Slice
Type	NMOS	CMOS	NMOS	TTL
No. of Devices per CPU	1	1	1	
CPU Size (Pins)	40	40	40	40
Supply Voltage	5	5 to 10 (5 nominal)	±5, 12	5
CPU Power Dissipation (mw)	850	10	780	900
Architecture Data Word Size (bits)	8	12	8	Multiple of 4
Instruction Word Size (bits)	8, 16, 24	12	8, 16, 24	8
Directly Addressable Instruction Words (No.)	65K	4K (Expandable to 32K)	65K	
Clock Frequency (Hz/ext. phases required)	3 MHz/0 phase	4 MHz/0 phase	2 MHz/2 phase	0 to 10 MHz/1 phase
Register to Register Add Time (μsec/data word)	1.3	5 (2.5 at 10V)	2 (2 MHz clock)	0.085 typ. (6701)
No. of Registers Arithmetic	1	2	1	0
Index	0	0	0	0
General Purpose	7	4	6	17
Return Stack Size (No. x bits)	External RAM	None	External RAM	1x8 (67110)
Interrupts	Standard	Standard	Standard	67116
Type	Vectored, 4 Level + External	Vectored, 1 Level		16 Vectored
Direct Memory Access	Standard	Standard	Standard	No
BCD Arithmetic (Hardware)	Yes	No	Yes	No
Microprogrammable	No	No	No	Yes
Extended Temp. Range Available	−55°C to 125°C	−55°C to 125°C	No	−55°C to 125°C
Devices See System Components:	8085	6100	8080	67000
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes		No
Prototyping System (Hardware & software development system)	Yes	Yes		No
In-System Emulator (Tests system in place)	Yes	No		No
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	Yes	No
Cross Assembler	Fortran IV	Yes	Yes	Fortran IV
Simulator	Fortran IV	Forpal III		No
High Level Language	PL/M	Yes	PL/M	No
Programs Debug	Yes	Yes		No
Diagnostic	Yes	Yes		No
Edit	Yes	Yes		No
User Library (>25 programs from user)	Yes	Yes (DEC)		No
Delivery Start (Qtr.-Year)	1 Qtr. 77	2 Qtr. 75		4 Qtr. 75
Alternate Sources	AMD, NEC, Siemens	Harris		
Comments	8080A compatible with multiplexed bus operation.	Executive PDP-8, Instruction Set	CPU M58710S compatible with 8080.	RAM on-chip.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	MOS Technology 6500	Mostek F8	Mostek MK3870	Mostek Z80
General Structure	8-Bit CPU	8-Bit CPU	8-Bit CPU	8-Bit CPU
Type	NMOS	NMOS	NMOS	NMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	40 or 28	40	40	40
Supply Voltage	5	5, 12	5	5
CPU Power Dissipation (mw)	200	600	300	1100
Architecture Data Word Size (bits)	8	8	8	8
Instruction Word Size (bits)	8, 16, 24	8, 16, 24	8, 16, 24	8, 16, 24, 36
Directly Addressable Instruction Words (No.)	65K	65K	2K	65K
Clock Frequency (Hz/ext. phases required)	to 2 MHz/1 phase	2 MHz/0 phase	4 MHz/0 phase	2.5 MHz/2 phase (4 MHz opt.)
Register to Register Add Time (μsec/data word)	1	2	2	1.6 (2.5 MHz dock)
No. of Registers Arithmetic	1	1	1	1
Index	2	2	2	2
General Purpose	0	65	65	14
Return Stack Size (No. x bits)	External RAM	1x8 or RAM	1x8 or RAM	External RAM
Interrupts	Standard	Standard	Standard	Standard
Type	Vectored, 2 Level	Vectored, 1 Level/PSU	Vectored, 1 Level	Vectored, Multilevel
Direct Memory Access	Optional	Optional (MK3854)	None	MK3883-DMA
BCD Arithmetic (Hardware)	Yes	Yes	Yes	Yes
Microprogrammable	No	No	No	No
Extended Temp. Range Available	−55°C to 85°C		−40°C to 85°C	−55°C to 125°C
Devices See System Components:	6500	F8	F8	Z80
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes	Yes	Yes
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	Yes	Yes	Yes	Yes
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	Yes	Yes
Cross Assembler	Fortran IV	Fortran IV	Fortran IV	Fortran IV
Simulator	Fortran IV	Timesharing	No	Timesharing
High Level Language	No	No	No	PLZ
Programs Debug	Yes	Yes	Yes	Yes
Diagnostic	Yes	Yes	Yes	Yes
Edit	No	Yes	Yes	Yes
User Library (>25 programs from user)	No	No	No	No
Delivery Start (Qtr.-Year)	3 Qtr. 75	3 Qtr. 75	1 Qtr. 77	2 Qtr. 76
Alternate Sources	Synertek	Fairchild, SGS	Fairchild, Motorola	NEC, Zilog
Comments	DMA based on a stopping CPU, but address bus connections are not 3 state.	64 bytes of RAM in CPU 1024 bytes of ROM in PSU programmable timer.	One chip microcomputer. Programmable hardware, timer on-chip.	8080A Software compatible with additional instructions. Vectored priority interrupt in peripheral devices.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Motorola M2901	Motorola M3870	Motorola M6800	Motorola M10800
General Structure	4-Bit Slice	8-Bit CPU	8-Bit CPU	4-Bit Slice
Type	TTL	NMOS	NMOS	ECL
No. of Devices per CPU		1	1	
CPU Size (Pins)	40	40	40	48
Supply Voltage	5	5	5	−2, −5.2
CPU Power Dissipation (mw)	925	300	600	
Architecture Data Word Size (bits)	Multiple of 4	8	8	Multiple of 4
Instruction Word Size (bits)	9	8, 16, 24	8, 16, 24	
Directly Addressable Instruction Words (No.)		2K	65K	
Clock Frequency (Hz/ext. phases required)	to 10 MHz/1 phase	4 MHz/0 phase	1-2 MHz/2 phase	0 to 6 MHz/1 phase
Register to Register Add Time (μsec/data word)	0.125	2	1 (2 MHz clock)	0.041 typ. 16-Bit
No. of Registers Arithmetic	0	1	2	Ext.
Index	0	2	1 (16-Bit)	MC10803
General Purpose	17	65	0	MC10803
Return Stack Size (No. x bits)	4x4 (M2909)	1x8 or RAM	External RAM	MC10801
Interrupts	Optional	Standard	Standard	
Type		Vectored, 1 Level	Vectored, Multilevel	
Direct Memory Access	Optional	None	Optional	
BCD Arithmetic (Hardware)	No	Yes	Yes	Yes
Microprogrammable	Yes	No	No	Yes
Extended Temp. Range Available			No	No
Devices See System Components:	2900	F8	6800	10800
Hardware Support Processor Cards (CPU system on a card)	No	Yes	Yes	No
Prototyping System (Hardware & software development system)	No	Yes	Yes	No
In-System Emulator (Tests system in place)	No	Yes	Yes	No
Software Support (from this manufacturer) Resident Assembler	No	Yes	Yes	No
Cross Assembler	No	Fortran IV	Fortran IV	No
Simulator	No	No	Fortran IV	No
High Level Language	No	No	MPL (Fortran)	No
Programs Debug	No	Yes	Yes	No
Diagnostic	No	Yes	Yes	No
Edit	No	Yes	Yes	No
User Library (>25 programs from user)	No	No	No	No
Delivery Start (Qtr.-Year)	3 Qtr. 76	4 Qtr. 77	2 Qtr. 74	2 Qtr. 76
Alternate Sources	AMD, Fairchild, National, NEC, Raytheon, Signetics	Fairchild, Mostek	AMI, Fairchild, Hitachi	Future
Comments		One chip microcomputer. Programmable hardware, timer on-chip.	DMA through HALT and three state control.	

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	National IMP 16 Page 1656	National INS4004 (FIPS) Page 1656	National INS2650 Page 1656	National INS8080A Pages 1656, 1670
General Structure	4-Bit Slice	4-Bit CPU	8-Bit CPU	8-Bit CPU
Type	PMOS	PMOS	NMOS	NMOS
No. of Devices per CPU		1	1	1
CPU Size (Pins)	24	16	40	40
Supply Voltage	−12, 5	15 (or −10, 5)	5	±5, 12
CPU Power Dissipation (mw)		450	525	780
Architecture Data Word Size (bits)	16	4	8	8
Instruction Word Size (bits)	16	8, 16	8, 16, 24	8, 16, 24
Directly Addressable Instruction Words (No.)	65K	4K	32K	65K
Clock Frequency (Hz/ext. phases required)	to 700 kHz/4 phase	500 to 740 kHz/2 phase	0 to 1.25 MHz/1 phase	2 MHz/2 phase (2.6 & 3 MHz opt.)
Register to Register Add Time (μsec/data word)	4.6	10.8	4.8	2 (2 MHz)
No. of Registers Arithmetic	4	1	0	1
Index	4	0	0	0
General Purpose	4	16	7	6
Return Stack Size (No. x bits)	16x16	3x12	8x15	External RAM
Interrupts	Standard	None	Standard	Standard
Type	2 Level		Vectored	Vectored, Multilevel
Direct Memory Access	Optional	None	Standard	Standard
BCD Arithmetic (Hardware)	No	Yes	Standard	Yes
Microprogrammable	Yes	No	No	No
Extended Temp. Range Available	No		No	−40 to 85°C/ −55 to 125°C
Devices See System Components:	IMP	4004/4040	2650	8080
Hardware Support Processor Cards (CPU system on a card)	Yes	No	Yes	Yes
Prototyping System (Hardware & software development system)	Yes	No	Yes	Yes
In-System Emulator (Tests system in place)	No	No	Yes	Yes
Software Support (from this manufacturer) Resident Assembler	Yes	No	Yes	Yes
Cross Assembler	Fortran IV	No	Fortran IV, PDP-11	Yes
Simulator	No	No	Fortran IV	No
High Level Language	SM/PL	No	PLμS	Basic (LLL)
Programs Debug	Yes	No	Yes	Yes
Diagnostic	Yes	No	Yes	Yes
Edit	Yes	No	Yes	Yes
User Library (>25 programs from user)	Yes	No	No	No
Delivery Start (Qtr.-Year)	1 Qtr. 73	3 Qtr. 75		3 Qtr. 76
Alternate Sources	None	Intel	Signetics	AMD, Intel, Mitsubishi, NEC, Signetics, TI
Comments	DMA requires external controller.			Hardware and software support thru independent company.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	National INS8900 Pages 1656, 1702	National IPC-16 (PACE) Page 1656	National ISP-8A (SC/MP) Pages 1656, 1692	National MM5781/82 Page 1656
General Structure	16-Bit CPU	16-Bit CPU	8-Bit CPU	4-Bit CPU
Type	NMOS	PMOS	NMOS	PMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	40	40	40	28
Supply Voltage	±5, 12	−12, 5	5	8.5
CPU Power Dissipation (mw)		700	420	150
Architecture Data Word Size (bits)	8 or 16	8 or 16	8	4
Instruction Word Size (bits)	16	16	8, 16	8
Directly Addressable Instruction Words (No.)	65K	65K	65K	2K to 16K
Clock Frequency (Hz/ext. phases required)	2 MHz/1 phase	2 MHz/2 phase	4 MHz/0 phase	400 kHz/0 phase
Register to Register Add Time (μsec/data word)	8	8	7	10
No. of Registers Arithmetic	4	4	1	0
Index	2	2	4	0
General Purpose	4	4	3	3
Return Stack Size (No. x bits)	10x16	10x16	Software Stack	2x11
Interrupts	Standard	Standard	Standard	Standard
Type	Vectored, 6 Level	Vectored, 6 Level	Vectored	1 Level
Direct Memory Access	Optional	Optional	Standard	None
BCD Arithmetic (Hardware)	Standard	Standard	Standard	Yes
Microprogrammable	No	No	No	No
Extended Temp. Range Available	−55°C to 85°C	−55°C to 85°C	−55°C to 85°C	
Devices See System Components:	PACE	PACE	SCMP	5781/82
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes	Yes	Yes
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	No	No	Yes	Yes
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	Yes	No
Cross Assembler	Fortran IV	Fortran IV	Fortran IV, Timesharing	Yes
Simulator	No	No	No	Yes
High Level Language	Basic	Basic	Tiny Basic	No
Programs Debug	Yes	Yes	Yes	Yes
Diagnostic	Yes	Yes	Yes	Yes
Edit	Yes	Yes	Yes	Yes
User Library (>25 programs from user)	Yes	Yes	Yes	No
Delivery Start (Qtr.-Year)	3 Qtr. 77	2 Qtr. 75	1 Qtr. 76	4 Qtr. 75
Alternate Sources	None	None	Signetics	None
Comments		DMA requires external controller.		2 chip calculator based system, expandable RAM, ROM, I/O.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	National MM5799	National MM57140	NEC Micro μCOM-42 Page 1727	NEC Micro μCOM-43 Page 1727
General Structure	4-Bit Microcomputer	4-Bit Microcomputer	4-Bit Microcomputer	4-Bit Microcomputer
Type	PMOS	PMOS	PMOS	PMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	28	28	42	42
Supply Voltage	8.5	8.5	10	10
CPU Power Dissipation (mw)	150	125	300	300
Architecture				
Data Word Size (bits)	4	4	4	4
Instruction Word Size (bits)	8	8	10	8, 16
Directly Addressable Instruction Words (No.)	1536 (internal)	630 (internal)	1920	2000
Clock Frequency (Hz/ext. phases required)	400 kHz/0 phase	280 kHz/0 phase	200 kHz/1 phase	200 kHz/0 phase
Register to Register Add Time (μsec/data word)	10	14	10	10
No. of Registers Arithmetic	0	0	1	1
Index	0	0	0	0
General Purpose	3	3	96	96
Return Stack Size (No. x bits)	2x11	2x11	4x11	3x11
Interrupts	None	None	Yes	Yes
Type			Dual	Single
Direct Memory Access	None	None	None	None
BCD Arithmetic (Hardware)	Yes	Yes	Yes	Yes
Microprogrammable	No	No	No	No
Extended Temp. Range Available			No	No
Devices See System Components:	5799	5799	μCOM-4	μCOM-4
Hardware Support Processor Cards (CPU system on a card)	No	No	Yes	Yes
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	No		No	No
Software Support (from this manufacturer) Resident Assembler	No	No	No	No
Cross Assembler	Yes	Yes	8080/Fortran IV	8080/Fortran IV
Simulator	Timesharing		No	No
High Level Language	No	No	No	No
Programs Debug	Yes	Yes	No	No
Diagnostic	Yes	Yes	No	No
Edit	Yes	Yes	Yes	Yes
User Library (>25 programs from user)	No	No	No	No
Delivery Start (Qtr.-Year)	2 Qtr. 76	1 Qtr. 77	1 Qtr. 77	2 Qtr. 77
Alternate Sources	None	None	None	None
Comments	1 chip calculator based system, expandable RAM, I/O.	1 chip calculator based system, expandable I/O.		

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	NEC Micro μCOM-44 Page 1727	NEC Micro μCOM-45 Page 1727	NEC Micro μPB2901 Page 1850	NEC Micro μPDZ-80 Page 1760
General Structure	4-Bit Microcomputer	4-Bit Microcomputer	4-Bit Slice	8-Bit CPU
Type	PMOS	PMOS	TTL	NMOS
No. of Devices per CPU	1	1		1
CPU Size (Pins)	42	28	40	40
Supply Voltage	10	10	5	5
CPU Power Dissipation (mw)	300	300	925	800
Architecture Data Word Size (bits)	4	4	Multiple of 4	8, 16
Instruction Word Size (bits)	8, 16	8, 16	9	8, 16, 24, 32
Directly Addressable Instruction Words (No.)	1000	640		65K
Clock Frequency (Hz/ext. phases required)	200 kHz/0 phase	200 kHz/0 phase	>10 MHz/1 phase	2.5 MHz/1 phase
Register to Register Add Time (μsec/data word)	10	10	0.1	1.6
No. of Registers Arithmetic	1	1	0	1
Index	0	0	0	2
General Purpose	64	32	17	14
Return Stack Size (No. x bits)	1x10	1x10	4x4 (2909)	External RAM
Interrupts	Yes	Yes	Optional	Standard
Type	Single	Single		Vectored, Multilevel
Direct Memory Access	No	No	Optional	
BCD Arithmetic (Hardware)	Yes	Yes	No	Yes
Microprogrammable	No	No	Yes	No
Extended Temp. Range Available	No	No	No	No
Devices See System Components:	μCOM-4	μCOM-4	2900	Z80
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes	No	No
Prototyping System (Hardware & software development system)	Yes	Yes	No	No
In-System Emulator (Tests system in place)	No	No	No	No
Software Support (from this manufacturer) Resident Assembler	No	No	No	Yes
Cross Assembler	8080/Fortran IV	8080/Fortran IV	No	Yes
Simulator	No	No	No	No
High Level Language	No	No	No	PL/N
Programs Debug	No	No	No	No
Diagnostic	No	No	No	No
Edit	Yes	Yes	No	Yes
User Library (>25 programs from user)	No	No	No	No
Delivery Start (Qtr.-Year)	3 Qtr. 77	4 Qtr. 77	2 Qtr. 78	4 Qtr. 77
Alternate Sources	None	None	AMD, Fairchild, Motorola, National, Signetics, TI	Mostek, Zilog
Comments				

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	NEC Micro μPD8048 Page 1849	NEC μPD8080A Pages 1736, 1750	NEC Micro μPD8085 Page 1847	Panasonic MN1400
General Structure	8-Bit Microcomputer	8-Bit CPU	8-Bit CPU	4-Bit Microcomputer
Type	NMOS	NMOS	NMOS	NMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	40	40	40	28/40/64
Supply Voltage	5	±5, 12	5	5
CPU Power Dissipation (mw)	300	780	500	500
Architecture Data Word Size (bits)	8	8	8	4
Instruction Word Size (bits)	8, 16	8, 16, 24	8, 16, 24	8
Directly Addressable Instruction Words (No.)	4K	65K	65K	768 or 1024 (internal)
Clock Frequency (Hz/ext. phases required)	6 MHz/0 phase	2 MHz/2 phase (1.25 to 3 MHz Opt.)	2.5 MHz/0 phase	0-300 kHz/0 phase
Register to Register Add Time (μsec/data word)	2.5	2 (2 MHz clock)	2	10
No. of Registers Arithmetic	16	1	1	
Index	0	0	0	
General Purpose	64	6	7	
Return Stack Size (No. x bits)	8x16	External RAM	External RAM	
Interrupts	Yes	Standard	Standard	
Type	Dual, 1 Level, Vectored	Vectored, Multilevel	Vectored Multilevel	
Direct Memory Access	No	Standard	Standard	
BCD Arithmetic (Hardware)	Yes	Yes	Yes	No
Microprogrammable	No	No	No	No
Extended Temp. Range Available	No	No	No	None
Devices See System Components:	8048	8080	8085	1400
Hardware Support Processor Cards (CPU system on a card)	No	Yes	No	
Prototyping System (Hardware & software development system)	No	Yes	No	
In-System Emulator (Tests system in place)	No	No	No	
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	Yes	No
Cross Assembler	Yes	Timesharing	Fortran IV	Yes
Simulator	No		Yes	Yes
High Level Language	No	PL/N	PL/N	No
Programs Debug	No	Yes	No	Yes
Diagnostic	No	Yes	No	Yes
Edit	Yes	Yes	Yes	Yes
User Library (>25 programs from user)	No	No	No	No
Delivery Start (Qtr.-Year)	1 Qtr. 78	3 Qtr. 75	1 Qtr. 78	4 Qtr. 77
Alternate Sources	AMD, Intel, Signetics, Siemens	AMD, Intel, National, Signetics, TI	AMD, Intel, Siemens	None
Comments	μPD8048 has ROM, μPD8748 μV erasable PROM.	NEC μPD753 is 42 pin version		

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Raytheon Semi 2900	RCA CDP1802	Rockwell PPS-4/1	Rockwell PPS-4/2, PPS-4
General Structure	4-Bit Slice	8-Bit CPU	4-Bit CPU/Microcomputer	4-Bit CPU
Type	TTL	CMOS	PMOS	PMOS
No. of Devices per CPU		1	1	1
CPU Size (Pins)	40	40	28/42/52	42
Supply Voltage	5	4 to 6/3 to 12	15	17 (or −12, 5)
CPU Power Dissipation (mw)	925	6 to 40	200	225
Architecture Data Word Size (bits)	Multiple of 4	8	4	4
Instruction Word Size (bits)	9	8, 16, 24	8, 16	8, 16 (Multifunction instr.)
Directly Addressable Instruction Words (No.)		65K	Various	4K
Clock Frequency (Hz/ext. phases required)	to 10 MHz/1 phase	0-6.4 MHz/0 phase		(PPS-4) 256 kHz/2 phase (PPS-4/2) 199 kHz/0 or 2 phase
Register to Register Add Time (μsec/data word)	0.125	2.5 (6.4 MHz clock)		5
No. of Registers Arithmetic	0	1	1	0
Index	0	0	0	0
General Purpose	17	32	1	3
Return Stack Size (No. x bits)	4x4 (2909)	External RAM		2x12
Interrupts	Optional	Standard		Standard PPS-4
Type		1 Level		1 Level
Direct Memory Access	Optional	Standard (on-chip)		None
BCD Arithmetic (Hardware)	No	No	No	No
Microprogrammable	Yes	No	No	No
Extended Temp. Range Available	−55°C to 125°C	−55°C to 125°C Standard		−55°C to 125°C
Devices See System Components:	2900	1800	PPS-4, PPS-8	PPS-4, PPS-8
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes		Yes
Prototyping System (Hardware & software development system)	No	Yes	Yes	Yes
In-System Emulator (Tests system in place)	No	No	Yes	Yes
Software Support (from this manufacturer) Resident Assembler	No	Yes	Yes	Yes
Cross Assembler	Yes	Fortran IV, Timesharing		Fortran IV, Timesharing
Simulator	No	Yes	Yes	Yes
High Level Language	No	No	No	No
Programs Debug	No	Yes	Yes	Yes
Diagnostic	No	Yes	Yes	Yes
Edit	No	Yes	Yes	Yes
User Library (>25 programs from user)	No	No		Yes
Delivery Start (Qtr.-Year)	1 Qtr. 76	1 Qtr. 76	2 Qtr. 76	PPS-4 3 Qtr. 72 PPS-4/2 3 Qtr. 75
Alternate Sources	AMD, Fairchild, Motorola, National, NEC, Signetics	Hughes		
Comments	Microassembler on timeshare.		1-chip parallel microcomputer, several memory options and instruction sets.	The PPS-4/2 is a 2 chip clock, direct display drive, expanded I/O on CPU chip; 128-4 RAM, 2048x8 ROM, 16 I/O ports on separate memory-I/O chip.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Rockwell PPS-8	Rockwell R6500	Signetics N3000 Page 1860	Signetics 2650
General Structure	8-Bit CPU	8-Bit Microcomputer	2-Bit Slice	8-Bit CPU
Type	PMOS	NMOS	TTL	NMOS
No. of Devices per CPU	1	1		1
CPU Size (Pins)	42	28 or 40	28 and 40	40
Supply Voltage	17 (or −12, 5)	5	5	5
CPU Power Dissipation (mw)	225	700	800	525
Architecture Data Word Size (bits)	8	8	Multiple of 2	8
Instruction Word Size (bits)	8, 16, 24 (Multifunction instr.)	8, 16, 24	≥18	8, 16, 24
Directly Addressable Instruction Words (No.)	16K	to 65K	512	32K
Clock Frequency (Hz/ext. phases required)	(PPS-8/2) 189 kHz/0 phase (PPS-8) 256 kHz/2 phase	1 and 2 MHz/0-2 phase	to 6 MHz/1 phase	0 to 1.25 MHz/1 phase
Register to Register Add Time (μsec/data word)	(PPS-8/2) 5 (PPS-8) 4	1		4.8
No. of Registers Arithmetic	1	1	2	0
Index	0	2	0	0
General Purpose	6	0	10	7
Return Stack Size (No. x bits)	32x8	1x8	None	8x15
Interrupts	Standard	Standard	Optional	Standard
Type	3 Level	2 Level	8 Level Priority	Vectored
Direct Memory Access	Optional DMA Controller	Optional	No	Standard
BCD Arithmetic (Hardware)	No	Yes	No	Standard
Microprogrammable	No	No	Yes	No
Extended Temp. Range Available	−55°C to 125°C	No	No	No
Devices See System Components:	PPS-4, PPS-8	6500	3000	2650
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes	No	Yes
Prototyping System (Hardware & software development system)	Yes	Yes	No	Yes
In-System Emulator (Tests system in place)	Yes	Yes	No	Yes
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	No	Yes
Cross Assembler	Fortran IV, Timesharing	Yes	No	Fortran IV, PDP-11
Simulator	Yes	Yes	No	Fortran IV
High Level Language	No	No	No	PLμS
Programs Debug	Yes	Yes	No	Yes
Diagnostic	Yes	Yes	No	Yes
Edit	Yes	Yes	No	Yes
User Library (>25 programs from user)	No	No	No	No
Delivery Start (Qtr.-Year)	PPS-8 1 Qtr. 75, PPS-8/2 2 Qtr. 76	3 Qtr. 77	3 Qtr. 75	2 Qtr. 75
Alternate Sources		MOS Technology, Synertek	Intel	National
Comments		Bus compatible with 6800.	Uses 74S182 for Look-Ahead Carry.	Any of the general purpose registers can be used as an index register.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Signetics 8X02/2901-1 Pages 1851, 1877	Signetics 8X300 Page 1883	Signetics MP8080A	Synertek SY6500
General Structure	4-Bit Slice	8-Bit CPU	8-Bit CPU	8-Bit CPU
Type	TTL	TTL	NMOS	NMOS
No. of Devices per CPU		1	1	1
CPU Size (Pins)	28 and 40	50	40	40 or 28
Supply Voltage	5	5	±5, 12	5
CPU Power Dissipation (mw)	1320	2000	780	200
Architecture Data Word Size (bits)	Multiple of 4	8	8	8
Instruction Word Size (bits)	≥18	16	8, 16, 24	8, 16, 24
Directly Addressable Instruction Words (No.)		8K	65K	65K
Clock Frequency (Hz/ext. phases required)		8 MHz/phase	2 MHz/2 phase	to 2 MHz/1 phase
Register to Register Add Time (μsec/data word)		0.25	2	1
No. of Registers Arithmetic			1	1
Index			0	2
General Purpose	16	8	6	0
Return Stack Size (No. x bits)			External RAM	External RAM
Interrupts	Optional	Yes	Standard	Standard
Type		Polled	Vectored, Multilevel	Vectored, 2 Level
Direct Memory Access	No	Yes	Standard	Optional
BCD Arithmetic (Hardware)	No	No	Yes	Yes
Microprogrammable	Yes	No	No	No
Extended Temp. Range Available	No	Future		−55°C to 85°C
Devices See System Components:	2900	8X300	8080	6500
Hardware Support Processor Cards (CPU system on a card)	No	Yes		Yes
Prototyping System (Hardware & software development system)	No	Yes		Yes
In-System Emulator (Tests system in place)	No	Yes		Yes
Software Support (from this manufacturer) Resident Assembler	No	No		Yes
Cross Assembler	Yes	Yes		Fortran IV
Simulator	No			Fortran IV
High Level Language	No	No		No
Programs Debug	No	No		Yes
Diagnostic	No	Yes		Yes
Edit				No
User Library (>25 programs from user)	No	No		No
Delivery Start (Qtr.-Year)	4 Qtr. 77	3 Qtr. 76	4 Qtr. 77	4 Qtr. 75
Alternate Sources	AMD, Fairchild, Motorola, National, NEC, Raytheon		AMD, Intel, National, NEC, TI	MOS Technology, Rockwell
Comments	The 2901-1 can be used with 2909/2911 sequences as well as the 8X02.	Bipolar with fixed instructions.		DMA based on a stopping CPU, but address bus connections are not 3 state.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Texas Instruments SBP0400A/SBP0401A	Texas Instruments SBP9900	Texas Instruments SN54/74LS481	Texas Instruments SN74S481
General Structure	4-Bit Slice	16-Bit CPU	4-Bit Slice	4-Bit Slice
Type	I^2L	I^2L	TTL-LS	TTL-S
No. of Devices per CPU		1		
CPU Size (Pins)	40	64	48	48
Supply Voltage	200 mA at 0.85V	500 mA	5	5
CPU Power Dissipation (mw)	170	500	1000	2000
Architecture Data Word Size (bits)	9 (Microinstruction Select)	16	Multiple of 4	Multiple of 4
Instruction Word Size (bits)		16, 32, 48	11	
Directly Addressable Instruction Words (No.)	(512 Microinstructions)	32K	Multiple of 4 Bits	
Clock Frequency (Hz/ext. phases required)	to 2 MHz/1 phase	0-3 MHz/1 phase	0-9 MHz/1 phase	0-15 MHz/1 phase
Register to Register Add Time (μsec/data word)	0.5 (2 MHz clock)	4.67	0.11	0.06
No. of Registers Arithmetic	2	16	2	2
Index	0	15	0	0
General Purpose	8	16	16	16
Return Stack Size (No. x bits)	None	None	None	None
Interrupts	Optional	Standard	Optional	Optional
Type	Optional	Vectored, 16 Levels		
Direct Memory Access	Standard	Yes	Standard	Standard
BCD Arithmetic (Hardware)	Microprogrammable	No	Yes	Yes
Microprogrammable	(512 Microinstructions)	No	Yes	Yes
Extended Temp. Range Available	−55°C to 125°C	−55°C to 125°C Standard	−55°C to 125°C	Future
Devices See System Components:	SBP400	9900	54/74LS481	74S481
Hardware Support Processor Cards (CPU system on a card)	No	Yes	Yes	Yes
Prototyping System (Hardware & software development system)	Yes (hardware)	Yes	Future	Future
In-System Emulator (Tests system in place)	No	Yes	No	No
Software Support (from this manufacturer) Resident Assembler	No	Yes	No	No
Cross Assembler	Fortran microassembler	Yes	No	No
Simulator	No	Timesharing	No	No
High Level Language	No	Fortran, Cobol	No	No
Programs Debug	No	Yes	No	No
Diagnostic	No	Yes	No	No
Edit	No	Yes	No	No
User Library (>25 programs from user)	No	Yes	No	No
Delivery Start (Qtr.-Year)	1 Qtr. 75	1 Qtr. 77	1 Qtr. 78	4 Qtr. 77
Alternate Sources	None	None	None	None
Comments	Current drain can be set from 0.001 to 200 mA.	Software compatible with 990 minicomputer.	24780 Micro- and Macro- instructions.	24780 Micro- and Macro- instructions.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Texas Instruments TMS1000/1200	Texas Instruments TMS1070/1270	Texas Instruments TMS1100/1300	Texas Instruments TMS8080
General Structure	4-Bit Microcomputer	4-Bit Microcomputer	4-Bit Microcomputer	8-Bit CPU
Type	PMOS	PMOS	PMOS	NMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	28 or 40	28 or 40	28 or 40	40
Supply Voltage	9 or 15	15	9 or 15	±5, 12
CPU Power Dissipation (mw)	90	100	90	1500
Architecture Data Word Size (bits)	4	4	4	8
Instruction Word Size (bits)	8	8	8	8, 16, 24
Directly Addressable Instruction Words (No.)	1K	1K	2K	65K
Clock Frequency (Hz/ext. phases required)	300 kHz/0 phase	300 kHz/0 phase	300 kHz/0 phase	2 MHz/2 phase
Register to Register Add Time (μsec/data word)	34 (350 kHz clock)	34 (350 kHz clock)	34 (350 kHz clock)	2
No. of Registers Arithmetic	1	1	1	1
Index	0	0	0	0
General Purpose	1	1	1	6
Return Stack Size (No. x bits)	1x10	1x10	1x10	External RAM
Interrupts	None	None	None	Standard
Type				Vectored, 8 Level
Direct Memory Access	None	None	None	Standard
BCD Arithmetic (Hardware)	Microprogrammable	Microprogrammable	Microprogrammable	Yes
Microprogrammable	Yes	Yes	Yes	No
Extended Temp. Range Available		Yes	Yes	No
Devices See System Components:	1000	1000	1000	8080
Hardware Support Processor Cards (CPU system on a card)	No	No	No	No
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	No
In-System Emulator (Tests system in place)	Yes	No	Yes	No
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	Yes	No
Cross Assembler	Timesharing	Yes	Yes	Timesharing
Simulator	Timesharing	Yes	Yes	Timesharing
High Level Language	No	No	No	No
Programs Debug	Yes	Yes	Yes	Yes
Diagnostic	Yes	Yes	Yes	Yes
Edit	Yes	Yes	Yes	Yes
User Library (>25 programs from user)				No
Delivery Start (Qtr.-Year)	1 Qtr. 75	4 Qtr. 75	4 Qtr. 75	2 Qtr. 75
Alternate Sources	None	None	None	AMD, Intel, National, NEC, Signetics
Comments	A 64 pin version, TMS1099/SE-1, permits use of external PROM, RAM or ROM for program development.	35V output drive capability.	A 64-pin version, TMS1098/SE-2 permits use of external PROM/RAM/ROM for program development.	

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Texas Instruments TMS9900	Texas Instruments TMS9980	Toshiba TLCS-12A	Western Digital MP1600
General Structure	16-Bit CPU	8/16-Bit CPU	12-Bit CPU	16-Bit CPU
Type	NMOS	NMOS	PMOS	NMOS
No. of Devices per CPU	1	1	1	3
CPU Size (Pins)	64	40	36	40/device
Supply Voltage	±5, 12	±5, 12	±5	±5, 12
CPU Power Dissipation (mw)	1000	1000	800	600
Architecture Data Word Size (bits)	16	8	12	16
Instruction Word Size (bits)	16, 32, 48	16, 32, 48	12, 24	16
Directly Addressable Instruction Words (No.)	65K bytes/32K words	16K bytes	4K	65K
Clock Frequency (Hz/ext. phases required)	3 MHz/4 phase	2-3 MHz/phase	1.2 MHz/0 phase	3.3 MHz/4 phase
Register to Register Add Time (μsec/data word)	4.67	8.8 (2 MHz)	13	2.7
No. of Registers Arithmetic	16	16	0	4
Index	15	15	0	2
General Purpose	16 (in memory)	16 (in memory)	7	2
Return Stack Size (No. x bits)	None	None		External RAM
Interrupts	Standard	Standard	Yes	Standard
Type	Vectored, 16 Level	Vectored, 6 Level		Vectored
Direct Memory Access	Standard	Standard	Optional	Standard
BCD Arithmetic (Hardware)	No	No	No	Standard
Microprogrammable	No	No	No	Yes
Extended Temp. Range Available	−25°C to 85°C			No
Devices See System Components:	9900	9900	TLCS-12	1600
Hardware Support Processor Cards (CPU system on a card)	Yes 990/4	No	No	Yes
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	No	No	No	No
Software Support (from this manufacturer) Resident Assembler	Yes	Yes		Yes
Cross Assembler	Yes	Timesharing	Yes	No
Simulator	Timesharing	Timesharing	Yes	No
High Level Language	Fortran, Cobol	Fortran, Cobol	Yes	No
Programs Debug	Yes	Yes	Yes	Yes
Diagnostic	Yes	Yes	Yes	Yes
Edit	Yes	Yes	Yes	Yes
User Library (>25 programs from user)	Yes	Yes	Yes	No
Delivery Start (Qtr.-Year)	2 Qtr. 76	4 Qtr. 76	2 Qtr. 74	1 Qtr. 75
Alternate Sources	AMI	AMI	None	None
Comments	Instructions include hardware multiply and divide and are software compatible with 990 minicomputers.	8-Bit data bus, 16-Bit internal op. Software compatible TMS9900.		

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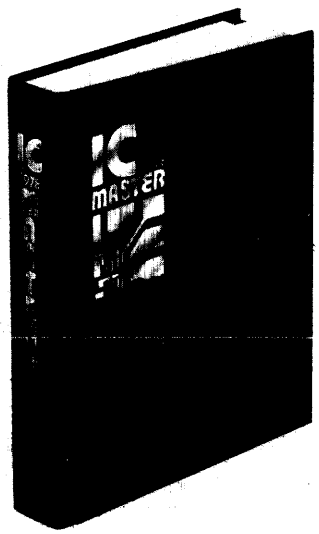
MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Western Digital MCP1600	Zilog Z80
General Structure	8-Bit CPU	8-Bit CPU
Type	NMOS	NMOS
No. of Devices per CPU	3	1
CPU Size (Pins)	40/device	40
Supply Voltage	±5, 12	5
CPU Power Dissipation (mw)	600	1100
Architecture Data Word Size (bits)	8 or 16	8, 16
Instruction Word Size (bits)	16	8, 16, 24, 32
Directly Addressable Instruction Words (No.)	65K (84 Microinstructions)	65K
Clock Frequency (Hz/ext. phases required)	3.3 MHz/4 phase	2.5 MHz/1 phase (4 MHz opt.)
Register to Register Add Time (μsec/data word)	0.3 (8-Bit), 0.6 (16-Bit)	1.6 (2.5 MHz clock)
No. of Registers Arithmetic	0	1
Index	0	2
General Purpose	26	14
Return Stack Size (No. x bits)	External RAM	External RAM
Interrupts	Standard	Standard
Type	Vectored, 4 Level	Vectored, Multilevel
Direct Memory Access	Standard	Z80-DMA
BCD Arithmetic (Hardware)	Microprogrammable	Yes
Microprogrammable	Yes	No
Extended Temp. Range Available	No	−55°C to 125°C
Devices See System Components:	1600	Z80
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes
Prototyping System (Hardware & software development system)	Yes	Yes
In-System Emulator (Tests system in place)	Yes	Yes
Software Support (from this manufacturer) Resident Assembler	No	Yes
Cross Assembler	Timesharing, PDP-11	Fortran IV
Simulator	Timesharing, PDP-11	Timesharing
High Level Language	No	PL/Z
Programs Debug	Yes	Yes
Diagnostic	Yes	Yes
Edit	Yes	Yes
User Library (>25 programs from user)	No	No
Delivery Start (Qtr.-Year)	3 Qtr. 75	1 Qtr. 76
Alternate Sources	None	Mostek, NEC
Comments	Can cross assemble and simulate with DEC PDP-11. Microcontroller version available.	8080A Software compatible.

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The AMI S6800 Microcomputer Systems Family

Part No.	Description	Process	Power Supplies	Input/ Output	Packages
S68A00	8-Bit Microprocessor (1.5MHz Clock Rate)	N-SiGate	+5V	TTL	40 Pin Side Brazed
S68B00	8-Bit Microprocessor (2.0MHz Clock Rate)	N-SiGate	+5V	TTL	40 Pin Side Brazed
S68A10	1024 Bit (128x8) Static Read/Write Memory (360ns Access Time)	N-SiGate	+5V	TTL	24 Pin Side Brazed
S68B10	1024 Bit (128x8) Static Read/Write Memory (250ns Access Time)	N-SiGate	+5V	TTL	24 Pin Side Brazed
S68A21	Peripheral Interface Adapter (PIA)	N-SiGate	+5V	TTL-CMOS	40 Pin Side Brazed
S68B21	Peripheral Interface Adapter (PIA)	N-SiGate	+5V	TTL-CMOS	40 Pin Side Brazed
S6831	16,384 Bit (2048x8) ROM	N-SiGate	+5V	TTL	24 Pin P, E, C*
S6831A	16,384 Bit (2048x8) ROM	N-SiGate	+5V	TTL	24 Pin P, E, C*
S6831B	16,384 Bit (2048x8) ROM	N-SiGate	+5V	TTL	24 Pin P, E, C*
S6831C	16,384 Bit (2048x8) ROM	N-SiGate	+5V	TTL	24 Pin P, E, C*
S6834	4096 Bit (512x8) Erasable and Electrically Reprogrammable ROM	P-SiGate	+5V, -12V	Three-State	24 Pin Ceramic
S68A50	Asynchronous Communication Interface Adapter (ACIA)	N-SiGate	+5V	TTL	24 Pin Side Brazed
S68B50	Asynchronous Communication Interface Adapter (ACIA)	N-SiGate	+5V	TTL	24 Pin Side Brazed

S2000/S2000A

The S2000 is a fast, flexible 4-bit microcomputer which is completely self-contained with ROM, RAM, processor and input/output on one chip. Its design allows easy expansion of program storage through off-chip ROM or PROM and gives access to all internal registers and memory for debug and test.

The AMI S9900 Microcomputer Systems Family

Part No.	Description	Process	Power Supplies	Input/ Output	Package
S9900	16-Bit Single Chip Microprocessor	N-SiGate	+12V, ± 5V	TTL	64 Pin Package
S9901	Programmable Systems Interface Circuit	N-SiGate	+5V	TTL	40 Pin Package
S9902	Asynchronous Communications Controller (ACC)	N-SiGate	+5V	TTL	18 Pin Package
S9903	Synchronous Communications Controller (SCC)	N-SiGate	+5V	TTL	20 Pin Package
S9940	16-Bit Single Chip Microcomputer	N-SiGate	+5V	TTL	18 Pin Package
S9980	16-Bit Single Chip Microcomputer	N-SiGate	+5V	TTL	40 Pin Package

*(P) = Plastic Package, (E) = Cer-DIP Package, (C) = Ceramic Package

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S6800 Microcomputer Systems

The AMI S6800

The AMI S6800 Microprocessing Family hardware includes a microprocessor, ROM and RAM memories, and data input/output circuits. These components may be assembled in a building block manner into a very simple microcomputer system or into any of progressively more complex systems, which can be used in many general or special purpose applications. The important feature of the S6800 family is that within any system all components are directly compatible in signal functions, circuit performance characteristics, and logic levels. All operate on a single +5V power supply.

It remains to the user to integrate the microcomputer into his own large system and to program it for a specific task. The task may be either simple or complex and either general in purpose or highly specialized for one application.

To facilitate system design and programming, AMI will provide a comprehensive set of reference documents, design and programming aids, a program library, and other applications support. For example, AMI will make available a comprehensive hardware and software reference manual, a S6800 program assembler, and a simulator. Such design and programming support is a continuing and expanding effort at AMI.

S6800 — 8-Bit Microprocessor

The S6800/S68A00/S68B00 is an 8-bit parallel processor with the ability to address up to 65K bytes of memory and execute instructions in two microseconds. It is manufactured using N-channel MOS technology and operates on a single +5V power supply. All inputs and outputs are TTL compatible. The MPU has six internal registers, four types of vectored interrupts and 72 basic instructions. The basic instructions can be used in different addressing modes to save instruction execution time and memory space.

Another important advantage that the S6800/S68A00/S68B00 has to offer in comparison with any other microcomputer system is input/output versatility. In any computer system, large or small, the CPU internal functions are determined by its architecture and the user usually has little opportunity or need to alter them. On the other hand, the I/O configuration is almost always determined by the user and subject to change as peripherals are added or other system alternations are introduced.

S68A10/S68B10 — 1024 Bit (128x8) Static Read/Write Memory

The S68A10 and S68B10 are static Read/Write memories designed and organized to be compatible with the S68A00 and S68B00 microprocessors. Interfacing to the S68A10 and S68B10 consists of an 8-bit bi-directional data bus, seven address lines, a single Read/Write control line, and six chip enable lines, four negative and two positive.

For ease of use, the S68A10 and S68B10 are totally static memories requiring no clocks or cell refresh. The S68A10 and S68B10 are fabricated with N-channel silicon gate depletion load technology to be fully DTL/TTL compatible with only a single +5V power supply required. The data, address and control line organization and functions of the S68A10 and S68B10 match those of the MPU.

S68A21/S68B21 — Peripheral Interface Adapter (PIA)

The S68A21/S68B21 are peripheral interface adapters that provide the univeral means of interfacing peripheral equipment to the S68A00 and S68B00 Microprocessing Units (MPU). These devices are capable of interfacing the MPU to peripheral through two 8-bit bi-directional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

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The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

The PIA interfaces to the S68A00/S68B00 MPUs with an 8-bit bi-directional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals in conjunction with the S68A00/S68B00 VMA output permit the MPU to have complete control over the PIA. VMA may be utilized to gate the input signals to the PIA.

S6831/A/B/C — 16,384 Bit (2048x8) Read Only Memory

The S6831/A/B/C is a 16,384-bit Read Only Memory organized 2K words by 8 bits. This ROM has been designed to supply large bit storage, high performance memory for microprocessors and other demanding applications with simple interface requirements. The device will operate from a single +5V power supply and is manufactured with N-channel silicon gate depletion load technology. This device is available in all common high-density ROM pinouts.

S6834 — 4096 Bit (512x8) Erasable and Electrically Reprogrammable ROM

The S6834 is a high-speed, static, 512x8 bit, erasable and electrically programmable read only memory designed for use in bus-organized systems. Both input and output are TTL compatible during both read and write modes. Packaged in a 24-pin hermetically sealed dual in-line package, the bit pattern can be erased by exposing the chip to an ultra-violet light source through the transparent lid, after which a new pattern can be written. The device has +5V and -12V power supplies and is processed using a mature P-channel process.

S68A50/S68B50 — Asynchronous Communication Interface Adapter (ACIA)

The S68A50/S68B50 Asynchronous Communication Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data communications to bus organized systems such as the S68A00/S68B00 Microprocessing Units.

The S68A50/S68B50 includes select enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. Word lengths, clock division ratios and transmit control through the Request-to-Send output may be programmed. For modem operation three control lines are provided.

Basic S6800 Microcomputer System

In a basic system built with the S6800 components the S6800/S68A00/S68B00 Microprocessor is supported by over 1K bytes of memory and controls one input/output interface circuit. The 1024-byte ROM is used to store the operating program, the 128-byte RAM provides working storage for the MPU, and the Peripheral Interface Adapter (PIA) provides two independently programmable 8-bit input/output ports for communicating with two peripheral devices.

The S6800 system is bus oriented. Eight lines from the data bus and 16 more lines make up the address bus. The MPU controls the bus and all other devices — the memories and the PIA — attach to the busses and wait for instructions from the MPU to supply or receive data.

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The basic system is a complete microcomputer, which can be used for a large variety of applications. It is simple but versatile, because it can be easily reprogrammed by changing the ROM. The user must provide only the two-phase clock signal source, a power-up/restart circuit, and a single +5V power supply to complete the hardware.

Expanding the S6800 System

The basic system can be altered or expanded in many different ways. For example, the S68A50/S68B50 Asynchronous Communication Interface Adapter (ACIA) can be substituted for the PIA, to enable the microcomputer to interface with a telecommunications modem. Or, additional memory can be added — either RAM or ROM — to expand the processing capability of the MPU. In general, the system can be expanded in a modular manner, by adding onto the bus as many as ten devices out of the S6800 family. These can be any combination of memory or input/output interface circuits. In this manner a system of nearly any complexity and configuration can be assembled. (Systems with more than ten devices on the bus require the addition of address and data bus buffers to operate at full speed.)

By building a microcomputer from the S6800 family of devices, advantage is taken of the compatibility of the devices. They all conform to the bus discipline, all are compatible in load levels, and the entire system runs on a common system clock. In effect you eliminate most all circuit design, save for the simple clock and power-up/restart circuits. Because you are dealing with only a small number of integrated circuits, circuit layout is simple and the entire microcomputer can be located on a single circuit card.

In some special purpose applications you may need to attach your own interface devices to the bus. As a result, more circuit design will be required, but you will find the S6800 MPU easy to work with. It has features that allow it to be used in many different systems. For example, by using the Halt, Three-State Control, and Data Bus Enable lines, you can easily design a direct memory access system in which either the MPU or a peripheral device can read or write into the RAM and utilize the bus on a priority basis. You can also design a multiprocessor system in which several MPUs can be attached to the same bus and share processing assignments as well as memory space.

S6800 Input/Output

One of the most important advantages that any S6800 system has to offer is its input/output versatility.

In a S6800 system the MPU relegates most of the I/O control to such I/O interfaces as the PIA or ACIA. Each of these circuits is programmable and can interface with peripheral devices without directly involving the MPU. For example, the MPU can preprogram a PIA to either output data to the MPU or to receive it. Thereafter, the PIA circuits assume all functions of interfacing with the peripherals and the MPU never has to look at the interface until service is required. It must service interrupts from the PIA, but never needs to wait for input data to become available or for output data to be accepted. This relieves the MPU of its I/O functions, makes it more efficient in its primary task of data processing, and significantly increases system throughput.

The I/O interfaces and memory are both located in the same address space with the S6800 system. The MPU can access any I/O device the same as a memory location — with address lines, instead of separate I/O control lines. Therefore, it can manipulate data in the I/O interface registers with the same programmed instructions as it uses for memory locations. This adds flexibility and increases system efficiency.

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The S6800 Instruction Set complements the above I/O addressing capability with specific instructions that can be used to access memory as well as I/O circuit registers and perform directly various manipulations on the data.

S6800 Instruction Set

The S6800 MPU has a set of 72 basic instructions. These include binary and decimal arithmetic functions as well as logical, shift, rotate, load, store, branch, interrupt, and stack manipulation functions. Most of the instructions have several variations and most can be used with several memory addressing modes. The total complex of instructions available to the programmer is actually 197.

An instruction can be from one to three bytes long, depending on the addressing mode used with the instruction. The first byte always contains the operation code, which designates the kind of operation the MPU will perform. In single byte instructions no memory address is required, because the operation is performed on one of the internal MPU registers. In multiple byte instructions the second and third byte can be the operand, or a memory address for the operand.

A noteworthy feature of the S6800 MPU is that some of the instructions can operate directly on any memory location. In other computer systems it is common that the processor fetches an operand from memory, stores it in the accumulator, then executes the operation in the ALU and finally writes the result back into the memory. The S6800 is able to accomplish the same with only a single instruction, because it operates with any external location in the same manner as with an internal register. For example, it can directly increment or decrement the contents of a memory location. Because the MPU addresses I/O devices just like a memory location, it can do the same with registers inside the PIA or ACIA. The ASL, ASR, LSR, and ROL are other examples of instructions which operate in this manner.

MPU Registers

Accumulators A and B — Two separate 8-bit accumulators that are used to hold operands and results of operations in the ALU.

Index Register — A 16-bit register used for memory address storage in Indexed Addressing operations.

Program Counter — A 16-bit register that holds the current program instruction address. Once the initial program starting address is loaded into the program counter, it is incremented under control of the MPU hardware.

Stack Pointer — A 16-bit register used for storage of the next available location in an external push-down/pop-up stack.

Condition Code Register — An 8-bit register that stores certain results of operations in the ALU. These bits are used as testable conditions for the conditional branch instructions. In addition, one bit position stores the interrupt mask bit and the two high order bits are unused.

Memory Register

External Stack — The MPU uses a push-down/pop-up stack that can be located anywhere in RAM and be of any convenient size. It is accessed with the stack pointer address and has several uses. First, it always stores the MPU register contents following an interrupt and return addresses during subroutine execution. Second, it can also be used by the programmer to store data during program execution.

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Microcomputer Development Center

What is the AMI MDC?

The AMI MDC (Microcomputer Development Center) is an intelligent stand-alone hardware debugging and software development station serving the combined needs of the engineer and programmer.

The MDC-100 is the ideal tool for design projects. The standard configuration includes an integrated terminal/computer unit and a dual floppy disk drive.

With the 16K of RAM supplied (expandable to 48K), and the remarkable display-oriented Text Editor, a source program can be created or modified very quickly. Then a Macro Assembler — one for the S6800 and another for the S2000 — can generate an object program.

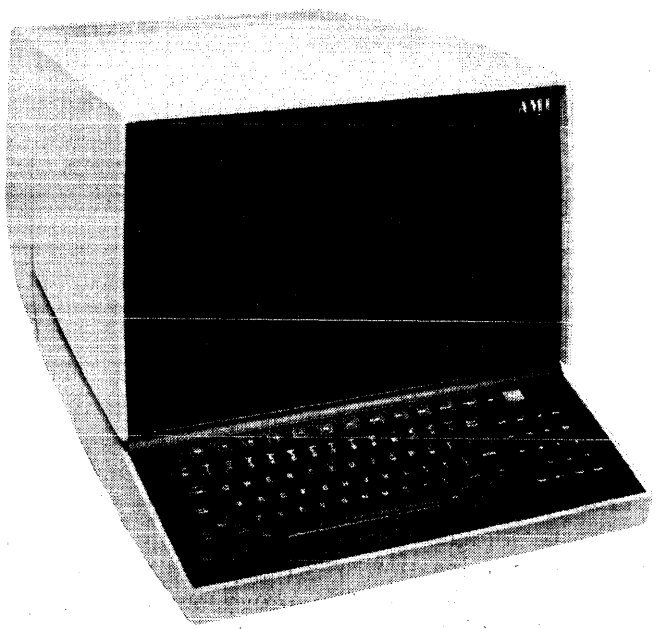
The MDC's free software also support debugging with breakpoints and single steps, tracing with mnemonic disassembly, and file exchange between the floppies and a communications interface. The purchase of other software can be arranged.

A "burner" for AMI EPROMs is built into every MDC and options for some other EPROMs are available.

S2000 designers can connect the MDC to a running prototype by using the DEV-2000 Debug Module. The SES-2000 Hardware Emulator Module with its own memory can be used as a stand-alone emulator.

The MDC-140 is a general-purpose Logic Analyzer which plugs into the MDC-100. The analyzer's trace memory holds 1024 steps. All patterns are 40 channels wide — two separate event qualifiers, a data-dependent clock, and an outbound trigger.

Operation is software-controlled through the MDC's keyboard and screen, including the creation and disk storage of user-defined display formats



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in any mixture of binary, octal, hex, ASCII, and mnemonics.

A special keyboard design is specifically oriented toward the Development Center's function. The full ASCII keyboard with auxiliary keypad, specia. function keys and cursor controls allow rapid data entry, screen manipulation and editing.

A 16-position card cage and suitable power supply are contained in the intelligent terminal chassis so that the Development Center's options can fit inside the terminal.

A dual drive IBM-compatible floppy disk mass storage system is housed in a separate chassis. It communicates with the intelligent terminal and permits 512 kilobytes of additional on-line storage.

The AMI MDC completely eliminates the need for paper tape and offers far superior throughput over paper tape and cassette based systems. A powerful disk based operating and file management system is included to provide rapid software development. A typical edit/assembly sequence is reduced from hours in a paper tape system to minutes with the MDC.

The AMI MDC is a multi-function development center that single-handedly satisfies your requirements for:

Software Development — with a full complement of support software including FDOS-II Operating and File Management System, Text Editor, Assembler, Debugger, Trace, Telecommunications and Utilities.

Hardware Development — with remote front panel and ROM simulator functions and a modular bus-oriented PC card cage supported by general purpose breadboard cards, Extender cards, EPROM programming capability and MDC self-testing firmware.

Prototype Checkout — with the advantages of a real-time test environment, rapid test program retrieval, single/multiple step execution and hardware and software breakpoints.

The AMI Development System Concept

- Multifunctional, modular and expandable to serve not just some, but all system development needs; with simple, problem-free expandability.

- Ready-to-use, easy-to-use. Plug in and go. Simple, easy to learn means error-free operation.

- Rapid, but quiet terminal response. No long waiting for responses to operator actions. No loud pounding of print hammers to deafen and distract the operator. A fast CRT.

- Mass storage with disk-based operating system to end the problems of running out of memory, loading programs, and storing files. A removable storage media with full operating system support.

- Immediate access to stored programs with file management support to move quickly from one development phase to another. To draw instantly from a pool of development support software. A program library of development aids at your fingertips.

- Complete software development support to include everything necessary for the effective generation of microcomputer based software, beginning with a Disk Operating System and including text editor, assembler, debugger, trace and more.

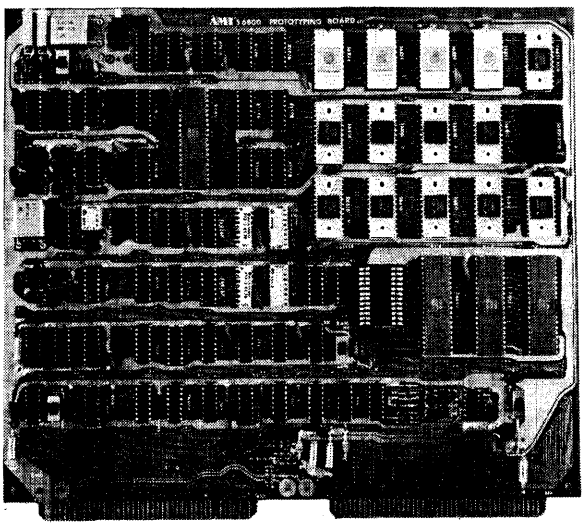
- Complete hardware development support to solve prototype development and test problems. A bus-oriented card cage, common plug-in modules, wire wrap module, extender card, EPROM programmer and complete control-panel-type functions such as single step, stop-on-address, display, alter, and more.

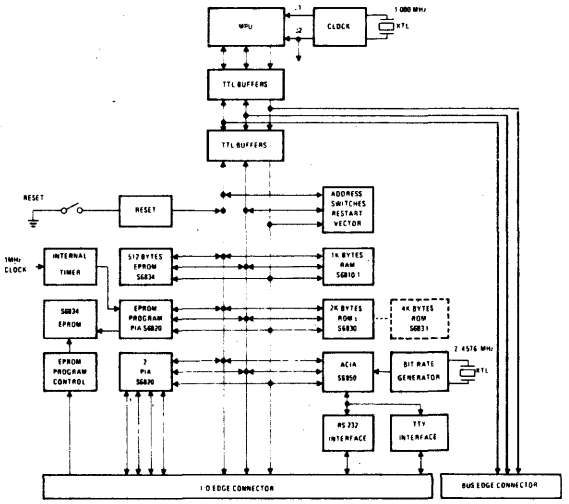
The AMI Floppy Disk drive is designed to be interchangeable with an IBM 3540 or 3740 system. The recording mode is Frequency Modulation (double frequency recording) to assure high reliability. The AMI FDOS-II Floppy Disk Operating and File Management System work in conjunction with the MDC to provide unique features designed for direct use with microcomputers and microprocessors.

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EVK99
EVK100
EVK200
EVK300

ADVANCED PRODUCT DESCRIPTION





77680 BLOCK DIAGRAM

FEATURES

- 2K Bytes ROM (Expandable to 4K Bytes)
- 512 Bytes EPROM (Expandable to 2K Bytes)
- 1K Bytes RAM
- EPROM Programming for S6834
- 3 PIA's = 58 I/O lines
- TTY Current Loop or RS232 Interface
- TTY Operating System Program
- ROM Subroutine Program Library
- Totally Buffered MPU Lines
- Single +5V Power Supply except when using EPROMs or RS232 Interface
- Restart Address Selection
- Selectable DMA Mode
- Interval Timer (100μs or 1 ms)
- Tiny Basic

FUNCTIONAL DESCRIPTION

The EVK 200 Prototyping Board is a kit for a single PCB, hardware/software prototyping system. It allows system development using a functionally compatible system and reduced development time. With this board, the basic 6800 family parts (S6800, S6810-1, S6820, S6831, S6834 and S6850) can be evaluated. It can also serve as a general purpose microcomputer for low volume systems to which the user can easily add I/O and memory. The 10½" x 12" card has two edge connectors, one for the MPU Bus and one for I/O.

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FUNCTIONAL DESCRIPTION (Cont.)

All of the S6800 microprocessor lines are available at the bus edge connector and are buffered to allow 40 mA of drive capacity for expanding the development system. The standard system clock is adjustable from 300 kHz to 1MHz by using the potentiometers on the board. An optional 1 MHz crystal may be selected to control the accuracy for those applications requiring critical timings.

An on-board interval timer gives 1 ms and 100μs timing marks for general use and for EPROM programming. Three types of DMA operation are possible using the Prototyping Board, Halt Processor, Cycle Steal or Multiplexing.

MEMORY

Memory and I/O addresses are assigned to the upper 8K bytes of the available memory space. (See memory map for address assignments.) This gives the system developer the flexibility to use the remaining 56K bytes as he wishes. All of the memory and I/O on the board may be disabled externally by an edge connector line called MEMORY DISABLE, leaving the MPU free to operate totally in an external memory.

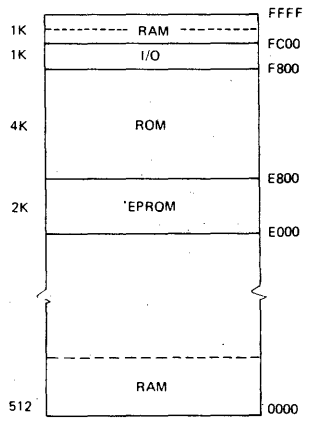
The S6831 ROM contains the Prototype Operating Library (PROTO) and a ROM Subroutine Library $(RS)^3$. The 2K of EPROM locations may also be used for program verification. The S6831 ROM locations (2K x 8 each) will expand the ROM capacity to 4K bytes.

The RAM is assigned to the upper 1K of available memory space. The PROTO and $(RS)^3$ programs require about 256 bytes of this RAM so the rest is available for general programming. With all restart vectors automatically assigned to the upper memory addresses, restart vectoring is forced from a set of 16 switches. This allows the restart address to be vectored to any memory location.

The RAM has further been divided into two 512 byte sections such that the upper 512 bytes remain fixed in the assigned address block and the lower 512 bytes are moveable through a switch selection option. 512 bytes of RAM are relocatable to the lowest address space to take advantage of the S6800's direct addressing mode. This is only recommended if no external memory is added. When adding external memory, it is advisable to use the RAM in the upper address space and the external memory as the low addresses.

There are 512 bytes of ultra-violet erasable EPROM supplied with the board. The board has capacity for four S6834 EPROMs giving a total memory space of 2K bytes for further expansion.

ADDRESS ASSIGNMENT MEMORY MAP



1176164

*Optional Low order RAM assignment

I/O

An S6850 ACIA is used to provide a 20 mA current loop interface to a TTY or RS232 terminal. A 20 mA current loop interface and an EIA RS232 interface are both available on the board. A bit rate generator allows operation using any of the standard communication frequencies (see table) so a large variety of terminal types can be used.

Three S6820 PIAs allow up to 58 I/O lines, giving flexibility in I/O through the parallel interfaces.

TABLE

Communication Frequencies

50	baud	300	baud	19.2K baud
75	baud	600	baud	
110	baud	1200	baud	
134.5	baud	1800	baud	
150	baud	2400	baud	
200	baud	4800	baud	
		9600	baud	

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EPROM PROGRAMMING

Unique to the AMI 6800 Prototyping Board is the ability to program S6834 EPROMs (512 x 8) on the board. The programming software can program an EPROM from any memory location, RAM, ROM or EPROM. It can verify a word and, if desired, change a single bit in the EPROM, provided that the change is from LOW to HIGH.

SOFTWARE

The Prototyping Board Software is comprised of a TTY Operating Program (PROTO) and is supported by a ROM Subroutine Library $(RS)^3$. The PROTO program operates on the following commands:

L	Load Memory from TTY paper tape
P	Punch a Memory location to TTY paper tape
S	Set Memory to a given value
D	Display the contents of a memory location
G	Go to a specific address and begin program execution
R	Print contents of MPU registers on the TTY
B	Burn (program) an EPROM from Memory location indicated
V	Verify the contents of an EPROM with a specified memory location
I	Input Program EPROM to RAM
M	Move a specific block of memory to a designated location
E	End of Transmission (EOT)

The commands will operate on a single character op code plus address parameters from the TTY keyboard.

The ROM Subroutine Library $(RS)^3$ operates on a single SWI (3F) command and a second byte of offset giving the S6800 an additional set of two-byte instructions. Specific subroutines (offsets) are as follows.

SUBROUTINE	MNEMONIC	FUNCTION
0	PUSHALL	All registers are pushed on to user stack
1	POPALL	All registers on user stack are loaded into MPU
2	TXAB	Contents of Index Register are transferred to A & B Accumulators
3	TABX	Contents of A & B Accumulators are transferred to Index Register
4	XABX	Contents of A & B Accumulators are exchanged with contents of Index Register
5	PUSX	Contents of Index Register are pushed onto user stack
6	PULX	Index Register is loaded with contents of user stack
7	ADDXAB	Contents of Index Register are added to contents of A & B Accumulators. Sum is in A & B Accumulators.
8	ADDABX	Contents of A & B Accumulators are added to contents of Index Register. Sum is in Index Register
9	ADDAX	Contents of Accumulator A are added to contents of Index Register. Sum is in Index Register

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SUBROUTINE	MNEMONIC	FUNCTION
A	ADDBX	Contents of Accumulator A are added to contents of Index Register. Sum is in Index Register
B	SUBXAB	Contents of Index Register are subtracted from contents of A & B Accumulators. Remainder is in Accumulators A & B
C	SUBABX	Contents of Accumulators are subtracted from contents of Index Register. Remainder is in Index Register
D	SUBAX	Contents of Accumulator A are subtracted from contents of Index Register. Remainder is in Index Register.
E	SUBBX	Contents of Accumulator B are subtracted from contents of Index Register. Remainder is in Index Register
F	P2HEX	Two Hexidecimal Characters (one MPU byte) are printed on the TTY
10	P4HEX	Four Hexidecimal Characters (two MPU bytes) are printed on the TTY
11	PRINTA	ASCII Character designated is printed on TTY
12	PMESS	Message designated is printed on TTY
13	VALAN	Character (byte) is checked to see if it is a valid alpha/numeric character
14	INPUTA	ASCII Character at TTY is input to MPU
15	CONHB	ASCII Character string is scanned looking for a valid Hexidecimal number. Binary equivalent is returned in Accumulators A & B
16	INDEX	Contents of Accumulator A are multiplied with the contents of Accumulator B and the product is added to the contents of the Index Register
17	MUL8	Contents of Accumulator A are multiplied with the contents of Accumulator B. Product remains in both Accumulators

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8-Bit Microprocessor

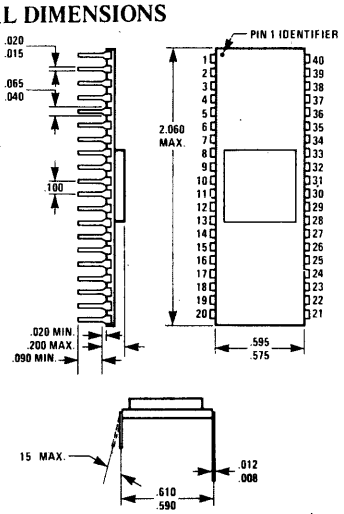
FEATURES

- Eight-Bit Parallel Processing
- Bi-Directional Data Bus
- Sixteen-Bit Address Bus – 65536 Bytes of Addressing
- 72 Instructions – Variable Length
- Seven Addressing Modes – Direct, Relative, Immediate, Indexed, Extended, Implied and Accumulator
- Variable Length Stack
- Vectored Restart
- 2 Microsecond Instruction Execution
- Maskable Interrupt Vector
- Separate Non-Maskable Interrupt – Internal Registers Saved in Stack
- Six Internal Registers – Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- Direct Memory Access (DMA) and Multiple Processor Capability
- Clock Rates – S68A00 – 1.5 MHz
  S68B00 – 2.0 MHz
- Simple Bus Interface Without TTL
- Halt and Single Instruction Execution Capability

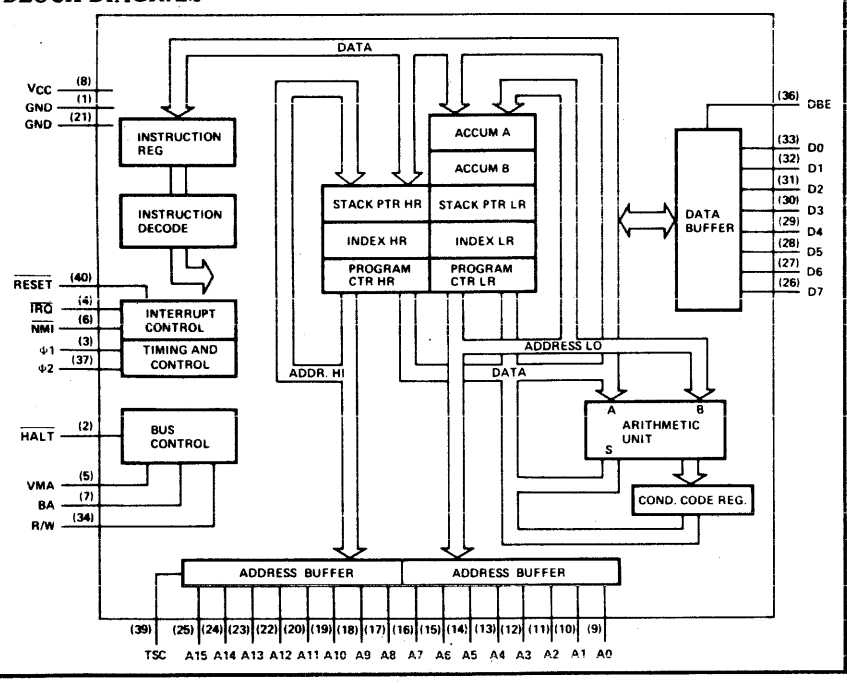
ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}
Input Voltage V_{IN} . . . . . -0.3V to +7.0V
Operating Temperature Range T_A . . . . . 0°C to +70°C
Storage Temperature Range T_{stg} . . . -55°C to +150°C

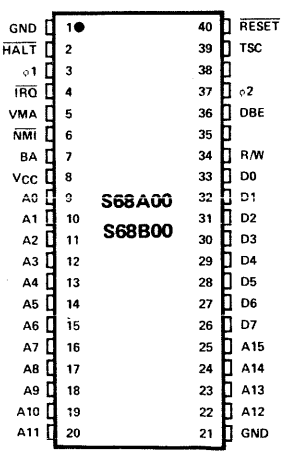
PHYSICAL DIMENSIONS



BLOCK DIAGRAM



PIN CONFIGURATION



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ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, ± 5%, V_{SS} = 0, T_A unless otherwise noted.)

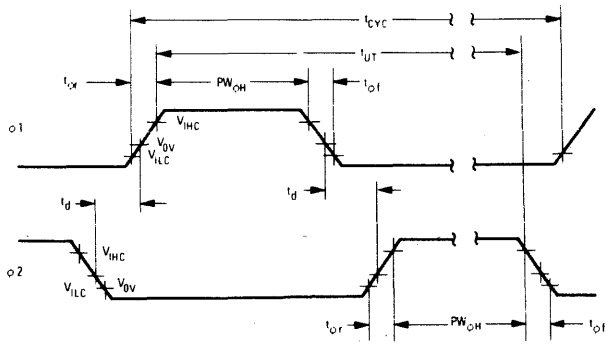
SYMBOL	CHARACTERISTICS		MIN	TYP	MAX	UNIT
V_{IH} V_{IHC}	Input High Voltage (Normal Operating Levels)	Logic $\phi1, \phi2$	V_{SS} + 2.0 V_{CC} - 0.6	– –	V_{CC} V_{CC} + 0.3	Vdc
V_{IL} V_{ILC}	Input Low Voltage (Normal Operating Levels)	Logic $\phi1, \phi2$	V_{SS} - 0.3 V_{SS} - 0.3	– –	V_{SS} + 0.8 V_{SS} + 0.4	Vdc
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.25V, V_{CC} = Max) (V_{IN} = 0 to 5.25V, V_{CC} = 0.0V)	 Logic* $\phi1, \phi2$	 – –	 1.0 –	 2.5 100	μAdc
I_{TSI}	Three-State (Off State) Input Current V_{IN} = 0.4 to 2.4V, V_{CC} = Max	D0 – D7 A0 – A15, R/W	– –	2.0 –	10 100	μAdc
V_{OH}	Output High Voltage (I_{LOAD} = - 205μAdc, V_{CC} = Min) (I_{LOAD} = - 145μAdc, V_{CC} = Min) (I_{LOAD} = - 100μAdc, V_{CC} = Min)	 D0 – D7 A0 – A15, R/W, VMA BA	 V_{SS} + 2.4 V_{SS} + 2.4 V_{SS} + 2.4	 – –	 – –	Vdc
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mAdc, V_{CC} = Min)		–	–	V_{SS} + 0.4	Vdc
P_D	Power Dissipation		–	0.5	1.0	W
C_{IN}	Capacitance # (V_{IN} = 0, T_A = 25°C, f = 1.0 MHz)	 $\phi1$ $\phi2$ D0 – D7 Logic Inputs	 – – – –	 – – 10 6.5	 35 70 12.5 10	pF
C_{OUT}		A0 – A15, R/W, VMA	–	–	12	pF
f	Frequency of Operation	S68A00 S68B00	0.1 0.1	 –	1.5 2.0	MHz
t_{CYC}	Clock Timing (Figure 1) Cycle Time	S68A00 S68B00	0.666 0.50	– –	10 10	μs
$PW_{\phi H}$	Clock Pulse Width Measured at V_{CC} - 0.6V	$\phi1, \phi2$ – S68A00 $\phi1, \phi2$ – S68B00	230 180	– –	9500 9500	ns
t_{UT}	Total $\phi1$ and $\phi2$ Up Time	S68A00 S68B00	600 440	– –	– –	ns
$t_{\phi r}, t_{\phi f}$	Rise and Fall Times Measured between V_{SS} + 0.4 and V_{CC} - 0.6		5.0	–	100	ns
t_d	Delay Time or Clock separation Measured at V_{OV} = V_{SS} + 0.6V		0	–	9100	ns

**Except $\overline{IRQ}$ and $\overline{NMI}$, which require KΩ pullup load resistor for wire-OR capability at optimum operation.*
#Capacitances are periodically sampled rather than 100% tested.

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READ/WRITE TIMING

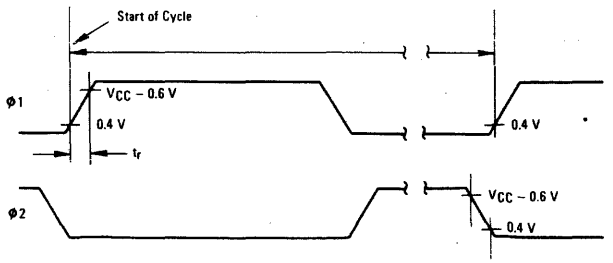
SYMBOL	CHARACTERISTICS		S68A00			S68B00		UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{AD}	Address Delay							ns
	C = 90 pF	–	–	180	–	–	150	
	C = 30 pF	–	–	165	–	–	135	
t_{ACC}	Peripheral Read Access Time $t_{AC} = t_{UT} - (t_{AD} + t_{DSR})$	–	–	360	–	–	250	ns
t_{DSR}	Data Setup Time (Read)	60	–	–	40	–	–	ns
t_H	Input Data Hold Time	10	–	–	10	–	–	ns
t_H	Output Data Hold Time	10	25	–	10	25	–	ns
t_{AH}	Address Hold Time (Address, R/W, VMA)	10	75	–	10	75	–	ns
t_{EH}	Enable High Time for DBE Input	280	–	–	220	–	–	ns
t_{DDW}	Date Delay Time (Write)	–	165	200	–	–	160	ns
	Processor Controls							
t_{PCS}	Processor Control Setup Time	200	–	–	200	–	–	ns
t_{PC_r}, t_{PC_f}	Processor Control Rise and Fall Time	–	–	100	–	–	100	ns
t_{BA}	Bus Available Delay	–	–	270	–	–	270	ns
t_{TSE}	Three-State Enable	–	–	40	–	–	40	ns
t_{TSD}	Three-State Delay	–	–	270	–	–	270	ns
$t_{\overline{DBE}}$	Data Bus Enable Down Time During $\phi 1$ Up Time	150	–	–	70	–	–	ns
t_{DBE_r}, t_{DBE_f}	Data Bus Enable Rise and Fall Times	–	–	25	–	–	25	ns



777229

CLOCK TIMING WAVEFORM

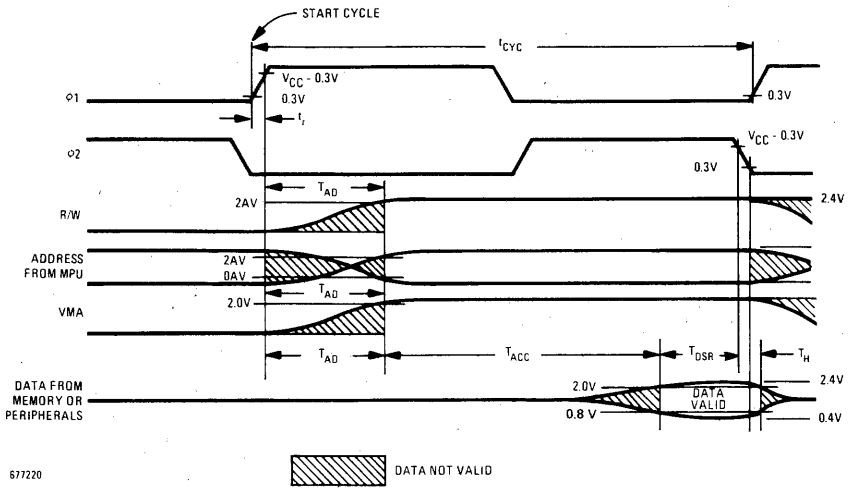
Measurement point for $\phi 1$ and $\phi 2$ are shown below. Other measurements are the same as for MC6800.



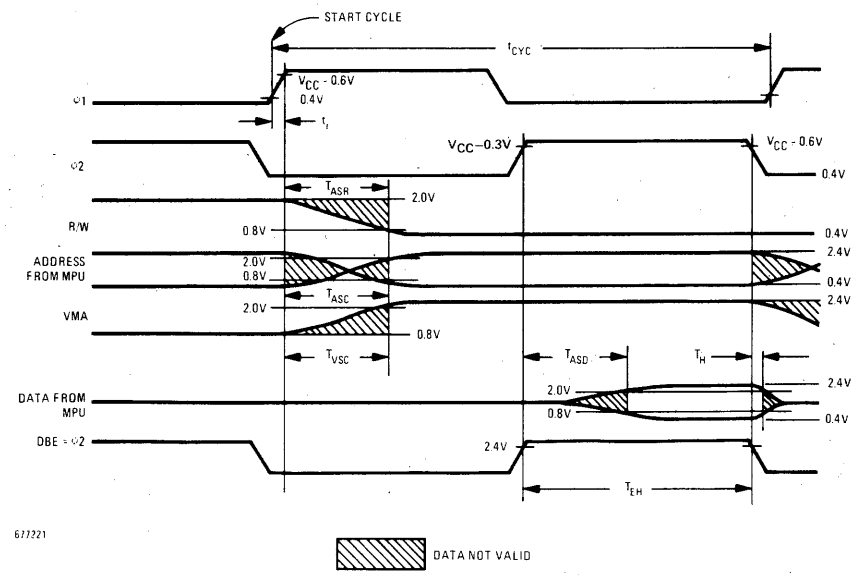
877235

READ/WRITE TIMING WAVEFORM

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READ DATA FROM MEMORY OR PERIPHERALS



WRITE DATA IN MEMORY OR PERIPHERALS

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1024 Bit (128×8) Static Read/Write Memory

Features

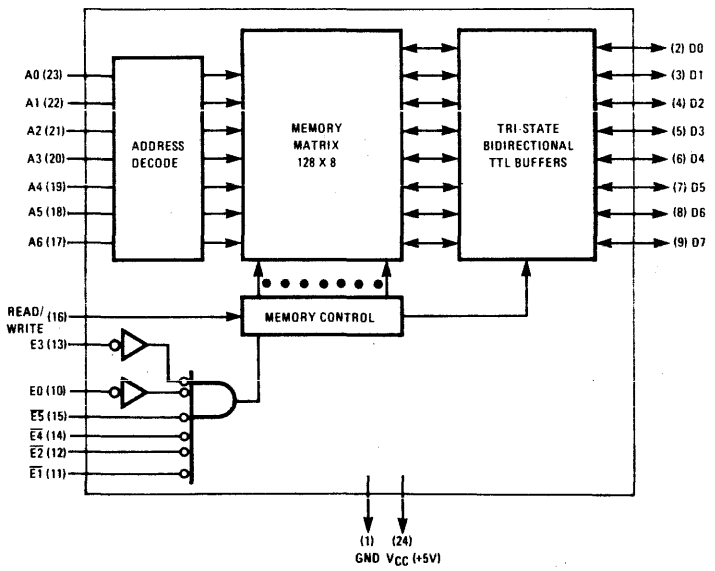
- ☐ Organized as 128 Bytes of 8 Bits
- ☐ Static Operation
- ☐ Bidirectional Three-State Data Input/Output
- ☐ Six Chip Enable Inputs (Four Active Low, Two Active High)
- ☐ Single 5 Volt Power Supply
- ☐ TTL Compatible
- ☐ Maximum Access Time:
  —360ns for S68A10
  —250ns for S68B10

General Description

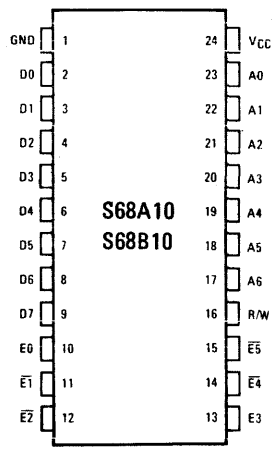
The S68A10 and S68B10 are static 128x8 Read/Write Memories designed and organized to be compatible with the S68A00 and S68B00 Microprocessors. Interfacing to the S68A10 and S68B10 consists of an 8-bit bidirectional data bus, seven address lines, a single Read/Write control line, and six chip enable lines, four negative and two positive.

For ease of use, the S68A10 and S68B10 are a totally static memory requiring no clocks or cell refresh. The S68A10 and S68B10 are fabricated with N-channel silicon gate depletion load technology to be fully DTL/TTL compatible with only a single +5 volt power supply required.

Block Diagram



Pin Configuration



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Absolute Maximum Ratings

Supply Voltage	-0.3V to +7.0V
Input Voltage	-0.3V to +7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C

DC Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{IN}	Input Current (A_n, R/W, CS_n, $\overline{CS}_n$)			2.5	μAdc	V_{IN} = 0V to 5.25V
V_{OR}	Output High Voltage	2.4			Vdc	I_{OH} = -205μA
V_{OL}	Output Low Voltage			0.4	Vdc	I_{OL} = 1.0mA
I_{LO}	Output Leakage Current (Three-State)			10	μAdc	CS = 0.8V or $\overline{CS}$ = 2.0V, V_{OUT} = 0.4V to 2.4V
I_{CC}	Supply Current			80	mAdc	V_{CC} = 5.25V, all other pins grounded, T_A = 0°C

AC Characteristics

Read Cycle (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

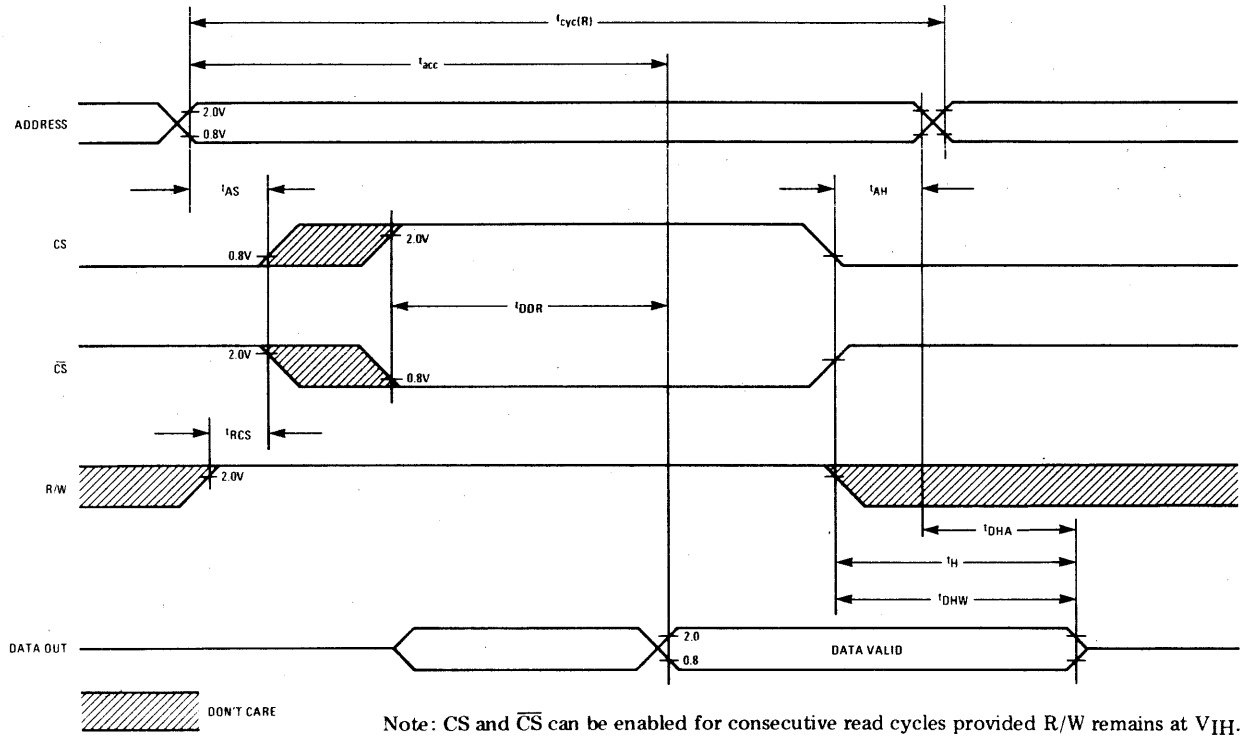
Symbol	Parameter	S68A10		S68B10		Units
		Min.	Max.	Min.	Max.	
$t_{cyc(R)}$	Read Cycle Time	360		250		ns
t_{acc}	Access Time		360		250	ns
t_{AS}	Address Setup Time	20		20		ns
t_{AH}	Address Hold Time	0		0		ns
t_{DDR}	Data Delay Time (Read)		220		180	ns
t_{RCS}	Read to Select Delay Time	0		0		ns
t_{DHA}	Data Hold from Address	10		10		ns
t_H	Output Hold Time	10		10		ns
t_{DHW}	Data Hold from Write	10	60	10	60	ns

Write Cycle (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	S68A10		S68B10		Units
		Min.	Max.	Min.	Max.	
$t_{cyc(W)}$	Write Cycle Time	360		250		ns
t_{AS}	Address Setup Time	20		20		ns
t_{AH}	Address Hold Time	0		0		ns
t_{CS}	Chip Select Pulse Width	250		210		ns
t_{WCS}	Write to Chip Select Delay Time	0		0		ns
t_{DSW}	Data Setup Time (Write)	80		60		ns
t_H	Input Hold Time	10		10		ns

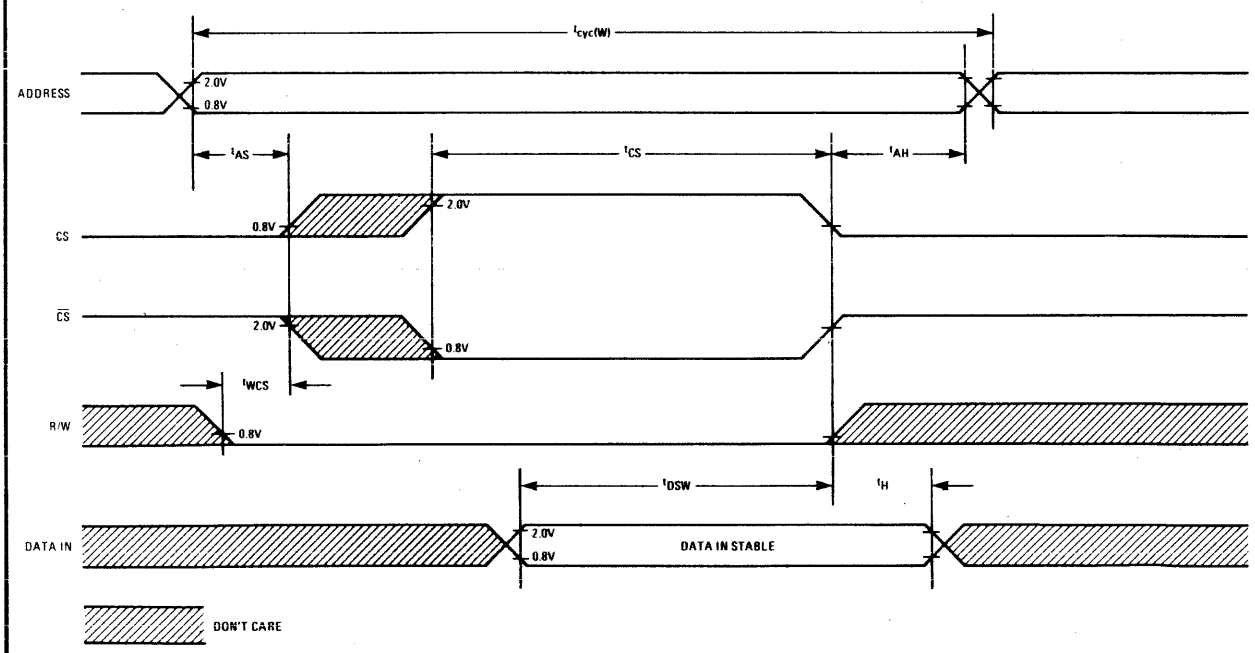
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Read Cycle Timing



Note: CS and $\overline{CS}$ can be enabled for consecutive read cycles provided R/W remains at V_{IH}.

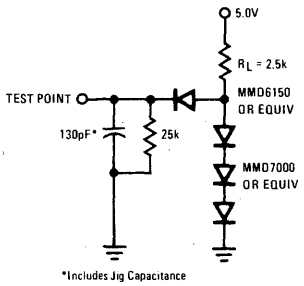
Write Cycle Timing



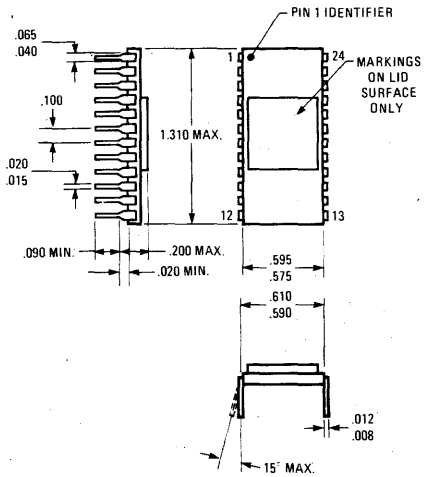
Note: CS and $\overline{CS}$ can be enabled for consecutive write cycles provided R/W is strobed to V_{IH} before or coincident with the Address change, and remains high for time t_{AS}.

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AC Test Load



Physical Dimensions



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Peripheral Interface Adapter (PIA)

Features

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines: Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance Three-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Compatible Peripheral Lines

General Description

The S68A21/S68B21 are peripheral Interface Adapters that provide the universal means of interfacing peripheral equipment to the S68A00 and the S68B00 Microprocessing Units (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

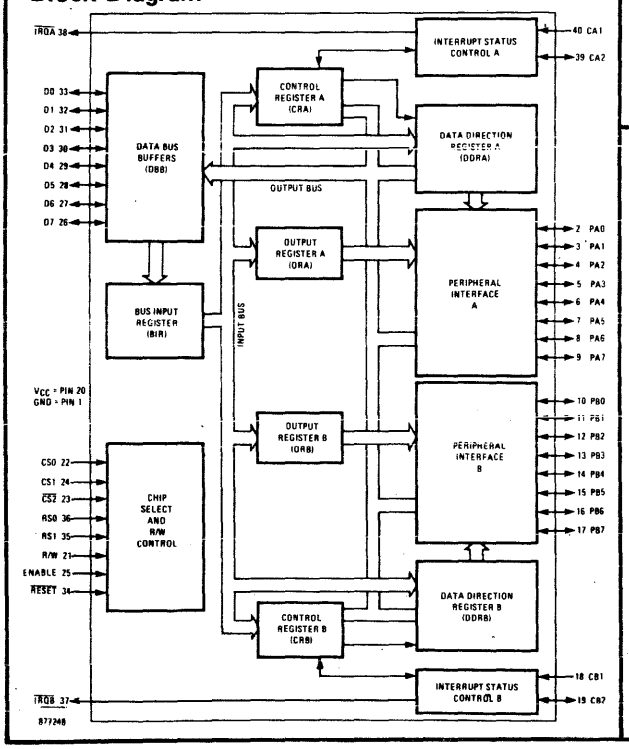
The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

The PIA interfaces to the S68A00/S68B00 MPUs with an eight-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with the S68A00/S68B00 VMA output, permit the MPU to have complete control over the PIA. VMA may be utilized to gate the input signals to the PIA.

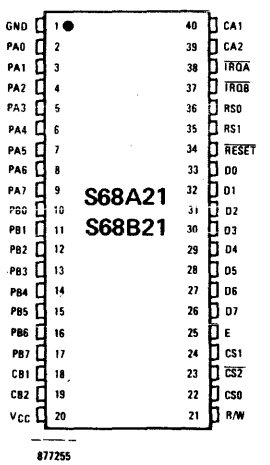
Absolute Maximum Ratings

Supply Voltage	-0.3V to +7.0V
Input Voltage	-0.3V to +7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C

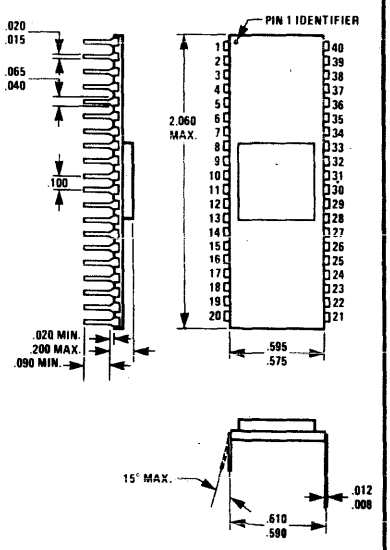
Block Diagram



Pin Configuration



Physical Dimensions



Note:
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any votage higher than maximum rated voltages to this high impedance circuit.

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Electrical Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Voltage	V_{SS}+2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS}- 0.3		V_{SS}+0.8	Vdc	
I_{in}	Input Leakage Current R/W, $\overline{Reset}$, RS0, RS1, CS0, $\overline{CS2}$, CS1, CA1, CB1, Enable		1.0	2.5	μAdc	V_{in} = 0Vdc to +5.25Vdc
I_{TSI}	Three-State (Off State) Input Current D0-D7, PB0-PB7, CB2		2.0	10	μAdc	V_{in} = 0.4Vdc to 2.4Vdc
I_{IH}	Input High Current PA0-PA7, CA2	- 200	- 400		μAdc	V_{IH} = 2.4Vdc
I_{IL}	Input Low Current PA0-PA7, CA2		- 1.3	- 2.4	mAdc	V_{IL} = 0.4Vdc
V_{OH}	Output High Voltage					
	D0-D7	V_{SS}+2.4			Vdc	I_{Load} = - 205μAdc
	Other Outputs	V_{SS}+2.4			Vdc	I_{Load} = - 200μAdc
V_{OL}	Output Low Voltage					
	D0-D7			V_{SS}+0.4	Vdc	I_{Load} = 1.6mAdc
	Other Outputs			V_{SS}+0.4	Vdc	I_{Load} = 3.2mAdc
I_{OH}	Output High Current (Sourcing)					
	D0-D7	- 205			μAdc	V_{OH} = 2.4Vdc
	Other Outputs	- 100			μAdc	
	PB0-PB7, CB2	- 1.0	- 2.5	- 10	mAdc	V_O = 1.5Vdc, the current for driving other than TTL, e.g., Darlington Base
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQA}$, $\overline{IRQB}$		1.0	10	μAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation			550	mW	
C_{in}	Capacitance					
	D0-D7			12.5	pF	V_{in} = 0, T_A = +25°C, f = 1.0MHz
	PA0-PA7, PB0-PB7, CA2, CB2			10	pF	
	Enable, R/W, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1			7.5	pF	
C_{out}	$\overline{IRQA}$, $\overline{IRQB}$			5.0	pF	

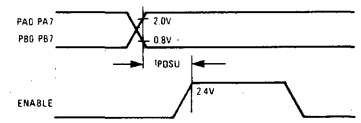
Note: The PA0-PA7 Peripheral Data lines and the CA2 Peripheral Control line can drive two standard TTL loads. In the input mode, the internal pullup resistor on these lines represents a maximum of 1.5 standard TTL loads.

Timing Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	MC68A21 Min.	MC68A21 Max.	MC68B21 Min.	MC68B21 Max.	Units	Conditions
t_{PDSU}	Peripheral Data Setup Time	135		100		ns	
t_{PDH}	Peripheral Data Hold Time	0		0		ns	
t_{CA2}	Delay Time, Enable Negative Transition to CA2 Negative Transition		0.670		0.5	μs	
t_{RS1}	Delay Time, Enable Negative Transition to CA2 Positive Transition		0.670		0.5	μs	
t_r, t_f	Rise and Fall Times for CA1 and CA2 Input Signals		1.0		1.0	μs	
t_{RS2}	Delay Time from CA1 Active Transition to CA2 Positive Transition		1.35		1.0	μs	
t_{PDW}	Delay Time, Enable Negative Transition to Peripheral Data Valid		0.670		0.5	μs	
t_{CMOS}	Delay Time, Enable Negative Transition to Peripheral CMOS PA0-PA7, CA2 Data Valid		1.35		1.0	μs	V_{CC} - 30% V_{CC}; Figure 6, Load C
t_{CB2}	Delay Time, Enable Positive Transition to CB2 Negative Transition		0.670		0.5	μs	
t_{DC}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	20		20		ns	
t_{RS1}	Delay Time, Enable Positive Transition to CB2 Positive Transition		0.670		0.5	μs	
PW_{CT}	Peripheral Control Output Pulse Width, CA2/CB2	550		550		ns	
t_r, t_f	Rise and Fall Time for CB1 and CB2 Input Signals		1.0		1.0	μs	
t_{RS2}	Delay Time, CB1 Active Transition to CB2 Positive Transition		1.35		1.0	μs	
t_{IR}	Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$		1.1		0.85	μs	
t_{RS3}	Interrupt Response Time		1.0		1.0	μs	
PW_I	Interrupt Input Pulse Width	500		500		ns	
t_{RL}	Reset Low Time*	0.66		0.5		μs	

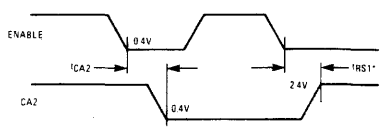
*The Reset line must be high a minimum of 1.0μs before addressing the PIA.

Peripheral Data Setup Time (Read Mode)



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CA2 Delay Time (Read Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)



*Assumes part was deselected during the previous E pulse.

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A.C. (Dynamic) Characteristics Loading = 30pF and one TTL load for PA0-PA7, PB0-PB7, CA2, CB2
= 130pF and one TTL load for D0-D7, $\overline{IRQA}$, $\overline{IRQB}$
(V_{CC} = +5.0V ±5%, T_A = 0°C to +70°C unless otherwise noted.)

Bus Timing Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

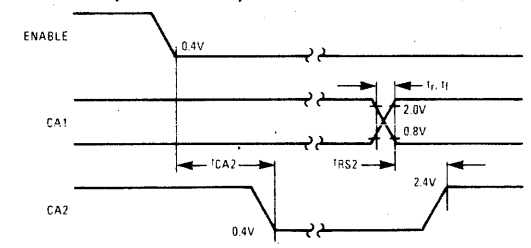
Read

Symbol	Parameter	S68A21 Min.	S68A21 Max.	S68B21 Min.	S68B21 Max.	Units
t_{cycE}	Enable Cycle Time	0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.280		0.22		μs
PW_{EL}	Enable Pulse Width, Low	0.280		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	140		70		ns
t_{DDR}	Data Delay Time		220		180	ns
t_H	Data Hold Time	10		10		ns
t_{AH}	Address Hold Time	10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25	ns

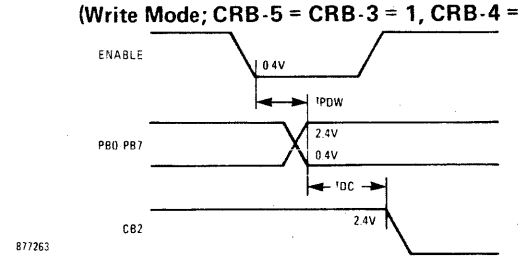
Write

Symbol	Parameter	S68A21 Min.	S68A21 Max.	S68B21 Min.	S68B21 Max.	Units
t_{cycE}	Enable Cycle Time	0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.280		0.22		μs
PW_{EL}	Enable Pulse Width, Low	0.280		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	140		70		ns
t_{DSW}	Data Setup Time	80		60		ns
t_H	Data Hold Time	10		10		ns
t_{AH}	Address Hold Time	10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25	ns

CA2 Delay Time
(Read Mode; CRA-5 = 1, CRA-3 = CRA-4 = 0)

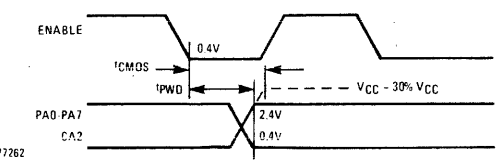


Peripheral Data and CB2 Delay Times
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)

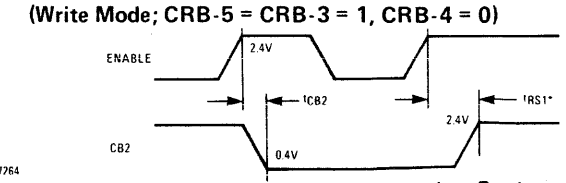


CB2 Note: CB2 goes low as a result of the positive transition of Enable.

Peripheral CMOS Data Delay Times
(Write Mode: CRA-5 = CRA-3 = 1, CRA-4 = 0)



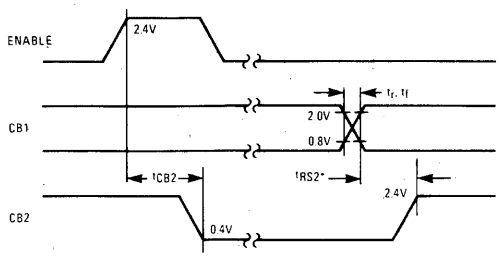
CB2 Delay Time
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



*Assumes part was deselected during the previous E pulse.

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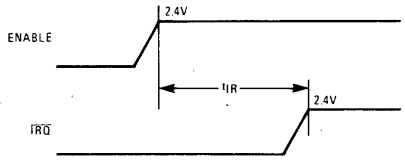
CB2 Delay Time
(Write Mode; CRB-5 = 1, CRB-3 = CRB-4 = 0)



877265

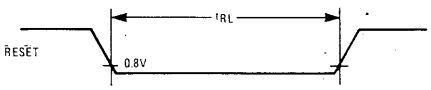
*Assumes part was deselected during any previous E pulse.

$\overline{IRQ}$ Release Time



877266

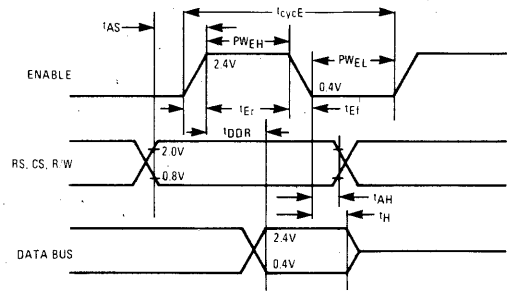
$\overline{RESET}$ Low Time



*The $\overline{Reset}$ line must be a V_{IH} for a minimum of 1.0μs before addressing the PIA.

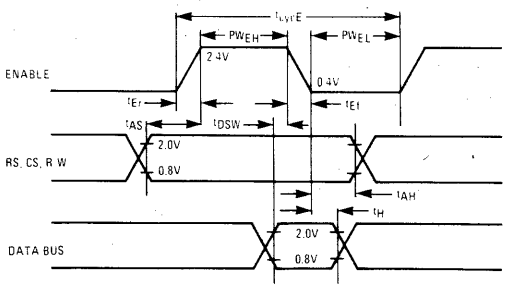
877267

Bus Read Timing Characteristics
(Read Information from PIA)



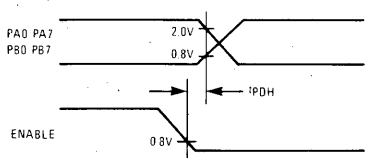
877268

Bus Write Timing Characteristics
(Write Information into PIA)



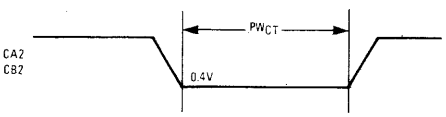
877269

Peripheral Data Hold Time
(Read Mode)



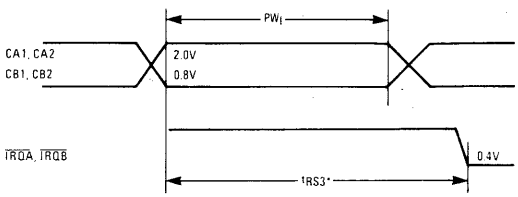
877270

Peripheral Control Output Pulse Width



877271

Interrupt Pulse Width and $\overline{IRQ}$ Response



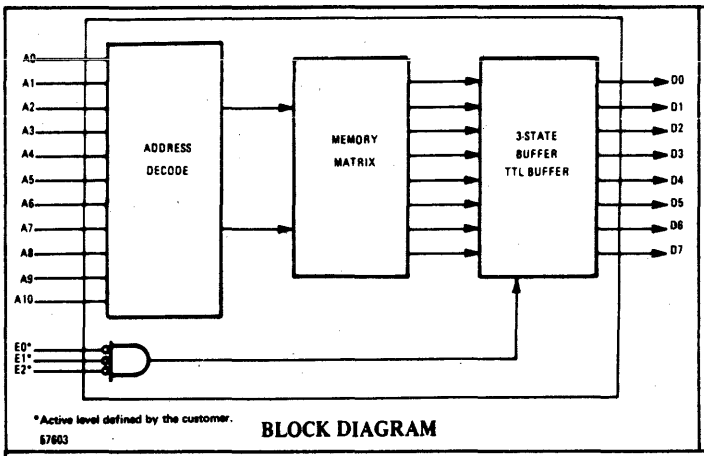
877272

*Assumes Interrupt Enable Bits are set.

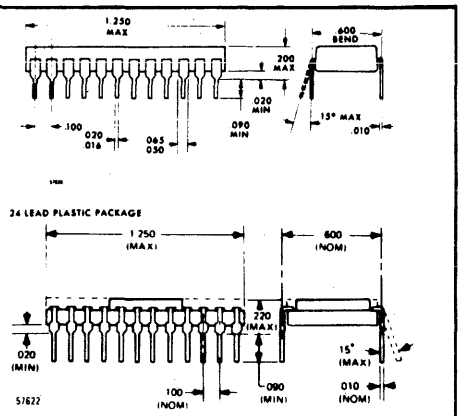
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16,384 Bit (2048×8) ROM

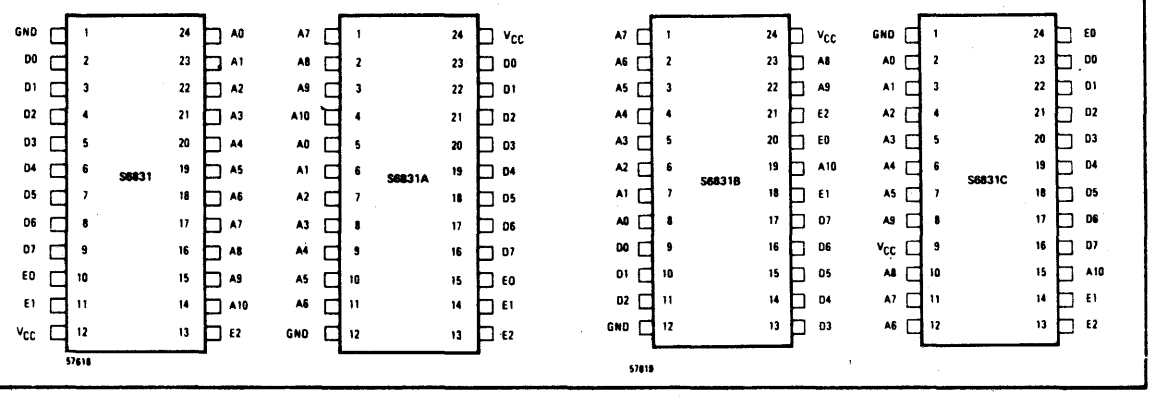
ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION



- Maximum Access Time = 450 ns @ C_L = 130 pF
- Low Power 150 mW avg.
- Organized as 2048-Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- 3 Chip Enable Inputs (Mask Programmable)
- The S6831 is pinout similar with the S6830
- The S6831A is pinout compatible with the 2316A, 8316A
- The S6831B is pinout compatible with the Intel 2316B, MC68317
- The S6831C is pinout compatible with the EA4600
- Single 5-Volt Power Supply
- TTL Compatible Input/Output

FUNCTIONAL DESCRIPTION

The S6831/A/B/C is a 16,384 bit Read Only Memory organized 2K words x 8 bits. This ROM has been designed to supply large bit storage, high performance memory for microprocessors and other demanding applications with simple interface requirements. The device will operate from a single +5V supply and is manufactured with a N-channel silicon gate depletion load technology. This device is available in all common high density ROM pinouts.

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Supply Voltage V_{CC}	- 0.5 to + 7.0V	Operating Temperature Range T_A	0 to + 70°C
Input Voltage V_{in}	- 0.5 to + 7.0V	Storage Temperature Range T_{stg}	- 55 to + 150°C

NOTE 1 Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

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DC (STATIC) CHARACTERISTICS (V_{CC} = + 5 Volt ± 5%; T_A = 0°C to + 70°C)

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage (Norm. Op. Levels)	2.0	–	5.25	Vdc	
V_{IL}	Input Low Voltage (Norm. Op. Levels)	- 0.5	–	0.8	Vdc	
I_I	Input Current (V_I = 0 to 5.25 V)	–	–	2.5	μAdc	
V_{OH}	Output High Voltage (I_{OH} =-100μA)	2.4	–	–	Vdc	
V_{OL}	Output Low Voltage (I_{OL} = 2.1 mA)	–	–	0.4	Vdc	
I_{LOH}	Output Leakage Current (V_O = 2.4, $\overline{E}$ = 0.4V, E = 2.4V)	–	–	10	μAdc	
I_{LOL}	Output Leakage Current (V_O = 0.4V, $\overline{E}$ = 0.4V, E = 2.4V)	–	–	10	μAdc	
I_{CC}	Supply Current (V_{CC} = 5.25V, T_A = 0°C)	–	30		mAdc	

CAPACITANCE

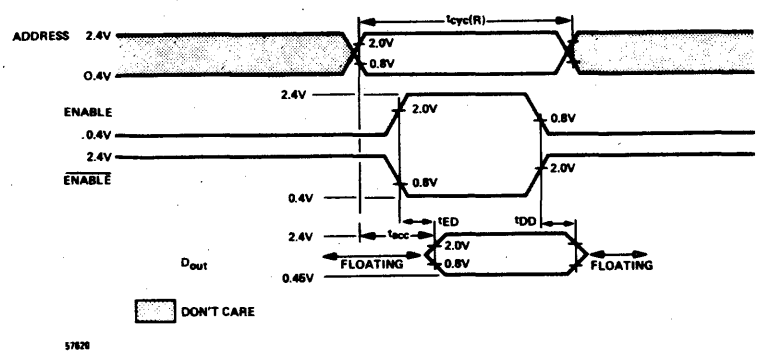
Symbol	Characteristic	Min.	Typ.	Max	Unit	Conditions
C_{in}	Input Capacitance	–	–	7.5	pF	f = 1.0 MHz
C_{out}	Output Capacitance	–	–	10	pF	T_A = 25°C

AC (DYNAMIC) CHARACTERISTICS V_{CC} = + 5 Volt ± 5%; T_A = 0°C to + 70°C

READ CYCLE (All timing with $t_r = t_f$ = 20 ns, Load of Figure 1)

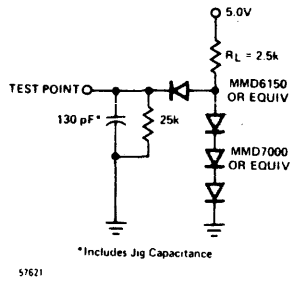
Symbol	Characteristic	Min.	Max.	Unit
t_{cyc} (R)	Read Cycle Time	450	–	ns
t_{ED}	Output Enable Delay Time	–	200	ns
t_{DD}	Output Disable Delay Time	10	150	ns
t_{ACC}	Read Access Time	–	450	ns

READ CYCLE TIMING



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FIGURE 1 – AC TEST LOAD



CUSTOM PROGRAMMING

The preferred method of pattern submission is the AMI Hex format as described below with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler/Loader. The format is as follows and may be on paper tape, punched card or other media readable by AMI.

ASCII Character	Description
1	**Start of record** (S)
2	**Type of record** 0 – Header record 1 – Data record 9 – End of file record
3 – 4	**Byte Count** Since each data byte is represented as two hex characters, the byte count must be multiplied by two fo get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length being defined in each record by the byte count.
5, 6, 7, 8	**Address Value** The memory location where this record is to be stored.
9, . . . , N	**Data** Each data byte is represented by two hex characters. Most significant character first.
N + 1, N + 2	**Checksum** The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

AMI will accept the input format used for the EA4600 or for the Intel 8316A or B in addition to the above format.

EXAMPLE:

```
S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 1 D
S 9 0 3 0 0 0 0 F C

S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 1 D
```

START OF RECORD
TYPE OF RECORD
BYTE COUNT (HEX)
START ADDRESS
DATA
CHECK SUM

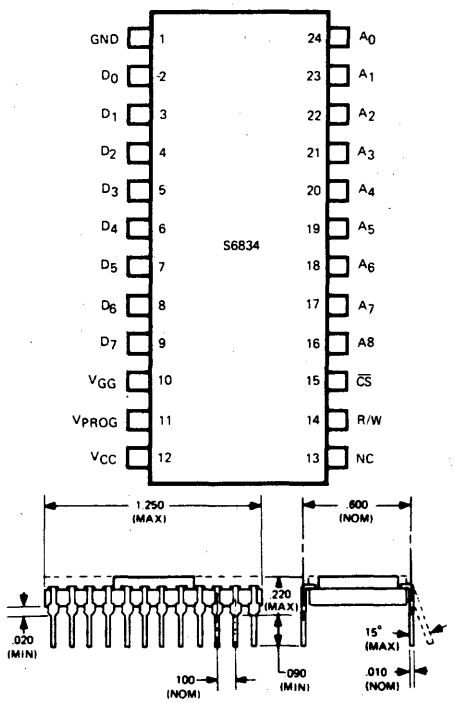
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4096 Bit (512×8) Erasable and Electrically Reprogrammable ROM

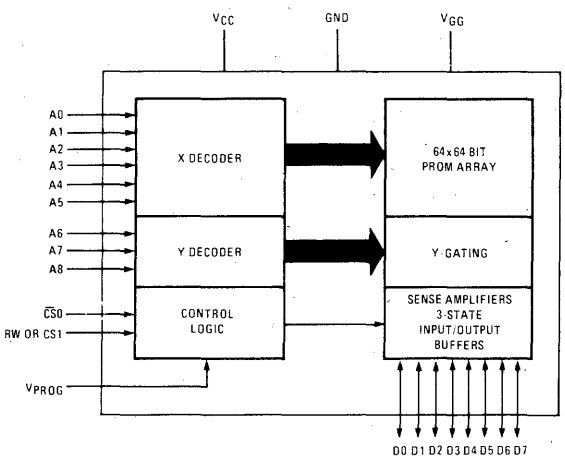
FEATURES

- On-Board Programmability
- Fast Access Time – 500 ns Typ.
- Pin Configuration Similar to the S6830 1K x 8 Bit ROM
- High Speed Programming – Less than 1 Minute for all 4096 Bits
- Programmed with R/W, CS and V_{PROG} Pins
- Completely TTL Compatible – Excluding the V_{PROG} Pin during Read and Write
- Ultraviolet Light Erasable – Less than 10 Minutes
- Static Operation – No Clocks Required
- Three-State Data I/O
- Standard Power Supplies +5V and –12V
- Mature P-Chan Process

PIN/PACKAGE CONFIGURATION



BLOCK DIAGRAM



TYPICAL APPLICATIONS

- ROM Program Debugging
- Code Translation
- Microprogramming
- Look-up Tables
- Random Logic Replacement
- Programmable Waveforms
- Character Generation
- Electronic Keyboards

FUNCTIONAL DESCRIPTION

The S6834 is a high speed, static, 512 x 8 bit, eraseable and electrically programmable read only memory designed for use in bus-organized systems. Both input and output are TTL compatable during both read and write modes. Packaged in a 24 pin hermetically sealed dual in-line package the bit pattern can be erased by exposing the chip to an ultra-violet light source through the transparent lid, after which a new pattern can be written.

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} except the V_{PROG} pin	+0.3V to -20V
Voltage on the V_{PROG} pin relative to V_{SS}	+0.3V to -55V
Operating Temperature	0°C to +70°C
Storage Temperature (programmed)	-55°C to +85°C
Storage Temperature (unprogrammed)	-55°C to +150°C

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

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DC (STATIC) CHARACTERISTICS (V_{CC} = +5.0V ± 5%, V_{GG} = −12.0V ± 5% T_A = 0 − 70°C unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
V_{IL}	INPUT VOLTAGE LOW		0.8	V
V_{IH}	INPUT VOLTAGE HIGH	V_{CC} −2.25	V_{CC} to .3	V
V_{OL}	OUTPUT VOLTAGE LOW I_{OL} = 1.6 ma		0.4	V
V_{OH}	OUTPUT VOLTAGE HIGH I_{OH} = 200μA	2.4		V
I_{LI}	INPUT LEAKAGE CURRENT		10	μa
I_{LO}	OUTPUT LEAKAGE CURRENT CS = 5V		20	μa
I_{GG}	V_{GG} SUPPLY CURRENT		45	ma
I_{CC}	V_{CC} SUPPLY CURRENT		50	ma
P_D	POWER DISSIPATION		750	mw

NOTE: Program input V_{PROG} may be tied to V_{CC} during the Read.

AC (DYNAMIC) CHARACTERISTICS (Loading is as shown in Figure 1 unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX (6834)	MAX (6834−1)	UNIT
T_{ACC}	ACCESS TIME		575	750	ns
T_{CO}	CHIP SELECT TO OUTPUT DELAY		300	400	ns
T_{DD}	CHIP DESELECT TO OUTPUT DELAY		250	325	ns

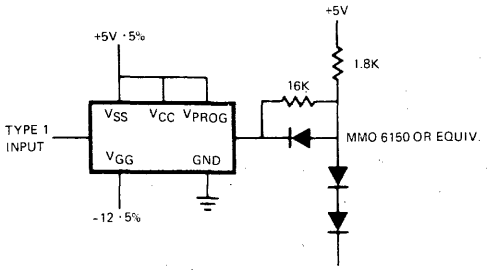
PROGRAM CHARACTERISTICS (R/W G_{nd}, Program pulse rise and fall time (10% to 90%) are both at 1μs max).

SYMBOL	CHARACTERISTICS	MIN	MAX	UNIT
T_{AS}	ADDRESS SET UP TIME	10		μs
T_{CSS}	CHIP SELECT SET UP TIME	10		μs
T_{DS}	DATA SET UP TIME	10		μs
T_{AH}	ADDRESS HOLD TIME	10		μs
T_{CSH}	CHIP SELECT HOLD TIME	10		μs
T_{DH}	DATA HOLD TIME	10		μs
T_{PWL}	PROGRAM PULSE WIDTH LOW	3	5	ms
T_{PWH}	PROGRAM PULSE WIDTH HIGH	500		μs
V_{PROG}*	PROGRAM AMPLITUDE	−55	−50	V
I_{PROG}	PROGRAM CURRENT		35	ma
T_{WS}	WRITE SET UP TIME	10		μs
T_{WH}	WRITE HOLD TIME	5		μs
T_{RS}	READ SET UP TIME	10		μs

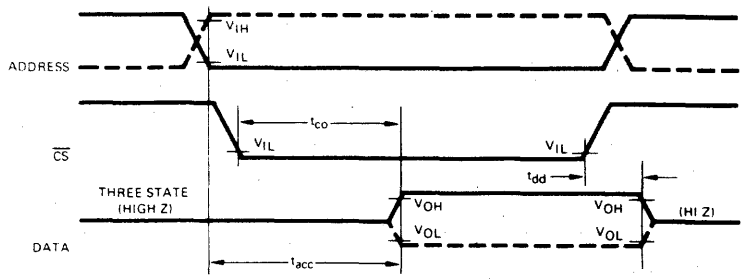
*Note that in the WRITE mode the MIN value of V_{PROG} should not be exceeded and that chip select, address, and data lines may remain at TTL level, as in the READ mode.

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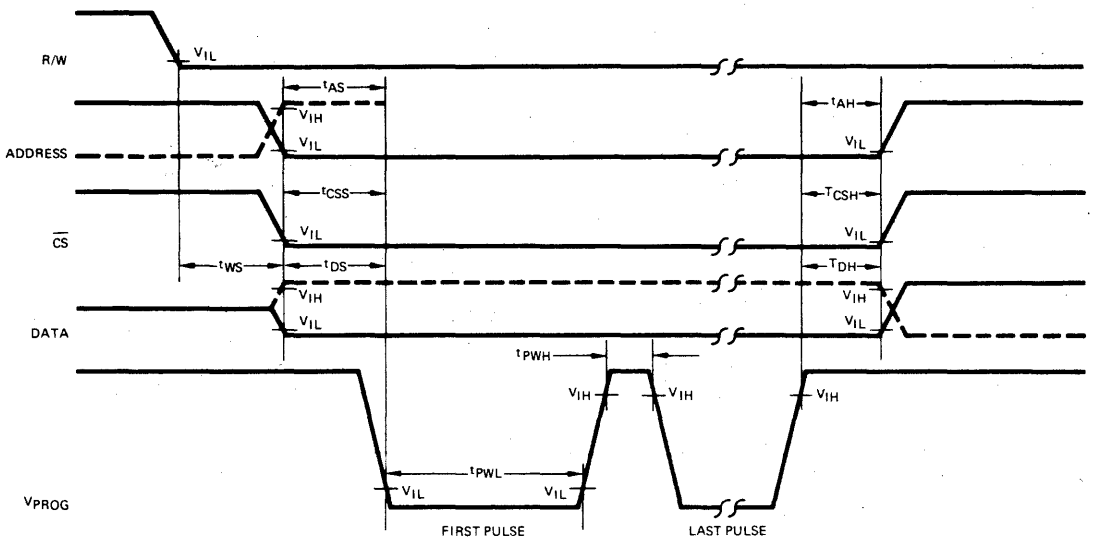
TEST CONDITIONS



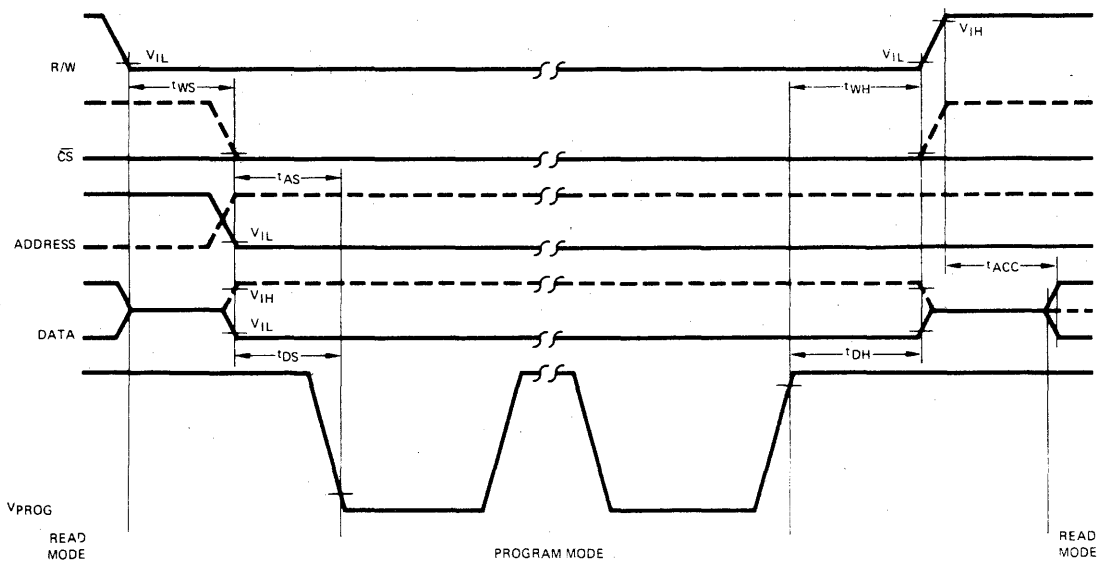
READ CYCLE TIMING WAVEFORMS



PROGRAMMING CYCLE TIMING WAVEFORMS



READ/PROGRAM/READ CYCLE TIMING WAVEFORM



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CONTROL FUNCTION TRUTH TABLE

CS	R/W	V_{PROG}	MODE	OUTPUTS
0	0	V_{PROG}	Write	Active Data Inputs
0	1	V_{CC}	Read	Active
1	X	X	Standby	Floating

OPERATION

Initially, and after each erasure, all bits of the 6834 are in the logic "0" state (output 0 volts). Data is stored by selectively programming a logic "1" into the desired bit locations. The R/W input (pin 14) is used to select the desired mode of operation. When the R/W input is at logic "0" the chip is in the write enable mode of operation. The outputs (0_1 –0_8) are disabled (floating) with the corresponding pins becoming the data inputs ($0_1 \rightarrow D_{IN\ 1}$ etc.). The word address is selected in the same manner as in the read mode. Data to be programmed are presented 8 bits in parallel and after the address and data are set up a programming pulse (V_P –50 volts) is applied. V_{PROG} electrically writes the data into the memory array. Writing may be inhibited by deselecting the chip with the CS input at a logic "1" during the write cycle. This feature allows true "on board" programming in bus organized systems where the R/W and V_{PROG} inputs are common and the device to be programmed is selected by means of the chip select input as during read operations.

The amount of program energy required to insure memory retention may be defined as a function of the number of program pulses (N) times the program pulse width (t_{pw}) ($N \times t_{pw} \geqslant 60$ msec). This means if a 3 ms pulse is used, 20 program pulses are required, and if a 5 ms pulse is used 12 program pulses are required.

The read operation is accomplished by a logic "1" at the R/W input with the program input connected to V_{SS} potential. True data (data out = data in) is valid after the address is stable. The CS input will disable (float) the outputs when at a logic "1" to allow or tie capability.

Erasure is accomplished by exposing the array to a high intensity ultra-violet light source (such as, Ultra-Violet Products, Inc. Lamp Model S52 or UVS-54) for a period of 7 to 10 minutes. The clear optical lid should be approximately one inch away from the lamp tubes.

INTERFACE DESCRIPTION

Pin	Label	Function
(2)	D0	**Data Lines** – with the R/W line selected for Read (V_{IH}), the Data Lines (D0 through D7) are set to reflect the contents of the selected memory location. When the R/W line is set for Write (V_{IL}), the Data Lines are input to the addressed location of the 6834 when V_{PROG} is present. The Data Bus output drivers are three-state devices that remain in the high impedance (off) state when CS is in the V_{IH} state or when R/W is in the V_{IL} state.
(3)	D1	
(4)	D2	
(5)	D3	
(6)	D4	
(7)	D5	
(8)	D6	
(9)	D7	
(14)	R/W	**Read/Write** – When this input line is set to V_{IH}, the device is in the Read mode, a low (V_{IL}) signal puts it into the Write mode.
(15)	CS	**Chip Select** – This input line must be set to V_{IL} for a Read or Write operation to be performed. When it is High (V_{IH}) the output data bus is set to a high-impedance three-state condition and disables the Write operation.
(11)	V_{PROG}	**Program** – In the Write mode, a programming pulse (–50V dc) at this input causes the data at the Data Lines to be stored in the selected address. This pin should be tied to V_{CC} for normal Read operations.
(24)	A0	**Address Lines** – These lines select the 8 bit word in memory for Read or Write operation
(23)	A1	
(22)	A2	
(21)	A3	
(20)	A4	
(19)	A5	
(18)	A6	
(17)	A7	
(16)	A8	

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Asynchronous Communication Interface Adapter (ACIA)

Features

- 8 Bit Bidirectional Data Bus for Communication with MPU
- False Start Bit Deletion
- Peripheral/Modem Control Functions
- Double Buffered Receiver and Transmitter
- One or Two Stop Bit Operation
- Eight and Nine-Bit Transmission with Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Programmable Control Register
- Optional ÷1, ÷16, and ÷64 Clock Modes
- Up to 500,000 bps Transmission

Absolute Maximum Ratings

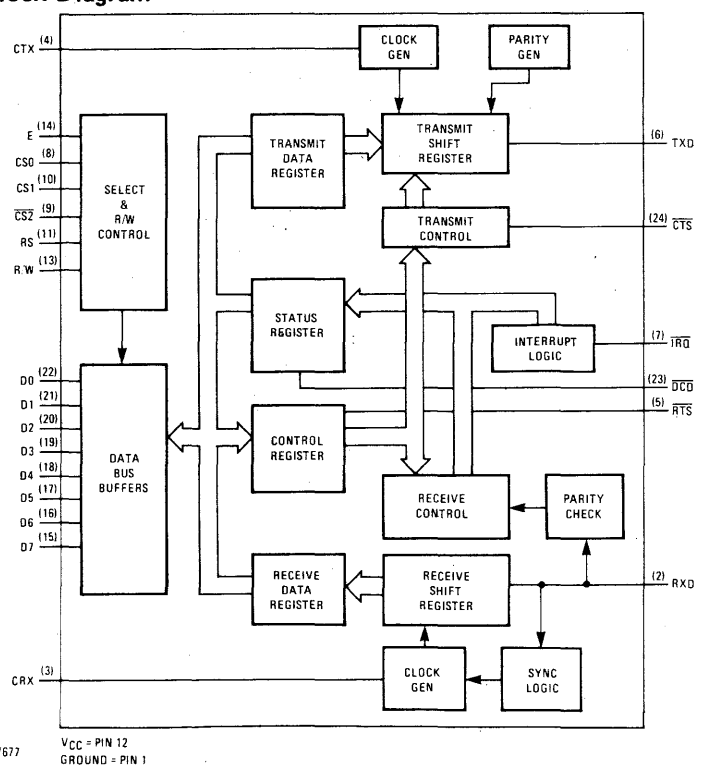
Supply Voltage	−0.3V to +7.0V
Input Voltage	−0.3V to +7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C

General Description

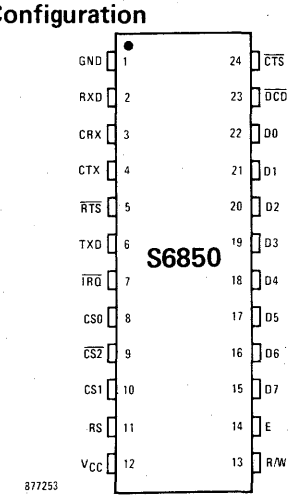
The S68A50/S68B50 Asynchronous Communications Interface Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data communications to bus organized systems such as the S68A00/S68B00 Microprocessing Units.

The S68A50/S68B50 includes select enable, read/write, interrupt and bus interface logic to allow data transfer over an eight-bit bidirectional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. Word lengths, clock division ratios and transmit control through the Request to Send output may be programmed. For modem operation three control lines are provided.

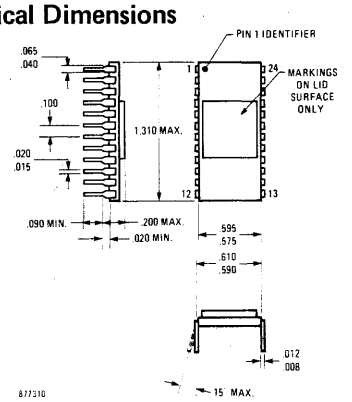
Block Diagram



Pin Configuration



Physical Dimensions



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Electrical Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Voltage		V_{SS}+2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage		V_{SS}-0.3		V_{SS}+0.8	Vdc	
I_{IN}	Input Leakage Current	R/W,CS0,CS1,$\overline{CS2}$,Enable		1.0	2.5	μAdc	V_{IN} = 0Vdc to 5.25Vdc
I_{TSI}	Three-State (Off State) Input Current	D0-D7		2.0	10	μAdc	V_{IN} = 0.4Vdc to 2.4Vdc
V_{OH}	Output High Voltage						
		D0-D7	V_{SS}+2.4			Vdc	I_{LOAD} = -205μAdc, Enable Pulse Width <25μs
		Tx Data, $\overline{RTS}$	V_{SS}+2.4			Vdc	I_{LOAD} = -100μAdc, Enable Pulse Width <25μs
V_{OL}	Output Low Voltage				V_{SS}+0.4	Vdc	I_{LOAD} = 1.6mAdc, Enable Pulse Width <25μs
I_{LOH}	Output Leakage Current (Off State)	$\overline{IRQ}$		1.0	10	μAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation			300	525	mW	
C_{IN}	Capacitance						
		D0-D7		10	12.5	pF	
		E,Tx,Clk,Rx Clk,R/W,RS,Rx Data, CS0,CS1,$\overline{CS2}$,$\overline{CTS}$,$\overline{DCD}$		7.0	7.5	pF	V_{IN} = 0, T_A = 25°C, f = 1.0MHz
C_{OUT}		$\overline{RTS}$,Tx Data			10	pF	
		$\overline{IRQ}$			5.0	pF	
PW_{CL}	Minimum Clock Pulse Width, Low	÷16, ÷64 Modes	600			ns	
PW_{CH}	Minimum Clock Pulse Width, High	÷16, ÷64 Modes	600			ns	
f_C	Clock Frequency	÷1 Mode			500	kHz	
		÷16, ÷64 Modes			800	kHz	
t_{TDD}	Clock-to-Data Delay for Transmitter				1.0	μs	
t_{RDSU}	Receive Data Setup Time	÷1 Mode	500			ns	
t_{RDH}	Receive Data Hold Time	÷1 Mode	500			ns	
t_{IR}	$\overline{Interrupt\ Request}$ Release Time				1.2	μs	
t_{RTS}	$\overline{Request\text{-}to\text{-}Send}$ Delay Time				1.0	μs	
t_r,t_f	Input Transition Times (Except Enable)				1.0*	μs	

*1.0μ or 10% of the pulse width, whichever is smaller.

Bus Timing Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Read

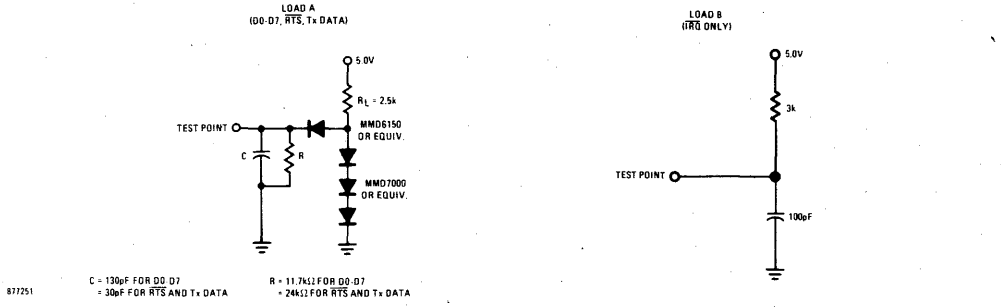
Symbol	Parameter	S68A50		S68B50		Units
		Min.	Max.	Min.	Max.	
t_{cycF}	Enable Cycle Time	0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.28	25	0.22	25	μs
PW_{EL}	Enable Pulse Width, Low	0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	140		70		ns
t_{DDR}	Data Delay Time		220		180	ns
t_H	Data Hold Time	10		10		ns
t_{AH}	Address Hold Time	10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25	ns

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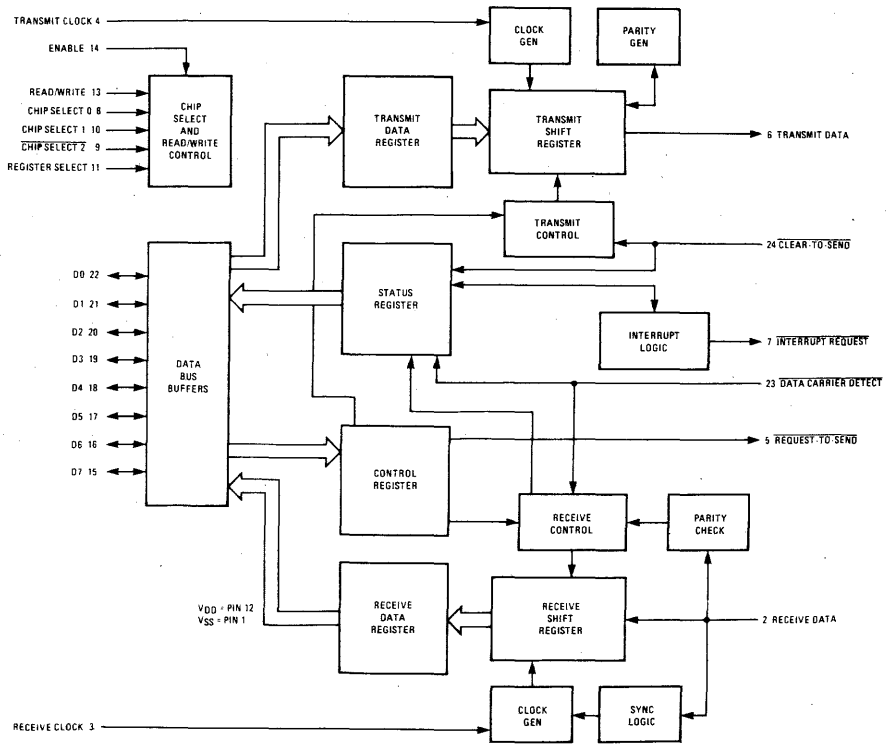
Write

Symbol	Parameter	S68A50 Min.	S68A50 Max.	S68B50 Min.	S68B50 Max.	Units
t_{cycE}	Enable Cycle Time	0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.28	25	0.22	25	μs
PW_{EL}	Enable Pulse Width, Low	0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	140		70		ns
t_{DSW}	Data Setup Time	80		60		ns
t_H	Data Hold Time	10		10		ns
t_{AH}	Address Hold Time	10		10		ns
t_{Fr}, t_{Ef}	Rise and Fall Time for Enable Input		25		25	ns

Bus Timing Test Loads



Expanded Block Diagram



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Figure 1. Clock Pulse Width, Low State

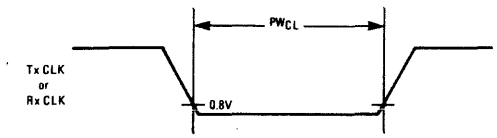


Figure 2. Clock Pulse Width, High State

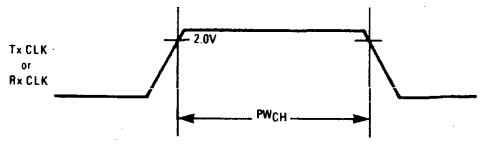


Figure 3. Transmit Data Output Delay

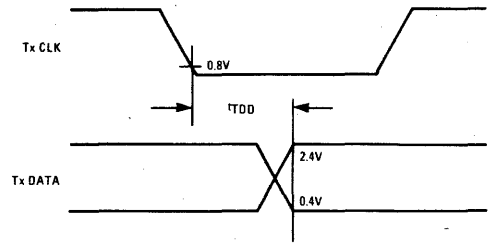


Figure 4. Receive Data Setup Time (÷1 Mode)

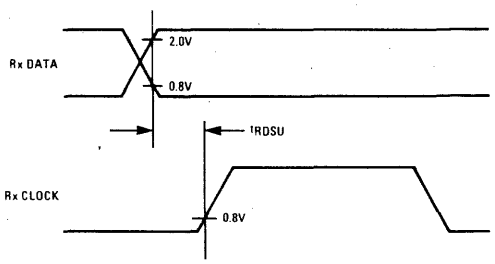


Figure 5. Receive Data Hold Time (÷1 Mode)

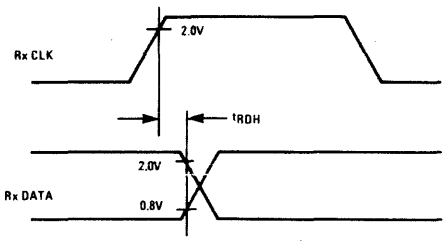


Figure 6. Request-to Send Delay and Interrupt-Request Release Times

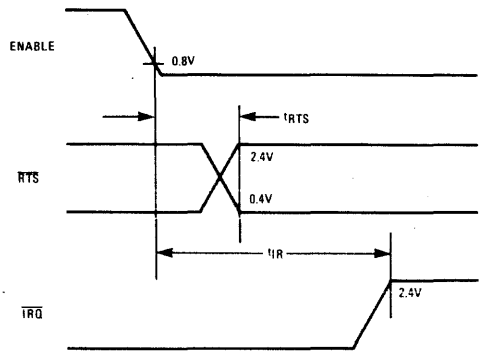


Figure 7. Bus Read Timing Characteristics (Read Information from ACIA)

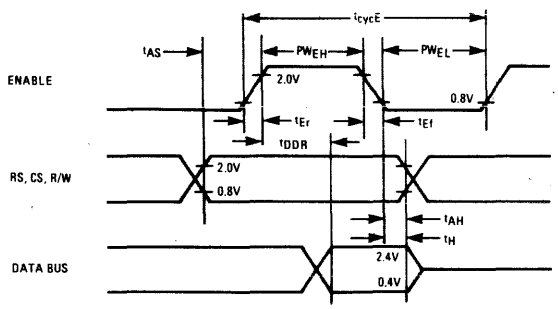
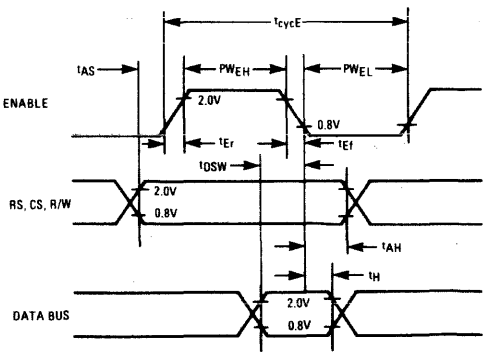


Figure 8. Bus Write Timing Characteristics (Write Information into ACIA)



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4-Bit Microcomputer

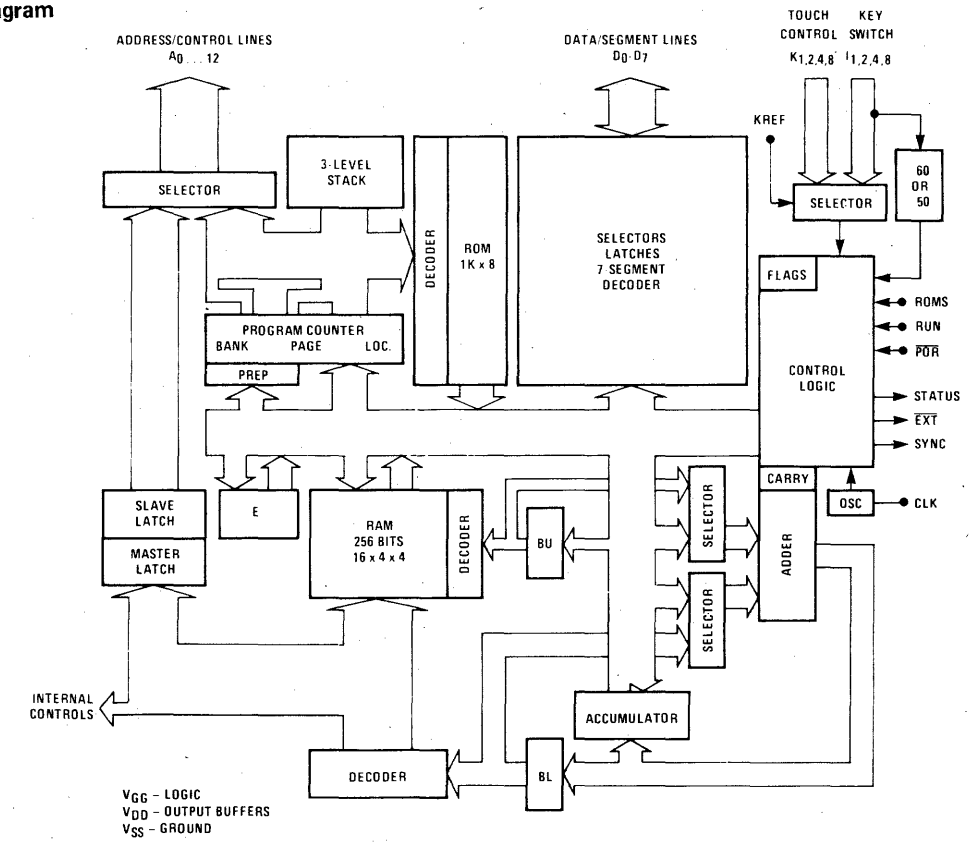
Features

- ☐ Single-Chip Architecture
- ☐ 1K x 8 ROM On Chip (Expandable to 8K x 8)
- ☐ 64x4 RAM On Chip
- ☐ 13 Outputs, 8 Inputs and 8 Bi-Directional Three-State Lines
- ☐ 7-Segment Decoder and Display Drivers On Chip:
  - S2000 — LED Drivers
  - S2000A — Vacuum Fluorescent Drivers
- ☐ TouchControl™ Capacitive Touchplate Compatibility
- ☐ Internal Timer (50Hz or 60Hz)
- ☐ Single +9V Power Supply
- ☐ Fast 4μs Execution Cycle
- ☐ 51 Instructions — All Single-Byte; 49 Single Cycle
- ☐ Three-Level Subroutine Stack
- ☐ TTL Compatible Outputs
- ☐ Reset, Test, and Step Modes

General Description

The S2000 is a fast, flexible 4-bit microcomputer which is completely self-contained with ROM, RAM, processor and input/output on one chip. Its design allows easy expansion of program storage through off-chip ROM or PROM and gives access to all internal registers and memory for debug and test.

Block Diagram



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Applications

The S2000 provides the advantages of computer architecture to low-cost, minimum-parts-count display/keyboard oriented control systems. Sophisitcated I/O and ROM expandability yield a cost-effective single-chip computer that functions like more expensive multi-chip processors. It is especially suited for applications which require:

Keyboard or touch switch inputs

LED or fluorescent display

50 Hz or 60 Hz line synchronization

Motor control (phase control and/or Triac drive)

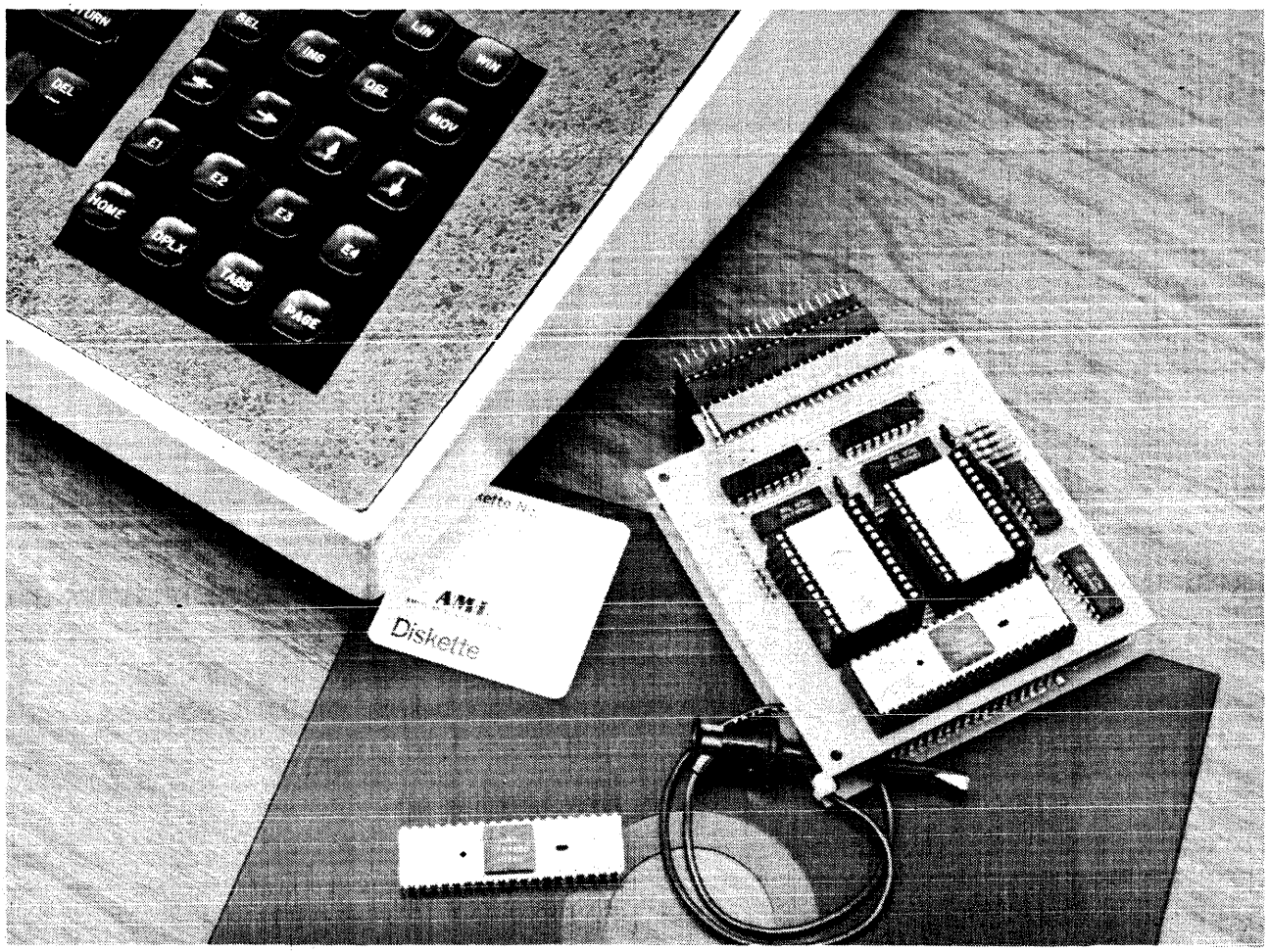
Multiple product lines where feature differentiation or model upgrading is required

S2000 Support

Complete development support is available in the forms of the MDC (Microcomputer Development Center), the DEV-2000 Debugger, the SES-2000 Emulator, the MDC-140 Logic Analyzer, TES-2000 Tester, software packages, applications engineers, and seminars.

Microcomputer Development Center

The MDC provides easy display-oriented text editing, macro assembly, software simulation, and EPROM burning.



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DEV-2000

The DEV-2000 Development & Debug Module links the user's prototype to the MDC. It gives quick-turn-around, on-line debug of hardware and software, including trace, step, and macro capabilities.

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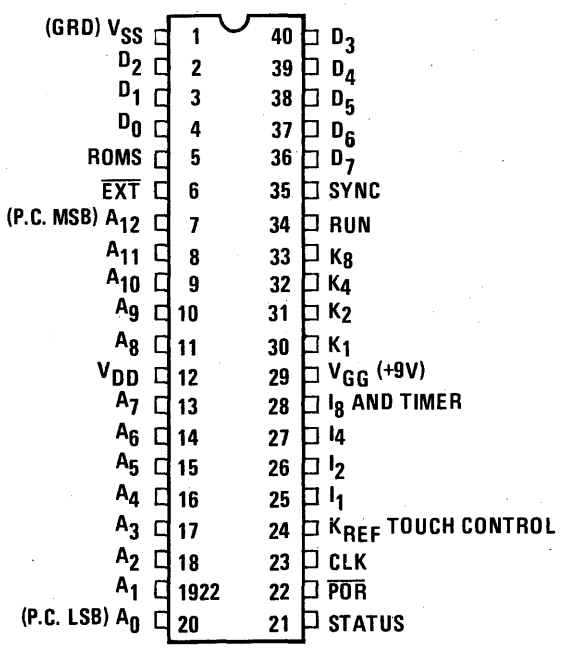
MDC-140 Logic Analyzer

This advanced Logic Analyzer provides a user-programmable MDC display of 1024 significant events appearing at its 40-channel input. Features include data-dependent clocking and oscilloscope trigger output, prewritten formats, four clock sources and programmable delay.

TES-2000

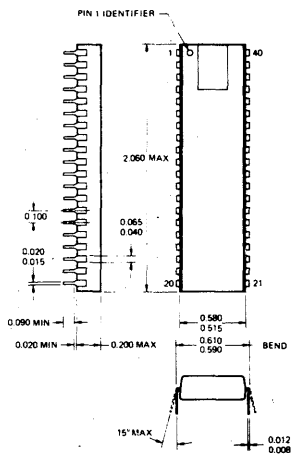
The TES-2000 is a dedicated S2000 tester which allows functional go/no-go comparison of CPU and ROM.

Pin Configuration

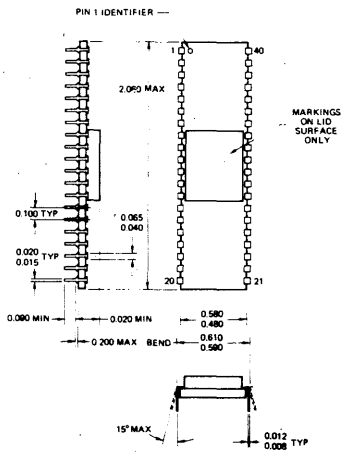


Physical Dimensions

40-PIN PLASTIC



40-PIN SLAM



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Absolute Maximum Ratings: (All voltages measured with respect to V_{SS})

Storage Temperature	-55°C to +125°C
Operating Temperature	0°C to +70°C
Maximum Positive Voltage	+18 Volts
Maximum Negative Voltage	-0.3 Volts
Maximum Output Currents	(See "Conditions" below)
I_{DD} Supply Current (depends on output loads)	75mA
Total Average Power Dissipation	500mW

Electrical Characteristics: (V_{SS} = 0V, V_{GG} = 9 ± 0.5V, V_{DD} = 5V*, T_A = 25°C)

	Parameter	Min.	Typ.	Max.	Units	Conditions
INPUTS	K_1 thru K_8					
	Low Level	0		K_{REP} -0.5	V	
	High Level	K_{REF} +0.5		V_{GG}	V	
INPUT	K_{REF}	0.28 V_{GG}		V_{GG}	—	
INPUTS	I_1 thru I_8 $\overline{POR}$ Schmitt-trigger					(Note 1)
	Low Level	0		.5	V	
	High Level	5.3		V_{GG}	V	
INPUTS	ROMs, RUN					
	Low Level	0		0.8	V	
	High Level	3.5		V_{GG}	V	
INPUTS	D_0 thru D_7					
	Low Level	0		0.8	V	
	High Level	4.5		V_{GG}	V	
OUTPUTS	A_0 thru A_3					
	High Level	3.5		*V_{DD}	V	I=-5mA
	Low Level	0		0.8	V	I=+25mA
OUTPUTS	A_4 thru A_{12} $\overline{EXT}$, SYNC, & S					
	High Level	3.5		*V_{DD}	V	I=-5mA
	Low Level	0		0.6	V	I=+5mA
OUTPUTS	D_0 thru D_7					
	High Level	3.5		*V_{DD}	V	I=-5mA
	Low Level	0		1.0	V	I=+12mA
I_{GG}	Supply Current		28	50	mA	

NOTE 1: There is an internal pull-up ≈ 100K from each of these inputs to V_{GG}.

*V_{DD} may be connected to V_{GG} if single power supply operation is desired.

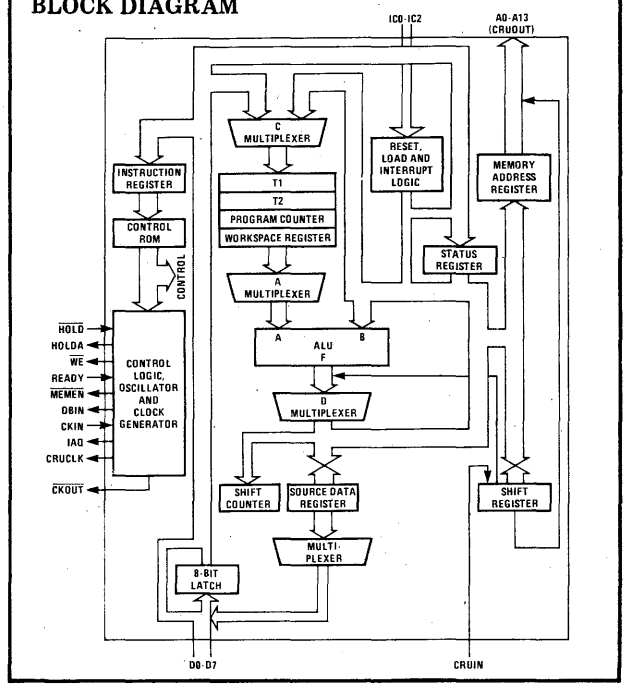
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16-Bit Single Chip Microprocessor

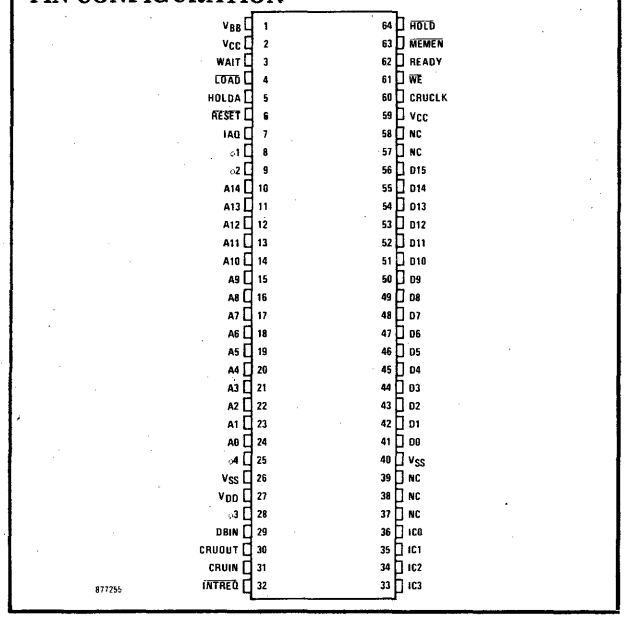
FEATURES

- 16-Bit Instruction Word
- 8 and 16-Bit Data Format
- Bi-directional Parallel 16-Bit Data Bus
- Parallel 15-Bit Address Bus Directly Addresses 32K Words or 64K Bytes
- Advanced Memory-to-Memory Architecture that Places Multiple Register Files in Memory
- 69 Instructions, Including Multiply and Divide
- Complete Software Compatibility with the TI9900 Minicomputer Family
- 7 Addressing Modes, 16 Prioritized Interrupts, 16 General Purpose Registers per File
- Direct Memory Access
- Easy Interface with Slow Memories
- TTL Compatible
- Standard Supply Voltages (+12V, +5V, -5V)

BLOCK DIAGRAM



PIN CONFIGURATION



The S9900 microprocessor is a single-chip 16-bit central processing unit produced using N-channel silicon gate MOS technology. The instruction set of the S9900 includes the capabilities offered by full minicomputers. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort. AMI provides a compatible set of MOS memory and logic function circuits to be used with an S9900 system. The system is fully supported by software and a complete prototyping system.

S9900 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
			ADDRESS BUS
A_0 (MSB)	24	OUT	A_0 through A_{14} comprise the address bus. This 3-state bus provides the memory-address vector to the external-memory system when MEMEN is active and I/O-bit addresses and external-instruction addresses to the I/O system when MEMEN is inactive. The address bus assumes the high-impedance state when HOLDA is active.
A_1	23	OUT	
A_2	22	OUT	
A_3	21	OUT	
A_4	20	OUT	
A_5	19	OUT	
A_6	18	OUT	
A_7	17	OUT	
A_8	16	OUT	
A_9	15	OUT	
A_{10}	14	OUT	
A_{11}	13	OUT	
A_{12}	12	OUT	
A_{13}	11	OUT	
A_{14} (LSB)	10	OUT	

SIGNATURE	PIN	I/O	DESCRIPTION
			DATA BUS
D_0 (MSB)	41	I/O	D_0 through D_{15} comprise the bi-directional 3-state data bus. This bus transfers memory data to (when writing) and from (when reading) the external-memory system when MEMEN is active. The data bus assumes the high-impedance state when HOLDA is active.
D_1	42	I/O	
D_2	43	I/O	
D_3	44	I/O	
D_4	45	I/O	
D_5	46	I/O	
D_6	47	I/O	
D_7	48	I/O	
D_8	49	I/O	
D_9	50	I/O	
D_{10}	51	I/O	
D_{11}	52	I/O	
D_{12}	53	I/O	
D_{13}	54	I/O	
D_{14}	55	I/O	
D_{15} (LSB)	56	I/O	

SIGNATURE	PIN	I/O	DESCRIPTION
			POWER SUPPLIES
V_{BB}	1		Supply voltage (-5V NOM)
V_{CC}	2,59		Supply voltage (5V NOM) Pins 2 and 59 must be connected in parallel.
V_{DD}	27		Supply voltage (12V NOM)
V_{SS}	26,40		Ground reference. Pins 26 and 40 must be connected in parallel.
			CLOCKS
$\phi 1$	8	IN	Phase-1 clock
$\phi 2$	9	IN	Phase-2 clock
$\phi 3$	28	IN	Phase-3 clock
$\phi 4$	25	IN	Phase-4 clock

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SIGNATURE	PIN	I/O	DESCRIPTION
			BUS CONTROL
DBIN	29	OUT	Data bus in. When active (high), DBIN indicates that the S9900 has disabled its output buffers to allow the memory to place memory-read data on the data bus during $\overline{\text{MEMEN}}$. DBIN remains low in all other cases except when HOLDA is active.
$\overline{\text{MEMEN}}$	63	OUT	Memory enable. When active (low), $\overline{\text{MEMEN}}$ indicates that the address bus contains a memory address.
$\overline{\text{WE}}$	61	OUT	Write enable. When active (low), $\overline{\text{WE}}$ indicates that memory write data is available from the S9900 to be written into memory.
CRUCLK	60	OUT	CRU clock. When active (high), CRUCLK indicates that external interface logic should sample the output data on CRUOUT or should decode external instructions on A_0 through A_2.
CRUIN	31	IN	CRU data in. CRUIN, normally driven by 3-state or open-collector devices, receives input data from external interface logic. When the processor executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A_3 through A_{14}).
CRUOUT	30	OUT	CRU data out. Serial I/O data appears on the CRUOUT line when an LDCR, SBZ, or SBO instruction is executed. The data on CRUOUT should be sampled by external I/O interface logic when CRUCLK goes active (high).
			INTERRUPT CONTROL
$\overline{\text{INTREQ}}$	32	IN	Interrupt request. When active (low), $\overline{\text{INTREQ}}$ indicates that an external interrupt is requested. If $\overline{\text{INTREQ}}$ is active, the processor loads the data on the interrupt-code-input lines IC_0 through IC_3 into the internal interrupt-code-storage register. The code is compared to the internal mask bits of the status register. If equal or higher priority than the enabled interrupt level (interrupt code equal or less than status register bits 12 through 15) the S9900 interrupt sequence is initiated. If the comparison fails, the processor ignores the request. $\overline{\text{INTREQ}}$ should remain active and the processor will continue to sample IC_0 through IC_3 until the program enables a sufficiently low priority to accept the request interrupt.
IC_0 (MSB) IC_1 IC_2 IC_3 (LSB)	36 35 34 33	IN IN IN IN	Interrupt codes. IC_0 is the MSB of the interrupt code, which is sampled when $\overline{\text{INTREQ}}$ is active. When IC_0 through IC_3 are LLLH, the highest external-priority interrupt is being requested and when HHHH, the lowest priority interrupt is being requested.
			MEMORY CONTROL
$\overline{\text{HOLD}}$	64	IN	Hold. When active (low), $\overline{\text{HOLD}}$ indicates to the processor that an external controller (e.g., DMA device) desires to utilize the address and data buses to transfer data to or from memory. The S9900 enters the hold state following a hold signal when it has completed its present memory cycle.* The processor then places the address and data buses in the high-impedance state (along with $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) and responds with a hold-acknowledge signal (HOLDA). When $\overline{\text{HOLD}}$ is removed, the processor returns to normal operation.
HOLDA	5	OUT	Hold acknowledge. When active (high), HOLDA indicates that the processor is in the hold state and the address and data buses and memory control outputs ($\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) are in the high-impedance state.
READY	62	IN	Ready. When active (high), READY indicates that memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the S9900 enters a wait state and suspends internal operation until the memory systems indicate ready.
WAIT	3	OUT	Wait. When active (high), WAIT indicates that the S9900 has entered a wait state because of a not-ready condition from memory.
			TIMING AND CONTROL
IAQ	7	OUT	Instruction acquisition. IAQ is active (high) during any memory cycle when the S9900 is acquiring an instruction. IAQ can be used to detect illegal op codes.
$\overline{\text{LOAD}}$	4	IN	Load. When active (low), $\overline{\text{LOAD}}$ causes the S9900 to execute a nonmaskable interrupt with memory address $FFFC_{16}$ containing the trap vector (WP and PC). The load sequence begins after the instruction being executed is completed. $\overline{\text{LOAD}}$ will also terminate an idle state. If $\overline{\text{LOAD}}$ is active during the time $\overline{\text{RESET}}$ is released, then the $\overline{\text{LOAD}}$ trap will occur after the $\overline{\text{RESET}}$ function is completed. $\overline{\text{LOAD}}$ should remain active for one instruction period. IAQ can be used to determine instruction boundaries. This signal can be used to implement cold-start ROM loaders. Additionally, front-panel routines can be implemented using CRU bits as front-panel interface signals and software-control routines to control the panel operations.
$\overline{\text{RESET}}$	6	IN	Reset. When active (low), $\overline{\text{RESET}}$ causes the processor to be reset and inhibits $\overline{\text{WE}}$ and CRUCLK. When $\overline{\text{RESET}}$ is released, the S9900 then initiates a level-zero interrupt sequence that acquires WP and PC from locations 0000 and 0002, sets all status register bits to zero, and starts execution. $\overline{\text{RESET}}$ will also terminate an idle state. $\overline{\text{RESET}}$ must be held active for a minimum of three clock cycles.

* If the cycle following the present memory cycle is also a memory cycle, it, too, is completed before the S9900 enters the hold state. The maximum number of consecutive memory cycles is three.

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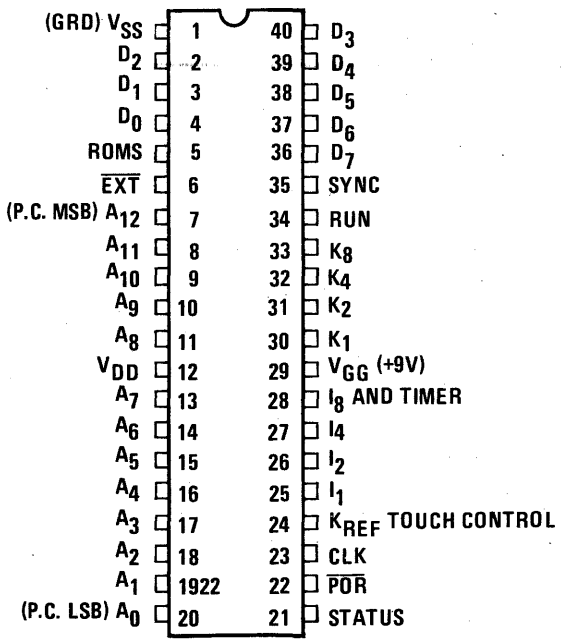
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TES-2000

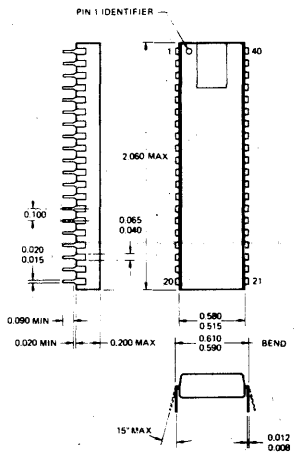
The TES-2000 is a dedicated S2000 tester which allows functional go/no-go comparison of CPU and ROM.

Pin Configuration

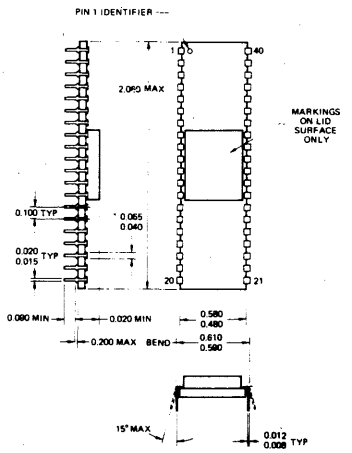


Physical Dimensions

40-PIN PLASTIC



40-PIN SLAM



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Absolute Maximum Ratings: (All voltages measured with respect to V_{SS})

Storage Temperature	-55°C to +125°C
Operating Temperature	0°C to +70°C
Maximum Positive Voltage	+18 Volts
Maximum Negative Voltage	-0.3 Volts
Maximum Output Currents	(See "Conditions" below)
I_{DD} Supply Current (depends on output loads)	75mA
Total Average Power Dissipation	500mW

Electrical Characteristics: (V_{SS} = 0V, V_{GG} = 9 ± 0.5V, V_{DD} = 5V*, T_A = 25°C)

	Parameter	Min.	Typ.	Max.	Units	Conditions
INPUTS	K_1 thru K_8					
	Low Level	0		K_{REP} -0.5	V	
	High Level	K_{REF} +0.5		V_{GG}	V	
INPUT	K_{REF}	0.28 V_{GG}		V_{GG}	—	
INPUTS	I_1 thru I_8 $\overline{POR}$ Schmitt-trigger					(Note 1)
	Low Level	0		.5	V	
	High Level	5.3		V_{GG}	V	
INPUTS	ROMs, RUN					
	Low Level	0		0.8	V	
	High Level	3.5		V_{GG}	V	
INPUTS	D_0 thru D_7					
	Low Level	0		0.8	V	
	High Level	4.5		V_{GG}	V	
OUTPUTS	A_0 thru A_3					
	High Level	3.5		*V_{DD}	V	I=-5mA
	Low Level	0		0.8	V	I=+25mA
OUTPUTS	A_4 thru A_{12} $\overline{EXT}$, SYNC, & S					
	High Level	3.5		*V_{DD}	V	I=-5mA
	Low Level	0		0.6	V	I=+5mA
OUTPUTS	D_0 thru D_7					
	High Level	3.5		*V_{DD}	V	I=-5mA
	Low Level	0		1.0	V	I=+12mA
I_{GG}	Supply Current		28	50	mA	

NOTE 1: There is an internal pull-up ≈ 100K from each of these inputs to V_{GG}.

*V_{DD} may be connected to V_{GG} if single power supply operation is desired.

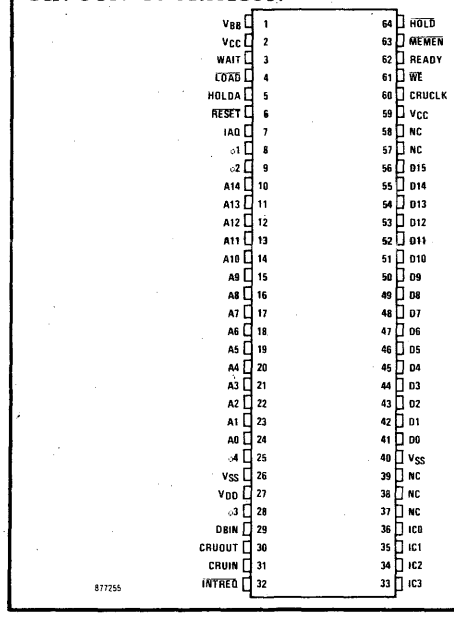
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16-Bit Single Chip Microprocessor

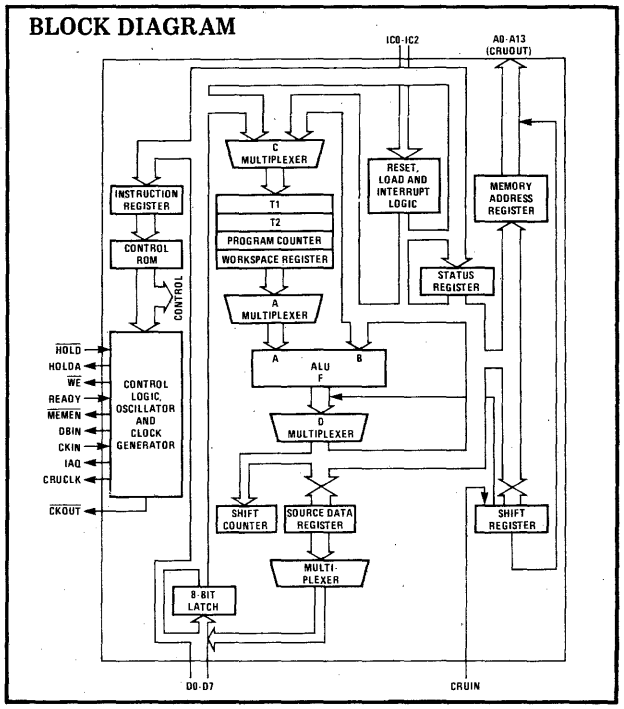
FEATURES

- 16-Bit Instruction Word
- 8 and 16-Bit Data Format
- Bi-directional Parallel 16-Bit Data Bus
- Parallel 15-Bit Address Bus Directly Addresses 32K Words or 64K Bytes
- Advanced Memory-to-Memory Architecture that Places Multiple Register Files in Memory
- 69 Instructions, Including Multiply and Divide
- Complete Software Compatibility with the TI9900 Minicomputer Family
- 7 Addressing Modes, 16 Prioritized Interrupts, 16 General Purpose Registers per File
- Direct Memory Access
- Easy Interface with Slow Memories
- TTL Compatible
- Standard Supply Voltages (+12V, +5V, -5V)

PIN CONFIGURATION



BLOCK DIAGRAM



The S9900 microprocessor is a single-chip 16-bit central processing unit produced using N-channel silicon gate MOS technology. The instruction set of the S9900 includes the capabilities offered by full minicomputers. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort. AMI provides a compatible set of MOS memory and logic function circuits to be used with an S9900 system. The system is fully supported by software and a complete prototyping system.

S9900 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
			ADDRESS BUS
A_0 (MSB)	24	OUT	A_0 through A_{14} comprise the address bus. This 3-state bus provides the memory-address vector to the external-memory system when MEMEN is active and I/O-bit addresses and external-instruction addresses to the I/O system when MEMEN is inactive. The address bus assumes the high-impedance state when HOLDA is active.
A_1	23	OUT	
A_2	22	OUT	
A_3	21	OUT	
A_4	20	OUT	
A_5	19	OUT	
A_6	18	OUT	
A_7	17	OUT	
A_8	16	OUT	
A_9	15	OUT	
A_{10}	14	OUT	
A_{11}	13	OUT	
A_{12}	12	OUT	
A_{13}	11	OUT	
A_{14} (LSB)	10	OUT	

SIGNATURE	PIN	I/O	DESCRIPTION
			DATA BUS
D_0 (MSB)	41	I/O	D_0 through D_{15} comprise the bi-directional 3-state data bus. This bus transfers memory data to (when writing) and from (when reading) the external-memory system when MEMEN is active. The data bus assumes the high-impedance state when HOLDA is active.
D_1	42	I/O	
D_2	43	I/O	
D_3	44	I/O	
D_4	45	I/O	
D_5	46	I/O	
D_6	47	I/O	
D_7	48	I/O	
D_8	49	I/O	
D_9	50	I/O	
D_{10}	51	I/O	
D_{11}	52	I/O	
D_{12}	53	I/O	
D_{13}	54	I/O	
D_{14}	55	I/O	
D_{15} (LSB)	56	I/O	

SIGNATURE	PIN	I/O	DESCRIPTION
			POWER SUPPLIES
V_{BB}	1		Supply voltage (-5V NOM)
V_{CC}	2,59		Supply voltage (5V NOM) Pins 2 and 59 must be connected in parallel.
V_{DD}	27		Supply voltage (12V NOM)
V_{SS}	26,40		Ground reference. Pins 26 and 40 must be connected in parallel.
			CLOCKS
$\phi 1$	8	IN	Phase-1 clock
$\phi 2$	9	IN	Phase-2 clock
$\phi 3$	28	IN	Phase-3 clock
$\phi 4$	25	IN	Phase-4 clock

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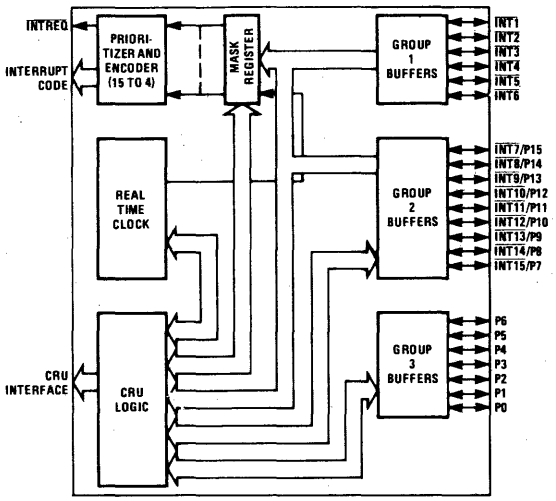
SIGNATURE	PIN	I/O	DESCRIPTION
			BUS CONTROL
DBIN	29	OUT	Data bus in. When active (high), DBIN indicates that the S9900 has disabled its output buffers to allow the memory to place memory-read data on the data bus during $\overline{\text{MEMEN}}$. DBIN remains low in all other cases except when HOLDA is active.
$\overline{\text{MEMEN}}$	63	OUT	Memory enable. When active (low), $\overline{\text{MEMEN}}$ indicates that the address bus contains a memory address.
$\overline{\text{WE}}$	61	OUT	Write enable. When active (low), $\overline{\text{WE}}$ indicates that memory write data is available from the S9900 to be written into memory.
CRUCLK	60	OUT	CRU clock. When active (high), CRUCLK indicates that external interface logic should sample the output data on CRUOUT or should decode external instructions on A_0 through A_2.
CRUIN	31	IN	CRU data in. CRUIN, normally driven by 3-state or open-collector devices, receives input data from external interface logic. When the processor executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A_3 through A_{14}).
CRUOUT	30	OUT	CRU data out. Serial I/O data appears on the CRUOUT line when an LDCR, SBZ, or SBO instruction is executed. The data on CRUOUT should be sampled by external I/O interface logic when CRUCLK goes active (high).
			INTERRUPT CONTROL
$\overline{\text{INTREQ}}$	32	IN	Interrupt request. When active (low), $\overline{\text{INTREQ}}$ indicates that an external interrupt is requested. If $\overline{\text{INTREQ}}$ is active, the processor loads the data on the interrupt-code-input lines IC_0 through IC_3 into the internal interrupt-code-storage register. The code is compared to the internal mask bits of the status register. If equal or higher priority than the enabled interrupt level (interrupt code equal or less than status register bits 12 through 15) the S9900 interrupt sequence is initiated. If the comparison fails, the processor ignores the request. $\overline{\text{INTREQ}}$ should remain active and the processor will continue to sample IC_0 through IC_3 until the program enables a sufficiently low priority to accept the request interrupt.
IC_0 (MSB)	36	IN	Interrupt codes. IC_0 is the MSB of the interrupt code, which is sampled when $\overline{\text{INTREQ}}$ is active. When IC_0 through IC_3 are LLLH, the highest external-priority interrupt is being requested and when HHHH, the lowest priority interrupt is being requested.
IC_1	35	IN	
IC_2	34	IN	
IC_3 (LSB)	33	IN	
			MEMORY CONTROL
$\overline{\text{HOLD}}$	64	IN	Hold. When active (low), $\overline{\text{HOLD}}$ indicates to the processor that an external controller (e.g., DMA device) desires to utilize the address and data buses to transfer data to or from memory. The S9900 enters the hold state following a hold signal when it has completed its present memory cycle.* The processor then places the address and data buses in the high-impedance state (along with $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) and responds with a hold-acknowledge signal (HOLDA). When $\overline{\text{HOLD}}$ is removed, the processor returns to normal operation.
HOLDA	5	OUT	Hold acknowledge. When active (high), HOLDA indicates that the processor is in the hold state and the address and data buses and memory control outputs ($\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) are in the high-impedance state.
READY	62	IN	Ready. When active (high), READY indicates that memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the S9900 enters a wait state and suspends internal operation until the memory systems indicate ready.
WAIT	3	OUT	Wait. When active (high), WAIT indicates that the S9900 has entered a wait state because of a not-ready condition from memory.
			TIMING AND CONTROL
IAQ	7	OUT	Instruction acquisition. IAQ is active (high) during any memory cycle when the S9900 is acquiring an instruction. IAQ can be used to detect illegal op codes.
$\overline{\text{LOAD}}$	4	IN	Load. When active (low), $\overline{\text{LOAD}}$ causes the S9900 to execute a nonmaskable interrupt with memory address $FFFC_{16}$ containing the trap vector (WP and PC). The load sequence begins after the instruction being executed is completed. $\overline{\text{LOAD}}$ will also terminate an idle state. If $\overline{\text{LOAD}}$ is active during the time $\overline{\text{RESET}}$ is released, then the $\overline{\text{LOAD}}$ trap will occur after the $\overline{\text{RESET}}$ function is completed. $\overline{\text{LOAD}}$ should remain active for one instruction period. IAQ can be used to determine instruction boundaries. This signal can be used to implement cold-start ROM loaders. Additionally, front-panel routines can be implemented using CRU bits as front-panel interface signals and software-control routines to control the panel operations.
$\overline{\text{RESET}}$	6	IN	Reset. When active (low), $\overline{\text{RESET}}$ causes the processor to be reset and inhibits $\overline{\text{WE}}$ and CRUCLK. When $\overline{\text{RESET}}$ is released, the S9900 then initiates a level-zero interrupt sequence that acquires WP and PC from locations 0000 and 0002, sets all status register bits to zero, and starts execution. $\overline{\text{RESET}}$ will also terminate an idle state. $\overline{\text{RESET}}$ must be held active for a minimum of three clock cycles.

* If the cycle following the present memory cycle is also a memory cycle, it, too, is completed before the S9900 enters the hold state. The maximum number of consecutive memory cycles is three.

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Programmable Systems Interface Circuit

BLOCK DIAGRAM

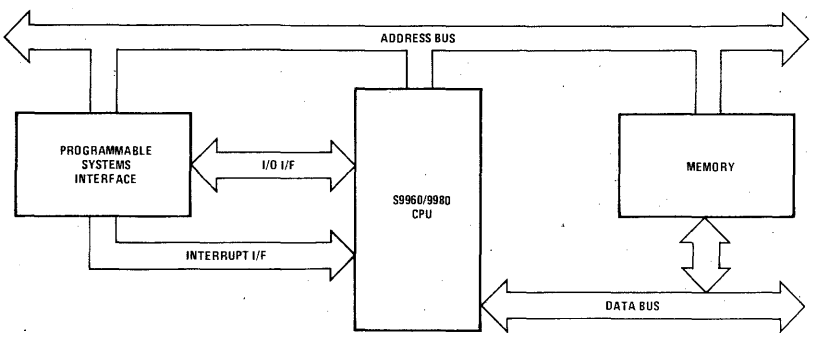


FEATURES

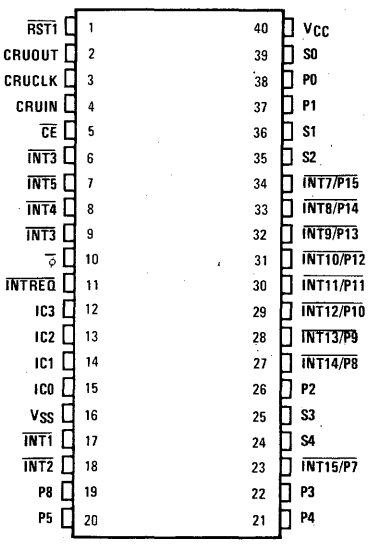
- N-Channel Silicon Gate Process
- S9900 Series CPU Peripheral
- Performs Interrupt and I/O Functions
  - 6 Dedicated Interrupt Input Lines
  - 7 Dedicated I/O Ports
  - 9 Ports Programmable as Interrupt or I/O
- Easily Stacked for Interrupt and I/O Expansion
- Interval and Event Timer
- Single +5V Power Supply

The S9901 Programmable Systems Interface is a multi-functioned component designed to provide low cost interrupts and I/O ports in a S9900/S9980 microprocessor system. It is fabricated with N-channel silicon gate technology and is completely TTL compatible on all inputs and outputs including the +5V power supply and single-phase clock, I/O ports, and a real-time clock. The main interface is through the Communications Register Unit as well as the interrupt control lines.

9900/9980 SYSTEM



PIN CONFIGURATION



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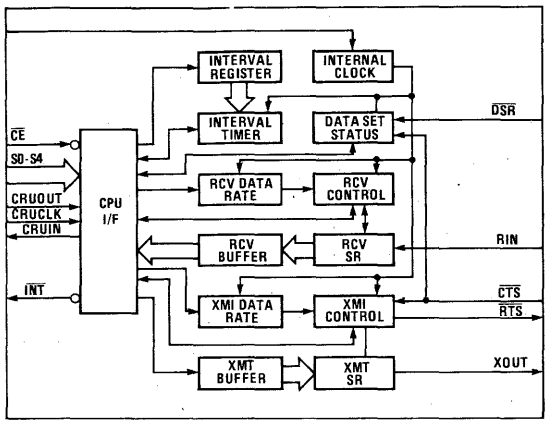
S9901 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{\text{INTREQ}}$	11	OUT	INTERRUPT Request. When active (low) $\overline{\text{INTREQ}}$ indicates that an enabled interrupt has been received. $\overline{\text{INTREQ}}$ will stay active until all enabled interrupt inputs are removed.
IC0 (MSB)	15	OUT	Interrupt Code lines. IC0-IC3 output the binary code corresponding to the highest priority enabled interrupt. If no enabled interrupts are active IC0-IC3 = (1, 1, 1, 1).
IC1	14	OUT	
IC2	13	OUT	
IC3 (LSB)	12	OUT	
$\overline{\text{CE}}$	5	IN	Chip Enable. When active (low) data may be transferred through the CRU interface to the CPU. $\overline{\text{CE}}$ has no effect on the interrupt control section.
S0	39	IN	Address select lines. The data bit being accessed by the CRU interface is specified by the 5-bit code appearing on S0-S4.
S1	36	IN	
S2	36	IN	
S3	25	IN	
S4	24	IN	
CRUIN	4	OUT	CRU data in (to CPU). Data specified by S0-S4 is transmitted to the CPU by CRUIN. When $\overline{\text{CE}}$ is not active CRUIN is in a high-impedance state.
CRUOUT	2	IN	CRU data out (from CPU). When $\overline{\text{CE}}$ is active, data present on the CRUOUT input will be sampled during CRUCLK and written into the command bit specified by S0-S4.
CRUCLK	3	IN	CRU Clock (from CPU). CRUCLK specifies that valid data is present on the CRUOUT line.
$\overline{\text{RST1}}$	1	IN	Power Up Reset. When active (low) $\overline{\text{RST1}}$ resets all interrupt masks to "0", disables the clock, and programs all I/O ports to inputs. $\overline{\text{RST1}}$ has a Schmitt-Trigger input to allow implementation with an RC circuit as shown in Figure 6.
V_{CC}	40		Supply Voltage. +5V nominal.
V_{SS}	16		Ground Reference.
$\overline{\phi}$	10		System clock ($\overline{\phi}3$ in S9900 system, $\overline{\text{CKOUT}}$ in S9980 system).
$\overline{\text{INT1}}$	17	IN	Group 1, interrupt inputs. When active (low) the signal is ANDed and its corresponding mask bit and if enabled sent to the interrupt control section. INT1 has highest priority.
$\overline{\text{INT2}}$	18	IN	
$\overline{\text{INT3}}$	9	IN	
$\overline{\text{INT4}}$	8	IN	
$\overline{\text{INT5}}$	7	IN	
$\overline{\text{INT6}}$	6	IN	
$\overline{\text{INT7}}$/P15	34	I/O	Group 2, programmable interrupt (active low) or I/O pins (true logic). Each pin is individually programmable as an interrupt, an input port, or an output port.
$\overline{\text{INT8}}$/P14	33	I/O	
$\overline{\text{INT9}}$/P13	32	I/O	
$\overline{\text{INT10}}$/P12	31	I/O	
$\overline{\text{INT11}}$/P11	30	I/O	
$\overline{\text{INT12}}$/P10	29	I/O	
$\overline{\text{INT13}}$/P9	28	I/O	
$\overline{\text{INT14}}$/P8	27	I/O	
$\overline{\text{INT15}}$/P7	23	I/O	
P0	38	I/O	Group 3, I/O ports (true logic). Each pin is individually programmable as an input port or an output port.
P1	37	I/O	
P2	26	I/O	
P3	22	I/O	
P4	21	I/O	
P5	20	I/O	
P6	19	I/O	

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Asynchronous Communications Controller (ACC)

BLOCK DIAGRAM



FEATURES

- 5 to 8-Bit Character Length
- 1, 1½ or 2 Stop Bits
- Even, Odd, or No Parity
- Fully Programmable Data Rate Generation
- Interval Timer with Resolution from 64 to 16,329μs
- Fully TTL Compatible, Including Single Power Supply

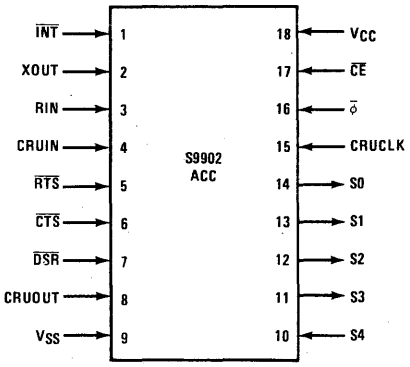
The S9902 Asynchronous Communication Controller (ACC) is a peripheral device for the S9900 family of microprocessors. The ACC provides an interface between the microprocessor and a serial asynchronous communication channel, performing the timing and data serialization and deserialization, thus facilitating the control of the asynchronous channel by the microprocessor.

S9902 PIN ASSIGNMENTS AND FUNCTIONS

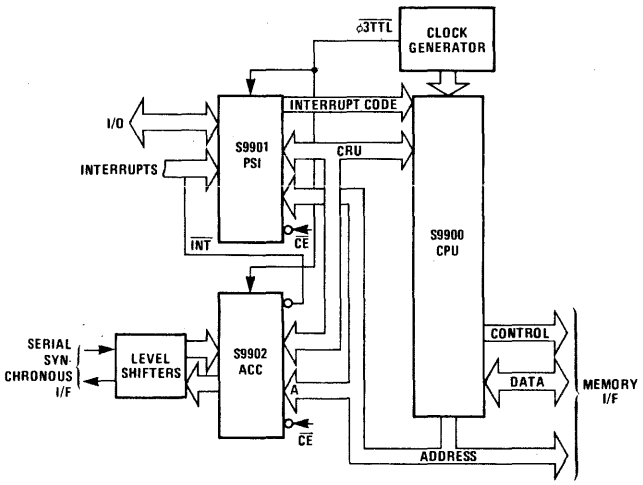
SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{INT}$	1	O	Interrupt — when active (low), the $\overline{INT}$ output indicates that at least one of the interrupt conditions has occured.
XOUT	2	O	Transmitter serial data output line — XOUT remains inactive (high) when S9902 is not transmitting.
RIN	3	I	Receiver serial data input line — RCV — must be held in the inactive (high) state when not receiving data. A transition from high to low will activate the receiver circuitry.
CRUIN	4	O	Serial data output pin from S9902 to CRUIN input pin of the CPU.
$\overline{RTS}$	5	O	Request-to-send output from S9902 to modem. This output is enabled by the CPU and remains active (low) during transmission from the S9902.
$\overline{CTS}$	6	I	Clear-to-send input from modem to S9902. When active (low), it enables the transmitter section of S9902.
$\overline{DSR}$	7	I	Data set ready input from modem to S9902. This input generates an interrupt when going On or Off.
CRUOUT	8	I	Serial data input line to S9902 from CRUOUT line of the CPU.
V_{SS}	9	I	Ground reference voltage.
S4 (LSB)	10	I	
S3	11	I	
S2	12	I	
S1	13	I	
S0	14	I	Address bus S0-S4 are the lines that are addressed by the CPU to select a particular S9902 function.
CRUCLK	15	I	CRU Clock. When active (high) S9902 from CRUOUT line of the CPU.
$\overline{\phi}$	16	I	TTL Clock.
$\overline{CE}$	17	I	Chip enable — when $\overline{CE}$ is inactive (high), the S9902 address decoding is inhibited which prevents execution of any S9902 command function. CRUIN remains at high-impedance when $\overline{CE}$ is inactive (high).
V_{CC}	18	I	Supply voltage (+5V nominal).

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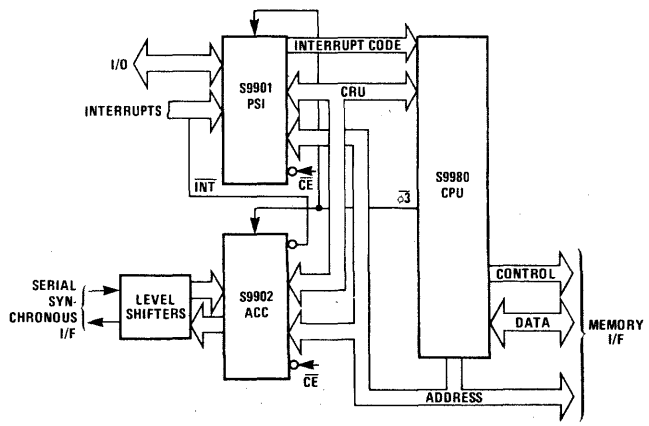
PIN CONFIGURATION



S9902 ACC IN A S9900 SYSTEM



S9902 ACC IN A S9980 SYSTEM



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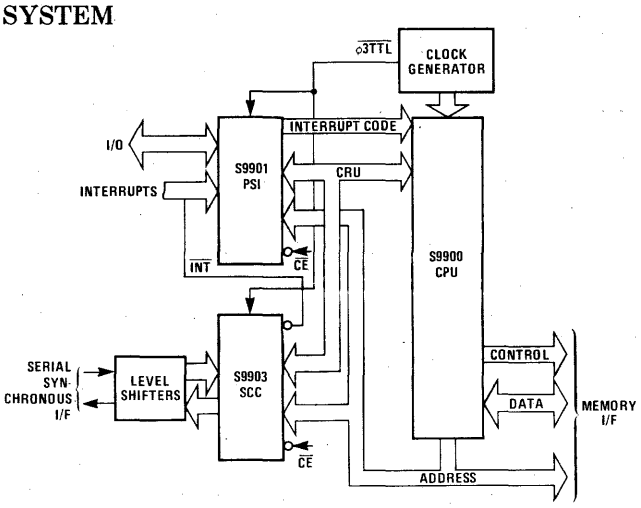
Synchronous Communications Controller

FEATURES

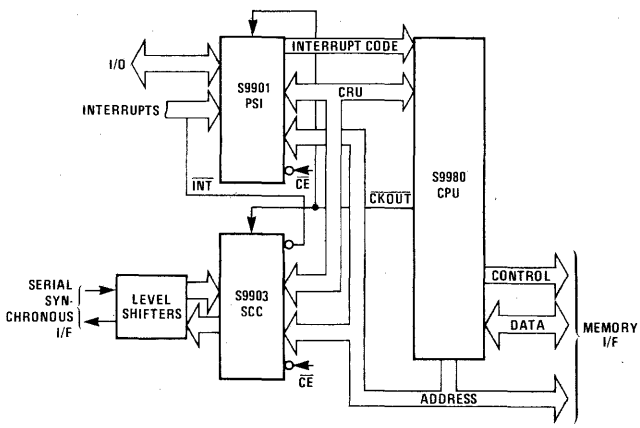
- Versatile CRU Interface to Synchronous and Asynchronous Serial Devices for the S99XX Series of Microprocessors
- Dynamic Character Length Selection
- Programmable Polynominal CRC Generation and Detection
- Two Programmable Sync Registers
- On-Chip Interval Timer (61μs to 16.32 ms)
- Single +5V Power Supply, 20-Pin DIP, All Inputs and Outputs TTL Compatible

The S9903 is a versatile device which provides the system designer with a wide range of capabilities in synchronous and asynchronous communications control. The S9903 operates in a multi-mode configuration that allows a broad range in the degree of active participation required in the control of sync and fill characters, timing, CRC generation and detection. Established protocols such as BI-SYNC, SDLC, and HDLC are implemented through various combinations of hardware and software.

S9903 SCC IN A S9900 SYSTEM

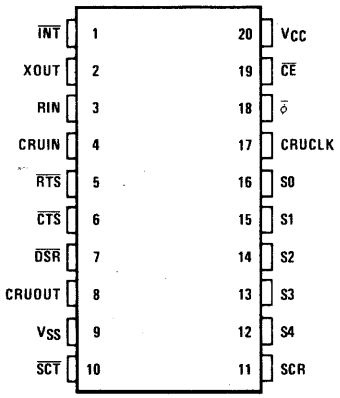


S9903 SCC IN A S9980 SYSTEM



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PIN CONFIGURATION



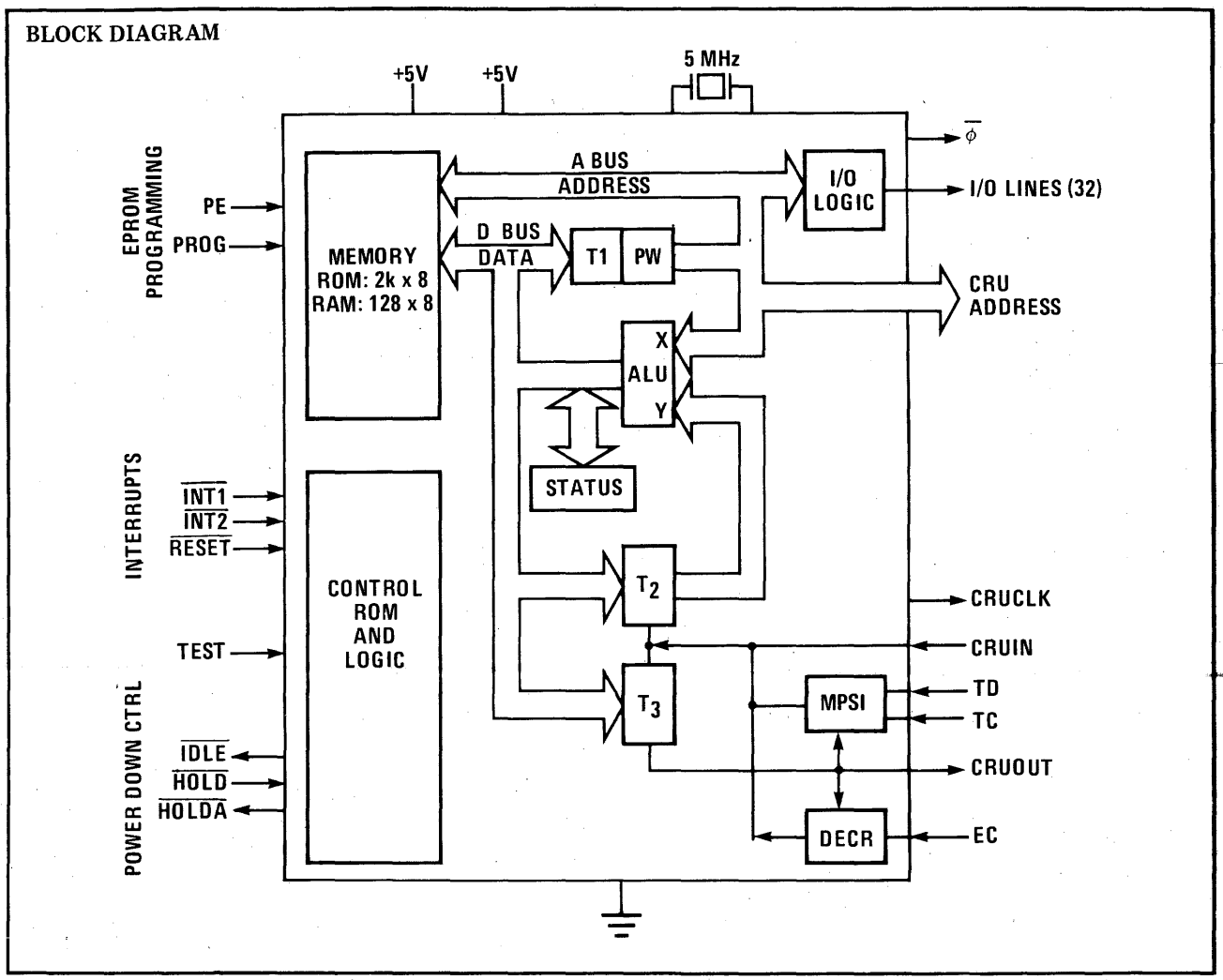
S9903 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{INT}$	1	OUT	Interrupt — When active (low), the $\overline{INT}$ output indicates that at least one of the interrupt conditions has occurred.
XOUT	2	OUT	Transmitter serial data output line.
RIN	3	IN	Receiver serial data input line.
CRUIN	4	OUT	Serial Data Output line from S9903 to CRUIN input line of the CPU.
$\overline{RTS}$	5	OUT	Request to Send output from S9903 to modem. This output is enabled by the CPU and remains active (low) during data transmission from S9903.
$\overline{CTS}$	6	IN	Clear-to-send input from modem to S9903. When active (low), it enables the transmitter section of the S9903.
$\overline{DSR}$	7	IN	Data Set Ready input from modem to S9903. This input generates an interrupt when going On or Off.
CRUOUT	8	IN	Serial data input line to S9903 from CRUOUT line of the CPU.
V_{SS}	9	IN	Ground Reference Voltage
$\overline{SCT}$	10	IN	Transmit clock — Transmitter data is shifted out on one-to-zero transition of $\overline{SCT}$.
SCR	11	IN	Receiver clock — Receiver serial data (RIN) is sampled at zero-to-one transition of SCR.
S4(LSB)	12	IN	Address bus S0-S4 are the lines that are addressed by the CPU to select a particular S9903 function.
S3	13	IN	
S2	14	IN	
S1	15	IN	
S0(MSB)	16	IN	
CRUCLK	17	IN	CRU Clock. When active (high), S9903 samples the input data on CRUOUT line.
$\bar{\phi}$	18	IN	TTL Clock
$\overline{CE}$	19	IN	Chip Enable — When $\overline{CE}$ is inactive (high), the S9903 address decoding is inhibited. CRUIN remains at high impedance when $\overline{CE}$ is inactive (high).
V_{CC}	20	IN	Supply voltage (+5V nominal)

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16-Bit Single Chip Microcomputer

BLOCK DIAGRAM



FEATURES

- 32 Bits General Purpose I/O, 256 Bits I/O Expansion
- Multiprocessor System Interface
- Single +5V Power Supply
- Power Down Mode for Low Standby Power
- 5MHz Operation
- 58 Instructions Including Multiply and Divide
- 128 Bytes RAM and 2048 Bytes ROM On Chip
- Mask Programmable and EPROM Versions
- 16 General Purpose Registers, 4 Prioritized Interrupts 16 User-Defined Program Control Flags
- Timer/Event Counter On Chip

The S9940 is a single-chip microcomputer containing a 16-bit CPU memory and extensive input/output capability. The memory consists of 128 bytes of read/write RAM and 2048 bytes of either mask programmable ROM (S9940N) or electrically reprogrammed ROM (S9940E). The S9940 is directly compatible with all members of the S9900 family of peripherals and is fully supported by both hardware and software development systems.

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AMI custom microcircuits are complex digital circuits designed to perform a specific function. Most could be described as "dedicated microprocessors." Because they are designed from scratch for a particular end product, custom microcircuits waste no space or capability, packing the maximum number of functions into the minimum area on the MOS/LSI chip. For volume applications, when compared with microprocessors, combinations of standard microcircuits, discrete electronic components, or electromechanical devices, custom microcircuits are often the most cost effective alternative.

No other company can match AMI's track record in developing state-of-the-art custom MOS circuits. Since 1966 AMI has been providing customers with circuits that have enhanced the marketability of their products by added features, continuously increasing reliability and reduced space requirements.

AMI not only has the experience but also the design engineering organization, and the technologically advanced production and testing facilities, to make the highest quality MOS/LSI circuits. Because AMI also manufactures standard, memory, and microprocessor products, all using a variety of advanced microcircuit process technologies, the company can be objective in helping customers determine their most cost effective approach. For example, AMI will participate in the design cycle of the custom circuit only to the extent needed by the customer. This ranges from zero to the complete design task.

With more than 1,000 custom devices designed and manufactured during the past 10 years, AMI has more experience than any other IC manufacturer in building a wide variety of custom microcircuits. The following are some of the products in which AMI custom circuits are being used: consumer, business, communications/navigation, industrial/instrumentation, and terminal/peripheral.

AMI's custom capability encompasses the entire development sequence of a product. The services which AMI provides to the customer start with five conceptual planning steps:

- System Definition
- System Design and Partitioning
- Preliminary Logic Design and Simulation
- Final Logic Design
- Chip Circuit Design

First, system definition requires the customer to have full knowledge of the system requirements for the circuit. Working with AMI's MOS/LSI application experts, the two companies form a team to develop a system which not only meets the needs, but also optimizes performance and economy.

Step two, system partitioning, follows the joint system definition. Partitioning involves the cataloguing of functions into MOS subfunctions and then into chip functions. During this step of the program the best MOS process for the application is selected. Usually, functional flow charts and timing diagrams are generated as a preliminary step in the logic design.

Once partitioning is accomplished, preliminary logic design and simulation can be done. The chip functions, as catalogued in step two, are translated into MOS logic diagrams and traditional breadboarding techniques are quite often used to verify these logic designs. AMI also uses proprietary computerized simulation programs for verification. These programs check the design, as well as help reduce time and cost of design verification.

Final logic design is next. First, errors discovered through breadboarding or simulation are corrected. Earlier partitioning may be refined, if the final logic design indicates a need. During the final logic design step, all system design objectives are analyzed again, MOS logic diagrams are finalized, chip sizes are estimated, and testing procedures are generated.

And then — chip circuit design. The topological chip layout is a precise science. The exact dimensions and placement of each transistor and other functions must be determined. The list of factors affecting chip design is almost endless: the use of space, the economy of functions, the versatility of functions, the power requirements, the manufacturing processes, the interconnections, the packaging, the performance of the circuit, the reliability of the design, and so on. All must be considered in the circuit layout design leading to final topological definition. Here again, AMI uses computerized circuit analysis programs to validate chip design and verify that the design meets performance objectives determined during system definition. The computerized analysis not only substantiates the logic, it is an integral part of the ongoing quality assurance program at AMI.

The AMI Quality Assurance Program is an ongoing activity that pervades the entire design and manufacturing process. The quality assurance function includes a special group of inspectors, organizationally separate from production. The main responsibility of these inspectors is to examine and test custom circuits and all the raw materials that go into them. The following is a partial list of the quality control checkpoints in the creation of a custom circuit. At each of these preproduction steps, meticulous checks of both design and workmanship are made.

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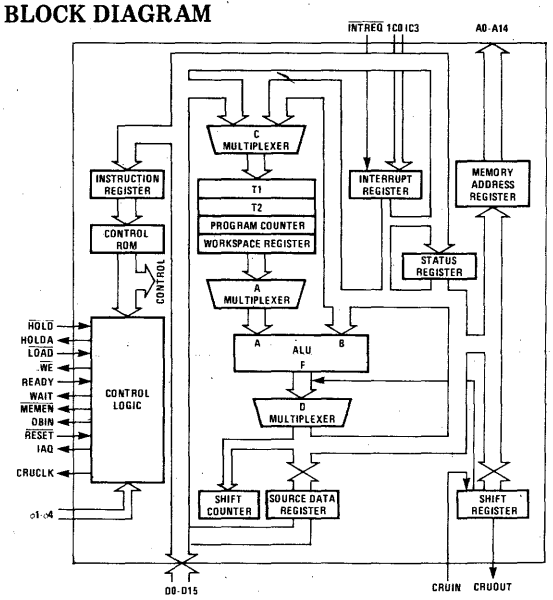
16-Bit Single Chip CPU

FEATURES

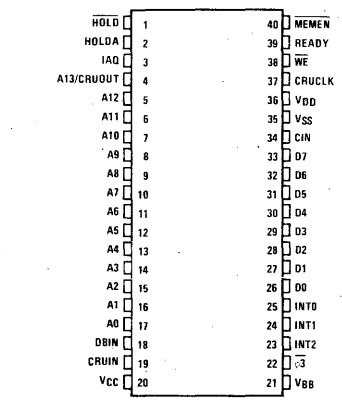
- 16-Bit Instruction Word
- Full Minicomputer Instruction Set Capability Including Multiple and Divide
- Up to 16,384 Bytes of Memory
- 8-Bit Memory Data Bus
- Advanced Memory-to-Memory Architecture
- Separate Memory, I/O, and Interrupt-Bus Structures
- 16 General Registers, 4 Prioritized Interrupts
- Programmed and DMA I/O Capability
- On-Chip Oscillator with External Frequency Option

The S9980 is a software-compatible member of AMI's S9900 family of microprocessors. Designed to minimize the system cost for smaller systems, the S9980 is a single-chip 16-bit CPU which has an 8-bit data bus, on-chip clock, and is packaged in a 40-pin package. The instruction set of the S9980 includes the capabilities offered by full minicomputers and is exactly the same as the S9900. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort. AMI provides a compatible set of MOS memory and logic function circuits to be used with an S9980 system.

BLOCK DIAGRAM



PIN CONFIGURATION



877255

S9980 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
			ADDRESS BUS
A_0 (MSB)	17	OUT	A_0 through A_{13} comprise the address bus. This 3-state bus provides the memory-address vector to the external-memory system when $\overline{MEMEN}$ is active and I/O-bit addresses and external-instruction addresses to the I/O system when $\overline{MEMEN}$ is inactive. The address bus assumes the high-impedance state when HOLDA is inactive.
A_1	16	OUT	
A_2	15	OUT	
A_3	14	OUT	
A_4	13	OUT	
A_5	12	OUT	
A_6	11	OUT	
A_7	10	OUT	
A_8	9	OUT	
A_9	8	OUT	
A_{10}	7	OUT	
A_{11}	6	OUT	
A_{12}	5	OUT	
A_{13}/CRUOUT	4	OUT	
			CRUOUT
			Serial I/O data appears on A_{13} when an LDCR, SBZ and SBO instruction is executed. This data should be sampled by the I/O interface logic when CRUCLK goes active (high). One bit of the external instruction code appears on A_{13} during external instruction execution.
			DATA BUS
D_0 (MSB)	26	I/O	D_0 through D_7 comprise the bi-directional 3-state data bus. This bus transfers memory data to (when writing) and from (when reading) the external-memory system when $\overline{MEMEN}$ is active. The data bus assumes the high-impedance state when HOLDA is active.
D_1	27	I/O	
D_2	28	I/O	
D_3	29	I/O	

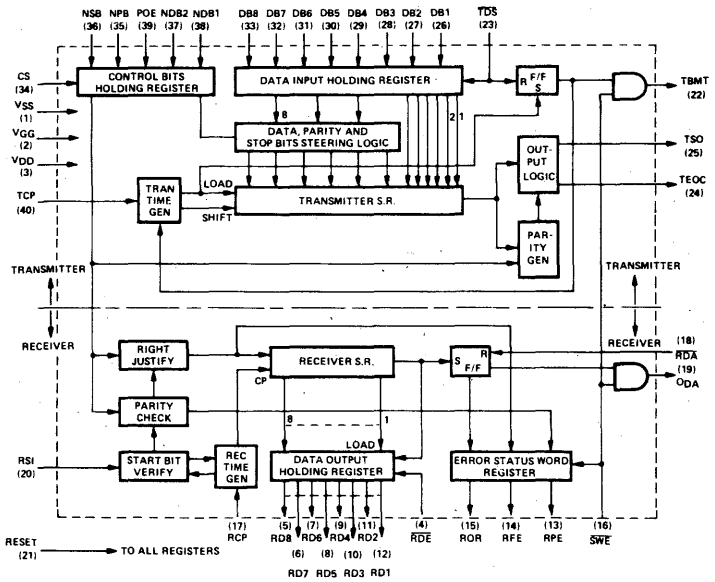
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SIGNATURE	PIN	I/O	DESCRIPTION
D_4	30	I/O	
D_5	31	I/O	
D_6	32	I/O	
D_7 (LSB)	33	I/O	
			POWER SUPPLIES
V_{BB}	21		Supply voltage (-5V NOM)
V_{CC}	20		Supply voltage (5V NOM)
V_{DD}	36		Supply voltage (12V NOM)
V_{SS}	35		Ground reference
			CLOCKS
CIN	34	IN	The S9980 has an on-chip oscillator to generate the system clock (2MHz). But an option is provided to allow external system clock. CKIN is tied to +12V to use the internal oscillator. Alternately, a TTL level periodic wave of frequency equal to or less than 12MHz may be applied to CKIN. In the latter case, the internal oscillator is ignored and external frequency is used to generate the system clock (3MHz or less).
$\overline{\phi 3}$	22	OUT	Clock phase 3 ($\overline{\phi 3}$) inverted.
			BUS CONTROLS
DBIN	18	OUT	Data bus in. When active (high), DBIN indicates that the S9980 has disabled its output buffers to allow the memory to place memory-read data on the data bus during $\overline{\text{MEMEN}}$. DBIN remains low in all other cases except when HOLDA is active.
$\overline{\text{MEMEN}}$	40	OUT	Memory enable. When active (low), $\overline{\text{MEMEN}}$ indicates that the address bus contains a memory address.
$\overline{\text{WE}}$	38	OUT	Write enable. When active (low), $\overline{\text{WE}}$ indicates that memory-write data is available from the S9980 to be written into memory.
CRUCLK	37	OUT	CRU clock. When active (high), CRUCLK indicates that external interface logic should sample the output data on CRUOUT or should decode external instructions on A_0, A_1, A_{13}.
CRUIN	19	IN	CRU data in. CRUIN, normally driven by 3-state or open-collector devices, receives input data from external interface logic. When the processor executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A_2 through A_{12}).
INT0	23	IN	Interrupt code. Refer to Section 2.2 for detailed description.
INT1	24	IN	
INT2	25	IN	
			MEMORY CONTROL
$\overline{\text{HOLD}}$	1	IN	Hold. When active (low), $\overline{\text{HOLD}}$ indicates to the processor that an external controller (e.g., DMA device) desires to utilize the address and data buses to transfer data to or from memory. The S9980 enters the hold state following a hold signal when it has completed its present memory cycle.* The processor then places the address and data buses in the high-impedance state (along with $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) and responds with a hold-acknowledge signal (HOLDA). When $\overline{\text{HOLD}}$ is removed, the processor returns to normal operation.
HOLDA	2	OUT	Hold acknowledge. When active (high), HOLDA indicates that the processor is in the hold state and the address and data buses and memory control outputs ($\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) are in the high-impedance state.
READY	39	IN	Ready. When active (high), READY indicates that memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the S9980 enters a wait state and suspends internal operation until the memory system indicates ready.
			TIMING AND CONTROL
IAQ	3	OUT	Instruction acquisition. IAQ is active (high) during any memory cycle when the S9980 is acquiring an instruction. IAQ can be used to detect illegal op codes. It may also be used to synchronize LOAD stimulus.

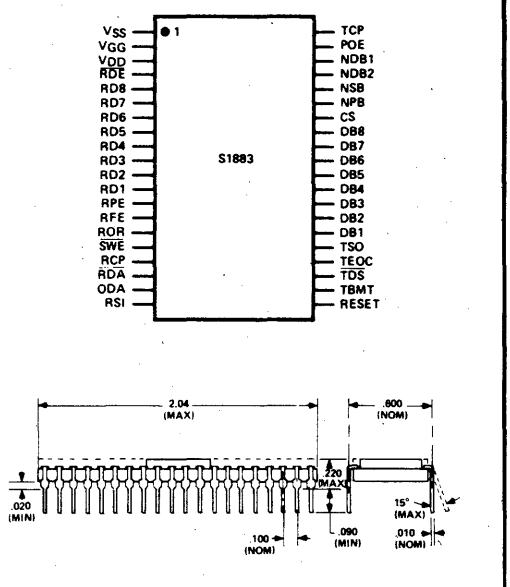
* If the cycle following the present memory cycle is also a memory cycle, it too is completed before S9980 enters hold state.

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Universal Asynchronous Receiver/Transmitter (UART)



S1883 BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- 12.5 K Baud Data Rates
- 5-8 Bit Word Length
- Parity Generation/Checking Odd, Even, None
- Framing and Overflow Error Detection
- 1, 1.5, or 2 Stop Bits
- Double Buffered Input/Output
- Independent Transmit/Receive Rates
- Start and Stop Bits Generated and Detected
- Interchangeable with TMS6011, COM2017, TR1602, AY-5-1013
- Tri-State Outputs

FUNCTIONAL DESCRIPTION

The S1883 Universal Asynchronous Receiver Transmitter (UART) is a single chip MOS/LSI device that totally replaces the asynchronous parallel to serial and serial to parallel conversion logic required to interface a word parallel controller or data terminal to a bit serial communication network.

For asynchronous data transmission with a non-contiguous data bit stream, the UART automatically inserts a START bit preceding each character and under program control 1, 1.5, or 2 stop bits at the end of each character. To detect incoming characters in a noisy environment the UART employs a START bit detection network and allows errorless recovery of data with up to 42% distortion.

The UART will transmit or receive data characters of 5, 6, 7, or 8 bit length. Options allow the generation and checking of odd, even parity or no parity. The odd or even parity bit is automatically added to the character length for transmission. The parity bit is removed, checked and an error flag set if incorrectly received.

The data or baud rate at the receiver input and transmitter output are determined independently by external clock inputs. The clock inputs must be 16 times the data rate required at the serial input and output. The independent clocks allow for either half or full duplex operation.

The UART provides a buffer register in both the transmitter and receiver to allow a full character time for responding to a received data ready or transmit data request signal. The UART generates a MARK signal if the transmit register is not loaded with a data character and also indicates an overflow error if two characters are received without a RDA input.

TYPICAL APPLICATIONS

- Computer Peripherals
- Communication Concentrators
- Integrated Modems
- Industrial Data Transmission
- TTY Terminals
- Time Division Multiplexing

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Positive Voltage on Any Pin with Respect to V_{SS}	+.3 Volt
Negative Voltage on Any Pin with Respect to V_{SS}	−20.0 Volt

NOTE: Stresses greater than those listed as Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operation section of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC (STATIC) CHARACTERISTICS

$T_A = 0° - +70°C$, $V_{SS} = +5$ Volt ±5%, $V_{GG} = -12$ Volt ±5%

Symbol	Parameter	Min	Max	Unit	Condition
V_{IH}	Input High Voltage	V_{SS} −1.0	V_{SS} +0.3	Volt	Internal Pull-up
V_{IL}	Input Low Voltage	V_{GG}	0.8	Volt	Resistor Provided
I_{LI}	Input Load Current		−1.2	mamp	V_{IN} = 0 Volt
V_{OH}	Output High Voltage	2.4		Volt	I_{OH} = - 100 uamp
V_{OL}	Output Low Voltage		.4	Volt	I_{OL} = 1.6 mamp
C_{IN}	Input Capacitance		20	pf	$V_{IN} = V_{SS}$
C_{OUT}	Output Capacitance		10	pf	$V_{OUT} = V_{SS}$
I_{SS}	V_{SS} Supply Current		30	mamp	$\overline{SWE} = \overline{RDE} = V_{IL}$
I_{GG}	V_{GG} Supply Current		40	mamp	ITTL Load

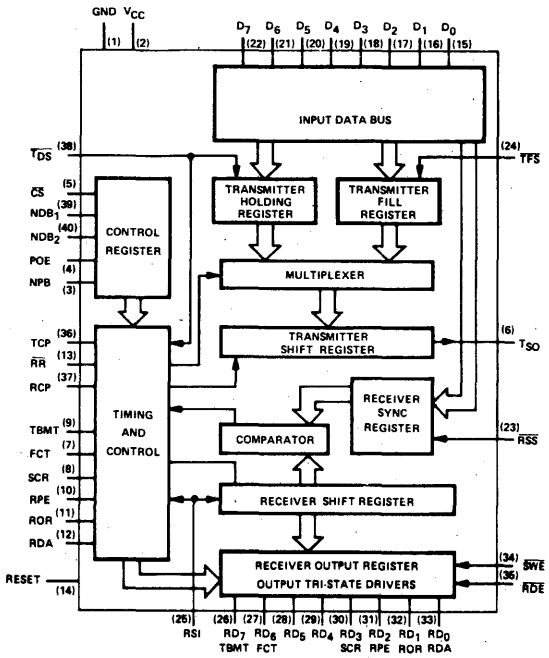
AC (DYNAMIC) CHARACTERISTICS

$T_A = 0°C - +70°C$; $V_{SS} = +5$ Volt ±5%; $V_{GG} = -12$ Volt ±5%

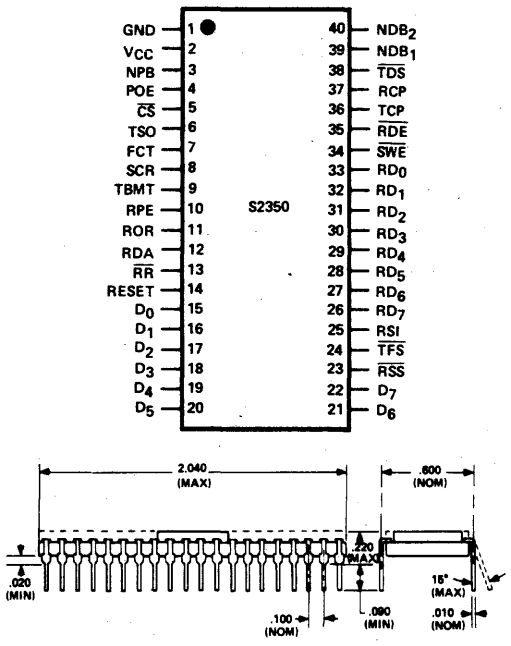
Symbol	Parameter	Min	Max	Unit	Condition
TCP, RCP	Clock Frequency	DC	200	KHz	
Input Pulse Widths					
PWTCP	Transmit Clock	2.5		usec	C_L = 20pf
PWRCP	Receive Clock	2.5		usec	1 TTL Load
PWCS	Control Strobe	250		nsec	
PWTDS	Transmit Data Strobe	250		nsec	
PWRST	RESET	1.0		μsec	
PWSWE	Status Word Enable	500		nsec	
PWRDA	Reset Data Available	500		nsec	
PWRDE	Receive Data Enable	250		nsec	
Switching Characteristics					
t_{CDS}	Control Set Up Time	0		nsec	Figure 1
t_{CDH}	Control Hold Time	20		nsec	Figure 1
t_{OE}	Output Enable Time		500	nsec	
t_{OD}	Output Disable Time		500	nsec	

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Universal Synchronous Receiver/Transmitter (USRT)



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- 500 KHz Data Rates
- Internal Sync Detection
- Fill Character Register
- Double Buffered Input/Output
- Bus Oriented Outputs
- 5–8 Bit Characters
- Odd/Even or No Parity
- Error Status Flags
- Single Power Supply (+5v)
- Input/Output TTL Compatible

FUNCTIONAL DESCRIPTION

The S2350 Universal Synchronous Receiver Transmitter (USRT) is a single chip MOS/LSI device that totally replaces the serial to parallel and parallel to serial conversion logic required to interface a word parallel controller or data terminal to a bit-serial, synchronous communication network.

The USRT consists of separate receiver and transmitter sections with independent clocks, data lines and status. Common with the transmitter and receiver are word length and parity mode. Data is transmitted and received in a NRZ format at a rate equal to the respective input clock frequency.

Data messages are transmitted as a contiguous character stream, bit synchronous with respect to a clock and character synchronous with respect to framing or "sync" characters initializing each message. The USRT receiver compares the contents of the internal Receiver Sync Register with the incoming data stream in a bit transparent mode. When a compare is made, the receiver becomes character synchronous formatting a 5, 6, 7, or 8 bit character for output each character time. The receiver has an output buffer register allowing a full character time to transfer the data out. The receiver status outputs indicate received data available (RDA), receiver overrun (ROR), receive parity error (RPE) and sync character received (SCR). Status bits are available on individual output lines and can also be multiplexed onto the output data lines for bus organized systems. The data lines have tri-state outputs.

The USRT transmitter outputs 5, 6, 7, or 8 bit characters with correct parity at the transmitter serial output (TSO). The transmitter is buffered to allow a full character time to respond to a transmitter buffer empty (TBMT) request for data. Data is transmitted in a NRZ format changing on the positive transition of the transmitter clock (TCP). The character in the transmitter fill register is inserted into the data message if a data character is not loaded into the transmitter after a TBMT request.

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TYPICAL APPLICATIONS

- Computer Peripherals
- Communication Concentrators
- Integrated Modems
- High Speed Terminals
- Time Division Multiplexing
- Industrial Data Transmission

ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0°C to + 70°C
Storage temperature	–65°C to +150°C
Positive voltage on any pin with respect to GROUND	+7 volt
Negative voltage on any pin with respect to GROUND	–0.5 volt
Power dissipation	0.75 watt

DC (STATIC) CHARACTERISTICS*

V_{CC} = +5V ±5V ±5%, T_A = 25°C unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{IH}	Input High Voltage	2.0	V_{CC}	Volt	
V_{IL}	Input Low Voltage	- 0.5	+0.8	Volt	
I_{IL}	Input Leakage Current		10	μa	V_{IN} = OTO V_{CC} Volts
V_{OH}	Output High Voltage	2.4		Volts	I_{OH} = –100μa
V_{OL}	Output Low Voltage		+0.4	Volts	I_{OL} = 1.6ma
C_{IN}	Input Capacitance		10	pf	V_{IN} = 0 Volt, f = 1.0 MHZ
C_{OUT}	Output Capacitance		12	pf	V_{IN} = 0 Volt, f = 1.0 MHZ
I_{CC}	V_{CC} Supply Current		100	ma	No Load

*Electrical characteristics included in this advanced product description are objective specifications and may be subject to change.

AC (DYNAMIC) CHARACTERISTICS

V_{CC} = +5V ±5%, T_A = 25°C unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Condition
TCP, RCP	Clock Frequency	DC	500	KHz	

Input Pulse Widths

P_{TCP}	Transmit Clock	900		nsec	C_L = 20pf
P_{RCP}	Receive Clock	900		nsec	1TTL Load
P_{RST}	Reset	500		nsec	
$P_{\overline{TDS}}$	Transmit Data Strobe	200		nsec	
$P_{\overline{TFS}}$	Transmit Fill Strobe	200		nsec	
$P_{\overline{RSS}}$	Receive Sync Strobe	200		nsec	
$P_{\overline{CS}}$	Control Strobe	200		nsec	
$P_{\overline{RDE}}$	Receive Data Enable	400		nsec	Note 1
$P_{\overline{SWE}}$	Status Word Enable	400		nsec	Note 1
$P_{\overline{RR}}$	Receiver Restart	500		nsec	

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4096 Bit (512×8) Erasable and Electrically Reprogrammable ROM

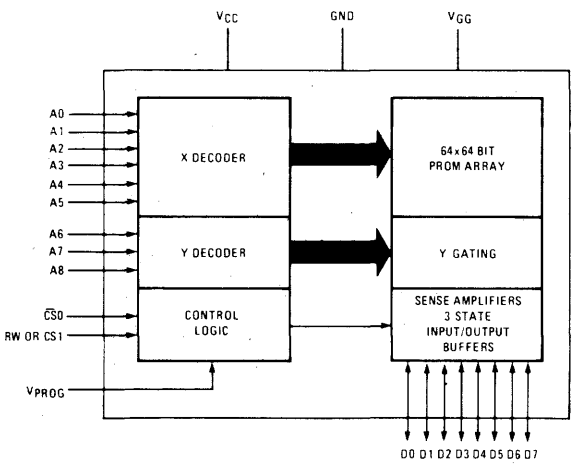
Features

- ☐ On-Board Programmability
- ☐ Fast Access Time — 750ns Max.
- ☐ High Speed Programming — Less than 1 Minute for all 4096 Bits
- ☐ Programmed with R/W, CS and V_{PROG} Pins
- ☐ Completely TTL Compatible — Excluding the V_{PROG} Pin during Read or Write
- ☐ Ultraviolet Light Erasable — Less than 10 Minutes
- ☐ Static Operation — No Clocks Required
- ☐ Three-State Data I/O
- ☐ Standard Power Supplies — +5V and -12V
- ☐ Mature P-Channel Process

General Description

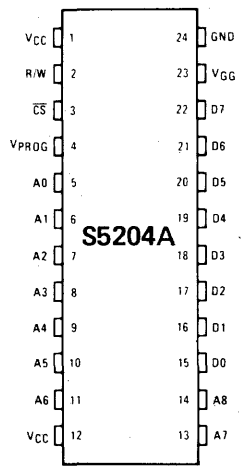
The S5204A is a high speed, static, 512x8 bit, erasable and electrically programmable read only memory designed for use in bus-organized systems. Both input and output are TTL compatible during both read and write modes. Packaged in a 24-pin hermetically sealed dual in-line package, the bit pattern can be erased by exposing the chip to an ultraviolet light source through the transparent lid, after which a new pattern can be written.

Block Diagram



77675

Pin Configuration



877254

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} except the V_{PROG} pin	+0.3V to -20V
Voltage on the V_{PROG} pin relative to V_{SS}	+0.3V to -60V
Operating Temperature	0°C to +70°C
Storage Temperature (programmed)	-55°C to +85°C
Storage Temperature (unprogrammed)	-55°C to +150°C

Typical Applications

- ☐ ROM Program Debugging
- ☐ Code Translation
- ☐ Microprogramming
- ☐ Look-up Tables
- ☐ Random Logic Replacement
- ☐ Programmable Waveforms
- ☐ Character Generation
- ☐ Electronic Keyboards

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

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DC (STATIC) CHARACTERISTICS (V_{CC} = +5.0V ± 5%, V_{GG} = −12.0V ± 5% T_A = 0 – 70°C unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
V_{IL}	INPUT VOLTAGE LOW		0.8	V
V_{IH}	INPUT VOLTAGE HIGH	V_{CC} −2.25	V_{CC} +.3	V
V_{OL}	OUTPUT VOLTAGE LOW I_{OL} = 1.6 ma		0.4	V
V_{OH}	OUTPUT VOLTAGE HIGH I_{OH} = 200 μA	2.4		V
I_{LI}	INPUT LEAKAGE CURRENT		10	μa
I_{LO}	OUTPUT LEAKAGE CURRENT CS = 5V		20	μa
I_{GG}	V_{GG} SUPPLY CURRENT		45	ma
I_{CC}	V_{CC} SUPPLY CURRENT		50	ma
P_D	POWER DISSIPATION		750	mw

NOTE: Program input V_{PROG} may be tied to V_{CC} during the Read.

AC (DYNAMIC) CHARACTERISTICS (Loading is as shown in Figure 1 unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
T_{ACC}	ACCESS TIME		750	ns
T_{CO}	CHIP SELECT TO OUTPUT DELAY		400	ns
T_{DD}	CHIP DESELECT TO OUTPUT DELAY			ns

PROGRAM CHARACTERISTICS (R/W G_{nd}, Program pulse rise and fall time (10% to 90%) are both at 1μs max).

SYMBOL	CHARACTERISTICS	MIN	MAX	UNIT
T_{AS}	ADDRESS SET UP TIME	10		μs
T_{CSS}	CHIP SELECT SET UP TIME	10		μs
T_{DS}	DATA SET UP TIME	10		μs
T_{AH}	ADDRESS HOLD TIME	10		μs
T_{CSH}	CHIP SELECT HOLD TIME	10		μs
T_{DH}	DATA HOLD TIME	10		μs
T_{PWL}	PROGRAM PULSE WIDTH LOW	3	5	ms
T_{PWH}	PROGRAM PULSE WIDTH HIGH	500		μs
V_{PROG}*	PROGRAM AMPLITUDE	−55	−50	V
I_{PROG}	PROGRAM CURRENT		35	ma
T_{WS}	WRITE SET UP TIME	10		μs
T_{WH}	WRITE HOLD TIME	5		μs
T_{RS}	READ SET UP TIME	10		μs

*Note that in the WRITE mode the MIN value of V_{PROG} should not be exceeded and that chip select, address, and data lines may remain at TTL level, as in the READ mode

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INTERFACE DESCRIPTION

Pin	Label	Function
(15)	D0	**Data Lines** – with the R/W line selected for Read (V_{IH}), the Data Line (D0 through D7) are set to reflect the contents of the selected memory location. When the R/W line is set for Write (V_{IL}), the Data Lines are stored at the addressed location of the 5204A when V_{PROG} is present. The Data Bus output drivers are three-state devices that remain in the high impedance (off) state whenever CS is in the V_{IH} state or when R/W is in the V_{IL} state.
(16)	D1	
(17)	D2	
(18)	D3	
(19)	D4	
(20)	D5	
(21)	D6	
(22)	D7	
(2)	R/W	**Read/Write** – When this input line is set to V_{IH}, the device is in the Write mode, a low (V_{IL}) signal puts it into the Read mode.
(3)	CS	**Chip Select** – This input line must be set to V_{IL} for a Read or Write operation to be performed. When it is High (V_{IH}) the output data bus is set to a high-impedance three-state condition.
(4)	V_{PROG}	**Program** – In the Write mode, a 50Volt programming pulse at this input causes the data at the Data Lines to be stored in the selected address location. This pin should be tied to V_{CC} for normal Read operations.
(5)	A0	**Address Lines** – These lines select the 8 bit word in memory for Read or Write operation.
(6)	A1	
(7)	A2	
(8)	A3	
(9)	A4	
(10)	A5	
(11)	A6	
(13)	A7	
(14)	A8	

CONTROL FUNCTION TRUTH TABLE

CS	R/W	V_{PROG}	MODE	OUTPUTS
0	1	V_{PROG}	Write	Active Data Inputs
0	0	V_{CC}	Read	Active
1	X	X	Standby	Floating

OPERATION

Initially, and after each erasure, all bits of the 5204A are in the LOW state (output 0 volts). Data is stored by selectively programming a HIGH into the desired bit locations. The R/W input (pin 2) is used to select the desired mode of operation. When the R/W input is HIGH the chip is in the write enable mode of operation. The outputs (D_0 – D_7) are disabled (floating) with the corresponding pins becoming the data inputs. The word address is selected in the same manner as in the Read mode. Data to be programmed is presented 8 bits in parallel and after the address and data are set up a programming pulse (V_P = - 50 volts) is applied. V_{PROG} electrically writes the data into the memory array. Writing may be inhibited by deselecting the chip with the CS input at a HIGH during the write cycle. This feature allows true "on board" programming in bus organized systems where the R/W and V_{PROG} inputs are common and the device to be programmed is selected by means of the chip select input as during read operations.

The amount of program energy required to insure memory retention may be defined as a function of the number of program pulses (N) times the program pulse width (t_{pw}) ($N \times t_{pw} \geq 60$ msec). This means if a 3 ms pulse is used, 20 program pulses are required, and if a 5 ms pulse is used 12 program pulses are required.

The read operation is accomplished by a LOW at the R/W input with the program input connected to V_{SS} potential. True data (data out = date in) is valid after the address is stable. The CS input will disable (float) the outputs when HIGH to allow capability with bus organized systems.

Erasure is accomplished by exposing the array to a 2537Å ultra-violet light source (such as Ultra-Violet Products, Inc. Lamp Model S52 or UVS-54, Turner Designs PROM Eraser, Model 30 or equivalent) for a period of 7 to 10 minutes. The clear optical lid should be approximately one inch away from the lamp tubes.

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THE FORMULATOR LINE OF F8 AND F3870 DESIGN AIDS

INTRODUCTION

The Microprocessor system designer can now create his own hardware and software development systems for the F8 and F3870 by selecting modular subassemblies from Fairchild's Formulator line of F8 and F3870 design aids. He may start development with a Mark I singleboard system, then expand to more sophisticated Mark II or Mark IIFD development systems that can handle both software and hardware development. Or he may graduate to a complete Formulator Mark III with intelligent front panel, power supply, and accessories or to the top of the line Formulator Mark IIIFD with floppy disk drives.

Three growth packages plus a selection of optional modules provide a practical method for upgrading the single-board Mark I to either the Mark II or Mark IIFD or to the maximum system configuration Mark III or Mark IIIFD. Using the growth packages, the designer can begin sophisticated system application programs at very low cost and then upgrade his development tools in relatively inexpensive steps, if he desires to do so at a later time.

The most elementary configuration, called the Formulator Mark I, includes a Processor module that contains an F8 CPU, Program Storage Unit that includes Fairbug monitor, Dynamic and Static Memory Interface circuits, 1024 bytes of random access memory, and the necessary buffers and other components for hardware development. It also includes a 13-slot card cage, an I/O cable kit, and a power cable.

The second level, the Formulator Mark II, includes all of the Mark I components plus a memory board with 16 kilobytes of RAM and the complete Formulator Operating System, designated FOS. FOS gives the user complete software development capability, including an assembler, editor, and debug package, and drivers for a teletype or the TI Silent 733 terminal.

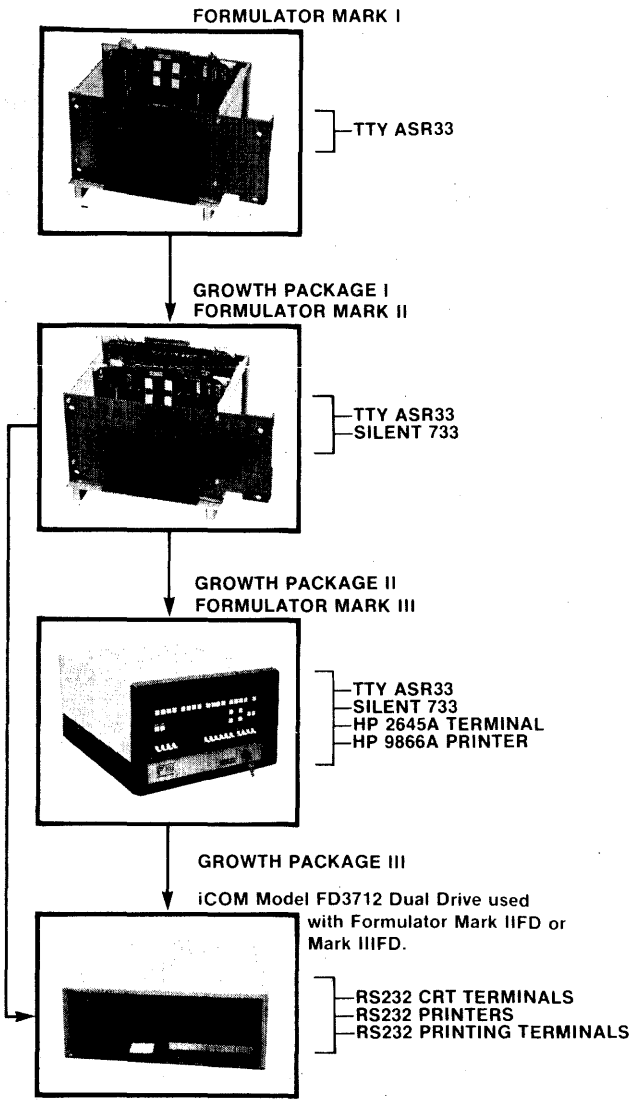
The third level, the Formulator Mark IIFD, is identical to the Mark II with the addition of interface cards and cables for an iCOM FD3712 dual-drive floppy disk system and Fairchild F8-DOS-III Floppy Disk Operating System.

The fourth level, the Formulator Mark III, includes an intelligent front panel, a serial communications module, a quad I/O module, an attractive cabinet, and a power supply. Also included are 16 kilobytes of RAM, the Formulator Processor Module, and the Formulator Operating System.

The top of the line is the Formulator Mark IIIFD. This microcomputer is identical to the Mark III except it interfaces to the iCOM dual drive floppy disk.

Three growth packages are available for Mark I, Mark II, and Mark III expansion. Growth Package I upgrades the Mark I system to the Mark II level. Growth Package II converts the Mark II to the full Mark III level. Growth Package III upgrades either the Mark II or Mark III to the Mark IIFD or the Mark IIIFD floppy disk configurations.

Other boards are available as options for all five Formulator configurations to increase the flexibility of the units by adding to their capabilities. These include 4-kilobyte RAM, 4-kilobyte PROM, and 16-kilobyte RAM boards, as well as and I/O light board, a communications board with UART, a parallel-byte board for peripheral interface, and a PROM programmer.



FORMULATOR GROWTH PATHS

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FORMULATOR MARK I

The first member of the Formulator family, the Formulator Mark I, is a basic microcomputer development tool providing the hardware necessary to build F8 or F3870 prototype systems. Included in the basic system is the Formulator Processor Module with the F8 CPU, Static Memory Interface, Dynamic Memory Interface, and Program Storage Unit devices. The Fairbug debug program, a 1K-byte monitor debug package, is included in the Program Storage Unit on the Processor Module. Fairbug provides the Mark I with sufficient debug capability to load a program, examine registers, monitor and alter memory locations, store a program on an external file, and generate a tape suitable for burning PROM memory devices. The Mark I also comes equipped with a 13-slot card cage and motherboard for attaching the modular Formulator printed circuit boards. Three slots are wired for the console control modules and one is dedicated to the Processor Module. The other nine connectors are general purpose slots which can accept additional Formulator modules for system expansion. Cables and documentation are also included in the F8 Formulator Mark I system, including a peripheral interface cable which can connect the Mark I to a Teletype ASR33 or TI Silent 733 for external communication.

Hardware

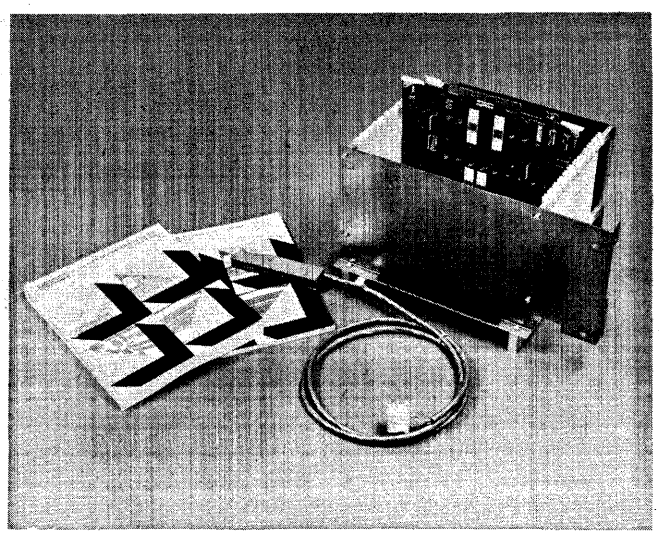
Formulator Processor Module
Formulator Card Cage and Motherboard
Processor Module to Peripheral Cable
Power Cable
Cable Kit

Software

Fairbug Debug Program

Documentation

Formulator User's Guide
Formulator Hardware Reference Manual
Formulator Mark I Systems Coverage Manual
Formulator Utilities Manual



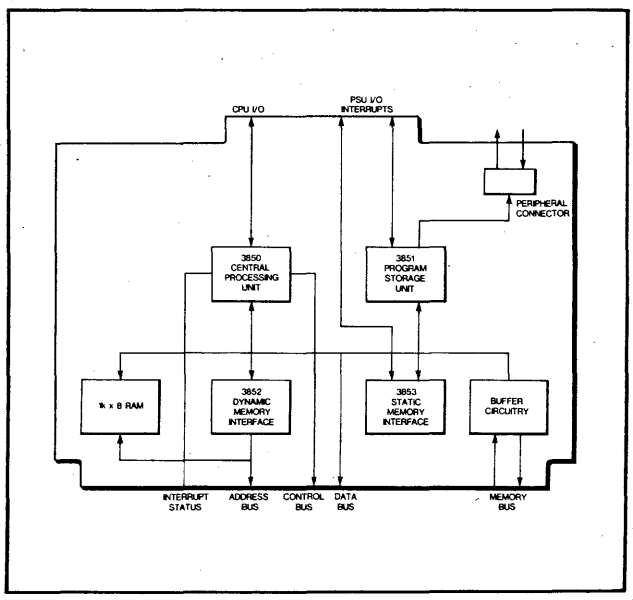
THE FORMULATOR PROCESSOR MODULE

The Formulator Processor Module is the heart of the Formulator family of development systems. As illustrated in the block diagram below, the 10½" × 7½" Processor Module contains a Central Processor Unit (F3850 CPU), a Program Storage Unit (F3851A PSU) with the Fairbug monitor, a Static Memory Interface circuit (F3853 SMI), a Dynamic Memory Interface circuit (F3852 DMI), a 1K-byte RAM memory, and a peripheral interface circuit. Also included is the circuitry necessary to drive the Formulator bus for easy expansion of system functions. The 32 bidirectional I/O lines are brought out to the top edge connector; bus signals are brought to a connector on the bottom of the board. The board connector plugs into the Formulator motherboard where the signals are bussed to twelve other sockets. The peripheral interface signals are brought out to a special connector mounted on the Processor Module. They include both a 20 mA current loop and an RS232 interface circuit.

Two interrupt levels are available on the Formulator Processor Module, one from the F3851A PSU and the other from the F3853 SMI. The on-board F3852 DMI allows dynamic memory refresh and direct memory access functions to be incorporated into expanded memory systems.

Switches on the Processor Module change the page address of the 1K-byte RAM memory. Additional switches are provided to change the port addresses of the PSU circuit, enable and disable the Fairbug program, select the clock mode (LC, crystal, or external), enable the interrupt priority, and select serial interface devices (RS232 or current loop).

The Fairbug program, located in the F3851A PSU communicates with an ASCII serial device, reads data from a parallel paper tape reader, and punches tape. The Fairbug program also performs a debug function allowing users to examine and alter internal registers and memory.



PROCESSOR MODULE

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FORMULATOR MARK II

The second member is the Formulator Mark II. This unit is a low cost microcomputer software and hardware development tool. It includes the basic hardware required to develop a system, as well as the necessary software tools to develop F8 and F3870 code. The Mark II consists of all the components of the Mark I, namely the Processor Module, card cage and motherboard, cable kit, and the Fairbug debug program, as well as an additional 16K-byte RAM module. Also a part of the Mark II is the Formulator Operating System, including the editor, relocating assembler, and debug package to allow the generation of the source codes and to create and check out the object codes. Peripheral interfaces are also available to connect the Mark II to a TI Silent 733 or Teletype ASR33.

Hardware

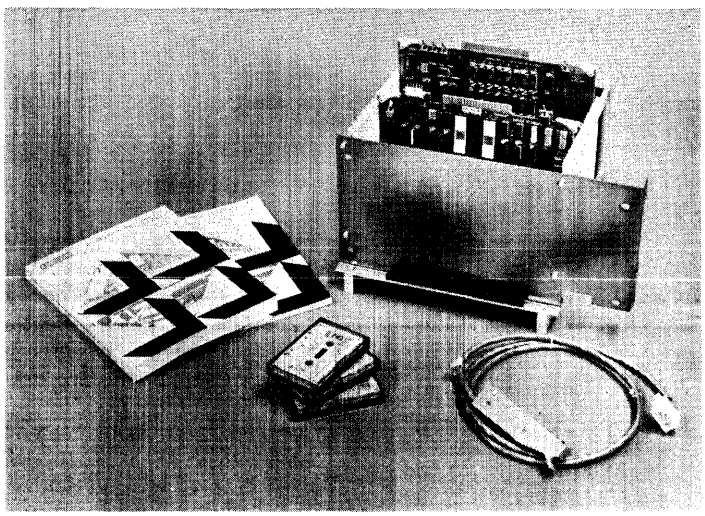
Formulator Processor Module
16K-Byte RAM Module
Formulator Card Cage and Motherboard
Processor Module to Peripheral Cable
Power Cable
Cable Kit

Software

Formulator Operating System

Documentation

Formulator User's Guide
Formulator Hardware Reference Manual
Formulator Mark II Systems Coverage Manual
Formulator Utilities Manual



MARK II FORMULATOR OPERATING SYSTEM—FOS

The software for the Formulator products is specifically designed to assist engineers and programmers during the development phase of a microcomputer-based system. Designated the Formulator Operating System (FOS), this software package consists of a monitor, an editor, an assembler, a linking loader, a debug package, and several utility programs.

The editor assists the user in the creation of a source file, which the assembler then converts into an object file ready for loading into the system. This object file may, at the option of the user, be a relocatable file. If several such relocatable object files exist, they may be combined by the linking loader and assigned absolute addresses at loading.

The debug portion of the Mark II FOS allows users to test for fast and efficient program testing, for setting software breakpoints, and for examining and altering memory, registers, and I/O ports.

Unlike other development systems with limited storage capability, the Formulator has enough memory so that the editor, relocating assembler, and debug packages are simultaneously resident, with transfer from one to the other controlled by the monitor. Thus, a program may be created, edited, assembled, and debugged without ever having to reload the system software, since the user may switch from the editor to the assembler to the debug program directly from the monitor.

The Formulator software also includes utility programs which perform specific functions. One, for instance, generates a file for producing a ROM code. Another creates a file needed by a PROM programmer. These utility programs are loaded into the system under the control of the monitor.

The combined effect of the interrelated portions of the Formulator Operating System is the rapid generation and checkout of F8 and F3870 microcomputer-based systems. These programs greatly simplify the effort required to develop and alter the end user software, making it easy to design and debug a system breadboard, easy in terms of reduced time and manpower.

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FORMULATOR MARK IIFD

The third member is the Formulator Mark IIFD, a floppy-disk based low-cost microcomputer software and hardware development tool. It includes the basic hardware required to develop a system, as well as the necessary software tools to develop F8 and F3870 code. The Mark IIFD consists of all the components of the Mark I, namely the Processor Module, card cage and motherboard, cable kit, and the Fairbug debug program, as well as an additional 16K-byte RAM Module. The F8-DOS-III is also a part of the Mark IIFD. It includes a floppy-disk file manager, editor, relocating assembler, and debug package to generate the source codes and to create and check out the object codes. The Mark IIFD can communicate with teletype ASR33 and other standard RS232 CRT or printing terminals.

Hardware

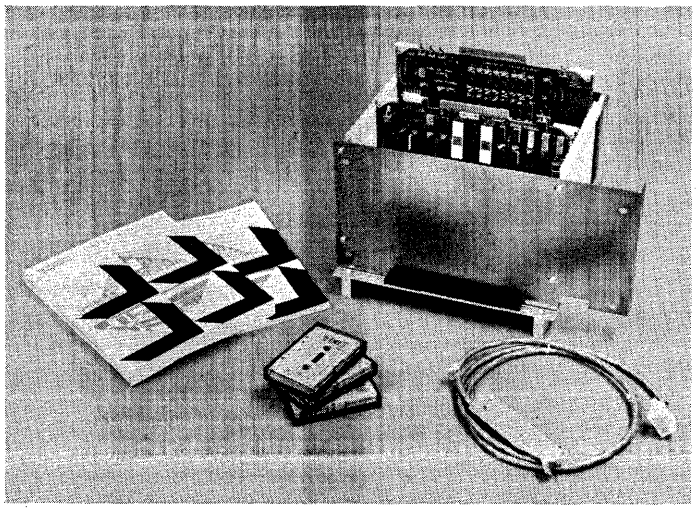
Parallel Interface Module Prom Boot Loader Module
Formulator Processor Module
16K-Byte RAM Module
Formulator Card Cage and Motherboard
Processor Module to Peripheral Cable
Power Cable
Cable Kit

Software

F8-DOS-III Floppy Disk Operating System

Documentation

Formulator User's Guide
Formulator Hardware Reference Manual
Formulator Mark II Systems Coverage Manual
Formulator Utilities Manual



MARK IIFD FLOPPY-DISK OPERATING SYSTEM — F8-DOS-III

The software for the Formulator products is specifically designed to assist engineers and programmers during the development phase of a microcomputer-based system. Designated the F8 DOS-III, this software package consists of a floppy-disk monitor, an editor, a relocating assembler, a linking loader, a debug package, and utility programs.

The disk monitor provides all of the necessary commands for fast and efficient file management during the creation, editing, assembly, and debugging of applications programs.

The editor assists the user in the creation of a source file, which the assembler then converts into an object file ready for loading into the system. This object file may, at the option of the user, be a relocatable file. If several such relocatable object files exist, they may be combined by the linking loader and assigned absolute addresses at loading.

The debug portion of the F8-DOS-III provides for fast and efficient program testing. Under software control, the user can set software breakpoints, and examine and alter memory, registers, and I/O ports.

Unlike development systems with limited storage capability, the Formulator Mark IIFD has enough memory so that the editor, assembler, and debug packages are resident as needed with transfer from one to the other controlled by the disk monitor. Thus, a program may be created, edited, assembled, and debugged without ever having to externally reload the system software, since the user may switch from the editor to the assembler to the debug program directly from the disk monitor.

The Formulator software also includes utility programs which perform specific functions. One, for instance, generates a file for producing a ROM code; another creates a file needed by a PROM programmer. These utility programs are loaded into the system under the control of the disk monitor.

The combined effect of the interrelated portions of the F8 DOS-III is the rapid generation and checkout of F8 and F3870 microcomputer-based systems. These programs greatly simplify the effort required to develop and alter the end-user software, making it easy to design and debug a system breadboard, easy in terms of reduced time and manpower.

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FORMULATOR MARK III

The fourth level of microprocessor development equipment is the Formulator Mark III, offering all of the design assistance required to develop F8 or F3970 based systems. The combination of hardware, software, and firmware offered by the Mark III assists the designer from the generation of source programs through the development of a prototype system. The Mark III is a modular microcomputer that accommodates a variety of memory, input/output, and communication configurations to form a new and powerful development system. It contains all of the components of the Mark II—the Processor Module, card cage and motherboard, cable kit, the Fairbug debug program, 16K bytes of RAM, and the Formulator Operating System. In addition, the Mark III includes a Quad I/O Module with four I/O ports and two interrupts, a Communications Module with an on-board UART, a universal breadboard for building user hardware configurations, an extender module, and an intelligent operator's panel. Power supplies for the Mark III may be either 100 volts, 115 volts, or 220 volts at 50/60 Hz. Peripheral interfaces are available to connect the Mark III with a TI Silent 733, a Teletype ASR33, or an HP 2645A Mini-Data Station.

Hardware

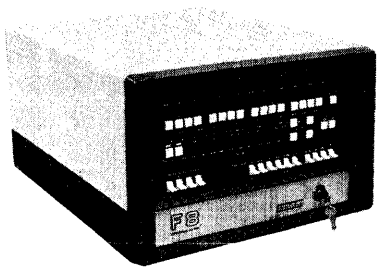
Formulator Mainframe
Designer's Console with Firmware
Formulator Processor Module
16K-Byte RAM Module
Quad I/O Port Module
Communications Module
Universal Breadboard
Extender Module
Cable Kit
User I/O Cable Assembly
Communications Module to Peripheral Cable

Software

Fairbug Debug Program
Formulator Operating System

Documentation

Formulator User's Guide
Formulator Hardware Reference Manual
Formulator Mark III Systems Coverage Manual
Formulator Utilities Manual



INTELLIGENT OPERATOR'S PANEL

Perhaps the most unique feature of the Mark III Formulator is the intelligent operator's panel, an array of lights and switches designed to give the user access to vital registers and memory locations within the microcomputer; thus enabling an important interaction between the user and the system hardware and software.

The benefits of having a firmware controlled front panel are extensive. In addition to performing the normal front panel operations, such as examining and loading the contents of memory, the user's console can also perform some very complicated functions. Chief among these are the front panel's relocatable initial program load capability, its test function, and the real time hardware breakpoint feature.

The self test function is initiated by the user by merely depressing a single switch on the front panel. The console then begins to check the electronics in the Formulator. When an error condition is detected, the LED indicators on the display indicate the type of error and its location.

Another feature of the front panel is its ability, under operator control, to set hardware breakpoints and to vary the number of times a memory location may be accessed before the break-in program execution occurs. This aids the user in performing fast, efficient debugging of his software.

MARK III FORMULATOR OPERATING SYSTEM

Like the Mark II Formulator Operating System, the Mark III FOS consists of a monitor, an editor, an assembler, a linking loader, a debug package, and several utility programs. In addition to the functions performed by each of these portions of the FOS in a Mark II system, the Mark III FOS includes the capability to set hardware breakpoints. It also contains a trace feature in the debug package which lets the user turn tracepoints on and off during the debug operation.

Two identical versions of the Formulator Operating System are available with the Formulator Mark III. One operates in the lower portion of memory and another operates in upper memory. The Low Memory Operating System resides in memory locations 1000 to 3FFF (Hex). Most of the lower 4K bytes of memory is reserved for user programs. The High Memory Operating System occupies locations with the hexadecimal addresses D000 to FFFF and uses the portion of memory from LC000 to D000 to store the symbol table. With this system, the user has up to 48K bytes of continuous memory addresses available, eliminating the need for splitting programs larger than 4K bytes.

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FORMULATOR MARK IIIFD

The top of the line in microprocessor development equipment is the floppy-disk-based Formulator Mark IIIFD, offering all of the design assistance required to develop F8 or F3870 based systems. The combination of hardware, software, and firmware offered by the Mark IIIFD assists the designer from the generation of source programs through the development of a prototype system. The Mark IIIFD is a modular microcomputer that accommodates a variety of memory, input/output, and communication configurations to form a new and powerful development system. It contains all of the components of the Mark IIFD, the Processor Module, card cage and motherboard, cable kit, the Fairbug debug program, parallel interface, PROM boot loader, 16K bytes of RAM, and the F8-DOS-III disk operating system. In addition, the Mark IIIFD includes a quad I/O module with four I/O ports and two interrupts, a communications module with an on-board UART, a universal breadboard for building user hardware configurations, an extender module, and an intelligent operator's panel. Power supplies for the Mark IIIFD may be either 100 volts, 115 volts or 220 volts at 50/60 Hz. The Mark IIIFD can communicate with teletype ASR33 or other standard RS232 glass or printing terminals.

Hardware

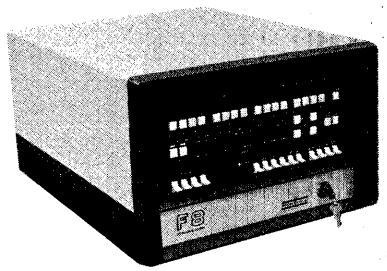
- Formulator Mainframe
- Designer's Console with Firmware
- Formulator Processor Module
- Parallel Interface Module
- PROM Boot Loader Module
- 16K-Byte RAM Module
- Quad I/O Port Module
- Communications Module
- Universal Breadboard
- Extender Module
- Cable Kit
- User I/O Cable Assembly
- Communications Module to Peripheral Cable

Software

- F8-DOS-III Floppy Disk Operating System

Documentation

- Formulator User's Guide
- Formulator Hardware Reference Manual
- Formulator Mark III Systems Coverage
- Formulator Utilities Manual



INTELLIGENT OPERATOR'S PANEL

A unique feature of the Mark IIIFD Formulator is the intelligent operator's panel, an array of lights and switches designed to give the user access to vital registers and memory locations within the microcomputer, thus enabling an important interaction between the user and the system hardware and software. The front panel functions of the Mark IIIFD are identical to those described in the Mark III section.

MARK IIIFD FLOPPY DISK OPERATING SYSTEM

The software for the Formulator products is specifically designed to assist engineers and programmers during the development phase of a microcomputer-based system. Designated the F8-DOS-III, this software package consists of a floppy disk monitor, an editor, a relocating assembler, a linking loader, a debug package, and utility programs. The disk monitor provides all of the necessary commands for fast and efficient file management during the creation, editing, assembly, and debugging of applications programs.

The editor assists the user in the creation of a source file, which the assembler then converts into an object file ready for loading into the system. This object file may, at the option of the user, be a relocatable file. If several such relocatable files exist, they may be combined by the linking loader and assigned absolute addresses at loading.

The debug portion of the Mark III F8-DOS-III provides for fast and efficient testing. Under Software Control, the user can set software and hardware breakpoints, and examine and alter memory, registers, and I/O ports.

Unlike development systems with limited storage capability, the Formulator Mark IIIFD has enough memory so that the editor, assembler, and debug packages are resident as needed with transfer from one to the other controlled by the disk monitor. Thus, a program may be created, edited, assembled, and debugged without ever having to externally reload the system software, since the user may switch from the editor to the assembler to the debug program directly from the disk monitor.

The Formulator software also includes utility programs which perform specific functions. One, for instance, generates a file for producing a ROM code; another creates a file needed by a PROM programmer. These utility programs are loaded into the system under the control of the disk monitor.

The combined effect of the interrelated portions of the Formulator F8-DOS-III is the rapid generation and checkout of F8 and F3870 microcomputer-based systems. These programs greatly simplify the effort required to develop and alter the end-user software, making it easy to design and debug a system breadboard, easy in terms of reduced time and manpower.

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F8-DOS-III DESCRIPTION

The Formulator F8-DOS-III operating system provides floppy-disk bulk storage capability for Fairchild's Formulator Mark IIFD and Mark IIIFD F8 microcomputers when used with up to four plug-compatible iCOM® series FD 360, FD3700 and Frugal Floppies™ providing for over one megabyte of total storage capacity.

F8-DOS-III provides a powerful and complete development software package with batch operation, linking loader, and relocating assembler, and provides an easy to use, reliable, fast and extremely efficient capability for auxiliary program and data storage during F8 and F3870 software development or in end-user applications.

iCOM® Advertised FD3700 Series Features	F8-DOS-III SUMMARY			
	Disk Monitor	**Editor**	**Relocating Assembler**	**Real-Time Debugger**
Fully IBM 3740 media and format compatible	Assemble (Relocating)	Move Line	No-List Option	Symbolic Debugging
Full formatter and controller built-in	Load (Linking)	Copy Line	No-Object Option	Set Up to 8 Breakpoint
Full sector Read/Write buffers allow	List Directory	Bottom	Error Messages	Clear Breakpoint
asynchronous or DMA data transfer	Print File	Change	Invalid Label	Clear All Breakpoints
Drive and diskette Write Protect capability	Rename File	Delete	Duplicate Label	Continue Execution
Positive latching door mechanism	Create File	File	Invalid Op Code	Go To Location
Up to 4 drives with no software or hardware	Delete File	Find String	Operand Error	Return to Monitor
modifications	Copy File	Insert	Syntax Error	Single Step
MTBF in excess of 2300 hours (FD 3712 dual	Copy Disk	Locate String	Undefined Symbol	Trace On Long
drive)	GenMod (Created	Next	Expression Storage	Trace on Short
Plug-in convenience allows MTTR of 18	Linked File)	Replace	Overflow	Trace Off
minutes	Edit Mode	Tab	Relocatability	Display Memory
Front panel LED status indicators	Load (Absolute)	Top	Error	Display Register
LED drive select indicators	DeBug Mode	Type	Pseudo Operand	Display Port
Fully retracting head and pressure pad for	Assign Virtual I/O	Up	Error	Store Memory
maximum diskette life	Burn PROM		Cross Reference	Store Register
50 pin flat ribbon cable with 3M interface	Convert			Store Port
connector—FD 360 compatible	ROM Dump			

FORMULATOR GROWTH PACKAGES

The Mark I, Mark II, and Mark III Formulator systems previously described are all upwards compatible. The Mark I can be expanded to become a Mark II; likewise, the Mark II may be developed into a Mark III. In addition, a Mark II can be expanded to a Mark IIFD and a Mark III into a Mark IIIFD. This means that a microprocessor system designer may enter the microcomputer design at a level which best matches the needs at hand—amount of available money, time, microprocessor experience—and be able to increase the Formulator's capabilities as his needs grow. Three growth packages are available to Formulator product owners. Growth Package 1 converts a Mark I system to a Mark II; Growth Package 2 extends the capabilities of the Mark II into the Formulator Mark III, and Growth Package 3 extends a Mark II or III into a Mark IIFD or IIIFD.

Growth Package I
- 16K-Byte RAM Module
- Mark II Formulator Operating System

Growth Package 2
- Quad I/O Module
- Communications Module
- Power Supply
- Fan
- Console Control Modules
- Internal Cable Wiring
- Universal Breadboard
- Extender Module
- I/O Cable Assembly
- Communications Module to Peripheral Cable
- Mark III Formulator Operating System

Growth Package 3
- Parallel Interface Module
- PROM Boot Loader Module
- F8-DOS-III System Diskette

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PERIPHERAL OPTIONS

The Formulator Mark II systems interface with either a Teletype ASR33 with the auto read/auto punch option or a TI Silent 733 ASR with the ADC option. The teletype terminal provides a paper tape based system, while the 733 allows file storage on magnetic tape cassettes. To decrease load times, a Remex high speed paper-tape reader (or equivalent) may be used with either peripheral unit.

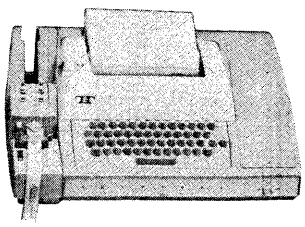
The Formulator Mark III provides an interface for the HP Mini-Data Station as well. This high speed unit combines the efficiency of the magnetic tape cartridges with an intelligent terminal and thermal line printer to allow the rapid development and debugging of application programs.

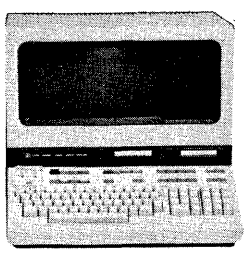
The Formulator Mark IIFD and IIIFD systems interface with any standard RS232 glass terminal and printer or printing terminal to offer maximum peripheral cost/speed flexibility.

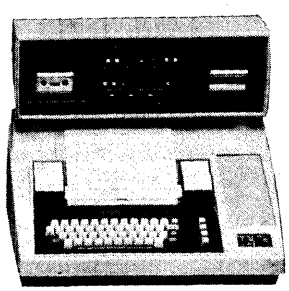
HP MINI-DATA STATION

The HP 2645A Mini-Data Station features an interactive CRT Terminal with high resolution display and a fully integrated mass storage capability, making it easy to use both on- and off-line. It uses 2½″ × 3¼″ × ½″ magnetic cartridges which store up to 110 kilobytes of formatted data. The Mini-Data Station has two mini cartridge drives, allowing for a total of 220 kilobytes of data storage on matnetic tape. Thus, all files—both operating system and user files—are resident on the magnetic tape. Loading and storing files is accomplished by reading and writing onto the cartridge. The user's time is decreased and efficiency increased when the magnetic tapes are used.

The 2645 Mini-Data Station comes equipped with three data cartridges, an Owner's Manual, and an Installation and Service Manual.









HP 9866A PRINTER SUBSTATION

The HP 9866A line printer is a moderately priced, high performance companion to the HP 2645A Mini-Data Station, providing a permanent record of the contents of the Mini-Data Station display and memory for future use. The printer operates at up to 240 lines per minute with a maximum line width of 80 characters. The character set consists of 64 alphanumeric characters generated by a 5 × 7 dot matrix. Since a thermal printing mechanism is used to make this printer quiet enough for normal office use, thermal sensitive paper is required. This paper is 8¾ inches wide and available in 250 foot rolls.

The 9866A thermal printer comes equipped with two rolls of paper, a power cord, an interface card and cable, and an Instruction Manual.

iCOM F3712 DUAL FLOPPY DISK

The iCom FD3700 Series Floppy Disk System for microcomputers continues the tradition fo the iCOM FD360. The FD3700 brings to the OEM, and to the development lab, proven reliability and popular features, while incorporating advanced styling and new convenience items.

The iCOM FD3700 Series features the following:

- Fully IBM 3740 media and format compatible
- Full formatter and controller built in
- Full sector read/write buffers allow asynchronous or DMA data transfer
- Drive and diskette write-protect capability
- Positive latching door mechanism
- Up to four drives with no software or hardware modifications
- MTBF in excess of 2300 hours (FD3712 dual drive)
- Plug-in convenience allows MTTR of 18 minutes
- Front panel LED status indicators
- LED drive select indicators
- Fully retracting head and pressure pad for maximum diskette life
- 50-pin flat ribbon cable with 3M interface connector—FD360 compatible

iCOM Performance features are as follows:

- Disk speed 360 RPM ± 1.5%
- 10 ms track-to-track access time
- 40 ms head load time
- 5 ms sector read/write time
- 83 ms average latency time
- 700 ms automatic head unload time
- 1 ms interrecord time

Power Requirements Are:

110-125 V_{ac}, 60 Hz, 200 W max
Optional 220-240 V_{ac}, 50 Hz, 200 W is available

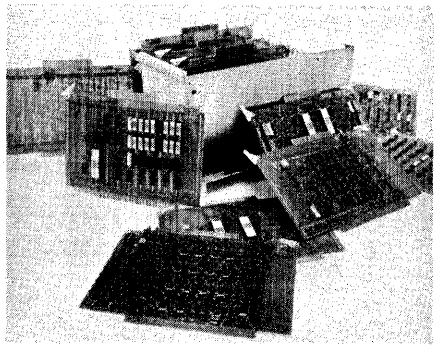
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OPTIONAL FORMULATOR MODULES

Expansion of the Formulator microcomputers need not occur along the path indicated by the growth packages. Optional Formulator modules are available to expand RAM, PROM I/O, and communications, so the user can develop a custom system which is perfectly suited to his specific needs. These optional modules may be attached to the Formulator via the 13 card slots in the motherboard. The first three slots are dedicated to front panel operations of the Mark III. Another slot is reserved for the Processor Module. The remaining nine slots are linked on a common bus whose signals are compatible with the modules themselves. Additional system functions may be easily added to any Formulator system by simply plugging in one of the modules. Thus, the initial Formulator investment is preserved. Nothing needs to be discarded as demands upon the system increase. Unless otherwise noted, all of the following optional modules are available to update any Mark I, Mark II, Mark IIFD, Mark III, or Mark IIIFD system to meet expanded requirements.

Optional Modules

- 4K-Byte RAM Module
- 16K-Byte RAM Module
- Quad I/O Port Module
- 4K-Byte PROM Module
- Communications Module
- Byte Parallel Interface Module
- ROM Simulation Module
- Universal Breadboard
- Extender Module
- I/O Light Display Board



4K-BYTE RAM MODULE

The 4K-Byte Ram Module simplifies memory expansion in the Formulator Development Systems. Fully compatible with all Formulator bus signals, this board adds 4096 bytes of random access memory (using 2102 type static RAMs) to a system. Switches mounted on the printed circuit board allow the user to select the upper four address bits, so multiple memory modules may be used in a system. A write-protect switch puts the memory in a read-only mode at the user's discretion. Board dimensions are 10½" × 7½".

16K-BYTE RAM MODULE

The 16K-Byte RAM Module provides additional modularly expandable memory for the Formulator Development System. Fully compatible with all Formulator bus signals, this board adds 16 kilobytes of random access memory (4K N-MOS Dynamic RAM) to a system. Switches mounted on the printed circuit board allow the user to select the upper two address bits, so multiple memory modules may be used in a system. Four write-protect switches put the memory in a 'read only' mode at the user's discretion. The refresh of the dynamic memory is controlled by the F3852 Dynamic Memory Interface circuit mounted on the Processor Module. The refresh cycles are performed during unused data bus periods, and do not interfere with normal system timing. The board dimensions are 10½" × 7½".

4K-BYTE PROM MODULE

Additional memory expansion in the Formulator systems may be easily performed with the use of the 4K-Byte PROM Module. This board adds 4096 bytes of nonvolatile memory storage capability. It provides 16 sockets for the Fairchild 93446 TTL fuseable link 512 × 4-bit PROMs configured in a 4-kilobyte array. Four switches mounted on the printed circuit board allow the memory page to be switch selectable. All data bus and control bus signals are compatible with the Formulator system, so the board plus directly into the Formulator motherboard. The 93446 PROM devices may be programmed by the Formulator PROM Programmer. The board dimensions are 10½" × 7½".

QUAD I/O PORT MODULE

The Quad I/O Port Module makes expanding the Formulator I/O capability an easy task. This board uses existing F8 I/O ports, so actual F8 signal levels are brought out to the edge connector on the top of the module. This module has two F8 circuits, each with two I/O ports, one interrupt level, and one programmable timer. Thus, a total of four ports (32 bits), two interrupt levels, and two timers are available to the user. Switches mounted on the card allow the user to select the I/O port addresses and the interrupt vector addresses for each F8 circuit. Thus, since each board may use different I/O ports, multiple boards may be used in a system. The board dimensions are 10½" × 7½".

COMMUNICATIONS MODULE

The Communications Module provides the electrical interface for any one of three types of serial peripheral devices, a standard teletype 20 mA current loop, RS-232 interface, or a TTL compatible device. An on board UART (Universal Asynchronous Receiver Transmitter) is used to perform the conversion between the 8-bit parallel microcomputer data and the serial signal, thus permitting high speed data transfer. Thirteen baud rates, ranging from 50 to 9600 baud, can be set from switches mounted on the card. A crystal is used to ensure accurate timing. The UART-microcomputer interface is maintained via two F8 I/O ports, also located on the printed circuit board. The F8 timer and interrupt logic are also available to the user, with the interrupt address vector and F8 I/O port numbers switch selectable. Board dimensions are 10½" × 7½".

I/O LIGHT DISPLAY BOARD

The I/O Light Display Board monitors the status of the F8 I/O signals of either the Formulator Processor Module or the

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Formulator Quad I/O Module. Mounted on the printed circuit cards are red LEDs, grouped in two rows of twenty, allowing up to four I/O ports plus power supplies to be viewed simultaneously. On-board drivers provide sufficient current levels to drive the LEDs. Additional lights on the board show the status of the external interrupts. The board dimensions are 10½" × 4½".

BYTE PARALLEL INTERFACE MODULE

The Byte Parallel Interface Module interfaces the Formulator system to external devices in a parallel format. This 10½" × 7½" module creates a data bus and a control bus for passing information to and from the system. The bidirectional data bus can be used for either 8- or 16-bit parallel words. The 8-bit control bus synchronizes data transfer to and from the Formulator system. The F8 I/O ports. One level of F8 interrupt logic and one F8 interval timer are also available to the user. On-board switches select the F8 interrupt address vector and the F8 I/O port addresses. The signal levels for the device interface are given below.

Receive

V_{IL}	I_{IL}	V_{IH}	I_{IH}	V_{CC}
0.4V	−0.2mA	5.25V	25 μA	5.25V

Drive

V_{OL}	I_{OL}	V_{OH}	I_{OH}	V_{CC}
0.5V	48mA	2.4V	−10mA	4.75V

ROM Simulation Module

The ROM Simulation Module allows the user to interface the F3851A and F3856 Program Storage Units to the Formulator systems. Two of these 40-pin devices may be inserted in each ROM Simulation Module, creating an excellent environment for checking out ROM codes stored on the PSUs.

EXTENDER MODULE

During the checkout of the user's own breadboard systems, the Formulator Extender Module can be used to facilitate access to the user's hardware configuration contained on the universal breadboard. The 10½" × 7½" extender module plugs directly into the Formulator motherboard, and the module to be examined attaches to the 100-pin connector on the top edge of the extender card. Thus, the user's module is elevated above the other modules in the Formulator card cage for easy access.

UNIVERSAL BREADBOARD

The universal breadboard is an empty Formulator module board which can aid in the development of the user's own breadboards. It is a 10½" × 7½" Formulator motherboard-compatible module which is predrilled to accept standard 14, 16, 18, 22, 24, and 40-pin dual inline packages. It will accomodate forty-four 16-pin packages. With the universal breadboard, the Formulator user may design his own breadboard configuration of non-microprocessor circuits while in constant contact with the microprocessor development tools of the Formulator.

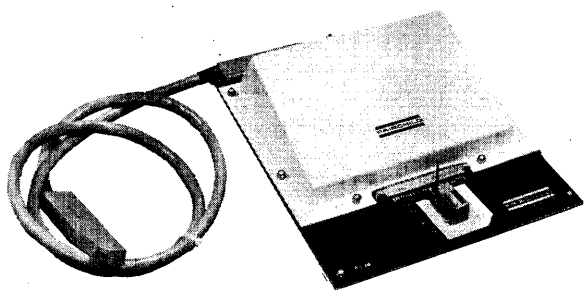
PROM PROGRAMMER

The ability to easily program permanent memory devices is essential to any microprocessor design. The Formulator PROM Programmer connects to a Quad I/O Module within either a Formulator Mark II or a Formulator Mark III, permitting the programming of any of the following fuseable link or ultraviolet light eraseable PROMs from a pattern stored in the Formulator memory.

The 11" × 12" × 4" PROM Programmer is driven by a utility program contained within the Formulator Operating System and features a simple, easy to use command set. The commands, entered into the PROM Programmer from the Formulator peripheral via the keyboard, allow the user to transfer data from a PROM to memory, burn a PROM, verify a PROM pattern, manually enter a single byte of data, and display PROM locations using the system software. The programming idiosyncrasies of each PROM are contained in software look-up tables to relieve the user of intricate repetitious set-up. The procedure is simply to identify the PROM type (like 93448) and the PROM parameter look-up table is automatically invoked, defining such things as number of words, word bit length, burn time, wait time, retry conditions, etc. The programming is convenient enough to allow the PROM Programmer to be used in a production environment.

Included in the basic system are two socket boards, one for the Fairchild 93436/93446 PROMs and one for the 93438/93448 PROMs. Socket boards for the ultraviolet eraseable devices are also available. A cable to the Quad I/O Module and a power cord are also included in the basic unit.

Fairchild Fusible Link PROMS	Ultraviolet Eraseable PROMs
93436 (512 × 4)	2704 (512 × 8)
93446 (512 × 4)	2708 (1024 × 8)
93438 (512 × 8)	
93448 (512 × 8)	



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F3870 DEVELOPMENT SUPPORT

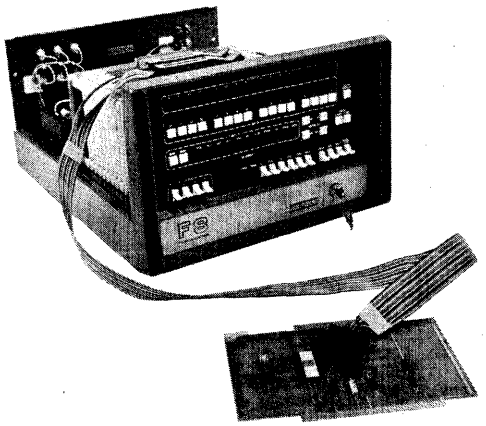
The F8 Formulator family of development equipment also supports the F3870, the one-chip microcomputer manufactured by Fairchild. The Formulator Operating System, utility program, and the Fairbug monitor are completely compatible with the F3870, since it shares the same instruction set with the Formulator. A Simulation (Quad I/O) Module and an In-Circuit Emulation (ICE) cable are available to extend the Formulator features to the user's prototype or production breadboard. This creates a powerful design tool for creating the user's own F3870 software. In addition, the F3870 Emulator, a single stand-alone module for emulating the final F3870 software in PROMs, is available for building prototype systems.

F3870 STIMULATION

The non-microprocessor elements of the user's hardware configuration can be assembled on a breadboard and connected to Mark I, II, IIFD, III or IIIFD via the ICE cable plugged into a 40-pin socket on the user's board. The cable connector on the Processor Module in the Formulator provides I/O ports 0 and 1, while the Simulation (Quad I/O) Module provides I/O ports 4 and 5. This system provides real-world simulation of the user's components in their actual environment with the vital microprocessor signals, including the complete software debugging features of the Formulator, cabled to the external breadboard.

F3870 EMULATOR

After F3870 ROM codes are frozen, a smaller, easier-to-handle and less expensive tool is required. To accomplish this design-in task, Fairchild has developed the F3870 Emulator. The F3870 Emulator contains sockets for two 2708s or two 2716 EROMs in place of the F3870 on-chip ROM so ROM codes can be verified and easily changed. The F3870 Emulator plugs directly into the F3870 40-pin socket in the production prototype using a short Emulator cable. The printed circuit module is approximately 5″ by 7 ″.

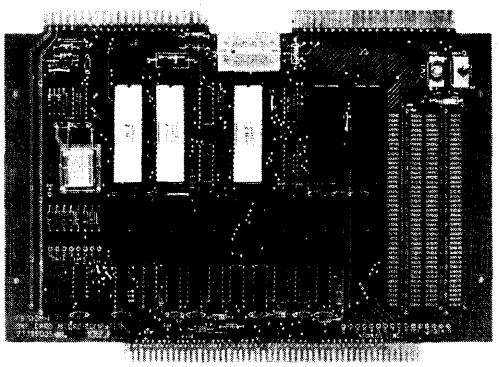


OCM-1 ONE-CARD MICROCOMPUTER

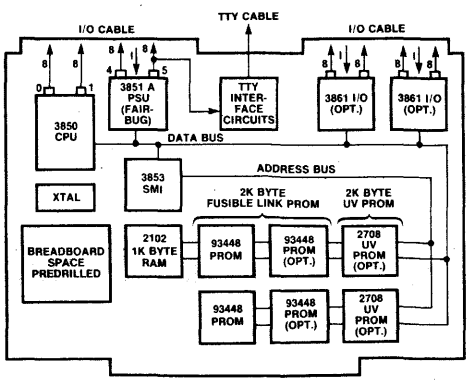
The OCM-1 is a complete microcomputer system contained on a single printed circuit board and offering the following features:

- 64-byte scratch pad memory
- 1K-byte RAM
- 8K-byte ROM (1K supplied, sockets provided for balance)
- 4K-byte EPROM (sockets provided)
- 4K-byte PROM (sockets provided)
- Up to four programmable timers
- Up to four programmable interrupts
- RS232 interface (current loop optional)
- 2 MHz clock
- Self-contained Fairbug teletype operating system
- Up to 64 individually programmable, bidirectional, latched I/O lines.

The unit is based on the F8 microcomputer and is fully supported by the Formulator family of program development aids. In addition, the OCM-1 contains a built-in teletype operating system, called Fairbug I, contained in the F3851A Program Storage Unit. Using an OCM-1-to-TTY cable assembly, the board can be directly coupled to a teletype or RS232 terminal to display or alter memory location, to load and punch paper tape, or to make entries from the keyboard or by program instruction. An alternative built-in operating system, K-D Bug, contained in the F3856A PSU is also available. It provides all of the Fairbug I functions plus a resident monitor to facilitate operation with a low-cost calculator-style keyboard and LED display. A Fairbug user's guide is provided with the OCM-1. The K-D Bug should be ordered as a separate item.



OCM-1 Module



OCM-1 Block Diagram

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The OCM-1 processor section includes the 3850 Central Processing Unit, the F3853 Static Memory Interface, a 2 MHz clock, and reset circuitry.

The OCM-1 memory section contains the capability for the use of five different types of storage including 64 bytes of scratch pad, 1K bytes of RAM, sockets for 2K bytes of EROM (2708), sockets for 2K bytes of fusible link PROM (93448), and the Fairbug I operating system.

The I/O portion of the system is contained in the F3850 Central Processing Unit and a F3851A Program Storage Unit, each containing two 8-bit I/O ports. Two sockets are provided for inserting standard F8 PIO circuits (F3861 or F3871) or, if more ROM is required, standard PSUs (F3851 or F3856) may be inserted. In either case, four additional I/O ports are provided bringing the maximum total to eight I/O ports (64 lines). Only single-byte instructions are required to individually program these lines for either input or output functions. Latches on each line reduce external hardware cost. A circuit on the board gives the OCM-1 the capability of communicating with a teletype, RS232 device or 20mA current loop.

In its standard configuration, the OCM-1 contains two interrupts and two timers, one in the F3851A PSU and one in the F3853 SMI. Two additional interrupts and timers may be added by plugging the two additional PIOs into their sockets. A "daisy-chained" priority system determines which interrupt will be serviced if two or more requests are made simultaneously.

The OCM-1 requires three power supply voltages: +12 V @ 0.255 A, −5 V @ 0.4 A and −5 V @ 0.09 A. The −5V supply is used only for the 2708 EROM devices. All supply voltages are ± 5 % maximum.

The entire microcomputer is contained on a single board (epoxy glass with solder mask) measuring approximately 7.5 inches by 10.5 inches. It includes a 2-inch by 4-inch predrilled breadboarding area for users who want to develop unique system configurations. In addition, a Formulator-compatible 100-pin edge connector, a special connector for TTY or terminal, and two 44-pin edge connectors for F8 signals, are contained on the board. A switch to enable the Fairbug operating system is also provided. The OCM-1 is delivered completed with OCM-1 Users Manual, Fairbug Users Guide and F8 Guide to Programming.

FORMULATOR SUPPORT

In addition to the optional boards, peripherals, cables, and other accessories, the Mark I, Mark II, and Mark III Formulator systems are supported by a wide range of documentation, and an intensive training program.

FORMULATOR DOCUMENTATION

The Formulator user has access to a full range of reference and instructional manuals to aid him in his system design and programming.

F8 USER'S GUIDE

The F8 User's Guide is a detailed description of the F8 family of microprocessor devices. Microprocessor systems are discussed, with the configurations of the F8 circuits examined in depth. The User's Guide also outlines the F8 instruction set. Detailed specifications of each member of the F8 microprocessor family is given, including functional descriptions, logic diagrams, signal load levels, and timing diagrams for each circuit. Typical F8 system configurations are also presented.

GUIDE TO PROGRAMMING

The Guide to Programming is written for logic designers with little or no background in computer programming. It introduces machine and assembly language programming to the potential user of microprocessors and microcomputer systems. Introductory topics include flowcharting, memory allocation, source and object programs, and assembly language. More advanced topics include programmed /O, interrupts, programmable timers, subroutines, macros, data manipulation, and programmed direct memory access channels. Numerous examples of these programming techniques are given.

FORMULATOR USER'S GUIDE

The Formulator User's Guide fully describes the operation of the Formulator Development System. It covers the Mark I, Mark II, and Mark III hardware configurations and contains a detailed description of the Formulator software—the monitor, the editor, the assembler, and the debug program. The F8 DOS-III User's Guide is also available for Mark IIFD and Mark IIIFD systems.

FORMULATOR HARDWARE REFERENCE MANUAL

This book presents an in-depth technical description of the F8 Formulator System, its component subsystems, and options. The technical description includes general functional characteristics, theory of operation, and detailed description of interface signals.

F8 TRAINING CLASS

To help applications engineers start designing with the F8 microprocessor, Fairchild offers an intensive four-day training course. Lectures are presented dealing with F8 features, architecture, and programming. In laboratory sessions, students prepare and run small F8 programs using the Formulator development systems.

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F8 AND MICROMACHINE SERIES

Versatile . . . Efficient . . . Inexpensive

THE F8 SERIES

The ultimate goal, from design concept through development and production, was to produce the most versatile, efficient, cost-effective microprocessor system available today. To accomplish this, five stringent parameters, based on user experience with other systems, were set forth as guidelines for the F8.

- **MINIMUM PARTS COUNT**
- **COST EFFECTIVENESS**
- **SIMPLE PERIPHERAL INTERFACES**
- **EASY EXPANSION THROUGH MODULAR ARCHITECTURE**
- **SIMPLIFIED PROGRAMMING AND DEBUGGING**

How Were These Goals Met?

By . . . *unique system partioning* the system functions have been divided amont the various circuits of the F8 family to provide sophisticated modularity. As a result, it is now possible to build a minimum microprocessor system with only two devices. To this system PSU, RAM and I/O devices can be added to form medium size or memory intensive systems, with a minimum of use of external parts. And, finally, for solving complex problems, the F8 devices can be connected as subsystems into a synergistic system of independent microprocessors.

By . . . *incorporating the I/O structure on the chips* so that the majority of the peripheral devices can be directly controlled without the need for special circuits. The trick is to accommodate the characteristics of a given peripheral device in the software. The I/O hardware structure includes a programmable timer, an efficient interrupt system and bidirectional I/O ports.

THE MICROMACHINE SERIES

The Micromachine series offers a single-chip solution for the cost sensitive microprocessor controller applications. The F3870 8-bit microcomputer is the first device in this series.

The Result?

A complete family of F8 and Micromachine circuits which cover the microprocessor spectrum from the most simple to the most complex.

FAIRCHILD

464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA 94042 (415) 962-5011/TWX 910-379-6435

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Manufactured under one or more of the following U.S. Patents: 2981877, 3015048, 3025589, 3064167, 3108359, 3117260; other Patents pending.

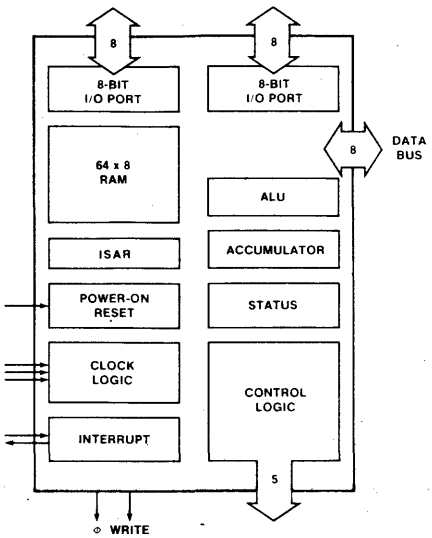
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THE F8 SERIES

3850 Central Processing Unit (CPU)

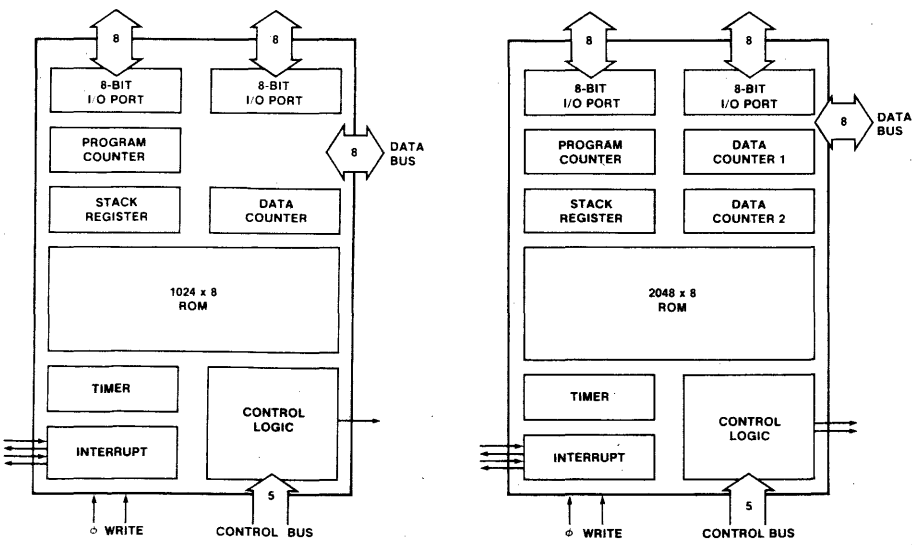
Fairchild's F8 CPU contains all of the functions needed to provide the most inexpensive solution to your design problems. The 3850 has 64 bytes of RAM, 16 I/O ports and a complete set of easy to understand instructions with both binary and decimal arithmetic operations.

3850
CPU BLOCK DIAGRAM



3851/3856 Program Storage Units (PSUs)

The 3851 PSU contains 1K of program storage and the 3856 2K. Both provide 16 bits of bi-directional I/O ports, a timer and external interrupt and a vectored, prioritized interrupt structure. Additional PSUs may be added as required and I/O expansion naturally follows. Each PSU may be considered a generalized peripheral controller.



PSU BLOCK DIAGRAM

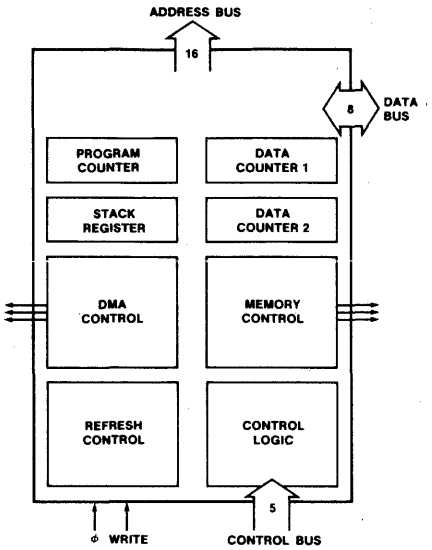
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3852/3853/3857 Memory Interface Circuits

Additional memory can be easily added to the system by using any of the three Memory Interface Circuits. Each device generates the 16 address lines and signals necessary to interface with up to 65K bytes of RAM, PROM or ROM memory and they all may be used in conjunction with any standard semiconductor memory device.

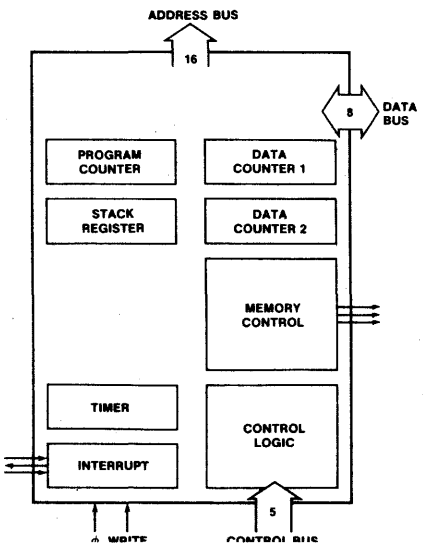
The 3852 Dynamic Memory Interface (DMI) provides memory refresh and DMA logic which run transparent to the CPU without any degradation in the system throughput time.

3852
DMI BLOCK DIAGRAM



The 3853 Static Memory Interface (SMI) provides a programmable timer and external interrupt capability with a software loadable interrupt vector address in addition to the 16 address lines and memory control logic.

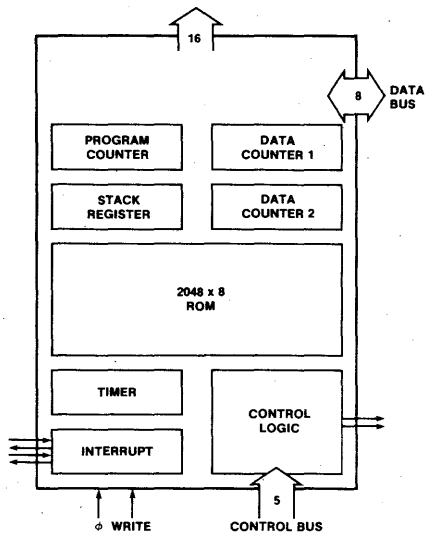
3853
SMI BLOCK DIAGRAM



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The 3857 Program Storage and Memory Interface (PSMI) provides 2K of ROM, an external interrupt and timer with masked interrupt vector as well as 16 address lines and memory control logic.

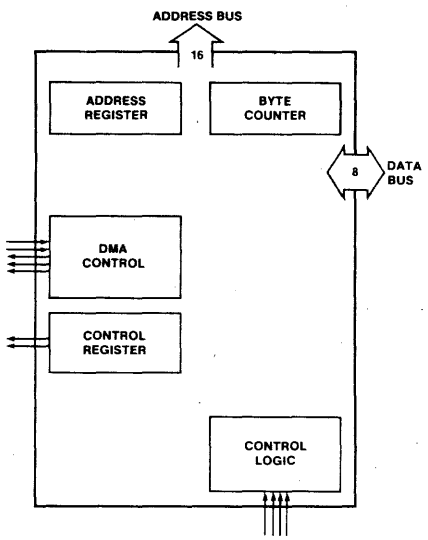
3857
PSMI BLOCK DIAGRAM



3854/3855 Direct Memory Access (DMA)

The DMA circuits provide a high-speed data path between a system memory and the peripheral electronics with up to 500 kilo bytes of transparent data transfer per second. These circuits can transfer data blocks of up to 4096 bytes and can interrupt the CPU when this data transfer is complete or can be programmed to continue transferring until stopped.

3854
DMA BLOCK DIAGRAM

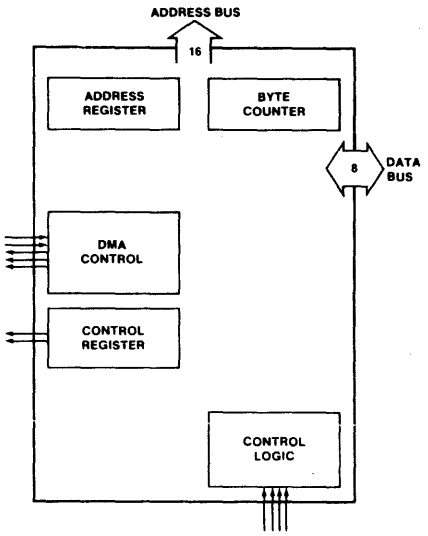


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The 3854, when working in conjunction with the 3852, does not require overhead electronics to track memory addresses, bytes transferred and handshaking signals.

The 3855 DMA is designed for use with other processors such as the Fairchild 6800 or the 8080 and Z80 circuits.

3855
DMA BLOCK DIAGRAM

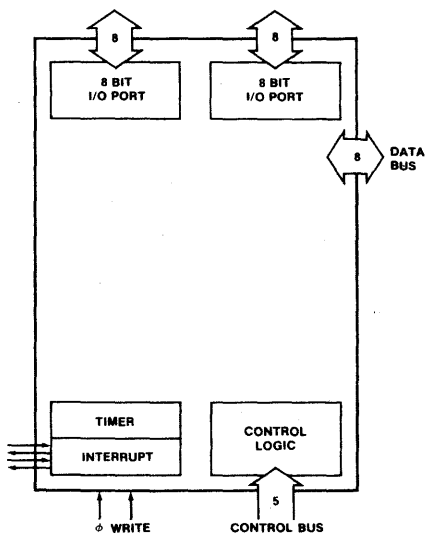


3861/3871 Peripheral Input/Output

The 3861 PIO circuit contains all of the logic of the 3851 PSU without the 1K ROM. The 3861 is available in five versions as listed below.

TYPE	I/O PORTS	INTERRUPT ADDRESS VECTOR	
		TIMER	EXTERNAL
A	4-7	0600	0680
B	8-13	0340	03C0
C	20-23	0320	03A0
D	24-27	0360	03E0
E	4-7	0020	00A0

3861
PIO BLOCK DIAGRAM

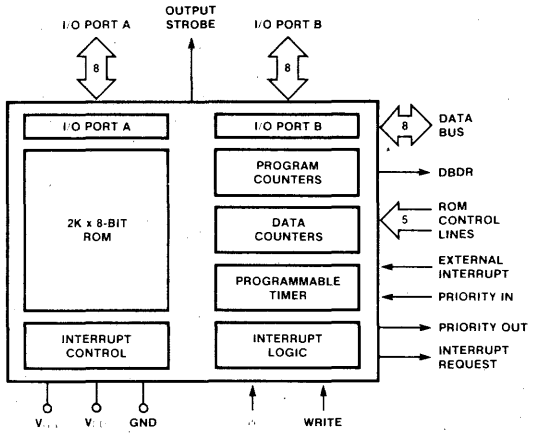


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The 3871 contains an improved timer and event counter identical to that used on the 3870. The 3871 is available in four versions as listed below.

TYPE	I/O PORTS	PORT TYPE	INTERRUPT ADDRESS VECTOR	
			TIMER	EXTERNAL
E	4-7	Standard	0020	00A0
F	4-7	Direct Drive	0020	00A0
G	4-7	Open Drain	0020	00A0
H	8-B	Standard	0420	04A0

3871
PIO BLOCK DIAGRAM



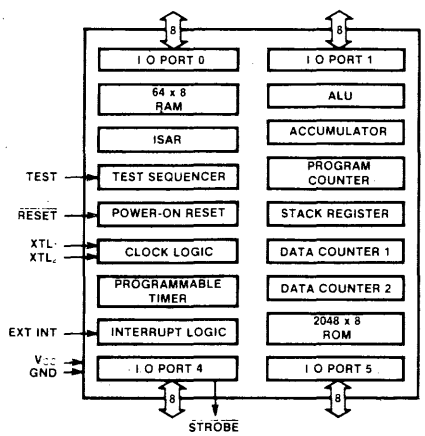
THE MICROMACHINE SERIES

F3870 MicroMachine™2

The Fairchild MicroMachines are a series of single-chip microcomputer circuits to serve the high-volume cost-sensitive controller market. The F3870 MicroMachine 2 is the first offering in this series. The F3870 is a complete 8-bit microcomputer on a single MOS integrated circuit. The F3870 can execute the F8 instruction set of more than 70 commands, allowing expansion into multi-chip configurations with software compatibility. The device features 2048 bytes of ROM, 64 bytes of scratch-pad RAM, a programmable binary timer, 32 bits of I/O, and a single +5 Volt power supply requirement.

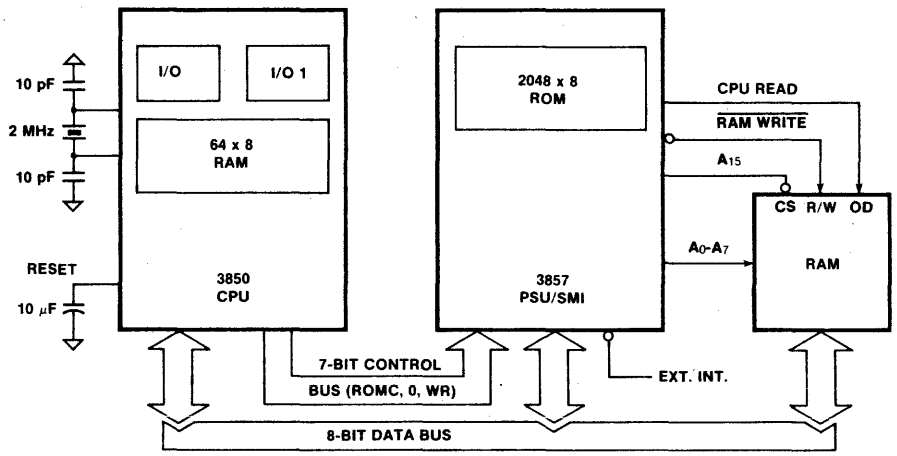
Utilizing ion-implanted, n-channel silicon-gate technology and advanced circuit design techniques, the single-chip F3870 offers maximum cost effectiveness in a wide range of control and logic replacement applications.

F3870
8-BIT MICROCOMPUTER
BLOCK DIAGRAM

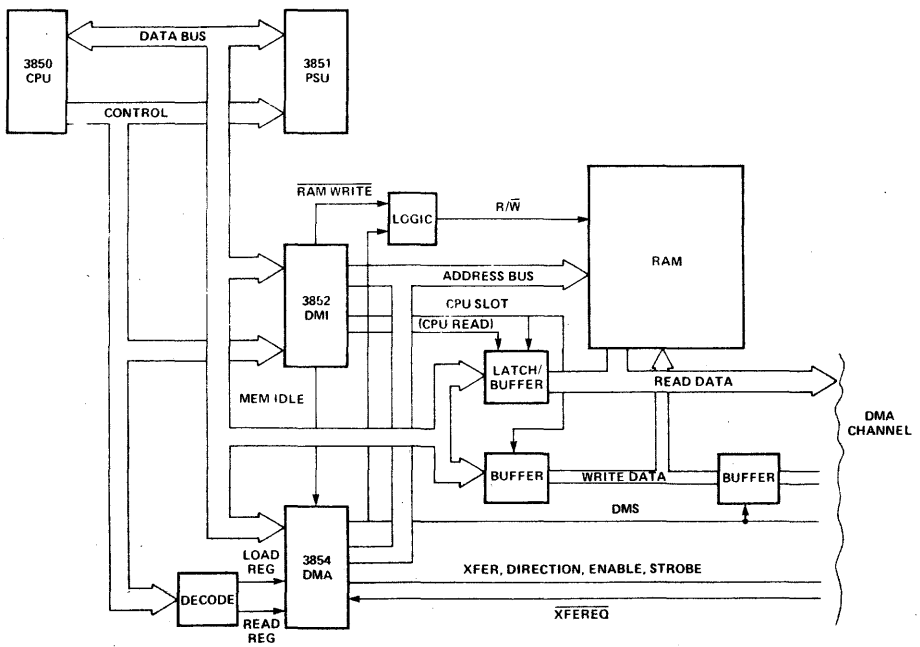


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F8 APPLICATIONS



TYPICAL SYSTEM CONFIGURATION



A TYPICAL DMA CONFIGURATION

Fairchild Semiconductor
MICROPROCESSOR

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9403

FIRST-IN FIRST-OUT (FIFO) BUFFER MEMORY

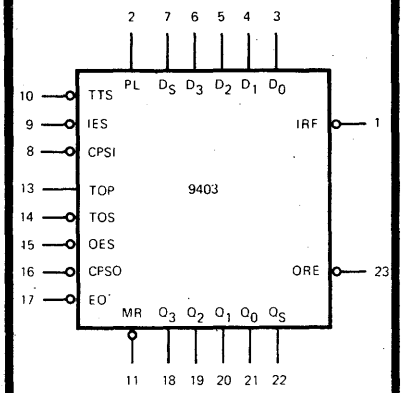
FAIRCHILD TTL MACROLOGIC

DESCRIPTION – The 9403 is an expandable fall-through type high-speed First-In First-Out (FIFO) Buffer Memory optimized for high speed disc or tape controllers and communication buffer applications. It is organized as 16 words by four bits and may be expanded to any number of words or any number of bits (in multiples of four). Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

The 9403 has 3-state outputs which provide added versatility and is fully compatible with all TTL families.

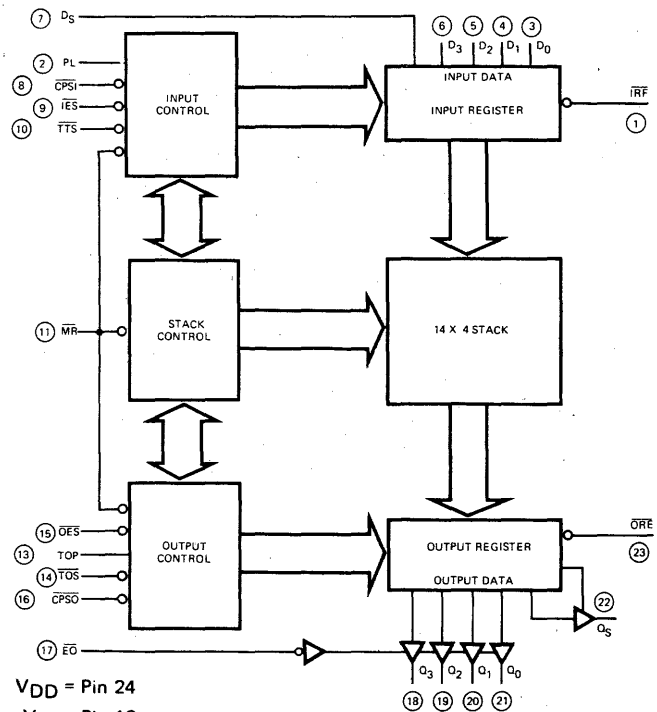
- **10 MHz SERIAL OR PARALLEL DATA RATE**
- **SERIAL OR PARALLEL INPUT**
- **SERIAL OR PARALLEL OUTPUT**
- **EXPANDABLE WITHOUT EXTERNAL LOGIC**
- **3-STATE OUTPUTS**
- **FULLY COMPATIBLE WITH ALL TTL FAMILIES**
- **SLIM 24-PIN PACKAGE**

LOGIC SYMBOL



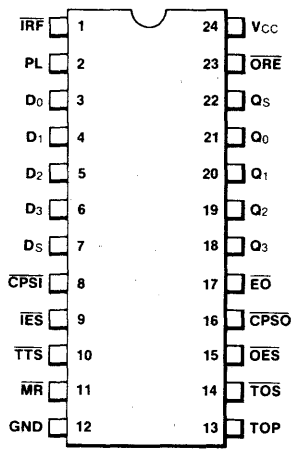
V_{CC} = Pin 24
GND = Pin 12

BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12
◯ = Pin Numbers

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

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PIN NAMES

PIN NAME	DESCRIPTION	LOADING (Note a) HIGH	LOADING (Note a) LOW	COMMENTS
$D_0 - D_3$	Parallel Data Inputs	1.0 U.L.	0.23 U.L.	
D_S	Serial Data Input	1.0 U.L.	0.23 U.L.	
PL	Parallel Load Input	1.0 U.L.	0.23 U.L.	HIGH on PL enables $D_0 - D_3$. Not edge triggered. Ones catching.
$\overline{CPSI}$	Serial Input Clock	1.0 U.L.	0.23 U.L.	Edge triggered. Activates on falling edge.
$\overline{IES}$	Serial Input Enable	1.0 U.L.	0.23 U.L.	Enables serial and parallel input when LOW.
$\overline{TTS}$	Transfer to Stack Input	1.0 U.L.	0.23 U.L.	A LOW on this pin initiates fall through.
$\overline{OES}$	Serial Output Enable Input	1.0 U.L.	0.6 U.L.	Enables serial and parallel output when LOW.
$\overline{TOS}$	Transfer Out Serial Input	1.0 U.L.	0.23 U.L.	A LOW on this pin enables a word to be transferred from the stack to the output register. (TOP must be HIGH also for the transfer to occur). Not edge triggered.
TOP	Transfer Out Parallel Input	1.0 U.L.	0.23 U.L.	A HIGH on this pin enables a word to be transferred from the stack to the output register. ($\overline{TOS}$ must be LOW for the transfer to occur). Not edge triggered.
$\overline{MR}$	Master Reset	1.0 U.L.	0.23 U.L.	Active LOW.
$\overline{EO}$	Output Enable	1.0 U.L.	0.23 U.L.	Active LOW.
$\overline{CPSO}$	Serial Output Clock Input	1.0 U.L.	0.23 U.L.	Edge triggered. Activates on falling edge.
$Q_0 - Q_3$	Parallel Data Outputs	130 U.L.	10 U.L.	(Note b)
Q_S	Serial Data Output	10 U.L.	10 U.L.	(Note b)
$\overline{IRF}$	Input Register Full Output	10 U.L.	5 U.L.	LOW when input register is full (Note b).
$\overline{ORE}$	Output Register Empty Output	10 U.L.	5 U.L.	HIGH when output register contains valid data.

NOTE: a. 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b. Output fan-out with $V_{OL} \leq 0.5$ V.

FUNCTIONAL DESCRIPTION – As shown in the block diagram the 9403 consists of three sections:

1. An Input Register with parallel and serial data inputs as well as control inputs and outputs for input handshaking and expansion.
2. A 4-bit wide, 14-word deep fall-through stack with self-contained control logic.
3. An Output Register with parallel and serial data outputs as well as control inputs and outputs for output handshaking and expansion.

Since these three sections operate asynchronously and almost independently, they will be described separately below:

Input Register (Data Entry):
The Input Register can receive data in either bit-serial or in 4-bit parallel form. It stores this data until it is sent to the fall-through stack and generates the necessary status and control signals.

Figure 1 is a conceptual logic diagram of the input section. As described later, this 5-bit register is initialized by setting the F3 flip-flop and resetting the other flip-flops. The Q-output of the last flip-flop (FC) is brought out as the "Input Register Full" output ($\overline{IRF}$). After initialization this output is HIGH.

Parallel Entry – A HIGH on the PL input loads the $D_0 - D_3$ inputs into the $F_0 - F_3$ flip-flops and sets the FC flip-flop. This forces the $\overline{IRF}$ output LOW indicating that the input register is full. During parallel entry, the $\overline{CPSI}$ input must be LOW. If parallel expansion is not being implemented, $\overline{IES}$ must be LOW to establish row mastership (see Expansion section).

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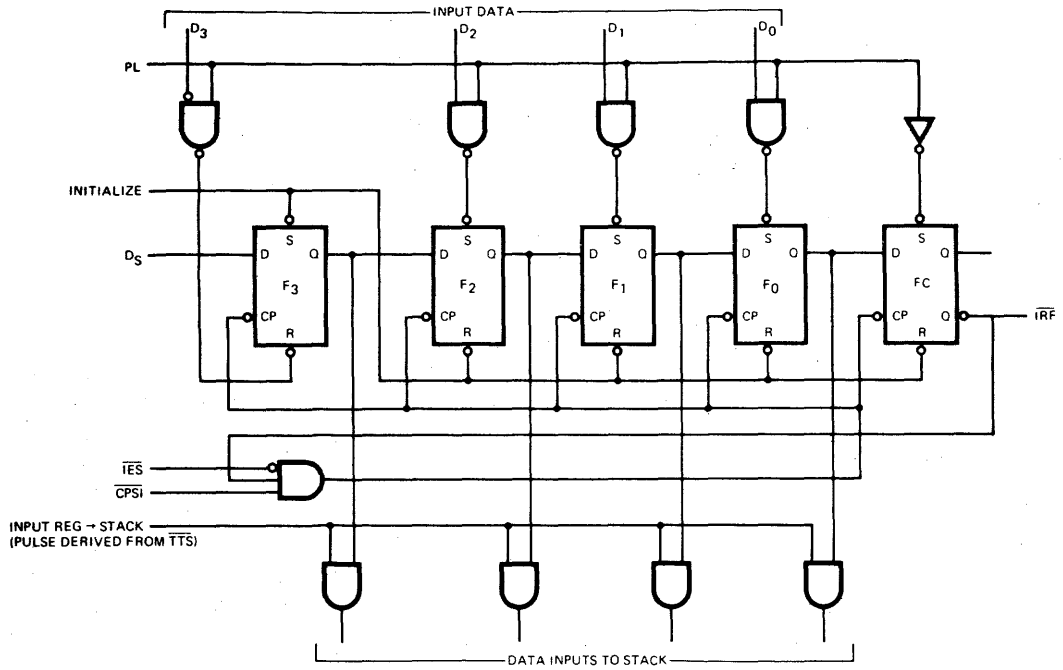


Fig. 1
CONCEPTUAL INPUT SECTION

Serial Entry – Data on the D_S input is serially entered into the F_3, F_2, F_1, F_0, FC shift register on each HIGH-to-LOW transition of the CPSI clock input, provided IES and PL are LOW.

After the fourth clock transition, the four data bits located in the four flip-flops F_0 – F_3. The FC flip-flop is set, forcing the $\overline{IRF}$ output LOW and internally inhibiting $\overline{CPSI}$ clock pulses from effecting the register. *Figure 2* illustrates the final positions in a 9403 resulting from a 64-bit serial bit train. B_0 is the first bit, B_{63} the last bit.

Transfer to the Stack –The outputs of Flip-Flops F_0 – F_3 feed the stack. A LOW level on the $\overline{TTS}$ input initiates a "fall-through" action. If the top location of the stack is empty, data is loaded into the stack and the input register is re-initialized. Note that this initialization is postponed until PL is LOW again. Thus, automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

An RS Flip-Flop (the Request Initialization Flip-Flop shown in *Figure 10*) in the control section records the fact that data has been transferred to the stack. This prevents multiple entry of the same word into the stack despite the fact the $\overline{IRF}$ and $\overline{TTS}$ may still be LOW. The Request Initialization Flip-Flop is not cleared until PL goes LOW. Once in the stack, data falls through the stack automatically, pausing only when it is necessary to wait for an empty next location. In the 9403, as in most modern FIFO designs, the $\overline{MR}$ input only initializes the stack control section and does not clear the data.

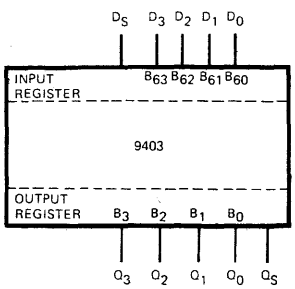


Fig. 2
FINAL POSITIONS IN A 9403 RESULTING FROM A 64-BIT SERIAL TRAIN

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Output Register (Data Extraction) – The Output Register receives 4-bit data words from the bottom stack location, stores it and outputs data on a 3-state 4-bit parallel data bus or on a 3-state serial data bus. The output section generates and receives the necessary status and control signals. *Figure 3* is a conceptual logic diagram of the output section.

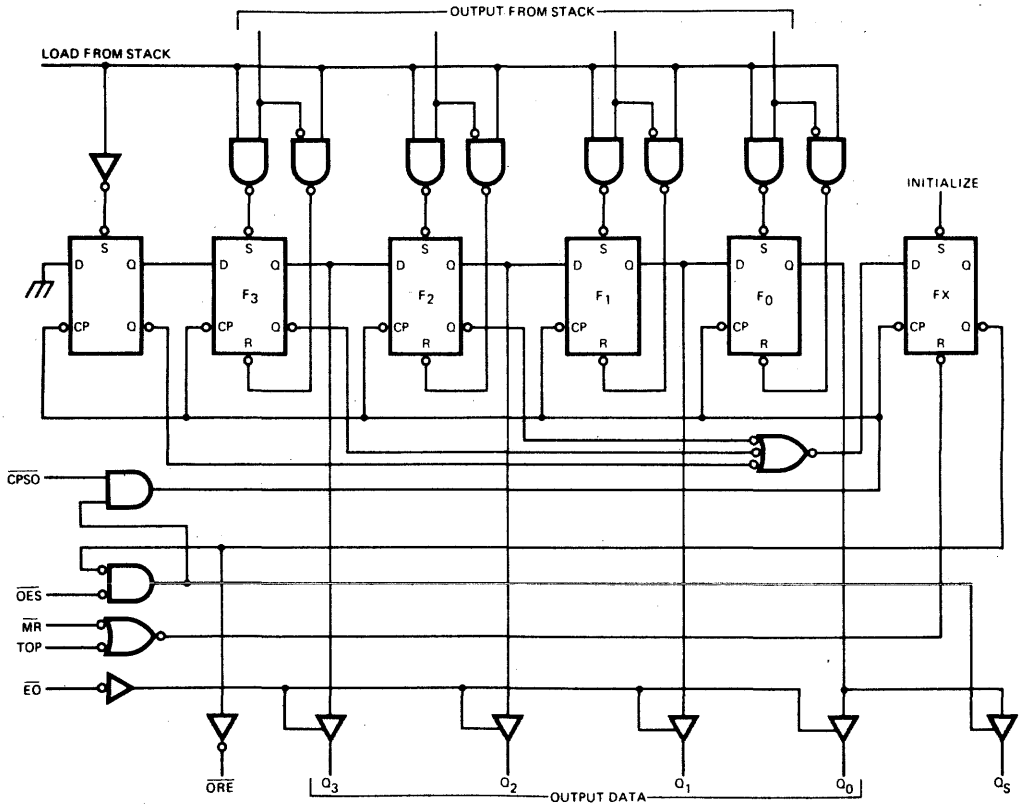


Fig. 3
CONCEPTUAL OUTPUT SECTION

Parallel Data Extraction – When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided the "Transfer Out Parallel" (TOP) input is HIGH. As a result of the data transfer $\overline{ORE}$ goes HIGH, indicating valid data on the data outputs (provided the 3-state buffer is enabled). TOP can now be used to clock out the next word. When TOP goes LOW, $\overline{ORE}$ will go LOW indicating that the output data has been extracted, but the data itself remains on the output bus until the next HIGH level at TOP permits the transfer of the next word (if available) into the Output Register. During parallel data extraction $\overline{CPSO}$ should be LOW. $\overline{TOS}$ should be grounded for single slice operation or connected to the appropriate $\overline{ORE}$ for expanded operation (see Expansion section).

TOP is not edge triggered. Therefore, if TOP goes HIGH before data is available from the stack, but data does become available before TOP goes LOW again, that data will be transferred into the Output Register. However, internal control circuitry prevents the same data from being transferred twice. If TOP goes HIGH and returns to LOW before data is available from the stack, ORE remains LOW indicating that there is no valid data at the outputs.

Serial Data Extraction – When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided $\overline{TOS}$ is LOW and TOP is HIGH. As a result of the data transfer $\overline{ORE}$ goes HIGH indicating valid data in the register. The 3-state Serial Data Output, Q_S, is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{CPSO}$. To prevent false shifting, $\overline{CPSO}$ should be LOW when the new word is being loaded into the Output Register. The fourth transition empties the shift register, forces $\overline{ORE}$ output LOW and disables the serial output, Q_S (refer to *Figure 3*). For serial operation the $\overline{ORE}$ output may be tied to the $\overline{TOS}$ input, requesting a new word from the stack as soon as the previous one has been shifted out.

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Horizontal and Vertical Expansion - The 9403 can be expanded in both the horizontal and vertical directions without any external parts and without sacrificing any of its FIFO's flexibility for serial/parallel input and output. The interconnections necessary to form a 31-word by 16-bit FIFO are shown in *Figure 4.* Using the same technique, any FIFO of (15m + 1) words by (4n) bits can be constructed, where m is the number of devices in a column and n is the number of devices in a row. *Figures 5* and *6* show the timing diagrams for serial data entry and extraction for the 31-word by 16-bit FIFO shown in *Figure 4.* The final position of data after serial insertion of 496 bits into the FIFO array of *Figure 4* is shown in *Figure 7.*

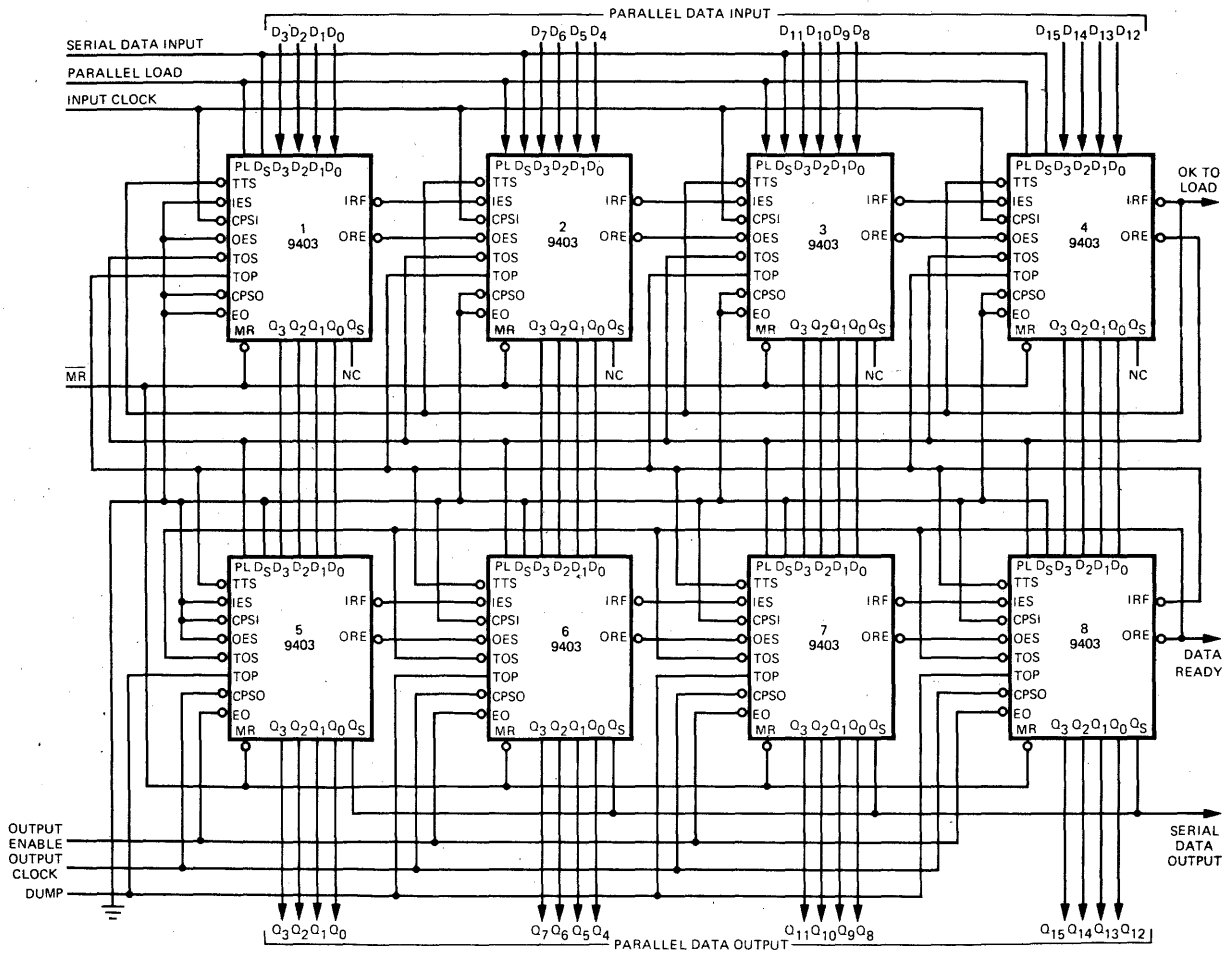


Fig. 4
A 31 X 16 FIFO ARRAY

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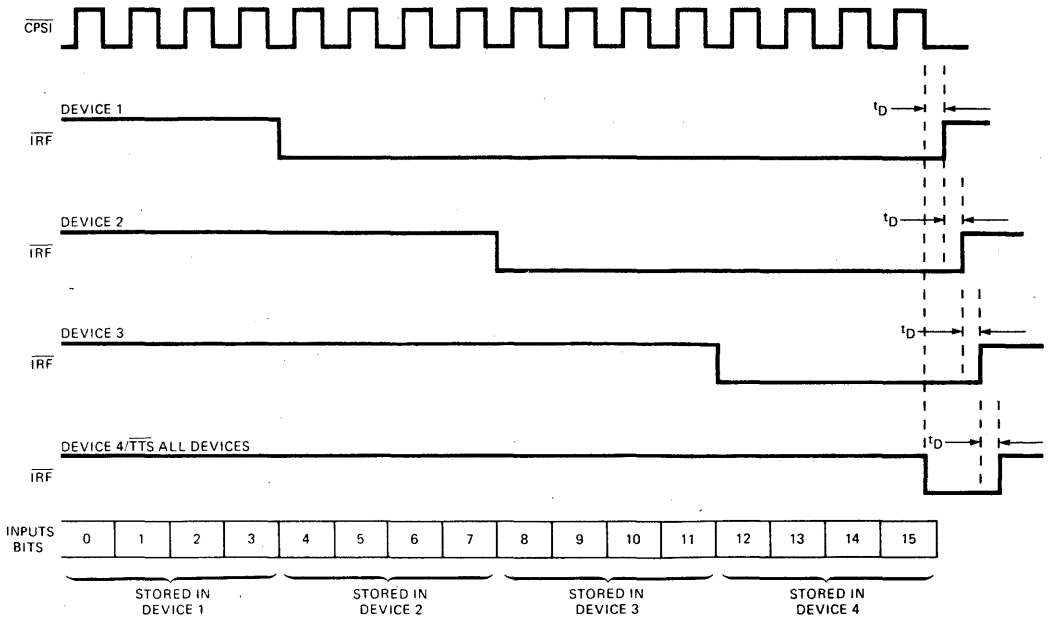


Fig. 5
SERIAL DATA ENTRY FOR ARRAY OF FIG. 6

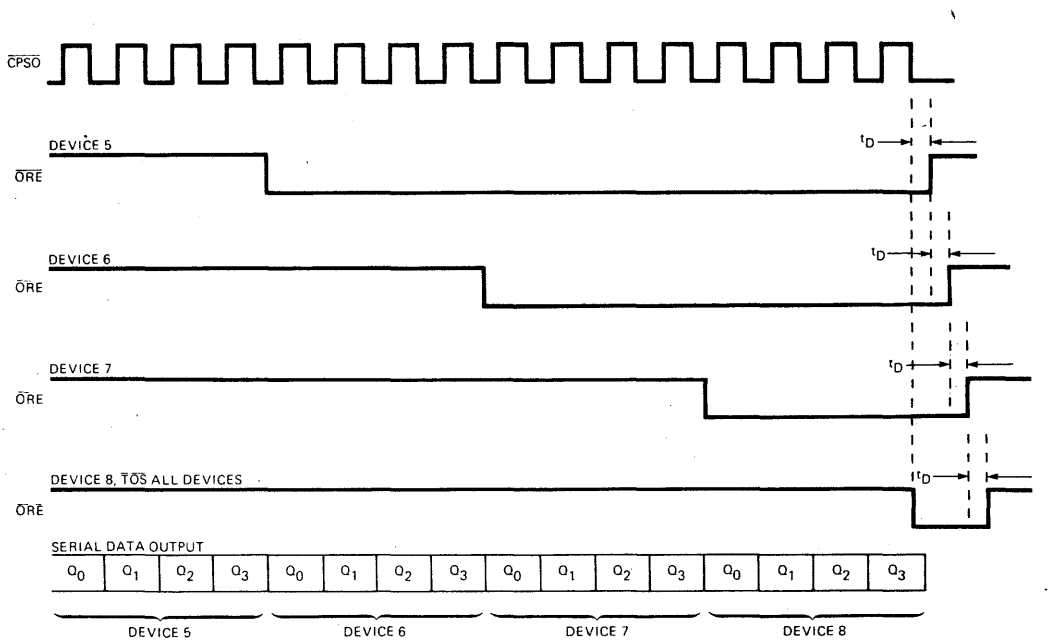


Fig. 6
SERIAL DATA EXTRACTION FOR ARRAY OF FIG. 6

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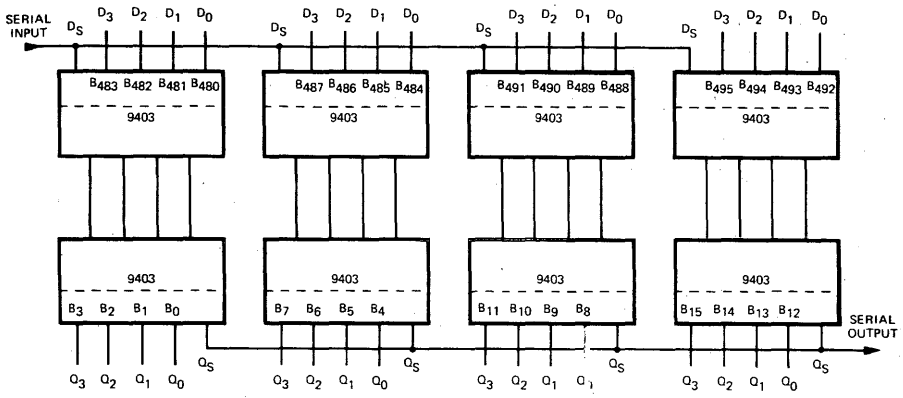


Fig. 7
FINAL POSITION OF A 496-BIT SERIAL INPUT

Interlocking Circuitry – Most conventional FIFO designs provide status signals analogous to $\overline{IRF}$ and $\overline{ORE}$. However, when these devices are operated in arrays, variations in unit to unit operating speed require external gating to assure all devices have completed an operation. The 9403 incorporates simple but effective "master/slave" interlocking circuitry to eliminate the need for external gating.

In the 9403 array of *Figure 4* devices 1 and 5 are defined as "row masters" and the other devices are slaves to the master in their row. No slave in a given row will initialize its Input Register until it has received LOW on its $\overline{IES}$ input from a row master or a slave of higher priority.

In a similar fashion, the $\overline{ORE}$ outputs of slaves will not go HIGH until their $\overline{OES}$ inputs have gone HIGH. This interlocking scheme ensures that new input data may be accepted by the array when the $\overline{IRF}$ output of the final slave in that row goes LOW and that output data for the array may be extracted when the $\overline{ORE}$ of the final slave in the output row goes HIGH.

The row master is established by connecting its $\overline{IES}$ input to ground while a slave receives its $\overline{IES}$ input from the $\overline{IRF}$ output of the next higher priority device. When an array of 9403 FIFOs is initialized with a LOW on the $\overline{MR}$ inputs of all devices, the $\overline{IRF}$ outputs of all devices will be HIGH. Thus, only the row master receives a LOW on the $\overline{IES}$ input during initialization. *Figure 8* is a conceptual logic diagram of the internal circuitry which determines master/slave operation. Whenever $\overline{MR}$ and $\overline{IES}$ are LOW, the Master Latch is set. Whenever $\overline{TTS}$ goes LOW the Request Initialization Flip-Flop will be set. If the Master Latch is HIGH, the Input Register will be immediately initialized and the Request Initialization Flip-Flop reset. If the Master Latch is reset, the Input Register is not initialized until $\overline{IES}$ goes LOW. In array operation, activating the $\overline{TTS}$ initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a $\overline{TOS}$ or TOP input initiates a load-from-stack operation and sets the ORE Request Flip-Flop. If the Master Latch is set, the last Output Register Flip-Flop is set and $\overline{ORE}$ goes HIGH. If the Master Latch is reset, the $\overline{ORE}$ output will be LOW until an $\overline{OES}$ input is received.

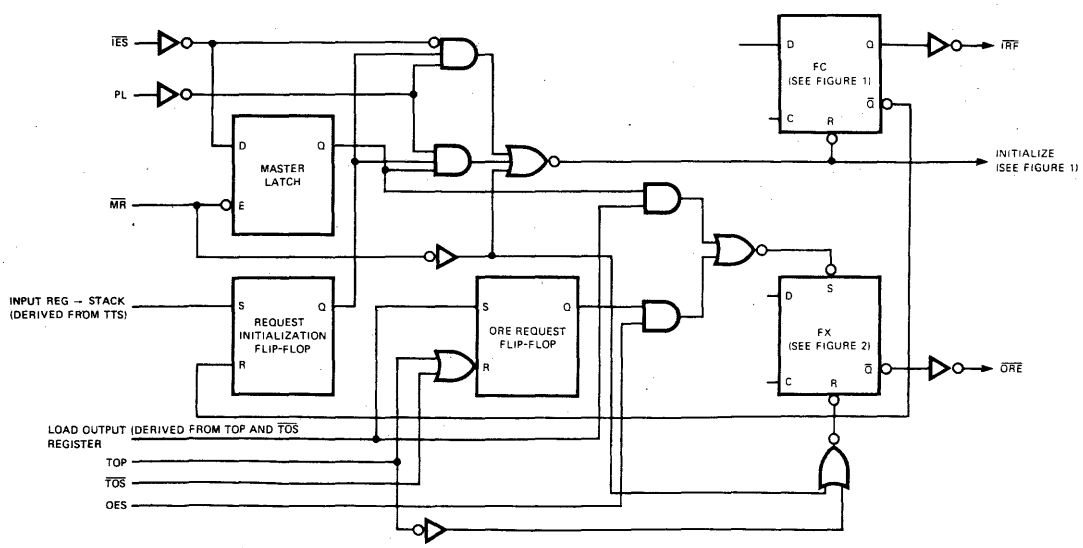


Fig. 8
CONCEPTUAL DIAGRAM, INTERLOCKING CIRCUITRY

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9405A

ARITHMETIC LOGIC REGISTER STACK

FAIRCHILD TTL MACROLOGIC

DESCRIPTION – The 9405A Arithmetic Logic Register Stack (ALRS) is designed to implement accumulators/general registers in high performance, microprogrammed digital systems (microprocessors). The 9405A is a 4-bit slice with expansion features for larger word lengths.

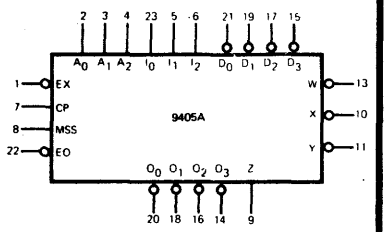
The device contains a 4-bit ALU, 8-word by 4-bit RAM, a 4-bit edge triggered output register and associated control logic. The ALU implements eight arithmetic and logic functions on two 4-bit operands. The desired function is specified by three instruction inputs (I-field). One of the operands is supplied from an external source (D-Bus). The second operand is supplied internally from one of the eight RAM locations. The desired RAM location is specified by the address inputs (A-field) when the clock input is HIGH. The result from the ALU is loaded into a RAM location during the period when the clock input is LOW. The address for the desired RAM location for writing is also specified by the A-field. Moreover, the result from the ALU is also loaded into the output register on LOW-to-HIGH transistion of the clock input. The output register provides the 4-bit output (O-Bus) through 3-state buffers.

For accumulator oriented microprocessor architectures, the A-field inputs to the 9405A remain the same during the HIGH and LOW period of the clock cycle. However, in general register oriented architectures, the A-field inputs are changed appropriately to realize the source and destination registers during HIGH and LOW period of the clock respectively.

Carry propagate and carry generate outputs are provided by the 9405A to facilitate carry lookahead expansion. The industry standard 93S42/74S182 carry lookahead unit can be used for this purpose. If high speed arithmetic is not needed, ripply carry expansion can be used. The ripple expansion eliminates the need for an external carry lookahead unit. The 9405A also provides four status signals (condition codes) to characterize the result of an operation – Zero, Negative, Overflow and Carry.

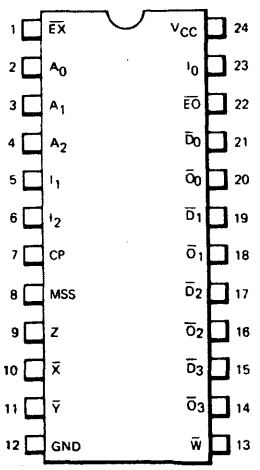
The 9405A is downward compatible with the 9405 and should be used in new designs. The 9405A is fully compatible with all TTL families.

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



- EIGHT GENERAL REGISTERS/ACCUMULATORS IN A SINGLE PACKAGE
- OPTIMIZED FOR MICROPROGRAMMED OPERATION
- HIGH SPEED - 13 MHz MICROINSTRUCTION RATE (SINGLE SLICE)
- EXPANDABLE IN MULTIPLES OF FOUR BITS
- PROVIDES FOR RIPPLE OR CARRY LOOKAHEAD
- PROVIDES STATUS - CARRY, ZERO, NEGATIVE AND OVERFLOW
- 3-STATE OUTPUTS
- SLIM 24-PIN PACKAGE

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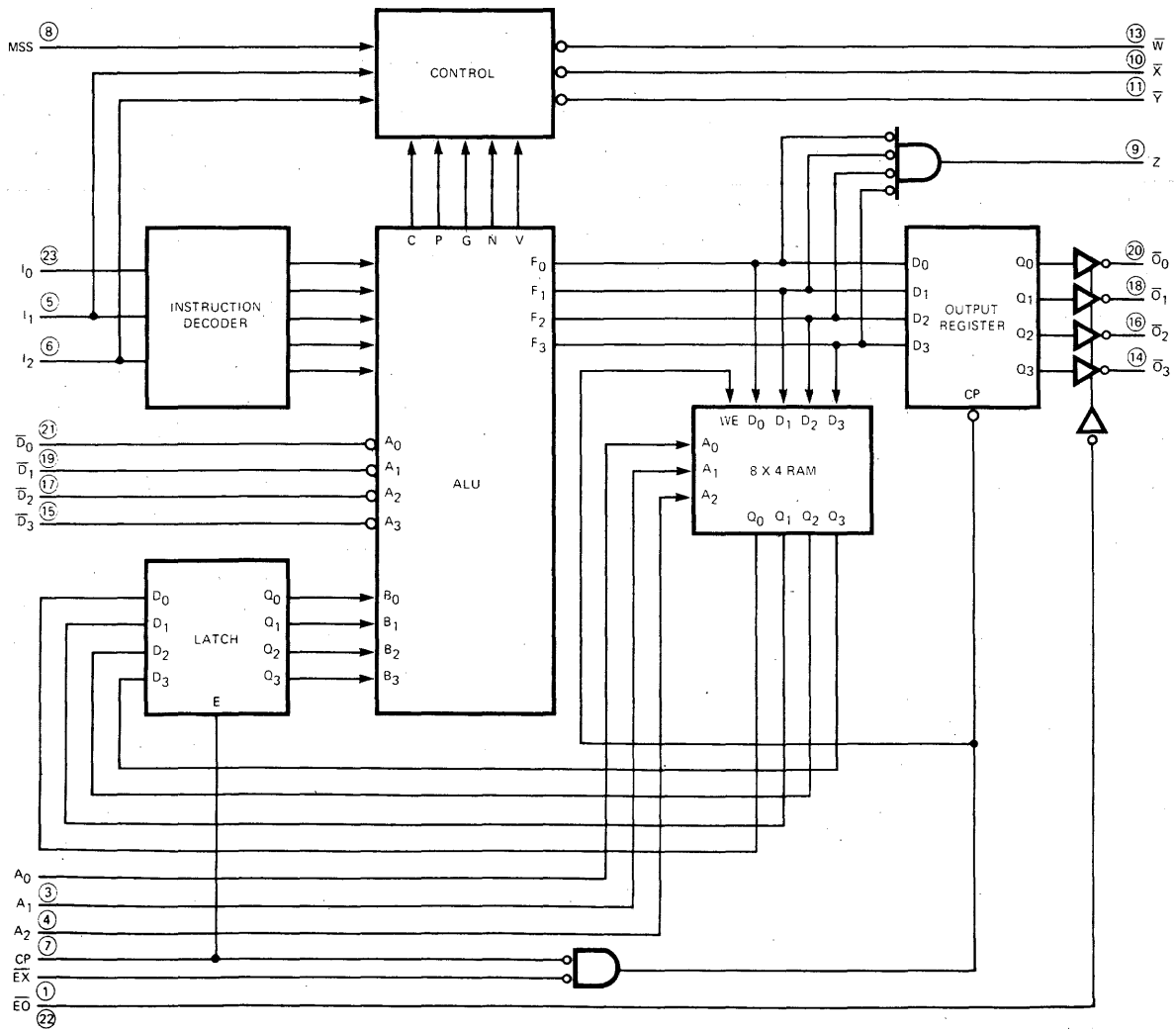
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PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{D}_0 - \overline{D}_3$	Data Inputs (Active LOW)	1.0 U.L.	0.23 U.L.
$A_0 - A_2$	Address Inputs	1.0 U.L.	0.23 U.L.
$I_0 - I_2$	Instruction Inputs (Note b)	1.0 U.L.	0.23 U.L.
MSS	Most Significant Slice Input (Active HIGH)	1.0 U.L.	0.23 U.L.
CP	Clock Input	1.0 U.L.	0.23 U.L.
$\overline{EO}$	Output Enable Input (Active LOW)	1.0 U.L.	0.23 U.L.
$\overline{EX}$	Execute Input (Active LOW)	1.0 U.L.	0.23 U.L.
$\overline{O}_0 - \overline{O}_3$	Data Outputs (Active LOW)	130 U.L.	10 U.L.
$\overline{W}$	Ripple Carry Output (Active LOW) (Note c)	10 U.L.	5.0 U.L.
$\overline{X}$	Carry Propagate Output (Note d)	10 U.L.	5.0 U.L.
$\overline{Y}$	Carry Generate Output (Note e)	10 U.L.	5.0 U.L.
Z	Zero Status Output (Active HIGH, Open Collector)(Note f)		5.0 U.L.

NOTES:
a) 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW (0.5 V).
b) I_0 used also for carry input.
c) W output also carries instruction information.
d) X output provides Negative status (active LOW) on most significant slice.
e) Y output provides Overflow status (active LOW) on most significant slice.
f) An external pull-up resistor is required to supply HIGH drive capability.

BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION – As shown in the block diagram, the 9405A consists of a 4-bit ALU, 8-word by 4-bit RAM with latches, an Instruction Decoder, control logic and a 4-bit Output Register.

The ALU receives the active LOW data ($\overline{D}_0$ – $\overline{D}_3$) as one operand while the RAM provides the second operand through its latches. The ALU output is fed as input to the RAM and the Output Register. The active LOW output bus ($\overline{O}_0$ – $\overline{O}_3$) is from the Output Register through 3-state buffers. A HIGH on the $\overline{EO}$ input disables the buffers (high impedance state) while a LOW enables them.

The 6-bit instruction input for the 9405A consists of two 3-bit fields: A-field and I-field. A_0 – A_2 specifies the operation to be performed. The 8-word RAM can be considered to be providing eight registers (R_0 – R_7) and eight different operations can be performed on these registers. The I-field inputs are decided by the Instruction Decoder to generate necessary control signals for the ALU. The ALU generates Carry (C), Carry Propagate (P), Carry Generate (G), Negative (N) and Overflow (V) signals to be used by the control logic. The control logic manipulates these signals as a function of the I-field inputs and an external control input signal MSS. The MSS input separates the most significant slice in an array of 9405As from the remaining slices. A HIGH on the MSS denotes the most significance (MSS input may be tied directly to V_{CC}). In general, all except the most significant 9405A will have a LOW on the MSS input. The control logic generates three user outputs, $\overline{W}$, $\overline{X}$ and $\overline{Y}$. The significance of these outputs is discussed under the Expansion section. The Zero output (Z) is provided by an open collector transistor.

Table 1 lists the I-field assignment for the 9405A. There are only two arithmetic instructions in the table which require carry. It can also be noticed that the I_0 is the carry input. In the 9405A operation I_0 plays a dual role and will be discussed in the Expansion section.

The CP input is used to clock the 9405A. The content of the specified RAM location is read into the output latches whenever the CP input is HIGH. These latches are disabled when the CP is LOW. Thus, the information that was presented when CP was HIGH will be stored in the latches. Writing of the ALU result occurs whenever the CP and $\overline{EX}$ inputs are LOW. If the CP or $\overline{EX}$ input becomes HIGH, writing into the RAM will be terminated and the result will be loaded into the Output Register on the transition.

Operation – The 9405A can be used in two modes: general register and accumulator. In the general register mode, one address (R_X) is used to select a register (R_0 – R_7) for the source operand and another address (R_Y) is used to select a register (R_0 – R_7) as the destination for the result. This is accomplished by changing the A-field during the negative half cycle of the clock. In the accumulator mode, a single address is used to select a register (R_0 – R_7) for the source operand and the result is loaded back into the same register (implied destination). This mode is achieved by keeping the A-field unchanged for the entire clock cycle. The following page describes these modes in more detail.

TABLE 1
INSTRUCTION FIELD ASSIGNMENT

I_2	I_1	I_0	ACCUMULATOR MODE ($R_x = R_y$)		GENERAL REGISTER MODE ($R_x \neq R_y$)	
L	L	L	R_x *plus* $\overline{\text{D-Bus}}$ *plus* 1 → R_x	Accumulate and Increment	R_x *plus* $\overline{\text{D-Bus}}$ *plus* 1 → R_y	Add with Carry
L	L	H	R_x *plus* $\overline{\text{D-Bus}}$ → R_x	Accumulate	R_x *plus* $\overline{\text{D-Bus}}$ → R_y	Add
L	H	L	$R_x \cdot \overline{\text{D-Bus}}$ → R_x	Logical AND	$R_x \cdot \overline{\text{D-Bus}}$ → R_y	Logical AND
L	H	H	$\overline{\text{D-Bus}}$ → R_x	Load	$\overline{\text{D-Bus}}$ → R_y	Load
H	L	L	R_x → Output Register	Read	R_x → R_y	Transfer
H	L	H	$R_x + \overline{\text{D-Bus}}$ → R_x	Logical OR	$R_x + \overline{\text{D-Bus}}$ → R_y	Logical OR
H	H	L	$R_x \oplus \overline{\text{D-Bus}}$ → R_x	Exclusive OR	$R_x \oplus \overline{\text{D-Bus}}$ → R_y	Exclusive OR
H	H	H	D-Bus → R_x	Load Complement	D-Bus → R_y	Load Complement

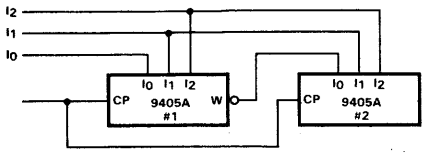
NOTES:
1. R_x is the RAM location addressed by A_0 – A_2 when CP is HIGH.
2. R_y is the RAM location addressed by A_0 – A_2 when CP is LOW.
3. The result of any operation is always loaded into the Output Register at the end of the cycle provided that $\overline{EX}$ is LOW.

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AC CHARACTERISTICS: MULTIPLE SLICE OPERATION

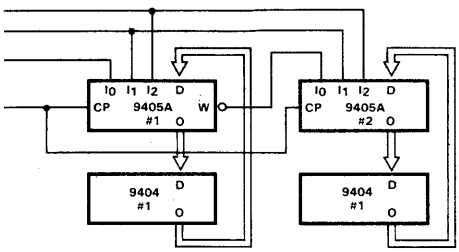
A single 9405A slice operating without overhead is guaranteed to operate at 13.3 MHz (75 ns). Such a configuration, however, would be extremely rare. AC guarantees for multiple slice operation depend on the configuration actually used. Several examples follow.

8-bit Machine with Ripple Carry



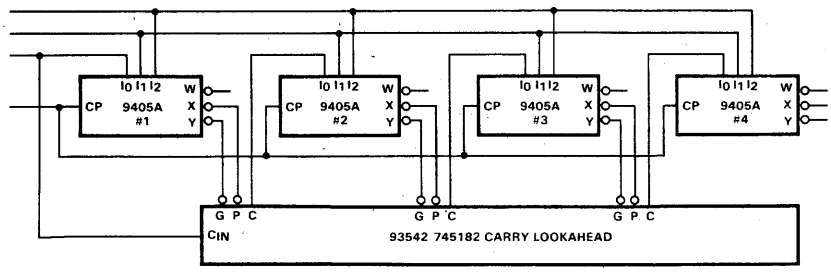
DESCRIPTION	TYP	MAX
Assume that at time, t = 0, the clock goes HIGH and the instruction and address information appear at the 9405A inputs		
t_{pd}-Address to $\overline{W}$ of 9405A # 1 ($\overline{W}$ is the carry-out pin)	44 ns	60 ns
t_{pd}-9405A # 2, I_0 to Status Flags (See Note 1)	30 ns	40 ns
Total clock period required	74 ns	100 ns
Frequency	13.5 MHz	10 MHz

8-bit Machine with Ripple Carry and DPS in Data Path (Note 2)



DESCRIPTION	TYP	MAX
Assume that at time, t = 0, the clock goes HIGH and the instruction and address information appear at the 9404 and 9405A inputs		
t_{pd}-Rising edge of clock to $\overline{O}$ outputs of 9405A # 1	18 ns	25 ns
t_{pd}-9404 # 1, $\overline{D}$ inputs to 9404 #1, O outputs (See 9404 data sheet)	15 ns	25 ns
t_{pd}-9405A # 1, $\overline{D}$ inputs to $\overline{W}$ ($\overline{W}$ is the carry-out pin)	30 ns	40 ns
t_{pd}-9405A # 2, I_0 to Status Flags (See Note 1)	30 ns	40 ns
Total clock period required	93 ns	130 ns
Frequency	10.7 MHz	7.7 MHz

16-bit Machine with Carry Lookahead

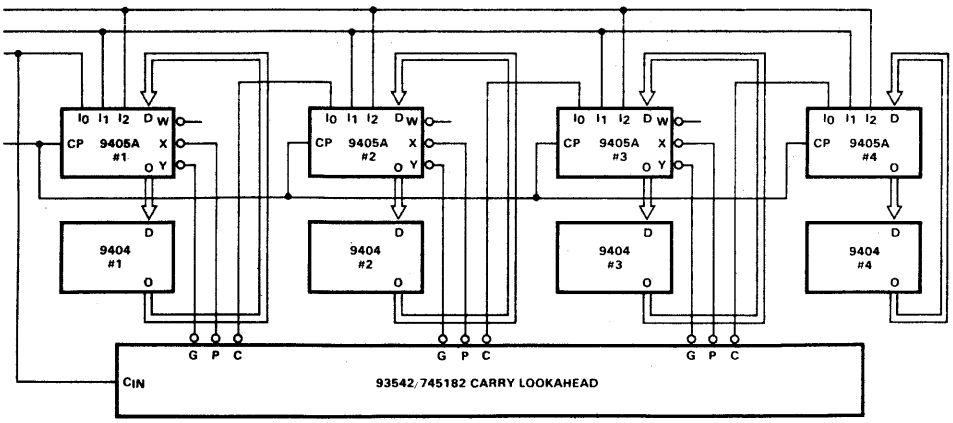


DESCRIPTION	TYP	MAX
Assume that at time, t = 0, the clock goes HIGH and the instruction and address information appear at the 9404 and 9405A inputs		
t_{pd}-Address inputs to $\overline{X}$, $\overline{Y}$ outputs of 9405A # 1	42 ns	58 ns
t_{pd}-G and P inputs of carry lookahead (Note: All G and P outputs are generated simultaneously. Therefore, 9405A # 2, # 3, # 4 set-up simultaneously.)	5 ns	7 ns
t_{pd}-9405A # 4, I_0 to Status Flags (See Note 1)	30 ns	40 ns
Total clock period required	77 ns	105 ns
Frequency	13 MHz	9.5 MHz

Notes on following pages.

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16-bit Machine with Carry Lookahead and DPS in Data Path (Note 3)



DESCRIPTION	TYP	MAX
Assume that at t = 0, the clock goes HIGH and the instruction and address information appear at the 9404 and 9405A inputs.		
t_{pd}-Rising edge of clock to $\overline{O}$ output of 9405A # 1	18 ns	25 ns
t_{pd}-9404 # 1, $\overline{D}$ inputs to $\overline{O}$ outputs	15 ns	25 ns
t_{pd}-9405A # 1, $\overline{D}$ inputs to $\overline{X}$, $\overline{Y}$ outputs (X, Y are carry propagate and generate)	30 ns	40 ns
t_{pd}-Carry propagate and generate inputs of carry lookahead to carry out. (Note that all carry outs are generated simultaneously.)	5 ns	7 ns
t_{pd}-9405A # 4, I_0 to Status Flags (See Note 1)	30 ns	40 ns
Total clock period required	98 ns	137 ns
Frequency	10 MHz	7.3 MHz

Architectures with Finite Delay between Rising Clock and the Appearance of Instructions and Address Information

Consider the previous case (16-bit with carry lookahead and DPS). After the clock rises, 25 ns is required before data appears at the input of the 9404. During this 25 ns there is no need for instruction or address information. Therefore, so long as the address and instructions appear within this 25 ns, no time is lost. Consequently, a pipeline system where the propagation delay of the pipeline register is less than 25 ns will operate at the speed guaranteed for the data path alone; *i.e.*, 7.3 MHz guaranteed for a 16-bit machine employing carry lookahead, 9404s in the data path, and a pipeline register with propagation delay less than 25 ns.

NOTES:
1. The 9405s could actually respond to a rising clock after the 18 ns (the I_0 to rising clock set-up time max). However, the status flags are not available until 40 ns have elapsed.
2. In this configuration, carry out for 9405A # 1 cannot be generated until the D inputs are present. These originate from the 9405A # 1 output register and must pass through 9404 # 1 before reaching the 9405A # 1 inputs.
3. In this configuration, carry propagate and generate outputs from 9405A # 1 cannot be generated until the D inputs are present. These originate from 9405A # 1 outputs register and must pass through 9404 # 1 before reaching the 9405A # 1 inputs.

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9408/9408A

MICROPROGRAM SEQUENCER

FAIRCHILD I^3L^{TM} MACROLOGIC

DESCRIPTION – The 9408/A Microprogram Sequencers control the order in which microinstructions are fetched from the control memory. It contains a 10-bit program counter, a 4-level last-in first-out stack and associated control logic. It can control up to a maximum of 1024 words of memory. For larger word capacities external paging can be used. The 9408/A are controlled by a 4-bit instruction input. The instruction set includes Fetch, Conditional and Unconditional Branches, Branch to Subroutine and Return from Subroutine.

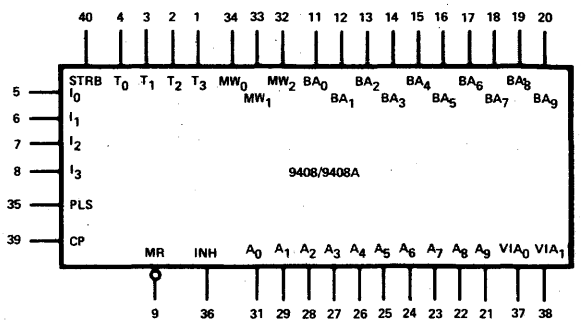
There are seven test inputs – four participate in conditional branches, and three in multiway branches. The conditional test lines are flip-flop buffered. These flip-flops can be tested individually by appropriate branch instructions. The three multiway test inputs are used to form the least significant three bits of the branch address for a multiway branch. Thus, branching occurs at one of eight unique locations depending on the bit pattern present on these three inputs.

The 9408/A are designed to operate in pipeline or non-pipeline mode as desired by the user. The device operates synchronously with the clock input and can be initialized using the Master Reset input.

The 9408/A are fabricated using Integrated Injection Logic (I^3L^{TM}) technology and fully compatiable with all TTL families.

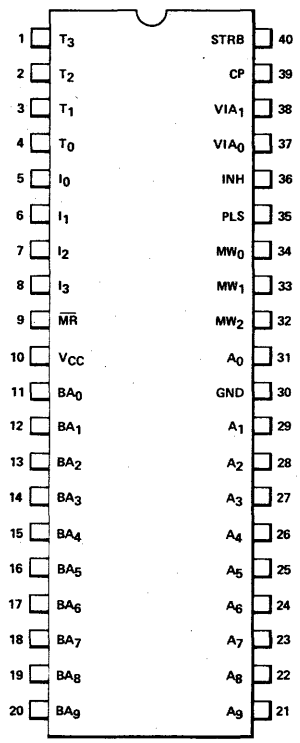
- **CONTROLS 1024 WORDS OF MICROPROGRAM MEMORY (10-BIT ADDRESS)**
- **UNRESTRICTED BRANCHING WITHIN 10-BIT ADDRESS SPACE**
- **16 INSTRUCTIONS**
- **FOUR FLIP-FLOP BUFFERED TEST INPUTS FOR CONDITIONAL BRANCHES**
- **8-WAY BRANCH CAPABILITY**
- **PIPELINE/NON-PIPELINE MODE OF OPERATION**

LOGIC SYMBOL



V_{CC} = Pin 10
GND = Pin 30

CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
BA_0–BA_9	Branch Address Inputs	0.5 U.L.	0.23 U.L.
T_0–T_3	Test Inputs	0.5 U.L.	0.23 U.L.
MW_0–MW_2	Multiway Branch Inputs	0.5 U.L.	0.23 U.L.
I_1	Instruction Input	0.5 U.L.	0.23 U.L.
I_0, I_2, I_3	Instruction Inputs	1.0 U.L.	0.46 U.L.
PLS	Pipeline Select Input	0.5 U.L.	0.23 U.L.
$\overline{MR}$	Master Reset Input (Active LOW)	0.5 U.L.	0.23 U.L.
CP	Clock Pulse Input	1.0 U.L.	0.46 U.L.
STRB	Strobe Input	0.5 U.L.	0.23 U.L.
A_0–A_9	Address Outputs	10 U.L.	5.0 U.L.
VIA_0, VIA_1	VIA Outputs	10 U.L.	5.0 U.L.
INH	Inhibit Output	10 U.L.	5.0 U.L.

Note a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

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FAIRCHILD

Fairchild Semiconductor
MICROPROCESSOR

BLOCK DIAGRAM

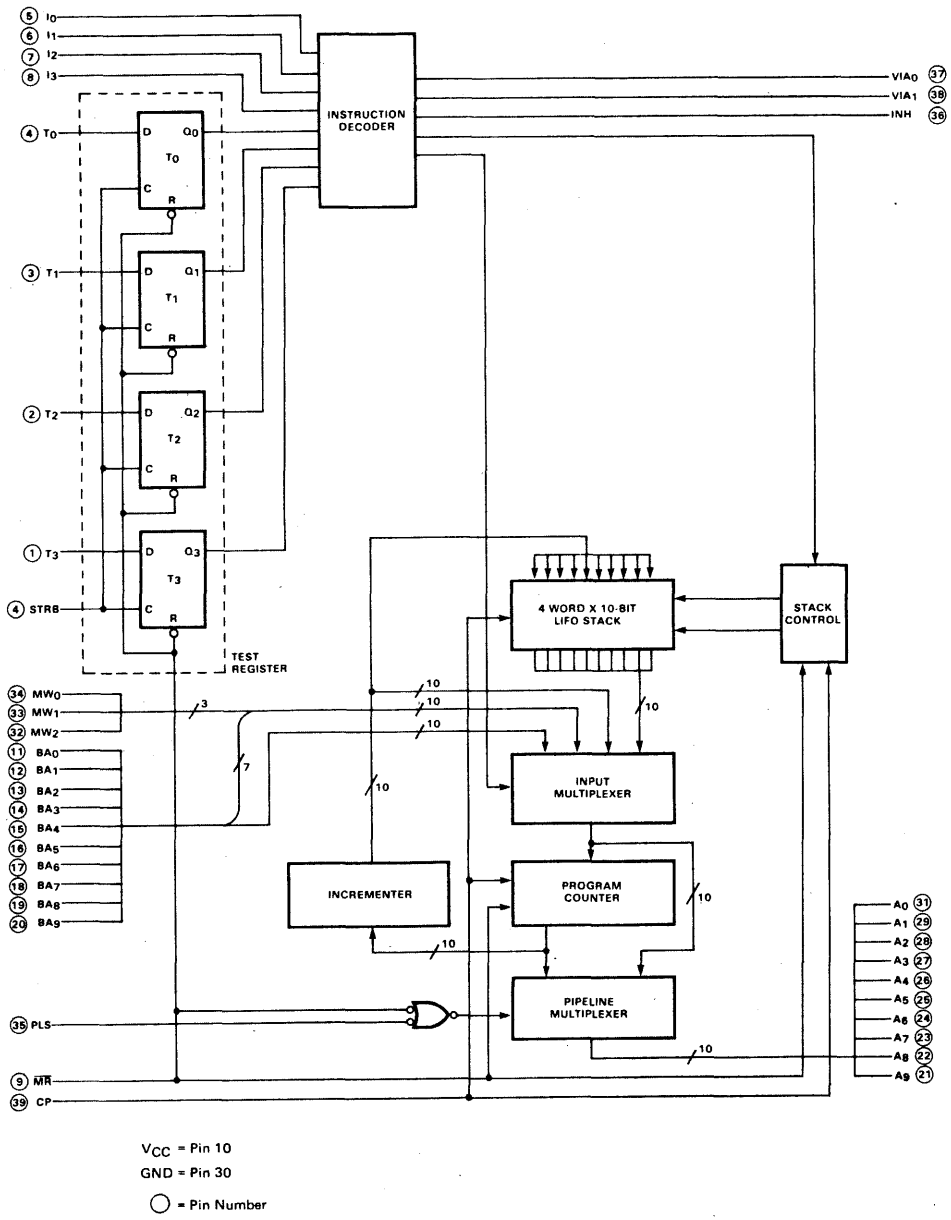


TABLE 1
9408/A INSTRUCTION SET

	MNEMONIC	DEFINITION	$I_3I_2I_1I_0$	$T_3T_2T_1T_0$	$O_9O_8O_7 \cdots O_2O_1O_0$	VIA_1VIA_0	INH	DESCRIPTION OF OPERATION
Unconditional Branch Instructions	BRV_0	Branch VIA_0	L H L L	X X X X	$BA_9\ BA_8 \cdots BA_1\ BA_0$	L L	H	$BA_0 \cdot BA_9 \rightarrow PC$
	BRV_1	Branch VIA_1	L H L H	X X X X	$BA_9\ BA_8 \cdots BA_1\ BA_0$	L H	H	$BA_0 \cdot BA_9 \rightarrow PC$
	BRV_2	Branch VIA_2	L H H L	X X X X	$BA_9\ BA_8 \cdots BA_1\ BA_0$	H L	H	$BA_0 \cdot BA_9 \rightarrow PC$
	BRV_3	Branch VIA_3	L H H H	X X X X	$BA_9\ BA_8 \cdots BA_1\ BA_0$	H H	H	$BA_0 \cdot BA_9 \rightarrow PC$
	BMW	Branch Multiway	L L H H	X X X X	$BA_9\ BA_3 \cdots MW_2\ MW_0$	L L	H	$MW_0 \cdot MW_2$; $BA_3 \cdot BA_9 \rightarrow PC$
	BSR	Branch to Subroutine	L L L H	X X X X	$BA_9\ BA_8 \cdots BA_1\ BA_0$	L L	H	$BA_0 \cdot BA_9 \rightarrow PC$ & Push the Stack
Conditional Branch Instructions	BTH_0	Branch on T_0 HIGH	H H L L	X X X H X X X L	$BA_9\ BA_8 \cdots BA_1\ BA_0$ PC+1	L L	H	If Test Register 0 is HIGH $BA_0 \cdot BA_9 \rightarrow PC$ If Test Register 0 is LOW $PC+1 \rightarrow PC$
	BTH_1	Branch on T_1 HIGH	H H L H	X X H X X X L X	$BA_9\ BA_8 \cdots BA_1\ BA_0$ PC+1	L L	H	If Test Register 1 is HIGH $BA_0 \cdot BA_9 \rightarrow PC$ If Test Register 1 is LOW $PC+1 \rightarrow PC$
	BTH_2	Branch on T_2 HIGH	H H H L	X H X X X L X X	$BA_9\ BA_8 \cdots BA_1\ BA_0$ PC+1	L L	H	If Test Register 2 is HIGH $BA_0 \cdot BA_9 \rightarrow PC$ If Test Register 2 is LOW $PC+1 \rightarrow PC$
	BTH_3	Branch on T_3 HIGH	H H H H	H X X X L X X X	$BA_9\ BA_8 \cdots BA_1\ BA_0$ PC+1	L L	H	If Test Register 3 is HIGH $BA_0 \cdot BA_9 \rightarrow PC$ If Test Register 3 is LOW $PC+1 \rightarrow PC$
	BTL_0	Branch on T_0 LOW	H L L L	X X X L X X X H	$BA_9\ BA_8 \cdots BA_1\ BA_0$ PC+1	L L	H	If Test Register 0 is LOW $BA_0 \cdot BA_9 \rightarrow PC$ If Test Register 0 is HIGH $PC+1 \rightarrow PC$
	BTL_1	Branch on T_1 LOW	H L L H	X X L X X X H X	$BA_9\ BA_8 \cdots BA_1\ BA_0$ PC+1	L L	H	If Test Register 1 is LOW $BA_0 \cdot BA_9 \rightarrow PC$ If Test Register 1 is HIGH $PC+1 \rightarrow PC$
	BTL_2	Branch on T_2 LOW	H L H L	X L X X X H X X	$BA_9\ BA_8 \cdots BA_1\ BA_0$ PC+1	L L	H	If Test Register 2 is LOW $BA_0 \cdot BA_9 \rightarrow PC$ If Test Register 2 is HIGH $PC+1 \rightarrow PC$
	BTL_3	Branch on T_3 LOW	H L H H	L X X X H X X X	$BA_9\ BA_8 \cdots BA_1\ BA_0$ PC+1	L L	H	If Test Register 3 is LOW $BA_0 \cdot BA_9 \rightarrow PC$ If Test Register 3 is HIGH $PC+1 \rightarrow PC$
Miscellaneous Instructions	RTS	Return from Subroutine	L L L L	X X X X	Contents of the Stack Addressed by Read Pointer	L L	L	Pop the Stack
	FTCH	FETCH	L L H L	X X X X	PC+1	L L	L	$PC+1 \rightarrow PC$

L LOW Level
H HIGH Level
X Don't Care

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FUNCTIONAL DESCRIPTION – The 9408/A Microprogram Sequencers, shown in the block diagram consists of a 10-bit Program Counter (PC), a 4-word by 10-bit Last-In First-Out (LIFO) Stack with associated control, an Input Multiplexer, a Pipeline Multiplexer, an Instruction Decoder, a 10-bit Incrementer, and a 4-bit Test Register comprised of four edge-triggered D flip-flops.

The Pipeline Multiplexer has two ports – the PC output provides the input port for the non-pipeline mode and the Input Multiplexer output provides the input port for the pipeline mode. Port selection is controlled by the Pipeline Select (PLS) and Master Reset (MR) inputs. A LOW level on the MR input forces the non-pipeline mode of operation and clears the PC. Thus when the 9408/A are initialized by the MR input the A_0 through A_9 outputs are LOW regardless of the state of the PLS input. A LOW on the PLS input specifies non-pipeline mode and a HIGH specifies pipeline mode.

The Program Counter is a 10-bit edge-triggered register. The LOW-to-HIGH transition on the Clock (CP) input loads the Input Multiplexer output into the PC. Because of the edge-triggered nature of the PC register, the PC output remains static for a full clock cycle. Thus, in the non-pipeline mode, the PC output can be used to address a control memory built with static devices without storing the memory output in an external microinstruction register. However, in the pipeline mode, the 9408/A provide the next address information as soon as available; therefore, execution of a microinstruction can be overlapped with the fetching of the next microinstruction. To ensure microinstruction stability for a full clock cycle, the control-memory output should be buffered with an external microinstruction register.

The Input Multiplexer receives data from four different sources. One port is the output of the LIFO Stack; a second is the output of the 10-bit Incrementer. The Incrementer always adds one to the PC contents. The third and fourth ports are the branch and multiway-branch ports, the latter comprised of the seven most significant Branch Address inputs (BA_3 through BA_9) and the three Multiway inputs, (MW_0 through MW_2).

The 4-word by 10-bit LIFO Stack is a RAM and receives data from the Incrementer output. The stack control logic generates the appropriate control signals, while stack pointers in the Stack Control generate the read and write addresses.

The 4-bit Test Register consists of four type-D flip-flops. The data inputs, which are the four Test inputs (T_0 through T_3) are loaded on the LOW-to-HIGH transition of the Strobe input (STRB).

The Instruction Decoder receives the 4-bit Instruction input (I_0 through I_3) and the Test Register output and generates VIA_0, VIA_1 and Inhibit (INH) outputs of the 9408/A. In addition, it generates appropriate logic signals for the Stack Control and Input Multiplexer.

Stack Control – The 9408/A have a 4-level subroutine nesting capability as detailed in *Figure 1*. The R_0 and R_1 (Read Address) inputs to the 4-word by 10-bit LIFO Stack specify the address from which information will be read. The W_0 and W_1 (Write Address) inputs specify the address into which information will be written; and the 9408/A Increment output provides the information to be written into the stack (see block diagram). In addition, writing into the memory is controlled by the Write Enable ($\overline{WE}$) and $\overline{CP}$ inputs.

The R_0, R_1 and W_0, W_1 inputs of the LIFO Stack are derived from the outputs of a 3-bit edge-tirggered register called the Stack Pointer (SP). The least significant two bits (SP_0 and SP_1) of this register are the read address inputs to the memory. The SP outputs are also connected to a Stack-Pointer Incrementer and a Decrementer that generate SP + 1 and SP – 1 respectively. The least significant two bits of the Incrementer are the write address bits for the memory.

The outputs of the Incrementer, Decrementer and the Stack Pointer are fed as inputs to a 3-port Stack-Pointer Multiplexer which, in turn, feeds the Stack Pointer inputs. Stack pointer loading always occurs on the LOW-to-HIGH transition of the $\overline{CP}$ input. The $\overline{MR}$ input clears the Stack Pointer. The stack Pointer Control receives two inputs from the 9408/A instruction Decoder – the BSR input, which is active whenever a Branch-to-Subroutine (BSR) instruction is present on the I_0 through I_3 inputs, and the RTS input, which is active whenever a Return-from-Subroutine (RTS) instruction is specified. The port selection of the Stack Pointer Multiplexer is controlled by the outputs of the Stack Pointer Control. For all 9408/A instructions except BSR and RTS, the Stack Pointer Multiplexer selects the Stack Pointer outputs as the instruction source.

Writing into the memory takes place whenever the $\overline{WE}$ and $\overline{CP}$ inputs are LOW. Note that the most significant register bit, SP_2, controls the $\overline{WE}$ input to prevent writing into the memory when all four locations are filled with return addresses. Thus the 9408/A do not store and return addresses beyond four nesting levels.

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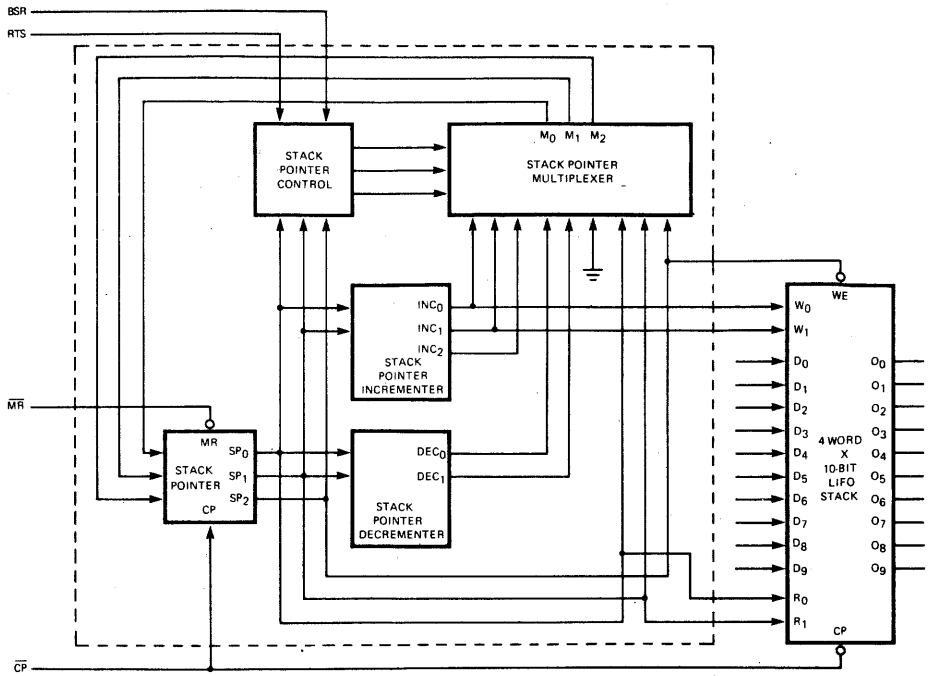


Fig. 1
STACK CONTROL

9408/A INSTRUCTIONS

The 9408/A instruction set have 16 instructions (*Table 1*). These instructions can be divided into three groups – unconditional branches, conditional branches and miscellaneous – and are specified by appropriate logic levels on the $I_0 - I_3$ inputs.

The unconditional branch group consists of four Branch VIA instructions ($BRV_0 - BRV_3$), Branch Multiway (BMW) and Branch to Subroutine (BSR). This group requires that the next address be explicitly specified on the BA inputs.

The conditional branch group consists of eight instructions, Branch Test HIGH ($BTH_0 - BTH_3$) and Branch Test LOW ($BTL_0 - BTL_3$), for interrogating the four test flip-flops of the 9408/A individually. The $BTH_0 - BTH_3$ instructions test flip-flops $T_0 - T_3$ respectively for a HIGH on the Q output (see block diagram). Similarly $BTL_0 - BTL_3$ test for a LOW on the corresponding Q input. If the test condition is satisfied, the next address is taken from the Branch ($BA_0 - BA_9$) inputs. If the test condition is not satisfied the 9408/A perform a Fetch operation.

The miscellaneous group consists of two instructions – Fetch (FTCH) and Return from Subroutine (RTS). These instructions do not require explicit specification of the next address. For the FTCH instruction, the next address is assumed to be the address of the current microinstruction + 1. For RTS, the next address is taken from the Stack. *The Inhibit (INH) outputs of the 9408/A are LOW only for FTCH and RTS instructions. For all other instructions, the INH output is HIGH.*

The VIA outputs of the 9408/A (VIA_0, VIA_1) are LOW for all instructions except $BRV_1 - BRV_3$. For BRV_1, the VIA_0 is HIGH and VIA_1 LOW. For BRV_2, the VIA_0 is LOW and VIA_1 HIGH. For BRV_3, both VIA_0 and VIA_1 are HIGH.

Unconditional Branches

$BRV_0 - BRV_3$ – Whenever a Branch VIA instruction code is present on the $I_0 - I_3$ inputs, the Instruction Decoder (see block diagram) establishes the appropriate HIGH/LOW pattern on the VIA_0 and VIA_1 outputs per *Table 1*. The Instruction Decoder also forces the INH output HIGH. Moreover, the $BA_0 - BA_9$ inputs are selected as the source of the next address by the Input Multiplexer.

If the 9408/A are in the pipeline mode (PLS input HIGH), the Pipeline Multiplexer transfers the $BA_0 - BA_9$ inputs to the $A_0 - A_9$ outputs. The $BA_0 - BA_9$ inputs are loaded into the PC on the LOW-to-HIGH transition of the CP input. On the other hand, if the non-pipeline mode of operation is selected, the $BA_0 - BA_9$ inputs appear on the output only after the LOW-to-HIGH transition of the CP input.

BMW – For a Branch Multiway instruction, the Instruction Decoder forces the VIA_0 and VIA_1 outputs LOW and INH output HIGH. The Input Multiplexer selects the $BA_3 - BA_9$ inputs as the most significant seven bits and $MW_0 - MW_2$ inputs as the least significant three bits of the next address. If the pipeline mode of operation is selected, the next address formed by the Input Multiplexer ($BA_3 - BA_9$ and $MW_0 - MW_2$ inputs) is transferred to the $A_0 - A_9$ outputs. On the LOW-to-HIGH transition of the CP input, this next address is also leaded into the PC. For non-pipeline mode, the next address is available on the $A_0 - A_9$ output only after the CP transition.

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BSR – During a Branch-to-Subroutine instruction, the Instruction Decoder forces a LOW on the VIA_0 and VIA_1 outputs and a HIGH on the INH output. The Input Multiplexer selects the BA_0 – BA_9 inputs as the source for the next address. If the pipeline mode is selected, this next address is transferred to the A_0 – A_9 outputs by the Pipeline Multiplexer. As usual, the PC is updated with this next address on the LOW-to-HIGH transition of the CP input. During non-pipeline operation, the next address appears on the output only after the CP transition.

The PC holds the address of the current microinstruction. For the BSR instruction, the return address must be stored in the Stack, which is fed by the PC through an Incrementer (see block diagram). When the CP input is LOW, the incremented value is written into the Stack as a return address. The LOW-to-HIGH transition of the CP input not only loads the PC with the next address, *i.e.*, BA_0 – BA_9 inputs, but also increments the Stack Pointer as explained above.

Conditional Branches

BTH_0 – BTH_3 – For a Branch Test HIGH instruction, the Instruction Decoder establishes a LOW on VIA_0 and VIA_1 outputs and HIGH on the INH output. It then tests for a HIGH on the Q output of the corresponding flip-flop in the test register. If a HIGH level is found, the Input Multiplexer selects the BA_0 – BA_9 inputs as the source for the next address.

On the other hand, if the tested Q output of the flip-flop is LOW, the Incrementer output is selected as the source of the next address by the Input Multiplexer. In either case, the PC is loaded with the next address on the LOW-to-HIGH transition of the CP input. As usual, if the pipeline mode is selected, the next address is transferred to the A_0 – A_9 outputs. For non-pipeline mode, the next address appears on the output after the clock transition.

BTL_0 – BTL_3 – Operation of the Branch Test LOW instructions is identical to BTH_0 – BTH_3 except that Q outputs of the test register flip-flops are tested for a LOW. If the tested output is LOW, a branch occurs. If tested output is HIGH the Incrementer output is the next address.

Miscellaneous

FTCH – For a Fetch instruction, the Instruction Decoder establishes a LOW on the VIA_0 and VIA_1 outputs. In addition, the INH output is also LOW. The Input Multiplexer selects the Incrementer output as the next address. If pipeline mode is selected, the Incrementer output is transferred to the A_0 – A_9 outputs. For non-pipeline mode, the incremented address appears at the output only after the clock transition.

RTS – For a Return-from-Subroutine instruction, the Instruction Decoder establishes a LOW on the VIA_0, VIA_1 and the INH outputs. The Input Multiplexer selects the Stack output as the source of the next address. As usual, for the pipeline mode, the next address is transferred to the output by the Pipeline Multiplexer. For non-pipeline operation, the next address appears on the output only after the clock transition. In addition, this instruction also decrements the Stack Pointer as described above.

DC CHARACTERISTICS: (Over Operating Temperature Range unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP (2)	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.4			
V_{OL}	Output LOW Voltage			0.25	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current, All except CP, I_0, I_2, I_3			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Input HIGH Current, CP, I_0, I_2, I_3			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Input HIGH Current, All Inputs				1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current, All except CP, I_0, I_2, I_3			0.21	0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	Input LOW Current, CP, I_0, I_2, I_3			0.42	0.72		
I_{OS}	Output Short Circuit Current, Q_0–Q_3, Q_S		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 (Note 3)
I_{CC}	Supply Current			130		mA	V_{CC} = MAX, MR LOW

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

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AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

SYMBOL	PARAMETER	9408 LIMITS			9408/A LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
t_{PHH}	Propagation Delay,		35	60		35	46	ns	I_1, I_2 HIGH, I_3 LOW
t_{PLL}	Instruction to VIA		35	50		35	44	ns	I_0 = Input, VIA_0 = Output
t_{PHH}	Propagation Delay,		35	50		35	44	ns	I_1 HIGH, I_2, I_3 LOW
t_{PLL}	Instruction to INHIBIT		35	48		35	44	ns	I_0 = Input, I_{NH} = Output
t_{PHH}	Propagation Delay, Positive		45	68		45	52	ns	I_1 HIGH, PL, I_0, I_2, I_3 LOW
t_{PHL}	Going CP to Any A (Non-Pipeline)		52	74		52	64	ns	
t_{PHH}	Propagation Delay, Positive		98	156		98	110	ns	PL, I_1 HIGH,
t_{PHL}	Going CP to Any A (Pipeline)		98	166		98	110	ns	I_0, I_2, I_3 LOW
t_{PHH}	Propagation Delay,		22	26		22	26	ns	PL, I_0, I_1, I_2 HIGH
t_{PLL}	BA to A (Pipeline)		28	44		28	38	ns	I_3 LOW
t_{PHH}	Propagation Delay,		72	120		72	94	ns	I_0, I_1, BA_0, PL HIGH I_3, MW_0 LOW, A_0 = Output
t_{PLL}	Instruction to Any A (Pipeline)		72	110		72	94	ns	I_2 = Input, A_0 = Output
t_{PWH}	Min CP Pulse Width (HIGH)	40	18		30	18		ns	I_1 HIGH
t_{PWL}	Min CP Pulse Width (LOW)	40	30		35	30		ns	I_0, I_2, I_3, PL LOW
t_s	Set-up Time, BA to CP		15	35		15	25	ns	I_2 HIGH, I_0, I_1, I_3, PL LOW BA_0 = Input, A_0 = Output
t_h	Hold Time, BA to CP		5	10		5	10	ns	I_2 HIGH, I_0, I_1, I_3 PL LOW BA_0 = Input, A_0 = Output
t_s	Set-up Time, Instruction to CP		90	135		90	95	ns	I_0, I_1, BA_0 HIGH I_3, MW_0, PL LOW
t_h	Hold Time, Instruction to CP		−20	0		−20	0	ns	I_2 = Input, A_0 = Output
t_s	Set-up Time, Strobe to CP (Required to achieve conditional branch in the same microcycle)		60	115		60	85	ns	I_3, $TEST_0$ HIGH I_0, I_1, I_2, PL, BA_0 LOW Strobe = Input, A_0 = Output
t_s	Set-up Time, Test to Strobe		5	15		5	15	ns	I_2, I_3, PL HIGH I_0, I_1, BA_0 LOW $TEST_0$ = Input, A_0 = Output
t_h	Hold Time, Test to Strobe		15	20		15	20	ns	I_2, I_3, PL HIGH I_0, I_1, BA_0 LOW $TEST_0$ = Input, A_0 = Output
t_{rec}	Recovery Time, MR to CP		20	40		20	30	ns	

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION

Preliminary

HM-6100

Low Power CMOS 12-Bit Microprocessor

Features

DESIGN

- Silicon Gate Complementary MOS
- Fully Static-0 to 8 MHz
- Single Power Supply
  - HM-6100/6100C V_{CC} = 5 volts
  - HM-6100A V_{CC} = 10 volts
- Crystal Controlled On Chip Timing
- Low Power Dissipation <10mW @ 4MHz @ 5 volts
- Wide Power Supply $4V \leq V_{CC} \leq 11V$
- TTL Compatible at 5 volts
- Excellent Noise Immunity
- -55°C to +125°C Operation

ARCHITECTURAL

- Executes PDP-8/E, Instruction Set
- Direct, Indirect, and Autoindexed Memory Addressing
- 12-Bit Memory Accumulator ADD Instruction
  - HM-6100 5 μsec @ +5 volts/4.0 MHz
  - HM-6100A 2.5 μsec @ +10 volts/8.0 MHz
  - HM-6100C 6 μsec @ +5 volts/3.3 MHz
- Input-Output Instruction
  - HM-6100 8.5 μsec @ +5 volts/4.0 MHz
  - HM-6100A 4.25 μsec @ +10 volts/8 MHz
  - HM-6100C 10.2 μsec @ +5 volts/3.3 MHz
- Single-Clock, Single-Instruction Capability
- Direct Memory Access (DMA)
- Interrupt
- Dedicated Control Panel Features

INTERFACE

- Memory – Any Speed, by Using WAIT Line
- Control Panel
- Switch Register
- Asynchronous CPU – Memory and CPU – Device Communication
- 63 I/O Devices with PDP-8/E Compatible Interface
- Device Controlled Input-Output
- All Control Signals Produced by the CPU

Applications

- Intelligent Computer Terminals
- POS Terminals
- Portable Terminals
- Aerospace/Satellite Systems
- Automotive Systems
- Remote Data Acquisition Systems
- Process Control
- Instrumentation
- Medical Electronics
- Displays
- Traffic Control
- Navigation

Description

The HM-6100 is a single address, fixed word length, parallel transfer microprocessor using 12-bit, two's complement arithmetic. The processors recognize the instruction set of Digital Equipment Corporation's PDP8/E minicomputer. The internal circuitry is completely static and is designed to operate at any speed between DC and the maximum operating frequency. Two pins are available to allow for an external crystal thereby eliminating the need for clock generators and level translators. The crystal can be removed and the processor clocked by an external clock generator. A 12-bit memory-accumulator ADD instruction, using a +5 volt supply, is performed in 5 μsec by the HM-6100, in 6 μsec by the HM-6100C and in 2.5 μsec by the HM-6100A using a +10 volt supply. The device design is optimized to minimize the number of external components required for interfacing with standard memory and peripheral devices.

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Preliminary

HD-6402

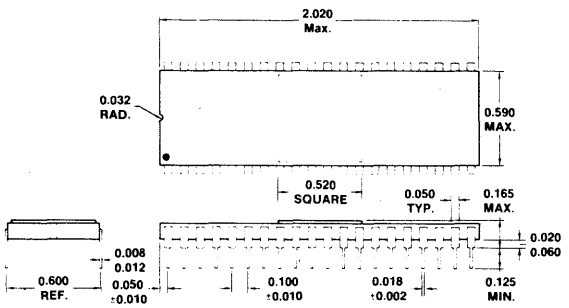
CMOS/LSI Universal Asynchronous Receiver (UART)

Features

- OPERATION FROM D.C. TO 2.0MHz
- LOW POWER – TYP 5mW @ 2.0MHz
- 4V – 11V OPERATION
- PROGRAMMABLE WORD LENGTH, STOP BITS AND PARITY
- AUTOMATIC DATA FORMATTING AND STATUS GENERATION
- COMPATIBLE WITH INDUSTRY STANDARD UARTs
- SINGLE POWER SUPPLY

Package

40 PIN D.I.P.

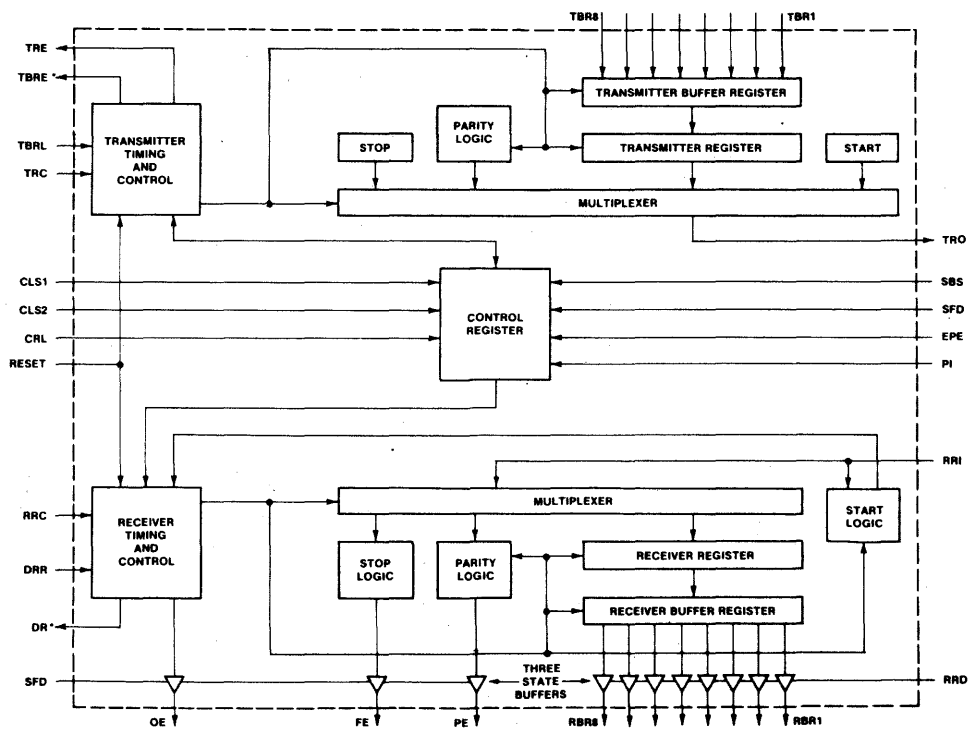


Description

The HD-6402 is a CMOS/LSI subsystem for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits to parallel data, verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one, two or one and one-half when transmitting 5 bit code.

The HD-6402 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. CMOS/LSI technology permits operating clock frequencies up to 2.0MHz (125K Baud) an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 300mW to 5mW. Status logic increases flexibility and simplifies the user interface.

Functional Block Diagram



* These outputs are three state.

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION

Preliminary

HD-6101

CMOS Parallel Interface Element

Features

- HM-6100 COMPATIBLE
- LOW POWER – TYP. < 5.0μW STANDBY
- 4 – 11 VOLT SUPPLIES
- HIGH SPEED
- STATIC OPERATION

Description

The HD-6101 Parallel Interface Element (PIE) is a high speed, low power, silicon gate CMOS general purpose device which provides addressing, interrupt and control for a variety of peripheral functions, such as UARTs, FIFOs, Keyboards, etc. The PIE is designed to eliminate external logic. Data transfers between the HM-6100 CMOS Microprocessor and the HD-6101 are via IOT instructions, control lines and DX bus.

Data transfers between peripheral devices and the DX bus are controlled by the PIE via 2 read, 2 write, 4 sense and 4 flag functions. The A and B registers program write polarities, sense polarities, sense levels or edges, flag values and interrupt enables. The vector register has 10 bits writeable from the HM-6100 and 2 bits indicating the highest priority SENSE input that generated the interrupt.

Functions

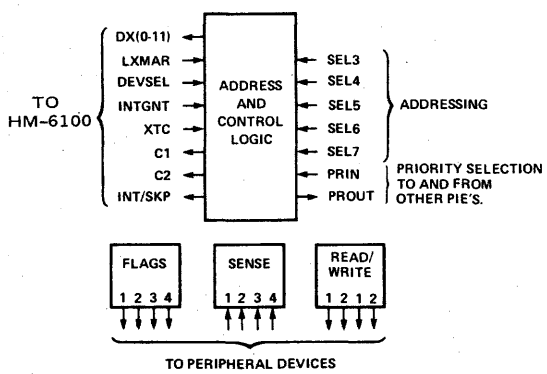
- UNIVERSAL I/O PERIPHERAL CONTROLLER
- VECTORED PRIORITY INTERRUPT
- SET AND SENSE EXTERNAL FLAGS AND CONDITIONS VIA SOFTWARE

Instructions

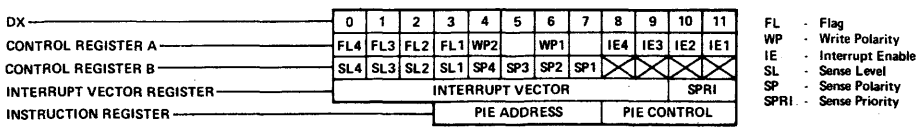
1000 – READ 2	0000 – READ 1
1001 – WRITE 2	0001 – WRITE 1
1010 – SKIP 3	0010 – SKIP 1
1011 – SKIP 4	0011 – SKIP 2
1100 – WVR	0100 – RCRA
1101 – WCRB	0101 – WCRA
1110 – SFLAG 3	0110 – SFLAG 1
1111 – CFLAG 3	0111 – CFLAG 1

6007 – CAF (Internal IOT) clears interrupt requests

Functional Diagram



Register Bit Assignments



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HARRIS SEMICONDUCTOR PRODUCTS DIVISION

HD-4702/6405

Programmable Bit Rate Generator

FEATURES

- HD-4702 – PROVIDES 13 COMMONLY USED BIT RATES
- HD-6405 – PROVIDES 15 COMMONLY USED BIT RATES
- USES A 2.4576MHz CRYSTAL/INPUT FOR STANDARD FREQUENCY OUTPUT (16 TIMES BIT RATE)
- TTL COMPATIBLE – OUTPUT WILL SINK 1.6mA
- LOW POWER DISSIPATION HD-6405 4.0mW TYP. @ 2.4576MHz HD-4702 4.5mW TYP. @ 2.4576MHz
- CONFORMS TO EIA RS-404
- ONE HD-4705 OR HD-6405 CONTROLS UP TO EIGHT TRANSMISSION CHANNELS
- INITIALIZATION CIRCUIT FACILITATES DIAGNOSTIC FAULT ISOLATION
- ON-CHIP INPUT PULL-UP CIRCUIT – HD-4702 ONLY

DESCRIPTION

The HD-4702/6405 Bit Rate Generator provides the necessary clock signals for digital data transmission systems, such as UART. It generates 13(HD-4702) or 15(HD-6405) commonly used bit rates using an on-chip crystal oscillator or an external input. For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576MHz (i.e. 9600 Baud x 16 x 16, since there is an internal ÷16 prescaler). A lower input frequency will result in a proportionally lower output frequency.

The HD-4702/6405 can provide multi-channel operation with a minimum of external logic by having the clock frequency CO and the ÷ 8 prescaler outputs Q_0, Q_1, and Q_2 available externally. All signals have a 50% duty cycle except 1800 Baud and 2000 Baud which has less than 0.39% distortion and 3600 Baud which has less than 0.78% distortion.

The four rate select inputs (S_0-S_3) select which bit rate is at the output (Z). The table lists select code and output bit rate. Two of the 16 for the HD-4702 and one of the 16 for the HD-6405 do not select an internally generated frequency, but select an input into which the user can feed either a different frequency, or a static level (High or Low) to generate "ZERO BAUD".

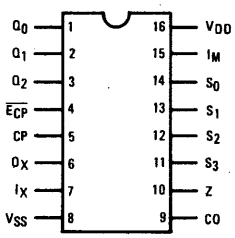
The bit rate most commonly used in modern data terminals (110, 150, 300, 1200, 2400 Baud) require that no more than one input be grounded for the HD-4702, which is easily achieved with a single, 5-position switch.

The HD-4702/6405 has an initialization circuit which generates a common master reset for all flip-flops. This signal is derived from a digital differentiator that senses the first high level on the CP input after the $\overline{E_{CP}}$ input goes low. When $\overline{E_{CP}}$ is high, selecting the crystal input, CP must be low. A high level on CP would apply a continuous reset.

For the HD-4702, all inputs except I_X have on-chip pull-up circuits which provide TTL compatibility and eliminate the need to tie a permanently high input to V_{DD}.

PINOUT

CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

CP	External Clock Input
$\overline{E_{CP}}$	External Clock Enable Input (Active LOW)
I_X	Crystal Input
I_M	Multiplexed Input
S_0-S_3	Rate Select Inputs
CO	Clock Output
O_X	Crystal Drive Output
Q_0-Q_2	Scan Counter Outputs
Z	Bit Rate Output

NOTE:
The Flatpack version has the same pinouts (Connection Diagram) as the Dual-In-Line Package.

TRUTH TABLES

TABLE 1
CLOCK MODES AND INITIALIZATION

I_X	E_{CP}	CP	OPERATION
∿∿	H	L	Clocked from I_X
X	L	∿∿	Clocked from CP
X	H	H	Continuous Reset
X	L	⎍	Reset During First CP = HIGH Time

H = HIGH Level
L = LOW Level
X = Don't care
⎍ = 1st HIGH Level Clock Pulse after E_{CP} goes LOW
∿∿ = Clock Pulse

NOTE: Actual output frequency is 16 times the indicated Output Rate, assuming a clock frequency of 2.4576MHz.

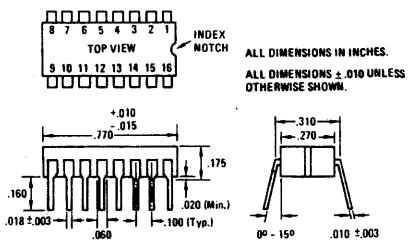
TABLE 2
TRUTH TABLE FOR RATE SELECT INPUTS

S_3	S_2	S_1	S_0	OUTPUT RATE (Z) HD-4702	OUTPUT RATE (Z) HD-6405
L	L	L	L	MIXED INPUT(I_M)	MIXED INPUT(I_M)
L	L	L	H	MIXED INPUT(I_M)	2000 BAUD
L	L	H	L	50 BAUD	50 BAUD
L	L	H	H	75 BAUD	75 BAUD
L	H	L	L	134.5 BAUD	134.5 BAUD
L	H	L	H	200 BAUD	200 BAUD
L	H	H	L	600 BAUD	600 BAUD
L	H	H	H	2400 BAUD	3600 BAUD
H	L	L	L	9600 BAUD	9600 BAUD
H	L	L	H	4800 BAUD	4800 BAUD
H	L	H	L	1800 BAUD	1800 BAUD
H	L	H	H	1200 BAUD	1200 BAUD
H	H	L	L	2400 BAUD	2400 BAUD
H	H	L	H	300 BAUD	300 BAUD
H	H	H	L	150 BAUD	150 BAUD
H	H	H	H	110 BAUD	110 BAUD

PACKAGING

16 LEAD CERDIP

Available in Cerdip and Epoxy Dual-In-Line packages.



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Ouput Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-4702-9/6405-9	-40°C to +85°C
Military HD-4702-2/6405-2	-55°C to +125°C
Operating Voltage Range	+4V to +7V

ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±10%: T_A = -40°C to +85°C(-9); T_A = -55°C to +125°C(-2)

D.C.

PARAMETER	SYMBOL	HD-4702-2/6402-2 MIN	TYP	MAX	HD-4702-9/6405-9 MIN	TYP	MAX	UNITS	TEST CONDITIONS
Input High Voltage	V_{IH}	V_{CC} -1.5			V_{CC} -1.5			V	
Input Low Voltage	V_{IL}			1.5			1.5	V	
Output High Voltage	V_{OH1}	V_{CC} -.05			V_{CC} -.05			V	I_{OH} -1μA
Output Low Voltage	V_{OL1}			0.05			0.05	V	I_{OI} +1μA
Input High Current	I_{IH}	-1		+1	-1		+1	μA	V_I = VDD, All other pins = 0V
Input HD- 4702 (all inputs LOW except IX)	I_{IL}[1]		-30	-50		-30	-50	μA	
CURRENT IX Input	I_{ILX}	-1		+1	-1		+1	μA	V_I = 0, All other pins = V_{DD}
HD-6405 - All pins	I_{IL}	-1		+1	-1		+1	μA	
OUTPUT OX HIGH (all other outputs)	I_{OHX}	-0.1			-0.1			mA	V_{OUT} = V_{CC} -.5
	I_{OH1}	-1.0			-1.0			mA	V_{OUT} = 2.5V
CURRENT (all other outputs)	I_{OH2}	-0.3			-0.3			mA	V_{OUT} = V_{CC} -.5
									Input at 0 or V_{DD} per Logic Function or Truth Table
OUTPUT OX LOW	I_{OLX}	0.1			0.1			mA	V_{OUT} = .4V
CURRENT (all other outputs)	I_{OL}	1.6			1.6			mA	V_{OUT} = .4V
SUPPLY CURRENT HD-4702	I_{CC}			500			1500	μA	$\overline{E_{CP}}$ = V_{DD}, CP = 0, All other inputs = GND
HD-4702				150			1000	μA	$\overline{E_{CP}}$ = V_{DD}, CP = 0, All other inputs = V_{DD}
HD-6405				150			150	μA	$\overline{E_{CP}}$ = V_{DD}, CP = 0, All other inputs = V_{DD} or GND

ELECTRICAL CHARACTERISTICS V_{CC} = 5V; T_A = 25°C

A.C.

PARAMETER	SYMBOL	HD-4702-2/6405-2 MIN	TYP	MAX	HD-4702-9/6405-9 MIN	TYP	MAX	UNITS	TEST CONDITIONS
Propagation Delay, I_X to CO	t_{PLH}			300			300	ns	$C_L \leq 7pf$ on OX
	t_{PHL}			250			250	ns	
Propagation Delay, CP to CO	t_{PLH}			215			215	ns	C_L = 15pF Input Transition Times ≤ 20ns
	t_{PHL}			195			195	ns	
Propagation Delay, CO to O_n	t_{PLH}			(5)			(5)	ns	
	t_{PHL}							ns	
Propagation Delay, CO to Z	t_{PLH}			75			75	ns	
	t_{PHL}			65			65	ns	
Output Transition Time (except OX)	t_{TLH}			80			80	ns	
	t_{THL}			40			40	ns	
Propagation Delay, I_X to CO	t_{PLH}			350			350	ns	$C_L \leq 7pF$ on OX
	t_{PHL}			275			275	ns	
Propagation Delay, CP to CO	t_{PLH}			260			260	ns	C_L = 50pF Input Transition Times ≤ 20ns
	t_{PHL}			220			220	ns	
Propagation Delay, CO to O_n	t_{PLH}			(5)			(5)	ns	
	t_{PHL}							ns	
Propagation Delay, CO to Z	t_{PLH}			85			85	ns	
	t_{PHL}			75			75	ns	
Output Transition Time (except OX)	t_{TLH}			160			160	ns	
	t_{THL}			75			75	ns	
Set-Up Time, Select to CO	t_s	350			350			ns	$C_L \leq 7pF$ on OX
Hold Time, Select to CO	t_h	0			0			ns	
Set-Up Time, I_M to CO	t_s	350			350			ns	C_L = 15pF Input Transition Times ≤ 20ns
Hold Time, I_M to CO	t_h	0			0			ns	
Minimum Clock Pulse-Width Low and High	$t_{WCP(L)}$	120			120			ns	
	$t_{WCP(H)}$	0			0			ns	
Minimum I_X Pulse Width, Low and High	$t_{WCP(L)}$	160			160			ns	
	$t_{WCP(H)}$	160			160			ns	

1. Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull-up circuits on all inputs except I_X. This is done for TTL compatibility.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transistion Times (t_{TLH} and t_{THL}) will change with Ouput Load Capacitance (C_L). Set-Up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
3. The first High Level Clock Pulse after $\overline{E_{CP}}$ goes Low must be at least 350ns long to guarantee reset of all Counters.
4. It is recommended that input rise and fall times to the Clock Inputs (CP, I_X) be less than 15ns.
5. For multichannel operation, Propagation Delay (CO to ON) plus Set-Up Time, Select to CO, is guaranteed to be ≤ 307ns.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -.05V to V_{CC} +0.5V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-4702A-9/6405A-9	-40°C to +85°C
Military HD-4702A-2/6405A-2	-55°C to +125°C
Operating Voltage Range	+4V to +11V

ELECTRICAL CHARACTERISTICS V_{CC} = 10V ±10%; T_A = -40°C to +85°C(-9); T_A = -55°C to +125°C(-2)

D.C.

PARAMETER	SYMBOL	HD-4702A/6405A-2 MIN	TYP	MAX	HD-4702A/6405A-9 MIN	TYP	MAX	UNITS	TEST CONDITIONS
Input High Voltage	V_{IH}	70% V_{CC}						V	
Input Low Voltage	V_{IL}			20% V_{CC}			20% V_{CC}	V	
Output High Voltage	V_{OH1}	V_{CC} -.1			V_{CC} -.1			V	$I_{OH} \leq -1\mu A$
Output Low Voltage	V_{OL1}	GND +.1			GND +.1			V	$I_{OL} \leq +1\mu A$
Input High Current	I_{IH}	-1		+1	-1		+1	μA	$V_I = V_{DD}$, All other pins = 0V
INPUT HD-4702 (All inputs LOW except I_X)	I_{IL1}		-110	-170		-110	-170	μA	
CURRENT I_X inputs	I_{ILX}	-1		+1	-1		+1	μA	V_I = 0 All other pins = V_{DD}
HD-6405 – All pins	I_{IL}	-1		10	-1		10	μA	
OUTPUT OX HIGH	I_{OHX}	0.2			0.2			mA	V_{OUT} = 9.5V; Input at 0 or V_{DD} per Logic Function or Truth Table
CURRENT(All other outputs)	I_{OH2}	0.6			0.6			mA	V_{OUT} = 9.5V
OUTPUT OX LOW	I_{OLX}	0.2			0.2			mA	V_{OUT} = .5V
CURRENT (All other outputs)	I_{OL}	3.2			3.2			mA	V_{OUT} = .5V
SUPPLY CURRENT HD-4702A				1000			3000	μA	$\overline{ECP}$ = V_{DD}, CP = 0, All other inputs = GND
HD-4702A				500			1000	μA	$\overline{ECP}$ = V_{DD}, CP = 0, All other inputs = V_{DD}
HD-6405A				500			500	μA	$\overline{ECP}$ = V_{DD}, CP = 0, All other inputs = V_{DD} or GND

ELECTRICAL CHARACTERISTICS V_{CC} = 10V; T_A = 25°C

A.C.

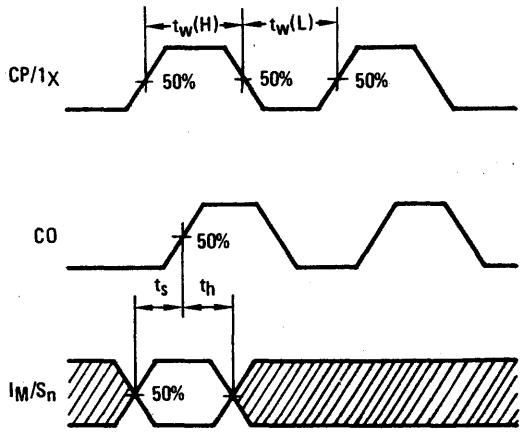
PARAMETERS	SYMBOL	HD-4702A/6405A-2 MIN	TYP	MAX	HD-4702A/6405A-9 MIN	TYP	MAX	UNITS	TEST CONDITIONS
Propagation Delay, I_X to CO	t_{PLH} t_{PHL}			150 125			150 125	ns ns	$C_L \leq 7pF$ on OX
Propagation Delay, CP to CO	t_{PLH} t_{PHL}			110 100			110 100	ns ns	C_L = 15pF Input Transition Times ≤ 20ns
Propagation Delay, CO to O_n	t_{PLH} t_{PHL}			(5)			(5)	ns ns	
Propagation Delay, CO to Z	t_{PLH} t_{PHL}			40 35			40 35	ns ns	
Output Transition Time (except OX)	t_{TLH} t_{THL}			40 20			40 20	ns ns	
Propagation Delay, I_X to CO	t_{PLH} t_{PHL}			175 140			175 140	ns ns	$C_L \leq 7pF$ on OX
Propagation Delay, CP to CO	t_{PLH} t_{PHL}			130 110			130 110	ns ns	C_L = 50pF Input Transition Times ≤ 20ns
Propagation Delay, CO to O_n	t_{PLH} t_{PHL}			(5)			(5)	ns ns	
Propagation Delay, CO to Z	t_{PLH} t_{PHL}			45 40			45 40	ns ns	
Output Transition Time (except OX)	t_{TLH} t_{THL}			80 40			80 40	ns ns	
Set-Up Time, Select to CO	t_s	175			175			ns	$C_L \leq pF$ on OX
Hold Time, Select to CO	t_h	0			0			ns	
Set-Up Time, I_M to CO	t_s	175			175			ns	C_L = 15pF Input Transition Times ≤ 20ns
Hold Time, I_M to CO	t_h	20			20			ns	
Minimum Clock Pulse Width Low and High	$t_{w}CP(L)$ $t_{w}CP(H)$	60 0			60 0			ns ns	
Minimum I_X Pulse Width, Low and High	$t_{w}CP(L)$ $t_{w}CP(H)$	80 80			80 80			ns ns	

1. Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull-up circuits on all inputs except I_X. This is done for TTL compatibility.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Ouput Load Capacitance (C_L). Set-Up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
3. The first High Level Clock Pulse after $\overline{ECP}$ goes Low must be at least 350ns long to guarantee reset of all Counters.
4. It is recommended that input rise and fall times to the Clock Inputs (CP, I_X) be less than 15ns.
5. For mulitchannel operation, Propagation Delay (CO to ON) plus Set-Up Time, Select to CO, is guaranteed to be ≤ 150ns.

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SWITCHING WAVEFORMS

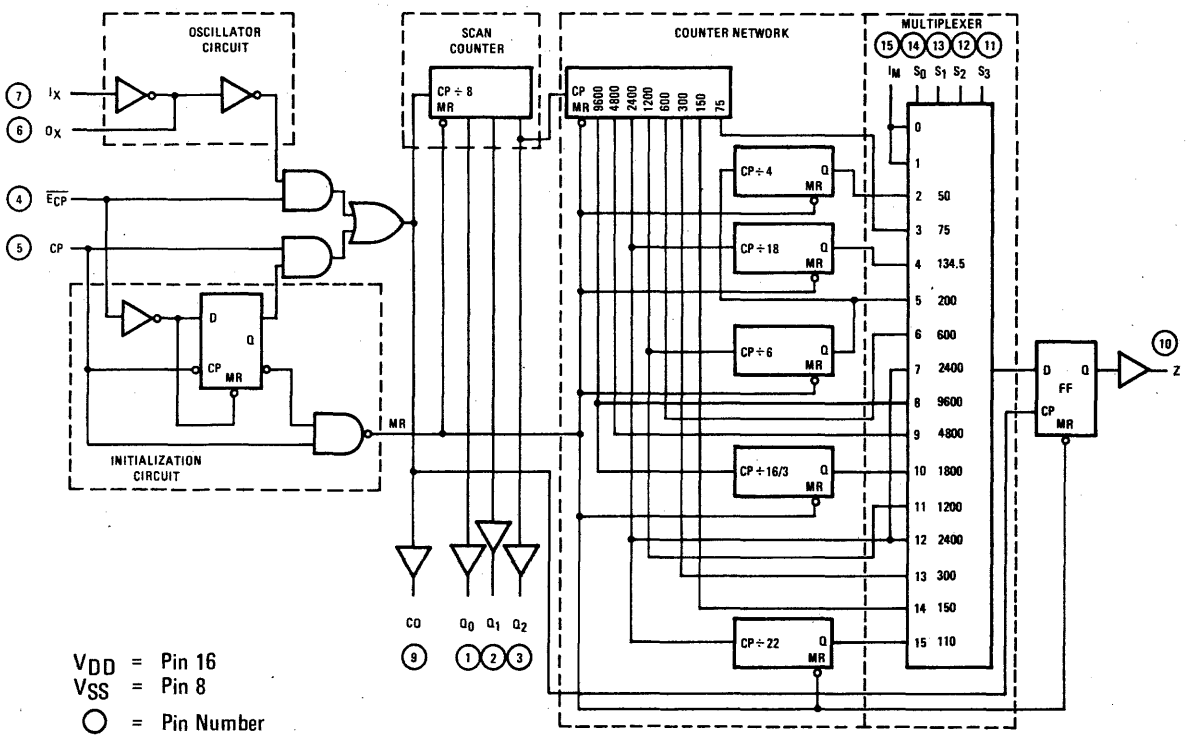
NOTE: Set-Up and Hold Times are shown as positive values but may be specified as negative values.



MINIMUM CP AND I_X PULSE WIDTHS AND SET-UP AND HOLD TIMES, SELECT INPUT (S_n) TO CLOCK OUTPUT (CO) AND I_M INPUT TO CLOCK OUTPUT (CO)

BLOCK DIAGRAM

HD-4702 Only



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SINGLE CHANNEL BIT RATE GENERATOR

Figure 1 shows the simplest application of the HD-4702/6405. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The Bit Rate Output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 110, 150, 300, 1200, and 2400 or 3600 Baud. For many low cost terminals these five bit rates are adequate.

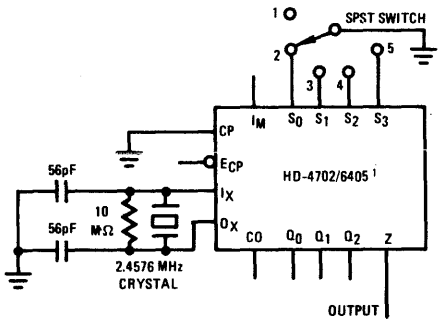
SIMULTANEOUS GENERATION OF SEVERAL BIT RATES

Fixed Programmed Multichannel Operation

Figure 2 shows a simple scheme that generates eight bit rates on eight output lines, using one HD-4702/6405 and one 93L34 Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs. As shown in the block diagram, these outputs (Q_0 to Q_2) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter Outputs back to the Select Inputs of the mulitplexer causes the HD-4702/6405 to interrogate sequentially the state of eight different frequency signals. The 93L34 8-Bit Addressable Latch, addressed by the same Scan Counter Outputs, reconverts the multiplexed single Output (Z) of the HD-4702/6405 into eight parallel output frequency signals. In the simple scheme of Figure 2, input S_3 is left open (HIGH) and the following bit rates are generated:

Q_0: 110 Baud Q_1: 9600 Baud Q_2: 4800 Baud
Q_3: 1800 Baud Q_4: 1200 Baud Q_5: 2400 Baud
Q_6: 300 Baud Q_7: 150 Baud

Other bit rate combinations can be generated by changing the Scan Counter to Selector interconnection or by inserting logic gates into this path.



SWITCH POSITION	HD-4702 BIT RATE	HD-6405 BIT RATE
1	110 Baud	110 Baud
2	150 Baud	150 Baud
3	300 Baud	300 Baud
4	1200 Baud	1200 Baud
5	2400 Baud	3600 Baud

Figure 1
SWITCH SELECTABLE BIT RATE GENERATOR CONFIGURATION PROVIDING FIVE BIT RATES

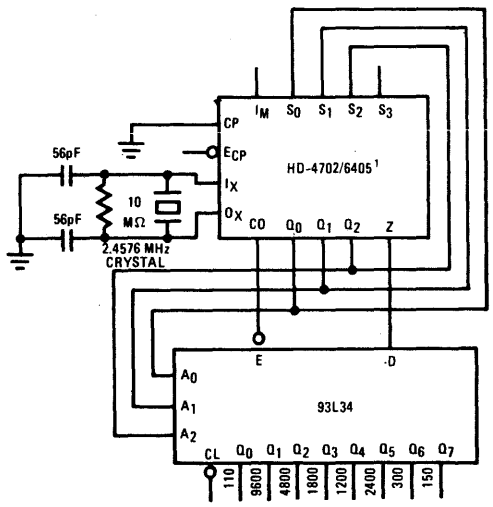


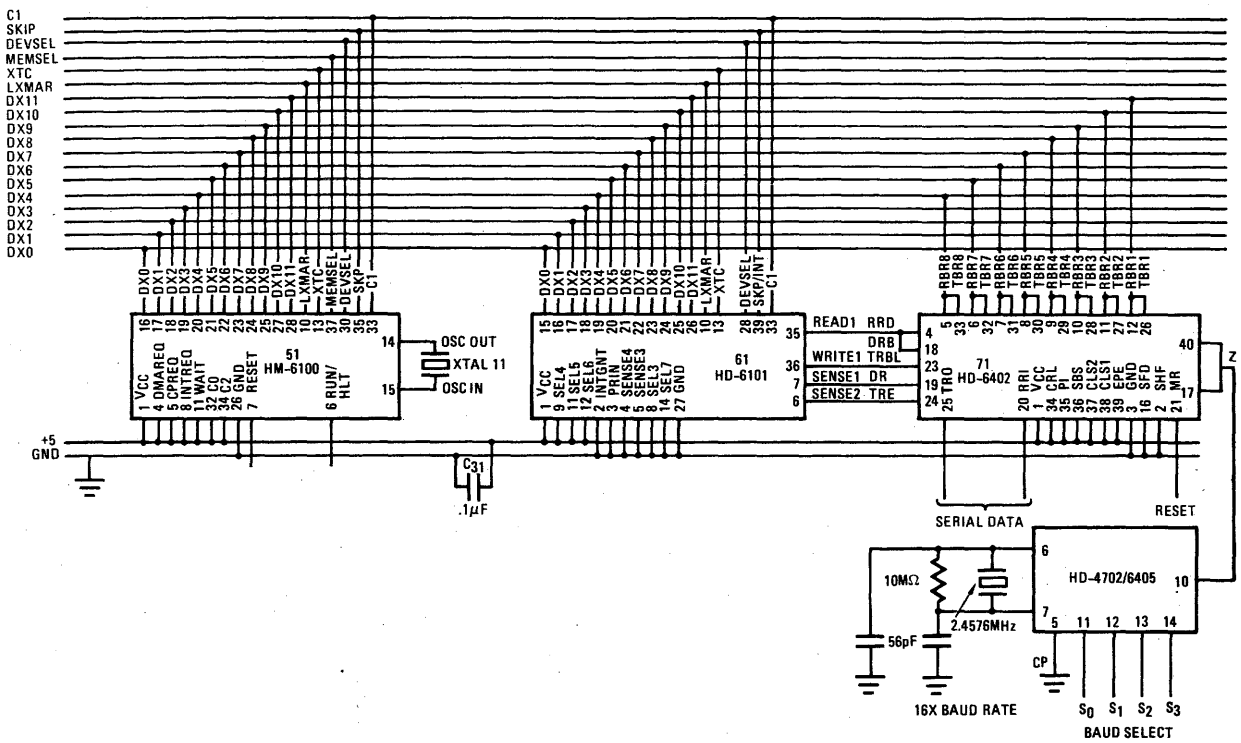
Figure 2
BIT RATE GENERATOR CONFIGURATION WITH EIGHT SIMULTANEOUS FREQUENCIES

NOTE 1: Need to add pull-up resistor on all inputs for the HD-6405.

TABLE 3 CRYSTAL SPECIFICATIONS

PARAMETERS	TYPICAL CRYSTAL SPEC
Frequency	2.4576MHz "AT" Cut
Series Resistance (Max)	250
Unwanted Modes	-6.0dB (Min)
Type of Operation	Parallel
Load Capacitance	32pF $^{+}$0.5

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The bit rate generator is shown supplying the transmit and receive clocks for the UART.

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION

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INTELLEC® MICROCOMPUTER DEVELOPMENT SYSTEMS

Intellec. The first microcomputer development system with in-circuit emulation dramatically shortens development time for your microcomputer-based products.

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Making your microprocessor design team more effective. To achieve optimum design of a microcomputer-based product at lowest cost, software and hardware must be considered simultaneously throughout the development cycle. The Intellec system provides the ICE™ concept to integrate the hardware/software efforts early in the cycle.

Software is tested on the actual prototype, not in a simulated environment designed to look like a description of the product.

Hardware and software development converge as soon as the microprocessor system bus is designed. At this early stage, memory and other Intellec resources can be shared to provide workable system configurations while the actual prototype boards are being built.

Both the Intellec text editor, and the resident PL/M-80 compiler or 8080/8085 or 8048 macro assemblers allow you to incorporate changes to prototype software in a quick, convenient manner, after a debug session.

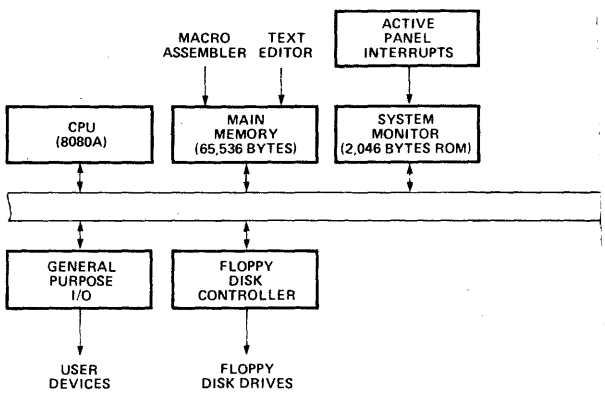
Few companies in the past could enjoy the benefits of their own in-house computer-aided digital design center. The low cost of an Intellec system means that the smallest companies can now share in the benefits of design automation.

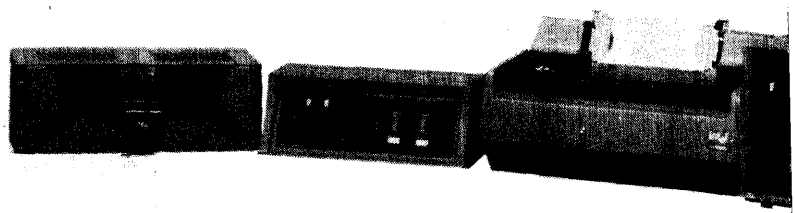
Modular configuration exactly fits your needs. The basic Intellec system includes an 8080-based central processing unit (with a 2 micro-second instruction cycle time, unlimited subroutine nesting, and 78 powerful instructions), 16K bytes of RAM memory, 2K bytes of ROM memory containing the system monitor, and hardware interfaces for a teletypewriter, CRT, line printer, high-speed paper tape reader and punch, and Universal PROM Programmer.

The Intellec system has an eight level nested priority interrupt structure and DMA memory modules; PROM memory can be expanded by the addition of two 6K or 16K PROM memory modules. You satisfy customized I/O requirements by adding general purpose I/O modules which contain four 8-bit input ports, four 8-bit output ports, and eight system interrupt lines. You maximize the efficiency of data transfers between Intellec memory and selected I/O devices by using direct memory access (DMA) modules. The Intellec universal bus supports multi-processor configurations and is not limited to any one Intel microcomputer family.

But the single feature providing you the greatest ease and versatility in developing your products—and the heart of the multi-processor system configuration—is the In-Circuit Emulator known as ICE.

In-circuit emulation provides a window into your prototype. The most significant and versatile feature of the Intellec system is the In-Circuit Emulator—ICE. ICE extends the Intellec systems powerful execution and debug capabilities into your own prototype and production systems. ICE plugs directly into your system replacing your prototype's CPU with a 40 pin plug which is component-level compatible with your microprocessor. ICE modules are available to support user configured 8048, 8085, 8080, 8021, 8049 and 3000 systems.





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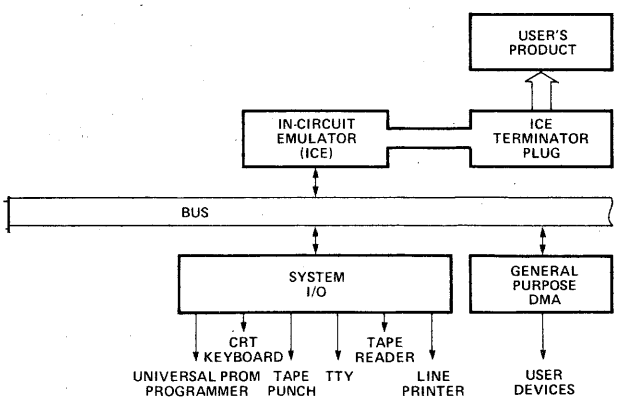
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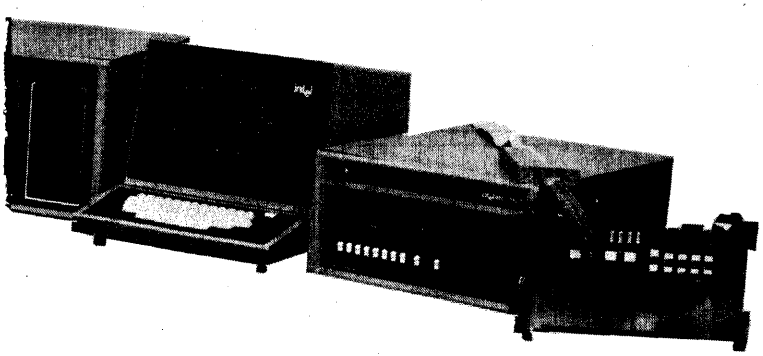
With ICE, you control, interrogate, revise and completely debug your system in its own environment. When you plug ICE into your system in place of your processor, you gain all the diagnostic power and flexibility built into the Intellec system.

You don't need to build your own special display or debug hardware to support your development as these are integral parts of the Intellec system. You can use Intellec memory and input/output facilities in the early phases of testing your prototype. Then, on a step-by-step basis, you replace shared system resources with prototype resident memory and I/O.

ICE checks for hardware and software break conditions. A special external breakpoint probe is provided to attach to any logic signal on a prototype board to detect hardware conditions not directly accessible to the microprocessor bus.

ICE provides the capability to examine and alter CPU registers, main memory, pin and flag values, and automatically collects and stores address, data and status information for machine cycles emulated. And, for the first time, you can examine and modify your system using symbolic references instead of absolute values.





Powerful diskette software reduces program development time. Intel's System Implementation Supervisor (ISIS) is a general purpose, high speed data handler and file manipulation system for use with the Intellec system and its peripherals. It significantly reduces program development time during edit, assembly, compilation, and debugging of programs.

ISIS provides high speed I/O and data storage for the Intellec system. ISIS has a 1/2 million byte storage capacity with two diskette drives, and can store up to 200 program files per diskette.

A wide range of system commands is supplied, offering powerful file and program manipulation features in an easy to use English context. Dynamic allocation of diskette sectors, variable length files and peripheral device independence are all standard features of ISIS. The ISIS text editor provides powerful string search, substitution, insertion, and deletion commands.

The ISIS-II diskette operating system also includes a macro assembler which generates relocatable code, a relocation and linkage package, and a Library Manager™.

The linkage capability enables the user to link several independently assembled or compiled relocatable object modules to form a single relocatable object module.

During the linking process, all external address and data references between program modules are satisfied automatically.

Programs are created, edited, assembled, executed and debugged without paper tape handling. Listings produced by the macro-assembler and PL/M-80 can be directed to diskette for later interrogation from the high speed Intellec console CRT/keyboard, or written directly to line printer.

Resident PL/M brings you high-level programming. The PL/M-80 compiler runs directly on the Intellec system using the ISIS software operating system.

To the user, this means faster development time, lower programming costs, better program reliability, more concise documentation and easier program maintenance.

The PL/M-80 compiler produces efficient relocatable code which can be easily linked with other PL/M-80 and/or assembly language programs.

The PL/M-80 code optimizer performs compile-time analysis, resulting in tighter, more efficient code generation.

Other features of the resident PL/M-80 compiler include: "Innerlist" of generated assembly language code: cross reference listing; listing format options for easy page formatting; easy linkage to external code and data; all required constructs for structured programming and capability for defining re-entrant procedures.

With PL/M-80 the user can create, compile, modify, link, relocate and debug programs entirely on the Intellec system itself with no requirements for large in-house computers or time-sharing services.

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SYMBOLIC DEBUGGING CAPABILITY

ICE-85 allows the user to make symbolic references to I/O ports, memory addresses and data in his program. Symbols and PL/M statement number may be substituted for numeric values in any of the ICE-85 commands. The user is relieved from looking up addresses of variables or program subroutines.

The user symbol table generated along with the object file during a PL/M-80 compilation or by the ISIS-II 8080/8085 Macro Assembler is loaded into the Intellec® System memory along with the user program which is to be emulated. The user may add to this symbol table any additional symbolic values for memory addresses, constants, or variables that are found useful during system debugging. By referring to symbol memory addresses, the user can examine, change or break at the intended location.

ICE-85 provides symbolic definition of all 8085 registers, interrupt bits and flags. The following symbolic references are also provided for user convenience: TIMER, the low-order 16 bits of a register containing the number of 2 MHz clock pulses elapsed during emulation; HTIMER, the high-order 16 bits of the timer counter; PPC, the address of the last instruction emulated; BUFFERSIZE, the number of frames of valid trace data (between 0 and 1022).

PERSONALITY GROUPED DISPLAYS

Trace data in the 1023 by 42-channel real-time trace memory buffer is displayed in easy to read format. The user has the option to specify trace data displays in actual 8085 assembler instruction mnemonics. The data collected from the External Trace Module can be grouped and symbolically named according to user specifications and displayed in the appropriate number base designation. Simple ICE-85 commands allow the user to select any portion of the 42K-bit trace buffer for immediate display.

MEMORY AND I/O MAPPING

Memory and I/O for the user system can be resident in the user system or "borrowed" from the Intellec® System through ICE-85's mapping capability.

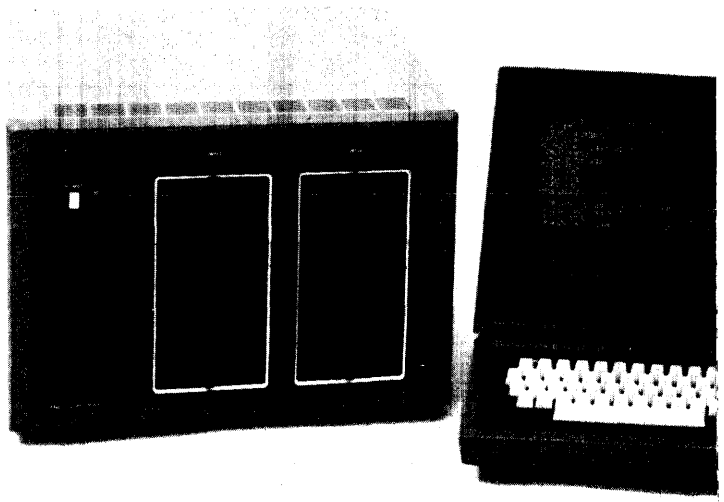
ICE-85 separates user memory into 32 2K blocks. Each block of memory can be defined independently. The user may assign Intellec® System equivalents to take the place of devices not yet designed for the user system during prototyping. In addition, Intellec® System memory or I/O can be accessed in place of suspect user system devices during prototyping or production checkout.

The user can also designate a block of memory or I/O as nonexistent. ICE-85 issues error messages when memory or I/O designated as nonexistent is accessed by the user program.

INTEGRATED HARDWARE/SOFTWARE DEVELOPMENT

The user prototype need consist of no more than an 8085 CPU socket and a user bus to begin integration of software and hardware development efforts. Through ICE-85 mapping capabilities, Intellec® System equivalents can be accessed for missing prototype hardware. Hardware designs can be tested using the system software which will drive the final product.

The system integration phase, which can be so costly when attempting to mesh completed hardware and software products, becomes a convenient two-way debug tool when begun early in the design cycle.



TYPICAL ICE INTERROGATION AND UTILITY COMMANDS

DISPLAY/ CHANGE	Display/Changes the values of symbols and the contents of 8085 registers, pseudo-registers, status flags, interrupt bits, I/O ports and memory.
EVALUATE	Displays the value of an expression in the binary, octal, decimal or hexadecimal.
SEARCH	Searches user memory between locations in a user program for specified contents.
CALL	*Emulates* a procedure starting at a specified memory address in user memory.
ICALL	*Executes* a user-supplied procedure starting at a specified memory address in the Intellec® System memory.
EXECUTE	Saves emulated program registers and emulates a user-supplied subroutine to access peripheral chips in the user's system.

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REAL TIME TRACE

ICE-85 captures valuable trace information from the emulating CPU and the External Trace Module while the user is executing programs in real time. The 8085 status, the user memory or port addressed, the data read or written, the serial data lines and data from 18 external signals, is stored for the last 1023 machine states executed (511 machine cycles). This provides ample data for determining how the user system was reacting prior to emulation break. It is available whether the break was user-initiated or the result of an error condition.

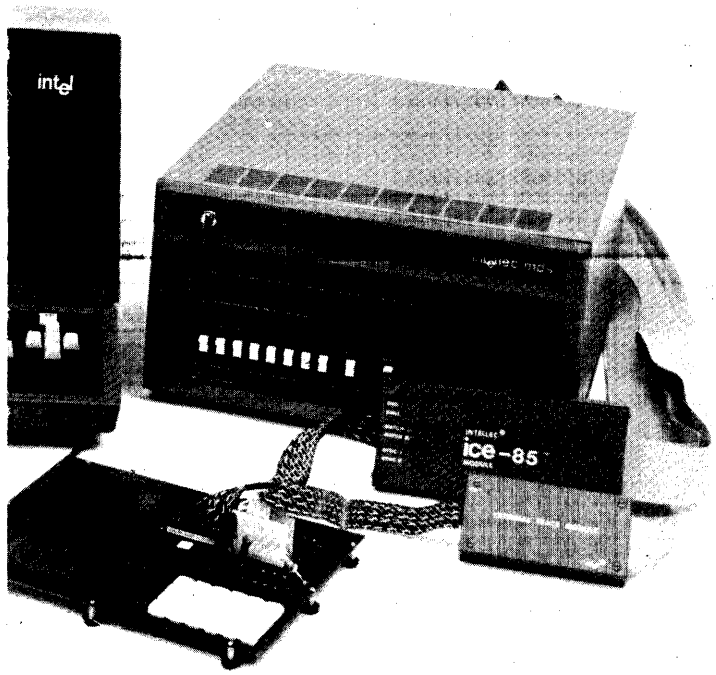
For detailed information on the actions of CPU registers, flags, or other system operations, the user may operate in single or multi-step sequences tailored to system debug needs.

EXTERNAL TRACE MODULE

TTL level signals from 18 points in the user system may be synchronously sampled by the External Trace Module and collected in ICE-85's trace buffer. The signals can be collected from a single peripheral chip via the supplied 40-pin DIP clip or may be placed by the user on up to 18 separate signal nodes using the supplied 18 individual probe clips. These signals are included in the 42-channel breakpoint comparisons and clock qualifiers. Also, data from these 18 channels may be displayed in each to read, user-defined groupings.

SYNCHRONOUS OPERATION WITH OTHER DESIGN AIDS

ICE-85 can be synchronized with other Intellec® design aids by means of two external synchronization lines. These lines are used to enable and disable ICE-85 trace data collection and to cause break conditions based on an external signal which may not be included in the ICE-85 breakpoint registers. In addition, ICE-85 can generate signals on these lines which may be used to control other design aids.



BREAK REGISTERS/TRACE MEMORY

ICE-85 has two breakpoint registers which are used to break emulation, and two trace qualifier registers which are used to control the collection of trace data during emulation. Each register is 42 entries wide, one entry for each channel and each entry can take any one of the three values 0, 1 or "don't care".

The trace buffer, also 42 entries wide, collects data sampled from 24 8085 processor channels and 18 external channels sampled by the External Trace Module. The signals collected from the 8085 include address lines, data lines, status lines and serial input and output lines. The 18 channels extending from the External Trace Module synchronously sample and collect into the trace buffer any user-specified TTL compatible signal from the rest of the prototype system. "Break" and "trace qualification" may therefore occur as a result of a match of any combination of up to 42 channels of CPU and external circuitry signals.

EMULATION CONTROLS AND COMMANDS

GROUP	Defines into a symbolically named group, a channel or combination of channels from the 8085 Microcprocessor and/or the External Trace Module.
GO	Initiates real-time emulation and controls emulation break conditions.
STEP	Initiates emulation in single instruction steps. User may specify the type and amount of information displayed following each step, and define conditions under which stepping should continue.
PRINT	Prints the user-specified portion of the trace memory to the selected list device.

Other In-Circuit Emulators Available From Intel:

ICE 30 ICE 48
ICE 41 ICE 80
ICE 49

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intel®

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

8085A
SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

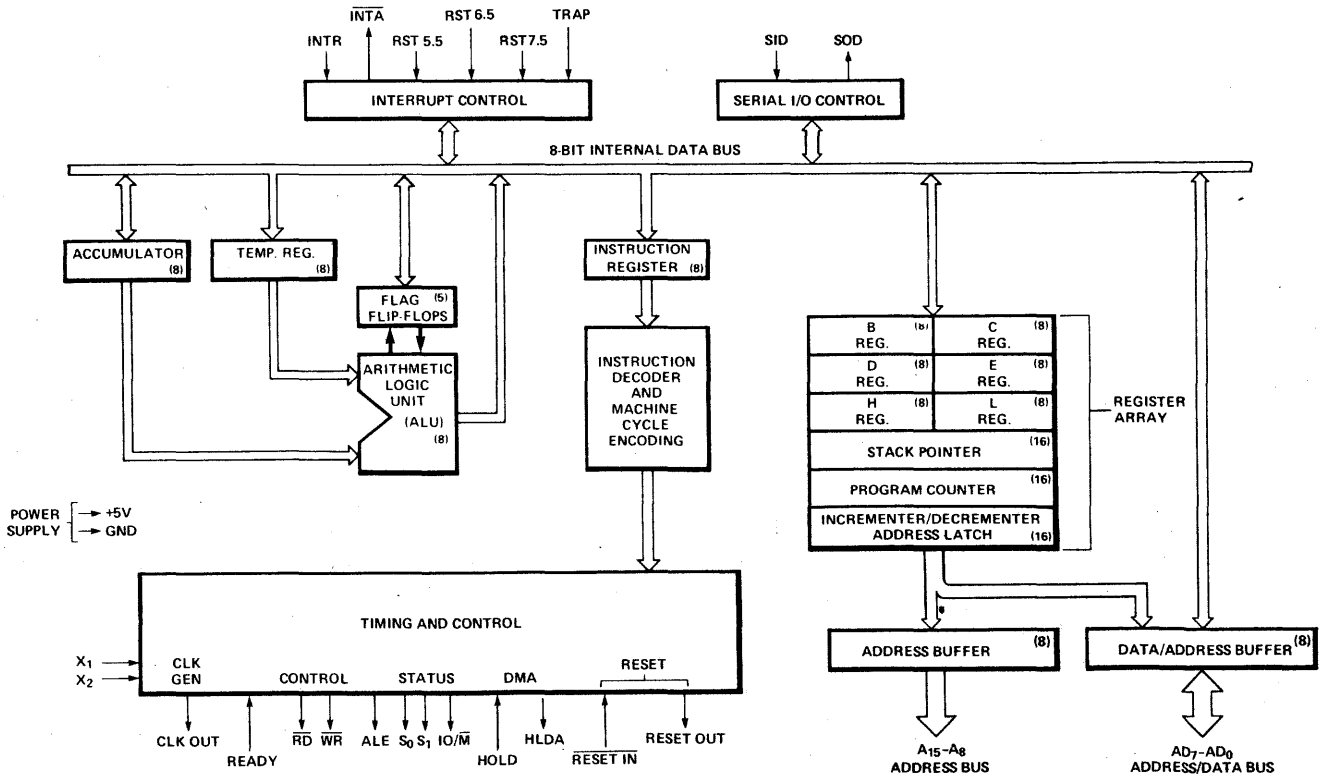
- **Single +5V Power Supply**
- **100% Software Compatible with 8080A**
- **1.3 μs Instruction Cycle**
- **On-Chip Clock Generator (with External Crystal or RC Network)**
- **On-Chip System Controller**
- **Four Vectored Interrupts (One is non-Maskable)**
- **Serial In/Serial Out Port**
- **Decimal, Binary and Double Precision Arithmetic**
- **Direct Addressing Capability to 64K Bytes of Memory**

The Intel® 8085A is a new generation, complete 8 bit parallel central processing unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's: 8085A (CPU), 8156 (RAM) and 8355/8755 (ROM/PROM).

The 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080, thereby offering a high level of system integration.

The 8085A uses a multiplexed Data Bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155/8355/8755 memory products allows a direct interface with 8085A.

8085 CPU FUNCTIONAL BLOCK DIAGRAM



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8155/8156

2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

8155 — Active Low Chip Enable ($\overline{CE}$)
8156 — Active High Chip Enable (CE)

*Directly Compatible With 8085 CPU

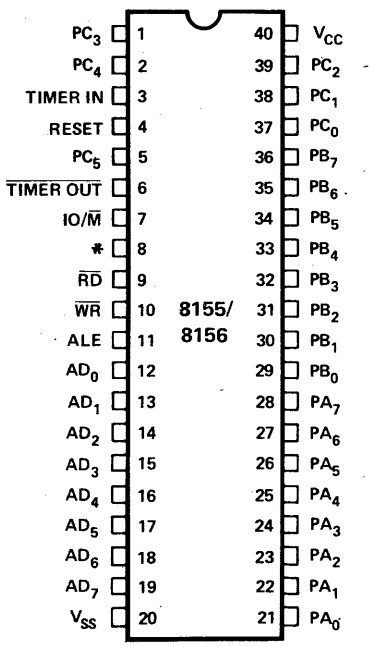
- 256 Word x 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8 Bit I/O Ports
- 1 Programmable 6 Bit I/O Port
- Programmable 14 Bit Binary Counter/Timer
- Multiplexed Address and Data Bus
- 40 Pin DIP

The 8155 and 8156 are RAM and I/O chips to be used in the MCS-85™ microcomputer system. The RAM portion is designed with 2K bit static cells organized as 256 x 8. They have a maximum access time of 400ns to permit use with no wait states in 8085 CPU.

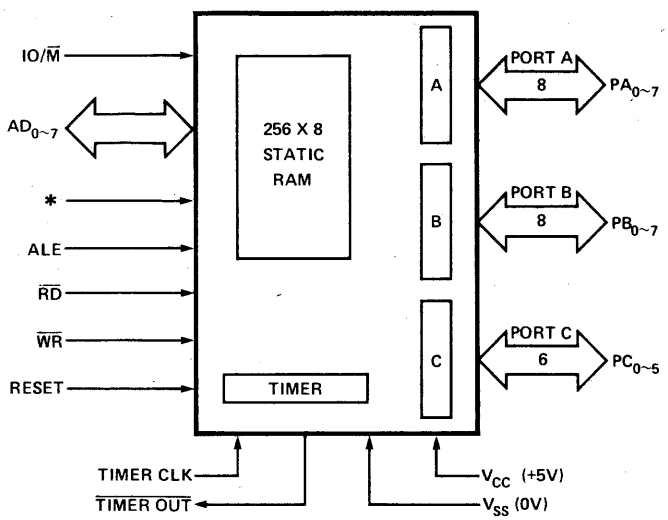
The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14 bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system. It operates in binary countdown mode, and its timer modes are programmable.

PIN CONFIGURATION



BLOCK DIAGRAM



* : 8155 = $\overline{CE}$, 8156 = CE

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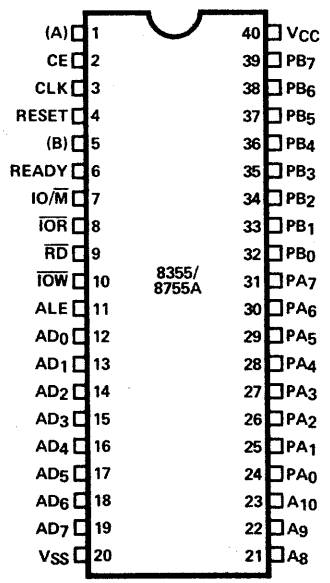
8355/8755A
8355-16,384 BIT ROM WITH I/O
8755A-16,384 BIT EPROM WITH I/O
*Directly Compatible With 8085 CPU

- 2048 Words × 8 Bits
- Single +5V Power Supply
- Internal Address Latch
- 2 General Purpose 8 Bit I/O Ports
- Each I/O Port Line Individually Programmable as Input or Output
- Multiplexed Address and Data Bus
- 40 Pin DIP

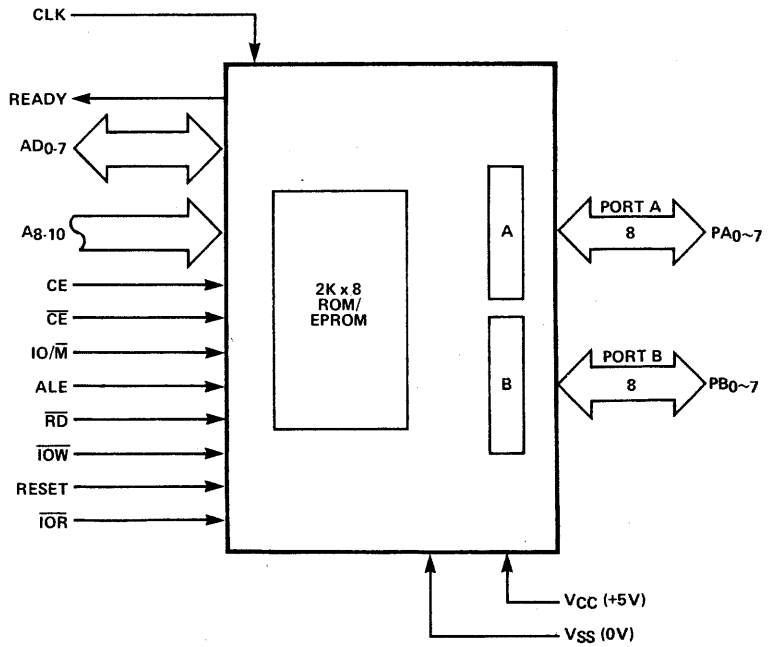
The 8355 is a ROM and I/O chip to be used in the MCS-85™ microcomputer system. The 8755 is a UV erasable and electrically reprogrammable ROM (EPROM) and I/O chip. The ROM portion is organized as 2048 x 8. It has maximum access time of 400 ns to permit use with no wait states in 8085 CPU.

The I/O portion consists of two general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

PIN CONFIGURATION



BLOCK DIAGRAM



	8355	8755A
(A)	$\overline{CE}$	PROG AND $\overline{CE}$
(B)	NOT CONNECTED	V_{DD} (+5V DURING OPERATION)

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OCTOBER 1977

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SDK-85
MCS-85™ SYSTEM DESIGN KIT

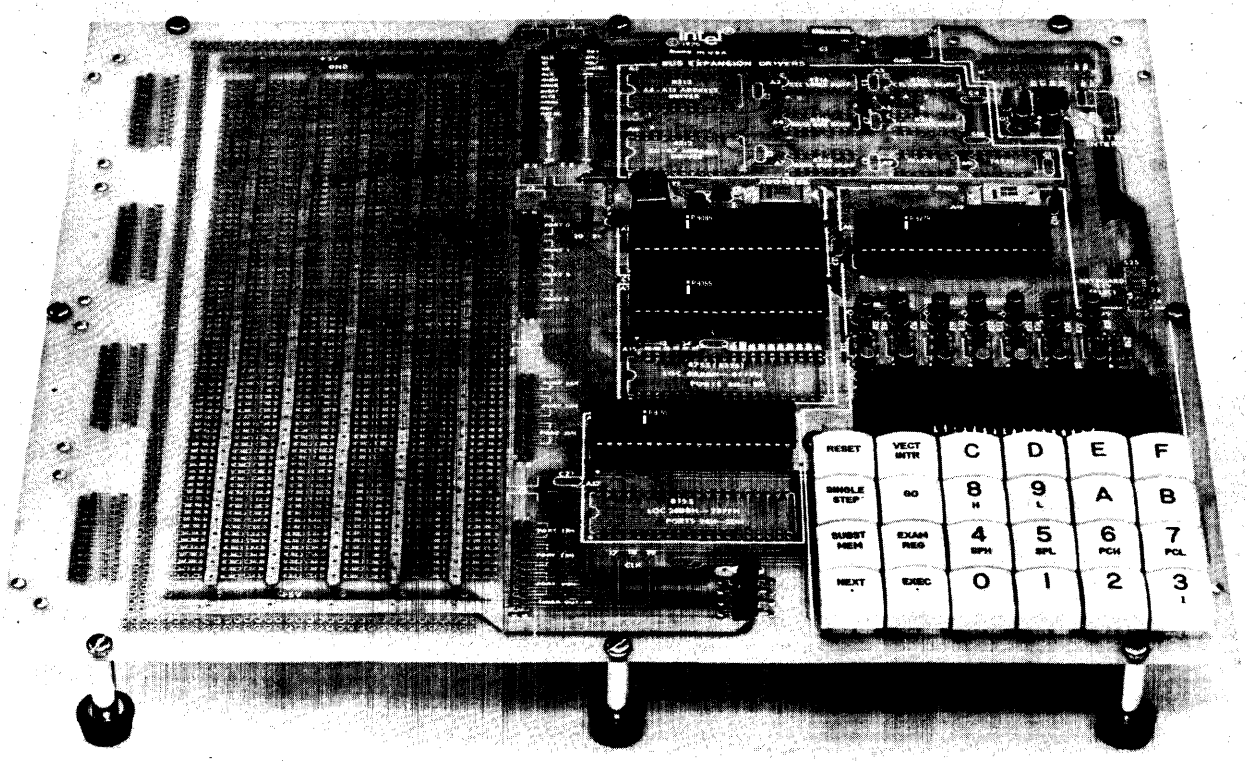
PRELIMINARY
Notice: This is not a final specification. Some parameter limits are subject to change.

- Complete Single Board Microcomputer System Including CPU, Memory and I/O
- Easy to Assemble Kit-Form
- High-Performance 3MHz 8085 CPU (1.3 μs Instruction Cycle)
- Popular 8080A Instruction Set
- Interfaces Directly With TTY
- Interactive LED Display and Keyboard.
- Large Wire-Wrap area for Custom Interfaces
- Extensive System Monitor Software in ROM
- Comprehensive Design Library Included
- Low Cost

The MCS-85 System Design Kit (SDK-85) is a complete, single board, microcomputer system in kit form. It contains all necessary components, including LED Display, Keyboard, resistors, caps, crystal and miscellaneous hardware to complete construction. Included is a preprogrammed ROM that contains the system monitor for general software utilities and system diagnostics.

The SDK-85 includes 6 digit LED display and 24 key-keyboard for a direct insertion, examination and execution of a user's program. In addition, it can be directly interfaced with a teletype terminal.

The SDK-85 is an inexpensive, high-performance prototype system that has designed-in flexibility for simple interface to the user's application.



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PRELIMINARY
Intel reserves the right to make changes to specifications at any time, without notice. Some specifications may be subject to change.

8048/8748/8035

SINGLE COMPONENT 8-BIT MICROCOMPUTER

***8048 Mask Programmable ROM**
***8748 User Programmable/Erasable EPROM**
***8035 External ROM or EPROM**

- **8-Bit CPU, ROM, RAM, I/O in Single Package**
- **Interchangeable ROM and EPROM Versions**
- **Single 5V Supply**
- **2.5 µsec and 5.0 µsec Cycle Versions All Instructions 1 or 2 Cycles.**
- **Over 90 Instructions: 70% Single Byte**
- **1K x 8 ROM/EPROM 64 x 8 RAM 27 I/O Lines**
- **Interval Timer/Event Counter**
- **Easily Expandable Memory and I/O**
- **Compatible with MCS-80™ Peripherals**
- **Single Level Interrupt**

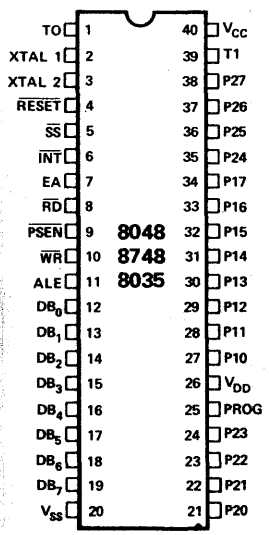
The Intel® 8048/8748/8035 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process.

The 8048 contains a 1K x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the 8048 can be expanded using standard memories and MCS-80™ (8080A) peripherals. The 8035 is the equivalent of an 8048 without program memory.

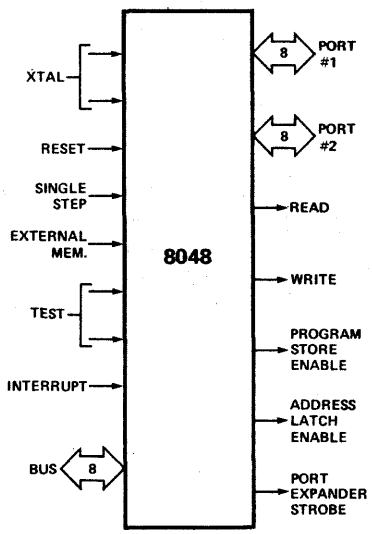
To reduce development problems to a minimum and provide maximum flexibility, three interchangeable pin-compatible versions of this single component microcomputer exist: the 8748 with user-programmable and erasable EPROM program memory for prototype and preproduction systems, the 8048 with factory-programmed mask ROM program memory for low-cost high volume production, and the 8035 without program memory for use with external program memories.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

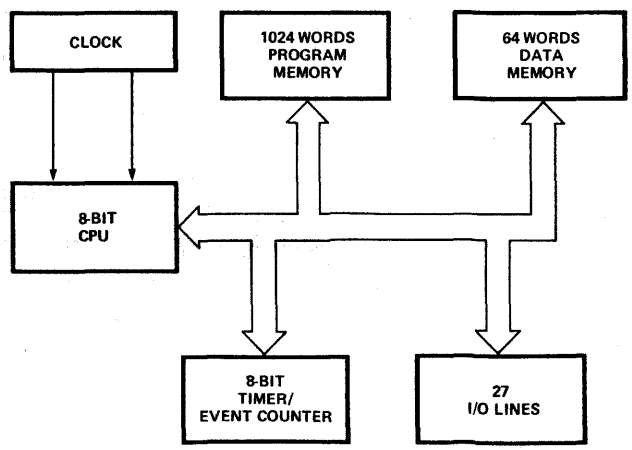
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



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8021

SINGLE COMPONENT 8-BIT MICROCOMPUTER

- **8-Bit CPU, ROM, RAM, I/O in Single 28-Pin Package**
- **Single 5V Supply (+4.5V to 6.5V)**
- **10 μsec Cycle; All Instructions 1 or 2 Cycles**
- **Instructions —8748 Subset**
- **High Current Drive Capability—2 Pins**
- **1K × 8 ROM**
  64 × 8 RAM
  21 I/O Lines
- **Interval Timer/Event Counter**
- **Clock Generated With Single Resistor or Inductor**
- **Zero-Cross Detection Capability**
- **Easily Expandable I/O**

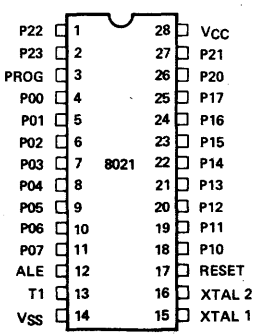
The Intel® 8021 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process. The features of the 8021 include a subset of the 8048 optimized for low-cost, high volume applications, plus additional I/O flexibility and power.

The 8021 contains a 1K X 8 program memory, a 64 X 8 data memory, 21 I/O lines, and an 8-bit timer/event counter, in addition to on-board oscillator and clock circuits. For systems that require extra I/O capability, the 8021 can be expanded using the 8243 or discrete logic.

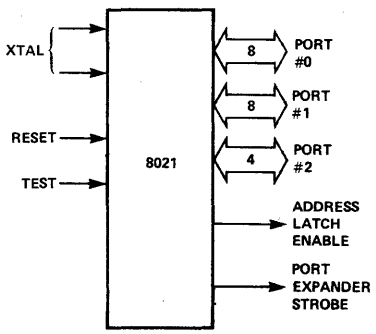
This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8021 has bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

To minimize development problems and maximize flexibility, an 8021 system can be easily designed using the 8021 emulation board, EMB-21. The EMB-21 contains a 40-pin socket which can accomodate either the 8748 shipped with the board or an ICE-48 plug. Also, the necessary discrete logic to reproduce the 8021's additional I/O features is included.

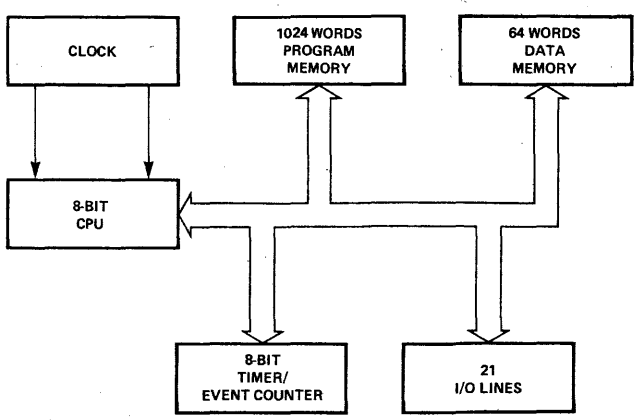
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



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SEPTEMBER 1977

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8049/8039
SINGLE COMPONENT 8-BIT MICROCOMPUTER

EARLY PRODUCTION

*8049 Mask Programmable ROM
*8039 External ROM or EPROM

- 8-Bit CPU, ROM, RAM, I/O in Single Package
- Single 5V ±10% Supply
- 2.5 μsec Cycle; All Instructions 1 or 2 Cycles
- Over 90 Instructions: 70% Single Byte
- Pin Compatible with 8048/8748
- 2K x 8 ROM
  128 x 8 RAM
  27 I/O Lines
- Interval Timer/Event Counter
- Easily Expandable Memory and I/O
- Compatible with MCS-80/85™ Peripherals
- Single Level Interrupt

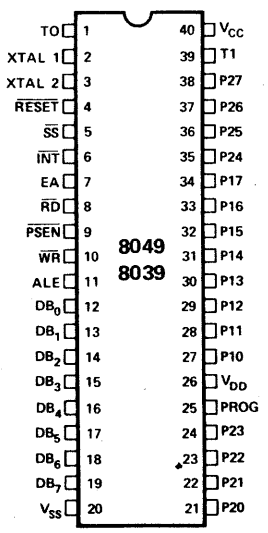
The Intel® 8049/8039 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process.

The 8049 contains a 2K x 8 program memory, a 128 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the 8049 can be expanded using standard memories and MCS-80™/MCS-85™ peripherals. The 8039 is the equivalent to an 8049 without program memory.

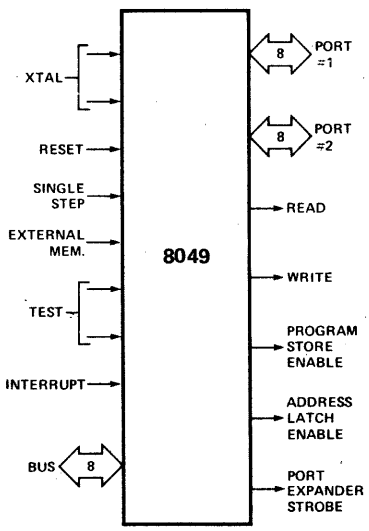
To reduce development problems to a minimum and provide maximum flexibility, two interchangeable pin-compatible versions of this single component microcomputer exist: the 8049 with factory-programmed mask ROM program memory for low-cost high volume production, and the 8039 without program memory for use with external program memories in prototype and preproduction systems.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8049 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

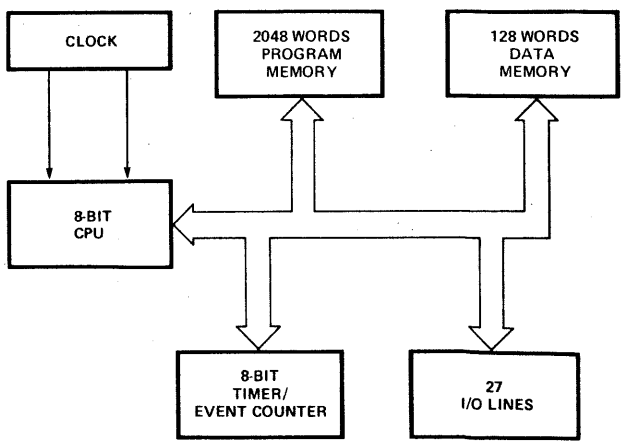
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



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8041/8741 UNIVERSAL PERIPHERAL INTERFACE

- Fully Compatible with MCS-80™ and MCS-48™ Microprocessor Families
- Single Level Interrupt
- 8-Bit CPU Plus ROM, RAM, I/O, Timer, and Clock in a Single Package
- Single 5V Supply
- Alternative to Custom LSI
- Pin Compatible ROM and EPROM Versions
- 1Kx8 ROM/EPROM, 64x8 RAM, 18 Programmable I/O Pins
- Asynchronous Data Register for Interface to Master Processor
- Expandable I/O

8243 INPUT/OUTPUT EXPANDER

- Low Cost
- Simple Interface to MCS-48™ Microcomputers
- Four 4-Bit I/O Ports
- AND and OR Directly to Ports
- 24-Pin DIP
- Single 5V Supply
- High Output Drive
- Direct Extension of Resident 8048 I/O Ports

8271 PROGRAMMABLE FLOPPY DISK CONTROLLER

- Supports Standard or Minifloppy Drives
- IBM3740 Soft Sectored Format Compatible
- Associative Scan Search Commands
- Programmable Record Lengths
- Multi-Sector Capability
- Maintain Dual Drives with Minimum Software Overhead Expandable to 4 Drives
- Automatic Read/Write Head Positioning and Verification
- Internal CRC Generation and Checking
- Programmable Step Rate, Settle-Time, Head Load Time, Head Unload Index Count
- Fully Compatible with 8080/8085 CPU
- Single +5 Volt Supply
- 40-Pin Package

8273 SDLC PROTOCOL CONTROLLER

- IBM SDLC Compatible
- Frame Level Commands
- Full Duplex, Half Duplex, or Loop SDLC Operation
- Two User Progrrammable Modem Control Ports
- Up to 64K Baud Transfers
- Automatic FCS (CRC) Generation and Checking
- Programmable NRZI Encode/Decode
- N-Bit Reception Capability
- Minimum CPU Overhead
- Digital Phase Locked Loop Clock Recovery
- Fully Compatible with 8080/8085 CPU
- Single +5 Volt Supply
- 40-Pin Package

8275 PROGRAMMABLE CRT CONTROLLER

- Programmable Screen and Character Formats
- Six Independent Visual Field Attributes
- Eleven Visual Character Attributes (Graphic Capability)
- Cursor Control (4 Types)
- Light Pen Detection and Registers
- Fully MCS-80™ and MCS-85™ Compatible
- Dual Row Buffers
- Programmable DMA Burst Mode
- Single +5 Volt Supply
- 40-Pin Package

8279, 8279-5 PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

- MCS-85™ Compatible 8279-5
- Simultaneous Keyboard Display Operations
- Scanned Keyboard Mode
- Scanned Sensor Mode
- Strobed Input Entry Mode
- 8 Character Keyboard FIFO
- 2-Key Lockout or N-Key Rollover
- Dual 8 or 16 Numerical Display
- Single 16-Character Display
- Right or Left Entry 16-Byte Display RAM
- Mode Programmable from CPU
- Programmable Scan Timing
- Interrupt Output on Key Entry

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8×8 Multiplier

57558/67558

FEATURES

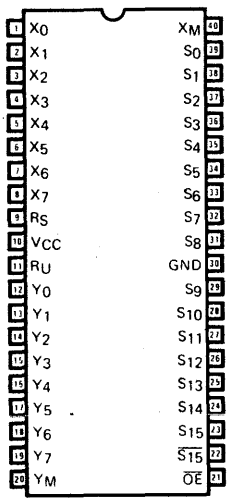
- Unsigned, Signed or Mixed Multiplication
- Rounding Inputs for Signed or Unsigned Operation
- Inverted Most Significant Output For Signed Expansion
- Three-State Outputs for Bus Operation
- High Speed – 100 ns Typ

PART NUMBER	PACKAGE	TEMPERATURE RANGE
67558	D40	0°C TO +75°C
57558	D40	-55°C TO +125°C

DESCRIPTION

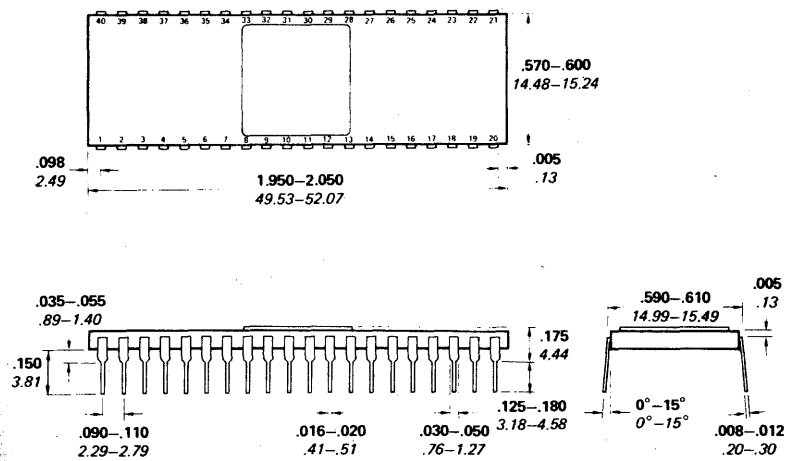
The 57558/67558 is a high speed 8 x 8 combinatorial Multiplier which can multiply two eight-bit unsigned or signed 2s complement numbers and generate the sixteen-bit unsigned or signed product. Each input operand X and Y has an associated Mode control line, X_M and Y_M respectively. When a Mode control line is at a Low logic level the operand is treated as an unsigned eight-bit number while if the Mode control is at a High logic level the operand is treated as an eight-bit signed 2s complement number. Two additional inputs R_S and R_U allow the addition of a bit in the multiplier array at the appropriate bit positions for rounding signed or unsigned fractional numbers. The most significant product bit is available in both True and Complement form to assist in expansion to larger signed multipliers. The product outputs are three-state, controlled by an active Low Output Enable which allows several Multipliers to be connected to a parallel bus or to be used in a pipelined system. The device uses a single +5V power supply and is packaged in a standard 40-pin DIP.

PIN OUT

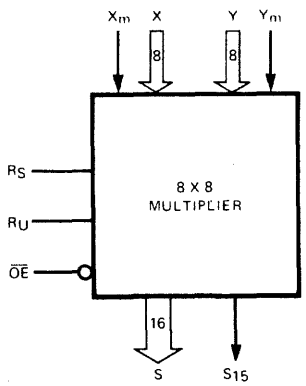


PACKAGE DRAWING

D40 Ceramic DIP (side-brazed)



LOGIC SYMBOL



Monolithic Memories
1165 East Arques Ave., Sunnyvale CA 94086
Tel: (408) 739-3535/TWX: (910) 339-9229

MICROPROCESSOR MMI

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . -0.5V to +7.0V
Input Voltage . . . . . -1.5V to +5.5V
Input Current . . . . . -20 mA to +5 mA
Output Current . . . . . 100 mA
Storage Temperature Range . . . . . -65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	57558, 57558-1			67558, 67558-1			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply Voltage	4.5	5.0	5.5	4.75	5.0	5.25	V
T_A	Operating Free Air Temperature				0	25	75	°C
T_C	Operating Case Temperature	-55	25	125				°C
I_{OH}	High Level Output Current			-2.0			-2.0	mA
I_{OL}	Low Level Output Current			8			8	mA

ELECTRICAL CHARACTERISTICS

Over recommended operating free air temperature range unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP [1]	MAX	UNIT
V_{IH}	High Level Input Current		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = -18 mA		-1.0	-1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = -2.0 mA	2.4	3.0		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 8 mA		0.3	0.5	V
I_{HZ}	High Level Off-State Output Current	V_{CC} = Max, V_O = 2.4V			50	μA
I_{LZ}	Low Level Off-State Output Current	V_{CC} = Max, V_O = 0.5V			-50	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V			1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			100	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			-1.0	mA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, V_O = 0V	-10		-90	mA
I_{CC}	Supply Current	V_{CC} = Max		180	280	mA

NOTE 1. Typical values are at V_{CC} = 5.0V, T_A = 25°C

SWITCHING CHARACTERISTICS

Over recommended operating V_{CC} and temperature range

SYMBOL	PARAMETER	DEVICE	MIN	TYP	MAX	UNIT
t_{PXZ}, t_{PZX}	Delay from OE to Outputs	67558-1, 67558		30	40	ns
		57558-1, 57558		30	50	
t_{PD1}	Delay from Y, X to S_{0-3}	67558		80	135	ns
		57558		80	140	
		67558-1		80	115	
		57558-1		80	125	
t_{PD2}	Delay from Y, X to S_{4-15}, S_{15}	67558		100	150	ns
		57558		100	155	
		67558-1		100	125	
		57558-1		100	135	

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Microprogram Controller

57110/67110

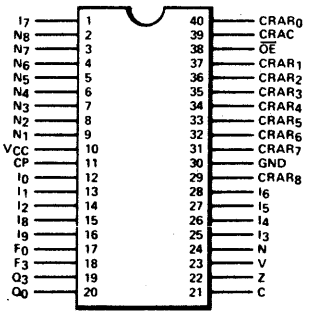
FEATURES

- Addresses 512 words
- Easily expandable
- Microsubroutine capability
- Loop control
- Multi-path branching
- Shift control for data slice
- Three-state output bus
- High speed
- Standard 40-pin package

APPLICATIONS

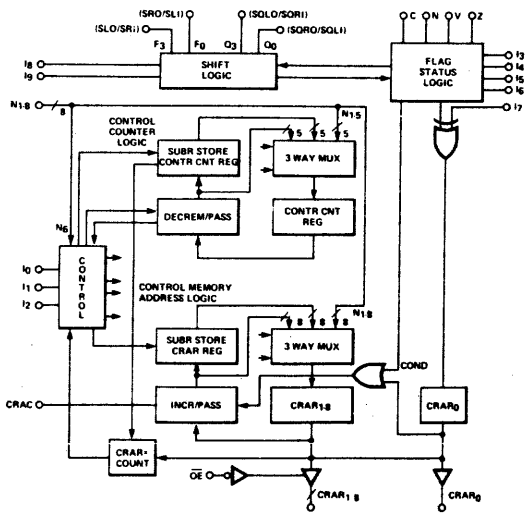
- Minicomputer microprogram controller
- High-speed disk controller
- Line printer controller
- CRT terminal controller

PIN CONFIGURATION



The 57110/67110 Microprogram Controller (MPC) is a member of the 57000/67000 computer logic family of high-performance bipolar compatible Schottky TTL components. The device is designed to work in conjunction with 4-bit slice microprocessors and standard ROMs and PROMs for the design of extremely powerful computing systems. The power and flexibility of the MPC also allow it to be used for general purpose control applications.

BLOCK DIAGRAM



FIFO

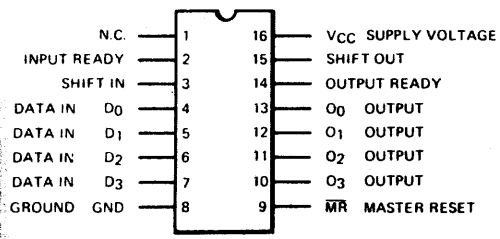
57401/67401

The 57401/67401 First-In, First-Out (FIFO) Serial Memory is used to receive data at one clock rate and to transmit this data at a different clock rate. The device is useful whenever data is incoming to a system asynchronously to the rate at which the system is operating such as in data acquisition. The 57401/67401 is arranged in 64 word by 4-bit wide architecture and is provided with separate input/output clocks and input/output ready indicator lines. Common active low and master reset are provided. Five volt power supplies are used with TTL input/output levels at data rates in excess of 10MHz. Military and commercial temperature range devices are available.

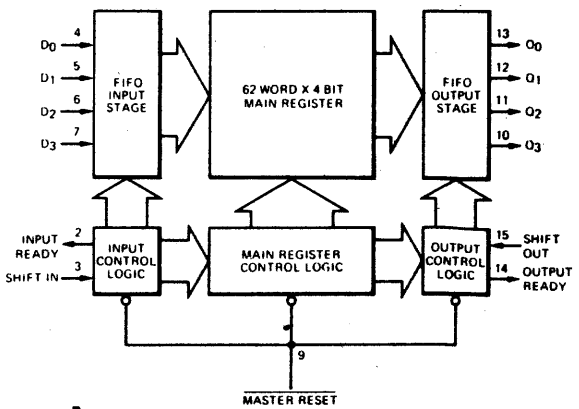
PRODUCT FEATURES

- 10MHz shift in/shift out rates
- Advanced Schottky bipolar processing
- TTL inputs and outputs
- Readily expandable in word and bit dimensions
- Asynchronous or synchronous operation
- Pin compatible with Fairchild's F3341 MOS FIFO and ten times as fast.

PIN CONFIGURATION



BLOCK DIAGRAM



Monolithic Memories
1165 East Arques Ave., Sunnyvale CA 94086
Tel: (408) 739-3535/TWX: (910) 339-9229

MMI
MICROPROCESSOR

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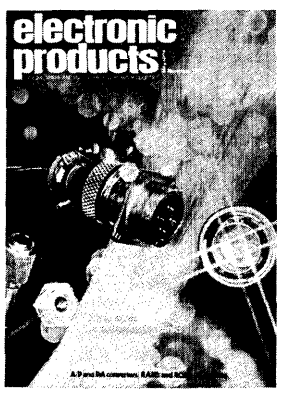
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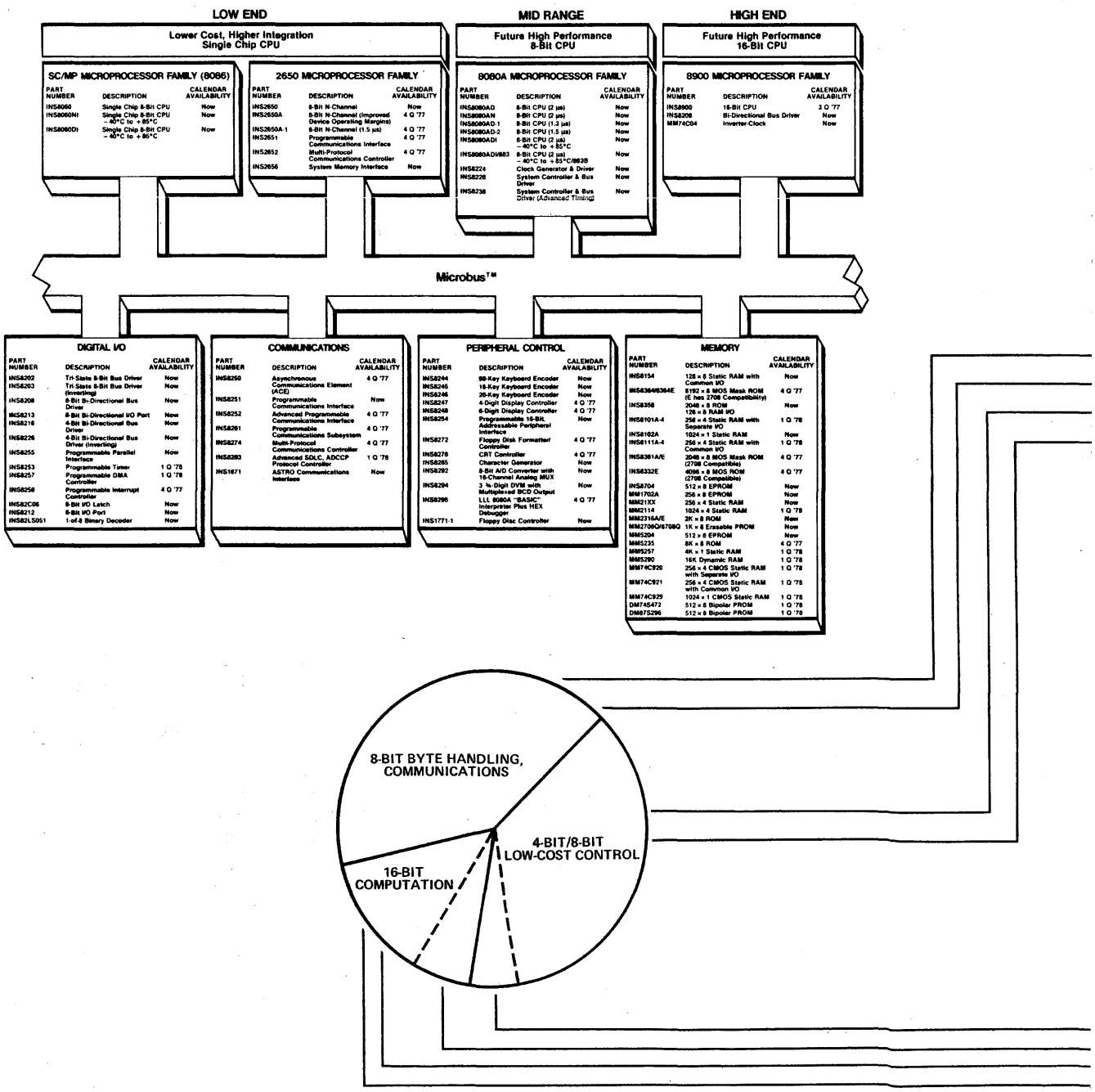
National's Full Spectrum of Microprocessors

National Semiconductor, offers the broadest line of microprocessors of any semiconductor manufacturer in the world. National has expanded its microprocessor base so any microprocessor application can be designed and produced using its products. From the simplest electronic toy or control mechanism to large control arrays, point-of-sale systems, and large data-processing systems, National can supply your needs. Some of the features and benefits of dealing with National follow.

- Cost effectiveness – because of our variety, our microprocessors afford designs that can be tailored to a multitude of applications
- Broad product family of microprocessors and peripherals:
- 16-Bit COMPUTATION microprocessors for precision control functions
- 8-Bit BYTE HANDLING microprocessors for terminals
- 4/8-Bit LOW-COST CONTROL microprocessors for industrial controllers
- Second sourced families
- Ready availability – off-the-shelf shopping
- Micro-Plus – special reliability and quality program
- Full development system support – all the way from the high-powered PACE development system (with numerous software packages and a DOS) to low-cost development systems (for PACE and SC/MP) to do-it-yourself PACE and SC/MP kits

National Semiconductor also offers the most extensive line of CPU-to-peripheral support products – for digital input/output, communications, peripheral control, and memory. And National Semiconductor is expanding the support lines, so you can expect to see even more!

Microprocessors and Peripherals from National – Compatibility Plus



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For a Full Spectrum of Applications

National's INS2650 Family

The 2650 Family consists of a series of memory and peripheral components built around the 2650A 8-bit microprocessor. This second-sourced processor family offers excellent byte and bit manipulation for a variety of applications.

Seventy-five variable-length instructions – one, two, and three bytes – comprise the instruction set, thus minimizing memory requirements. Some of National's INS2650 family features:

- Single-phase clock, using only one interface pin and requiring only a normal TTL voltage swing, no special clock driver is required
- Single 5-volt power supply
- TRI-STATE data and address signals, simplifying system design and allowing asynchronous memory and I/O interface signals – means DMA is easy to implement
- Single-level, address-vectoring interrupt mechanism – means that the interrupting device can force execution of code at a device-determined memory location

National's INS8080A Family

Positioned between the cost-effective SC/MP and the highly versatile PACE, National's INS8080A can be used in systems which range from a few family components to designs which utilize its full capabilities. National offers the broadest line of peripheral circuits and memories to complement the basic 8080A CPU, with most parts available *now*. National's 8080A features and benefits:

- Family approach to system design
- Complete CPU group
- Programmable input/output concepts
- Multiple source availability
- Complete line of support components
- Total product support

National's N8080 family is supported by industry-standard design kits, easy-to-use development systems, and a full complement of cross and resident assemblers. Various components and software also are available to support the N8080 family from experimentation to final production.

National's SC/MP Family

SC/MP is National's simplest true microprocessor. It is the lowest-cost replacement for electrical, mechanical and hydraulic control systems. Typical applications include business machines, scales, cash registers and other human-interface devices.

The growing family of SC/MP devices presently includes PMOS and a new, double-speed NMOS CPU (SC/MP-II), a RAM-I/O chip with 16 I/O lines, and a variety of bus-oriented interface and memory devices. The SC/MP CPU itself incorporates unique multiprocessor control logic to facilitate distributed processing systems with the lowest number of components. SC/MP also has a built-in Clock, Parallel and Serial I/O; it uses low power; and it can interface to standard memory and peripheral products. Also available is a BASIC high-level language called NIBL, which can be obtained in ROM form for fast software development.

SC/MP CPU, RAM, and ROM/PROM application cards are also available to help speed prototyping and production for users who need these functions ready-made. To develop programs, use the SC/MP Low Cost Development System – or the PACE Development System, which has a full complement of support software for preparing SC/MP programs.

National's FIPS Family

FIPS (INS4004) is National's second source to the MCS-4* family. This was the first production microprocessor system, and it is still a popular 4-bit microprocessor because of its simplicity and low cost. The INS4004 is fabricated using P-channel silicon gate MOS technology.

Some of National's INS4004 features:

- Four-bit parallel CPU
- Applicable for use in test systems, terminals, billing machines, process control, and random logic replacement
- Readily interfaces with keyboards, switches, displays, A/D converters, and various peripheral equipment
- Ability of CPU to address 4K 8-bit instruction words, 5120 bits of RAM, up to 16 4-bit input ports, and 16 4-bit output ports
- In volume production

*A registered trademark of Intel Corporation

National's COPS Family

Calculator Oriented Processor Systems (COPS) provide a low-cost solution to low-end computing and control problems. Manufactured by National's volume-proven P-channel MOS/LSI calculator process, COPS offers an attractive, low-risk alternative to custom LSI.

The COPS Family includes three different CPU/memory controller chips, as well as a variety of special-purpose drivers and interfaces to handle displays, keyboards, printers, and other peripherals.

National's IDM 2900 Family

The IDM 2900 Bipolar Slice Family from National consists of a series of devices using low-power Schottky TTL technology. The heart of the IDM 2900 family is the IDM 2901A 4-Bit Slice CPU, which has become the industry standard in slice architecture. An outstanding feature of the IDM 2900 family is that they may be used in sundry combinations to emulate a multitude of CPU architectures – in contrast to fixed-instruction microprocessors, which can execute only one set of instructions. Also, the word length of an IDM 2900-based microprocessor may be any multiple of 4 bits. Each IDM 2900 device performs a basic function, which is controlled by an appropriate microinstruction of a microprogrammed system.

The fast bipolar speed, the design flexibility, and the 4-bit-slice feature of the IDM 2900 Family add to the already broad base of microprocessors and support devices available from National Semiconductor.

National's PACE Family

PACE is a complete, 16-bit "minicomputer on a chip." Its wide word length, hardware-vectored interrupt structure, and sophisticated addressing modes make it ideal for laboratory instrumentation, data acquisition and process control applications, where number handling and fast response are most important.

Among the outstanding features of PACE are its 8-bit or 16-bit data handling, exceptional data-processing throughput, compatibility with National's IMP-16 microprocessors, large variety of support chips, CPU and memory application cards for prototyping and production runs, a low-cost development system, and a sophisticated and more-powerful development system (which includes a full complement of software). Best of all PACE, family components are in volume production NOW.

National's IMP-16 Family

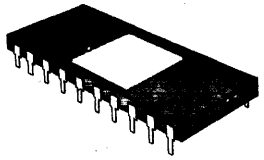
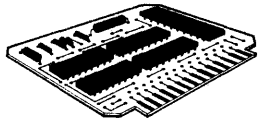
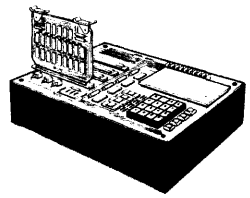
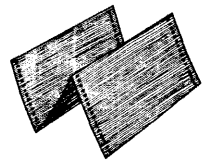
IMP-16, brother to PACE, is the most versatile of the 16-bit processors. Offering the user an expandable, bit-slice architecture and a variety of instruction sets, IMP-16 is uniquely suited to complex control, analysis, and data-reduction tasks.

Included in the IMP-16 family is the IMP-16P development system, which is supported by a full complement of software. Additionally available are CPU, memory, arithmetic, and input/output application cards.

National's IMP-16 microprocessors have been the forerunners of the industry and have proven their usefulness and applicability, in National's own DATACHECKER point-of-sale system, for example.

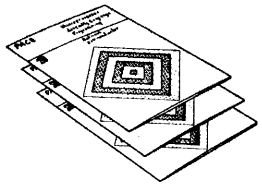
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SC/MP 8-Bit Microprocessor Family

	NEW ■	PART NUMBER	DESCRIPTION
	**Chips**	ISP-8A/500D	SC/MP CPU Chip
	■	ISP-8A/600D/N	SC/MP-II CPU Chip
	■	DP8304D	Bus Transceiver
	■	ISP-8A/650D/N	128 x 8 RAM with 16 Prog. I/O Ports
	■	INS2656	ROM/RAM/I/O
	■	MM5235	8K x 8 ROM
	**Cards**	ISP-8C/100	SC/MP CPU Card with 256 x 8 RAM, 512 x 8 ROM/PROM Socket
	■	ISP-8C/100N	SC/MP-II CPU Card with 256 x 8 ROM/PROM Socket
		ISP-8C/002N	RAM Card (2K x 8 Static Memory RAM, 512 x 8)
		ISP-8C/004B	PROM/ROM Socket Card – 4K x 8 (accepts 8 MM5204Q/MM5214)
		ISP-8C/004P	PROM/ROM Memory Card – 4K x 8 (with 8 blank MM5204Q)
		IPC-8C/801	Wire Wrap Prototyping Card
	■	ISP-8P/802	Common Bus Cable Card ASM
	**Systems**	ISP-8P/301K	SC/MP-II LCDS Retrofit Kit
		ISP-8P/301	SC/MP Low-Cost Development System (includes CPU Application Card)
	■	ISP-8P/301N	SC-MP-II Low-Cost Development System (includes CPU Application Card)
		ISP-8K/200	SC/MP Kit – An Introductory Package for New Users
	■	ISP-8K/205	SC/MP-II Retrofit Kit
		ISP-8K/220	SC/MP Kit Fully Assembled and Tested
		ISP-8K/400	SC/MP Keyboard Kit – Hex Keyboard/Display
	**Software**	ISP-8S/100C	IMP-16 Based Cross Assembler – 4K (paper tape)
		ISP-8S/101C	IMP-16 Based Macro Cross Assembler – 8K (paper tape)
		ISP-8S/103C	PACE-P Based Macro Cross Assembler – 8K (paper tape)
		ISP-8S/102P	Fortran IV Cross Assembler for 16-Bit Word or Larger Computers
	■	ISP-8F/111	SC/MP-II LCDS Firmware Assembler Package (SUPAK): Line Assembler, Source Editor, P/N Tape Generator (in 8 MM5214 ROMs)
	■	ISP-8F/351	SC/MP-II National Industrial Basic Lang. (NIBL) Firmware (in 8 MM5214 ROMs)
	■	ISP-8F/352	SC/MP-II NIBL Firmware (in 2 MM2316A ROMs)

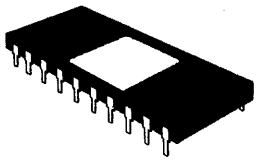
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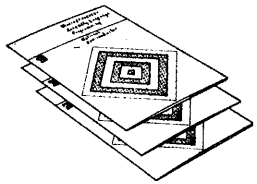


	NEW	PART NUMBER	DESCRIPTION
Literature	■	ISP-8S/994Y	SC/MP Assembly Language Programming Manual
			SC/MP-II Brochure
		4200079A	SC/MP – Technical Description
	■	420305239-001A	SC/MP Applications Handbook
	■		SC/MP-II Data Sheet (ISP-8A/600)
	■		SC/MP Data Sheet (ISP-8A/500)

2650 8-Bit Microprocessor Family

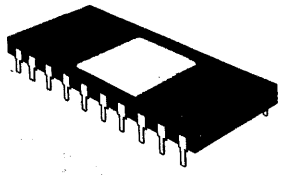


	NEW	PART NUMBER	DESCRIPTION
Chips	■	INS2650A	Single 5V, 8-Bit CPU
	■	INS2651	USART/Baud Rate Gen
	■	INS2652	Multi Protocol Comm. (SDLC)
	■	INS2655	Programmable I/O Parallel, Serial, Timer
	■	INS2656	RAM, ROM, I/O

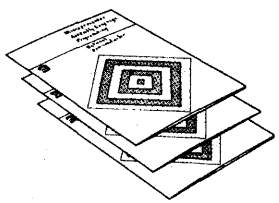


	NEW		DESCRIPTION
Literature	■		2650 Series Data Sheets

8080A 8-Bit Microprocessor Family



	NEW ■	PART NUMBER	DESCRIPTION
Chips		INS8080AD/−1/−2	8-Bit CPU, 2μsec/1.3μsec/1.5μsec Cycle
		DP8224D/N	Clock Generator
		DP8228D/N	System Controller
		DP8238D/N	System Controller
		DP8212N/J	8-Bit I/O Port
		INS8255D	Programmable Peripheral Interface
		INS8251D	Programmable Communications Interface
		DP8216/26N/J	4-Bit Bi-Directional Bus Driver
	■	INS8253	Programmable Timer
	■	INS8257	Programmable DMA Controller
	■	INS8259	Programmable Interrupt Controller
	■	INS1671	ASTRO Communications Interface
	■	INS1771−1	Floppy Disc Controller
	■	INS2651	USART/Baud Rate Gen.
	■	INS2652	Multi Protocol Comm. (SDLC)
	■	BP8350	Programmable CRT Controller
	■	INS2656	ROM/RAM/I/O
	■	ISP-8A/650D/N	128 x 8 RAM with 16 Prog. I/O Ports
		MM2708Q	1K x 8 Erasable PROM
		MM2316A	2K x 8 ROM
	■	MM5235	8K x 8 ROM

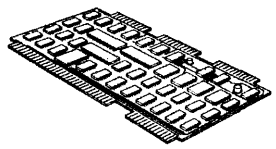
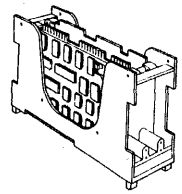
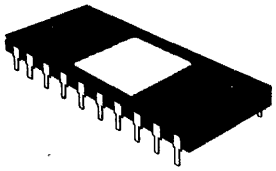
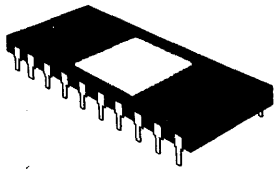
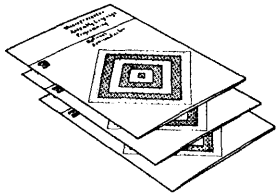


Literature			INS8080A Data Sheet
			INS8080A−1/−2 Data Sheet
			DP8212 Data Sheet
			DP8224 Data Sheet
			DP8228/38 Data Sheet
	■		INS8255 Data Sheet
	■	INS-8A/900	System Design Manual

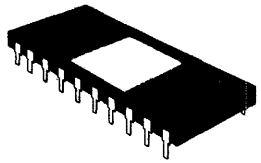
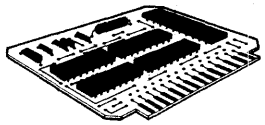
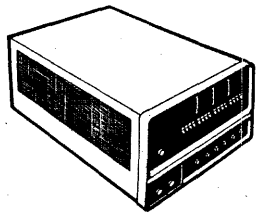
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Series/80 Microcomputer Family

	NEW ■		PART NUMBER	DESCRIPTION
	Cards	■	BLC 80/10	Board Level Computer
		■	BLC 016	16K RAM Memory Board
		■	BLC 406	6K ROM/PROM Expansion Board
		■	BLC 905	Universal Prototyping Board
		■	BLC 104	Memory I/O Expansion Board
		■	BLC 508	I/O Expansion Board
		■	BLC 416	16K ROM/PROM Expansion Board
	Systems	■	BLC 80P	Prototyping Package
		■	BLC 604	Card Cage with Backplane
		■	BLC 614	Expansion Card Cage with Backplane
	Firmware	■	BLC 910	Prototyping System Monitor
	Chips	■	BLC 901	220Ω/330Ω Terminator
		■	BLC 902	1kΩ Terminator
	Literature	■	BLC 80P	Prototyping Package Users Manual
		■	BLC 80/10	Hardware Reference Manual
		■	BLC 016	Hardware Reference Manual
		■	BLC 406	Hardware Reference Manual
		■	BLC 104	Hardware Reference Manual
		■	BLC 508	Hardware Reference Manual
		■	BLC 416	Hardware Reference Manual

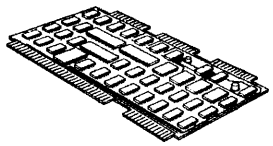
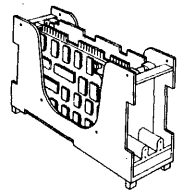
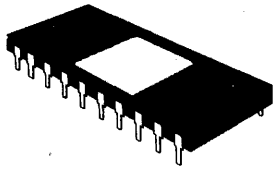
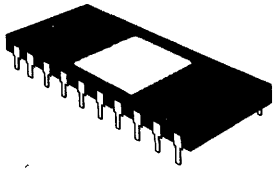
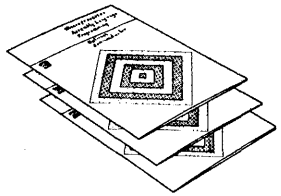
PACE 16-Bit Microprocessor Family

	NEW ■		PART NUMBER	DESCRIPTION
	Chips		IPC-16A/520D	PACE CPU Chip (750ns)
			DP8300N	Monolithic Bus Transceiver (BTE)
			DP8301D	Monolithic 8-Bit I/O Port (MILE)
			DP8302J	Monolithic System Timing Element (STE)
	Cards		IPC-16C/100	PACE CPU Card
			IMP-16C/001B	ROM/PROM Socket Card – 1K x 16 Capacity (MM5203Q)
			IPC-16C/001P	ROM/PROM Card with 1K x 16 (eight) MM5203Q's Inserted
			IPC-16C/002B	ROM/PROM Socket Card – 2K x 16 Capacity (MM5204Q)
			IPC-16C/002P	ROM/PROM Card with 2K x 16 (eight) MM5204Q's Inserted
			IPC-16C/001	RAM Card with 1K x 16 (MM2102) Memory
		■	IPC-16C/011	LCDS Common Bus RAM Card 1K x 16 (MM2102) Memory
		■	IPC-16C/012B	LCDS Common Bus ROM/PROM Socket Card with 2K x 16 Capacity (MM5204Q)
		■	IPC-16C/012P	LCDS Common Bus ROM/PROM Card with 2K x 16 (eight) MM5204Q's Inserted
			IPC-16C/801	Wire Wrap Prototyping Card
		■	IPC-16P/802	Common Bus Cable Card ASM
	Systems		IPC-16P/108	PACE 8K Development System†
			IPC-16P/108H	PACE 8K Development System and Heavy Duty† Supply
			(All Above Include Complete Resident System Software – IPC-16S/901C)	
			IPC-16P/004A	PACE Development System Static RAM Card (4K x 16)
			IPC-16P/008B	PACE Development System ROM/PROM Socket Card (8K x 16)
			IPC-16P/008P	PACE Development ROM/PROM Card (8K x 16)
			IPC-16P/301	PACE Low Cost Development System (LCDS)

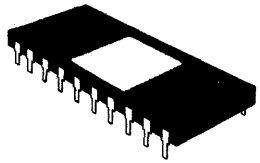
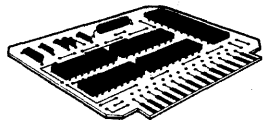
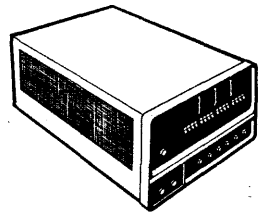
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Series/80 Microcomputer Family

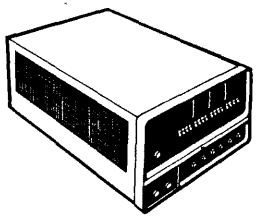
	NEW ■		PART NUMBER	DESCRIPTION
	Cards	■	BLC 80/10	Board Level Computer
		■	BLC 016	16K RAM Memory Board
		■	BLC 406	6K ROM/PROM Expansion Board
		■	BLC 905	Universal Prototyping Board
		■	BLC 104	Memory I/O Expansion Board
		■	BLC 508	I/O Expansion Board
		■	BLC 416	16K ROM/PROM Expansion Board
	Systems	■	BLC 80P	Prototyping Package
		■	BLC 604	Card Cage with Backplane
		■	BLC 614	Expansion Card Cage with Backplane
	Firmware	■	BLC 910	Prototyping System Monitor
	Chips	■	BLC 901	220Ω/330Ω Terminator
		■	BLC 902	1kΩ Terminator
	Literature	■	BLC 80P	Prototyping Package Users Manual
		■	BLC 80/10	Hardware Reference Manual
		■	BLC 016	Hardware Reference Manual
		■	BLC 406	Hardware Reference Manual
		■	BLC 104	Hardware Reference Manual
		■	BLC 508	Hardware Reference Manual
		■	BLC 416	Hardware Reference Manual

PACE 16-Bit Microprocessor Family

	NEW ■		PART NUMBER	DESCRIPTION
	Chips		IPC-16A/520D	PACE CPU Chip (750ns)
			DP8300N	Monolithic Bus Transceiver (BTE)
			DP8301D	Monolithic 8-Bit I/O Port (MILE)
			DP8302J	Monolithic System Timing Element (STE)
	Cards		IPC-16C/100	PACE CPU Card
			IMP-16C/001B	ROM/PROM Socket Card – 1K x 16 Capacity (MM5203Q)
			IPC-16C/001P	ROM/PROM Card with 1K x 16 (eight) MM5203Q's Inserted
			IPC-16C/002B	ROM/PROM Socket Card – 2K x 16 Capacity (MM5204Q)
			IPC-16C/002P	ROM/PROM Card with 2K x 16 (eight) MM5204Q's Inserted
			IPC-16C/001	RAM Card with 1K x 16 (MM2102) Memory
		■	IPC-16C/011	LCDS Common Bus RAM Card 1K x 16 (MM2102) Memory
		■	IPC-16C/012B	LCDS Common Bus ROM/PROM Socket Card with 2K x 16 Capacity (MM5204Q)
		■	IPC-16C/012P	LCDS Common Bus ROM/PROM Card with 2K x 16 (eight) MM5204Q's Inserted
			IPC-16C/801	Wire Wrap Prototyping Card
		■	IPC-16P/802	Common Bus Cable Card ASM
	Systems		IPC-16P/108	PACE 8K Development System†
			IPC-16P/108H	PACE 8K Development System and Heavy Duty† Supply
			(All Above Include Complete Resident System Software – IPC-16S/901C)	
			IPC-16P/004A	PACE Development System Static RAM Card (4K x 16)
			IPC-16P/008B	PACE Development System ROM/PROM Socket Card (8K x 16)
			IPC-16P/008P	PACE Development ROM/PROM Card (8K x 16)
			IPC-16P/301	PACE Low Cost Development System (LCDS)

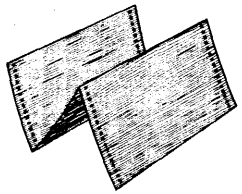
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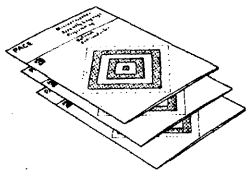
Systems

	IPC-16P/100	IMP16/PACE System Conversion Kit (CPU Card, PACE Software and Development System Firmware)
	IPC-16P/805	PROM Programmer for Development System
	IPC-16P/812	Centronics Printer
■	IPC-16P/840	Floppy Disc Operating System: Dual Floppy Disc Drive; Interface Card; ROM Resident Firmware Card; Software on Diskette (requires 12K Memory)
	IPC-16P/852	Paper Tape Reader (Plessey 1000 cps)



Software

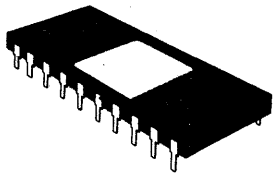
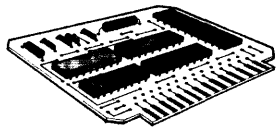
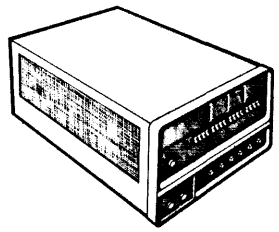
	IPC-16S/101C	IMP-16 Based Cross Assembler – 8K Memory Required (paper tape)
	IPS-16S/102P	Fortran IV Cross Assembler for 16-Bit or Larger Word Computers (Cards)
	IPC-16S/201C	Basic Interpreter – 8K Memory Required (paper tape)
	IPC-16S/901C	Resident System Software Package: Source Editor; 4K, 8K and Conversational Assemblers, Absolute and General Loaders; Hardware Diagnostics; plus DEBUG and Utility Software (paper tape)
		IMP/16 PACE Translator and PACE Cross Assembler Available Through Timeshare Utility Companies
■	IPC-16S/902M	Floppy Disc Operating System Software Package on Diskette (copies)



Literature

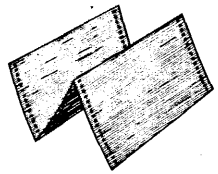
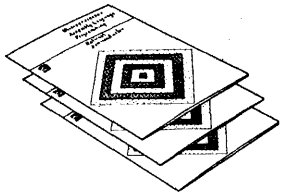
	IPC-16A/927	Logic Designer's Guide
■	IPC-16A/928	System Design Manual
■	IPC-16S/969Y	Assembly Language Programming Manual
■	IPC-16P/840Y	PACE DOS Users Manual
■	IPC-16S/201Y	PACE Basic Users Manual
■	IPC-16P/301Y	PACE LCDS Users Manual
■	IPC-16P/108Y	PACE Development System Users Manual
		IPC-16A/520 Data Sheet
		DP8300N Data Sheet
		DP8302J Data Sheet

IMP-16 16-Bit Microprocessor Family

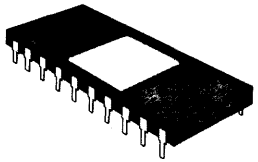
	NEW ■	PART NUMBER	DESCRIPTION
	Chips	IMP-00A/520N/D	Register, Arithmetic and Logic Unit (RALU)
		IMP-16A/521N/D	Control Read Only Memory (CROM)
		IMP-16A/522N/D	CROM – Extended 16-Bit, 17 Instruction Set
		IMP-16A/523D	CROM – With POWR I/O Instruction Set
		IMP-16A/524D	CROM – With Extended Arithmetic Instruction Set
		IMP-16A/500N/D	Chip Set (4-520 RALUs & 1-521 CROM)
	■	IMP-16A/502N/D	Chip Set (4-520 RALUs & 1-521 CROM & 1-522 CROM)
	Cards	IMP-16C/200A	16-Bit Microprocessor System on 8½" x 11" PCB
		IMP-16C/300	IMP-16C/200A + IMP-16A/522N
		IMP-16C/400	16-Bit Microprocessor 1K RAM, 1K ROM
		IMP-16C/500	IMP-16C/400 + IMP-16A/522N
		IMP-16P/004A	4K x 16 Static RAM Card
	■	IMP-16P/008B/P	8K x 16 PROM/ROM Card
	■	IMP-16L/300	16-Bit Microprocessor, with Extended Instruction Set
	■	IMP-16L/004	4K x 16 Dynamic RAM Card, with DMA Port
	■	IMP-16L/006B/P	2K x 16 Static RAM and 4K x 16 ROM/PROM
	Systems	IMP-16P/208	Development System, 8K x 16 RAM†
		IMP-16P/308	IMP-16P/208 + IMP-16A/522N CROM†
		IMP-16P/208H	Development System, 8K x 16 RAM, and Heavy Duty Power Supply†
		IMP-16P/308H	Development System, 8K x 16 RAM, IMP-16A/522N, and Heavy Duty Power Supply†
		IMP-16P/805	PROM Programmer
		IMP-16P/812	Centronics Printer
		IMP-00/852	Paper Tape Reader (Plessey 1000 cps)
		IMP-16P/840	Dual-Drive Floppy Disk Subsystem (Shugart)
	■	IMP-16L/308	Development System, 8K x 16 RAM†
	■	IMP-16L/805	PROM Programmer
	■	IMP-16L/812	Centronics Printer

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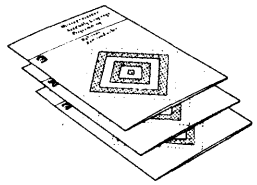
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	Software		IMP-16S/900	FORTRAN IV Cross Assembler for 16-Bit Word or Larger Computers
			IMP-16S/901C	Resident System Software Package Including 4K, 8K and Conversational Assemblers; Absolute and General Loaders; Hardware Diagnostics; plus Debug and Utility Software (paper tape)
			IMP-16S/902M	Complete Resident System Software Package on Diskette (2 copies) with Listings IMP Cross-Assembler Version Also Available Through Timeshare Utility Companies.
	Literature	■	IMP-16C/921	IMP-16C Application Manual
			IMP-16L/928	IMP-16L Users Manual
			IMP-16P/937	IMP-16P Users Manual
			IMP-16S/102Y	IMP-16 Programming and Assembler Manual RALU Data Sheet – IMP-00A/520 CROM Data Sheet – IMP-16A/521 POWR I/O Tech. Description – IMP-16A/984 Arithmetic CROM Tech. Description – IMP-16A/993

2900 Bit-Slice Microprocessor Family

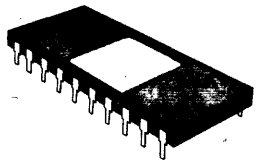


	NEW ■	PART NUMBER	DESCRIPTION
Chips	■	IDM2901A	4-Bit Slice Microprocessor
	■	IDM2902	Carry Look-Ahead Generator
	■	IDM2909	Microsequencer
	■	IDM2911	Microsequencer
	■	IDM29702	16 x 4 Bit RAM (Open Collector)
	■	IDM29703	16 x 4 Bit RAM (Tri-State)
	■	IDM29750	32 x 8 PROM (Open Collector)
	■	IDM29751	32 x 8 Bit PROM (Tri-State)
	■	IDM29760	256 x 4 Bit PROM (Tri-State)
	■	IDM29760	256 x 4 Bit PROM (Open Collector)
	■	IDM29761	256 x 4 Bit PROM (Tri-State)
	■	IDM29803	16-Way Branch Controller
	■	IDM29811	Next Address Controller
	■	DM74LS374	Octal Tri-State Register
		DM74148J/N	Priority Encoder
		DM85S68D/N	16 x 4 Bit Clocked RAM
		DM87S202	256 x 8 ROM with Output Latches
	■	DM87S222	256 x 8 PROM with Output Latches



Literature		2900-Bit Slice System Manual and Data Sheets

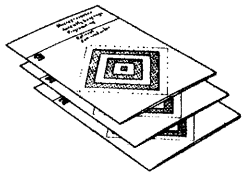
4004 4-Bit Microprocessor Family (FIPS)



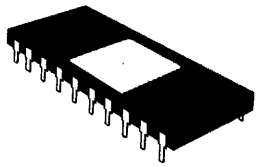
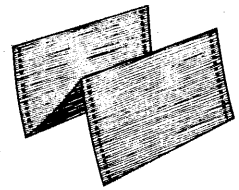
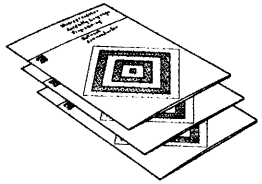
	NEW ■	PART NUMBER	DESCRIPTION
Chips		INS4001XXX/N/D	ROM
		INS4002-1N/D	RAM (SRC 0, 1)
		INS4002-2N/D	RAM (SRC 3, 4)
		INS4003N/D	Shift Register
		INS4004D	CPU
		INS4008N/D	Address Latch
		INS4009N/D	Multiplexer
		INS4201N/J	Clock
		INS4702AD/AQ	Reprogrammable PROM

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	Literature		FIPS Data Sheet – 4000 Series (001 - 009) INS4201/DP4201 Data Sheet INS4702AD/AQ Data Sheet

COPS 4-Bit Microprocessor Family

	NEW ■		PART NUMBER	DESCRIPTION
	Chips	■	MM57129	4K x 8 ROM
		■	MM5781	2K x 8 ROM
		■	MM5782	CPU and RAM
		■	MM5799	Single Chip Processor 1.5K x 8 ROM 96 x 4 RAM
		■	MM57140	Single Chip Processor 630 x 8 ROM 55 x 4 RAM
	Software	■		Copmonitor – Cross Assembler and COPS System Emulator to Run On IMP-16P System
	Literature	■		Individual Device Data Sheets Programming Manual

Support Devices and Literature

	NEW ■		PART NUMBER	DESCRIPTION
Universal Interface			DP8212N/J	8-Bit I/O Port
			INS8255D	Programmable Parallel Interface
			81LS95/98	Tri-State® Octal Buffers
			DM8542N	Quad I/O Register
			MM74C173/174N	4-Bit CMOS Latches
			DM74173/174N	4-Bit Tri-State® Latches
			DM74LS173/174N	4-Bit Low Power Schottky Latches
			DM8546N	Tri-State® 8-Bit Universal I/O Shift Reg.
			LM555CN/556CN	Interval Timer
			DM74147N/748N	Priority Encoder (Interrupt/DMA Control)
			DS8833N	Tri-State® Quad Bus XCVR
			DS8835N	Bi-Directional Bus Driver Inv.
			DM74LS138N	1-of-8 Binary Decoder (replaces Intel 8205)
			DP8301D	Monolithic 8-Bit I/O Port
		■	DP8304	Octal Bus Driver
		■	INS8253	Programmable Timer
		■	INS8257	Programmable DMA Controller
		■	INS8259	Programmable Interrupt Controller
		■	BP8350	Programmable CRT Controller
Human Interface			MM74C922/3	16 & 20-Key Keyboard Encoders
			MM5740AAX/N	90-Key Keyboard Encoder
			DM8544N	Tri-State® Quad Switch Debouncer
			DS8859, 69N	Hex Latch/Led Driver
			CD4511CN	7-Segment Latch Decoder Driver
			DS8692, 3, 4	Seiko Printer Interface Set
			DM8678XXX/N/J	CRT Character Generator
Instrument & Machine Interface			DM8334N	8-Bit Bit-Addressable Latch
			ADC0800PCN	8-Bit A-to-D Converter
			ADC1210, 11	CMOS A-to-D Converter (12/10 Bit)
			DAC1200, 02CN	12-Bit D-to-A Converter (Binary/BCD)
			CD4051CN	8-Ch. Analog Mux/Demux
			DAC1201, 03CN	10-Bit D-to-A Converter
Memory with Input/Output		■	INS2656	ROM/RAM/I/O
			ISP-8A/650D/N	128 x 8 RAM with 16 Prog I/O Port
RAMs			MM2114	1k x 4 Static RAM
			MM5257	4k x 1 Static RAM
			MM2102/2N	1k x 1 Static RAM
			MM5269N	256 x 4 Static RAM with Latched Inputs
			MM5270, 80D	4k x 1 Dynamic RAMs
			MM74C920D	1k x 1 CMOS Static RAM
			MM2111-2N	256 x 4 Static RAM, Common I/O
			MM2102AN-4	1k x 1 Static RAM, 450ns

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ROMs			MM5214N	512 x ROM
			MM5242N	1k x 8 NMOS ROM
			MM2316A	2k x 8 ROM
			DM85S28XXX/J/N	1k x 8 ROM (Pinout Similar to MM2708)
		■	MM5235	8K x 8 ROM
PROMs			DM2704N	512 x 8 PROM with 2708 Pinouts
			MM5204Q	512 x 8 Erasable PROM
			MM1702AQ	256 x 8 Erasable PROM
			MM2708Q	1k x 8 Erasable PROM
			DM87S222N	256 x 8 PROM with Latched Inputs (20 pin DIP)
			DM74S472N	512 x 8 PROM (20 pin DIP)
			DM87S296N	512 x 8 PROM
Communications			MM5307AA/N	Baud Rate Gen./Prog. Real Time Clock
			MM5303N	UART
			INS57101	Asynchronous Communication Element
			INS8251	Programmable Communications Interface
		■	INS1671	Astro Communications Interface
		■	INS1771-1	Floppy Disc Controller
		■	INS2651	USART/Baud Rate Gen.
		■	INS2652	Multi Protocol Comm. (SDLC)
Literature				TTL Products Catalog
				Interface Products Catalog
				Special Function Products Catalog
				Memory Products Catalog
		■		Microprocessor Full Spectrum Brochure
		■		Microprocessor Cards & System Brochure
		■		Microprocessor Training Brochure

INS8080A 8-Bit N-Channel Microprocessor

general description

The INS8080A is an 8-bit microprocessor housed in a standard, 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate MOS technology, functions as the central processing unit (CPU) in National Semiconductor's N8080 microcomputer family.

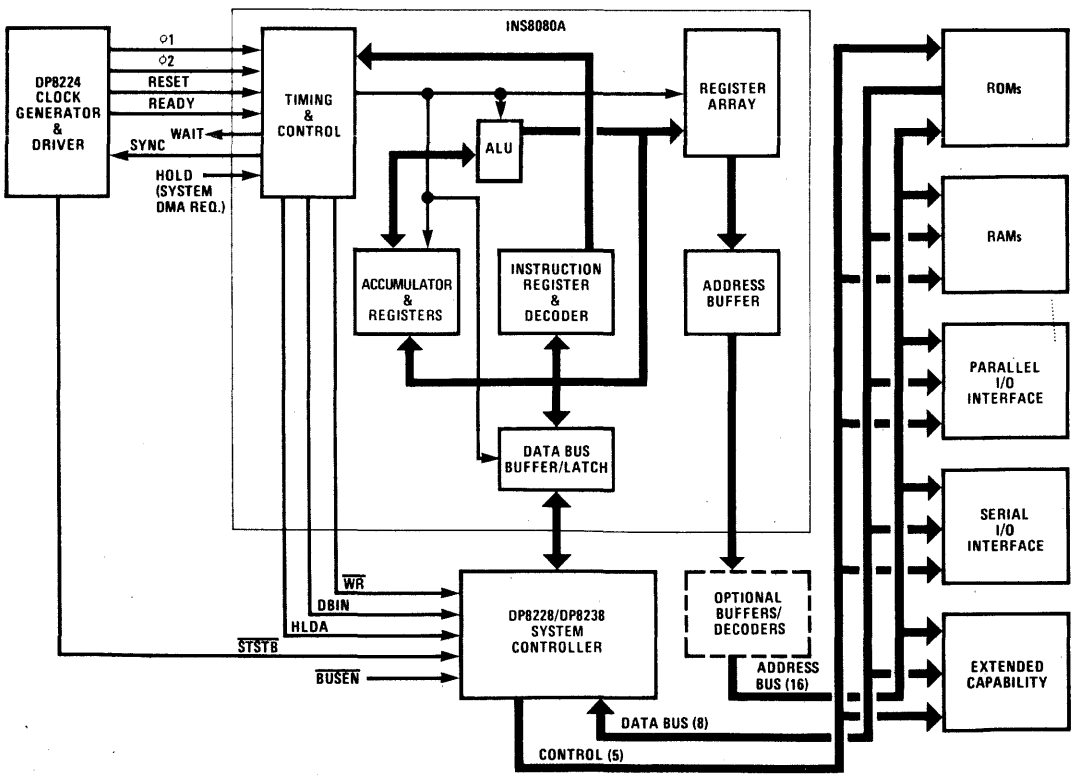
The INS8080A has a 16-bit address bus that is capable of addressing up to 65k bytes of memory and up to 256 input and 256 output devices. Data is routed to and from the INS8080A on a separate bidirectional 8-bit bus. This data bus is also TRI-STATE®, making direct memory addressing (DMA) and multiprocessing applications possible. The INS8080A directly provides signals to control the interface to memory and I/O ports. All buses, including control, are TTL compatible.

An asynchronous interrupt capability is included in the INS8080A to allow external signals to change the instruction sequence. The interrupting device may vector the program to a particular service routine location (or some other direct function) by specifying an interrupt instruction to be executed.

features

- 2μs Instruction Cycle
- Variable Length Instructions
- General Purpose Registers – Six plus an Accumulator
- Direct Addressing up to 65k Bytes
- Variable Length Stack Accessed by 16-bit Stack Pointer
- Addresses 256 Input and 256 Output Ports
- Provisions for Vectored Interrupts
- TRI-STATE® Bus for DMA and Multiprocessing Capability
- TRI-STATE TTL Drive Capabilities for Address and Data Buses
- Decimal Arithmetic Capability
- Multiple Addressing Modes
  - Direct
  - Register
  - Register Indirect
  - Immediate
- Direct Plug-in Replacement for Intel 8080A

N8080A microcomputer family block diagram



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absolute maximum ratings

Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . -65°C to +150°C
All Input or Output Voltages
with Respect to V_{BB} . . . . . -0.3V to +20V
V_{CC}, V_{DD} and V_{SS} with Respect to V_{BB} . . -0.3V to +20V
Power Dissipation 1.5W

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

dc electrical characteristics

T_A = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, unless otherwise noted.

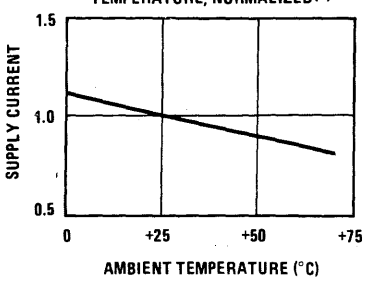
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	V_{SS}-1		V_{SS}+0.8	V	
V_{IHC}	Clock Input High Voltage	9.0		V_{DD}+1	V	
V_{IL}	Input Low Voltage	V_{SS}-1		V_{SS}+0.8	V	
V_{IH}	Input High Voltage	3.3		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs,
V_{OH}	Output High Voltage	3.7			V	I_{OH} = 150μA.
$I_{DD\,(AV)}$	Avg. Power Supply Current (V_{DD})		40	70	mA	Operation
$I_{CC\,(AV)}$	Avg. Power Supply Current (V_{CC})		60	80	mA	t_{CY} = 0.48μs
$I_{BB\,(AV)}$	Avg. Power Supply Current (V_{BB})		0.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leq V_{CLOCK} \leq V_{DD}$
I_{DL}[2]	Data Bus Leakage in Input Mode			-100	μA	$V_{SS} \leq V_{IN} \leq V_{SS}$ + 0.8V
				-2.0	mA	V_{SS} + 0.8V $\leq V_{IN} \leq V_{CC}$
I_{FL}	Address and Data Bus Leakage			+10	μA	$V_{ADDR/DATA} = V_{CC}$
	During HOLD			-100	μA	$V_{ADDR/DATA} = V_{SS}$ + 0.45V

capacitance

T_A = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V, V_{BB} = -5V

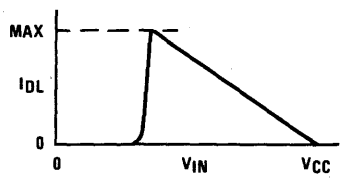
Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pF	f_c = 1MHz
C_{IN}	Input Capacitance	6	10	pF	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pF	Returned to V_{SS}

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED[3]



Notes:
1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pullup will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = -0.45%/°C.

DATA BUS CHARACTERISTIC DURING DBIN



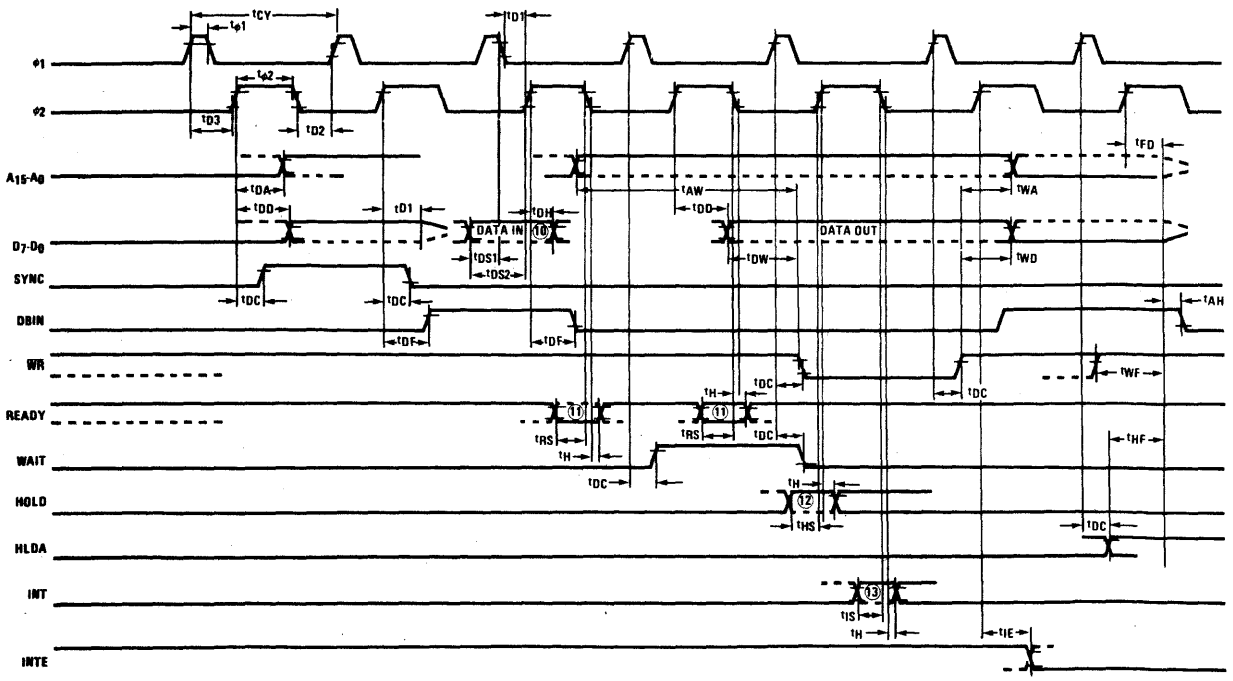
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ac electrical characteristics

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CY} [3]	Clock Period	0.48	2.0	μs	
t_r, t_f	Clock Rise and Fall Time	0	50	ns	
$t_{\phi 1}$	ϕ_1 Pulse Width	60		ns	
$t_{\phi 2}$	ϕ_2 Pulse Width	220		ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0		ns	
t_{D2}	Delay ϕ_2 to ϕ_1	70		ns	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	80		ns	
t_{DA} [2]	Address Output Delay from ϕ_2		200	ns	C_L = 100pF
t_{DD} [2]	Data Output Delay from ϕ_2		220	ns	
t_{DC} [2]	Signal Output Delay from ϕ_1 or ϕ_2 (SYNC, $\overline{WR}$, WAIT, HLDA)		120	ns	C_L = 50pF
t_{DF} [2]	DBIN Delay from ϕ_2	25	140	ns	
t_{DI} [1]	Delay for Input Bus to Enter Input Mode		t_{DF}	ns	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	30		ns	

timing waveforms [14]

Note: Timing measurements are made at the following reference voltages: CLOCK '1' = 8.0V, '0' = 1.0V; INPUTS '1' = 3.3V, '0' = 0.8V; OUTPUTS '1' = 2.0V, '0' = 0.8V.



See notes on following page.

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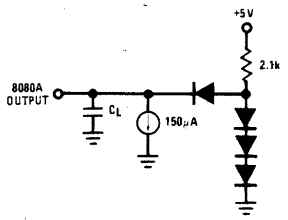
ac electrical characteristics (cont'd.)

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	150		ns	
t_{DH} [1]	Data Hold Time from ϕ_2 During DBIN	1		ns	
t_{IE} [2]	INTE Output Delay from ϕ_2		200	ns	C_L = 50pF
t_{RS}	READY Setup Time During ϕ_2	120		ns	
t_{HS}	HOLD Setup Time to ϕ_2	140		ns	
t_{IS}	INT Setup Time During ϕ_2 (During ϕ_1 in Halt Mode)	120		ns	
t_H	Hold Time from ϕ_2 (READY, INT, HOLD)	0		ns	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		120	ns	
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	5		ns	C_L = 100pF : Address, Data C_L = 50pF: $\overline{WR}$, HLDA, DBIN
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	6		ns	
t_{WD} [2]	Output Data Stable from $\overline{WR}$	7		ns	
t_{WA} [2]	Address Stable from $\overline{WR}$	7		ns	
t_{HF} [2]	HLDA to Float Delay	8		ns	
t_{WF} [2]	$\overline{WR}$ to Float Delay	9		ns	
t_{AH} [2]	Address Hold Time After DBIN During HLDA	-20		ns	

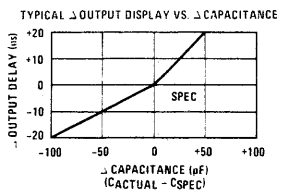
Notes:

1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50ns or t_{DF}, whichever is less.

2. Typical load circuit:

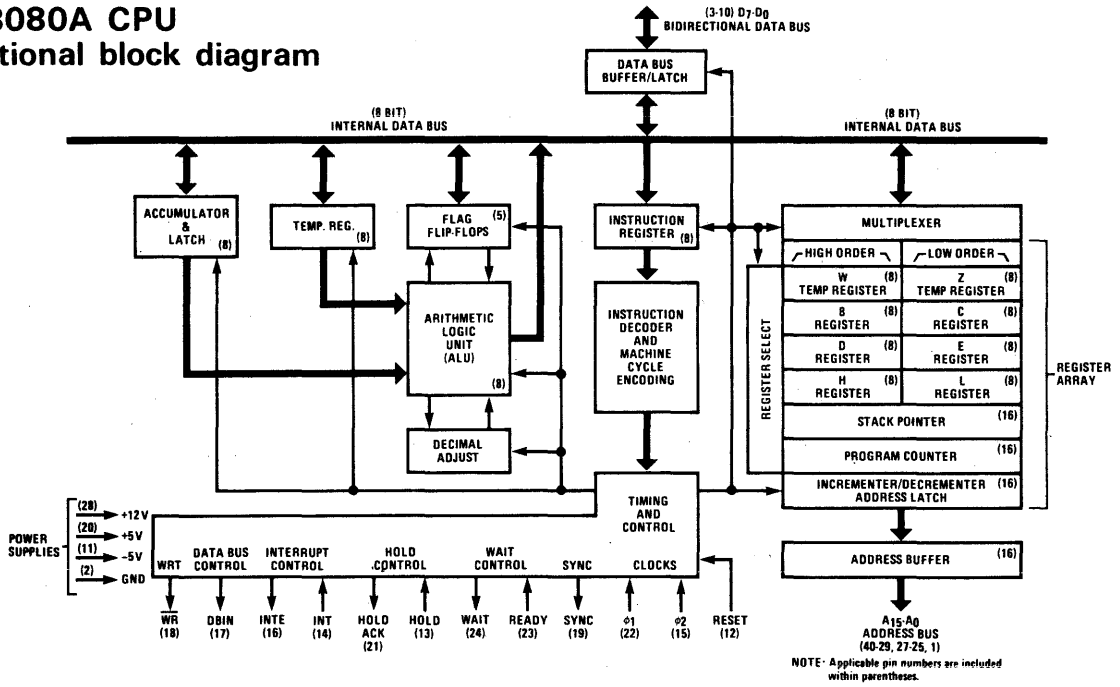


3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{D2} + t_{f\phi2} + t_{r\phi1} \geq 480$ns.



4. The following are relevant when interfacing the INS8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from 0.8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output Delay when measured to 3.0V = SPEC + 60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add 0.6ns/pF if $C_L > C_{SPEC}$, subtract 0.3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2t_{CY} - t_{D3} - t_{r\phi2} - 140$ns.
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 170$ns.
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi2} - 50$ns.
9. $t_{WF} = t_{D3} + t_{r\phi2} - 10$ns.
10. Data in must be stable for this period during DBIN · T_3. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5, and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

INS8080A CPU functional block diagram



INS8080A functional pin definition

The following describes the function of all of the INS8080A input/output pins. Some of these descriptions reference internal timing periods.

INPUT SIGNALS

Ready: When high (logic 1), indicates that valid memory or input data are available to the CPU on the INS8080A data bus. The READY signal is used to synchronize the CPU with slower memory or input/output devices. If the INS8080A does not receive a high READY input after sending out an address to memory or an input/output device, the INS8080A enters a WAIT mode for as long as the READY input remains low (logic 0). The CPU may also be single stepped by the use of the READY signal.

Hold: When high, requests that the CPU enter the HOLD mode. When the CPU is in the HOLD mode, the CPU address and data buses both will be in the high-impedance state. The HOLD mode allows an external device to gain control of the INS8080A address and data buses immediately following the completion of the current machine cycle by the CPU. The CPU acknowledges the HOLD mode via the HOLD ACKNOWLEDGE (HLDA) output line. The HOLD request is recognized under the following conditions:

- The CPU is in the HALT mode.
- The READY signal is active and the CPU is in the t_2 or t_W microcycle.

Interrupt (INT) Request: When high, the CPU recognizes an interrupt request on this line after completing the current instruction or while in the HALT mode. An interrupt request is not honored if the CPU is in the HOLD mode (HLDA = logic 1) or the Interrupt Enable Flip-flop is reset (INTE = logic 0).

Reset: When activated (high) for a minimum of three clock periods, the content of the Program Counter is cleared and the Interrupt Enable and Hold Acknowledge Flip-flops are reset. Following a RESET, program execution starts at memory location 0. It should be noted that the status flags, accumulator, stack pointer, and registers are not cleared during the RESET sequence.

ϕ_1 and ϕ_2 Clocks: Two non-TTL compatible clock phases which provide nonoverlapping timing references for internal storage elements and logic circuits of the CPU.

+12 Volts: V_{DD} Supply.

+5 Volts: V_{CC} Supply.

-5 Volts: V_{BB} Supply.

Ground: V_{SS} (0 volt) reference.

OUTPUT SIGNALS

Synchronizing (SYNC) Signal: When activated (high), the beginning of a new machine cycle is indicated and the status word is outputted on the Data Bus.

Address (A_{15} - A_0) Bus: This bus comprises sixteen TRI-STATE output lines. The bus provides the address to memory (up to 65k bytes) or denotes the input/output device number for up to 256 input and 256 output peripherals.

Wait: When high, acknowledges that the CPU is in the WAIT mode.

Write ($\overline{WR}$): When low, the data on the data bus are stable for WRITE memory or output operation.

Hold Acknowledge (HLDA): Goes high in response to a logic 1 on the HOLD line and indicates that the data and address bus will go to the high-impedance state. The HLDA begins at one of the following times:

- The t_3 microcycle of a READ memory input operation.
- The clock period following the t_3 microcycle of a WRITE memory output operation.

In both cases, the HLDA signal starts after the rising edge of the ϕ_1 clock, and high impedance occurs after the rising edge of the ϕ_2 clock.

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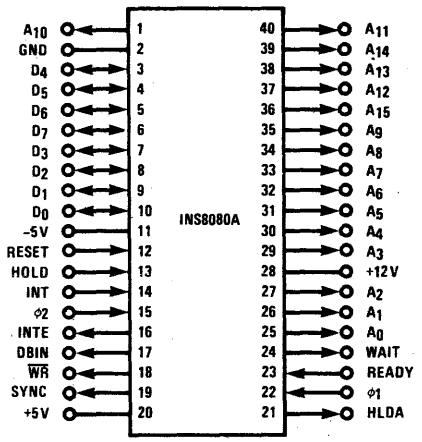
Interrupt Enable (INTE): Indicates the content of the internal Interrupt Enable Flip-flop. The Enable and Disable Interrupt (EI and DI) Instructions cause the Interrupt Enable Flip-flop to be set and reset, respectively. When the flip-flop is reset (INTE = logic 0), it inhibits interrupts from being accepted by the CPU. In addition, the Interrupt Enable Flip-flop is automatically reset (thereby disabling further interrupts) at the t_1 microcycle of the instruction fetch cycle, when an interrupt is accepted; it is also reset by the RESET Signal.

Data Bus In (DBIN): When high, indicates to external circuits that the data bus is in the input mode. The DBIN Signal should be used to gate data from memory or an I/O device onto the Data Bus.

INPUT/OUTPUT SIGNALS

Data ($D_7 - D_0$) Bus: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communication between the CPU, memory, and input/output devices for instructions and data transfers. A status word (which describes the current machine cycle) is also outputted on the data bus during the first microcycle of each machine cycle (SYNC = logic 1).

pin configuration



8080A status

Instructions for the 8080A require from one to five machine cycles for complete execution. The 8080A sends out 8 bits of status information on the data bus at the beginning of each machine cycle (during SYNC time). The following table defines the status information.

Status Information Definition

Symbols	Data Bus Bit	Definition
INTA*	D_0	Acknowledge signal for INTERRUPT request. Signal should be used to gate a restart instruction onto the data bus when DBIN is active.
$\overline{WO}$	D_1	Indicates that the operation in the current machine cycle will be a WRITE memory or OUTPUT function (WO = 0). Otherwise, a READ memory or INPUT operation will be executed.
STACK	D_2	Indicates that the address bus holds the pushdown stack address from the Stack Pointer.
HLTA	D_3	Acknowledge signal for HALT Instruction.
OUT	D_4	Indicates that the address bus contains the address of an output device and the data bus will contain the output data when WR is active.
M_1	D_5	Provides a signal to indicate that the CPU is in the fetch cycle for the first byte of an instuction.
INP*	D_6	Indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when DBIN is active.
MEMR*	D_7	Designates that the data bus will be used for memory read data.

*These three status bits can be used to control the flow of data onto the INS8080A data bus.

Status Word Chart

Machine Cycle	Type	Data Bus Bit							
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction Fetch	1	1	0	1	0	0	0	1	0
Memory Read	2	1	0	0	0	0	0	1	0
Memory Write	3	0	0	0	0	0	0	0	0
Stack Read	4	1	0	0	0	0	1	1	0
Stack Write	5	0	0	0	0	0	1	0	0
Input Read	6	0	1	0	0	0	0	1	0
Output Write	7	0	0	0	1	0	0	0	0
Interrupt Acknowledge	8	0	0	1	0	0	0	1	1
Halt Acknowledge	9	1	0	0	0	1	0	1	0
Interrupt Acknowledge While Halt	10	0	0	1	0	1	0	1	1

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instruction set

Mnemonic		Description	Operation	Op Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	No. of Bytes	No. of Machine (M) Cycles	No. of μcycles (T)	Condition Flags S	Z	AC	P	CY
DATA TRANSFER GROUP																			
LDA		Load Accumulator Direct	(A) ← ((byte 3)(byte 2))	0	0	1	1	1	0	1	0	3	4	13					
LDAX	B	Load Accumulator Indirect	(A) ← ((B))	0	0	0	0	1	0	1	0	1	2	7					
LDAX	D	Load Accumulator Indirect	(A) ← ((D))	0	0	0	1	1	0	1	0	1	2	7					
LHLD		Load H and L Direct	(L) ← ((byte 3)(byte 2)) (H) ← ((byte 3)(byte 2) + 1)	0	0	1	0	1	0	1	0	3	5	16					
LXI	B	Load Immediate, Registers B and C	(B) ← (byte 3) (C) ← (byte 2)	0	0	0	0	0	0	0	1	3	3	10					
LXI	D	Load Immediate, Registers D and E	(D) ← (byte 3) (E) ← (byte 2)	0	0	0	1	0	0	0	1	3	3	10					
LXI	H	Load Immediate, Registers H and L	(H) ← (byte 3) (L) ← (byte 2)	0	0	1	0	0	0	0	1	3	3	10					
LXI	SP	Load Immediate, Stack Pointer	(SPH) ← (byte 3) (SPL) ← (byte 2)	0	0	1	1	0	0	0	1	3	3	10					
MOV	M, r	Move to Memory	((H)(L)) ← (r)	0	1	1	1	0	*S*	*S*	*S*	1	2	7	(Flags Not Affected)				
MOV	r, M	Move from Memory	(r) ← ((H)(L))	0	1	*D*	*D*	*D*	1	1	0	1	2	7					
MOV	r1, r2	Move Registers	(r1) ← (r2)	0	1	*D*	*D*	*D*	*S*	*S*	*S*	1	1	5					
MVI	M	Move to Memory Immediate	((H)(L)) ← (byte 2)	0	0	1	1	0	1	1	0	2	3	10					
MVI	r	Move Immediate	(r) ← (byte 2)	0	0	*D*	*D*	*D*	1	1	0	2	2	7					
SHLD		Store H and L Direct	((byte 3)(byte 2)) ← (L) ((byte 3)(byte 2) + 1) ← (H)	0	0	1	0	0	0	1	0	3	5	16					
STA		Store Accumulator Direct	((byte 3)(byte 2)) ← (A)	0	0	1	1	0	0	1	0	3	4	13					
STAX	B	Store Accumulator Indirect	((B)) ← (A)	0	0	0	0	0	0	1	0	1	2	7					
STAX	D	Store Accumulator Indirect	((D)) ← (A)	0	0	0	1	0	0	1	0	1	2	7					
XCHG		Exchange H and L with D and E	(H) ↔ (D) (L) ↔ (E)	1	1	1	0	1	0	1	1	1	1	4					
ARITHMETIC GROUP																			
ACI		Add Immediate with Carry	(A) ← (A) + (byte 2) + (CY)	1	1	0	0	1	1	1	0	2	2	7	‡	‡	‡	‡	‡
ADC	M	Add Memory with Carry	(A) ← (A) + ((H)(L)) + (CY)	1	0	0	0	1	1	1	0	1	2	7	‡	‡	‡	‡	‡
ADC	r	Add Register with Carry	(A) ← (A) + (r) + (CY)	1	0	0	0	1	*S*	*S*	*S*	1	1	4	‡	‡	‡	‡	‡
ADD	M	Add Memory	(A) ← (A) + ((H)(L))	1	0	0	0	0	1	1	0	1	2	7	‡	‡	‡	‡	‡
ADD	r	Add Register	(A) ← (A) + (r)	1	0	0	0	0	*S*	*S*	*S*	1	1	4	‡	‡	‡	‡	‡
ADI		Add Immediate	(A) ← (A) + (byte 2)	1	1	0	0	0	1	1	0	1	2	7	‡	‡	‡	‡	‡
DAA		Decimal Adjust Accumulator	8-bit number in Accumulator is converted to two 4-bit BCD digits	0	0	1	0	0	1	1	1	1	1	4	‡	‡	‡	‡	‡
DAD	B	Add B and C to H and L	(H)(L) ← (H)(L) + (B)(C)	0	0	0	0	1	0	0	1	1	3	10	·	·	·	·	‡
DAD	D	Add D and E to H and L	(H)(L) ← (H)(L) + (D)(E)	0	0	0	1	1	0	0	1	1	3	10	·	·	·	·	‡
DAD	H	Add H and L to H and L	(H)(L) ← (H)(L) + (H)(L)	0	0	1	0	1	0	0	1	1	3	10	·	·	·	·	‡
DAD	SP	Add Stack Pointer to H and L	(H)(L) ← (H)(L) + (SP)	0	0	1	1	1	0	0	1	1	3	10	·	·	·	·	‡
DCR	M	Decrement Memory	((H)(L)) ← ((H)(L)) − 1	0	0	1	1	0	1	0	1	1	3	10	‡	‡	‡	‡	·
DCR	r	Decrement Register	(r) ← (r) − 1	0	0	*D*	*D*	*D*	1	0	1	1	1	5	‡	‡	‡	‡	·
DCX	B	Decrement Registers B and C	(B)(C) ← (B)(C) − 1	0	0	0	0	1	0	1	1	1	1	5	·	·	·	·	·
DCX	D	Decrement Registers D and E	(D)(E) ← (D)(E) − 1	0	0	0	1	1	0	1	1	1	1	5	·	·	·	·	·
DCX	H	Decrement Registers H and L	(H)(L) ← (H)(L) − 1	0	0	1	0	1	0	1	1	1	1	5	·	·	·	·	·
DCX	SP	Decrement Stack Pointer	(SP) ← (SP) − 1	0	0	1	1	1	0	1	1	1	1	5	·	·	·	·	·
INR	M	Increment Memory	((H)(L)) ← ((H)(L)) + 1	0	0	1	1	0	1	0	0	1	3	10	‡	‡	‡	‡	·
INR	r	Increment Register	(r) ← (r) + 1	0	0	*D*	*D*	*D*	1	0	0	1	1	5	‡	‡	‡	‡	·
INX	B	Increment Registers B and C	(B)(C) ← (B)(C) + 1	0	0	0	0	0	0	1	1	1	1	5	·	·	·	·	·
INX	D	Increment Registers D and E	(D)(E) ← (D)(E) + 1	0	0	0	1	0	0	1	1	1	1	5	·	·	·	·	·
INX	H	Increment Registers H and L	(H)(L) ← (H)(L) + 1	0	0	1	0	0	0	1	1	1	1	5	·	·	·	·	·
INX	SP	Increment Stack Pointer	(SP) ← (SP) + 1	0	0	1	1	0	0	1	1	1	1	5	·	·	·	·	·
SBB	M	Subtract Memory with Borrow	(A) ← (A) − ((H)(L)) − (CY)	1	0	0	1	1	1	1	0	1	2	7	‡	‡	‡	‡	‡
SBB	r	Subtract Register with Borrow	(A) ← (A) − (r) − (CY)	1	0	0	1	1	*S*	*S*	*S*	1	1	4	‡	‡	‡	‡	‡
SBI		Subtract Immediate with Borrow	(A) ← (A) − (byte 2) − (CY)	1	1	0	1	1	1	1	0	2	2	7	‡	‡	‡	‡	‡
SUB	M	Subtract Memory	(A) ← (A) − ((H)(L))	1	0	0	1	0	1	1	0	1	2	7	‡	‡	‡	‡	‡
SUB	r	Subtract Register	(A) ← (A) − (r)	1	0	0	1	0	*S*	*S*	*S*	1	1	4	‡	‡	‡	‡	‡
SUI		Subtract Immediate	(A) ← (A) − (byte 2)	1	1	0	1	0	1	1	0	2	2	7	‡	‡	‡	‡	‡
LOGICAL GROUP																			
ANA	M	AND Memory	(A) ← (A) ∧ ((H)(L))	1	0	1	0	0	1	1	0	1	2	7	‡	‡	·	‡	0
ANA	r	AND Register	(A) ← (A) ∧ (r)	1	0	1	0	0	*S*	*S*	*S*	1	1	4	‡	‡	·	‡	0
ANI		AND Immediate	(A) ← (A) ∧ (byte 2)	1	1	1	0	0	1	1	0	2	2	7	‡	‡	·	‡	0
CMA		Complement Accumulator	(A) ← ($\overline{A}$)	0	0	1	0	1	1	1	1	1	1	4	·	·	·	·	·
CMC		Complement Carry	(CY) ← ($\overline{CY}$)	0	0	1	1	1	1	1	1	1	1	4	·	·	·	·	‡
CMP	M	Compare Memory	(A) — ((H)(L))	1	0	1	1	1	1	1	0	1	2	7	‡	‡[a]	‡	‡	‡[a]
CMP	r	Compare Register	(A) — (r)	1	0	1	1	1	*S*	*S*	*S*	1	1	4	‡	‡[b]	‡	‡	‡[b]
CPI		Compare Immediate	(A) — (byte 2)	1	1	1	1	1	1	1	0	2	2	7	‡	‡[c]	‡	‡	‡[c]
ORA	M	OR Memory	(A) ← (A) ∨ ((H)(L))	1	0	1	1	0	1	1	0	1	2	7	‡	‡	0	‡	0
ORA	r	OR Register	(A) ← (A) ∨ (r)	1	0	1	1	0	*S*	*S*	*S*	1	1	4	‡	‡	0	‡	0
ORI		OR Immediate	(A) ← (A) ∨ (byte 2)	1	1	1	1	0	1	1	0	2	2	7	‡	‡	0	‡	0
RAL		Rotate Left through Carry	(A_{n+1}) ← (A_n); (CY) ← (A_7) (A_0) ← (CY)	0	0	0	1	0	1	1	1	1	1	4	·	·	·	·	‡
RAR		Rotate Right through Carry	(A_n) ← (A_{n+1}); (CY) ← (A_0) (A_7) ← (CY)	0	0	0	1	1	1	1	1	1	1	4	·	·	·	·	‡
RLC		Rotate Left	(A_{n+1}) ← (A_n); (A_0) ← (A_7) (CY) ← (A_7)	0	0	0	0	0	1	1	1	1	1	4	·	·	·	·	‡
RRC		Rotate Right	(A_n) ← (A_{n-1}); (A_7) ← (A_0) (CY) ← (A_0)	0	0	0	0	1	1	1	1	1	1	4	·	·	·	·	‡
STC		Set Carry	(CY) ← 1	0	0	1	1	0	1	1	1	1	1	4	·	·	·	·	1
XRA	M	Exclusive OR Memory	(A) ← (A) ∀ ((H)(L))	1	0	1	0	1	1	1	0	1	2	7	‡	‡	0	‡	0
XRA	r	Exclusive OR Register	(A) ← (A) ∀ (r)	1	0	1	0	1	*S*	*S*	*S*	1	1	4	‡	‡	0	‡	0
XRI		Exclusive OR Immediate	(A) ← (A) ∀ (byte 2)	1	1	1	0	1	1	1	0	2	2	7	‡	‡	0	‡	0

Notes: a. Z = 1 if (A) = (H)(L); CY = 1 if (A) < (H)(L)
b. Z = 1 if (A) = (r); CY = 1 if (A) < (r)
c. Z = 1 if (A) = (byte 2); CY = 1 if (A) < (byte 2)

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instruction set (cont'd.)

Mnemonic	Description	Operation	Op Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	No. of Bytes	No. of Machine (M) Cycles	No. of μcycles (T)	Condition Flags S	Z	AC	P	CY
BRANCH GROUP																		
CALL	Call Unconditional	((SP) – 1) ← (PCH) ((SP) – 2) ← (PCL) (SP) ← (SP) – 2 (PC) ← (byte 3)(byte 2)	1	1	0	0	1	1	0	1	3	5	17					
CC	Call on Carry	If CY = 1, ((SP) – 1) ← (PCH) ((SP) – 2) ← (PCL) (SP) ← (SP) – 2 (PC) ← (byte 3)(byte 2)	1	1	0	1	1	1	0	0	3	3/5	11/17					
CM	Call on Minus	If S = 1, ((SP) – 1) ← (PCH) ((SP) – 2) ← (PCL) (SP) ← (SP) – 2 (PC) ← (byte 3)(byte 2)	1	1	1	1	1	1	0	0	3	3/5	11/17					
CNC	Call on No Carry	If CY = 0, ((SP) – 1) ← (PCH) ((SP) – 2) ← (PCL) (SP) ← (SP) – 2 (PC) ← (byte 3)(byte 2)	1	1	0	1	0	1	0	0	3	3/5	11/17					
CNZ	Call on Not Zero	If Z = 0, ((SP) – 1) ← (PCH) ((SP) – 2) ← (PCL) (SP) ← (SP) – 2 (PC) ← (byte 3)(byte 2)	1	1	0	0	0	1	0	0	3	3/5	11/17	(Flags Not Affected)				
CP	Call on Positive	If S = 0, ((SP) – 1) ← (PCH) ((SP) – 2) ← (PCL) (SP) ← (SP) – 2 (PC) ← (byte 3)(byte 2)	1	1	1	1	0	1	0	0	3	3/5	11/17					
CPE	Call on Parity Even	If P = 1, ((SP) – 1) ← (PCH) ((SP) – 2) ← (PCL) (SP) ← (SP) – 2 (PC) ← (byte 3)(byte 2)	1	1	1	0	1	1	0	0	3	3/5	11/17					
CPO	Call on Parity Odd	If P = 0, ((SP) – 1) ← (PCH) ((SP) – 2) ← (PCL) (SP) ← (SP) – 2 (PC) ← (byte 3)(byte 2)	1	1	1	0	0	1	0	0	3	3/5	11/17					
CZ	Call on Zero	If Z = 1, ((SP) – 1) ← (PCH) ((SP) – 2) ← (PCL) (SP) ← (SP) – 2 (PC) ← (byte 3)(byte 2)	1	1	0	0	1	1	0	0	3	3/5	11/17					
JC	Jump on Carry	If CY = 1, (PC) ← (byte 3)(byte 2)	1	1	0	1	1	0	1	0	3	3	10					
JM	Jump on Minus	If S = 1, (PC) ← (byte 3)(byte 2)	1	1	1	1	1	0	1	0	3	3	10					
JMP	Jump Unconditional	(PC) ← (byte 3)(byte 2)	1	1	0	0	0	0	1	1	3	3	10					
JNC	Jump on No Carry	If CY = 0, (PC) ← (byte 3)(byte 2)	1	1	0	1	0	0	1	0	3	3	10					
JNZ	Jump on Not Zero	If Z = 0, (PC) ← (byte 3)(byte 2)	1	1	0	0	0	0	1	0	3	3	10					
JP	Jump on Positive	If S = 0, (PC) ← (byte 3)(byte 2)	1	1	1	1	0	0	1	0	3	3	10					
JPE	Jump on Parity Even	If P = 1, (PC) ← (byte 3)(byte 2)	1	1	1	0	1	0	1	0	3	3	10					
JPO	Jump on Parity Odd	If P = 0, (PC) ← (byte 3)(byte 2)	1	1	1	0	0	0	1	0	3	3	10					
JZ	Jump on Zero	If Z = 1, (PC) ← (byte 3)(byte 2)	1	1	0	0	1	0	1	0	3	3	10					
PCHL	H and L to Program Counter	(PCH) ← (H) (PCL) ← (L)	1	1	1	0	1	0	0	1	1	1	5					
RC	Return on Carry	If CY = 1, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	1	1	0	0	0	1	1/3	5/11					
RET	Return	(PCL) ← ((SP)); (PCH) ← ((SP) + 1); (SP) ← (SP) + 2;	1	1	0	0	1	0	0	1	1	3	10					
RM	Return on Minus	If S = 1, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	1	1	0	0	0	1	1/3	5/11					
RNC	Return on No Carry	If CY = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	1	0	0	0	0	1	1/3	5/11					
RNZ	Return on Not Zero	If Z = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	0	0	0	0	0	1	1/3	5/11					
RP	Return on Positive	If S = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	1	0	0	0	0	1	1/3	5/11					
RPE	Return on Parity Even	If P = 1, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	0	1	0	0	0	1	1/3	5/11					
RPO	Return on Parity Odd	If P = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	0	0	0	0	0	1	1/3	5/11					

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instruction set (cont'd.)

Mnemonic	Description	Operation	Op Code D_7 D_6 D_5 D_4	Op Code D_3 D_2 D_1 D_0	No. of Bytes	No. of Machine (M) Cycles	No. of μcycles (T)	Condition Flags S	Z	AC	P	CY
BRANCH GROUP (continued)												
RST	Restart	((SP) − 1) ← (PCH) ((SP) − 2) ← (PCL) (SP) ← (SP) − 2 (PC) ← 8 * (NNN)	1 1 *N* *N*	*N* 1 1 1	1	3	11					
RZ	Return on Zero	If Z = 1, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1 1 0 0	1 0 0 0	1	1/3	5/11					
STACK, I/O, AND MACHINE CONTROL GROUP												
DI	Disable Interrupts	The Interrupt system is disabled following the execution of the DI instruction.	1 1 1 1	0 0 1 1	1	1	4	·	·	·	·	·
EI	Enable Interrupts	The interrupt system is enabled following the execution of next instruction.	1 1 1 1	1 0 1 1	1	1	4	·	·	·	·	·
HLT	Halt	Processor is stopped; registers and flags are unaffected.	0 1 1 1	0 1 1 0	1	1	7	·	·	·	·	·
IN	Input	(A) ← (data)	1 1 0 1	1 0 1 1	2	3	10	·	·	·	·	·
NOP	No Operation	No operation is performed; registers and flags are unaffected.	0 0 0 0	0 0 0 0	1	1	4	·	·	·	·	·
OUT	Output	(data) ← (A)	1 1 0 1	0 0 1 1	2	3	10	·	·	·	·	·
POP B	Pop Registers B and C off Stack	(C) ← ((SP)) (B) ← ((SP) + 1) (SP) ← (SP) + 2	1 1 0 0	0 0 0 1	1	3	10	·	·	·	·	·
POP D	Pop Registers D and E off Stack	(D) ← ((SP)) (E) ← ((SP) + 1) (SP) ← (SP) + 2	1 1 0 1	0 0 0 1	1	3	10	·	·	·	·	·
POP H	Pop Registers H and L off Stack	(H) ← ((SP)) (L) ← ((SP) + 1) (SP) ← (SP) + 2	1 1 1 0	0 0 0 1	1	3	10	·	·	·	·	·
POP PSW	Pop Accumulator and Flags off Stack	(CY) ← $((SP))_0$ (P) ← $((SP))_2$ (AC) ← $((SP))_4$ (Z) ← $((SP))_6$ (S) ← $((SP))_7$ (A) ← ((SP) + 1) (SP) ← (SP) + 2	1 1 1 1	0 0 0 1	1	3	10	‡	‡	‡	‡	‡
PUSH B	Push Registers B and C on Stack	((SP) − 1) ← (B) ((SP) − 2) ← (C) (SP) ← (SP) − 2	1 1 0 0	0 1 0 1	1	3	11	·	·	·	·	·
PUSH D	Push Registers D and E on Stack	((SP) − 1) ← (D) ((SP) − 2) ← (E) (SP) ← (SP) − 2	1 1 0 1	0 1 0 1	1	3	11	·	·	·	·	·
PUSH H	Push Registers H and L on Stack	((SP) − 1) ← (H) ((SP) − 2) ← (L) (SP) ← (SP) − 2	1 1 1 0	0 1 0 1	1	3	11	·	·	·	·	·
PUSH PSW	Push Accumulator and Flags on Stack	((SP) − 1) ← (A) $((SP) - 2)_0$ ← (CY) $((SP) - 2)_1$ ← 1 $((SP) - 2)_2$ ← (P) $((SP) - 2)_3$ ← 0 $((SP) - 2)_4$ ← (AC) $((SP) - 2)_5$ ← 0 $((SP) - 2)_6$ ← (Z) $((SP) - 2)_7$ ← (S) (SP) ← (SP) − 2	1 1 1 1	0 1 0 1	1	3	11	·	·	·	·	·
SPHL	Move H and L to Stack Pointer	(SP) ← (H)(L)	1 1 1 1	1 0 0 1	1	1	5	·	·	·	·	·
XTHL	Exchange Top of Stack with H and L	(L) ↔ ((SP)) (H) ↔ ((SP) + 1)	1 1 1 0	0 0 1 1	1	5	18	·	·	·	·	·

condition flags and standard rules

There are five condition flags associated with the execution of instructions on the INS8080A. They are Zero, Sign, Parity, Carry, and Auxiliary Carry, and each flag is represented by a 1-bit register in the CPU. A flag is "set" by forcing the bit to 1, "reset" by forcing the bit to 0. The bit positions of the flags are indicated in the PUSH and POP PSW instructions.

Unless indicated otherwise, when an instruction affects a flag, it affects it in the following manner:

ZERO (Z): If the result of an instruction has the value 0, this flag is set; otherwise, it is reset.

SIGN (S): If the most significant bit of the result of the operation has the value 1, this flag is set; otherwise, it is reset.

PARITY (P): If the modulo 2 sum of the bits of the result of the operation is 0 (that is, if the result has even parity), this flag is set; otherwise, it is reset (that is, if the result has odd parity).

CARRY (CY): If the instruction resulted in a carry (from addition) or a borrow (from subtraction or a comparison) out of the high-order bit, this flag is set; otherwise, it is reset.

AUXILIARY CARRY (AC): If the instruction caused a carry out of bit 3 and into bit 4 of the resulting value, the auxiliary carry is set; otherwise, it is reset. This flag is affected by single-precision additions, subtractions, increments, decrements, comparisons, and logical operations; however, AC is used principally with additions and increments preceding a DAA (Decimal Adjust Accumulator) Instruction.

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symbols and abbreviations

The following symbols and abbreviations are used in the subsequent description of the INS8080A instructions:

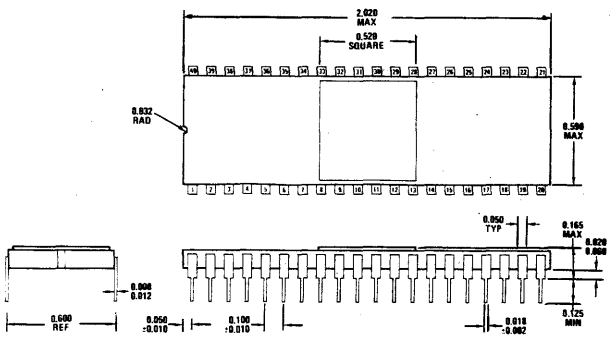
Symbols	Meaning
A	Register A (Accumulator)
B	Register B
C	Register C
D	Register D
H	Register H
L	Register L
DDD, SSS	The bit pattern designating one of the registers A, B, C, D, E, H, L (DDD = destination, SSS = source):

DDD or SSS	Register Name
111	A
000	B
001	C
010	D
011	E
100	H
101	L

byte 2	The second byte of the instruction
byte 3	The third byte of the instruction
port	8-bit address of an I/O device
r, r1, r2	One of the registers A, B, C, D, E, H, L

Symbols	Meaning
PC	16-bit program counter register (PCH and PCL are used to refer to the high-order and low-order 8 bits respectively.)
SP	16-bit stack pointer register (SPH and SPL are used to refer to the high-order and low-order 8 bits respectively.)
( )	The contents of the memory location or registers enclosed in the parentheses
←	"Is replaced by"
∧	Logical AND
∀	Exclusive OR
V	Inclusive OR
+	Addition
−	Twos complement subtraction
*	Multiplication
↔	"Exchange"
—	The ones complement (for example, $(\overline{A})$)
n	The restart number 0 through 7
NNN	The binary representation 000 through 111 for restart number 0 through 7 respectively
•	"Not affected"
0	"Reset"
1	"Set"
x	Unknown
↕	Flags affected according to Standard Rules

physical dimensions



Ceramic Dual-In-Line Package (D)
Order Number INS8080AD

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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National Semiconductor

IDM2901A 4-Bit Bipolar Microprocessor

General Description

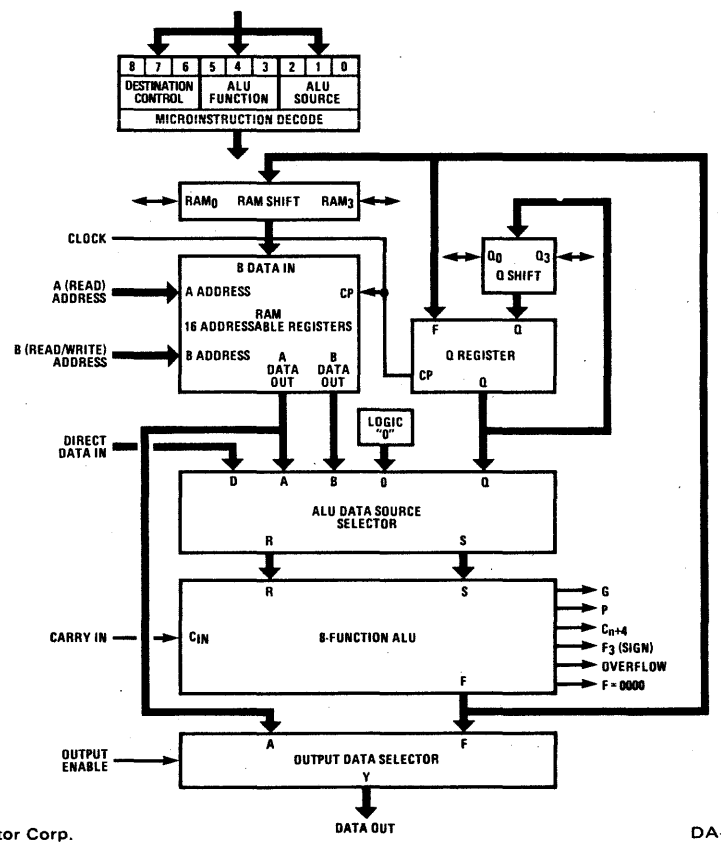
The IDM2901A 4-bit bipolar microprocessor slice is a cascadable device designed for use in Central Processing Units, programmable microprocessors, peripheral controllers, and other "high-speed" applications where economy, hardware/software flexibility, and easy expansion are system prerequisites. The building-block architecture and microinstruction format of the IDM2901A permits efficient emulation of most digital-based systems.

As shown in the simplified block diagram, the IDM2901A device consists of a 16-word by 4-bit 2-port RAM, a high-speed ALU, and the required shifting, decoding, and multiplexing circuits. The 9-bit microinstruction word is organized into three groups of three bits each – the first group (bits 0 - 2) selects ALU source operands, the second group (bits 3 - 5) selects the ALU function, and the last group (bits 6 - 8) selects the destination register within the ALU. The slice microprocessor is cascadable with full look-ahead or ripple carry; all outputs are TRI-STATE® and four status-flag outputs are available. To minimize power consumption and to maximize speed and reliability, the 40-pin LSI chip is fabricated using state-of-the-art (Low-Power Schottky) technology.

Features and Benefits

- **Multiple-address architecture** – improves system speed by providing simultaneous yet independent access to two working registers.
- **Multifunction ALU** – performs addition, two subtraction operations, and five logic functions on two source operands.
- **Flexible data-source selection** – for every ALU function, data is selected from five source ports for a total of 203 source operand pairs.
- **Left/right shift independent of ALU** – an arithmetic operation and a left or right shift can be obtained on the same machine cycle.
- **Four status flags** – carry, overflow, zero, and functional sign are available as outputs.
- **Expandable** – Connect any number of IDM2901As together for longer word lengths.
- **Microprogrammable** – three groups of 3 bits each for source operand, ALU function, and destination control.

Block Diagram



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Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +6.3 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

Operating Range

P/N	Ambient Temperature	V_{CC}
IDM2901A DC, PC	0°C to +70°C	4.75 V to 5.25 V
IDM2901A DM, FM	−55°C to +125°C	4.50 V to 5.50 V

Standard Screening (Conforms to MIL-STD-883 for Class C parts)

Step	MIL-STD-883 Method	Conditions	Level	
			DC, PC	DM, FM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C: 24-hour 150°C	100%	100%
Temperature Cycle	1010	C: −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B: 10,000 G	100%	100%
Fine Leak	1014	A: 5×10^{-8} atm-cc/cm^3	100%	100%
Gross Leak	1014	C2: Fluorocarbon	100%	100%
Electrical Test Subgroups 1 and 7 and 9	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B Parts				
Group A Sample Tests	5005	See below for definitions of subgroups		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 5
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 5

Additional Screening for Class B Parts

Step	MIL-STD-883 Method	Conditions	Level
			DMB, FMB
Burn-In	1015	D: 125°C, 160 hours min	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

Group A Subgroups

(as defined in MIL-STD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum rated temperature
11	Switching	Minimum rated temperature

Electrical Characteristics Over Operating Range

Symbol	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output High Voltage	V_{CC} = min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6 mA; $Y_0/Y_1/Y_2/Y_3$	2.4			V
			I_{OH} = −1.0 mA; C_{n+4}	2.4			
			I_{OH} = −800 μA; OVR/P	2.4			
			I_{OH} = −600 μA; F_3	2.4			
			I_{OH} = −600 μA; $RAM_{0,3}/Q_{0,3}$	2.4			
			I_{OH} = −1.6 mA; $\overline{G}$	2.4			

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Electrical Characteristics (cont'd.)

Symbol	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
I_{CEX}	Output Leakage Current for F = 0 Output	V_{CC} = min; V_{OH} = 5.5 V, V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output Low Voltage	V_{CC} = min; V_{IN} = V_{IH} or V_{IL}		I_{OL} = 20 mA (Com'l) $Y_0/Y_1/Y_2/Y_3$			0.5	V
				I_{OL} = 16 mA (Mil); $Y_0/Y_1/Y_2/Y_3$			0.5	
				I_{OL} = 16 mA; G/F = 0			0.5	
				I_{OL} = 10 mA; C_{n+4}			0.5	
				I_{OL} = 10 mA; OVR/$\overline{P}$			0.5	
				I_{OL} = 8 mA; $F_3/RAM_{0,3}/Q_{0,3}$			0.5	
V_{IH}	Input High Level	Guaranteed input logical high voltage for all inputs			2.0			V
V_{IL}	Input Low Level	Guaranteed input logical low voltage for all inputs					0.8	V
V_I	Input Clamp Voltage	V_{CC} = min; I_{IN} = −18 mA					−1.5	V
I_{IL}	Input Low Current	V_{CC} = max; V_{IN} = 0.5 V		Clock/$\overline{OE}$/C_n			−0.36	mA
				$A_0/A_1/A_2/A_3$			−0.36	
				$B_0/B_1/B_2/B_3$			−0.36	
				$D_0/D_1/D_2/D_3$			−0.36	
				$I_0/I_1/I_2/I_6$			−0.36	
				$I_3/I_4/I_5$			−0.36	
				I_7/I_8			−0.72	
				$RAM_{0,3}/Q_{0,3}$ (Note 4)			−0.36	
I_{IH}	Input High Current	V_{CC} = max; V_{IN} = 2.7 V		Clock/OE			20	μA
				$A_0/A_1/A_2/A_3$			20	
				$B_0/B_1/B_2/B_3$			20	
				$D_0/D_1/D_2/D_3$			20	
				$I_0/I_1/I_2/I_6/I_8$			20	
				$I_3/I_4/I_5/I_7$			20	
				$RAM_{0,3}/Q_{0,3}$ (Note 4)			100	
				C_n			20	
I_I	Input High Current	V_{CC} = max; V_{IN} = 5.5 V					1.0	mA
I_{OZH}, I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = max	$Y_0/Y_1/Y_2/Y_3$	V_O = 2.4 V			50	μA
				V_O = 0.5 V			−50	
			$RAM_{0,3}/Q_{0,3}$	V_O = 2.4 V (Note 4)			100	
				V_O = 0.5 V (Note 4)			−360	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = 5.75 V, V_O = 0.5 V	$Y_0/Y_1/Y_2/Y_3/G$		−30		−85	mA
			C_{n+4}		−30		−85	
			OVR/$\overline{P}$		−30		−85	
			F_3		−30		−85	
			$RAM_{0,3}/Q_{0,3}$		−30		−85	
I_{CC}	Power Supply Current (Note 6)	V_{CC} = max	T_A = 25°C			180	250	mA
			DC	T_A = 0°C to +70°C		180	265	
				T_A = +70°C		180	230	
			DM	T_C = −55°C to +125°C		180	280	
				T_C = +125°C		180	190	

Note 1: For conditions shown as min or max, use the appropriate value specified under Electrical Characteristics for the applicable device type.

Note 2: Typical limits are at V_{CC} = 5.0 V, 25° C ambient, and maximum loading.

Note 3: Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Note 4: These are TRI-STATE outputs internally connected to PNP inputs. Input characteristics are measured with $I_{6,7,8}$ in a state such that the TRI-STATE output is off (high-impedance).

Note 5: "Mil" = IDM2901A DM, FM; "Com'l" = IDM2901A DC, PC.

Note 6: Worst case I_{CC} is at minimum temperature.

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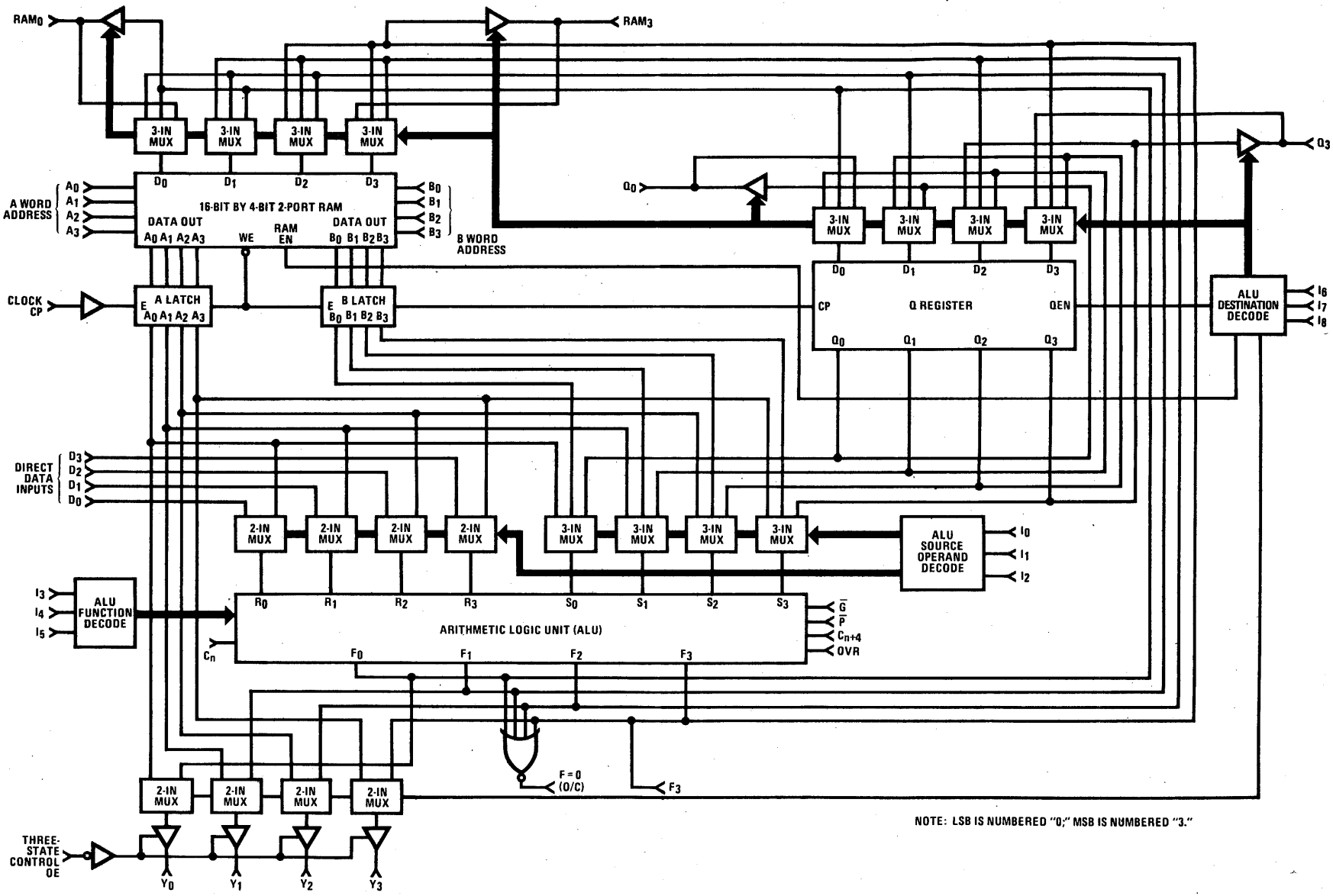


Figure 1. IDM2901A Microprocessor, Detailed Block Diagram

Figure 1 shows a detailed block diagram of the IDM2901A. Observe that all data paths are 4 bits wide; however, the 4-bit slice can be cascaded to the number of bits required for a particular application. Although all parts of the bipolar device are important, the two key elements are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Any one of the 16 words in RAM can be read from the A-port (A_3-A_0) or the B-port (B_3-B_0); the selected word for the A-port is determined by the 4-bit A-address field, whereas the B-address field controls the output of the B-port. If the two address codes are identical, the same file data appears simultaneously at both output ports (A and B).

When enabled by RAM EN, new data is written into the file "word" defined by the B-address field; the write function is implemented when the clock input is low.

Each bit of data to be written is input via a 3-input multiplexer; this scheme permits shifting up one bit position (from LSB towards MSB), shifting down one bit position (from MSB towards LSB), or not shifting at all. A similar scheme is used when data is written into the "Q" register.

Each of the A and B data ports drives an associated 4-bit latch. These latches hold the RAM data while the clock input is low; consequently, any possibility of race conditions when writing new data is eliminated.

The high-speed ALU can perform three binary arithmetic and five logic operations on the two 4-bit input words (R_3-R_0 and S_3-S_0). The R-input field is driven from a 2-input multiplexer, whereas the S-input field is driven by a 3-input multiplexer. Both the R- and S-multiplexers have an inhibit capability, where no data is passed – this is equivalent to a "zero" source operand. Referring to figure 1, observe that the A-port output of the RAM and the 4-bit direct-data inputs (D_3-D_0) are connected to the R-input multiplexers; the S-input multiplexer has three inputs – one from the A-port of RAM, one from the B-port of RAM, and one from the Q-register.

With the foregoing input-multiplexer scheme, the inputs (A, B, D, Q, and "Zero"), when taken in pairs, provide any one of ten source operands for the ALU – AB, AD, AQ, A0, BD, BQ, B0, DQ, D0, and Q0. When the A and B address fields for RAM are identical, it is clear that certain combinations (AD/BD, AQ/BQ, and A0/B0) are redundant; that is, the identical function is implemented for either operand. Only seven of the combinations are completely nonredundant. Eight of the ten combinations (source operands) are implemented by the IDM2901A microprocessor. The ALU source operands are selected by three microinstruction inputs – I_0, I_1, and I_2. These inputs are defined in figure 2. Each of the preceding D and Q operands provides an essential function. The D input (direct-data) is used to load the working registers inside the 2901 device; also, this input source can be used to modify data files within the ALU. The Q-register is an internal 4-bit data source that is well suited for a multiply/divide operation; however, for some applications, it can be used as a data-holding register or as an accumulator.

The ALU is a high-speed arithmetic/logic operator that is capable of performing three binary arithmetic functions and five logic functions. Three microinstruction inputs (I_3, I_4, and I_5) are used to select one of the eight functions; these inputs, along with their octal codes, are defined in figure 3.

Micro Code				ALU Source Operands	
I_2	I_1	I_0	Octal Code	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	O	Q
L	H	H	3	O	B
H	L	L	4	O	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	O

Figure 2. ALU Source Operand Control

Micro Code				ALU Function	Symbol
I_5	I_4	I_3	Octal Code		
L	L	L	0	R Plus S	R + S
L	L	H	1	S Minus R	S – R
L	H	L	2	R Minus S	R – S
L	H	H	3	R OR S	R ∨ S
H	L	L	4	R AND S	R ∧ S
H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
H	H	L	6	R EX-OR S	R ⊻ S
H	H	H	7	R EX-NOR S	$\overline{R \veebar S}$

Figure 3. ALU Function Control

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Normally, the look-ahead carry mode is used when cascading the ALUs of several microprocessor devices. The carry generate ($\overline{G}$) and carry propagate ($\overline{P}$) outputs are suitable for use in a carry-look-ahead generator. A carry-out (C_{n+4}) is also generated and is available for use as the carry flag in a status register or as a ripple-carry output. Both carry-in (C_n) and carry-out (C_{n+4}) are active-high signals. Three other status-oriented outputs are available from the ALU; these are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU, and, without enabling the TRI-STATE outputs, it can be used to determine positive or negative results. When enabled, the logic level of F_3 is identical to that of sign bit Y_3. The F = 0 output is used for zero detect; F = 0 is high when all F outputs are low. The F = 0 output is of the open-collector type and can be wire ORed between microprocessor slices. The overflow (OVR) output is used to flag arithmetic operations that exceed the available twos-complement number range. When an overflow exists (C_{n+3} and C_{n+4} are of opposite polarity), the OVR output is high.

Outputs from the ALU can be stored in the register file or the Q register, or can be transmitted to the outside world. Eight possible destination codes are defined by microinstruction inputs I_6, I_7, and I_8; the various destination control codes are shown in figure 4. The 4-bit data field (Y_3-Y_0) is a TRI-STATE output that can be directly bus organized. The Y outputs are enabled by $\overline{OE}$; when this control signal is high, the Y-outputs are TRI-STATEd. A 2-input multiplexer is also used at the Y-output port to select either the A port of RAM or the F output of the ALU; this selection is controlled by the previously described microinstruction inputs (I_6, I_7, and I_8).

As previously described, the RAM inputs (register file) are driven by a 3-input multiplexer. Thus, outputs from the ALU can be entered nonshifted, shifted up (towards MSB) one position (x 2), or shifted down (towards LSB) one position (÷ 2). The shifter is equipped with two ports — RAM_0 and RAM_3; both ports consist of a TRI-STATE buffer-driver, each of which supplies one input to the foregoing multiplexer. In the shift-up (x 2) mode, the RAM_3 output driver and the RAM_0 multiplexer input are enabled, whereas in the shift-down (÷ 2) mode, the RAM_0 output driver and RAM_3 multiplexer input are enabled; in the no-shift mode, both drivers are TRI-STATE and neither multiplexer input is enabled. The shifter is controlled by the I_6, I_7, and I_8 microinstruction inputs.

The Q register likewise is driven from a 3-input multiplexer and the Q shifter is equipped with two input/output ports — Q_0 and Q_3. Operation of these two ports is similar to that of the RAM shifter, and the ports are controlled by I_6, I_7, and I_8. In the shift-up or shift-down modes, the Q register is shifted in a specified direction with the input/output terminals of the register being an input (for a shift-up) or an output (for a shift-down). In the no-shift mode, the multiplexer may enter the ALU data into the Q register; in this case, input/output lines of the register are TRI-STATE.

The clock input shown in figure 1 controls the RAM, the A and B latches, and the Q register. When the clock input is high, the A and B latches are open and data from the RAM outputs is allowed to pass through to the ALU or "Y" outputs. When the clock input is low, both latches are closed and the last data entered is retained. When the clock input is low and if the input control code (I_6, I_7, and I_8) has enabled a file-write operation, new data, as defined by the 4-bit B-address field, is written into the RAM file. When enabled, data is clocked into the Q register on the low-to-high transition of the clock pulse.

Source Operands and ALU Functions

Any one of eight source operand pairs can be selected by instruction inputs I_0, I_1, and I_2 for use by the ALU; instruction inputs I_3, I_4, and I_5 then control function selection for the ALU — five logic and three arithmetic functions. In the arithmetic mode, the carry input (C_n) also affects the ALU functions; the carry input has no effect on the "F" result in the logic mode. These control parameters (I_6-I_0 and C_n) are summarized in figure 5 to completely define the ALU/source operand functions.

The ALU functions can also be examined on a task basis: that is, add, subtract, AND, OR, and so on. Again, in the arithmetic mode, the carry input will affect the result, whereas in the logic mode it will not. Figures 6 and 7, respectively, define the various logic and arithmetic functions of the ALU; both carry states ($C_n = 0/C_n = 1$) are defined in the function matrices.

Figure 4. ALU Destination Control

Micro Code				RAM Function		Q-Reg. Function		Y Output	RAM Shifter		Q Shifter	
I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
L	L	L	0	X	None	None	F → Q	F	X	X	X	X
L	L	H	1	X	None	X	None	F	X	X	X	X
L	H	L	2	None	F → B	X	None	A	X	X	X	X
L	H	H	3	None	F → B	X	None	F	X	X	X	X
H	L	L	4	Down	F/2 → B	Down	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
H	L	H	5	Down	F/2 → B	X	None	F	F_0	IN_3	Q_0	X
H	H	L	6	Up	2F → B	Up	2Q → Q	F	IN_0	F_3	IN_0	Q_3
H	H	H	7	Up	2F → B	X	None	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a TRI-STATE output which is in the high-impedance state.
B = Register Addressed by B inputs.
Up is toward MSB, Down is toward LSB.

Figure 5. Source Operand and ALU Function Matrix

	$I_{2,1,0}$ Octal	0	1	2	3	4	5	6	7
Octal $I_{5,4,3}$	ALU Source / ALU Function	A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L R Plus S C_n = H	A + Q Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q − A − 1 Q − A	B − A − 1 B − A	Q − 1 Q	B − 1 B	A − 1 A	A − D − 1 A − D	Q − D − 1 Q − D	− D − 1 − D
2	C_n = L R Minus S C_n = H	A − Q − 1 A − Q	A − B − 1 A − B	− Q − 1 − Q	− B − 1 − B	− A − 1 − A	D − A − 1 D − A	D − Q − 1 D − Q	D − 1 D
3	R OR S	A V Q	A V B	Q	B	A	D V A	D V Q	D
4	R AND S	A Λ Q	A Λ B	0	0	0	D Λ A	D Λ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ Λ Q	$\overline{A}$ Λ B	Q	B	A	$\overline{D}$ Λ A	$\overline{D}$ Λ Q	0
6	R EX-OR S	A ⊻ Q	A ⊻ B	Q	B	A	D ⊻ A	D ⊻ Q	D
7	R EX-NOR S	A ⊻ Q	A ⊻ B	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \veebar A}$	$\overline{D \veebar Q}$	$\overline{D}$

+ = Plus; − = Minus; V = OR, Λ = AND; ⊻ = EX-OR.

Figure 6. ALU Logic Mode Functions (C_n Irrelevant)

Octal $I_{5,4,3}/I_{2,1,0}$	Group	Function
40	AND	A Λ Q
41		A Λ B
45		D Λ A
46		D Λ Q
30	OR	A V Q
31		A V B
35		D V A
36		D V Q
60	EX-OR	A ⊻ Q
61		A ⊻ B
65		D ⊻ A
66		D ⊻ Q
70	EX-NOR	$\overline{A \veebar Q}$
71		$\overline{A \veebar B}$
75		$\overline{D \veebar A}$
76		$\overline{D \veebar Q}$
72	INVERT	$\overline{Q}$
73		$\overline{B}$
74		$\overline{A}$
77		$\overline{D}$
62	PASS	Q
63		B
64		A
67		D
32	PASS	Q
33		B
34		A
37		D
42	"ZERO"	0
43		0
44		0
47		0
50	MASK	$\overline{A}$ Λ Q
51		$\overline{A}$ Λ B
55		$\overline{D}$ Λ A
56		$\overline{D}$ Λ Q

Figure 7. ALU Arithmetic Mode Functions

Octal $I_{5,4,3}/I_{2,1,0}$	C_n = 0 (Low)		C_n = 1 (High)	
	Group	Function	Group	Function
00	ADD	A + Q	ADD plus one	A + Q + 1
01		A + B		A + B + 1
05		D + A		D + A + 1
06		D + Q		D + Q + 1
02	PASS	Q	Increment	Q + 1
03		B		B + 1
04		A		A + 1
07		D		D + 1
12	Decrement	Q − 1	PASS	Q
13		B − 1		B
14		A − 1		A
27		D − 1		D
22	1s Comp	− Q − 1	2s Comp (Negate)	− Q
23		− B − 1		− B
24		− A − 1		− A
17		− D − 1		− D
10	Subtract (1s Comp)	Q − A − 1	Subtract (2s Comp)	Q − A
11		B − A − 1		B − A
15		A − D − 1		A − D
16		Q − D − 1		Q − D
20		A − Q − 1		A − Q
21		A − B − 1		A − B
25		D − A − 1		D − A
26		D − Q − 1		D − Q

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Logic Functions for G, P, Cn+4, and OVR

When the IDM2901A is in the add or the subtract mode, four signals (G, P, C_{n+4}, and OVR) are available to indicate carry and overflow conditions. Based on the eight ALU functions, logic equations for these signals are as follows. (Note: The "R" and "S" inputs are selected according to figure 2.)

Definitions (+ = OR):

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$

$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$

$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$

$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$

$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

Pinout Descriptions of IDM 2901A

Pin functions for the IDM2901A 4-bit slice microprocessor are as follows:

$A_3 - A_0$ 4-bit address field used to select one of the file registers whose contents are displayed through the A port of RAM.

$B_3 - B_0$ 4-bit address field used to select one of the file registers whose contents are displayed through the B port of RAM. When the clock is low, new data can be written into the selected B-port register.

$I_8 - I_0$ Nine instruction-control lines — $I_0/I_1/I_2$ determine data sources of ALU, $I_3/I_4/I_5$ select ALU function, and $I_6/I_7/I_8$ select data inputs for the Q register or the register file.

Q_3/RAM_3 Serves as shift data input/output lines for the most significant bit (MSB) of Q register (Q_3) and the register stack (RAM_3). These lines are TRI-STATE outputs that connect to TTL inputs within the IDM2901A device. When the destination code, as defined by $I_6/I_7/I_8$, indicates an up-shift (octal 6 or 7), the TRI-STATE outputs are enabled; accordingly, the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, these output lines are TRI-STATE or serve as LS-TTL inputs. When a down-shift is indicated by the destination code, the Q_3 and RAM_3 pins are used as data inputs to the MSB of the Q register or RAM.

Q_0/RAM_0 These shift lines are similar to Q_3 and RAM_3, except they operate on the least significant bit (LSB) of the Q register and RAM. To transfer data for up- and down-shifts of the Q register and the ALU, the Q_0 and RAM_0 pins are connected, respectively, to the next less-significant device (Q_n and RAM_n) in the cascaded chain.

$D_3 - D_0$ A 4-bit data field that can be selected as a source of external data for ALU — D_0 is the least significant bit.

$Y_3 - Y_0$ 4-bit output data of IDM2901A. These lines are TRI-STATE; when enabled, they provide either the ALU output or data from the A port of the register file — the selected source is determined by the destination code, as defined by I_6, I_7, and I_8.

$\overline{OE}$ When the Output Enable ($\overline{OE}$) signal is high, the Y outputs are inactive; when the signal is active-low, the active high or low outputs are enabled.

$\overline{P}/\overline{G}$ Carry generate and propagate outputs — see figure 8 for logic equations.

OVR The overflow flag corresponds to the exclusive-OR of the carry-in and carry-out of the MSB of the ALU. When set high, it indicates that the result of an arithmetic twos-complement operation has overflowed into the sign bit — see figure 8 for the logic equation.

F = 0 An open-collector output that goes high if all data lines ($F_3 - F_0$) are low, that is, the result of an ALU operation is zero.

C_n Carry-in to ALU.

C_{n+4} Carry-out of ALU — see figure 8 for logic equations.

CP Clock input. Outputs of Q register and file are clocked on low-to-high transition; the low interval of the clock input corresponds to the "write enable" period of the 16-by-4 RAM, that is, the "master" latches of the register file. When the clock is low, the output latches store the data previously held at the RAM outputs; thus, synchronous master-slave operation of the register file is permitted.

F_3 Most significant (sign) bit output of the ALU.

$I_{5,4,3}$	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S − R	Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions.			
2	R − S	Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions.			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R}$ ∧ S	LOW	Same as R ∧ S equations, but substitute $\overline{R_i}$ for R_i in definitions.		
6	R $\forall$ S		Same as R $\forall$ S equations, but substitute $\overline{R_i}$ for R_i in definitions.		
7	$\overline{R \forall S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$	See Note 1	See Note 2

Note 1: $\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0(G_0 + \overline{C_n})}$ **Note 2:** $[\overline{P}_2 + \overline{G}_2\overline{P}_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \forall [\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$

Figure 8. Logic Equations for Flag Outputs

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Guaranteed Operating Conditions Over Temperature and Voltage

When operated in a system, the timing requirements for the IDM2901A are defined in tables 1, 2, and 3. Table 1 provides clock characteristics of the IDM2901A, table 2 gives the combinational delay times from input to output, and table 3 specifies setup and hold times. If used according to the specified delay and setup times, the device is guaranteed to function properly over the entire operating range. Table 3 defines the time prior to the end of the cycle (low-to-high transition of clock pulse) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Table 1. Cycle Time and Clock Characteristics

Time	IDM2901A	
	DC, PC	DM, FM
Read-Modify-Write Cycle (time from selection of A, B registers to end of cycle)	60 ns	75 ns
Maximum Clock Frequency to Shift Q Register (50% duty cycle)	20 MHz	16 MHz
Minimum Clock Low Time	25 ns	30 ns
Minimum Clock High Time	25 ns	30 ns
Minimum Clock Period	60 ns	75 ns

Table 2. Maximum Combinational Propagation Delays (all in ns; $C_L \leq 50$ pF)

	Commercial IDM2901A DC, PC (0°C to +70°C; 5 V ± 5%)								Military IDM2901A DM, FM (−55°C to +125°C; 5 V ± 10%)							
To Output / From Input	Y	F_3	C_{n+4}	$\overline{G}/\overline{P}$	F = 0 R_L = 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3	Y	F_3	C_{n+4}	$\overline{G}/\overline{P}$	F = 0 R_L = 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3
A, B	70	65	65	60	70	65	70	–	85	80	80	75	85	80	85	–
D (arithmetic mode)	45	45	45	45	55	45	50	–	55	55	55	55	70	55	60	–
D (I = X37)	45	45	–	–	55	–	50	–	55	55	–	–	70	–	60	–
C_n	32	32	20	–	40	30	35	–	40	40	25	–	50	35	45	–
$I_{2,1,0}$	55	50	50	45	60	50	60	–	70	60	60	55	75	60	75	–
$I_{5,4,3}$	50	50	50	45	55	50	50	–	60	60	60	55	70	60	60	–
$I_{8,7,6}$	25	–	–	–	–	–	30	30	30	–	–	–	–	–	40	40
$\overline{OE}$ Enable/Disable	30/25	–	–	–	–	–	–	–	40/25	–	–	–	–	–	–	–
A Bypassing ALU (I = 2xx)	40	–	–	–	–	–	–	–	50	–	–	–	–	–	–	–
Clock ↓ (Note 6)	60	60	60	50	60	55	60	35	75	75	75	65	75	70	75	45

Table 3. Setup and Hold Times (all in ns) — Note 1

		Commercial IDM2901A DC, PC (0°C to +70°C, 5 V ± 5%)		Military IDM2901A DM, FM (−55°C to +125°C, 5 V ± 10%)	
From Input	Notes	Setup Time	Hold Time	Setup Time	Hold Time
A, B Source	2, 3, 4, 5	60, $t_{pw}L$ + 20	0	75, $t_{pw}L$ + 25	0
B Destination	2, 4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
D (arithmetic mode)		40	0	50	0
D (I = X37)	5	40	0	50	0
C_n		25	0	30	0
$I_{2,1,0}$		45	0	55	0
$I_{5,4,3}$		45	0	55	0
$I_{8,7,6}$	4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
$RAM_{0,3}/Q_{0,3}$		20	0	25	0

Note 1: See figures 9 and 10.

Note 2: If the B address is used as a source operand, allow for the "A, B Source" setup time; if it is used only for the destination address, use the "B Destination" setup time.

Note 3: Where two numbers are shown, both must be met.

Note 4: "$t_{pw}L$" is the clock low time.

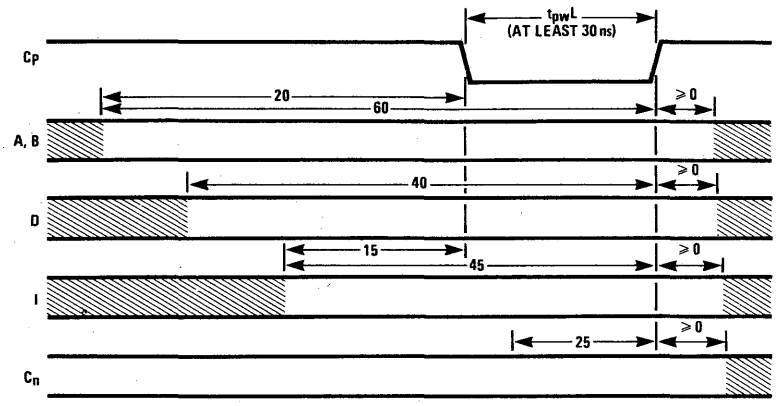
Note 5: DVO is the fastest way to load the RAM from the D inputs. This function is obtained with I = 337.

Note 6: Using Q register as source operand in arithmetic mode. Clock is not normally in critical speed path when Q is not a source.

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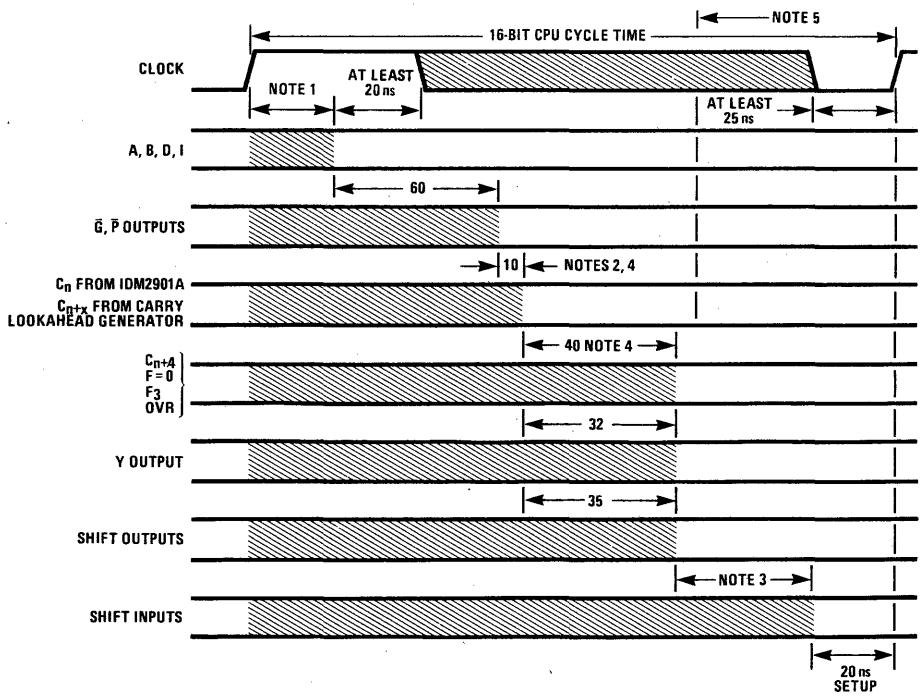
Set-Up and Hold Times (mimimum cycles from each input)

Setup and hold times are defined relative to the low-to-high transition of the clock pulse. At all times, inputs must be stable from the setup time prior to the clock until the hold time after the clock – observe that all hold times are "zero." The set-up times allow sufficient time to perform the correct operation on the correct data so that the correct ALU data can be written into the correct register.



Note: Numbers shown are minimum data-stable times in nanoseconds for commercial product – see table 3 for detailed information.

Figure 9. Setup Times for Input Parameters of IDM2901A



Notes:

1. This delay is the max t_{pd} of the register containing A, B, D, and I.
2. 10 ns for look-ahead carry. For ripple carry over 16 bits use 2 x ($C_n \rightarrow C_{n+4}$), or 60 ns.
3. This is the delay associated with the multiplexer between the shift outputs and the shift inputs on the IDM2901A.
4. Not applicable for logic operations.
5. Clock rising edge may occur here if add and shift do not occur on same cycle.

Figure 10. Switching Waveforms for 16-Bit System Assuming A, B, D, and I are Driven from Registers with the Same Propagation Delay and Clocked by the IDM2901A. (These are maximum times in nanoseconds using commercial-product specifications.)

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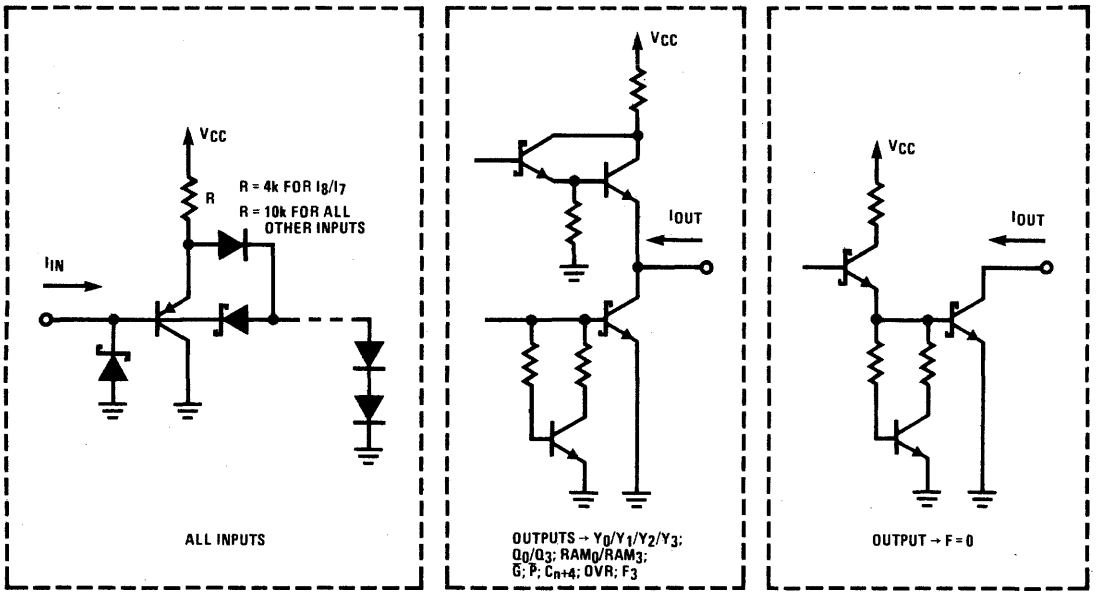


Figure 11. Input/Output Current Interface Conditions for IDM2901A

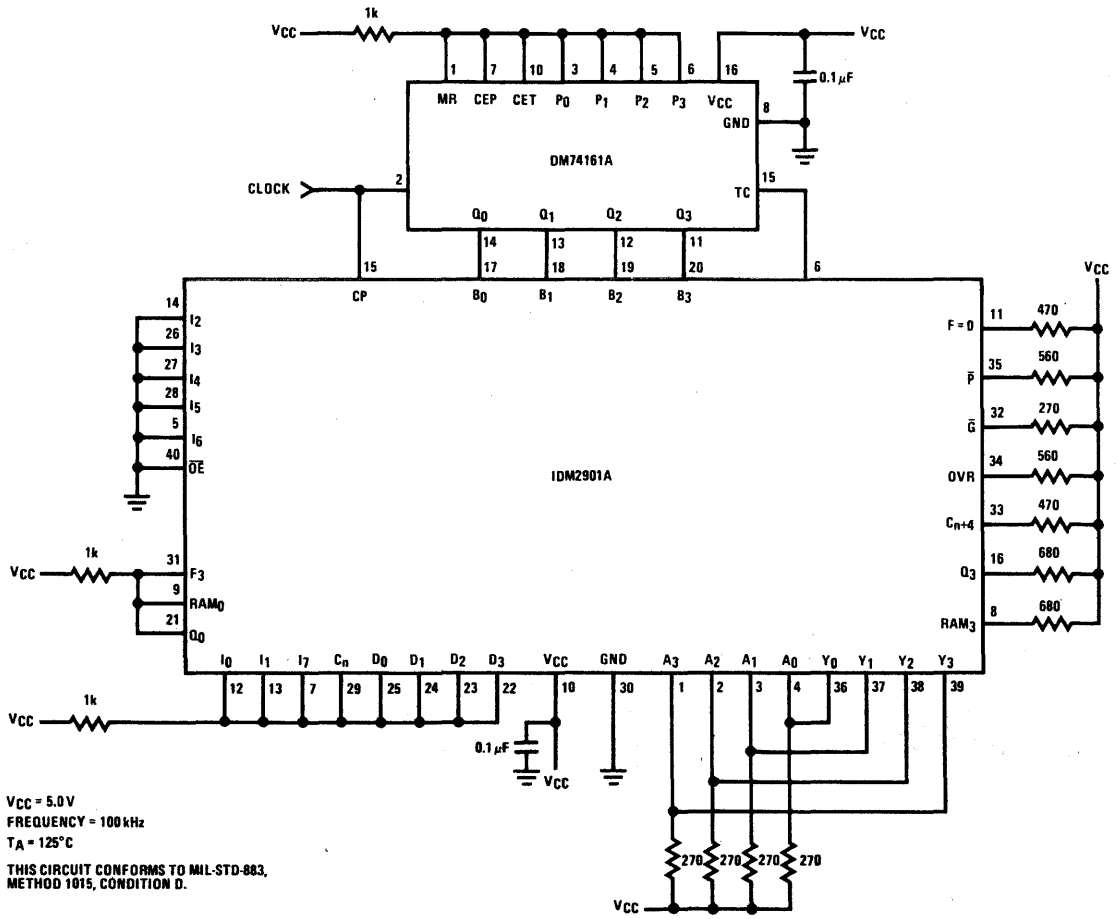
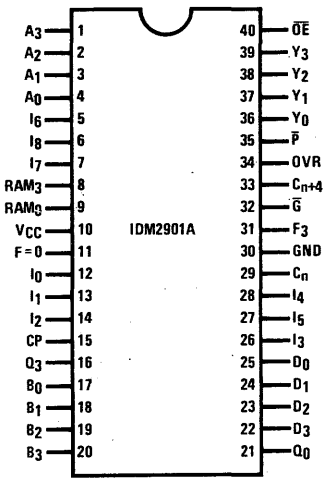


Figure 12. Burn-In Circuit for IDM2901A

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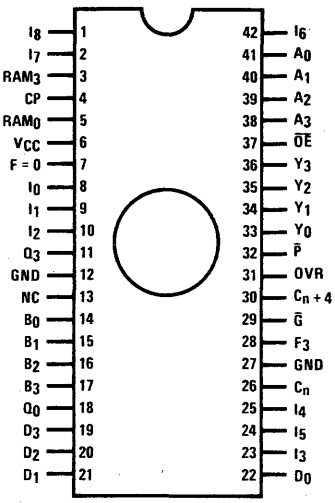
Connection Diagrams

DIP (Top View)



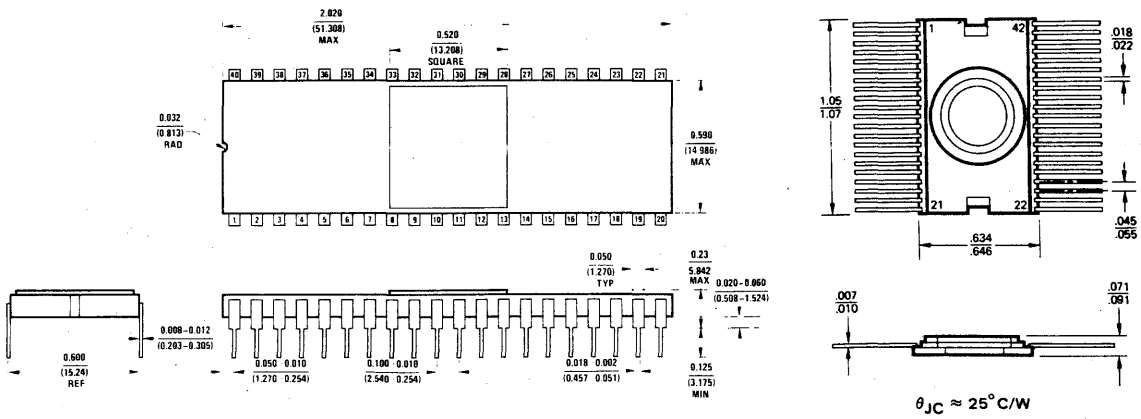
NOTE: PIN 1 IS MARKED FOR ORIENTATION.

Flat Pack (Top View)



NOTE: BOTH GROUNDS (PINS 12 and 27) MUST BE CONNECTED.

Physical Dimensions



Ordering Information

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	IDM2901APC
Hermetic DIP	0°C to +70°C	IDM2901ADC
Hermetic DIP	−55°C to +125°C	IDM2901ADM
Hermetic Flat Pack	−55°C to +125°C	IDM2901AFM
Dice	0°C to +70°C	IDM2901AXC

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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Pub. No. 426305290-001B

ISP-8A/600 single-chip 8-bit n-channel microprocessor (SC/MP-II)

general description

SC/MP (Simple Cost-effective MicroProcessor) is a single-chip 8-bit microprocessor packaged in a standard, 40-pin, dual-in-line package.

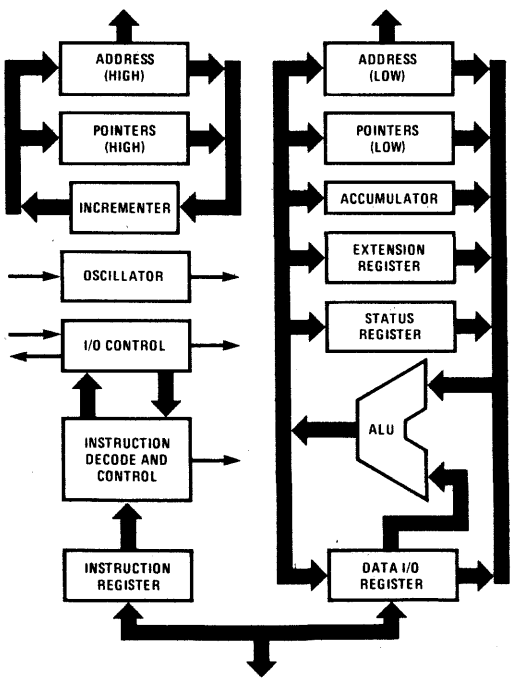
N-channel, silicon gate, depletion mode standard-process technology ensures high performance, high reliability, and high producibility.

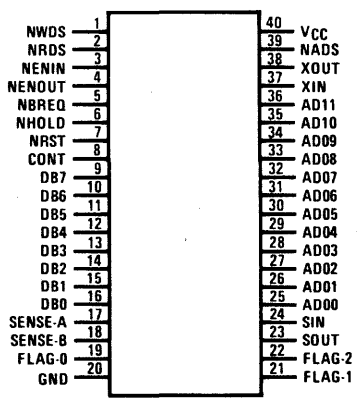
SC/MP is intended for use in general-purpose applications where cost per function is a most significant criterion. But cost efficiency is only a part of SC/MP's story. It goes on to include a variety of useful functions that are not even provided by some of the expensive microprocessors, like self-contained timing circuitry, 16-bit (65k) addressing capability, serial or parallel data-transfer capability and common memory/peripheral instructions. The built-in features in conjunction with the low initial cost describe what SC/MP really is — a microprocessor specifically designed to provide the simplest and most efficient solution to many application requirements.

customer benefits

- Simpler interfacing
  - Bidirectional TRI-STATE® 8-bit data bus
  - TTL-compatible input/output interface
- Si-gate N-channel ion-implant process
- Direct Memory Access (DMA) and multiprocessor capabilities
  - Handshake bus-access control on chip
- Simplified programming
  - Multiple addressing modes — program-counter-relative, immediate data, indexed, auto-indexed, and implied
- Direct control output
  - Three user-accessible control-flag outputs
- Simpler I/O hardware
  - Separate serial-data input and output ports
  - Two sense inputs
  - Direct interfacing to standard memory parts
- Simplified timing hardware
  - On-chip clock generator
- Interface flexibility
  - Capability to interface with memories or peripherals of any speed
- Large system capability
  - Address capability to 65k bytes of memory
- Simplified power requirements
  - Single 5-volt supply
  - Low power
- Lower cost
  - Plastic package

block and connection diagrams





SC/MP-II Pin Configuration

ISP-8A/600 single-chip 8-bit n-channel microprocessor (SC/MP-II)

MICROPROCESSOR National Semiconductor

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applications

- Test Systems and Instrumentation
- Machine Tool Control
- Small Business Machines
- Word Processing Systems
- Educational Systems
- Multiprocessor Systems
- Process Controllers
- Terminals
- Traffic Controls
- Laboratory Controllers
- Sophisticated Games
- Automotive

absolute maximum ratings (Note 1)

Voltage at Any Pin . . . . . −0.5V to +7.0V

Operating Temperature Range . . . . . 0°C to +70°C

Storage Temperature Range. . . . . −65°C to +150°C

Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

dc electrical characteristics (T_A = 0°C to +70°C, V_{CC} = +5V ± 5%)

Parameter	Conditions	Min.	Max.	Units
INPUT SPECIFICATIONS				
All Input Pins Except V_{CC} and GND Logic "1" Input Voltage		2.0	V_{CC}	V
Logic "0" Input Voltage		−0.5	0.8	V
Input Capacitance (All pins except V_{CC} and GND)			10	pF
Supply Current I_{CC}	T_A = 25°C outputs unloaded		45	mA
	T_A = 0°C outputs unloaded		50	mA
OUTPUT SPECIFICATIONS				
"TRI-STATE®" Pins (NWDS, NRDS, DB0 - DB7, AD00 - AD11) Logic "1" Output Voltage	I_{OUT} = −100μA	2.4		V
Logic "0" Output Voltage	I_{OUT} = 2.0mA		0.4	V
NADS, FLAG 0 - 2, SOUT, NENOUT Logic "1" Output Voltage	I_{OUT} = −100μA	V_{CC} − 1		V
Logic "1" Output Voltage	I_{OUT} = −1mA	1.5		V
Logic "0" Output Voltage	I_{OUT} = 2.0mA		0.4	V
NBREQ (Note 2) Logic "0" Output Voltage	I_{OUT} = 2.0mA		0.4	V
Logic "1" Output Current	$0 \leqslant V_{OUT} \leqslant V_{CC}$		±10	μA
XOUT Logic "1" Output Voltage	I_{OUT} = −100μA	2.4		V
Logic "0" Output Voltage	I_{OUT} = 1.6mA		0.4	V

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ac electrical characteristics [T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, 1 TTL Load (Note 3)]

Parameter	Conditions	Min.	Max.	Units
f_X		0.1	4.0	MHz
	R = 240Ω ± 5% (figure 2B) C = 300pF ± 10%	2.0	4.0	MHz
T_C (Note 4)		500		ns
Microcycle		1		μs
External Clock Input (see figure 2A)				
T_{W0}		120		ns
T_{W1}		120		ns
XOUT/ADS Timing Relationship (see figure 3)				
T_H (ADS)		100	225	ns
Address and Input/Output Status (see figures 5 and 6)				
T_{D1} (ADS)			$3T_C/2$	ns
T_W (ADS)		$(T_C/2) - 50$		ns
T_S (ADDR)		$(T_C/2) - 165$		ns
T_H (ADDR)		50		ns
T_S (STAT)		$(T_C/2) - 150$		ns
T_H (STAT)		50		ns
T_H (NBREQ)		0		ns
Data Input Cycle (see figure 5)				
T_D (RDS)		0		ns
T_W (RDS)		$T_C + 50$		ns
T_S (RD)		175		ns
T_H (RD)		0		ns
T_{ACC} (RD)		$2T_C - 200$		ns
Data Output Cycle (see figure 6)				
T_D (WDS)		$T_C - 50$		ns
T_W (WDS)		T_C		ns
T_S (WD)		$(T_C/2) - 200$		ns
T_H (WD)		100		ns
Input/Output Cycle Extend (see figure 7)				
T_S (HOLD)		200		ns
T_{D1} (HOLD)		130	275	ns
T_{D2} (HOLD)			350	ns
T_W (HOLD)			∞	ns
T_H (HOLD)		0		ns
Bus Access (see figure 4)				
T_D (NENOUT)			150	ns
T_{D2} (ADS)		$T_C/2$	$3T_C/2$	ns
T_H (NENIN)		0		ns
Output Load Capacitance				
XOUT			30	pF
All Other Output Pins			75	pF

Note 1: Maximum ratings indicate limits beyond which damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under electrical characteristics.

Note 2: NBREQ is an input/output signal that requires an external resistor to V_{CC}.

Note 3: All times measured from valid Logic "0" level = 0.8 V or valid Logic "1" level = 2.0 V.

Note 4: T_C is the time period for two clock cycles of the on-chip or external oscillator ($T_C = 2/f_X$). Refer to paragraph titled Timing Control for detailed definition.

Note 5: All times measured with a 50% duty cycle on the external clock.

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functional description

SC/MP is a self-contained general-purpose microprocessor designed for ease of implementation in stand-alone, DMA (Direct Memory Access), and multiprocessor applications. Communications between SC/MP and external memory/peripheral devices are effected via a 12-bit dedicated address bus and an 8-bit bidirectional data bus. During the address interval of each input/output cycle, SC/MP employs both busses to provide a 16-bit address output: the 12 least significant address bits are sent out over the 12-bit address bus and the 4 most significant address bits are sent out over the 8-bit data bus along with 4 status bits. Separate strobe outputs from SC/MP (NADS, NWDS, NRDS) indicate when valid address information is present on the two busses, and when valid input/output memory or peripheral data are present on the 8-bit bus. To further extend flexibility of application, serial data input/output ports are also provided so that serial data transfers can be effected under program control. The remaining input/output signals shown in figure 1 are dedicated to general-purpose control and status functions, including initialization, bus management, microprocessor halt, interrupt request, input/output cycle extension, and user-specified hardware/software interface functions. A detailed description of each input/output signal is provided in table 1.

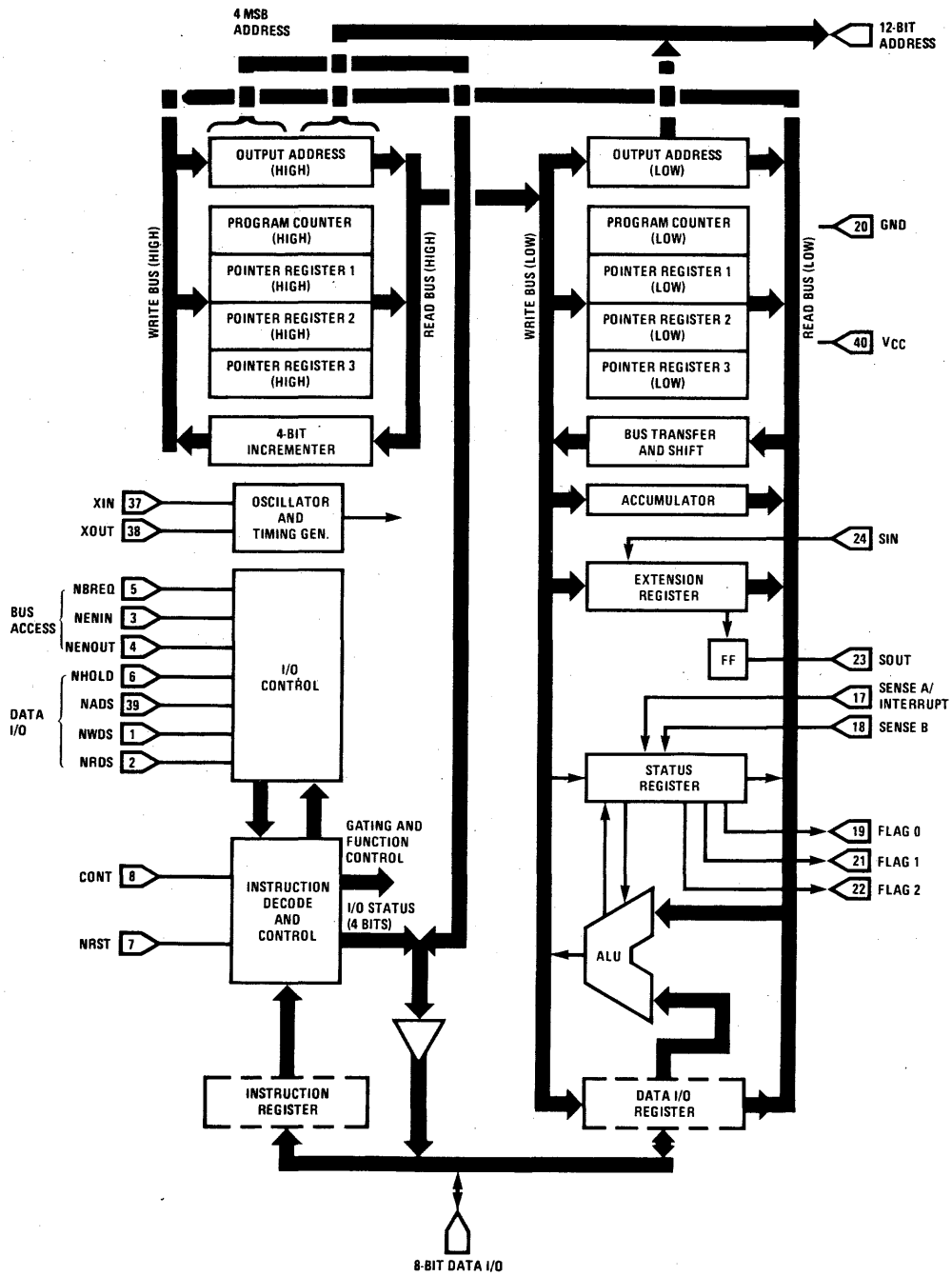


FIGURE 1. SC/MP-II Detailed Block Diagram

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TABLE 1. Input/Output Signal Description

Signal Mnemonic	Functional Name	Description
NRST	Reset Input	Set high for normal operation. When set low, aborts in-process operations. When returned high, internal control circuit zeroes all programmer-accessible registers; then, first instruction is fetched from memory location 0001_{16}.
CONT	Continue Input	When set high, enables normal execution of program stored in external memory. When set low, SC/MP operation is suspended (after completion of current instruction) without loss of internal status.
NBREQ	Bus Request Input/Output	Associated with SC/MP internal allocation logic for system bus. Can be used as bus request output or bus busy input. Requires external load resistor to V_{CC}.
NENIN	Enable Input	Associated with SC/MP internal allocation logic for system bus. When set low, SC/MP is granted access to system busses. When set high, places system busses in high-impedance (TRI-STATE®) mode.
NENOUT	Enable Output	Associated with SC/MP internal allocation logic for system bus. Set low when NENIN is low and SC/MP is not using system busses (NBREQ-high). Set high at all other times.
NADS	Address Strobe Output	Active-low strobe. While low, indicates that valid address and status output are present on system busses.
NRDS	Read Strobe Output	Active-low strobe. On trailing edge, data are input to SC/MP from 8-bit bidirectional data bus. High-impedance (TRI-STATE®) output when input/output cycle is not in progress.
NWDS	Write Strobe Output	Active-low strobe. While low, indicates that valid output data are present on 8-bit bidirectional data bus. High-impedance (TRI-STATE®) output when input/output cycle not in progress.
NHOLD	Input/Output Cycle Extend Input	When set low prior to trailing edge of NRDS or NWDS strobe, stretches strobe to extend input/output cycle; that is, strobe is held low until NHOLD signal is returned high.
SENSE A	Sense/Interrupt Request Input	Serves as interrupt request input when SC/MP internal IE (Interrupt Enable) flag is set. When IE flag is reset, serves as user-designated sense condition input. Sense condition testing is effected by copying status register to accumulator.
SENSE B	Sense Input	User-designated sense-condition input. Sense-condition testing is effected by copying status register to accumulator.
SIN	Serial Input to E Register	Under software control, data on this line are right-shifted into E register by execution of SIO instruction.
SOUT	Serial Output from E Register	Under software control, data are right-shifted onto this line from E register by execution of SIO instruction. Each data bit remains latched until execution of next SIO instruction.
FLAGS 0, 1, 2	Flag Outputs	User-designated general-purpose flag outputs of status register. Under program control, flags can be set and reset by copying accumulator to status register.
AD00-AD11	Address Bit 00 through Address Bit 11	Twelve TRI-STATE® address output lines. SC/MP outputs 12 least significant address bits on this bus when NADS strobe is low. Address bits are then held valid until trailing edge of read (NRDS) or write (NWDS) strobes. After trailing edge of NRDS or NWDS strobe, bus is set to high-impedance (TRI-STATE®) mode until next NADS strobe.

NOTE:

The 8-bit bidirectional data bus is set to the high-impedance (TRI-STATE®) mode except when it is actually in use by SC/MP (NADS, NRDS, or NWDS low). During the addressing interval of each input/output cycle (NADS low), SC/MP provides address and status outputs over the bus; during the ensuing data-transfer interval (NRDS or NWDS low), 8-bit input or output data bytes are routed over the bus.

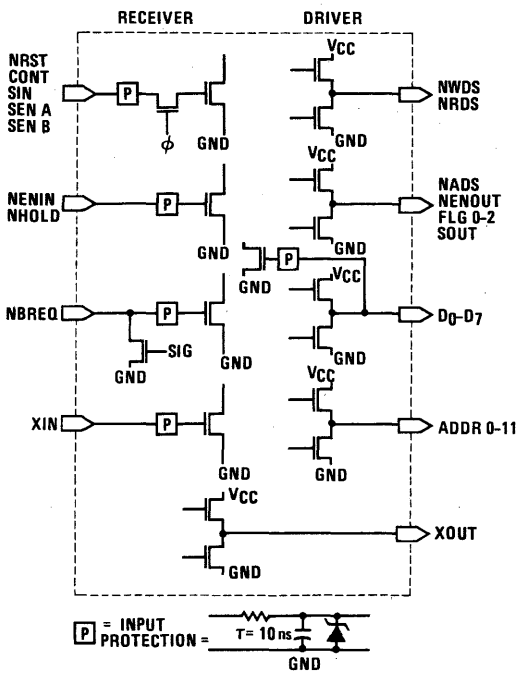
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TABLE 1. Input/Output Signal Description (Continued)

Signal Mnemonic/ Pin Designation	Output at NADS Time		Input at NRDS Time	Output at NWDS Time
	Functional Name	Description		
DB0	Address Bit 12	Fourth most significant bit of 16-bit address.	Input data are expected on the eight (DB0-DB7) lines.	Output data are valid on the eight (DB0-DB7) lines.
DB1	Address Bit 13	Third most significant bit of 16-bit address.		
DB2	Address Bit 14	Second most significant bit of 16-bit address.		
DB3	Address Bit 15	Most significant bit of 16-bit address.		
DB4	R-Flag	When high, data input cycle is starting; when low, data output cycle is starting.		
DB5	I-Flag	When high, first byte of instruction is being fetched.		
DB6	D-Flag	When high, indicates delay cycle is starting; that is, second byte of DLY instruction is being fetched.		
DB7	H-Flag	When high, indicates that Halt Instruction has been executed. (In some system configurations, the H-Flag output is latched and, in conjunction with the CONTinue input, provides a programmed halt.)	**Note:** The DB0 through DB7 (AD12-HFLG) lines are a high-impedance (open circuit) load when SC/MP does not have access to the input/output bus.	

DRIVERS AND RECEIVERS

Equivalent circuits for SC/MP drivers and receivers are shown below. All inputs have static charge protection circuits consisting of an RC filter and voltage clamp. These devices still should be handled with care, as the protection circuits can be destroyed by excessive static charge.



SC/MP-II Driver and Receiver Equivalent Circuits

TIMING CONTROL

All necessary timing signals are provided by a three-stage inverter ring oscillator contained on the SC/MP chip. Two control pins, XIN and XOUT, permit the frequency of the oscillator to be controlled by any of the following methods:

1. By leaving the XOUT pin unterminated and driving the XIN pin with an externally generated TTL clock that conforms to the parameters shown in figure 2A. For this method, the frequency of the oscillator is equal to the frequency of the external clock input.

2. By connecting a resistor-capacitor feedback network between the XIN and XOUT pins and GND as shown in figure 2B.

3. By connecting a crystal with low-pass filter network between the XIN and XOUT pins and GND as shown in figure 2C (for above 1 megahertz) or figure 2D (for 1 megahertz or below). For this method, the frequency of the oscillator is equal to the resonant frequency of the crystal and the low-pass filter prevents unwanted harmonic oscillations.

In addition to illustrating appropriate frequency-control networks for the on-chip oscillator, figures 2A through 2D also show how an optional driver may be used to derive a system clock from the oscillator signal present at the XOUT pin. For reference purposes, the timing relationship between the XOUT signal and the NADS strobe is shown in figure 3.

In the discussions that follow, instruction execution and input/output timing are described in terms of microcycles.

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The time interval of a microcycle is four times the period of the oscillator; that is:

period of one microcycle = $2T_C$

$$T_C = 2(\frac{1}{f_{osc}}) = 2(\frac{1}{f_{res}}) = 2(\frac{1}{f_{XIN}})$$

where:

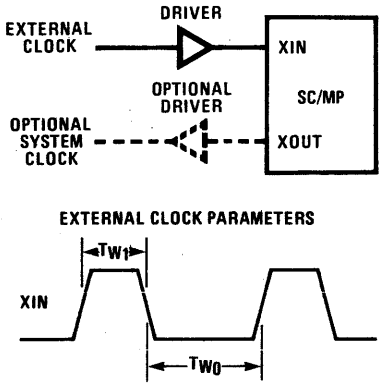
T_C = time period for two cycles of on-chip or external oscillator

f_{osc} = frequency of on-chip oscillator

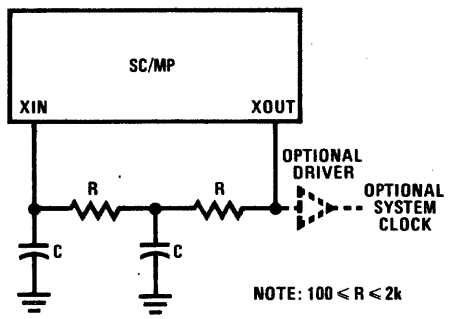
f_{res} = resonant frequency of crystal connected between XIN and XOUT pins

f_{XIN} = frequency of external clock applied to XIN pin

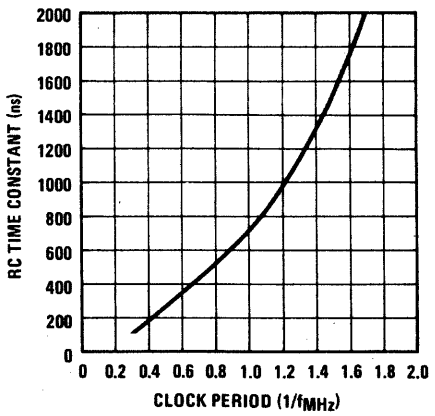
A. External Clock Input



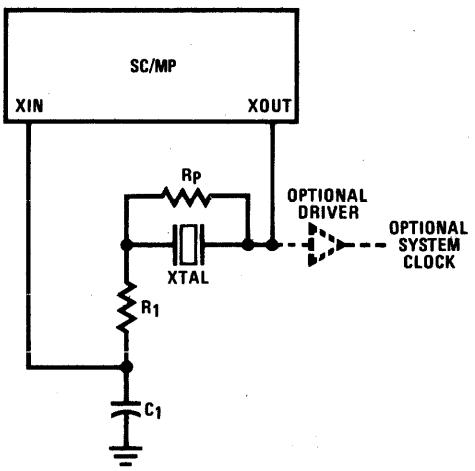
B. Resistor-Capacitor Feedback Network



Typical Oscillator Frequency vs RC Time Constant



C. Crystal with Low-Pass Filter (Above 1MHz)

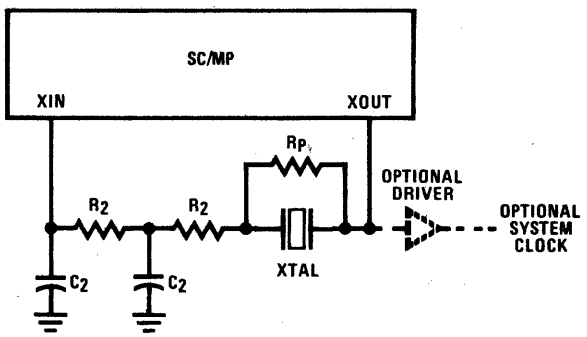


Suggested values for Crystal with Low-Pass Filter Network.

Crystal	R_P	C_1	R_1
2MHz	100kΩ	56pF	1kΩ
3.58MHz	100kΩ	27pF	1kΩ
4MHz	100kΩ	27pF	1kΩ

XTAL is parallel resonant with maximum series resonance equal to 1kΩ.

D. Crystal with Low-Pass Filter (1MHz or Below)



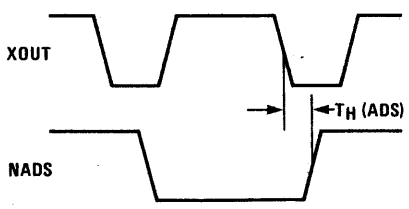


FIGURE 2. Frequency Control Networks for On-Chip Oscillator

FIGURE 3. XOUT/NADS Timing Relationship

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INSTRUCTION FORMAT

The SC/MP instruction repertoire includes both single-byte and double-byte instructions. A single-byte instruction consists of an 8-bit operation code that specifies an operation that SC/MP can execute without further reference to memory. A double-byte instruction consists of an 8-bit operation code and an 8-bit data or displacement field. When the second byte represents a data field, the data are processed by SC/MP during execution of the instruction, thereby eliminating the need for further memory references. When the second byte represents a displacement value, it is used to calculate a memory address that will be accessed (written into or read from) during execution of the instruction (refer to Addressing).

DATA STORAGE

As shown in figure 1, SC/MP provides ten internal registers, seven of which are accessible to the programmer. The purpose and function of these registers are described below.

Program Counter – The program counter is a 16-bit register that contains the address of the instruction being executed. The contents of this register are automatically incremented by one just before each instruction is fetched from memory to enable sequential execution of the stored instructions. Under program control, the contents of this register also may be modified or exchanged with the contents of a pointer register to effect subroutine calls and program branches.

NOTE:

The 16-bit address output of the program counter consists of a 4-bit high-order address and a 12-bit low-order address. When the program counter is incremented at the start of each instruction fetch input/output cycle, only the 12 low-order bits are affected; no carry is provided to the 4 high-order bits. For systems employing memories of 4k or less, the high-order bits can be ignored as they are set to 0000_{16} following initialization. For systems employing larger memories, the contents of a pointer register can be modified to select the desired 4k block of memory.

Pointer Registers – The pointer registers are 16-bit general-purpose registers that normally are loaded under program control with reference addresses that serve as page pointers, stack pointers, and subroutine pointers. In applications having minimal memory addressing requirements, these registers may be used alternately as data storage registers.

NOTE:

When interrupt requests are enabled, pointer register 3 is automatically referenced by the internal microprogram for formation of the starting address of the user-generated interrupt service routine. (See figure 9.) In this case, the contents of pointer register 3 must be set to one less than the memory location of the first instruction in the interrupt service routine.

Accumulator – The 8-bit accumulator (AC) is the primary working register of SC/MP. It is used for performing and storing the results of arithmetic and logic operations as well as for data transfers, shifts, rotates, and data exchanges with the program counter, the pointer registers, and the status register.

Extension Register – The extension register is used both for serial input/output data transfers and with the accumulator to effect arithmetic, logic, and data-transfer operations. If the second byte of an indexed or auto-indexed memory-reference instruction (refer to Addressing) equals -128_{10}, the contents of the extension register are used as the displacement value for address formation.

Status Register – The status register provides storage for arithmetic, control, and software status flags. For more-detailed information on the function of this register, refer to Status Register under the description of the Arithmetic and Logic Unit.

Instruction Register – The 8-bit instruction register is not accessible to the programmer. During the fetch phase of each instruction cycle, this register is loaded with the 8-bit instruction operation code retrieved from memory (for a single-byte instruction or the first byte of a double-byte instruction).

Data Input/Output Register – The data input/output register is not accessible to the programmer. It is used for temporary storage of all input/output data received via or transmitted over the 8-bit bidirectional data bus during the data-transfer interval of each input/output cycle (NRDS or NWDS low).

Address Register – The 16-bit address register is not accessible to the programmer. It is used for temporary storage of the 16-bit address transmitted during an input/output cycle.

ARITHMETIC AND LOGIC UNIT

The Arithmetic and Logic Unit (ALU) provides the data-manipulation capability that is an essential feature of any microprocessor. The operations provided by the ALU include OR, XOR, increment, decrement, binary addition, and decimal addition. For decimal addition, the data inputs to the ALU are treated as two 4-bit BCD digits, thereby eliminating the program-storage and execution time required to perform BCD to binary conversion.

BUS TRANSFER LOGIC

The bus transfer logic processes the gating and function control outputs of the instruction-decode logic to provide the shift-right (with link, without link, or with serial input data), rotate (with or without link), and bus-exchange functions necessary for data movement between the SC/MP internal read and write busses. A general summary of the data-manipulation capabilities available to the programmer follows.

1. Either the low-order or the high-order byte of any pointer register can be exchanged with the contents of the 8-bit accumulator. Thus, data exchanges between the pointer registers can be effected one byte at a time via the accumulator.

2. The contents of the program counter can be directly exchanged with the contents of any pointer register.

3. The contents of the extension register can be loaded into the accumulator or can be exchanged with the contents of the accumulator. When the accumulator is loaded from the extension register, the original contents of the accumulator are lost.

4. The contents of the status register can be copied into the accumulator to enable status modification or conditional-branch testing. When the status register is copied into the accumulator, the contents of the status register are not altered but the original contents of the accumulator are lost.

5. The contents of the accumulator can be copied into the status register to change the outputs of the status register, except for status bits 4 and 5 (Sense A and B inputs to SC/MP). Since these are read-only bits, they are not affected by data movements internal to SC/MP. Copying the accumulator into the status register does not alter the contents of the accumulator.

NOTE:

The flag 0, 1, and 2 outputs of the status register serve as latched flags; in other words, they are set to the specified state when the contents of the accumulator are copied into the status register, and they remain in the specified state until the contents of the status register are modified again under program control.

STATUS REGISTER

The function of each bit in the status register is described briefly below.

7	6	5	4	3	2	1	0
CY/L	OV	S_B	S_A	IE	F_2	F_1	F_0

User Flag 0 — User-assigned general-purpose status bit for implementation as software status bit or in system control applications. This status bit is available as an external output from SC/MP.

User Flag 1 — Same as User Flag 0.

User Flag 2 — Same as User Flag 0.

Interrupt Enable Flag — Internal status bit that is set and reset under program control. When set, SC/MP recognizes external interrupt requests received via Sense A input. When reset, inhibits SC/MP from recognizing interrupt requests.

Sense A — General-purpose status input for sensing external conditions. When IE flag is reset, this bit can be tested by copying status register to accumulator. When IE flag is set, this bit serves as interrupt request input causing SC/MP to automatically branch to user-generated interrupt-service routine in response to high input.

Sense B — Same as Sense A except that it is not tested for interrupt status.

NOTE:

Sense A and B inputs are read-only bits. Thus, they are not affected when the contents of the accumulator are copied into the status register.

Overflow (OV) — This bit is set if an arithmetic overflow occurs during an add (ADD, ADI, or ADE) or a complement-and-add instruction (CAD, CAI, or CAE). It is not affected by the decimal-add instructions (DAD, DAI, or DAE).

Carry/Link (CY/L) — This bit is set if a carry from the most significant bit occurs during an add, complement-and-add, or decimal-add instruction. Thus, it serves as a carry input to the next add instruction. In addition, it is included in the Shift Right with Link (SRL) and Rotate Right with Link (RRL) instructions.

CONTROL

The operation of the SC/MP microprocessor consists of repeatedly accessing or fetching instructions from the program stored in external memory and executing the operations specified by the instructions. These two steps are carried out under the control of an internal microprogram. (SC/MP is not user-microprogrammable.) The microprogram is similar to a state table specifying the series of states of system control signals necessary to carry out each instruction. Microprogram storage is provided in the instruction decode and control logic, and microprogram routines are implemented to fetch and execute instructions. The fetch routine first increments the program counter, and then causes the instruction address to be transferred from the program counter to the system busses via the output address register. The microprogram next initiates an input data transfer. When the instruction operation code is subsequently placed on the 8-bit data bus (single-byte instruction or first byte of double-byte instruction), the operation code is loaded into the instruction register. The operation code is then partially decoded to determine whether the instruction contains a second byte. If it does, a second input data transfer is effected to load the next byte in the data input/output register.

After the complete instruction is stored in the instruction and/or data input/output register(s), the instruction decoder transforms the instruction operation code into the address of the appropriate instruction-execution routine contained in the internal microprogram. The microprogram then branches to the specified internal address to initiate execution of the instruction. The resulting execution routine comprises one or more microinstructions that implement the required functions. For example, the first microcycle of an Extension Register Add Instruction (ADE) causes the contents of the extension register to be gated onto the read bus, transferred to the write bus via the bus control logic, and then written into the data input/output register. The next microcycle causes the contents of the accumulator to be gated onto the read bus, the contents of the read bus to be added to the contents of the data input/output register via the ALU, and the resultant output of the ALU to be written into the accumulator via the write bus. The final step of the execution routine is a jump back to the fetch routine to access the next instruction.

INITIALIZATION

Since SC/MP may power up in a random condition, the following power-up and initialization procedure is recommended.

1. Apply power (GND and V_{CC}) and set NRST low.

NOTE:

Allow ample time (typically, 250 ms) for the oscillator and the internal clocks to stabilize. In systems where NRST is set low after turning on power, NRST must remain low for a minimum of $4T_C$. While NRST is low, any in-process operations are aborted automatically. When NRST is low, strobes and address and data busses are in the Non-I/O state (high-Z state).

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2. Set NRST high. If the rise time of this input is too slow, the processor, first, will initialize and execute a few instructions and, then, will reinitialize. If the application is such that multiple initialization is undesireable, NRST should be brought high at a minimum rate of 2 volts per microcycle.

NOTE:

This causes the SC/MP internal control circuit to set the contents of all programmer-accessible registers to zero. Thus, when SC/MP is granted access to the system busses following initialization, the first instruction is fetched *always* from memory location 0001_{16}. The NBREQ output goes low, indicating the start of this input/output cycle; this occurs at a time within $13T_C$ after NRST is set high. Normal execution of the program continues as long as NRST remains high.

parallel data transfers

Parallel data transfers occur during each instruction fetch and during the ensuing read/write cycle associated with execution of the memory-reference instructions. This class of instruction could perhaps more properly be called the "Input/Output Reference Class" in the case of the SC/MP microprocessor, since all data transfers, whether with memory, peripheral devices, or a central processor data bus, occur through the execution of these instructions. This unified bus structure is in contrast with many other microprocessors and minicomputers that have one instruction type (input/output class) for communication with peripheral devices and another instruction type (memory reference class) for communication with memories. The advantage of the approach taken by SC/MP is that a wider variety of instructions (the entire memory-reference class) is available for communications with peripherals. Thus, the LD and ST (Load and Store) instructions can be used for basic transfers, the ILD and DLD (increment/decrement and load) instructions can be used for indexing peripheral registers, and the remaining memory reference instructions can be used, as required, for "one-step" retrieval and processing of peripheral input data.

BUS UTILIZATION

The bus utilization of SC/MP is shown in table 2.

NBREQ, NENIN, and NENOUT are active and bus access is controlled as shown in figure 4. If NENIN is returned high during an input/output cycle, the input/output cycle is repeated when NENIN is again returned low.

During an ILD or DLD instruction, SC/MP does not relinquish the bus between the loading of the data and the storing of the modified data. If NENIN is brought high after the data have been loaded, the load portion of the cycle is not repeated when NENIN is returned low.

BUS ACCESS

Before SC/MP can initiate parallel data transfers with memory or peripheral devices, it must have access to the system address and data busses. Three of the SC/MP input/output signals are associated with bus control: NBREQ, NENIN, and NENOUT. For simple stand-alone applications, the NENOUT signal can be ignored and the NENIN signal can be tied to GND to allow the SC/MP microprocessor to have continual access to the system busses. The NBREQ input/output line then goes low during each input/output cycle as shown in figures 5 and 6 to indicate when SC/MP is actually using the system busses.

NOTE:

The NBREQ input/output line must be tied to V_{CC} via an external load resistor to allow normal operation of the SC/MP microprocessor.

For DMA and multiprocessor applications, the NBREQ, NENIN, and NENOUT signals can be interconnected in various configurations to allow bus access to be granted to requesting devices according to user-specified priorities. Figure 4 illustrates the general sequence in which these signals are processed by SC/MP to gain access to the system busses and to indicate when the busses are actually being used.

INPUT/OUTPUT CYCLE

Once SC/MP has control of the system busses, the actual input/output cycle begins. As shown in figures 5 and 6, the functions of memory addressing, data reading, and data writing are implemented, respectively, by the address strobe (NADS), the read strobe (NRDS), and the write strobe (NWDS). Note that the NBREQ signal is reset high at the end of the input/output cycle to indicate that the system busses are now free for use by the highest-priority requesting device.

The first operation that SC/MP performs for each input/output cycle is to load the 12 least significant address bits onto the 12-bit address bus, and the 4 most significant address bits along with 4 status bits onto the 8-bit data bus. At the same time, SC/MP sets the NADS output low to indicate that the address and the status information are valid. The low-order address on the 12-bit bus is then held valid for the duration of the input/output cycle; the high-order address and the status information on the 8-bit bus remain valid only while NADS is low. While valid, the status bits have the following significance:

RFLG – When high, indicates that input/output cycle is read cycle; when low, indicates that input/output cycle is write cycle.

IFLG – Set high to indicate that instruction operation code (single-byte instruction or first byte of double-byte instruction) will be output from memory following NADS.

DFLG – Set high only when second byte of Delay Instruction is to be read from memory following NADS. Execution of the Delay Instruction then starts at trailing edge of NRDS. Upon completion, SC/MP provides NADS output to initiate next input/output cycle if bus access is granted. Time in microcycles from leading edge of delay flag to leading edge of subsequent NADS output is computed from the following formula:

$$\text{Delay} = [9 + 2(\text{AC}) + 2\ \text{disp} + 2^9\ \text{disp}]\ \text{microcycles}$$

where

(AC) = unsigned contents of accumulator

disp = unsigned displacement value contained in second byte of Delay Instruction

The time derived from the above formula does not include the four microcycles required to fetch the first byte of the Delay Instruction. Thus, when the Delay

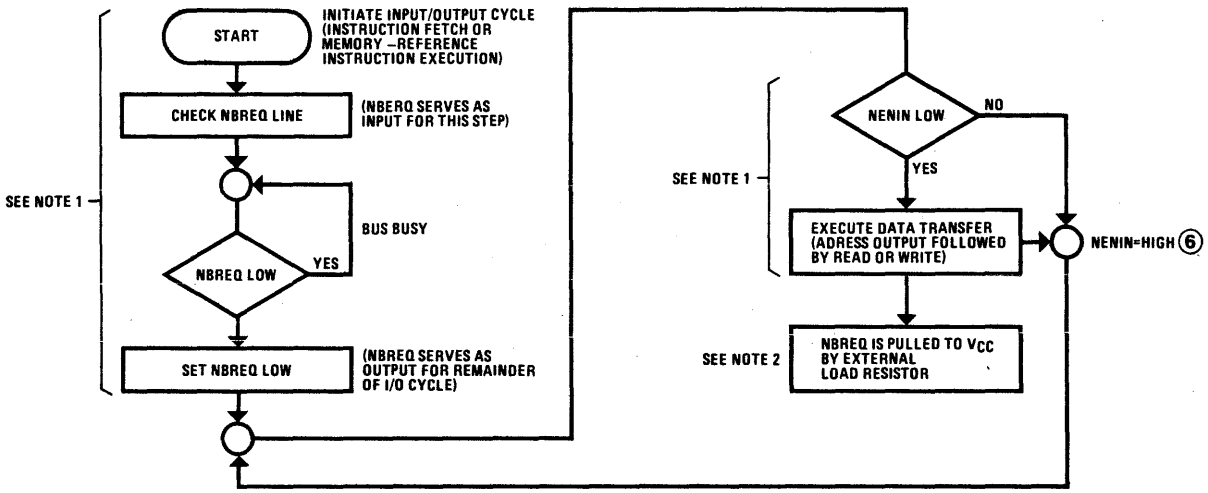
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Instruction is used for software timing, total instruction execution time equals [13 + 2(AC) + 2 disp + 2^9 disp] microcycles.

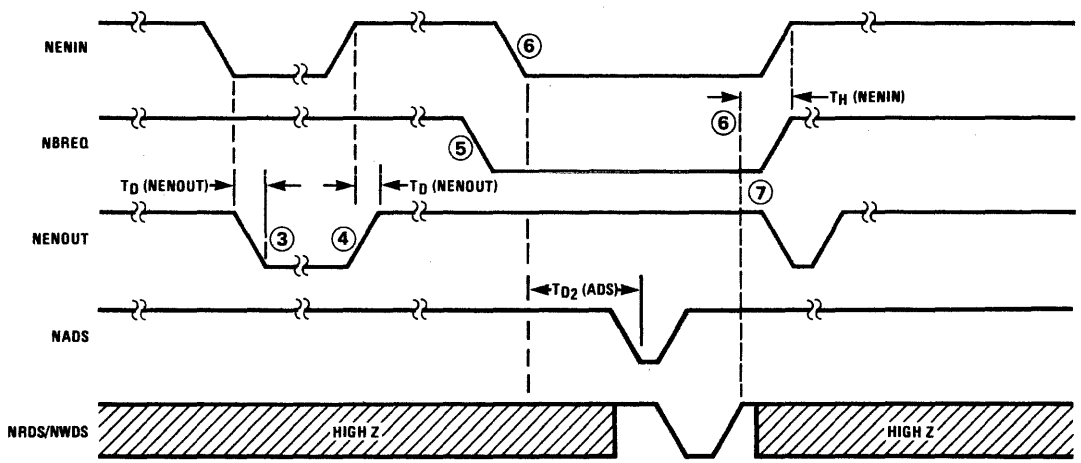
NOTE:

When Halt Instruction is executed, instruction decode and control logic inhibits incrementing of program counter for one input/output cycle. Thus, Halt Instruction is read from memory a second time to enable generation of HFLG output, but no further processing of Halt Instruction occurs. In effect, this procedure ensures HFLG is output in advance of the next instruction to be fetched from memory.

HFLG – Set high only during addressing interval of read cycle that follows Halt Instruction. HFLG may be used to cause user-provided external logic to set the CONT input low, and thereby to effect a programmed halt. Since HFLG read cycle precedes the next instruction



A. NBREQ and NENIN Processing Sequence



B. NBREQ, NENIN, and NENOUT Timing

Note 1: NENOUT is always high while SC/MP is actually using bus; that is, NENIN input and NBREQ output are low.

Note 2: When SC/MP is not using bus (NBREQ output or NENIN input high), NENOUT is held in same state as NENIN input.

Note 3: NENOUT goes low to indicate that SC/MP was granted access to bus (NENIN low) but is not using bus.

Note 4: NENOUT goes high in response to high NENIN input.

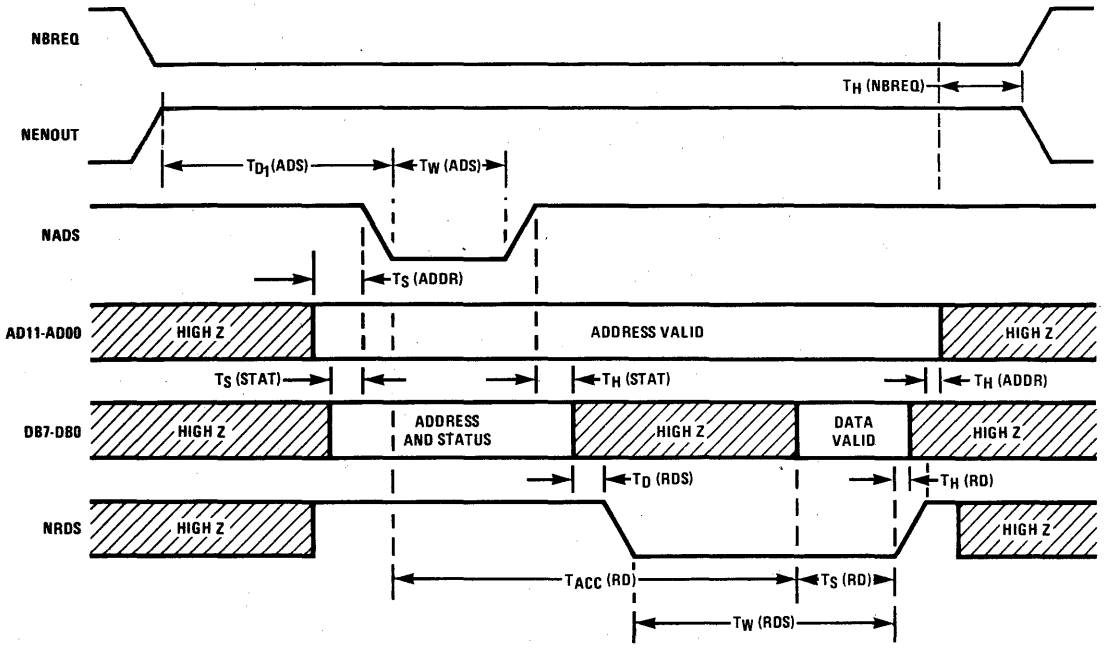
Note 5: SC/MP generates bus request; bus access not granted because NENIN high.

Note 6: NENIN goes low. Bus access now granted and input/output cycle actually initiated. If NENIN is set high while SC/MP has access to the bus, the address and data ports will go to the high-impedance (Tri-State®) state, but NBREQ will remain low. When NENIN is subsequently set low, the input/output cycle will begin again.

Note 7: Input/output cycle completed. NENOUT goes low to indicate that SC/MP granted access to bus but not using bus. If NENIN had been set high before completion of input/output cycle, NENOUT would have remained high.

FIGURE 4. Bus Access Control

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Note: Timing is valid when NENIN is low before NBREQ is set low by SC/MP; see figure 4 for NADS timing when NENIN is set low after NBREQ.

FIGURE 5. SC/MP Data Input Timing

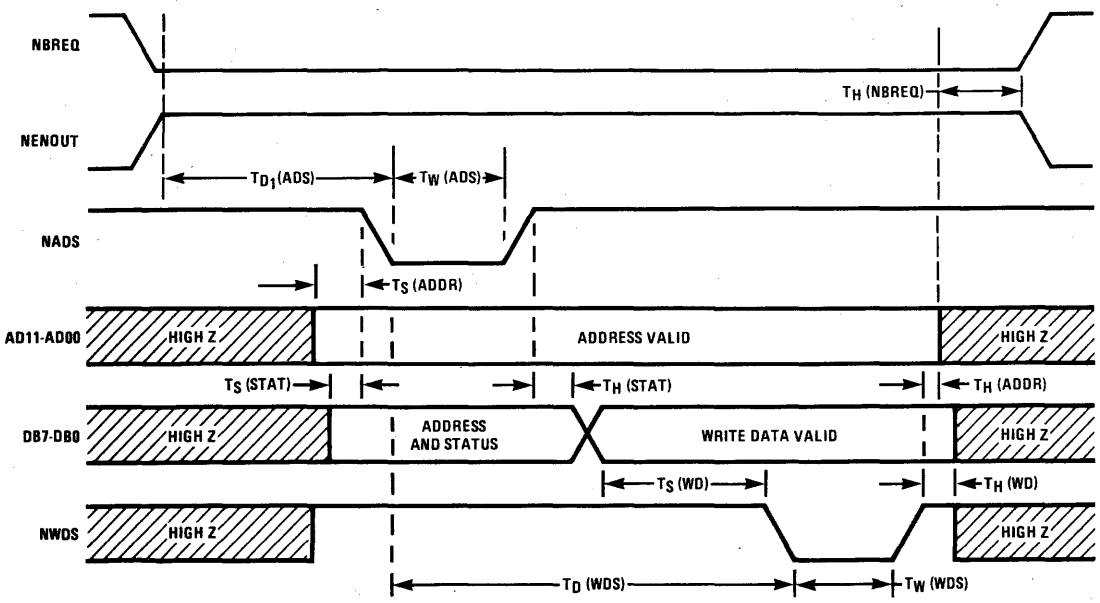


FIGURE 6. Data Output Timing

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fetch, termination of programmed halt enables fetch of first instruction that follows Halt Instruction.

After resetting the NADS output, SC/MP generates an NRDS or NWDS strobe, respectively, to initiate a data-input (read) or data-output (write) operation. For a read operation, input data are strobed into SC/MP from the 8-bit bus on the trailing edge of the NRDS strobe. For a write operation, SC/MP places valid output data on the 8-bit bus on the leading edge of the NWDS strobe. After resetting the NRDS or NWDS strobe to complete the data transfer, SC/MP then resets the NBREQ signal to indicate that the system busses are free for use by another controller.

INPUT/OUTPUT CYCLE EXTENSION

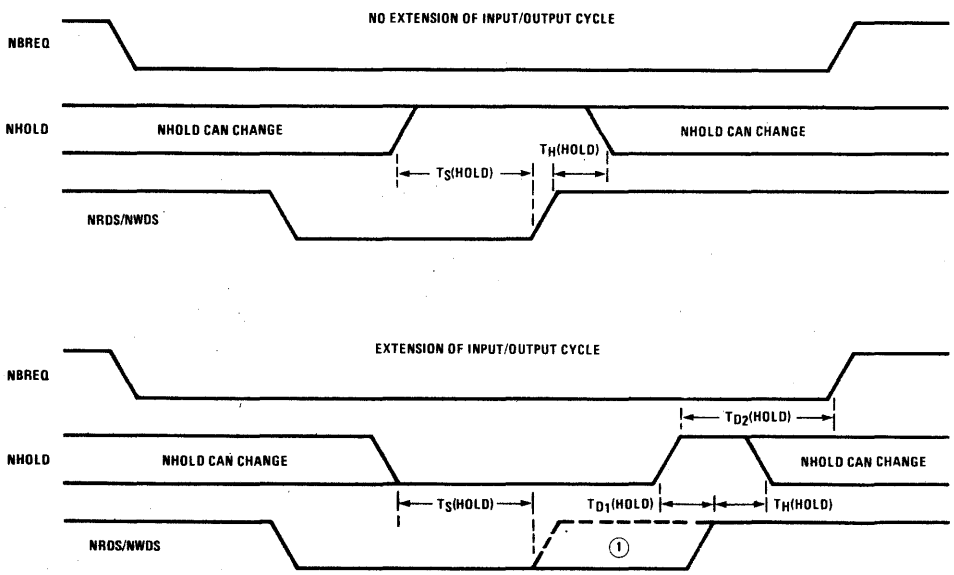
As shown in figure 7, the NHOLD signal may be set low prior to the trailing edge of the NRDS or NWDS strobe to cause SC/MP to lengthen the input/output cycle by holding the strobe active until after the NHOLD signal is returned high. Since there is no restriction on the maximum duration of the NHOLD signal, it can be used in a variety of applications ranging from accommodation of memories/peripherals with long access times to single-cycle control of the operating program for software debug purposes.

Figure 8 illustrates a typical circuit that may be used to generate an NHOLD signal of repeatable duration. The circuit shown employs a DM74165 8-Bit Parallel In/Serial Out Shift Register to allow selection of an input/output cycle extend time that ranges from $T_C/2$ to $2T_C$ in increments of $T_C/2$. Functional operation of the circuit is controlled by the NADS strobe and XOUT signals. Each time that the NADS strobe goes low, the data present at the A through H terminals are loaded into the shift register in parallel. When the NADS strobe subsequently returns high, the data are then shifted out serially on the positive-to-negative transitions of XOUT. Thus, the NHOLD output of the circuit is set low on the leading edge of each NADS strobe and, as shown in the chart that accompanies the circuit diagram, it remains low for a time period ranging from three clock cycles minimum (B, C, D, and E inputs = Logic "1") to seven clock cycles maximum (B, C, D, and E inputs = Logic "0").

It is important to note that instruction execution time is increased whenever an input/output cycle is extended via the NHOLD signal. For purposes of computing the increase in instruction execution time, it is necessary to distinguish between the terms *Input/Output Cycle Delay Period* and *Input/Output Cycle Extend Time*. The term *Input/Output Cycle Delay Period* refers to the time that the NRDS/NWDS strobe is actually "stretched" to provide the required memory or peripheral access time. The term *Input/Output Cycle Extend Time* refers to the additional number of microcycles required by the internal SC/MP microprogram to complete the extended input/output cycle; that is:

Input/Output Cycle Delay Period	Input/Output Cycle Extend Time
$T_C/2$ through $2T_C$ ($> 0 \leqslant 1$ μcycle)	1 μcycle
$5T_C/2$ through $4T_C$ ($> 1 \leqslant 2$ μcycles)	2 μcycles
$9T_C/2$ through $6T_C$ ($> 2 \leqslant 3$ μcycles)	3 μcycles
etc.	etc.

The total increase in instruction execution time, therefore, is equal to the *Input/Output Cycle Extend Time* multiplied by the total number of input/output cycles associated with the instruction. For example, a DLD Instruction is normally executed in 22 microcycles. Since this instruction employs three read input/output cycles and one write input/output cycle, an *Input/Output Cycle Extend Time* of one microcycle would increase total DLD Instruction execution time to 26 microcycles.

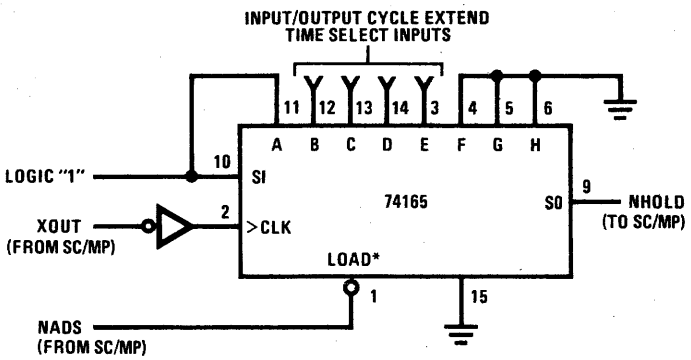


Note 1: In order to extend the input/output cycle, NHOLD must remain low until the point where NRDS/NWDS would have made a low-to-high transition with NHOLD inactive. Dashed line indicates the trailing edge of NRDS/NWDS when NHOLD is not active.

FIGURE 7. NHOLD Timing

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Data Inputs B C D E	NHOLD Duration (in clock cycles)	Input/Output Cycle		Required Memory Access Time [T_{ACC} (RD)]
		Delay Period	Extend Time in Microcycles	
1 1 1 1	3	0	0	$2T_C - 200$
1 1 1 0	4	$T_C/2$	1	$(5T_C/2) - 200$
1 1 0 0	5	T_C	1	$3T_C - 200$
1 0 0 0	6	$3T_C/2$	1	$(7T_C/2) - 200$
0 0 0 0	7	$2T_C$	1	$4T_C - 200$

FIGURE 8. Typical NHOLD Control Circuit

serial data transfers

Serial input/output data transfers can be used efficiently with very slow input/output peripherals such as X-Y plotters, teletypewriters, slow-speed printers, and so forth. Such transfers can be effected in any of the following manners:

1. By assigning serial input/output functions to the extension register via the SIO (Serial Input/Output) Instruction. When this instruction is executed, the contents of the extension register are shifted right one bit. At the same time, data present on the SIN line are shifted into bit position 7 of the extension register and the original contents of bit position 0 are shifted into a flip-flop to provide a latched output of the SOUT line. The SOUT data are then held latched until the next SIO instruction is executed.

2. By using one of the status flags as an output data bit and one of the sense lines as an input data bit.

3. By implementing external logic such that only one line of the 8-bit data input/output bus is used.

For synchronous systems, serial data input/output timing may be provided by program loops that employ the delay instruction, or by using one or more of the transfer instructions (see table 2) to test the output of an external timing circuit. For asynchronous systems, one of the sense inputs can be used for testing bit-received/ready status and a pulsed flag output can be provided, under program control, for peripheral indexing each time that a data bit is actually shifted in or out.

Systems that have several input/output devices must be multiplexed; device selection can then be accomplished using the status flag outputs of SC/MP, or by using parallel input/output commands to load an external latch. Systems that do not require serial input/output capability can employ the SIN and SOUT lines as a sense input and flag output, respectively.

interrupts

When the internal interrupt enable (IE) flag is set under program control, the Sense A line is enabled to serve as an interrupt request input; when the IE flag is reset, SC/MP is inhibited from detecting interrupts. Thus, while the IE flag is set, the Sense A input is tested prior to the fetch phase of each instruction as shown in figure 9. Upon detection of an interrupt request (Sense A high), the following events occur automatically.

1. The status register IE flag is reset to prevent SC/MP from responding to any further interrupt requests. Interrupt request capability can then be reenabled during or at the end of the ensuing user-generated interrupt service routine via the IEN (Enable Interrupt) Instruction or by copying the accumulator into the status register.

2. The contents of the program counter are exchanged with the contents of the pointer register 3.

3. The contents of the program counter are incremented by one to address the first instruction of the user-generated interrupt service routine.

The interrupt system must be armed before interrupts are enabled. This is accomplished as follows:

1. First, the Interrupt Enable Bit in the Status Register is set true by executing either an Enable Interrupt Instruction (IEN) or a Copy Accumulator to Status Register Instruction (CAS).

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2. Second, one additional instruction is fetched and executed.

A return from interrupt is accomplished by executing two instructions: Enable Interrupt (IEN) immediately followed by Exchange Pointer 3 with Program Counter (XPPC 3).

microprocessor halt

The CONT input to SC/MP is provided to enable suspension of operation without loss of internal status. Processing of the CONT input is shown in figure 9. Since this is an asynchronous input, it can be controlled by external timing logic, or as stated previously, the HALT flag output that appears on the 8-bit data bus (during the read cycle that follows execution of a Halt Instruction) can be used with an external circuit to effect a programmed halt condition. Note that when an interrupt request is detected while the CONT input is low, the first instruction of the user-generated interrupt service routine is automatically executed. Thus, the first instruction of the interrupt service routine can be used to reset the external CONT input logic and, thereby, to terminate the microprocessor halt condition if so desired.

After execution of an instruction, the CONT input must be high for a minimum time of $2T_C$ (1 microcycle) in order to fetch and execute the next instruction.

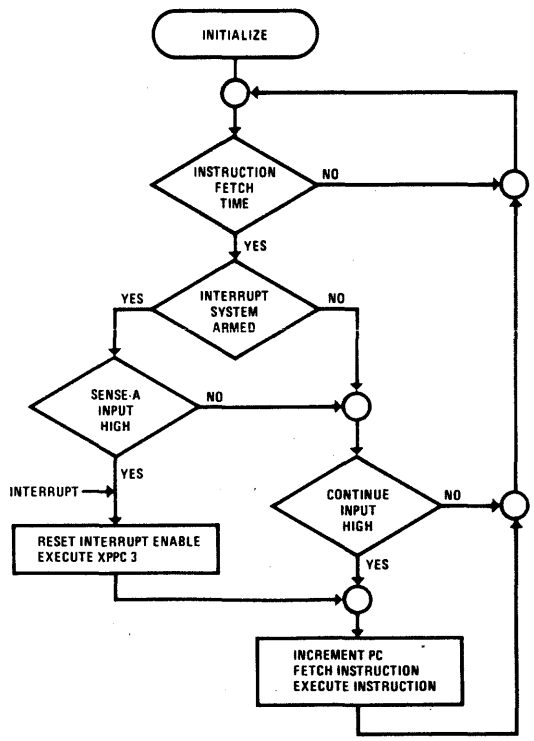


FIGURE 9.

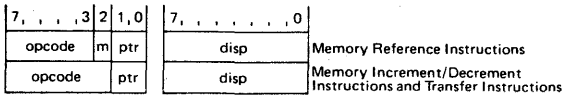
Microprocessor Halt and Interrupt Request Input Processing

instruction set

The SC/MP instruction set provides the general-purpose user of microprocessors a powerful programming capability along with above-average flexibility and speed. The instruction set consists of 46 instructions, which comprise eight general categories. A listing of the complete instruction set is provided in table 2; typical instruction execution times are given in table 3, and notations and symbols used as shorthand expressions of instruction capability are defined in table 4.

ADDRESSING

During execution, instructions and data defined in a program are stored into and loaded from specific memory locations, the accumulator, or selected registers. Because SC/MP, memory (read/write and read-only), and peripherals are on a common data bus, any instruction used to address memory may be used to address the peripherals. The formats of the instruction groups that reference memory are shown below.



Memory-reference instructions use the PC-relative, indexed, or auto-indexed methods of addressing memory. The memory-increment/decrement instructions and the transfer instructions use the PC-relative or indexed methods of addressing.

The various methods of addressing memory and peripherals are shown below.

Immediate addressing is an addressing format specific to the immediate instruction group.

Type of Addressing	Operand Formats		
	m	ptr	disp
PC-relative	0	0	-128 to +127
Indexed	0	1, 2, or 3	-128 to +127
Immediate	1	0	-128 to +127
Auto-indexed	1	1, 2, or 3	-128 to +127

For PC-relative, indexed, and auto-indexed memory-reference instructions, another feature of the addressing architecture is that the contents of the extension register are substituted for the displacement if the instruction displacement equals -128 (-X'80).

NOTE:

All arithmetic operations associated with address formation affect only the 12 low-order address bits; no carry is provided to the 4 high-order bits. For systems employing memories of 4k or less, the high-order bits can be ignored as they are set to 0000 following initialization. For systems employing larger memories, the high-order bits must be set to the starting address of the desired 4k block of memory. For example:

0001_2 enables memory locations 1000_{16} - $1FFF_{16}$ to be addressed.

0010_2 enables memory locations 2000_{16} - $2FFF_{16}$ to be addressed and so forth.

PC-Relative Addressing – A PC-relative address is formed by adding the displacement value specified in the operand field of the instruction to the current contents of the program counter. The displacement is an 8-bit twos-

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complement number, so the range of the PC-relative addressing format is -128_{10} to $+127_{10}$ locations from the current contents of the program counter.

Immediate Addressing – Immediate addressing uses the value in the second byte of a double-byte instruction as the operand for the operation to be performed (see below).

For example, compare a Load (LD) instruction to a Load Immediate (LDI) instruction. The Load instruction uses the contents of the second byte of the instruction in computing the effective address of the data to be loaded. The Load Immediate instruction uses the contents of the second byte as the data to be loaded.

Indexed Addressing – Indexed addressing enables the programmer to address any location in memory through the use of the pointer register and the displacement. When indexed addressing is specified in an instruction, the contents of the designated pointer register are added to the displacement to form the effective address. The contents of the pointer register are not modified by indexed addressing.

Auto-Indexed Addressing – Auto-indexed addressing provides the same capabilities as indexed addressing along with the ability to increment or decrement the designated pointer register by the value of the displacement. If the displacement is less than zero, the pointer register is decremented by the displacement before the contents of the effective address are fetched or stored. If the displacement is equal to or greater than zero, the pointer register is used as the effective address, and the pointer register is incremented by the displacement after the contents of the effective address are fetched or stored.

system implementation

Figures 10 through 12 illustrate typical SC/MP system configurations. In figure 10, SC/MP is shown interconnected to three memory devices to form a stand-alone 4-device system that provides 256 words of read/write memory and 2,048 words for program storage. Figure 11 shows SC/MP interconnected to an external controller for Direct Memory Access (DMA) operation, and figure 12 illustrates a multiprocessor application using SC/MP's built-in logic to control bus access.

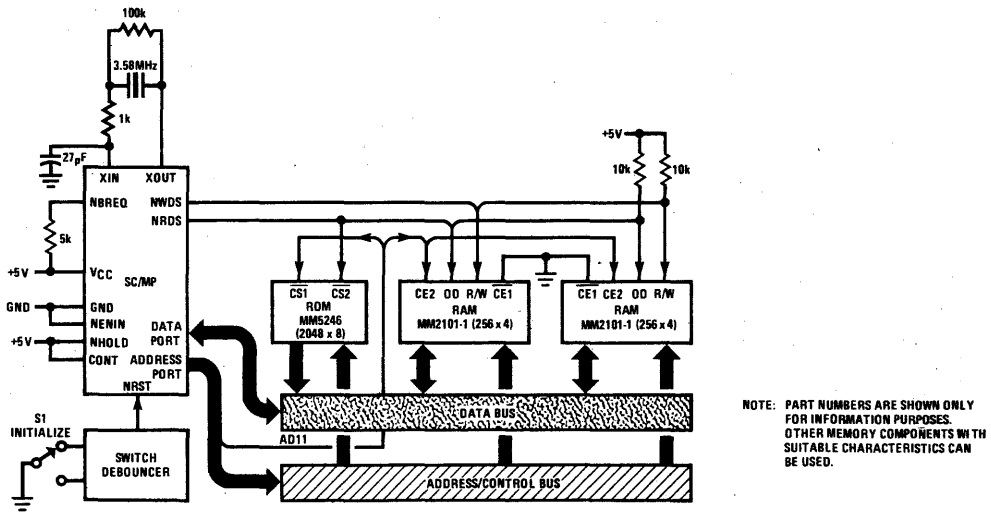


FIGURE 10. SC/MP-II Four-Chip System

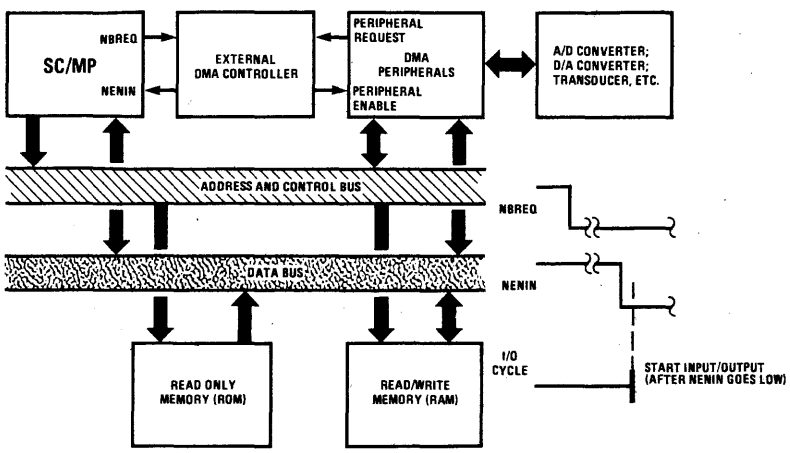


FIGURE 11. SC/MP-II Interconnected for Direct Memory Access (DMA) Operation

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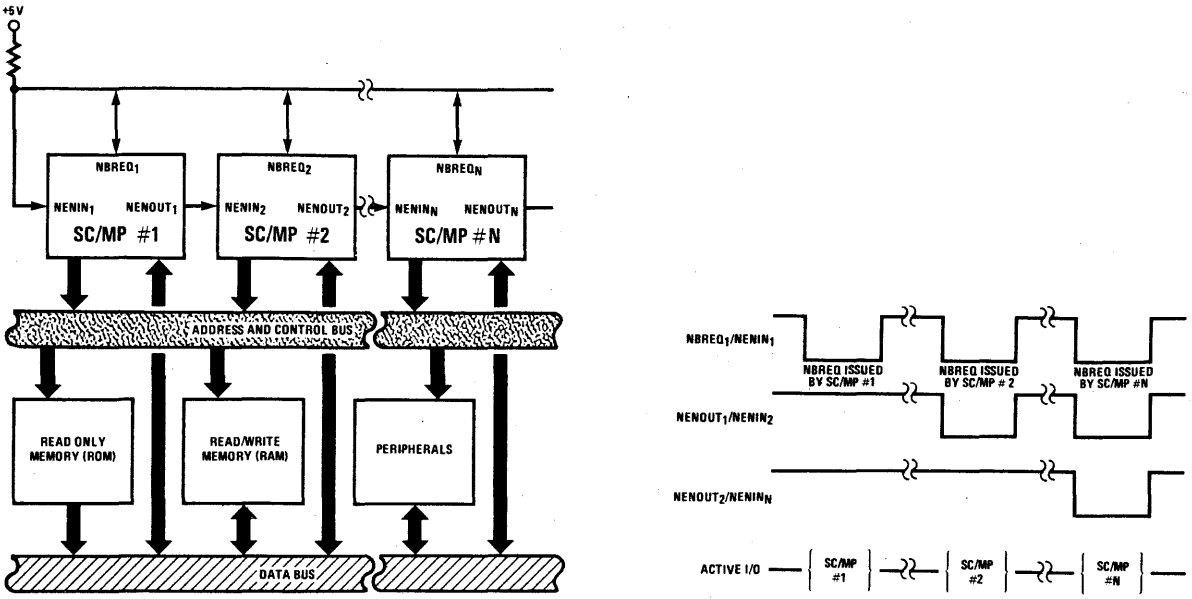
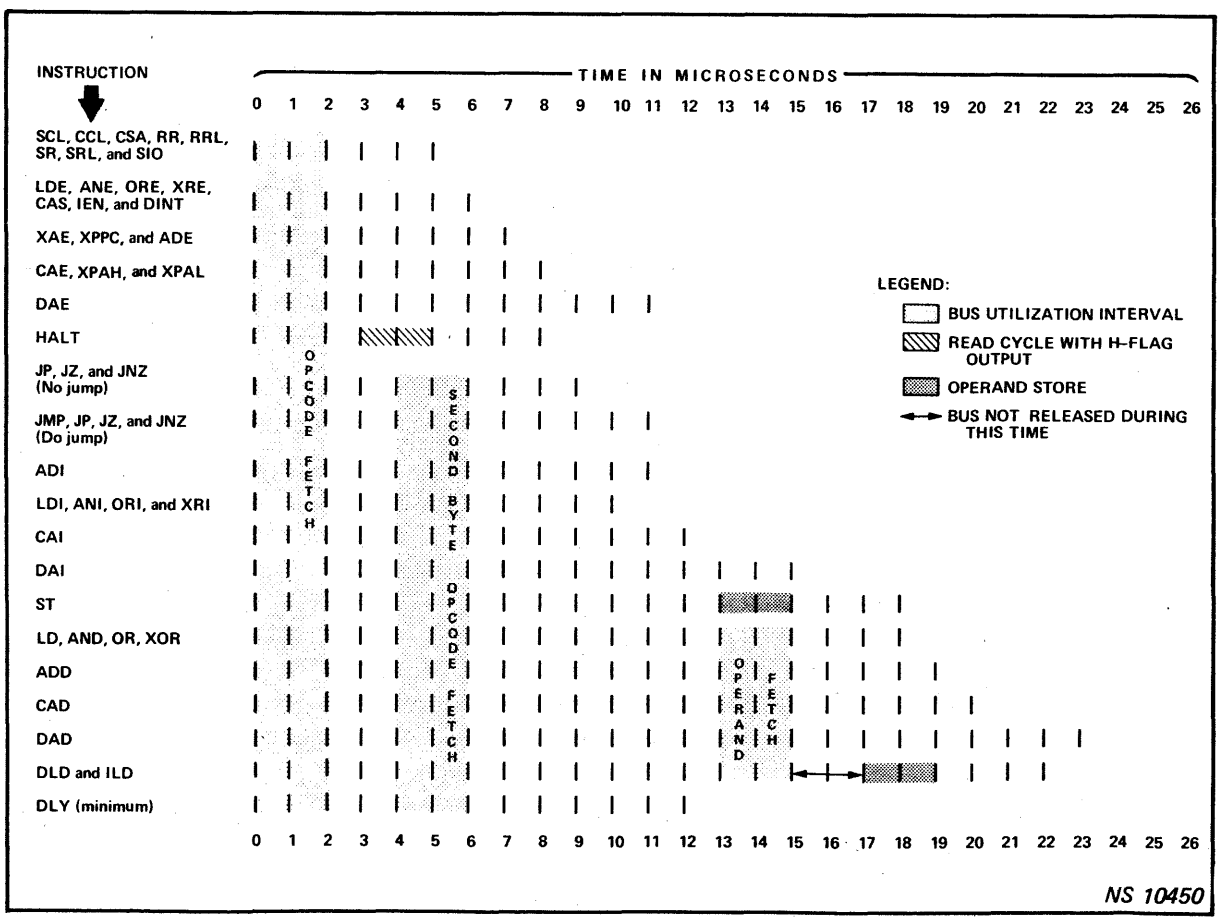


FIGURE 12. Multiprocessor System Using SC/MP-II Built-in Logic for Bus Control

TABLE 2. Bus Utilization of Each Instruction



National Semiconductor
MICROPROCESSOR

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DOUBLE-BYTE INSTRUCTIONS

TABLE 3. SC/MP Instruction Summary

MNEMONIC	DESCRIPTION	OBJECT FORMAT	OPERATION	MICRO-CYCLES
	Memory Reference Instructions	7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0		
LD	Load	1 1 0 0 0 m ptr | disp	(AC)←(EA)	18
ST	Store	1 1 0 0 1	(EA)←(AC)	18
AND	AND	1 1 0 1 0	(AC)←(AC) ∧ (EA)	18
OR	OR	1 1 0 1 1	(AC)←(AC) ∨ (EA)	18
XOR	Exclusive-OR	1 1 1 0 0	(AC)←(AC) $\forall$ (EA)	18
DAD	Decimal Add	1 1 1 0 1	$(AC)\leftarrow(AC)_{10} + (EA)_{10} + (CY/L);(CY/L)$	23
ADD	Add	1 1 1 1 0	(AC)←(AC) + (EA) + (CY/L);(CY/L),(OV)	19
CAD	Complement and Add	1 1 1 1 1	(AC)←(AC) + ~(EA) + (CY/L);(CY/L),(OV)	20
	Memory Increment/Decrement Instructions	7 6 5 4 3 2 | 1 0 | 7 6 5 4 3 2 1 0		
ILD	Increment and Load	1 0 1 0 1 0 ptr | disp	(AC), (EA)←(EA) + 1	22
DLD	Decrement and Load	1 0 1 1 1 0	(AC), (EA)←(EA) − 1	22
	Immediate Instructions	7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0		
LDI	Load Immediate	1 1 0 0 0 1 0 0 | data	(AC)← data	10
ANI	AND Immediate	1 1 0 1 0 1 0 0	(AC)←(AC) ∧ data	10
ORI	OR Immediate	1 1 0 1 1 1 0 0	(AC)←(AC) ∨ data	10
XRI	Exclusive-OR Immediate	1 1 1 0 0 1 0 0	(AC)←(AC) $\forall$ data	10
DAI	Decimal Add Immediate	1 1 1 0 1 1 0 0	$(AC)\leftarrow(AC)_{10} + data_{10} + (CY/L);(CY/L)$	15
ADI	Add Immediate	1 1 1 1 0 1 0 0	(AC)←(AC) + data + (CY/L);(CY/L),(OV)	11
CAI	Complement and Add Immediate	1 1 1 1 1 1 0 0	(AC)←(AC) + ~data + (CY/L);(CY/L),(OV)	12
	Transfer Instructions	7 6 5 4 3 2 | 1 0 | 7 6 5 4 3 2 1 0		
JMP	Jump	1 0 0 1 0 0 ptr | disp	(PC)←EA	11
JP	Jump if Positive	1 0 0 1 0 1	If (AC) ⩾ 0, (PC)←EA	9, 11
JZ	Jump if Zero	1 0 0 1 1 0	If (AC) = 0, (PC)←EA	9, 11
JNZ	Jump if Not Zero	1 0 0 1 1 1	If (AC) ≠ 0, (PC)←EA	9, 11
	Double-Byte Miscellaneous Instructions	7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0		
DLY	Delay	1 0 0 0 1 1 1 1 | disp	count AC to −1, delay = 13 + 2(AC) + 2 disp + 2^9 disp microcycles	13 to 131,593

SINGLE-BYTE INSTRUCTIONS

MNEMONIC	DESCRIPTION	OBJECT FORMAT	OPERATION	MICRO-CYCLES
	Extension Register Instructions	7 6 5 4 3 2 1 0		
LDE	Load AC from Extension	0 1 0 0 0 0 0 0	(AC)←(E)	6
XAE	Exchange AC and Extension	0 0 0 0 0 0 0 1	(AC)↔(E)	7
ANE	AND Extension	0 1 0 1 0 0 0 0	(AC)←(AC) ∧ (E)	6
ORE	OR Extension	0 1 0 1 1 0 0 0	(AC)←(AC) ∨ (E)	6
XRE	Exclusive-OR Extension	0 1 1 0 0 0 0 0	(AC)←(AC) $\forall$ (E)	6
DAE	Decimal Add Extension	0 1 1 0 1 0 0 0	$(AC)\leftarrow(AC)_{10} + (E)_{10} + (CY/L);(CY/L)$	11
ADE	Add Extension	0 1 1 1 0 0 0 0	(AC)←(AC) + (E) + (CY/L);(CY/L),(OV)	7
CAE	Complement and Add Extension	0 1 1 1 1 0 0 0	(AC)←(AC) + ~(E) + (CY/L);(CY/L),(OV)	8
	Pointer Register Move Instructions	7 6 5 4 3 2 1 0		
XPAL	Exchange Pointer Low	0 0 1 1 0 0 ptr	$(AC)\leftrightarrow(PTR_{7:0})$	8
XPAH	Exchange Pointer High	0 0 1 1 0 1	$(AC)\leftrightarrow(PTR_{15:8})$	8
XPPC	Exchange Pointer with PC	0 0 1 1 1 1	(PC)↔(PTR)	7
	Shift, Rotate, Serial I/O Instructions	7 6 5 4 3 2 1 0		
SIO	Serial Input/Output	0 0 0 1 1 0 0 1	$(E_i)\rightarrow(E_{i-1})$, SIN→$(E_7)$, (E_0)→SOUT	5
SR	Shift Right	0 0 0 1 1 1 0 0	$(AC_i)\rightarrow(AC_{i-1})$, 0→$(AC_7)$	5
SRL	Shift Right with Link	0 0 0 1 1 1 0 1	$(AC_i)\rightarrow(AC_{i-1})$, (CY/L)→$(AC_7)$	5
RR	Rotate Right	0 0 0 1 1 1 1 0	$(AC_i)\rightarrow(AC_{i-1})$, $(AC_0)\rightarrow(AC_7)$	5
RRL	Rotate Right with Link	0 0 0 1 1 1 1 1	$(AC_i)\rightarrow(AC_{i-1})$, $(AC_0)\rightarrow$(CY/L)→(AC_7)	5
	Single-Byte Miscellaneous Instructions	7 6 5 4 3 2 1 0		
HALT	Halt	0 0 0 0 0 0 0 0	Pulse H-flag	8
CCL	Clear Carry/Link	0 0 0 0 0 0 1 0	(CY/L)←0	5
SCL	Set Carry/Link	0 0 0 0 0 0 1 1	(CY/L)←1	5
DINT	Disable Interrupt	0 0 0 0 0 1 0 0	(IE)←0	6
IEN	Enable Interrupt	0 0 0 0 0 1 0 1	(IE)←1	6
CSA	Copy Status to AC	0 0 0 0 0 1 1 0	(AC)←(SR)	5
CAS	Copy AC to Status	0 0 0 0 0 1 1 1	(SR)←(AC)	6
NOP	No Operation	0 0 0 0 1 0 0 0	None	5

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TABLE 4. Instruction Execution Time

INSTRUCTION	READ CYCLES	WRITE CYCLES	TOTAL MICROCYCLES	INSTRUCTION	READ CYCLES	WRITE CYCLES	MICROCYCLES
ADD	3	0	19	JP	2	0	9, 11 for Jump
ADE	1	0	7	JZ	2	0	9, 11 for Jump
ADI	2	0	11	LD	3	0	18
AND	3	0	18	LDE	1	0	6
ANE	1	0	6	LDI	2	0	10
ANI	2	0	10	NOP	1	0	5
CAD	3	0	20	OR	3	0	18
CAE	1	0	8	ORE	1	0	6
CAI	2	0	12	ORI	2	0	10
CAS	1	0	6	RR	1	0	5
CCL	1	0	5	RRL	1	0	5
CSA	1	0	5	SCL	1	0	5
DAD	3	0	23	SIO	1	0	5
DAE	1	0	11	SR	1	0	5
DAI	2	0	15	SRL	1	0	5
DINT	1	0	6	ST	2	1	18
DLD	3	1	22	XAE	1	0	7
DLY	2	0	13 - 131593	XOR	3	0	18
HALT	2	0	8	XPAH	1	0	8
IEN	1	0	6	XPAL	1	0	8
ILD	3	1	22	XPPC	1	0	7
JMP	2	0	11	XRE	1	0	6
JNZ	2	0	9, 11 for Jump	XRI	2	0	10

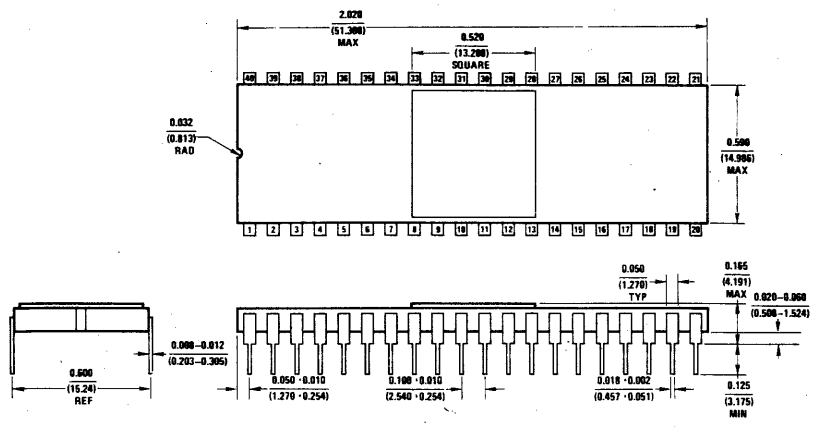
Note: If slow memory is being used, the appropriate delay should be added for each read or write cycle.

TABLE 5. Symbols and Notations Used to Express Instruction Execution

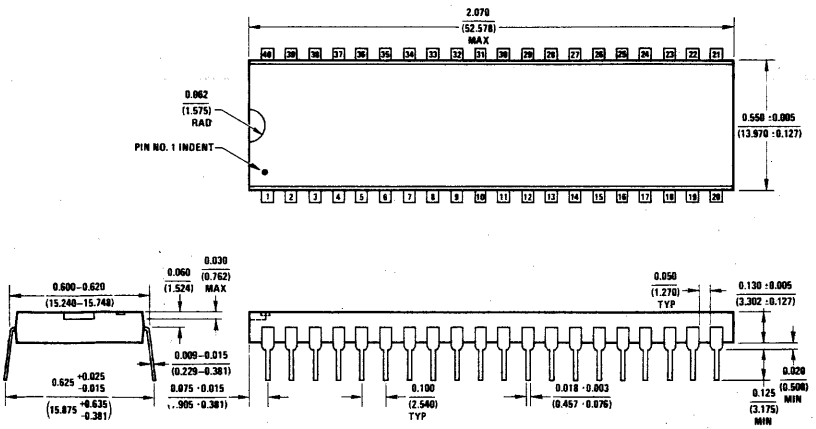
SYMBOL AND NOTATION	MEANING
AC	8-bit Accumulator.
CY/L	Carry/Link Flag in the Status Register.
data	Signed, 8-bit immediate data field.
disp	Displacement; represents an operand in a nonmemory reference instruction or an address modifier field in a memory reference instruction. It is a signed twos-complement number.
EA	Effective Address as specified by the instruction.
E	Extension Register; provides for temporary storage, variable displacements and separate serial input/output port.
i	Unspecified bit of a register.
IE	Interrupt Enable Flag.
m	Mode bit, used in memory reference instructions. Blank parameter sets m = 0, @ sets m = 1.
OV	Overflow Flag in the Status Register.
PC	Program Counter (Pointer Register 0); during address formation, PC points to the last byte of the instruction being executed.
ptr	Pointer Register (ptr = 0 through 3). The register specified in byte 1 of the instruction.
$ptr_{n:m}$	Pointer register bits; n:m = 7 through 0 or 15 through 8.
SIN	Serial Input pin.
SOUT	Serial Output pin.
SR	8-bit Status Register.
( )	Means "contents of." For example, (EA) is contents of Effective Address.
[ ]	Means optional field in the assembler instruction format.
~	Ones complement of value to right of ~.
→	Means "replaces."
←	Means "is replaced by."
↔	Means "exchange."
@	When used in the operand field of the instruction, sets the mode bit (m) to 1 for auto-incrementing/auto-decrementing indexing.
10^+	Modulo 10 addition.
∧	AND operation.
∨	Inclusive-OR operation.
⊻	Exclusive-OR operation.
⩾	Greater than or equal to.
=	Equals.
≠	Does not equal.

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physical dimensions



40-Lead Ceramic Dual-in-Line Package (D)



40-Lead Plastic Dual-in-Line Package (N)

ordering information

The SC/MP device may be ordered through the local National Semiconductor sales representative or by contacting our world or international headquarters listed below. The order numbers are as follows:

For an "N" package – ISP-8A/600N
For a "D" package – ISP-8A/600D

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

National Semiconductor Corporation
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Preliminary

INS8900 Single-Chip 16-Bit N-Channel Microprocessor

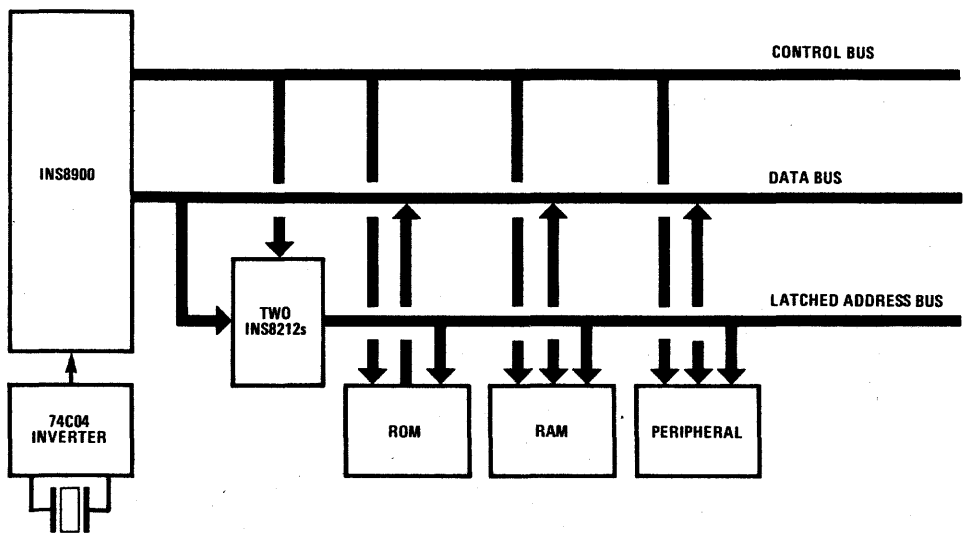
General Description

The INS8900 is a single-chip 16-bit microprocessor housed in a standard hermetically sealed 40-pin ceramic dual-in-line package. The INS8900 is fabricated using N-channel silicon gate MOS technology. The INS8900 is intended for use in applications where the convenience and efficiency of 16-bit word length is desired while maintaining the low cost inherent in single-chip fixed instruction microprocessors. The INS8900 is a true 16-bit central processor unit: it makes use of 16-bit instruction words and 16-bit data words, and features a powerful, efficient, and flexible set of 46 instructions. All instructions use a single-word 16-bit format, thus reducing memory accesses and program storage requirements. A unique feature of the INS8900 is the ability to operate on both 8-bit and 16-bit data words: this extends the inherent efficiency and power of a 16-bit processor to 8-bit applications.

Features

- 46 Instruction Types
- All Instructions Single Word
- Multiple Addressing Modes
  - Program-Counter Relative
  - Base Page
  - Indexed
  - Direct and Indirect
- Four General-Purpose Accumulators
- Byte and Word Processing
- Common Memory and Peripheral Addressing
- Six Hardware-Vectored Priority Interrupts
- 10-Word On-Chip Stack
- Three Control Flag Outputs
- Three Sense Inputs
- Four I/O Control Strobe Signals
- Single-Phase 2 MHz Clock
- Low-Power Schottky Compatible Outputs

INS8900 Minimum System Block Diagram



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Absolute Maximum Ratings

Voltage at Any Pin with Resepct to
Most Negative Supply (V_{BB}) . . . . . -0.3 V to +20 V
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range. . . . . -65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . +300°C

Electrical Characteristics

(T_A = 0°C to +70°C, V_{SS} = 0 V, V_{DD} = +12 V ± 5%, V_{CC} = +5 V ± 5%, V_{BB} = −8 V ± 5%)

Symbol	Parameter	Conditions	Min	Max	Units
OUTPUT SPECIFICATIONS					
	D00-D15, F11-F14, ODS, IDS, NADS (These are low-power Schottky-compatible push-pull outputs.)				
V_{OH}	Logic "1" Output Voltage	I_{OUT} = −500 μA	2.4		V
V_{OL}	Logic "0" Output Voltage	I_{OUT} = 900 μA		0.4	V
	NHALT, CONTIN (low-power Schottky outputs)				
V_{OH}	Logic "1" Output Voltage	I_{OUT} = −250 μA	2.4		V
V_{OL}	Logic "0" Output Voltage	I_{OUT} = 600 μA		0.4	V
INPUT SPECIFICATIONS					
	D00-D15, NIR2-NIR5, EXTEND, JC13-JC15, NINIT, CONTIN, NHALT (low-power Schottky inputs)				
V_{IH}	Logic "1" Input Voltage		2.4	V_{CC} + 1	V
V_{IL}	Logic "0" Input Voltage		−1.0	+0.8	V
I_L	Input Leakage Current (except NHALT, CONTIN, JC13-JC15)	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$ + 1		40	μA
I_{IL}	Logic "0" Input Current, NHALT, CONTIN (Note 2)	V_{IN} = 0.4 V		−7.0	mA
I_{IL}	Logic "0" Input Current, JC13-JC15 (Note 2)	V_{IN} = 0.4 V		−3.0	mA
	BPS (This is an MOS level input.)				
V_{IH}	Logic "1" Input Voltage		V_{DD} − 1	V_{DD} + 1	V
V_{IL}	Logic "0" Input Voltage		−1.0	+0.8	V
I_{IH}	Logic "1" Input Current (Note 3)	V_{IN} = 13.6 V		750	μA
	CLKX (This is an MOS level input.)				
V_{CIL}	Clock "0" Voltage		−1.0	+0.8	V
V_{CIH}	Clock "1" Voltage		V_{DD} − 1	V_{DD} + 1	V
C_{IN}	Input Capacitance			20	pF
I_{DD}	Average Supply Current (V_{DD}) (Note 4)	tp = 500 ns, T_A = 25°C		100	mA
I_{CC}	Average Supply Current (V_{CC}) (Note 4)	tp = 500 ns, T_A = 25°C		10	mA
I_{BB}	Average Supply Current (V_{BB})	V_{BB} = −8 V		−200	μA

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Timing Specifications

Symbol	Parameter	Conditions	Min	Max	Units
	CLKX				
t_r, t_f	Rise and Fall Times (Note 5) (Referenced to 10% and 90% amplitude)		5	30	ns
t_P	Clock Period		500	650	ns
t_{CLK}, t_{NCLK}	Pulse Width (Referenced to 50% amplitude)		$t_P/2 - 5\%$	$t_P/2 + 5\%$	ns
	EXTEND				
	Individual Extend Duration			2	μs
t_{ES}	Extend Setup Time (Note 6)		70		ns
t_{EH}	Extend Hold Time (Note 6)		120		ns
	Propagation Delay				
t_{DD1}	NHALT, CONTIN (Note 7)	C_L = 40 pF, 1 low-power Schottky load		200	ns
t_{DD2}	NADS, IDS, ODS, D00-D15 (Note 7)	C_L = 40 pF, 1 INS8208 load		200	ns
	D00-D15				
t_{DS}	Input Setup Time (Note 6)		50		ns
t_{DH}	Hold Time (Note 8)		0		ns
t_{FW}	F11-F14 Pulse Flag (PFLG) Pulse Width		$4t_P - 300$	$4t_P + 300$	ns
t_{NW}	NINIT Initialization Pulse Width		8		t_P
t_{IRW}	NIR2-NIR5 Input Pulse Width to Set Latch		1		t_P

Note 1: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.

Note 2: NHALT, CONTIN, and JC13-JC15 logic "0" input currents specified when the internal chip loads are putting out a logic "1."

Note 3: Pull-down transistor provided on chip.

Note 4: Supply currents measured with 40 pF and INS8208 loads.

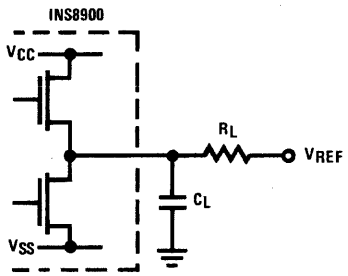
Note 5: Clamp diode and series damping resistor may be required to prevent clock overshoot.

Note 6: Measured with respect to appropriate valid logic level of CLKX.

Note 7: Delay measured from valid logic level on CLKX edge initiating change to valid output voltage level.

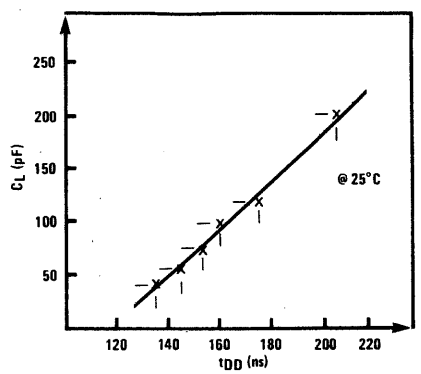
Note 8: With respect to the valid "0" level on the falling edge of Input Data Strobe (IDS).

Note 9: Typical load circuit:

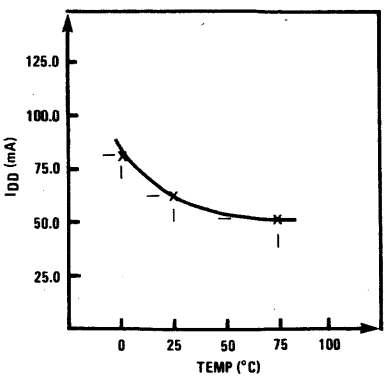


R_L = 3.6k (3.3k for testing)
C_L = 40 pF
V_{REF} = 1.72 V

Note 10: Typical output delay versus load capacitance C_L for load circuit in Note 9:



Note 11: Typical V_{DD} supply current versus temperature.



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Timing Waveforms

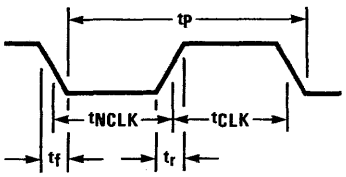


Figure 1. External Clock Timing (CLKX)

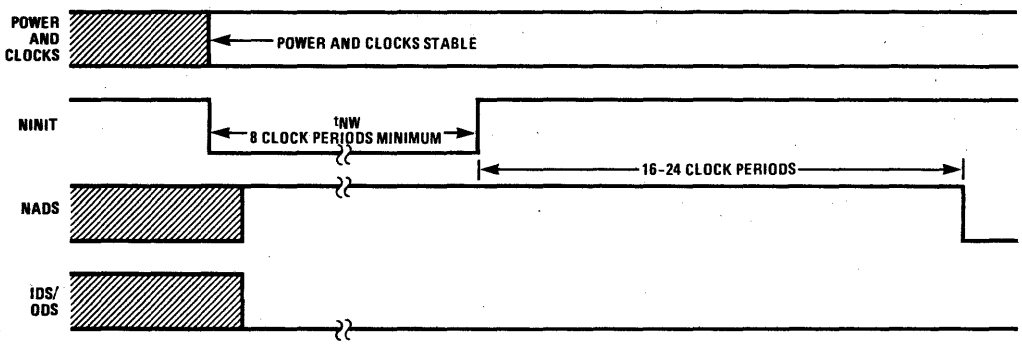
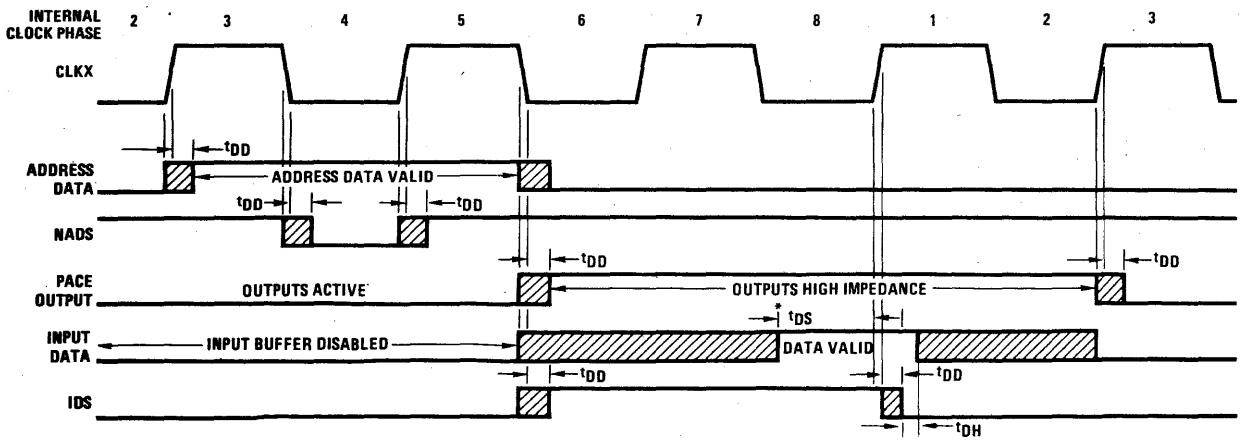


Figure 2. Initialization Timing



*V_{IN} MUST BE AT THE CORRECT LOGIC LEVEL AT THIS TIME.

NOTE: SIGNALS ARE REFERENCED TO VALID LOGIC LEVELS ON CLOCK INPUT. INTERNAL CLOCK PHASES ARE SHOWN FOR REFERENCE ONLY; THEY ARE NOT AVAILABLE EXTERNALLY.

Figure 3. Address Output and Data Input Timing

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Timing Waveforms (continued)

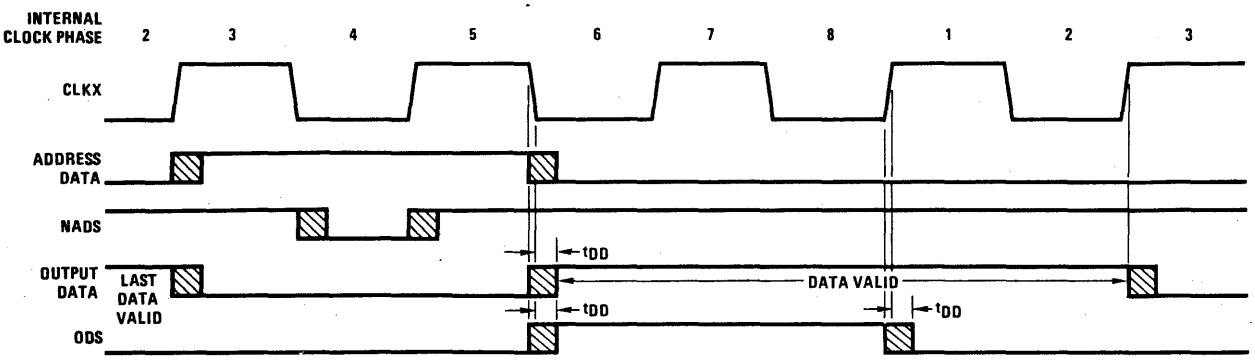


Figure 4. Data Output Timing

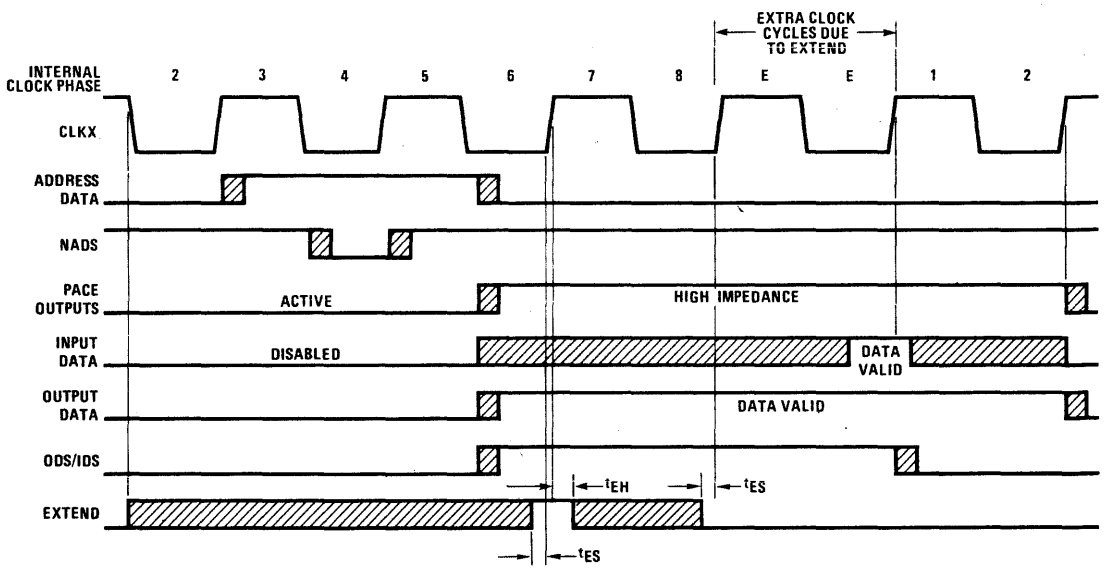


Figure 5. Extend I/O Signal Timing

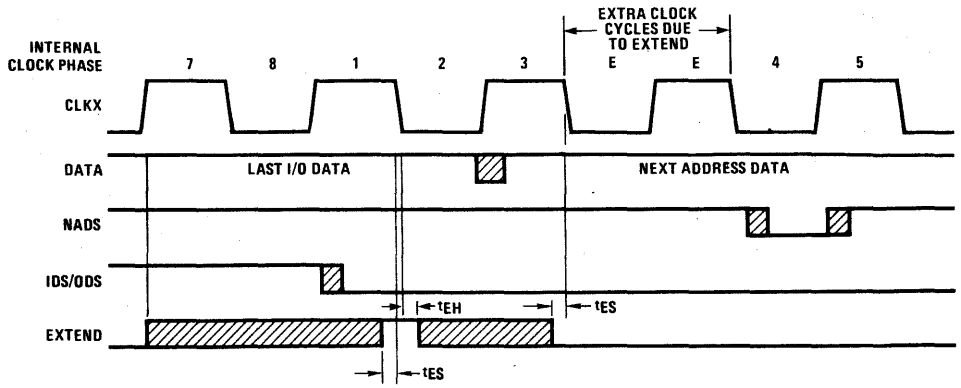
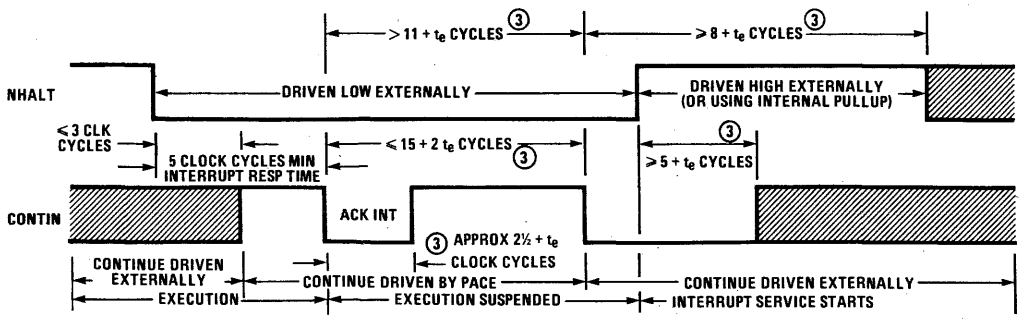


Figure 6. Suspend I/O Signal Timing

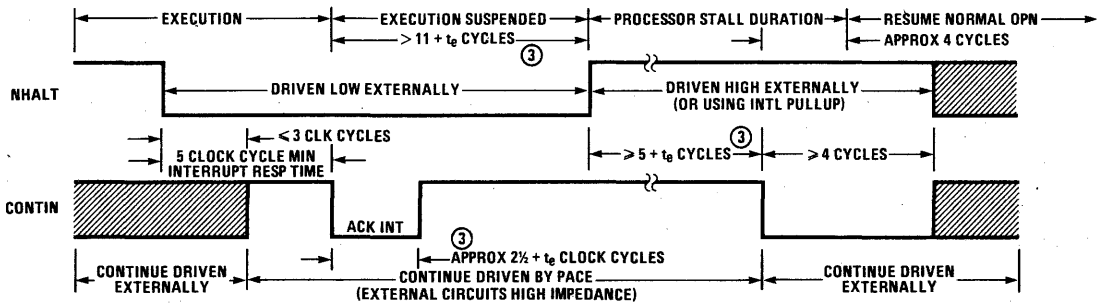
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Timing Waveforms (continued)



NOTES:
1. EXTERNALLY GENERATED TTL INPUTS OVERRIDE PACE OUTPUTS.
2. ▨ CROSSHATCH INDICATES "DON'T CARE" INPUT STATE.
3. t_e = DURATION OF EXTEND DURING PACE I/O CYCLES TIMING ASSUMES NO OTHER EXTENDS AND NO SUSPENDS.

Figure 7. Relative Timing for Level-0 Interrupt Generation



NOTES:
1. EXTERNALLY GENERATED TTL INPUTS OVERRIDE PACE OUTPUTS.
2. ▨ CROSSHATCH INDICATES "DON'T CARE" INPUT STATE.
3. t_e + DURATION OF EXTEND DURING PACE I/O CYCLES TIMING ASSUMES NO OTHER EXTENDS AND NO SUSPENDS.

Figure 8. Relative Timing for Processor Stall

The architecture of the INS8900 (shown in Figure 9) features a number of resources to minimize system program and read/write storage, increase throughput, and reduce the amount and cost of external support hardware. Principal resources that allow these efficiencies to be achieved include:

Four 16-bit general purpose working registers available to the user reduce the number of memory load and store operations associated with saving temporary and intermediate results in system memory.

An independent 16-bit status and control flag register automatically and continuously preserves system status. The user may operate on its contents as data, allowing masking, testing, and modification of several bit fields simultaneously.

A ten-word (16-bit) last-in, first-out (LIFO) stack inherently decreases response time to interrupts while eliminating both program and read/write system storage overhead associated with storing stack information outside the microprocessor chip.

Stack full/stack empty interrupts are provided to facilitate off-chip stack storage in those applications where additional stack capacity is desirable.

A six-level vectored priority interrupt system internal to the chip provides automatic interrupt identification, eliminating both program storage overhead and the time normally required to poll peripherals in order to identify the interrupting device.

Three sense inputs and four control flag outputs allow the user to respond directly to specific combinations of status present in the microprocessor-based system, thus eliminating costly hardware, program overhead, and throughput associated with implementing these functions over the system data bus.

A comprehensive set of input/output control signals provided by the internal control logic simplifies interfaces to memory and peripherals and allows flexible control of INS8900 operations.

Single-phase 2.0 MHz clock input is easily generated with a minimum of external components.

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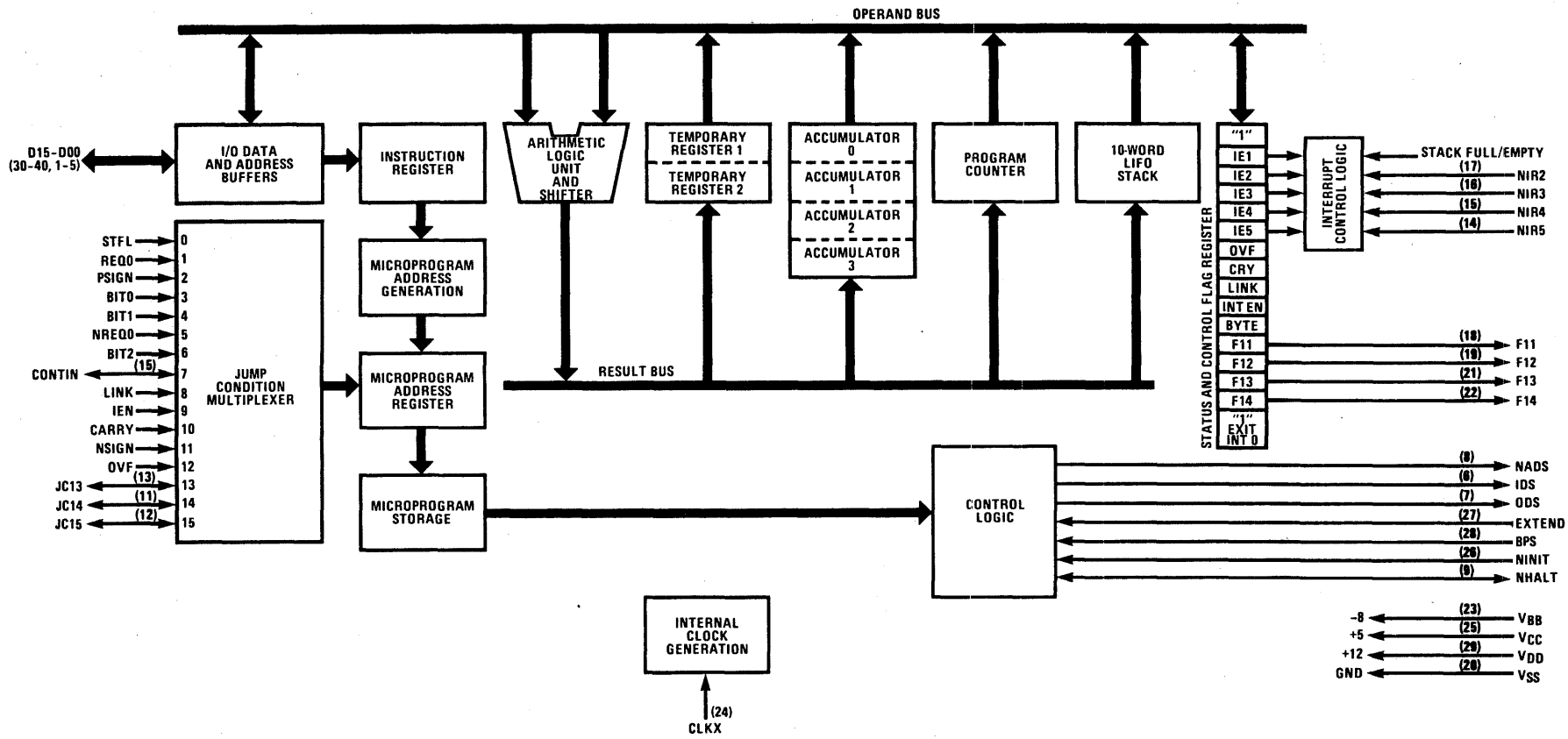


Figure 9. INS8900 Detailed Block Diagram

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INS8900 FUNCTIONAL PIN DEFINITIONS

The functions of each of the INS8900 signals are described below. Voltage and timing specifications for the signals are provided in the table of electrical characteristics and the timing diagrams, respectively.

CLKX (Input): External clock input (single-phase).

D00–D15 (Input/Output): Data bus lines. Bidirectional low-power Schottky-compatible lines used for input and output of data and for output of 16-bit addresses on I/O cycles.

NADS (Output): Address Data Strobe. The negative-true NADS signal is sent out at the beginning of every data input/output cycle and indicates that a memory or peripheral address has been output on the data bus lines. The address is stable on the data bus while the NADS signal is active low.

ODS (Output): Output Data Strobe. The ODS signal indicates to external circuits that the data bus contains valid output data.

IDS (Output): Input Data Strobe. The IDS signal indicates to external devices that the INS8900 is performing a data input cycle. The signal should be used by memory or peripheral devices to gate data onto the INS8900 data bus lines.

EXTEND (Input): Extended Data Transfer. The EXTEND signal is used by slower memory or peripheral devices to temporarily increase the time duration of data input/output transfers. The EXTEND signal should be driven high at the beginning of an ODS or IDS signal and held high until output data has been captured or input data is made available to the data bus. The EXTEND signal can also be used to suspend input/output operations by applying the signal after the end of ODS or IDS.

JC13, JC14, JC15 (Input): Jump Conditions 13, 14, and 15. JC13, -14, and -15 are user-specified inputs that can be tested using the Branch-On-Condition (BOC) Instruction. If the jump condition input specified in the BOC Instruction is high, a program branch is effected. The JC13–JC15 signals are useful for testing status of external devices and receiving serial data.

F11, F12, F13, F14 (Output): General-purpose control flag outputs from the INS8900 Status and Control Flag Register. Individual flags may be set by the Set Flag Instruction (SFLG) and pulsed or reset by the Pulse Flag Instruction (PFLG). The F11–F14 signals may be used for direct control of system functions or serial data output.

NIR2, NIR3, NIR4, NIR5 (Input): Interrupt Requests 2, 3, 4, and 5. When these negative-true input signals are low for 1 clock period, minimum, the associated internal Interrupt Request Latch is set if the corresponding interrupt enable has been set by the user's program. The interrupt will be serviced after completion of the current instruction if the Master Interrupt Enable is set. Interrupt Requests are prioritized, with NIR5 having lowest priority.

NHALT (Input/Output): Halt. When the negative-true NHALT signal is driven low by external logic, it effects a microprocessor stall or Level-0 Interrupt, depending on timing of the CONTIN signal. When not controlled by external logic, NHALT is driven low by the INS8900 for 7/8 of a duty cycle while a programmed halt condition exists. Programmed halt is initiated by the Halt Instruction and terminated by pulsing the CONTIN line via external logic.

CONTIN (Input/Output): Continue. The CONTIN signal is used in the input mode to terminate a programmed halt, or to exercise microprocessor stall and Level-0 Interrupt, or as a jump-condition input that can be tested using a BOC instruction. In the output mode, CONTIN transmits an interrupt acknowledge pulse to acknowledge CPU response to an active interrupt input.

BPS (Input): Base Page Select. The BPS signal enables one of two base-page addressing schemes to be selected. When BPS is low, the first 256_{10} words of memory constitute base page (page zero). When BPS is high, the first 128_{10} memory words and the last 128_{10} memory words constitute base page.

NINIT (Input): Initialize. Initialize is applied after power supplies and clock are stable. While the negative-true NINIT signal is low, the INS8900 operation is suspended, and the IDS/ODS signals are set to the inactive state. After NINIT completes a low-to-high transition, the program counter is set to zero, the internal stack pointer is cleared, and all flags and interrupt enables are set low except Level-0 Interrupt Enable, which is set high. All other registers contain arbitrary values.

POWER SUPPLIES

V_{SS}: Ground.

V_{DD}: +12 volts.

V_{CC}: +5 volts.

V_{BB}: –8 volts.

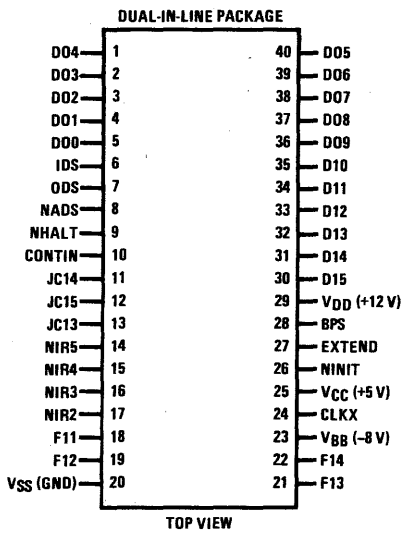


Figure 10. INS8900 Pin Assignment

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INTERRUPT SYSTEM

The INS8900 microprocessor provides a six-level, vectored, priority interrupt structure. This allows automatic identification of an interrupting device's level and allows all devices on an interrupt level to be enabled or disabled as a group, independent of other interrupt levels. An individual interrupt enable is provided in the status register for each level, as shown in figure 11, and a master interrupt enable (IEN) is provided for all 5 lower priority levels as a group. Negative true interrupt request inputs are provided to allow several interrupts to be wire ORed on each input. When an interrupt request occurs, it will set the interrupt request latch if the corresponding interrupt enable is true. The latch will be set by any pulse exceeding one clock period in duration, which is useful for capturing narrow timing or control pulses. If the master interrupt enable (IEN) is true, then an interrupt will be generated. During the interrupt sequence an address is provided by the output of the priority encoder and is used to access the pointer for the highest-priority interrupt request (IR0 is highest priority, IR5 is lowest priority). The pointers are stored in locations 2-7 (see table 1) for interrupt requests 1-5 and 0, respectively. The pointer specifies the starting address of the interrupt service routine for that particular interrupt level. Before executing the interrupt service routine, the program counter is pushed on the stack and IEN is set false. The interrupt service routine may set IEN true after turning off the interrupt enable for the level currently being serviced (or resetting the interrupt request). [The interrupt enables may be set and reset using the SFLG and PFLG instructions.]

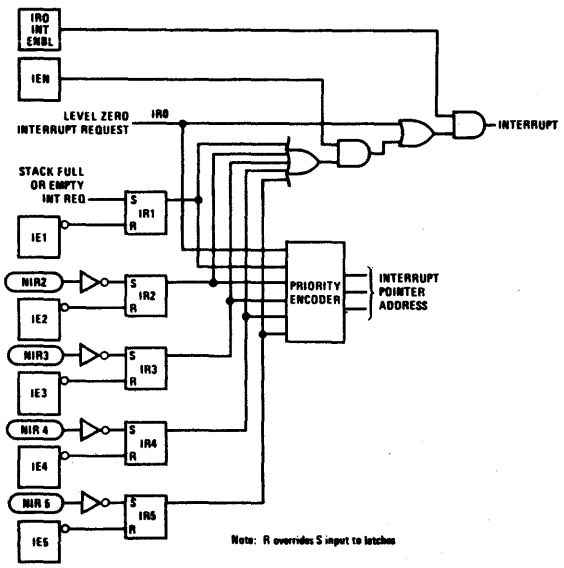


Figure 11. Interrupt System

Table 1. Interrupt Pointer Table

8	Int 0 Program
7	Int 0 PC Pointer
6	Int 5 Pointer
5	Int 4 Pointer
4	Int 3 Pointer
3	Int 2 Pointer
2	Int 1 Pointer
1	Not Assigned
Loc 0	Initialization Inst

The non-maskable level zero interrupt (IR0) is an exception to this interrupt procedure. It has a program counter storage location pointer (The program counter is not stored on the stack for this particular interrupt in order to preserve the processor state.) which is followed by the level zero interrupt service routine. The IR0 interrupt enable is cleared when a level zero interrupt occurs (IEN is unaffected) and may be set true by setting (non-existent) status flag 15. This allows execution of one more instruction (typically JMP@) to return from the IR0 interrupt routine before another interrupt will be acknowledged. This interrupt level is typically used by a control panel, which then can always interrupt the application program and does not affect system status.

Level zero interrupts are generated by exercising the NHALT and CONTIN lines as shown by the relative timing in figure 7. Note that the CONTIN Signal can be used as an interrupt acknowledge to indicate that the interrupt is being processed by the INS8900.

A processor stall may be implemented by driving the NHALT line low. Microprocessor operation is then suspended upon completion of the instruction presently under execution. The suspension may last indefinitely without loss of CPU status and may be terminated by use of the CONTIN Signal as shown by the relative timing in figure 8.

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DRIVERS AND RECEIVERS

Equivalent circuits for INS8900 drivers and receivers are shown in figure 12. All inputs have static charge protection circuits consisting of an RC filter and a voltage clamp. These devices should still be handled with care, as the protection circuits can be destroyed by excessive static charge. Pullup transistors on the jump condition inputs are turned on during one of the eight internal clock phases.

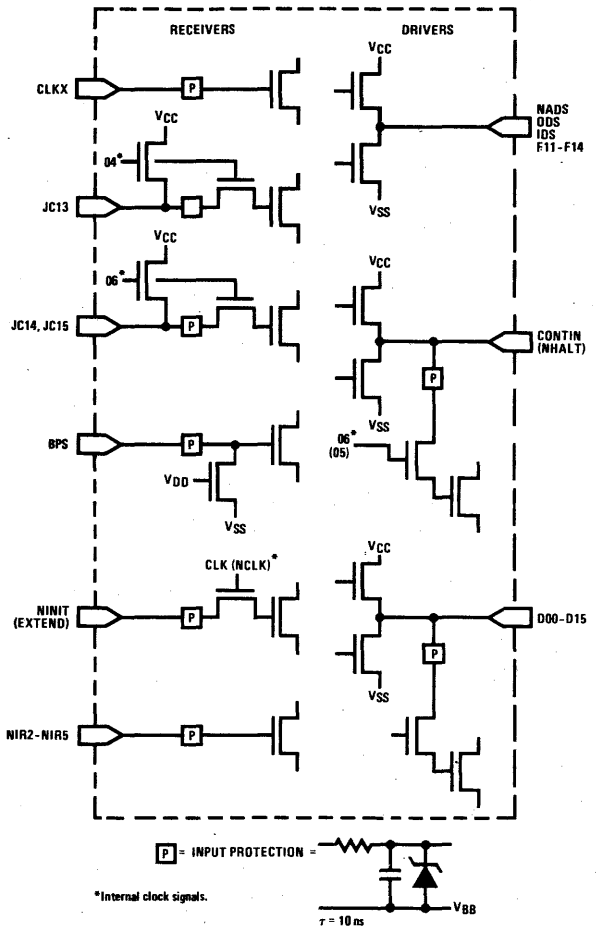


Figure 12. INS8900 Driver and Receiver Equivalent Circuits

EXTERNAL CLOCK TIMING

The INS8900 requires a single-phase clock as shown in figure 1. Refer to the electrical characteristics table for timing specifications.

INITIALIZATION

The INS8900 control circuitry may be initialized at any time by use of the NINIT input signal. The effects of the NINIT signal are described under "INS8900 Interface Signal Descriptions." The NINIT signal should always be used to initialize the processor after applying power. The minimum pulse width for NINIT is 8 clock periods (see figure 2). The INS8900 data strobes (NADS, ODS, IDS) are inactive for 16 to 24 clock periods after the trailing edge of the NINIT signal. After the 16 to 24 clock periods, the first NADS signal occurs and the first instruction is accessed from memory location zero.

Note: If the NINIT signal is held low while clock and/or power are first being applied, the NADS and NHALT outputs may have an undefined state for 8 clock periods after the trailing edge of NINIT.

DATA INPUT/OUTPUT OPERATIONS

All data transfers between the INS8900 and external memories or peripheral devices take place over the 16 data lines. These transfers are synchronized by the NADS, IDS, ODS, and EXTEND signals. Timing for address data output is shown in figure 3. Where signal timing is referenced to CLKX, the reference is to valid logic "1" or logic "0" clock levels. Cross-hatched areas indicate uncertainty of output transitions or "don't care" (optional) states for data inputs. Address data becomes valid one clock phase prior to the Address Data Strobe (NADS) and remains valid for one clock phase afterwards. Typically, NADS will be used to strobe the address data into a latch, either internal or external to the memory chips, or to clock decoded peripheral addresses into a flip-flop.

The INS8900 address output drivers assume a high-impedance state during the data input interval as shown in figure 3. The IDS signal may be used to disable output buffers and enable TRI-STATE® input buffers. Increased power supply current may occur during the transition period of the TRI-STATE enable signal, when several devices may be simultaneously enabled. Therefore, good power, ground layout, and bypass filtering practices should be observed. The data lines must be driven to valid input data logic levels by the end of IDS as specified by t_{DS}. TTL devices should actively drive the input to the right logic level. LS devices, for example, will drive the input to 2.7 V for a logic "1" level. Typically, this data input timing will allow operation of the microprocessor in a system at maximum speed if the access time of the system memory is less than 2 clock periods. For memories with longer access times, the clock frequency may be reduced or the I/O cycle extend feature may be used, as described below.

Data output timing is shown in figure 4. Output data becomes valid at the leading edge of ODS and remains valid for one clock period following the trailing edge. The Output Data Strobe is typically used as a read-write signal for memory and an output data latch strobe for peripheral interfaces.

For systems utilizing memories with access times greater than 2 clock periods it may be desirable to use the EXTEND input to lengthen the I/O cycle by multiples of the clock period. Timing for this is shown in figure 5. In the case of either input or output operations, the extend should be brought true prior to the end of clock phase 6. The timing shown in figure 5 will provide the minimum extend of one clock period. Holding EXTEND true for n additional clock periods will cause an extension of n+1 clock periods.

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In DMA or multiprocessor systems it may be desirable to prevent I/O operations by the INS8900 when the bus is in use by another device. This may be done immediately following an IDS or ODS signal (a data I/O operation) as shown in figure 6 or at any clock phase 6 regardless of whether a data I/O operation is in progress (as shown in figure 5).

INSTRUCTION SUMMARY

The instruction set is divided into eight instruction classes as listed in table 3. The branch instructions provide the means to transfer control anywhere in the 16-bit addressing space. Conditional branches are effected using the BOC instruction, which allows testing any one of 16 conditions, including status flags, the contents of AC0, and user inputs to the chip. Additional testing capability is provided by the skip instructions, which provide memory or peripheral to register comparisons without altering data. The memory data transfer instructions provide data transfers between the accumulators and memory or peripheral devices. The load with sign extended is provided to convert 8-bit twos complement data to 16-bit data, allowing 16-bit address modification when the 8-bit data length has been selected.

The memory data operate instructions provide operations between the principal working register (AC0) and memory or peripheral data. This includes both binary and BCD arithmetic instructions. The register data transfer instructions provide a very complete set of transfer possibilities between the accumulators, flag register, and stack, and include the capability to load immediate data. Register data operate instructions provide logical and arithmetic operations between any two accumulators. They may be used for address and data modification and to reduce the number of (time-consuming) memory references in a program. The shift and rotate instructions allow 8 different operations which are useful for multiply, divide, bit scanning, and serial input/output operations. The miscellaneous instructions include the capability to set or reset (pulse) any of the 16 bits of the status flag register individually.

The power of the instruction set is further enhanced by a flexible memory addressing scheme that provides three floating memory pages and one fixed page of 256 words each. Instructions which use both direct and indirect memory addressing are included in the instruction set. Three modes of direct memory addressing are available: base page, program counter relative, and index register relative. The direct addressing modes available are summarized in table 2. The mode of addressing is specified by the XR field of the instruction shown in the "Instruction Format" column of table 3.

Indirect addressing consists of first establishing an address in the same fashion as with direct addressing (by either the base page, relative to PC, or indexed [relative to AC2 or AC3] mode). The 16-bit contents of the memory location at this address is then used as the address of the operand, allowing any memory location to be addressed. The Branch Conditions of the INS8900 are listed in table 4 and the Status and Control Flags are listed in table 5.

Table 2. Direct Addressing Modes

XR Field	Addressing Mode	Effective Address
00	Base Page	EA = disp
01	Program Counter Relative	EA = disp + (PC)
10	AC2 Relative (indexed)	EA = disp + (AC2)
11	AC3 Relative (indexed)	EA = disp + (AC3)

Note 1: For base page addressing, disp is positive and in the range of 000 to 255 if BPS = 0, and is a signed number in the range of −128 to +127 if BPS = 1.

Note 2: For relative addressing, disp has a range of −128 to +127.

INS8900 BUFFERED SYSTEM

A block diagram of a fully buffered INS8900 system is illustrated in figure 13. Detailed schematics of the buffered INS8900 Microprocessor, Clock Generator, and Initialize Circuit are illustrated in figures 14, 15, and 16, respectively. The circuits as shown constitute a fully operational CPU module that can be used as the basis for a variety of systems regardless of their application.

NOTE

A 2.0 MHz crystal (Part No. NS209, Package Type HC-6U) for use with the INS8900 may be obtained from:

Electro Dynamics
5625 Foxridge
Shawnee Mission, Kansas 66201
(913) 262-2500

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Table 3. INS8900 Instruction Summary

Mnemonic	Meaning	Operation	Maximum Execution Time (Note)	Instruction Format
1. Branch Instructions				
BOC	Branch On Condition (Table 4)	(PC) ← (PC) + disp if cc true	5M + E_R + 1M if branch	0 1 0 0 | cc | disp
JMP	Jump	(PC) ← EA	4M + E_R	0 0 0 1 1 0 | xr
JMP@	Jump Indirect	(PC) ← (EA)	4M + 2E_R	1 0 0 1 1 0 |
JSR	Jump To Subroutine	(STK) ← (PC), (PC) ← EA	5M + E_R	0 0 0 1 0 1 |
JSR@	Jump To Subroutine Indirect	(STK) ← (PC), (PC) ← (EA)	5M + 2E_R	1 0 0 1 0 1 |
RTS	Return from Subroutine	(PC) ← (STK) + disp	5M + E_R	1 0 0 0 0 0 0 0 |
RTI	Return from Interrupt	(PC) ← (STK) + disp, IEN = 1	6M + E_R	0 1 1 1 1 1 0 0 |
2. Skip Instructions				
SKNE	Skip if Not Equal	If (ACr) ≠ (EA), (PC) ← (PC) + 1	5M + 2E_R + 1M if skip	1 1 1 1 r | xr | disp
SKG	Skip if Greater	If (AC0) > (EA), (PC) ← (PC) + 1	7M + 2E_R + 1M if skip	1 0 0 1 1 1 |
SKAZ	Skip if And is Zero	If [(AC0) ∧ (EA)] = 0, (PC) ← (PC) + 1	5M + 2E_R + 1M if skip	1 0 1 1 1 0 |
ISZ	Increment and Skip if Zero	(EA) ← (EA) + 1, if (EA) = 0, (PC) ← (PC) + 1	7M + 2E_R + E_W + 1M if skip	1 0 0 0 1 1 |
DSZ	Decrement and Skip if Zero	(EA) ← (EA) − 1, if (EA) = 0, (PC) ← (PC) + 1	7M + 2E_R + E_W + 1M if skip	1 0 1 0 1 1 |
AISZ	Add Immediate, Skip if Zero	(ACr) ← (ACr) + disp, if (ACr) = 0, (PC) ← (PC) + 1	5M + E_R + 1M if skip	0 1 1 1 1 0 | r
3. Memory Data Transfer Instructions				
LD	Load	(ACr) ← (EA)	4M + 2E_R	1 1 0 0 r | xr | disp
LD@	Load Indirect	(AC0) ← ((EA))	5M + 3E_R	1 0 1 0 0 0 |
ST	Store	(EA) ← (ACr)	4M + E_R + E_W	1 1 0 1 r |
ST@	Store Indirect	((EA)) ← (AC0)	4M + 2E_R + E_W	1 0 1 1 0 0 |
LSEX	Load With Sign Extended	(AC0) ← (EA) bit 7 extended	4M + 2E_R	1 0 1 1 1 1 |
4. Memory Data Operate Instructions				
AND	And	(AC0) ← (AC0) ∧ (EA)	4M + 2E_R	1 0 1 0 1 0 | xr | disp
OR	Or	(AC0) ← (AC0) ∨ (EA)	4M + 2E_R	1 0 1 0 0 1 |
ADD	Add	(ACr) ← (ACr) + (EA), OV, CY	4M + 2E_R	1 1 1 0 r |
SUBB	Subtract with Borrow	(AC0) ← (AC0) + ~ (EA) + (CY), OV, CY	4M + 2E_R	1 0 0 1 0 0 |
DECA	Decimal Add	(AC0) ← (AC0) $+_{10}$ (EA) $+_{10}$ (CY), OV, CY	7M + 2E_R	1 0 0 0 1 0 |
5. Register Data Transfer Instructions				
LI	Load Immediate	(ACr) ← disp	4M + E_R	0 1 0 1 0 0 | r | disp
RCPY	Register Copy	(ACdr) ← (ACsr)	4M + E_R	0 1 0 1 1 1 | dr | sr | 000 000
RXCH	Register Exchange	(ACdr) ← (ACsr), (ACsr) ← (ACdr)	6M + E_R	0 1 1 0 1 1 | dr | sr
XCHRS	Exchange Register and Stack	(STK) ← (ACr), (ACr) ← (STK)	6M + E_R	0 0 0 1 1 1 | r | 0 0
CFR	Copy Flags Into Register	(ACr) ← (FR)	4M + E_R	0 0 0 0 0 1 |
CRF	Copy Register Into Flags	(FR) ← (ACr)	4M + E_R	0 0 0 0 1 0 |
PUSH	Push Register Onto Stack	(STK) ← (ACr)	4M + E_R	0 1 1 0 0 0 |
PULL	Pull Stack Into Register	(ACr) ← (STK)	4M + E_R	0 1 1 0 0 1 |
PUSHF	Push Flags Onto Stack	(STK) ← (FR)	4M + E_R	0 0 0 0 1 1 0 0 |
PULLF	Pull Stack Into Flags	(FR) ← (STK)	4M + E_R	0 0 0 1 0 0 0 0 |
6. Register Data Operate Instructions				
RADD	Register Add	(ACdr) ← (ACdr) + (ACsr), OV, CY	4M + E_R	0 1 1 0 1 0 | dr | sr | 000 000
RADC	Register Add With Carry	(ACdr) ← (ACdr) + (ACsr) + (CY), OV, CY	4M + E_R	0 1 1 1 0 1 |
RAND	Register And	(ACdr) ← (ACdr) ∧ (ACsr)	4M + E_R	0 1 0 1 0 1 |
RXOR	Register Exclusive OR	(ACdr) ← (ACdr) ⊻ (ACsr)	4M + E_R	0 1 0 1 1 0 |
CAI	Complement and Add Immediate	(ACr) ← ~ (ACr) + disp	5M + E_R	0 1 1 1 0 0 | r | disp
7. Shift And Rotate Instructions				
SHL	Shift Left	(ACr) ← (ACr) shifted left n places, w/wo link	(5 + 3n) M + E_R, n = 1 – 127; 6M + E_R, n = 0	0 0 1 0 1 0 | r | n | ℓ
SHR	Shift Right	(ACr) ← (ACr) shifted right n places, w/wo link		0 0 1 0 1 1 |
ROL	Rotate Left	(ACr) ← (ACr) rotated left n places, w/wo link		0 0 1 0 0 0 |
ROR	Rotate Right	(ACr) ← (ACr) rotated right n places, w/wo link		0 0 1 0 0 1 |
8. Miscellaneous Instructions				
HALT	Halt	Halt		0 0 0 0 0 0 0 0 0 | 0000000
SFLG	Set Flag (Table 5)	(FR)$_{fc}$ ← 1	5M + E_R	0 0 1 1 | fc | 1
PFLG	Pulse Flag (Table 5)	(FR)$_{fc}$ ← 1, (FR)$_{fc}$ ← 0	6M + E_R	0 0 1 1 | fc | 0
NOP	No Operation	(PC) ← (PC) + 1	4M + E_R	0 1 0 1 1 1 0 0 0 |

Note: M = Machine cycle time = 4 clock periods
n = number of shifts
E_R = Extend time for read cycle
E_W = Extend time for write cycle
External interrupt response time is 7M + E_R plus time to finish current instruction.

Table 4. Branch Conditions

Number	Mnemonic	Condition
0	STFL	Stack full
1	REQ0	(AC0) equal to zero(1)
2	PSIGN	(AC0) has positive sign(2)
3	BIT 0	Bit 0 of AC0 true
4	BIT 1	Bit 1 of AC0 true
5	NREQ0	(AC0) is non-zero(1)
6	BIT 2	Bit 2 AC0 is true
7	CONTIN	CONTIN (continue) input is true
8	LINK	LINK is true
9	IEN	IEN is true
10	CARRY	CARRY is true
11	NSIGN	(AC0) has negative sign(2)
12	OVF	OVF is true
13	JC13	JC13 input is true
14	JC14	JC14 input is true
15	JC15	JC15 input is true

Note 1: If the selected data length is 8 bits, only bits 0-7 of AC0 are tested.
Note 2: Bit 7 is the sign bit (instead of bit 15) if the selected data length is 8 bits.

Table 5. Status and Control Flags

Register Bit	Flag Name	Function
0	"1"	Not used—always logic 1
1	IE1	Interrupt Enable Level 1
2	IE2	Interrupt Enable Level 2
3	IE3	Interrupt Enable Level 3
4	IE4	Interrupt Enable Level 4
5	IE5	Interrupt Enable Level 5
6	OVF	Overflow
7	CRY	Carry
8	LINK	Link
9	IEN	Master Interrupt Enable
10	BYTE	8-bit data length
11	F11	Flag 11
12	F12	Flag 12
13	F13	Flag 13
14	F14	Flag 14
15	"1"	Always logic 1, set for Interrupt 0 exit

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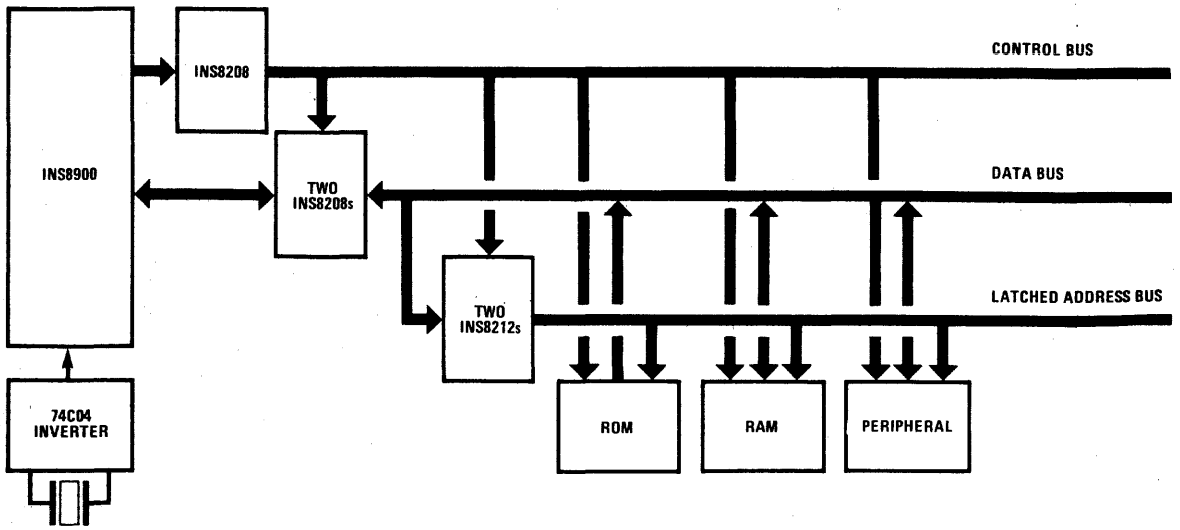


Figure 13. Fully Buffered INS8900 System

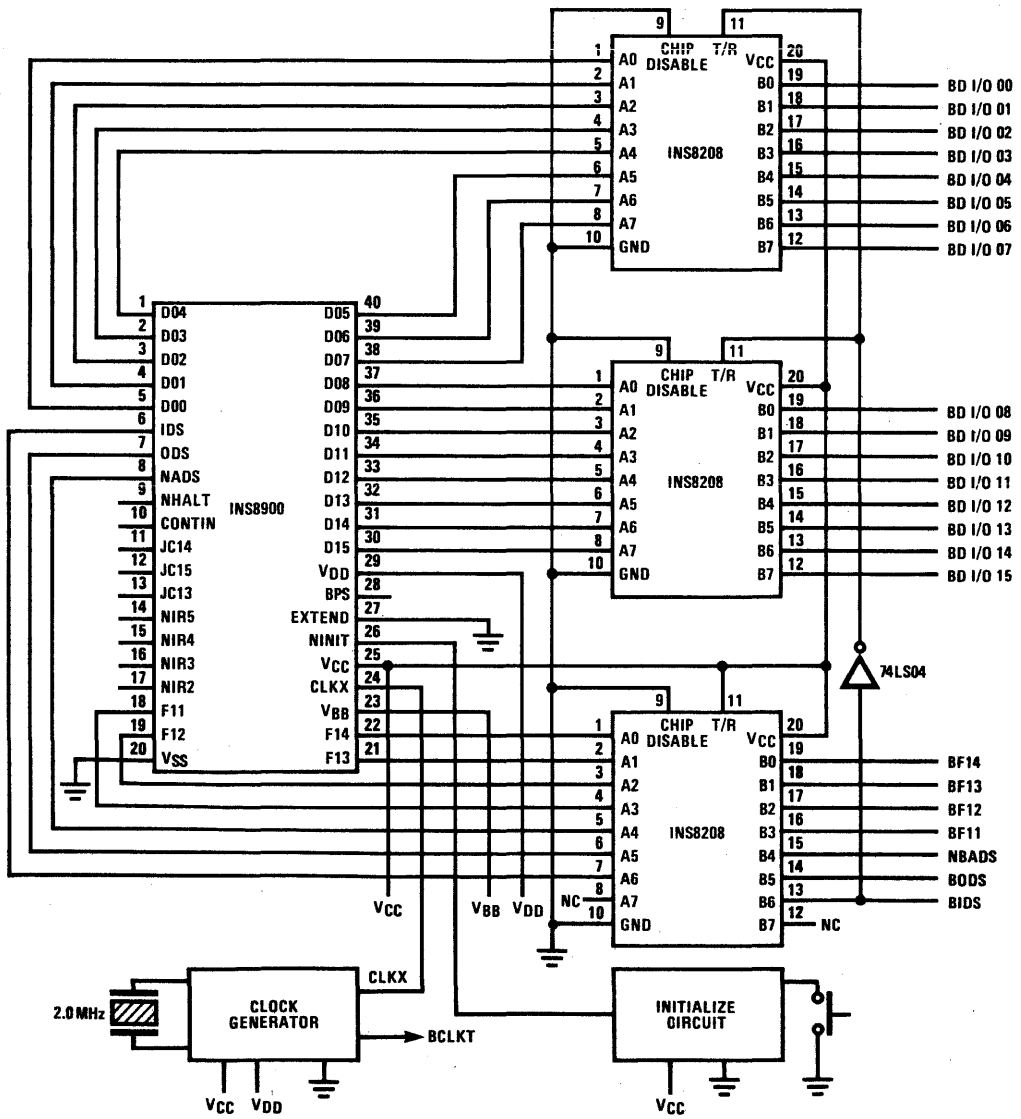


Figure 14. Fully Buffered INS8900 CPU Module

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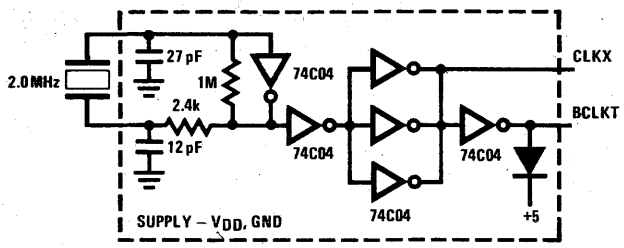


Figure 15. Clock Generator

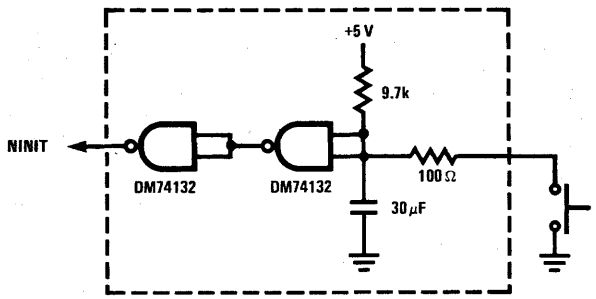
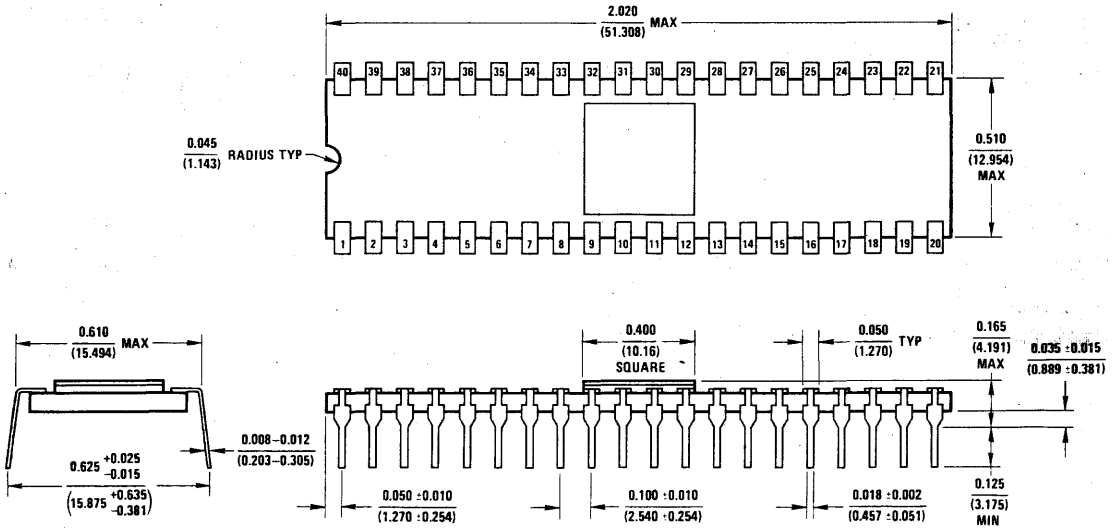


Figure 16. Initialize Circuit

Physical Dimensions

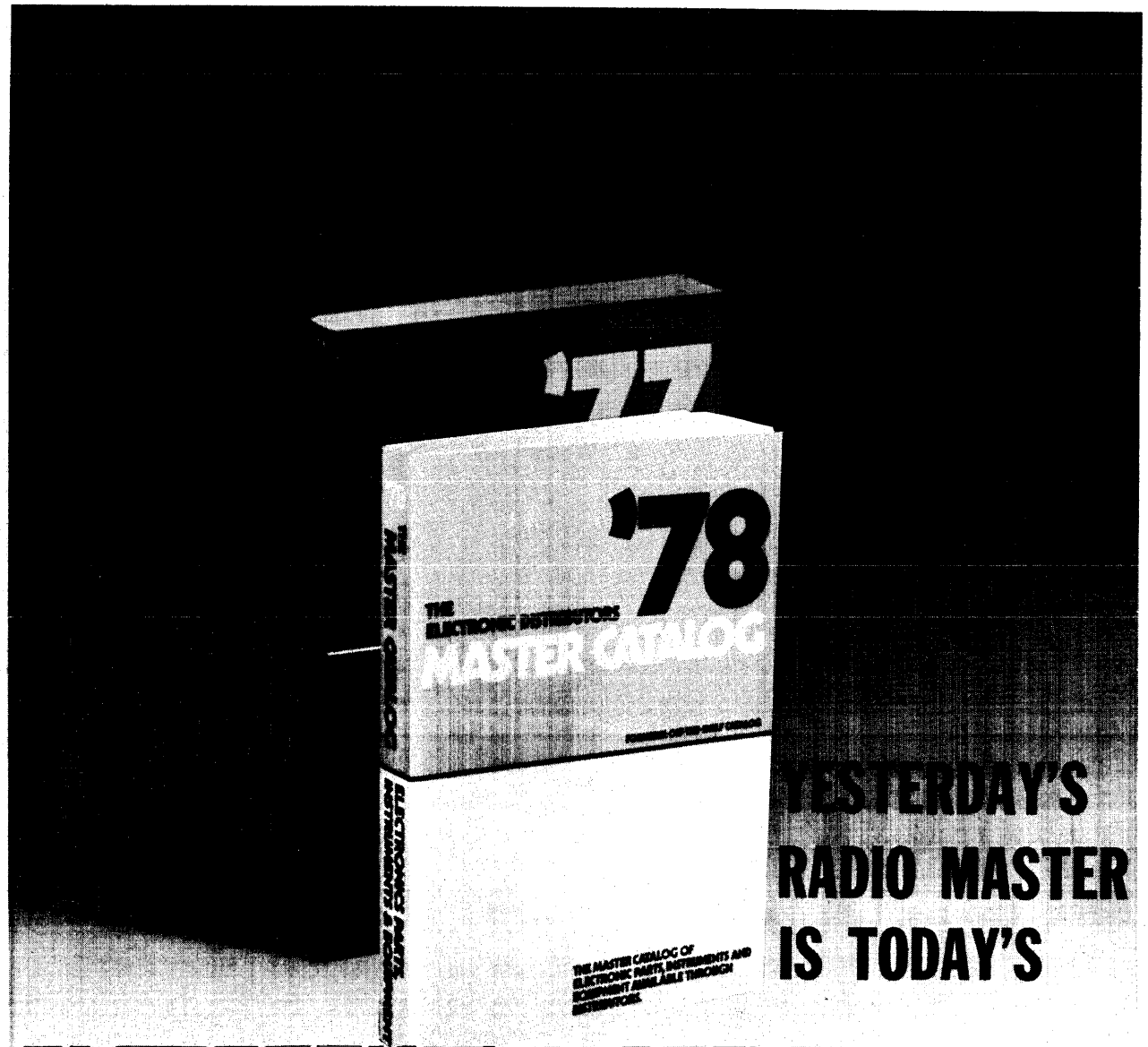


Cavity Dual-In-Line Package (D)
Order Number INS8900D
NS Package D40D

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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ELECTRONIC DISTRIBUTORS MASTER CATALOG

First published to serve you in 1935, The Radio Electronic Master has continuously changed over the years to better meet your needs. Today The Radio Master has become The Electronic Distributors MASTER CATALOG.

The 1978 edition of The Electronic Distributors MASTER CATALOG includes components, systems and subsystems sold through distributors.

It encompasses the following product areas: electronic and electromechanical components, audio and communications equipment, subassembly and panel components, hardware, production equipment and tools, test instrumentation, power sources, wire and cable, and chemicals.

The MASTER CATALOG is divided into four basic sections:

The **GENERAL INDEX** lists manufacturers and products alphabetically, including product cross references. Page numbers are displayed for both manufacturers and products. Manufacturers names are **bold-faced.**

The **MANUFACTURERS' CATALOG SECTION** is a collection of their respective product pages, alphabetically by manufacturer, again including addresses and phone numbers.

The **MANUFACTURERS DIRECTORY** is an alphabetical listing of all manufacturers whose products information is shown. Page numbers are referenced. Sales offices, representatives and distributors are included for many manufacturers.

The **DEALER/DISTRIBUTOR DIRECTORY** geographically lists distribution outlets by state and city. The listings were supplied by manufacturers cataloging in this edition.

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INTRODUCING THE μCOM-4 FAMILY — A LINE OF SINGLE CHIP 4-BIT MICROCOMPUTERS

In order to provide the power of microcomputers to the cost sensitive consumer/controller markets, NEC Microcomputers, Inc. offers a family of low cost, powerful 4-bit parallel single chip microcomputers. All of these devices contain on-chip read-only-memory (ROM) for program storage, data storage memory (RAM) and extensive input/output capability.

The family is divided into two applications areas. The μCOM-42 microcomputer's architecture and instruction set is designed to facilitate its use in Electronic Cash Register (ECR)/Scale products. The μCOM-43/44/45 microcomputers are designed for general purpose controller applications and are ideal devices for industrial controls, appliance controls, games, etc.

Both families are supported by NEC's high volume production capability, evaluation chips and evaluation kits, PDA-80 software development system and extensive documentation.

μCOM-42

DESCRIPTION

The μCOM-42 (Part No. μPD548C) is a single chip microcomputer that is ideally suited for Electronic Cash Register (ECR), Point of Sale (POS) and Electronic Scale applications.

Containing a 4-bit Parallel ALU, ROM for program storage and RAM for data storage, the μCOM-42 provides an economical and simple solution to many Vending/Calculating requirements.

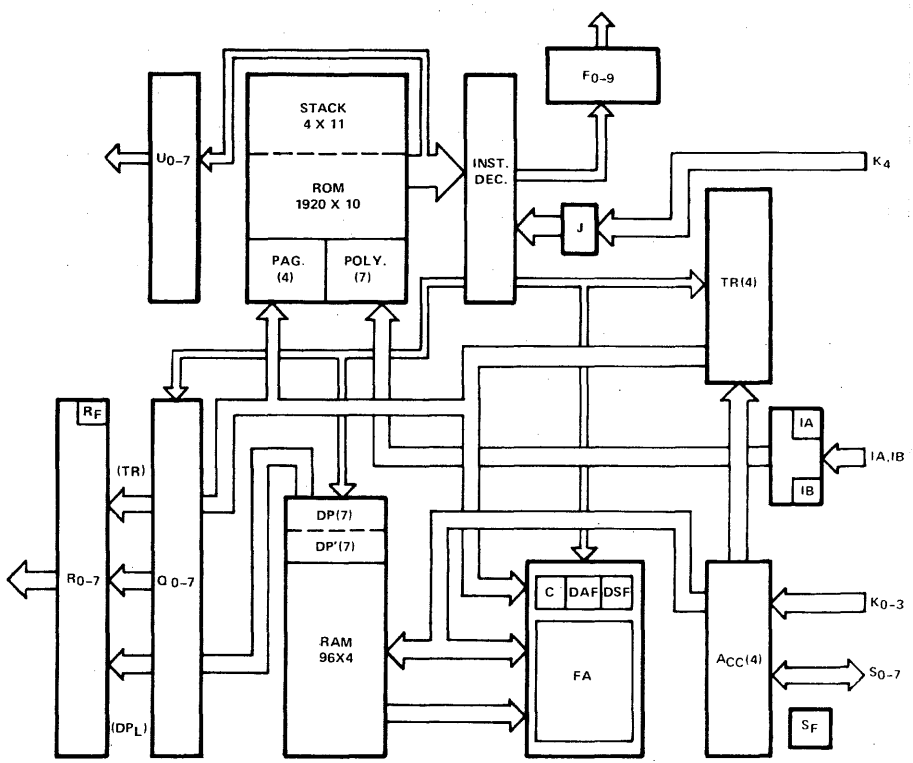
Because of its extensive instruction set and five input/output ports, the μCOM-42 is capable of controlling an 8 x 4 keyboard, an 8 digit display and low cost ECR-type printers.

Finally, the on-chip RAM space can be augmented by an external μPD5101 CMOS RAM (256 x 4 bits) for applications requiring low power data retention.

FEATURES

- Stand alone 4-bit microcomputer
- All 72 instructions are single byte
- 10 μsec instruction cycle
- 1920 x 10-bit program memory (ROM)
- 96 x 4-bit data memory (RAM)
- 4-level stack
- 2 interrupt request lines
- I/O compatible with TTL
- 10 discrete output ports ($F_0 - F_9$)
- Two 8-bit output ports ($U_0 - U_7$, $R_0 - R_7$)
- One 4-bit input port ($K_0 - K_3$)
- One 4-bit input/output port ($S_0 - S_3$)
- One single bit testable input port (K_4)
- Single phase TTL level clock (200 KHz max)
- Single supply, -10V PMOS technology
- 42 pin plastic dual-in-line package

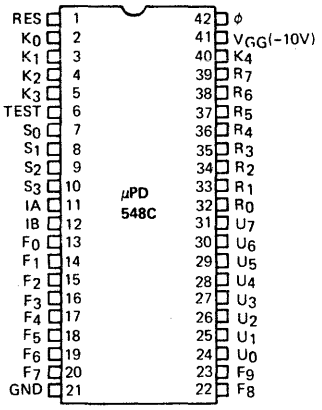
BLOCK DIAGRAM



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PIN NAMES

RES	Reset
K_0–K_3	Input Port K
TEST	Input for Testing (Normally V_{GG})
S_0–S_3	Input/Output Port S
IA, IB	Interrupt Input Ports
F_0–F_9	Output Port F
U_0–U_7	Output Port U
R_0–R_7	Output Port R
K_4	Input Port for Condition Test
ϕ	Clock Input



μCOM-42 PIN CONFIGURATION

μCOM-42 INSTRUCTION SET

①	②	③	④
CMA	1	$A_{CC} \leftarrow (\overline{A_{CC}})$	
CIA	1	$A_{CC} \leftarrow (\overline{A_{CC}})+1$	
INA	1/2	$A_{CC} \leftarrow (A_{CC})+1$	Carry=1
DEA	1/2	$A_{CC} \leftarrow (A_{CC})-1$	Borrow≠1
RFC	1	C←0	
SFC	1	C←1	
DSM	1	Decimal Subtract Mode	
DAM	1	Decimal Add Mode	
AD	1/2	$A_{CC} \leftarrow (A_{CC})+[DP]$	Carry=1
ADC	1	$A_{CC},C \leftarrow (A_{CC})+[DP]+(C)$	
ADI	1/2	$A_{CC} \leftarrow (A_{CC})+I_3I_2I_1I_0$	Carry=1
LM	1	$A_{CC} \leftarrow [DP]$ $DP_H \leftarrow (DP_H) \forall M_2M_1M_0$	
XM	1	$(A_{CC}) \leftrightarrow [DP]$ $DP_H \leftarrow (DP_H) \forall M_2M_1M_0$	
XMI	1/2	$(A_{CC}) \leftrightarrow [DP]$ $DP_H \leftarrow (DP_H) \forall M_2M_1M_0$ $DP_L \leftarrow (DP_L)+1$	$(DP_L)=8$ or $(DP_L)=0$
XMD	1/2	$(A_{CC}) \leftrightarrow [DP]$ $DP_H \leftarrow (DP_H) \forall M_2M_1M_0$ $DP_L \leftarrow (DP_L)-1$	$(DP_L)=F$ or $(DP_L)=7$
LI	1	$A_{CC} \leftarrow I_3I_2I_1I_0$	
LDI	1	$DP \leftarrow I_6$–I_0	
IND	1/2	$DP_L \leftarrow (DP_L)+1$	$(DP_L)=8$ or $(DP_L)=0$
DED	1/2	$DP_L \leftarrow (DP_L)-1$	$(DP_L)=F$ or $(DP_L)=7$
XDP	1	$(DP) \leftrightarrow (DP')$	
ZAG	1	$000DP_L \leftarrow (DP)$	

①	②	③	④
XTA	1	$(A_{CC}) \leftrightarrow (TR)$	
LTI	1	$TR \leftarrow I_3I_2I_1I_0$	
QS1	1	$Q_{n+1} \leftarrow Q_n, Q_0 \leftarrow 1$	
QS0	1	$Q_{n+1} \leftarrow Q_n, Q_0 \leftarrow 0$	
SB	1	$[DP,B_1,B_0] \leftarrow 1$	
RB	1	$[DP,B_1,B_0] \leftarrow 0$	
SBT	1/2	Skip if $[DP,B_1,B_0]=1$	$B_1B_0=1$
SC	1/2	Skip if (C)=1	(C)=1
SEM	1/2	Skip if $(A_{CC})=[DP]$	$(A_{CC})=[DP]$
SEI	1/2	Skip if $(A_{CC})=I_3I_2I_1I_0$	$(A_{CC})=I_3I_2I_1I_0$
SK4	1/2	Skip if $K_4=1$	$K_4=1$
JPT	1	$PC \leftarrow (TR), P_{6-0}$	
JPA	1	$PC_{6-4} \leftarrow P_{6-4}$ $PC_{3-0} \leftarrow P_{3-0} \vee (A_{CC})$	
JCP	1	$PC_{6-0} \leftarrow P_{6-0}$	
CAL	1	$[STACK] \leftarrow (PC)$ $PC \leftarrow 1000P_6P_5P_4P_3P_2P_1P_0$	
RT	1	$PC \leftarrow [STACK]$	
RTS	2	$PC \leftarrow [STACK]$ $PC \leftarrow (PC)+1$	
EIA	1	Enable IA port	
DIA	1	Disable IA port	
EIB	1	Enable IB port	
DIB	1	Disable IB port	
OIU	1	$U_{7-0} \leftarrow I_{7-0}$ $R_{7-0} \leftarrow (Q_{7-0})$	
ERO	1	Enable R port	
DRO	1	Disable R port	

①	②	③
OQR	1	$R \leftarrow (Q)$
OTR	1	$R_{7-4} \leftarrow (TR), R_{3-0} \leftarrow (DP_L)$
SFS	1	$S \leftarrow (A_{CC})$
RFS	1	S port Input Mode
IS	1	$A_{CC} \leftarrow S$
IK	1	$A_{CC} \leftarrow K$
RF1	1	$F_1 \leftarrow 0$
SF1	1	$F_1 \leftarrow 1$
RF2	1	$F_2 \leftarrow 0$
SF2	1	$F_2 \leftarrow 1$
RF3	1	$F_3 \leftarrow 0$
SF3	1	$F_3 \leftarrow 1$
RF4	1	$F_4 \leftarrow 0$
SF4	1	$F_4 \leftarrow 1$
RF5	1	$F_5 \leftarrow 0$
SF5	1	$F_5 \leftarrow 1$
RF6	1	$F_6 \leftarrow 0$
SF6	1	$F_6 \leftarrow 1$
RF7	1	$F_7 \leftarrow 0$
SF7	1	$F_7 \leftarrow 1$
RF8	1	$F_8 \leftarrow 0$
SF8	1	$F_8 \leftarrow 1$
RF9	1	$F_9 \leftarrow 0$
SF9	1	$F_9 \leftarrow 1$
RF0	1	$F_0 \leftarrow 0$
SF0	1	$F_0 \leftarrow 1$
NOP	1	No Operation

Notes: ① MNEMONIC
② CYCLES
③ DESCRIPTION
④ CONDITION FOR SKIP

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μCOM-43

DESCRIPTION

The μCOM-43 (Part No. μPD546C) is a 4-bit parallel microcomputer that is especially suited for a wide range of low cost, sophisticated controller applications.

The μPD546C contains all the functional blocks necessary to enable its use for both industrial and non-industrial controller applications. These blocks include: a 4-bit parallel ALU; 2K by 8-bit ROM for program storage; 96 x 4-bit RAM for data storage; 35 input/output lines; a programmable interval timer; interrupt capability; and on-board clock generator.

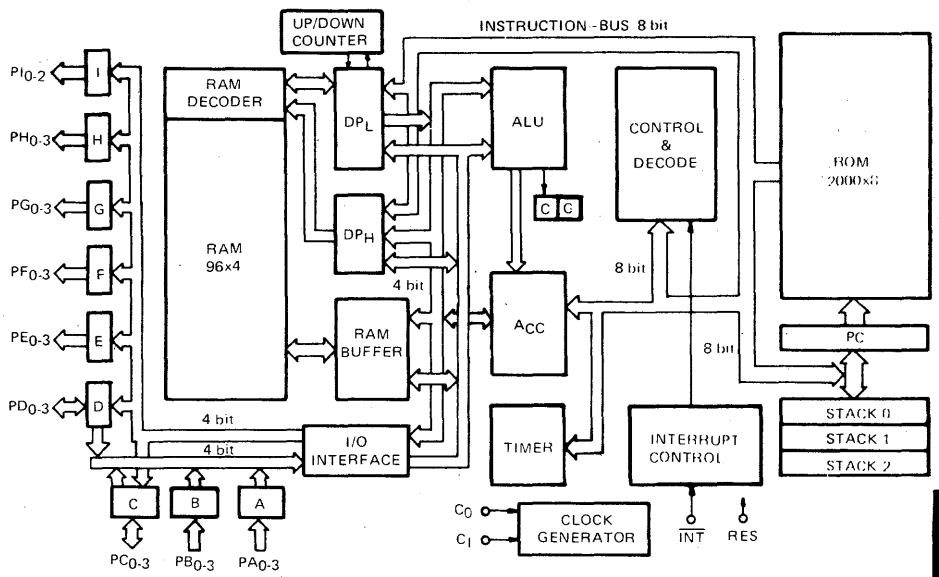
The 80 instructions of the μCOM-43 are designed to perform controller oriented functions and for efficient use of the program memory space. These 80 instructions include a number of multi-function instructions, powerful I/O instructions including single bit manipulation, and test-and-skip instructions for conditional processing.

Thus, the μCOM-43's large ROM memory, extensive I/O, and other hardware features in combination with its powerful instruction set opens up new areas for inexpensive yet sophisticated controllers.

FEATURES

- Stand alone 4-bit microcomputer for control applications
- 80 powerful instructions capable of: binary addition; decimal addition and subtraction; and logical operations
- 10 μsec instruction cycle
- 2000 x 8-bit program memory (ROM)
- 96 x 4-bit data memory (RAM)
- 35 input/output lines consisting of: two 4-bit input ports, two 4-bit input/output ports, four 4-bit output ports, one 3-bit output port. All capable of both single bit manipulation and 4-bit parallel processing
- 3-level stack
- Six 4-bit working registers
- Hardware interrupt including enable/disable capability
- On-chip programmable interval timer
- On-chip clock generator
- Open drain, TTL compatible outputs
- Single supply, -10V PMOS technology
- 42 pin plastic dual-in-line package

BLOCK DIAGRAM



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μCOM-44

DESCRIPTION

The μCOM-44 (Part No. μPD547C) is a 4-bit parallel microcomputer that is ideally suited for a wide range of low cost, general purpose controller applications.

The μPD546C contains all the functional blocks needed for a low cost, stand alone, high volume controller. These blocks include: a 4-bit parallel ALU; 1K by 8-bit ROM for program storage; 64 by 4-bit RAM for data storage; 35 input/output lines; interrupt capability and an on-board clock generator.

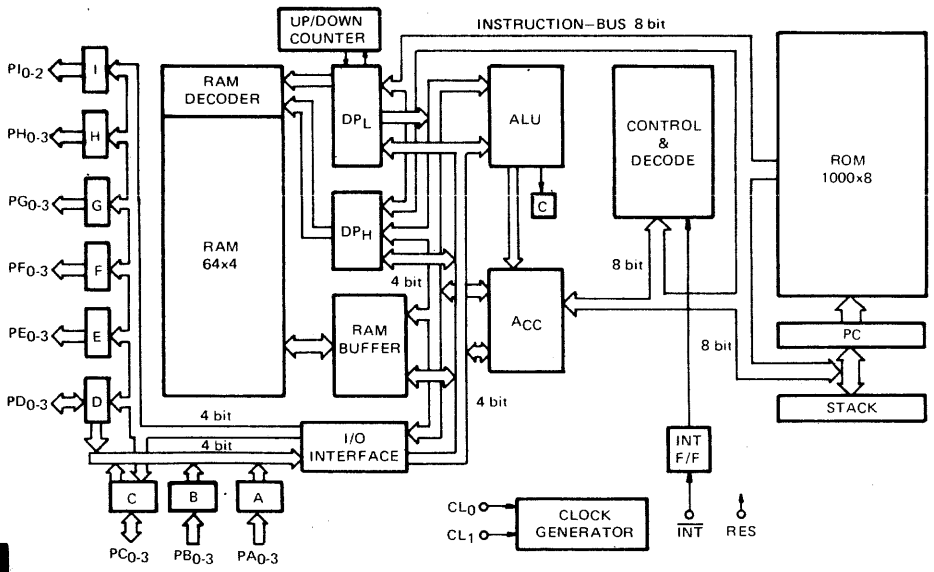
The 58 instructions of the μCOM-44 are designed to perform controller oriented functions and for efficient use of the program memory space. These 58 instructions include a number of multifunctional instructions, powerful I/O instructions including single bit manipulation, and test-and-skip instructions for conditional processing.

The μCOM-44 is ideally suited for consumer/industrial controller functions because of its extensive I/O, on-board ROM/RAM space and its powerful instruction set.

FEATURES

- Stand alone 4-bit microcomputer for control applications
- 58 powerful instructions capable of: binary addition; decimal addition and subtraction; and logical operations
- 10 μsec instruction cycle
- 1000 x 8-bit program memory (ROM)
- 64 x 4-bit data memory (RAM)
- 35 Input/Output lines consisting of: two 4-bit input ports; two 4-bit input/output ports; four 4-bit output ports, one 3-bit output port. All capable of both single bit manipulation and 4-bit parallel processing.
- Single level stack
- On-chip clock generator
- Open drain, TTL compatible outputs
- Single supply, -10V PMOS technology
- 42 pin plastic dual-in-line package

BLOCK DIAGRAM



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μCOM-45

DESCRIPTION

The μCOM-45 (Part No. μPD550C) is a single chip microcomputer designed for extremely low cost, general purpose controller/consumer/appliance applications.

The μPD550C contains all the system blocks necessary to build an inexpensive, yet fully functional controller. The blocks include: a 4-bit parallel ALU; 640 by 8-bit ROM for program storage; 32 by 4-bit RAM for data storage; 21 input/output lines; interrupt capability and an on-board clock generator.

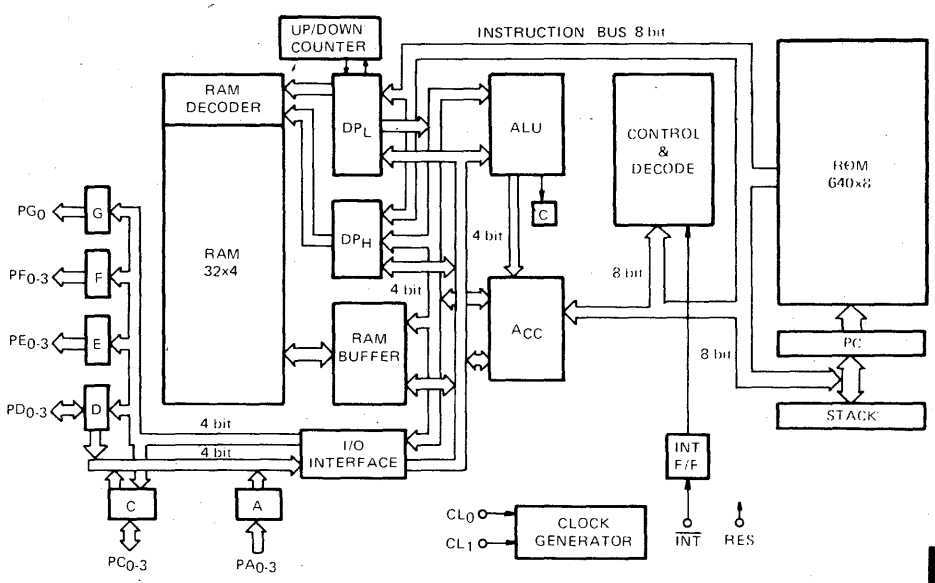
The 58 instructions of the μCOM-45 are designed to perform controller oriented functions and for efficient use of the program memory space. These 58 instructions include a number of multifunctional instructions, powerful I/O instructions including single bit manipulation, and test-and-skip instructions for conditional processing.

The μCOM-45 opens up entire new areas of controller applications because of its extremely low cost and powerful functions.

FEATURES

- Stand alone 4-bit microcomputer for consumer/control applications
- 58 powerful instructions capable of: binary addition; decimal addition and subtraction; and logical operations
- 10 μsec instruction cycle
- 640 x 8-bit program memory (ROM)
- 32 x 4-bit data memory (RAM)
- 21 Input/Output lines consisting of: one 4-bit input port; two 4-bit input/output ports; two 4-bit output ports; one 1-bit output port. All capable of both single bit manipulation and 4-bit parallel processing.
- Single level stack
- On-chip clock generator
- Open drain, TTL compatible outputs capable of -35V
- Single Supply, -10V PMOS technology
- 28 pin plastic dual-in-line package

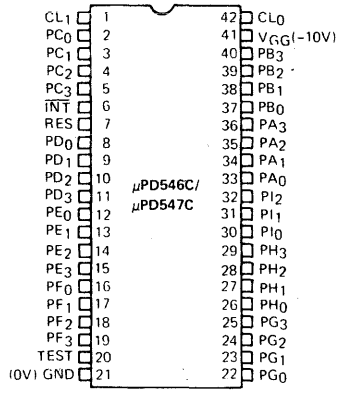
BLOCK DIAGRAM



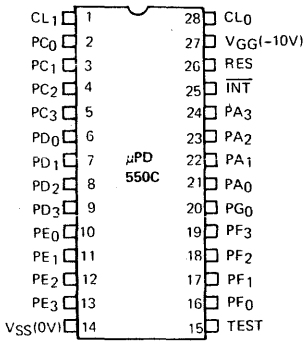
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PIN NAMES

CL_0–CL_1	External Clock Source
PC_0–PC_3	Input/Output Port C
$\overline{INT}$	Interrupt Input
RES	Reset
PD_0–PD_3	Input/Output Port D
PE_0–PE_3	Output Port E
PF_0–PF_3	Output Port F
TEST	Input for Testing (Normally GND)
PG_0–PG_3	Output Port G
PH_0–PH_3	Output Port H
PI_0–PI_3	Output Port I
PA_0–PA_3	Input Port A
PB_0–PB_3	Input Port B



μCOM-43/44/45 PIN CONFIGURATIONS



PIN NAMES

CL_0–CL_1	External Clock Source
PC_0–PC_3	Input/Output Port C
PD_0–PD_3	Input/Output Port D
PE_0–PE_3	Output Port E
PF_0–PF_3	Output Port F
PG_0	Output Port G
PA_0–PA_3	Input Port A
$\overline{INT}$	Interrupt Input
RES	Reset

μCOM-43/44/45 INSTRUCTION SETS

①	②	③	④	⑤
CLA	1	1	A_{CC} ← 0	
CMA	1	1	A_{CC} ← $(\overline{A_{CC}})$	
CIA	1	1	A_{CC} ← $(\overline{A_{CC}})+1$	
INC	1	1/2·3	A_{CC} ← $(A_{CC})+1$ skip if Carry	Carry
DEC	1	1/2·3	A_{CC} ← $(A_{CC})-1$ skip if Borrow	Borrow
CLC	1	1	C ← 0	
STC	1	1	C ← 1	
XC	1	1	(C) ↔ (C')	
RAR	1	1	$(A_{CCn-1}) \rightarrow (A_{CCn})$ C ← (A_{CC0}), $(A_{CC3}) \rightarrow$ (C)	
INM	1	1/2·3	[(DP)] ← [(DP)]+1 skip if [(DP)]=0	[(DP)]=0
DEM	1	1/2·3	[(DP)] ← [(DP)]−1 skip if [(DP)]=F	[(DP)]=F
AD	1	1/2·3	A_{CC} ← $(A_{CC})+[(DP)]$ skip if Carry	Carry
ADS	1	1/2·3	A_{CC},C ← $(A_{CC})+[(DP)]+(C)$ skip if Carry	Carry
ADC	1	1	A_{CC},C ← $(A_{CC})+[(DP)]+(C)$	
DAA	1	1	A_{CC} ← $(A_{CC})+6$	
DAS	1	1	A_{CC} ← $(A_{CC})+10$	
EXL	1	1	A_{CC} ← $(A_{CC}) \vee [(DP)]$	
LI	1	1	A_{CC} ← $I_3I_2I_1I_0$	
S	1	1	[(DP)] ← (A_{CC})	
L	1	1	A_{CC} ← [(DP)]	
LM	1	1	A_{CC} ← [(DP)] DP_H ← $(DP_H) \vee 0M_1M_0$	
X	1	1	$(A_{CC}) \leftrightarrow [(DP)]$	
XM	1	1	$(A_{CC}) \leftrightarrow [(DP)]$ DP_H ← $(DP_H) \vee 0M_1M_0$	
XD	1	1/2·3	$(A_{CC}) \leftrightarrow [(DP)]$ DP_L ← $(DP_L)-1$ skip if (DP_L)=F	(DP_L)=F
XMD	1	1/2·3	$(A_{CC}) \leftrightarrow [(DP)]$ DP_H ← $(DP_H) \vee 0M_1M_0$ DP_L ← $(DP_L)-1$ skip if (DP_L)=F	(DP_L)=F

①	②	③	④	⑤
XI	1	1/2·3	$(A_{CC}) \leftrightarrow [(DP)]$ $DP_L \leftarrow (DP_L)+1$ skip if (DP_L)=0	(DP_L)=0
XMI	1	1/2·3	$(A_{CC}) \leftrightarrow [(DP)]$ DP_H ← $(DP_H) \vee 0M_1M_0$ $DP_L \leftarrow (DP_L)+1$ skip if (DP_L)=0	(DP_L)=0
LDI	2	2	DP ← I_6–I_0	
LDZ	1	1	DP_H ← 0 DP_L ← $I_3I_2I_1I_0$	
DED	1	1/2·3	$DP_L \leftarrow (DP_L)-1$ skip if (DP_L)=F	(DP_L)=F
IND	1	1/2·3	$DP_L \leftarrow (DP_L)+1$ skip if (DP_L)=0	(DP_L)=0
TAL	1	1	$DP_L \leftarrow (A_{CC})$	
TLA	1	1	$A_{CC} \leftarrow (DP_L)$	
XHX	1	2	$(X) \leftrightarrow (DP_H)$	
XLY	1	2	$(Y) \leftrightarrow (DP_L)$	
THX	1	2	X ← (DP_H)	
TLY	1	2	Y ← (DP_L)	
XAZ	1	2	$(Z) \leftrightarrow (A_{CC})$	
XAW	1	2	$(W) \leftrightarrow (A_{CC})$	
TAZ	1	2	Z ← (A_{CC})	
TAW	1	2	W ← (A_{CC})	
XHR	1	2	$(R) \leftrightarrow (DP_H)$	
XLS	1	2	$(S) \leftrightarrow (DP_L)$	
SMB	1	1	[(DP,B_1B_0)] ← 1	
RMB	1	1	[(DP,B_1B_0)] ← 0	
TMB	1	1/2·3	skip if [(DP,B_1B_0)]=1	[(DP,B_1B_0)]=1
TAB	1	1/2·3	skip if $(A_{CC}(B_1B_0))$=1	$(A_{CC}(B_1B_0))$=1
CMB	1	1/2·3	skip if $(A_{CC}(B_1B_0))$ = [(DP,B_1B_0)]	$(A_{CC}(B_1B_0))$ = [(DP,B_1B_0)]
SFB	1	2	FLAG (B_1B_0) ← 1	
RFB	1	2	FLAG (B_1B_0) ← 0	
FBT	1	2/3·4	skip if (FLAG (B_1B_0))=1	(FLAG(B_1B_0))=1
FBF	1	2/3·4	skip if (FLAG (B_1B_0))=0	(FLAG(B_1B_0))=0
CM	1	1/2·3	skip if (A_{CC}) ≠ [(DP)]	(A_{CC}) ≠ [(DP)]
CI	2	2/3·4	skip if $(A_{CC}) \neq I_3I_2I_1I_0$	$(A_{CC}) \neq I_3I_2I_1I_0$
CLI	2	2/3·4	skip if $(DP_L) \neq I_3I_2I_1I_0$	$(DP_L) \neq I_3I_2I_1I_0$

①	②	③	④	⑤
TC	1	1/2·3	skip if (C)=1	(C)=1
TIT	1	1/2·3	skip if (INT F/F)=1 INT F/F ← 0	(INT F/F) 1
JCP	1	1	$PC_{5-0} \leftarrow P_5$–P_0	
JMP	2	2	$PC \leftarrow P_{10}$–P_0	
JPA	1	2	$PC_{5-0} \leftarrow A_3A_2A_1A_000$	
EI	1	1	INTE F F ← 1	
DI	1	1	INTE F F ← 0	
CZP	1	1	STACK ← (PC) PC ← 00000$P_3P_2P_1P_000$	
CAL	2	2	STACK ← (PC) PC ← P_{10}–P_0	
RT	1	2	PC ← (STACK)	
RTS	1	3–4	PC ← (STACK) PC ← (PC)+1,2	Unconditional
STM	2	2	TM F F ← 0 TIMER ← I_5–I_0	
TTM	1	1/2·3	skip if (TM F/F)=1	(TM F/F) 1
SEB	1	2	PORT E (B_1B_0) ← 1	
REB	1	1	PORT E (B_1B_0) ← 0	
SPB	1	1	PORT (DP_L,B_1B_0) ← 1	
RPB	1	1	PORT (DP_L,B_1B_0) ← 0	
TPA	1	2/3·4	skip if (PORT A (B_1B_0)) = 1	(PORT A (B_1B_0)) 1
TPB	1	1/2·3	skip if (PORT (DL_L,B_1B_0)) =1	(PORT (DP_L, B_1B_0)) 1
OE	1	2	PORT E ← (A_{CC})	
OP	1	1	PORT (DP_L) ← (A_{CC})	
OCD	2	2	PORT C,D ← I_7–I_0	
IA	2	2	A_{CC} ← (PORT A)	
IP	1	1	A_{CC} ← (PORT (DP_L))	
NOP	1	1	No Operation	

Notes: ① MNEMONIC
② BYTES
③ CYCLES
④ DESCRIPTION
⑤ CONDITION FOR SKIP
☐ These Instructions Apply Only to the μCOM-43.

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μCOM-4 FAMILY DEVELOPMENT TOOLS

The μCOM-4 microcomputer family is fully supported with all the necessary hardware and software development tools. These tools include assemblers, evaluation chips and evaluation kits.

For software development, cross-assemblers that run on our 8080A-based PDA-80 are available along with support documentation. The PDA-80 allows the user to program PROMs directly without having to use a paper tape medium.

For hardware and software development, evaluation kits and evaluation chips are available. The EVACHIPS (μPD555D for the μCOM-42 and μPD556D for the μCOM-43/44/45) have all the functional capabilities of their production equivalents, except they do not contain on-chip ROM. Instead they have the ability to address external memory. In addition, they give the designer the ability to single step through his program in order to ease debugging.

The evaluation kits (EVAKIT-42 and EVAKIT-43), using the appropriate EVACHIP, provide the designer with a single pc board containing: LED's for display of internal registers and instruction code; switches for setting breakpoints; on-board PROM sockets; and reset and single-step capability. The combination of EVAKIT and EVACHIP give the μCOM-4 system designer all the tools needed for initial design/debugging and prototype fabrication.

EVAKIT-42 μCOM-42 PROTOTYPING BOARD

DESCRIPTION

The EVAKIT-42 is a single board prototyping package for both hardware and software debugging of the μCOM-42 one-chip microcomputer system.

The heart of the EVAKIT-42 is the μPD555D evaluation chip which provides the same functionality as the μPD548C. Unlike the μCOM-42, the μPD555D does not contain a read only memory, but provides addressing capability to external memories instead.

The EVAKIT-42 also includes sockets for 2K bytes of EEPROM memory, LED displays to show register contents, switches for breakpoint and mode selection, and control logic for single step operation, all residing on a single printed circuit board.

FEATURES

- Single Step Execution
- Display of Instruction Code to be Executed
- Display of Contents of Program Counter
- BREAK Function at any Address
- Display of Contents of Accumulator and S Port
- Selection of Program Memory, On-Board PROM or External PROM

MAJOR SPECIFICATIONS

Product Name	EVAKIT-42
LSI's Used	CPU μPD555D PROM μPD454D (up to 16)
Clock Frequency	100 KHz to 200 KHz
Program Capacity	1920 Words (10 Bits/Word)
Operating Temperature	0°C to 45°C
Power Supplies	+7V ± 5% 0.6A (Max) −5V ± 5% 1.0A (Max) −10V ± 5% 0.2A (Max)
Dimension	240 mm x 310 mm
Connector	100-Pin Double-Sided PC Edge Connector with 0.125 inch (3.175 mm) Contact Center

EVAKIT-43 μCOM-43/44/45 PROTOTYPING BOARD

DESCRIPTION

The EVAKIT-43 is a single board prototyping package for both hardware and software debugging of the μCOM-43/44/45 one-chip microcomputer systems.

The heart of the EVAKIT-43 is the μPD556D evaluation chip which provides the same functionality as the μCOM-43 (μPD546D). This includes full I/O capability, on-chip timer and clock generator. Unlike the μPD546, which contains on-chip ROM, the μPD556 provides addressing capability to external memory instead.

The EVAKIT-43 also includes: sockets for 2K bytes of EEPROM (in either 256 or 1K byte increments); LED displays to show the contents of the program counter, accumulator, data pointer and instruction register; switches for breakpoint and mode selection; and control logic for single step operation.

FEATURES

- Single Step Execution
- Internal Register Display
- BREAK Function at any Address
- Selection of Program Memory, On-Board PROM or External PROM

MAJOR SPECIFICATIONS

Product Name	EVAKIT-43
LSI's Used	CPU μPD556D PROM μPD454D or μPD458D
Clock Frequency	100 KHz to 200 KHz
Program Capacity	2K Bytes
Operating Temperature	0°C to 45°C
Power Supplies	+5V ± 5% 0.8A (Max) −5V ± 5% 0.1A (Max)
Dimension	251 mm x 324 mm
Connector	100-Pin Double-Sided PC Edge Connector with 0.125 inch (3.175 mm) Contact Center

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EVACHIP-42

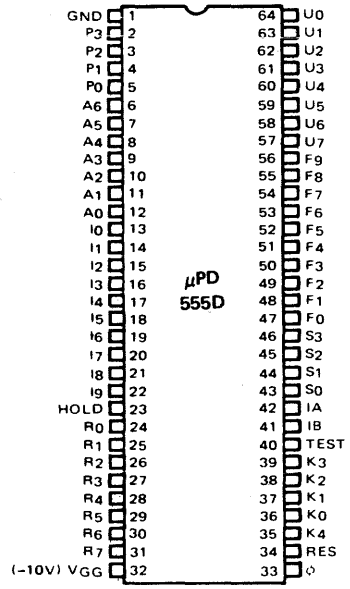
DESCRIPTION

The EVACHIP-42 (Part No. μPD555D) is an evaluation chip for the μCOM-42 single chip microcomputer. Designed to be used for both hardware and software debugging, the EVACHIP-42 is functionally equivalent to the μCOM-42, except that it does not contain on-chip ROM. Instead, it is able to address external memory and also has HOLD capability to enable single step operation of the program being evaluated.

FEATURES

- 4-Bit Parallel Processor
- Full 72 Instruction Set of μCOM-42
- 10 μsec Instruction Cycle
- Capable of Addressing 1920 x 10-Bits of External Program Memory
- HOLD Capability
- Full Functionality of μCOM-42
- Single Supply, −10V PMOS Technology
- 64 Pin Ceramic Dual-in-Line Package

PIN CONFIGURATION



PIN NAMES

$P_0 - P_3$	Page Output
$A_0 - A_6$	Address Output
$I_0 - I_9$	Instruction Input
HOLD	HOLD Input
$R_0 - R_7$	Output Port R
φ	Clock Input
RES	Reset Input
K4	K4 Test Input Line
$K_0 - K_3$	K Input Port
TEST	IC Test Input
IA, IB	Interrupt Input
$S_0 - S_3$	Input/Output Port S
$F_0 - F_9$	Output Port F
$U_0 - U_7$	Output Port U

EVACHIP-43

DESCRIPTION

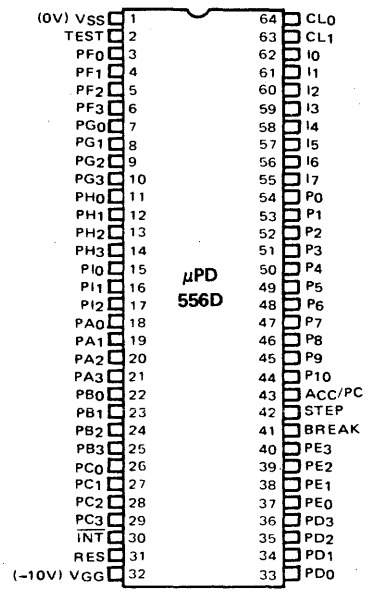
The EVACHIP-43 (Part No. μPD556D) is an evaluation chip for the μCOM-43/44/45 single chip microcomputers. Designed to be used for both hardware and software debugging, the EVACHIP-43 is functionally equivalent to the μCOM-43, except that it does not contain on-chip ROM. Instead, it is able to address external memory. In addition, in order to facilitate debugging, the μPD556 is capable of displaying the contents of the internal accumulator and data pointer and of being single stepped.

When the μPD556 is being used to evaluate μCOM-44/45 designs, the external memory capacity should be restricted to that of the respective on-chip ROM and the instructions used should be restricted to the 58 comprising the μCOM-44/45 instruction set.

FEATURES

- 4-bit Parallel Processor
- Full 80 Instruction Set of μCOM-43
- 10 μsec Instruction Cycle
- Capable of Addressing 2K x 8-Bits of External Program Memory
- Single Step Capability
- Full Functionality of μCOM-43
- Single Supply, −10V PMOS Technology
- 64 Pin Ceramic Dual-in-Line Package

PIN CONFIGURATION



PIN NAMES

$PF_0 - PF_3$	Output Port F
$PG_0 - PG_3$	Output Port G
$PH_0 - PH_3$	Output Port H
$PI_0 - PI_2$	Output Port I
$PA_0 - PA_3$	Input Port A
$PB_0 - PB_3$	Input Port B
$PC_0 - PC_3$	Input/Output Port C
$\overline{INT}$	Interrupt Input
RES	Reset
$PD_0 - PD_3$	Input/Output Port D
$PE_0 - PE_3$	Output Port E
BREAK	Hold Input
STEP	Single Step Input
A_{CC}/PC	Display A_{CC}/PC Input
$P_0 - P_{10}$	PC Output
$I_0 - I_7$	Instruction Input
$CL_0 - CL_1$	External Clock Source

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PDA-80 PROGRAM DEVELOPMENT AID

DESCRIPTION

The PDA-80 is a self-contained microcomputer development system providing unique features for rapid development of μCOM-4 Family software. A full software package is provided for program generation. This package includes: a resident MONITOR for program loading and system control; an EDITOR program for generating and modifying source language programs; ASSEMBLER programs for converting source programs to object programs and for generating symbol tables and program listings for documentation and debugging; and DIAGNOSTIC programs for testing the proper operation of the PDA-80 itself.

The PDA-80 shortens the design cycle, thus cutting your product development costs and getting your product on the market fast. One of its features providing shortened design time is the integral EEPROM PROGRAMMER. This allows the prototype designer to quickly reprogram and debug his hardware without the need for time-wasting UV erasure. (NEC's EEPROMs are available in 1K by 8 (μPD458) or 256 by 8 (μPD454) configurations with typical erase time of 60 sec and program time of 30 ms per byte).

Finally, the PDA-80 is available with a full line of peripherals to further speed program generation and software debugging. These include hard copy consoles of either 30 or 120 cps and the choice of either a floppy disk system or a high speed paper tape reader/punch. And it is also a full-blown 8080A hardware/software development system!

FEATURES

- Integral EEPROM Programmer
- 8080A Based
- TTY or RS-232C Compatible
- Up to 56K of RAM
- Self Diagnostic Programs
- Full Line of High Speed Peripherals Available
- Cross Assemblers for all μCOM-4 Family Processors

SPECIFICATION

Cabinet	15 x 17 x 8 inches (37 x 44 x 20 cm)
Power	100/117 Vac 60 Hz
Operating Temperature	0 to +55°C
Humidity Range	0 to 90%
Weight	45 pounds (20.5 Kg)

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μPD8080AF 8-BIT N-CHANNEL MICROPROCESSOR FAMILY

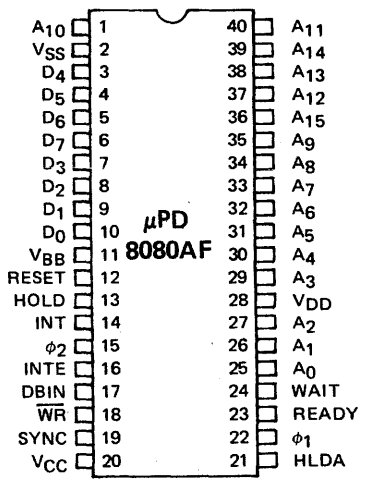
DESCRIPTION

The μPD8080AF is a complete 8-bit parallel processor for use in general purpose digital computer systems. It is fabricated on a single LSI chip using N-channel silicon gate MOS process, which offers much higher performance than conventional microprocessors (1.28 μs minimum instruction cycle). A complete microcomputer system is formed when the μPD8080AF is interfaced with I/O ports (up to 256 input and 256 output ports) and any type or speed of semiconductor memory. It is available in a 40 pin ceramic or plastic package.

FEATURES

- 78 Powerful Instructions
- Three Devices – Three Clock Frequencies
  μPD8080AF – 2.0 MHz
  μPD8080AF-2 – 2.5 MHz
  μPD8080AF-1 – 3.0 MHz
- Direct Access to 64K Bytes of Memory with 16-Bit Program Counter
- 256 8-Bit Input Ports and 256 8-Bit Output Ports
- Double Length Operations Including Addition
- Automatic Stack Memory Operation with 16-Bit Stack Pointer
- TTL Compatible (Except Clocks)
- Multi-byte Interrupt Capability
- **Fully** Compatible with Industry Standard 8080A
- Available in either Plastic or Ceramic Package

PIN CONFIGURATION



Rev/1

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FUNCTIONAL DESCRIPTION

The μPD8080AF contains six 8-bit data registers, an 8-bit accumulator, four testable flag bits, and an 8-bit parallel binary arithmetic unit. The μPD8080AF also provides decimal arithmetic capability and it includes 16-bit arithmetic and immediate operators which greatly simplify memory address calculations, and high speed arithmetic operations.

The μPD8080AF utilizes a 16-bit address bus to directly address 64K bytes of memory, is fully TTL compatible (1.9 mA), and utilizes the following addressing modes: Direct; Register; Register Indirect; and Immediate.

The μPD8080AF has a stack architecture wherein any portion of the external memory can be used as a last in/first out (LIFO) stack to store/retrieve the contents of the accumulator, the flags, or any of the data registers.

The μPD8080AF also contains a 16-bit stack pointer to control the addressing of this external stack. One of the major advantages of the stack is that multiple level interrupts can easily be handled since complete system status can be saved when an interrupt occurs and then restored after the interrupt is complete. Another major advantage is that almost unlimited subroutine nesting is possible.

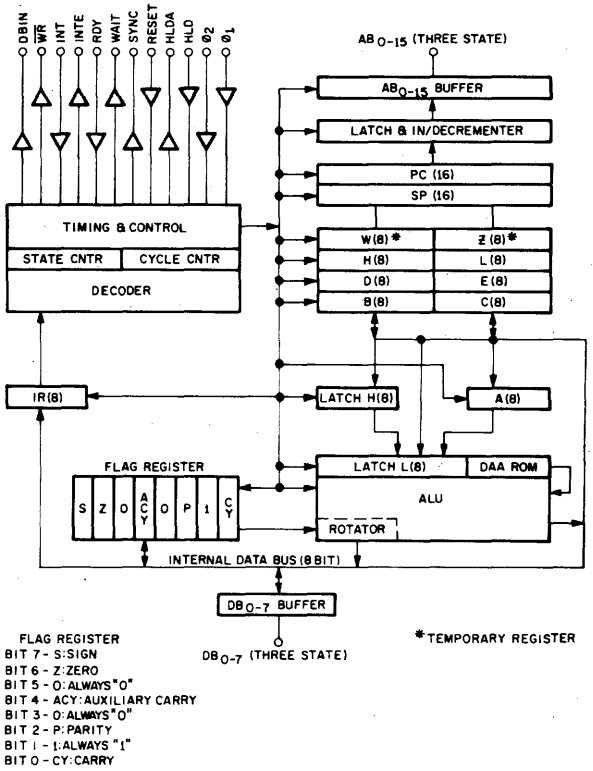
This processor is designed to greatly simplify system design. Separate 16-line address and 8-line bidirectional data busses are employed to allow direct interface to memories and I/O ports. Control signals, requiring no decoding, are provided directly by the processor. All busses, including the control bus, are TTL compatible.

Communication on both the address lines and the data lines can be interlocked by using the HOLD input. When the Hold Acknowledge (HLDA) signal is issued by the processor, its operation is suspended and the address and data lines are forced to be in the FLOATING state. This permits other devices, such as direct memory access channels (DMA), to be connected to the address and data busses.

The μPD8080AF has the capability to accept a multiple byte instruction upon an interrupt. This means that a CALL instruction can be inserted so that any address in the memory can be the starting location for an interrupt program. This allows the assignment of a separate location for each interrupt operation, and as a result no polling is required to determine which operation is to be performed.

NEC offers three versions of the μPD8080AF. These processors have all the features of the μPD8080AF except the clock frequency ranges from 2.0 MHz to 3.0 MHz. These units meet the performance requirements of a variety of systems while maintaining software and hardware compatibility with other 8080A devices.

BLOCK DIAGRAM



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PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1, 25-27, 29-40	$A_{15} - A_0$	Address Bus (output three-state)	The address bus is used to address memory (up to 64K 8-bit words) or specify the I/O device number (up to 256 input and 256 output devices). A_0 is the least significant bit.
2	V_{SS}	Ground (input)	Ground
3-10	$D_7 - D_0$	Data Bus (input/ output three-state)	The bidirectional data bus communicates between the processor, memory, and I/O devices for instructions and data transfers. During each sync time, the data bus contains a status word that describes the current machine cycle. D_0 is the least significant bit.
11	V_{BB}	V_{BB} Supply Voltage (input)	-5V ± 5%
12	RESET	Reset (input)	If the RESET signal is activated, the program counter is cleared. After RESET, the program starts at location 0 in memory. The INTE and HLDA flip-flops are also reset. The flags, accumulator, stack pointer, and registers are not cleared. (Note: External synchronization is not required for the RESET input signal which must be active for a minimum of 3 clock periods.)
13	HOLD	Hold (input)	HOLD requests the processor to enter the HOLD state. The HOLD state allows an external device to gain control of the μPD8080AF address and data buses as soon as the μPD8080AF has completed its use of these buses for the current machine cycle. It is recognized under the following conditions: • The processor is in the HALT state. • The processor is in the T_2 or T_W stage and the READY signal is active. As a result of entering the HOLD state, the ADDRESS BUS ($A_{15} - A_0$) and DATA BUS ($D_7 - D_0$) are in their high impedance state. The processor indicates its state on the HOLD ACKNOWLEDGE (HLDA) pin.
14	INT	Interrupt Request (input)	The μPD8080AF recognizes an interrupt request on this line at the end of the current instruction or while halted. If the μPD8080AF is in the HOLD state, or if the Interrupt Enable flip-flop is reset, it will not honor the request.
15	ϕ_2	Phase Two (input)	Phase two of processor clock.
16	INTE (1)	Interrupt Enable (output)	INTE indicates the content of the internal interrupt enable flip-flop. This flip-flop is set by the Enable (EI) or reset by the Disable (DI) interrupt instructions and inhibits interrupts from being accepted by the processor when it is reset. INTE is automatically reset (disabling further interrupts) during T_1 of the instruction fetch cycle (M_1) when an interrupt is accepted and is also reset by the RESET signal.
17	DBIN	Data Bus In (output)	DBIN indicates that the data bus is in the input mode. This signal is used to enable the gating of data onto the μPD8080AF data bus from memory or input ports.
18	$\overline{WR}$	Write (output)	$\overline{WR}$ is used for memory WRITE or I/O output control. The data on the data bus is valid while the $\overline{WR}$ signal is active ($\overline{WR}$ = 0).
19	SYNC	Synchronizing Signal (output)	The SYNC signal indicates the beginning of each machine cycle.
20	V_{CC}	V_{CC} Supply Voltage (input)	+5V ± 5%
21	HLDA	Hold Acknowledge (output)	HLDA is in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at: • T_3 for READ memory or input operations. • The clock period following T_3 for WRITE memory or OUTPUT operations. In either case, the HLDA appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2.
22	ϕ_1	Phase One (input)	Phase one of processor clock.
23	READY	Ready (input)	The READY signal indicates to the μPD8080AF that valid memory or input data is available on the μPD8080AF data bus. READY is used to synchronize the processor with slower memory or I/O devices. If after sending an address out, the μPD8080AF does not receive a high on the READY pin, the μPD8080AF enters a WAIT state for as long as the READY pin is low. (READY can also be used to single step the processor.)
24	WAIT	Wait (output)	The WAIT signal indicates that the processor is in a WAIT state.
28	V_{DD}	V_{DD} Supply Voltage (input)	+12V ± 5%

Note: (1) After the EI instruction, the μPD8080AF accepts interrupts on the second instruction following the EI. This allows proper execution of the RET instruction if an interrupt operation is pending after the service routine.

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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to + 70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	− 40°C to + 125°C
All Output Voltages ①	−0.3 to +20 Volts
All Input Voltages ①	−0.3 to +20 Volts
Supply Voltages V_{CC}, V_{DD} and V_{SS} ①	−0.3 to +20 Volts
Power Dissipation	1.5W

Note: ① Relative to V_{BB}.

COMMENT; Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

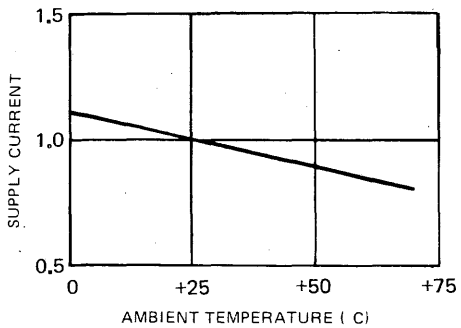
*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Input Low Voltage	V_{ILC}	V_{SS} − 1		V_{SS} + 0.8	V	
Clock Input High Voltage	V_{IHC}	9.0		V_{DD} + 1	V	
Input Low Voltage	V_{IL}	V_{SS} − 1		V_{SS} + 0.8	V	
Input High Voltage	V_{IH}	3.3		V_{CC} + 1	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.9 mA on all outputs
Output High Voltage	V_{OH}	3.7			V	I_{OH} = − 150 μA ②
Avg. Power Supply Current (V_{DD})	$I_{DD(AV)}$		40	70	mA	t_{CY} min
Avg. Power Supply Current (V_{CC})	$I_{CC(AV)}$		60	80	mA	t_{CY} min
Avg. Power Supply Current (V_{BB})	$I_{BB(AV)}$		0.01	1	mA	t_{CY} min
Input Leakage	I_{IL}			±10 ②	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Clock Leakage	I_{CL}			±10 ②	μA	$V_{SS} \leq V_{CLOCK} \leq V_{DD}$
Data Bus Leakage in Input Mode	I_{DL} ①			− 100 ②	μA	$V_{SS} \leq V_{IN} \leq V_{SS}$ + 0.8V
				−2 ②	mA	V_{SS} + 0.8V $\leq V_{IN} \leq V_{CC}$
Address and Data Bus Leakage During HOLD	I_{FL}			+10 ②	μA	$V_{ADDR/DATA} = V_{CC}$
				− 100 ②	μA	$V_{ADDR/DATA} = V_{SS}$ + 0.45V

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED ③



Notes: ① When DBIN is high and $V_{IN} > V_{IH}$ internal active pull-up resistors will be switched onto the data bus.
② Minus (−) designates current flow out of the device.
③ ΔI supply/ΔT_a = −0.45%/°C.

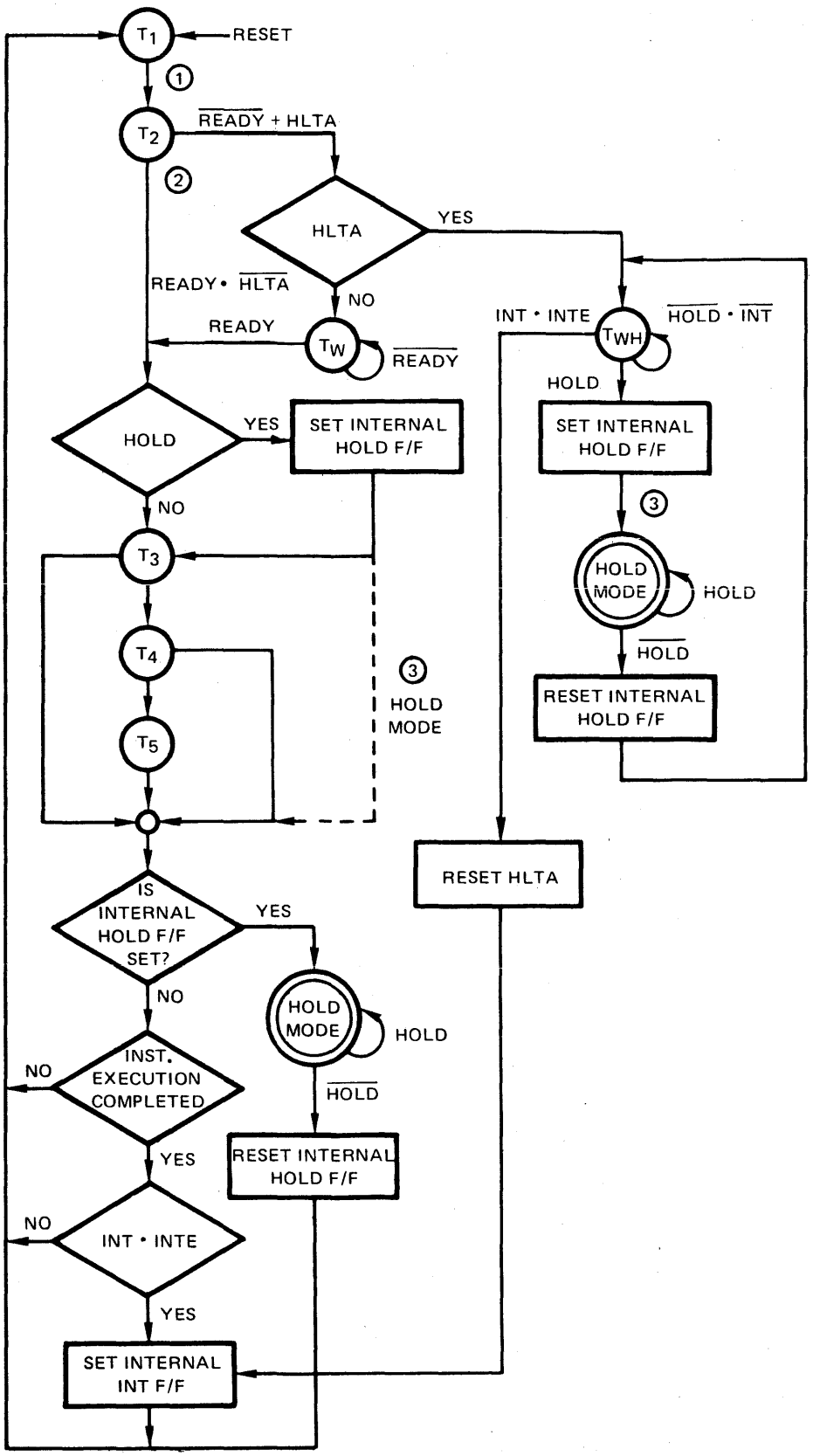
CAPACITANCE

T_a = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V, V_{BB} = −5V.

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Capacitance	C_ϕ		17	25	pF	f_c = 1 MHz
Input Capacitance	C_{IN}		6	10	pF	Unmeasured Pins
Output Capacitance	C_{OUT}		10	20	pF	Returned to V_{SS}

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PROCESSOR STATE TRANSITION DIAGRAM



Notes:
① INTE F/F IS RESET IF INTERNAL INT F/F IS SET.
② INTERNAL INT F/F IS RESET IF INTE F/F IS RESET.
③ IF REQUIRED, T_4 AND T_5 ARE COMPLETED SIMULTANEOUSLY WITH ENTERING HOLD STATE.

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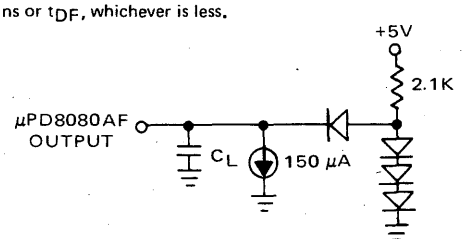
AC CHARACTERISTICS
μPD8080AF

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.48		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		50	nsec	
φ1 Pulse Width	$t_{\phi1}$	60			nsec	
φ2 Pulse Width	$t_{\phi2}$	220			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	70			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	80			nsec	
Address Output Delay From φ2	t_{DA} ②			200	nsec	C_L = 100 pF
Data Output Delay From φ2	t_{DD} ②			220	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			120	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		140	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	30			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	150			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	120			nsec	
HOLD Setup Time to φ2	t_{HS}	140			nsec	
INT Setup Time During φ2 (During φ1 in Halt Mode)	t_{IS}	120			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 100 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

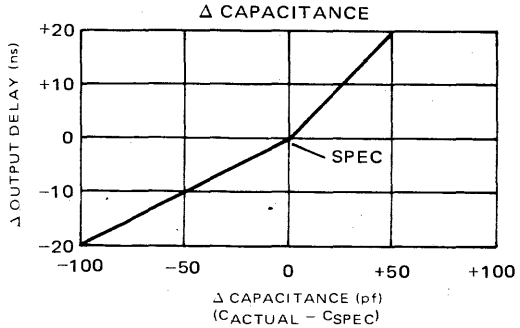
Notes: ① Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.

② Load Circuit.



③ Actual $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} > t_{CY}$ Min.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



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AC CHARACTERISTICS
μPD8080AF-2

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.38		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		50	nsec	
φ1 Pulse Width	$t_{\phi1}$	60			nsec	
φ2 Pulse Width	$t_{\phi2}$	175			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	70			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	70			nsec	
Address Output Delay From φ2	t_{DA} ②			175	nsec	C_L = 100 pF
Data Output Delay From φ2	t_{DD} ②			200	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			120	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		140	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	20			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	130			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	90			nsec	
HOLD Setup Time to φ2	t_{HS}	120			nsec	
INT Setup Time During φ2 (for all modes)	t_{IS}	100			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 100 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

Notes Continued:

④ The following are relevant when interfacing the μPD8080AF to devices having V_{IH} = 3.3V.

a. Maximum output rise time from 0.8V to 3.3V = 100 ns at C_L = SPEC.

b. Output delay when measured to 3.0V = SPEC +60 ns at C_L = SPEC.

c. If $C_L \neq$ SPEC, add 0.6 ns/pF if $C_L > C_{SPEC}$, subtract 0.3 ns/pF (from modified delay) if $C_L < C_{SPEC}$.

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AC CHARACTERISTICS
μPD8080AF-1

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.32		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		25	nsec	
φ1 Pulse Width	$t_{\phi1}$	50			nsec	
φ2 Pulse Width	$t_{\phi2}$	145			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	60			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	60			nsec	
Address Output Delay From φ2	t_{DA} ②			150	nsec	C_L = 50 pF
Data Output Delay From φ2	t_{DD} ②			180	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			110	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		130	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	10			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	120			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	90			nsec	
HOLD Setup Time to φ2	t_{HS}	120			nsec	
INT Setup Time During φ2 (for all modes)	t_{IS}	100			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 50 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

Notes Continued: ⑤

Device	t_{AW}
μPD8080AF	$2t_{CY} - t_{D3} - t_{r\phi2} - 140$
μPD8080AF-2	$2t_{CY} - t_{D3} - t_{r\phi2} - 130$
μPD8080AF-1	$2t_{CY} - t_{D3} - t_{r\phi2} - 110$

⑥

Device	t_{DW}
μPD8080AF	$t_{CY} - t_{D3} - t_{r\phi2} - 170$
μPD8080AF-2	$t_{CY} - t_{D3} - t_{r\phi2} - 170$
μPD8080AF-1	$t_{CY} - t_{D3} - t_{r\phi2} - 150$

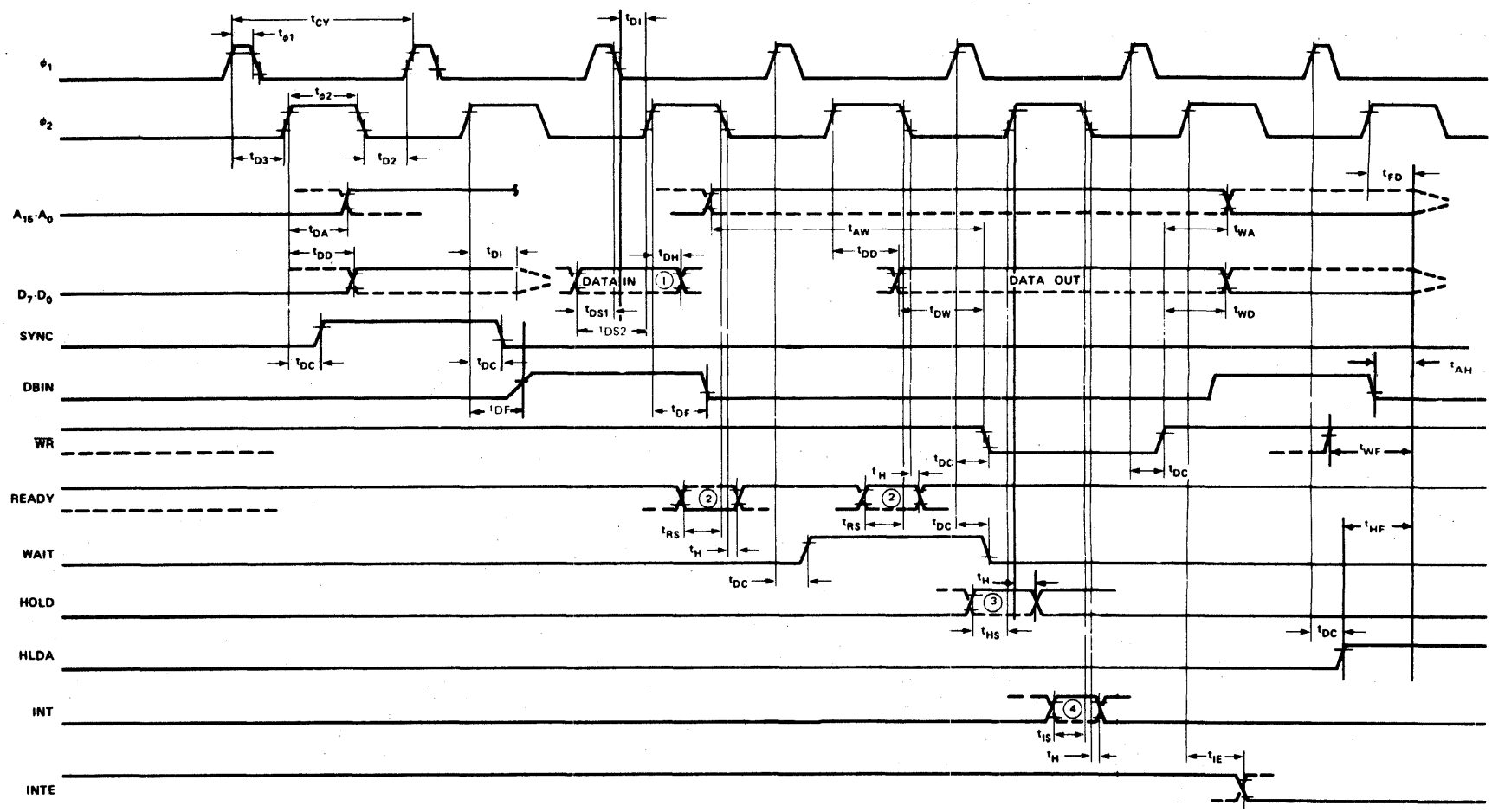
⑦ If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.

⑧ $t_{HF} = t_{D3} + t_{r\phi2} - 50$ ns.

⑨ $t_{WF} = t_{D3} + t_{r\phi2} - 10$ ns.

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TIMING WAVEFORMS ⑤ ⑥



Notes: ① Data in must be stable for this period during DBIN • T_3. Both t_{DS1} and t_{DS2} must be satisfied.

② Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)

③ Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)

④ Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized in the following instruction. (External synchronization is not required.)

⑤ This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

⑥ Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V, "0" = 1.0V; INPUTS "1" = 3.3V; "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.

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INSTRUCTION SET

The instruction set includes arithmetic and logical operators with direct, register, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, register, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with direct, conditional, or computed jumps. Also the ability to call and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Conditional jumps, calls and returns execute based on the state of the four testable flags (Sign, Zero, Parity and Carry). The state of each flag is determined by the result of the last instruction executed that affected flags. (See Instruction Set Table.)

The Sign flag is set (High) if bit 7 of the result is a "1"; otherwise it is reset (Low). The Zero flag is set if the result is "0"; otherwise it is reset. The Parity flag is set if the modulo 2 sum of the bits of the result is "0" (Even Parity); otherwise (Odd Parity) it is reset. The Carry flag is set if the last instruction resulted in a carry or a borrow out of the most significant bit (bit 7) of the result; otherwise it is reset.

In addition to the four testable flags, the μPD8080AF has another flag (ACY) that is not directly testable. It is used for multiple precision arithmetic operations with the DAA instruction. The Auxiliary Carry flag is set if the last instruction resulted in a carry or a borrow from bit 3 into bit 4; otherwise it is reset.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the μPD8080AF. The ability to increment and decrement memory, the six general registers and the accumulator are provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the μPD8080AF instruction set.

The special instruction group completes the μPD8080AF instruction set: NOP, HALT stop processor execution; DAA provides decimal arithmetic capability; STC sets the carry flag; CMC complements it; CMA complements the contents of the accumulator; and XCHG exchanges the contents of two 16-bit register pairs directly.

DATA AND INSTRUCTION FORMATS

Data in the μPD8080AF is stored as 8-bit binary integers. All data/instruction transfers to the system data bus are in the following format:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

MSB DATA WORD LSB

Instructions are one, two, or three bytes long. Multiple byte instructions must be stored in successive locations of program memory. The address of the first byte is used as the address of the instruction.

		TYPICAL INSTRUCTIONS
One Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable, or disable interrupt instructions
Two Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Immediate mode or I/O instructions
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OPERAND	
Three Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Jump, call or direct load and store instructions
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	LOW ADDRESS OR OPERAND 1	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	HIGH ADDRESS OR OPERAND 2	

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INSTRUCTION SET TABLE

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D7	D6	D5	D4	D3	D2	D1	D0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
MOVE														
MOV d,s	Move register to register	0	1	d	d	d	s	s	s	5				
MOV M,s	Move register to memory	0	1	1	1	0	s	s	s	7				
MOV d,M	Move memory to register	0	1	d	d	d	1	1	0	7				
MVI d,D8	Move immediate to register	0	0	d	d	d	1	1	0	7				
MVI M,D8	Move immediate to memory	0	0	1	1	0	1	1	0	10				
INCREMENT/DECREMENT														
INR d	Increment register	0	0	d	d	d	1	0	0	5	•	•	•	
DCR d	Decrement register	0	0	d	d	d	1	0	1	5	•	•	•	
INR M	Increment memory	0	0	1	1	0	1	0	0	10	•	•	•	
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10	•	•	•	
ALU – REGISTER TO ACCUMULATOR														
ADD s	Add register to A	1	0	0	0	0	s	s	s	4	•	•	•	•
ADC s	Add register to A with carry	1	0	0	0	1	s	s	s	4	•	•	•	•
SUB s	Subtract register from A	1	0	0	1	0	s	s	s	4	•	•	•	•
SBB s	Subtract register from A with borrow	1	0	0	1	1	s	s	s	4	•	•	•	•
ANA s	AND register with A	1	0	1	0	0	s	s	s	4	•	•	•	0
XRA s	Exclusive OR Register with A	1	0	1	0	1	s	s	s	4	•	•	•	0
ORA s	OR register with A	1	0	1	1	0	s	s	s	4	•	•	•	0
CMP s	Compare register with A	1	0	1	1	1	s	s	s	4	•	•	•	•
ALU – MEMORY TO ACCUMULATOR														
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7	•	•	•	•
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7	•	•	•	•
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7	•	•	•	•
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7	•	•	•	•
ANA M	AND memory with A	1	0	1	0	0	1	1	0	7	•	•	•	0
XRA M	Exclusive OR memory with A	1	0	1	0	1	1	1	0	7	•	•	•	0
ORA M	OR memory with A	1	0	1	1	0	1	1	0	7	•	•	•	0
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7	•	•	•	•
ALU – IMMEDIATE TO ACCUMULATOR														
ADI D8	Add immediate to A	1	1	0	0	0	1	1	0	7	•	•	•	•
ACI D8	Add immediate to A with carry	1	1	0	0	1	1	1	0	7	•	•	•	•
SUI D8	Subtract immediate from A	1	1	0	1	0	1	1	0	7	•	•	•	•
SBI D8	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7	•	•	•	•
ANI D8	AND immediate with A	1	1	1	0	0	1	1	0	7	•	•	•	0
XRI D8	Exclusive OR immediate with A	1	1	1	0	1	1	1	0	7	•	•	•	0
ORI D8	OR immediate with A	1	1	1	1	0	1	1	0	7	•	•	•	0
CPI D8	Compare immediate with A	1	1	1	1	1	1	1	0	7	•	•	•	•
ALU – ROTATE														
RLC	Rotate A left, MSB to carry (8-bit)	0	0	0	0	0	1	1	1	4				•
RRC	Rotate A right, LSB to carry (8-bit)	0	0	0	0	1	1	1	1	4				•
RAL	Rotate A left through carry (9-bit)	0	0	0	1	0	1	1	1	4				•
RAR	Rotate A right through carry (9-bit)	0	0	0	1	1	1	1	1	4				•
JUMP														
JMP ADDR	Jump unconditional	1	1	0	0	0	0	1	1	10				
JNZ ADDR	Jump on not zero	1	1	0	0	0	0	1	0	10				
JZ ADDR	Jump on zero	1	1	0	0	1	0	1	0	10				
JNC ADDR	Jump on no carry	1	1	0	1	0	0	1	0	10				
JC ADDR	Jump on carry	1	1	0	1	1	0	1	0	10				
JPO ADDR	Jump on parity odd	1	1	1	0	0	0	1	0	10				
JPE ADDR	Jump on parity even	1	1	1	0	1	0	1	0	10				
JP ADDR	Jump on positive	1	1	1	1	0	0	1	0	10				
JM ADDR	Jump on minus	1	1	1	1	1	0	1	0	10				
CALL														
CALL ADDR	Call unconditional	1	1	0	0	1	1	0	1	17				
CNZ ADDR	Call on not zero	1	1	0	0	0	1	0	0	11/17				
CZ ADDR	Call on zero	1	1	0	0	1	1	0	0	11/17				
CNC ADDR	Call on no carry	1	1	0	1	0	1	0	0	11/17				
CC ADDR	Call on carry	1	1	0	1	1	1	0	0	11/17				
CPO ADDR	Call on parity odd	1	1	1	0	0	1	0	0	11/17				
CPE ADDR	Call on parity even	1	1	1	0	1	1	0	0	11/17				
CP ADDR	Call on positive	1	1	1	1	0	1	0	0	11/17				
CM ADDR	Call on minus	1	1	1	1	1	1	0	0	11/17				
RETURN														
RET	Return	1	1	0	0	1	0	0	1	10				
RNZ	Return on not zero	1	1	0	0	0	0	0	0	5/11				
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11				
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11				
RC	Return on carry	1	1	0	1	1	0	0	0	5/11				
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11				
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11				
RP	Return on positive	1	1	1	1	0	0	0	0	5/11				
RM	Return on minus	1	1	1	1	1	0	0	0	5/11				

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D7	D6	D5	D4	D3	D2	D1	D0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
LOAD REGISTER PAIR														
LXI B,D16	Load immediate register pair BC	0	0	0	0	0	0	0	1	10				
LXI D,D16	Load immediate register pair DE	0	0	0	1	0	0	0	1	10				
LXI H,D16	Load immediate register pair HL	0	0	1	0	0	0	0	1	10				
LXI SP,D16	Load immediate Stack Pointer	0	0	1	1	0	0	0	1	10				
PUSH														
PUSH B	Push register pair BC on stack	1	1	0	0	0	1	0	1	11				
PUSH D	Push register pair DE on stack	1	1	0	1	0	1	0	1	11				
PUSH H	Push register pair HL on stack	1	1	1	0	0	1	0	1	11				
PUSH PSW	Push A and flags on stack	1	1	1	1	0	1	0	1	11				
POP														
POP B	Pop register pair BC off stack	1	1	0	0	0	0	0	1	10				
POP D	Pop register pair DE off stack	1	1	0	1	0	0	0	1	10				
POP H	Pop register pair HL off stack	1	1	1	0	0	0	0	1	10				
POP PSW	Pop A and flags off stack	1	1	1	1	0	0	0	1	10	•	•	•	•
DOUBLE ADD														
DAD B	Add BC to HL	0	0	0	0	1	0	0	1	10				•
DAD D	Add DE to HL	0	0	0	1	1	0	0	1	10				•
DAD H	Add HL to HL	0	0	1	0	1	0	0	1	10				•
DAD SP	Add Stack Pointer to HL	0	0	1	1	1	0	0	1	10				•
INCREMENT REGISTER PAIR														
INX B	Increment BC	0	0	0	0	0	0	1	1	5				
INX D	Increment DE	0	0	0	1	0	0	1	1	5				
INX H	Increment HL	0	0	1	0	0	0	1	1	5				
INX SP	Increment Stack Pointer	0	0	1	1	0	0	1	1	5				
DECREMENT REGISTER PAIR														
DCX B	Decrement BC	0	0	0	0	1	0	1	1	5				
DCX D	Decrement DE	0	0	0	1	1	0	1	1	5				
DCX H	Decrement HL	0	0	1	0	1	0	1	1	5				
DCX SP	Decrement Stack Pointer	0	0	1	1	1	0	1	1	5				
REGISTER INDIRECT														
STAX B	Store A at ADDR in BC	0	0	0	0	0	0	1	0	7				
STAX D	Store A at ADDR in DE	0	0	0	1	0	0	1	0	7				
LDAX B	Load A at ADDR in BC	0	0	0	0	1	0	1	0	7				
LDAX D	Load A at ADDR in DE	0	0	0	1	1	0	1	0	7				
DIRECT														
STA ADDR	Store A direct	0	0	1	1	0	0	1	0	13				
LDA ADDR	Load A direct	0	0	1	1	1	0	1	0	13				
SHLD ADDR	Store HL direct	0	0	1	0	0	0	1	0	16				
LHLD ADDR	Load HL direct	0	0	1	0	1	0	1	0	16				
MOVE REGISTER PAIR														
XCHG	Exchange DE and HL register pairs	1	1	1	0	1	0	1	1	4				
XTHL	Exchange top of stack and HL	1	1	1	0	0	0	1	1	18				
SPHL	HL to Stack Pointer	1	1	1	1	1	0	0	1	5				
PCHL	HL to Program Counter	1	1	1	0	1	0	0	1	5				
INPUT/OUTPUT														
IN A	Input	1	1	0	1	1	0	1	1	10				
OUT A	Output	1	1	0	1	0	0	1	1	10				
EI	Enable interrupts	1	1	1	1	1	0	1	1	4				
DI	Disable interrupts	1	1	1	1	0	0	1	1	4				
RST A	Restart	1	1	A	A	A	1	1	1	11				
MISCELLANEOUS														
CMA	Complement A	0	0	1	0	1	1	1	1	4				
STC	Set carry	0	0	1	1	0	1	1	1	4				1
CMC	Complement carry	0	0	1	1	1	1	1	1	4				CY
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4	•	•	•	•
NOP	No operation	0	0	0	0	0	0	0	0	4				
HLT	Halt	0	1	1	1	0	1	1	0	7				

Notes:

[1] Operand Symbols used
A = 8-bit address or expression
s = source register
d = destination register
PSW = Processor Status Word
SP = Stack Pointer
D8 = 8-bit data quantity, expression, or constant, always B_2 of instruction
D16 = 16-bit data quantity, expression, or constant, always B_3B_2 of instruction
ADDR = 16-bit Memory address expression

[2] ddd or sss – 000 B – 001 C – 010 D – 011 E – 100 H – 101 L – 110 Memory – 111 A.

[3] Two possible cycle times (5/11) indicate instruction cycles dependent on condition flags.

[4] • = flag affected
= flag not affected
0 = flag reset
1 = flag set

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INSTRUCTION CYCLE TIMES

One to five machine cycles ($M_1 - M_5$) are required to execute an instruction. Each machine cycle involves the transfer of an instruction or data byte into the processor or a transfer of a data byte out of the processor (the sole exception being the double add instruction). The first one, two or three machine cycles obtain the instruction from the memory or an interrupting I/O controller. The remaining cycles are used to execute the instruction. Each machine cycle requires from three to five clock times ($T_1 - T_5$). During $\phi 1 \cdot$ SYNC of each machine cycle, a status word that identifies the type of machine cycle is available on the data bus.

Execution times and machine cycles used for each type of instruction are shown below.

INSTRUCTION	MACHINE CYCLES EXECUTED	CLOCK TIMES (MIN/MAX)
RST X and PUSH RP	PCR5 (1) SPW3 (5) SPW3 (5)	11
All CALL Instructions	PCR5 (1) PCR3 (2) PCR3 (2) SPW3 (5) SPW3 (5)	11/17
All Conditional RETURN Instructions	PCR5 (1) SPR3 (4) SPR3 (4)	5/11
RET Instructions	PCR4 (1) SPR3 (4) SPR3 (4)	10
XTHL	PCR4 (1) SPR3 (4) SPR3 (4) SPW3 (5) SPW5 (5)	18
DAD RP	PCR4 (1) PCX3 (X) PCX3 (X)	10
INR R; INX RP, DCR R; DCX RP; PCHL; MOV R, R; SPHL	PCR5 (1)	5
All JUMP Instructions and LXI RP	PCR4 (1) PCR3 (2) PCR3 (2)	10
POP RP	PCR4 (1) SPR3 (4) SPR3 (4)	10
LDA	PCR4 (1) PCR3 (2) PCR3 (2) BBR3 (2)	13
STA	PCR4 (1) PCR3 (2) PCR3 (2) BBW3 (3)	13
LHLD	PCR4 (1) PCR3 (2) PCR3 (2) BBR3 (2) BBR3 (2)	16
SHLD	PCR4 (1) PCR3 (2) PCR3 (2) BBW3 (3) BBW3 (3)	16
STAX B	PCR4 (1) BCW3 (3)	7
STAX D	PCR4 (1) DEW3 (3)	7
LDAX B	PCR4 (1) BCR3 (2)	7
LDAX D	PCR4 (1) DER3 (2)	7
MOV R, M; ADD M; ADC M; SUB M; SB B M; ANA M; XRA M; ORA M; CMP M	PCR4 (1) HLR3 (2)	7
INR M and DCR M	PCR4 (1) HLR3 (2) HLW3 (3)	10
MVI M	PCR4 (1) PCR3 (2) HLW3 (3)	10
MVI R; ADI; ACI; SUI; SBI; ANI; XRI; ORI; CPI	PCR4 (1) PCR3 (2)	7
MOV M, R	PCR4 (1) HLW3 (3)	7
EI; DI ADD R; ADC R; SUB R; SBB R; ANA R; XRA R; ORA R; CMP R; RLC; RRC; RAL; RAR; DAA; CMA; STC; CMC; NOP; XCHG	PCR4 (1)	4
OUT	PCR4 (1) PCR3 (2) ABW3 (7)	10
IN	PCR4 (1) PCR3 (2) ABR3 (6)	10
HLT	PCR4 (1) PCX3 (9)	7

Machine Cycle Symbol Definition

XX Y Z (N)
- XX: Status word defining type of machine cycle (See Status Word Chart)
- Y: Number of clocks for this machine cycle
- Z: R = Read cycle — data into processor; W = Write cycle — data out of processor; X = No data transfer; PC = Program Counter used as address
- (N)

XX
- HL = Registers H and L used as address
- BC = Registers B and C used as address
- DE = Registers D and E used as address
- SP = Stack Pointer used as address
- BB = Byte 2 and 3 used as address
- AB = Byte 2 used as address

Underlined (XXYZ(N)) indicates machine cycle is executed if condition is True.

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STATUS INFORMATION DEFINITION

SYMBOLS	DATA BUS BIT	DEFINITION
INTA ①	D_0	Acknowledge signal for INTERRUPT request. Signal should be used to gate a restart or CALL instruction onto the data bus when DBIN is active.
$\overline{WO}$	D_1	Indicates that the operation in the current machine cycle will be a WRITE memory or OUTPUT function ($\overline{WO}$ = 0). Otherwise, a READ memory or INPUT operation will be executed.
STACK	D_2	Indicates that the address bus holds the pushdown stack address from the Stack Pointer.
HLTA	D_3	Acknowledge signal for HALT instruction.
OUT	D_4	Indicates that the address bus contains the address of an output device and the data bus will contain the output data when $\overline{WR}$ is active.
M_1	D_5	Provides a signal to indicate that the CPU is in the fetch cycle for the first byte of an instruction.
INP ①	D_6	Indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when DBIN is active.
MEMR ①	D_7	Designates that the data bus will be used for memory read data.

Note: ① These three status bits can be used to control the flow of data onto the μPD8080AF data bus.

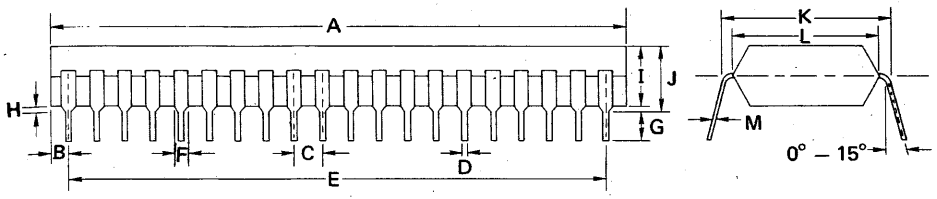
STATUS WORD CHART

TYPE OF MACHINE CYCLE

DATA BUS BIT	STATUS INFORMATION	INSTRUCTION FETCH	MEMORY READ	MEMORY WRITE	STACK READ	STACK WRITE	INPUT READ	OUTPUT WRITE	INTERRUPT ACKNOWLEDGE	HALT ACKNOWLEDGE	INT. ACK. WHILE HALT
		①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩
D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0

Ⓝ STATUS WORD

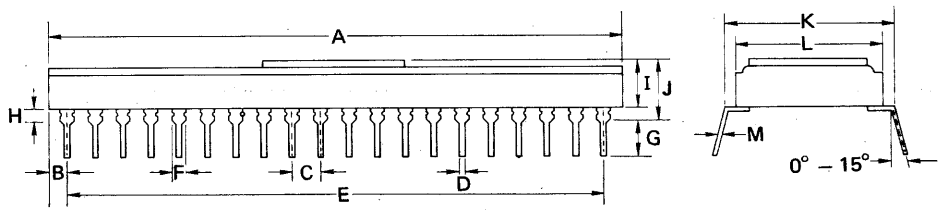
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PACKAGE OUTLINE
μPD8080AFC/D

μPD8080AFC
(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54	0.10
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



μPD8080AFD
(Ceramic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54	0.100
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.5	0.531
M	0.30 ± 0.1	0.012 ± 0.004

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8-BIT N-CHANNEL MICROPROCESSOR

DESCRIPTION

The μPD8080A is a complete 8-bit parallel processor for use in general purpose digital computer systems, which offers higher performance than conventional 8080A microprocessors. It is fabricated on a single LSI chip using N-channel silicon gate MOS process.

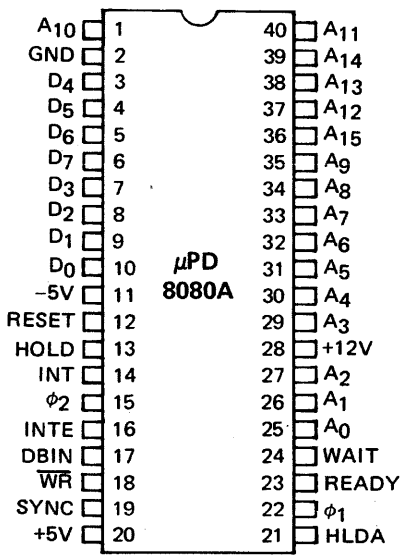
This processor is designed to greatly simplify system design. Separate 16-line address and 8-line bidirectional data busses are employed to allow direct interface to memories and I/O ports. Control signals, requiring no decoding, are provided directly by the processor. All busses, including the control bus, are TTL and CMOS compatible.

The μPD8080A has the capability to accept a multiple byte instruction upon an interrupt. This means that a CALL instruction can be inserted so that any address in the memory can be the starting location for an interrupt program. This can be accomplished without auxilliary circuit because INTA is active for all three bytes of the CALL instruction. Another important feature is that the decimal adjust accumulator instruction operates correctly after subtraction as well as after addition; thus BCD subtraction can be performed at the same speed as BCD addition.

FEATURES

- Software and Pin Compatible with Industry Standard 8080A
- Clock Frequency – 2.0 MHz
- Equivalent to the μPD8080AF with Enhancements
- Direct BCD Subtraction as well as Addition
- MOV r, r Executes in 4 Clock Cycles
- Interrupt Acknowledge is Active for 3 Byte Instructions such as CALL
- Available in a 40-pin Ceramic Package

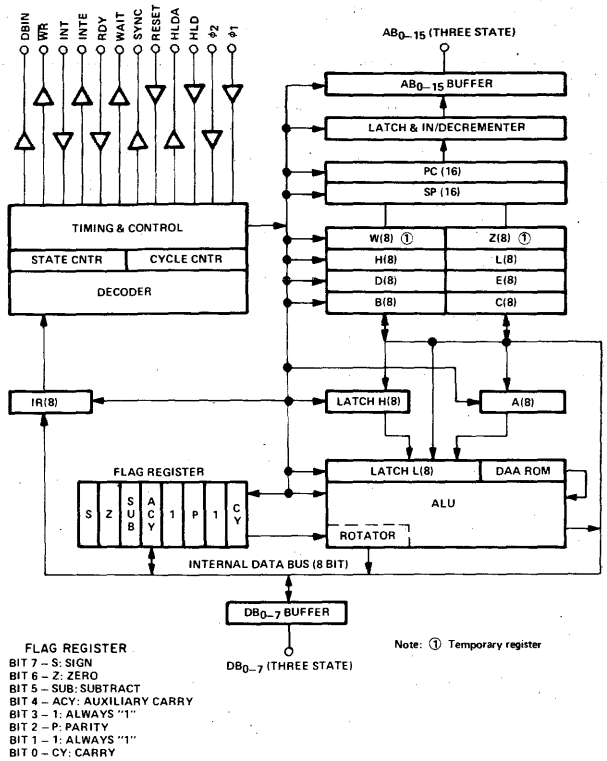
PIN CONFIGURATION



Rev/1

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BLOCK DIAGRAM



FLAG REGISTER
BIT 7 – S: SIGN
BIT 6 – Z: ZERO
BIT 5 – SUB: SUBTRACT
BIT 4 – ACY: AUXILIARY CARRY
BIT 3 – 1: ALWAYS "1"
BIT 2 – P: PARITY
BIT 1 – 1: ALWAYS "1"
BIT 0 – CY: CARRY

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages	−0.3 to +20 Volts ①
V_{CC}, V_{DD} and V_{SS}	−0.3 to +20 Volts ①
Power Dissipation	1.5W

Note: ① Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = GND, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Input Low Voltage	V_{ILC}	V_{SS} − 1		V_{SS} + 0.8	V	
Clock Input High Voltage	V_{IHC}	9.0		V_{DD} + 1	V	
Input Low Voltage	V_{IL}	V_{SS} − 1		V_{SS} + 0.8	V	
Input High Voltage	V_{IH}	3.0		V_{CC} + 1	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.9 mA on all outputs
Output High Voltage	V_{OH}	3.7 3.5			V V	I_{OH} = −150 μA ② I_{OH} = −1.0 mA
Avg. Power Supply Current (V_{DD})	$I_{DD(AV)}$		55	75	mA	t_{CY} min
Avg. Power Supply Current (V_{CC})	$I_{CC(AV)}$		50	70	mA	t_{CY} min
Avg. Power Supply Current (V_{BB})	$I_{BB(AV)}$		0.01	1	mA	t_{CY} min
Input Leakage	I_{IL}			±10 ②	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Clock Leakage	I_{CL}			±10 ②	μA	$V_{SS} \leq V_{CLOCK} \leq V_{DD}$
Data Bus Leakage in Input Mode	I_{DL} ①			+10 ② −10 ②	μA μA	$V_{IN} = V_{CC}$ $V_{IN} = V_{SS}$ + 0.45V
Address and Data Bus Leakage During HOLD	I_{FL}			+10 ② −10 ②	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS}$ + 0.45V

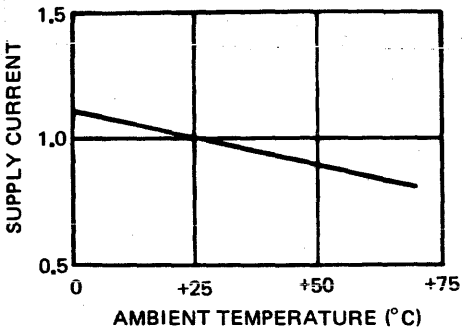
Notes: ① There are no internal pull-up resistors on the inputs.
② Minus (−) designates current flow out of the device.

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CAPACITANCE $T_a = 25°C$; $V_{CC} = V_{DD} = 0V$; $V_{BB} = -5V$

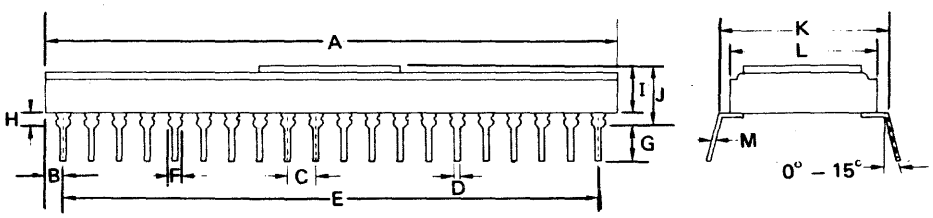
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Capacitance	$C\phi$		17	25	pF	f_c = 1 MHz
Input Capacitance	C_{IN}		6	10	pF	Unmeasured Pins
Output Capacitance	C_{OUT}		10	20	pF	Returned to V_{SS}

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED ①



Note: ① ΔI supply/ΔT_a = −0.45%/°C.

PACKAGE OUTLINE μPD8080AD



ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

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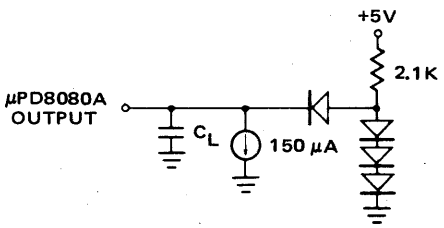
AC CHARACTERISTICS

T_a = −10°C to 70°C; V_{DD} = +12V ± 5%; V_{CC} = +5V ± 5%; V_{BB} = −5V ± 5%; V_{SS} = 0V, unless otherwise specified

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Clock Period	t_{CY} ③	0.48		2.0	μs	
Clock Rise and Fall Time	t_r, t_f	0		50	ns	
φ1 Pulse Width	$t_{\phi1}$	60			ns	
φ2 Pulse Width	$t_{\phi2}$	220			ns	
Delay φ1 to φ2	t_{D1}	0			ns	
Delay φ2 to φ1	t_{D2}	70			ns	
Delay φ1 to φ2 Leading Edges	t_{D3}	80			ns	
Address Output Delay From φ2	t_{DA} ②			200	ns	C_L = 100 pf
Data Output Delay From φ2	t_{DD} ②			220	ns	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			120	ns	C_L = 50 pf
DBIN Delay From φ2	t_{DF} ②	25		140	ns	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	ns	
Data Setup Time During φ1 and DBIN	t_{DS1}	30			ns	
	t_{DS2}	⑤				
Data Hold Time From φ2 During DBIN	t_{DH} ①	50			ns	
INTE Output Delay From φ2	t_{IE} ②			200	ns	C_L = 50 pf
READY Setup Time During φ2	t_{RS}	120			ns	
READY Setup Time to φ1 High	$t_{RS\phi1}$	240			ns	
HOLD Setup Time to φ2	t_{HS}	140			ns	
INT Setup Time During φ2 (for all modes)	t_{IS}	120			ns	
Hold Time From φ2 (READY, INT, HOLD)	t_H	0			ns	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	ns	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑥			ns	C_L = 100 pf: Address, Data C_L = 50 pf: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑦			ns	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑧			ns	
Address Stable From $\overline{WR}$	t_{WA} ②	⑧			ns	
HLDA to Float Delay	t_{HF} ②	⑨			ns	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑩			ns	
Address Hold Time After DBIN During HLDA	t_{AH} ②	-20			ns	

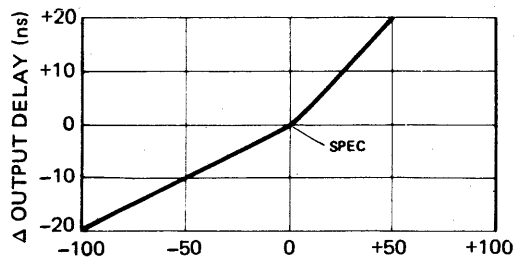
Notes: ① Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.

② Load Circuit



③ Actual $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} > t_{CY}$ Min.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



④ The following are relevant when interfacing the μPD8080A to devices having V_{IH} = 3.3V.

a. Maximum output rise time from 0.8V to 3.3V = 100 ns at C_L = SPEC.

b. Output delay when measured to 3.0V = SPEC + 60 ns at C_L = SPEC.

c. If $C_L \neq$ SPEC, add 0.6 ns/pF if $C_L > C_{SPEC}$, subtract 0.3 ns/pF (from modified delay) if $C_L < C_{SPEC}$.

⑤ No restrictions.

⑥ $t_{AW} = 2\ t_{CY} - t_{D3} - t_{r\phi2} - 140$

⑦ $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 170$

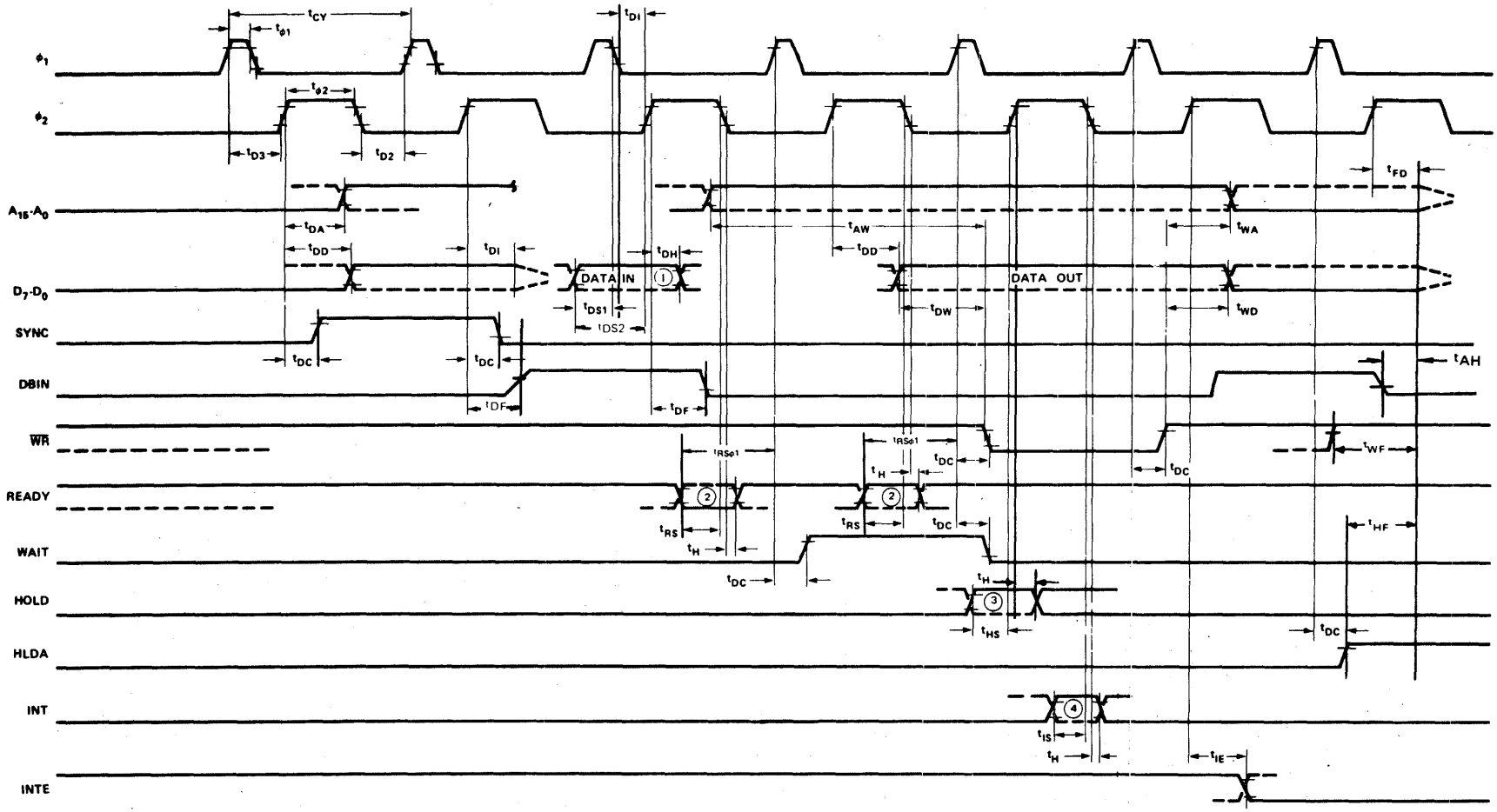
⑧ If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.

⑨ $t_{HF} = t_{D3} + t_{r\phi2} - 50$ ns.

⑩ $t_{WF} = t_{D3} + t_{r\phi2} - 10$ ns.

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TIMING WAVEFORMS ⑤ ⑥



① Data in must be stable for this period during DBIN T_3. t_{DS1} must be satisfied.

② Ready signal must be stable for this period during T_2. (Must be externally synchronized.)

③ Hold signal must be stable for this period during T_2 when entering hold mode, and during T_3, T_4 and T_5 when in hold mode. (External synchronization is not required.)

④ Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)

⑤ This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

⑥ Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V, "0" = 1.0V; INPUTS "1" = 3.0V; "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.

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INSTRUCTION SET TABLE

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D7 D6 D5 D4 D3 D2 D1 D0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
MOVE							
MOV d,s	Move register to register	0 1 d d d s s s	4				
MOV M,s	Move register to memory	0 1 1 1 0 s s s	7				
MOV d,M	Move memory to register	0 1 d d d 1 1 0	7				
MVI d,D8	Move immediate to register	0 0 d d d 1 1 0	7				
MVI M,D8	Move immediate to memory	0 0 1 1 0 1 1 0	10				
INCREMENT/DECREMENT							
INR d	Increment register	0 0 d d d 1 0 0	5	•	•	•	
DCR d	Decrement register	0 0 d d d 1 0 1	5	•	•	•	
INR M	Increment memory	0 0 1 1 0 1 0 0	10	•	•	•	
DCR M	Decrement memory	0 0 1 1 0 1 0 1	10	•	•	•	
ALU – REGISTER TO ACCUMULATOR							
ADD s	Add register to A	1 0 0 0 0 s s s	4	•	•	•	•
ADC s	Add register to A with carry	1 0 0 0 1 s s s	4	•	•	•	•
SUB s	Subtract register from A	1 0 0 1 0 s s s	4	•	•	•	•
SSB s	Subtract register from A with borrow	1 0 0 1 1 s s s	4	•	•	•	•
ANA s	AND register with A	1 0 1 0 0 s s s	4	•	•	•	o
XRA s	Exclusive OR register with A	1 0 1 0 1 s s s	4	•	•	•	o
ORA s	OR register with A	1 0 1 1 0 s s s	4	•	•	•	o
CMP s	Compare register with A	1 0 1 1 1 s s s	4	•	•	•	•
ALU – MEMORY TO ACCUMULATOR							
ADD M	Add memory to A	1 0 0 0 0 1 1 0	7	•	•	•	•
ADC M	Add memory to A with carry	1 0 0 0 1 1 1 0	7	•	•	•	•
SUB M	Subtract memory from A	1 0 0 1 0 1 1 0	7	•	•	•	•
SBB M	Subtract memory from A with borrow	1 0 0 1 1 1 1 0	7	•	•	•	•
ANA M	AND memory with A	1 0 1 0 0 1 1 0	7	•	•	•	o
XRA M	Exclusive OR memory with A	1 0 1 0 1 1 1 0	7	•	•	•	o
ORA M	OR memory with A	1 0 1 1 0 1 1 0	7	•	•	•	o
CMP M	Compare memory with A	1 0 1 1 1 1 1 0	7	•	•	•	•
ALU – IMMEDIATE TO ACCUMULATOR							
ADI D8	Add immediate to A	1 1 0 0 0 1 1 0	7	•	•	•	•
ACI D8	Add immediate to A with carry	1 1 0 0 1 1 1 0	7	•	•	•	•
SUI D8	Subtract immediate from A	1 1 0 1 0 1 1 0	7	•	•	•	•
SBI D8	Subtract immediate from A with borrow	1 1 0 1 1 1 1 0	7	•	•	•	•
ANI D8	AND immediate with A	1 1 1 0 0 1 1 0	7	•	•	•	o
XRI D8	Exclusive OR immediate with A	1 1 1 0 1 1 1 0	7	•	•	•	o
ORI D8	OR immediate with A	1 1 1 1 0 1 1 0	7	•	•	•	o
CPI D8	Compare immediate with A	1 1 1 1 1 1 1 0	7	•	•	•	•
ALU – ROTATE							
RLC	Rotate A left, MSB to carry (8-bit)	0 0 0 0 0 1 1 1	4				•
RRC	Rotate A right, LSB to carry (8-bit)	0 0 0 0 1 1 1 1	4				•
RAL	Rotate A left through carry (9-bit)	0 0 0 1 0 1 1 1	4				•
RAR	Rotate A right through carry (9-bit)	0 0 0 1 1 1 1 1	4				•
JUMP							
JMP ADDR	Jump unconditional	1 1 0 0 0 0 1 1	10				
JNZ ADDR	Jump on not zero	1 1 0 0 0 0 1 0	10				
JZ ADDR	Jump on zero	1 1 0 0 1 0 1 0	10				
JNC ADDR	Jump on no carry	1 1 0 1 0 0 1 0	10				
JC ADDR	Jump on carry	1 1 0 1 1 0 1 0	10				
JPO ADDR	Jump on parity odd	1 1 1 0 0 0 1 0	10				
JPE ADDR	Jump on parity even	1 1 1 0 1 0 1 0	10				
JP ADDR	Jump on positive	1 1 1 1 0 0 1 0	10				
JM ADDR	Jump on minus	1 1 1 1 1 0 1 0	10				
CALL							
CALL ADDR	Call unconditional	1 1 0 0 1 1 0 1	17				
CNZ ADDR	Call on not zero	1 1 0 0 0 1 0 0	11/17				
CZ ADDR	Call on zero	1 1 0 0 1 1 0 0	11/17				
CNC ADDR	Call on no carry	1 1 0 1 0 1 0 0	11/17				
CC ADDR	Call on carry	1 1 0 1 1 1 0 0	11/17				
CPO ADDR	Call on parity odd	1 1 1 0 0 1 0 0	11/17				
CPE ADDR	Call on parity even	1 1 1 0 1 1 0 0	11/17				
CP ADDR	Call on positive	1 1 1 1 0 1 0 0	11/17				
CM ADDR	Call on minus	1 1 1 1 1 1 0 0	11/17				
RETURN							
RET	Return	1 1 0 0 1 0 0 1	11				
RNZ	Return on not zero	1 1 0 0 0 0 0 0	5/11				
RZ	Return on zero	1 1 0 0 1 0 0 0	5/11				
RNC	Return on no carry	1 1 0 1 0 0 0 0	5/11				
RC	Return on carry	1 1 0 1 1 0 0 0	5/11				
RPO	Return on parity odd	1 1 1 0 0 0 0 0	5/11				
RPE	Return on parity even	1 1 1 0 1 0 0 0	5/11				
RP	Return on positive	1 1 1 1 0 0 0 0	5/11				
RM	Return on minus	1 1 1 1 1 0 0 0	5/11				

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D7 D6 D5 D4 D3 D2 D1 D0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
LOAD REGISTER PAIR							
LXI B,D16	Load immediate register pair BC	0 0 0 0 0 0 0 1	10				
LXI D,D16	Load immediate register pair DE	0 0 0 1 0 0 0 1	10				
LXI H,D16	Load immediate register pair HL	0 0 1 0 0 0 0 1	10				
LXI SP,D16	Load immediate Stack Pointer	0 0 1 1 0 0 0 1	10				
PUSH							
PUSH B	Push register pair BC on stack	1 1 0 0 0 1 0 1	11				
PUSH D	Push register pair DE on stack	1 1 0 1 0 1 0 1	11				
PUSH H	Push register pair HL on stack	1 1 1 0 0 1 0 1	11				
PUSH PSW	Push A and flags on stack	1 1 1 1 0 1 0 1	11				
POP							
POP B	Pop register pair BC off stack	1 1 0 0 0 0 0 1	10				
POP D	Pop register pair DE off stack	1 1 0 1 0 0 0 1	10				
POP H	Pop register pair HL off stack	1 1 1 0 0 0 0 1	10				
POP PSW	Pop A and flags off stack	1 1 1 1 0 0 0 1	10	•	•	•	•
DOUBLE ADD							
DAD B	Add BC to HL	0 0 0 0 1 0 0 1	11				•
DAD D	Add DE to HL	0 0 0 1 1 0 0 1	11				•
DAD H	Add HL to HL	0 0 1 0 1 0 0 1	11				•
DAD SP	Add Stack Pointer to HL	0 0 1 1 1 0 0 1	11				•
INCREMENT REGISTER PAIR							
INX B	Increment BC	0 0 0 0 0 0 1 1	5				
INX D	Increment DE	0 0 0 1 0 0 1 1	5				
INX H	Increment HL	0 0 1 0 0 0 1 1	5				
INX SP	Increment Stack Pointer	0 0 1 1 0 0 1 1	5				
DECREMENT REGISTER PAIR							
DCX B	Decrement BC	0 0 0 0 1 0 1 1	5				
DCX D	Decrement DE	0 0 0 1 1 0 1 1	5				
DCX H	Decrement HL	0 0 1 0 1 0 1 1	5				
DCX SP	Decrement Stack Pointer	0 0 1 1 1 0 1 1	5				
REGISTER INDIRECT							
STAX B	Store A at ADDR in B	0 0 0 0 0 0 1 0	7				
STAX D	Store A at ADDR in D	0 0 0 1 0 0 1 0	7				
LDAX B	Load A at ADDR in B	0 0 0 0 1 0 1 0	7				
LDAX D	Load A at ADDR in D	0 0 0 1 1 0 1 0	7				
DIRECT							
STA ADDR	Store A direct	0 0 1 1 0 0 1 0	13				
LDA ADDR	Load A direct	0 0 1 1 1 0 1 0	13				
SHLD ADDR	Store HL direct	0 0 1 0 0 0 1 0	16				
LHLD ADDR	Load HL direct	0 0 1 0 1 0 1 0	16				
MOVE REGISTER PAIR							
XCHG	Exchange DE and HL register pairs	1 1 1 0 1 0 1 1	4				
XTHL	Exchange top of stack and HL	1 1 1 0 0 0 1 1	17				
SPHL	HL to Stack Pointer	1 1 1 1 1 0 0 1	4				
PCHL	HL to Program Counter	1 1 1 0 1 0 0 1	5				
INPUT/OUTPUT							
IN A	Input	1 1 0 1 1 0 1 1	10				
OUT A	Output	1 1 0 1 0 0 1 1	10				
EI	Enable interrupts	1 1 1 1 1 0 1 1	4				
DI	Disable interrupts	1 1 1 1 1 0 0 1	4				
RST A	Restart	1 1 A A A 1 1 1	11				
MISCELLANEOUS							
CMA	Complement A	0 0 1 0 1 1 1 1	4				
STC	Set carry	0 0 1 1 0 1 1 1	4				1
CMC	Complement carry	0 0 1 1 1 1 1 1	4				Cy
DAA	Decimal adjust A	0 0 1 0 0 1 1 1	4	•	•	•	•
NOP	No-operation	0 0 0 0 0 0 0 0	4				
HLT	Halt	0 1 1 1 0 1 1 0	7				

NOTES:

[1] Operand Symbols used
A = 8-bit address or expression
s = source register
d = destination register
PSW = Processor Status Word
SP = Stack Pointer
D8 = 8-bit data quantity, expression, or constant, always B_2 of instruction
D16 = 16-bit data quantity, expression, or constant, always B_3B_2 of instruction
ADDR = 16-bit Memory address expression

[2] ddd or sss – 000 B – 001 C – 010 D – 011 E – 100 H – 101 L – 110 Memory – 111 A.

[3] Two possible cycle times (5/11) indicate instruction cycles dependent on condition flags.

[4] • = flag affected
= flag not affected
0 = flag reset
1 = flag set

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INSTRUCTION SET

The instruction set includes arithmetic and logical operators with direct, register, indirect, and immediate addressing modes. These instructions operate exactly like the μPD8080AF except as noted.

In addition to the four testable flags, the μPD8080A has two more flags (ACY, SUB) that are not directly testable. They are used for multiple precision arithmetic operations, particularly with the DAA instruction. The Auxiliary Carry flag is set if the last instruction resulted in a carry or a borrow from bit 3 into bit 4; otherwise it is reset. The Subtract flag is set if the last instruction resulted in a subtract operation being performed; it is reset if an add operation was performed. Also, arithmetic flags are not affected by logical instructions.

DATA AND INSTRUCTION FORMATS

Data in the μPD8080A is stored as 8-bit binary integers. All data/instruction transfers to the system data bus are in the following format:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

MSB DATA WORD LSB

Instructions are one, two, or three bytes long. Multiple byte instructions must be stored in successive locations of program memory. The address of the first byte is used as the address of the instruction.

		TYPICAL INSTRUCTIONS
One Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable, or disable interrupt instructions
Two Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Immediate mode or I/O instructions
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OPERAND	
Three Byte Instructions		Jump, call or direct load and store instructions
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	LOW ADDRESS OR OPERAND 1	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	HIGH ADDRESS OR OPERAND 2	

INSTRUCTION CYCLE TIMES

One to five machine cycles ($M_1 - M_5$) are required to execute an instruction. Each machine cycle involves the transfer of an instruction or data byte into the processor or a transfer of a data byte out of the processor (the sole exception being the double add instruction). The first one, two or three machine cycles obtain the instruction from the memory or an interrupting I/O controller. The remaining cycles are used to execute the instruction. Each machine cycle requires from three to five clock times ($T_1 - T_5$). During ϕ_1 SYNC of each machine cycle, a status word that identifies the type of machine cycle is available on the data bus.

Execution times and machine cycles used for each type of instruction are shown below.

INSTRUCTION	MACHINE CYCLES EXECUTED	CLOCK TIMES (MIN/MAX)
RST X and PUSH RP	PCR5 (1) SPW3 (5) SPW3 (5)	11
All CALL Instructions	PCR5 (1) PCR3 (2) PCR3 (2) SPW3 (5) SPW3 (5)	11/17
All RET Instructions	PCR5 (1) SPR3 (4) SPR3 (4)	5/11
XTHL	PCR5 (1) SPR3 (4) SPW3 (5) SPR3 (4) SPW3 (5)	17
DAD RP	PCR5 (1) PCX3 ◯ PCX3 ◯	11
INR R; INX RP; DCR R; DCX RP; PCHL	PCR5 (1)	5
All JUMP Instructions and LXI RP	PCR4 (1) PCR3 (2) PCR3 (2)	10
POP RP	PCR4 (1) SPR3 (4) SPR3 (4)	10
LDA	PCR4 (1) PCR3 (2) PCR3 (2) BBR3 (2)	13
STA	PCR4 (1) PCR3 (2) PCR3 (2) BBW3 (3)	13
LHLD	PCR4 (1) PCR3 (2) PCR3 (2) BBR3 (2) BBR3 (2)	16
SHLD	PCR4 (1) PCR3 (2) PCR3 (2) BBW3 (3) BBW3 (3)	16
STAX B	PCR4 (1) BCW3 (3)	7
STAX D	PCR4 (1) DEW3 (3)	7
LDAX B	PCR4 (1) BCR3 (2)	7
LDAX D	PCR4 (1) DER3 (2)	7
MOV R, M; ADD M; ADC M; SUB M; SB B M; ANA M; XRA M; ORA M; CMP M	PCR4 (1) HLR3 (2)	7
INR M and DCR M	PCR4 (1) HLR3 (2) HLW3 (3)	10
MVI M	PCR4 (1) PCR3 (2) HLW3 (3)	10
MVI R; ADI; ACI; SUI; SBI; ANI; XRI; ORI; CPI	PCR4 (1) PCR3 (2)	7
MOV M, R	PCR4 (1) HLW3 (3)	7
MOV R,R, EI, DI ADD R; ADC R; SUB R; SBB R; ANA R; XRA R; ORA R; CMP R; RLC; RRC; RAL; RAR; DAA; CMA; STC; CMC; NOP; XCHG, SPHL	PCR4 (1)	4
OUT	PCR4 (1) PCR3 (2) ABW3 (7)	10
IN	PCR4 (1) PCR3 (2) ABR3 (6)	10
HLT	PCR4 (1) PCX3 (10)	7

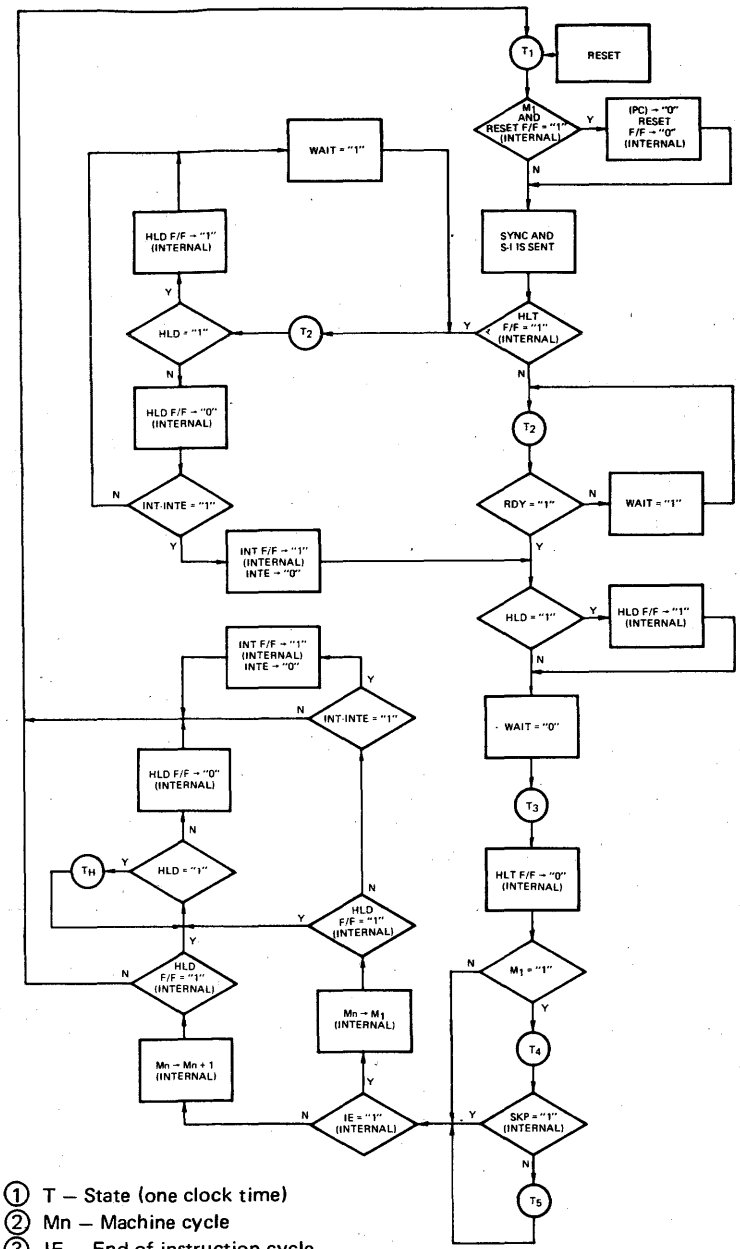
Machine Cycle Symbol Definition

XX Y Z (N)
- XX: HL = Registers H and L used as address; BC = Registers B and C used as address; DE = Registers D and E used as address; SP = Stack Pointer used as address; BB = Byte 2 and 3 used as address; AB = Byte 2 used as address.
- Y: Status word defining type of machine cycle (See Status Word Chart)
- Z: Number of clocks for this machine cycle
- (N): R = Read cycle – data into processor; W = Write cycle – data out of processor; X = No data transfer; PC = Program Counter used as address

Underlined (XXYZ(N)) indicates machine cycle is executed if condition is True.

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PROCESSOR STATE TRANSITION DIAGRAM



Notes:
1. T – State (one clock time)
2. Mn – Machine cycle
3. IE – End of instruction cycle
4. S-I – Status information
5. SKP – Skip signal (internal)
6. HLD F/F (internal) is reset when HLD signal returns to zero.
7. HLT F/F (internal) is set when HALT instruction is executed.
8. RESET F/F (internal) is set when reset signal is activated.

STATUS WORD CHART

TYPE OF MACHINE CYCLE

DATA BUS BIT	STATUS INFORMATION	① INSTRUCTION FETCH	② MEMORY READ	③ MEMORY WRITE	④ STACK READ	⑤ STACK WRITE	⑥ INPUT READ	⑦ OUTPUT WRITE	⑧ INTERRUPT ACKNOWLEDGE (M_1)	⑨ INT. ACK. (M_2, M_3)	⑩ HALT ACKNOWLEDGE	⑪ INT. ACK. WHILE HALT
												← (N) STATUS WORD
D_0	INTA	0	0	0	0	0	0	0	1	1	0	1
D_1	WO	1	1	0	1	0	1	0	1	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	0	1	0
D_4	OUT	0	0	0	0	0	0	1	0	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	0	0	0

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PRIORITY INTERRUPT CONTROLLER

DESCRIPTION

The μPB8214 is an eight-level priority interrupt controller. Designed to simplify interrupt driven microcomputer systems, the μPB8214 requires a single +5V power supply and is packaged in a 24 pin plastic Dual-in-line package.

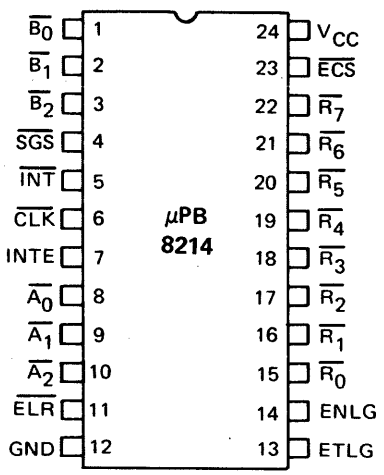
The μPB8214 accepts up to eight interrupts, determines which has the highest priority and then compares that priority with a software created current status register. If the incoming request is of a higher priority than the interrupt currently being serviced, an interrupt request to the processor is generated. Vector information that identifies the interrupting device is also generated.

The interrupt structure of the microcomputer system can be expanded beyond eight interrupt levels by cascading μPB8214s. The μPB8214's interrupt and vector information outputs are open collector and control signals are provided to simplify expansion of the interrupt structure.

FEATURES

- Eight Priority Levels
- Current Status Register and Priority Comparator
- Easily Expanded Interrupt Structure
- Single +5 Volt Supply

PIN CONFIGURATION

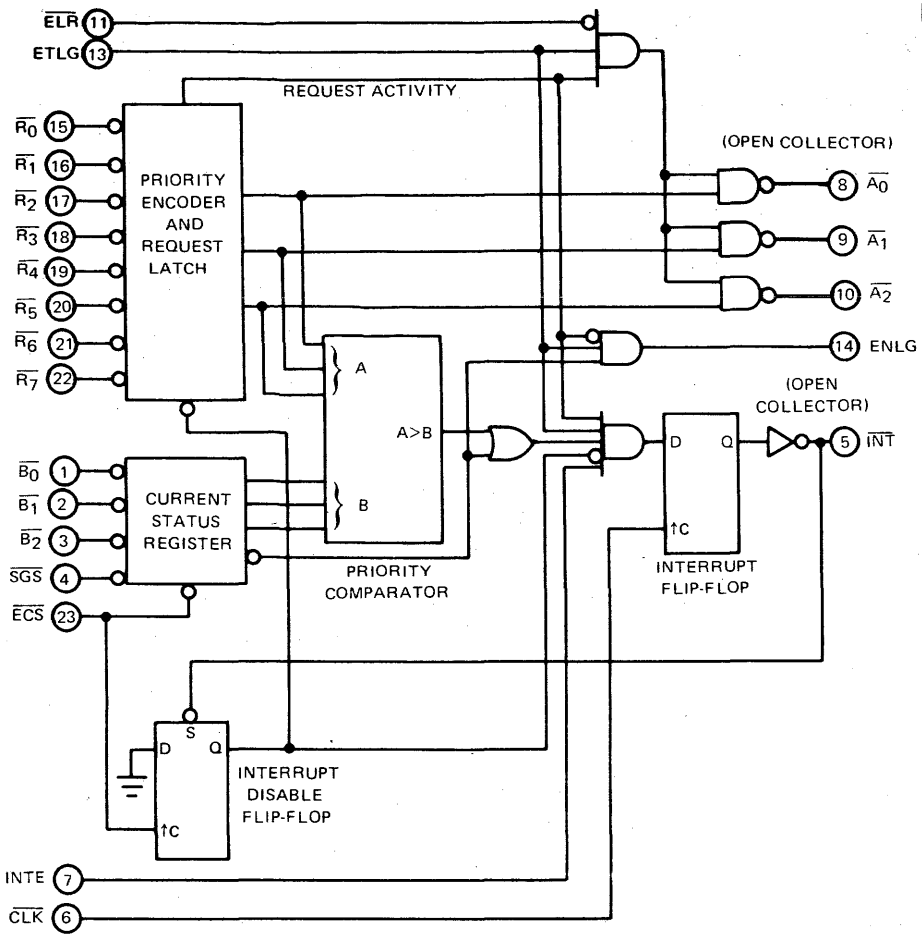


PIN NAMES

Inputs:		
$\overline{R_0}$–$\overline{R_7}$	Request Levels ($\overline{R_7}$ Highest Priority)	
$\overline{B_0}$–$\overline{B_2}$	Current Status	
$\overline{SGS}$	Status Group Select	
$\overline{ECS}$	Enable Current Status	
INTE	Interrupt Enable	
$\overline{CLK}$	Clock (INT F-F)	
$\overline{ELR}$	Enable Level Read	
ETLG	Enable This Level Group	
Outputs:		
$\overline{A_0}$–$\overline{A_2}$	Request Levels	Open
$\overline{INT}$	Interrupt (Act. Low)	Collector
ENLG	Enable Next Level Group	

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BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

General

The μPB8214 is an LSI device designed to simplify the circuitry required to implement an interrupt driven microcomputer system. Up to eight interrupting devices can be connected to a μPB8214, which will assign priority to incoming interrupt requests and accept the highest. It will also compare the priority of the highest incoming request with the priority of the interrupt being serviced. If the serviced interrupt has a higher priority, the incoming request will not be accepted.

A system with more than eight interrupting devices can be implemented by interconnecting additional μPB8214s. In order to facilitate this expansion, control signals are provided for cascading the controllers so that there is a priority established among the controllers. In addition, the interrupt and vector information outputs are open collector.

Priority Encoder and Request Latch

The priority encoder portion of the μPB8214 accepts up to eight active low interrupt requests ($\overline{R_0}$–$\overline{R_7}$). The circuit assigns priority to the incoming requests, with $\overline{R_7}$ having the highest priority and $\overline{R_0}$ the lowest. If two or more requests occur simultaneously, the μPB8214 accepts the one having the highest priority. Once an incoming interrupt request is accepted, it is stored by the request latch and a three-bit code is output. As shown in the following table, the outputs, ($\overline{A_0}$–$\overline{A_2}$) are the complement of the request level (modulo 8) and directly correspond to the bit pattern required to generate the one byte RESTART (RST) instructions recognized by an 8080A. Simultaneously with the $\overline{A_0}$–$\overline{A_2}$ outputs, a system interrupt request ($\overline{INT}$) is output by the μPB8214. It should be noted that incoming interrupt requests that are *not* accepted are not latched and must remain as an input to the μPB8214 in order to be serviced.

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FUNCTIONAL DESCRIPTION (CONT.)

RESTART GENERATION TABLE

PRIORITY REQUEST		RST	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
			1	1	$\overline{A_2}$	$\overline{A_1}$	$\overline{A_0}$	1	1	1
LOWEST	$\overline{R_0}$	7	1	1	1	1	1	1	1	1
	$\overline{R_1}$	6	1	1	1	1	0	1	1	1
	$\overline{R_2}$	5	1	1	1	0	1	1	1	1
	$\overline{R_3}$	4	1	1	1	0	0	1	1	1
	$\overline{R_4}$	3	1	1	0	1	1	1	1	1
	$\overline{R_5}$	2	1	1	0	1	0	1	1	1
	$\overline{R_6}$	1	1	1	0	0	1	1	1	1
HIGHEST	$\overline{R_7}$	0*	1	1	0	0	0	1	1	1

*CAUTION: RST 0 will vector the program counter to location 0 (zero) and invoke the same routine as the "RESET" input to 8080A.

Current Status Register

The current status register is designed to prevent an incoming interrupt request from overriding the servicing of an interrupt with higher priority. Via software, the priority level of the interrupt being serviced by the microprocessor is written into the current status register on $\overline{B_0}$–$\overline{B_2}$. The bit pattern written should be the complement of the interrupt level.

The interrupt level currently being serviced is written into the current status register by driving $\overline{ECS}$ (Enable Current Status) low. The μPB8214 will only accept interrupts with a higher priority than the value contained by the current status register. Note that the programmer is free to use the current status register for other than as above. Other levels may be written into it. The comparison may be completely disabled by driving $\overline{SGS}$ (Status Group Select) low when $\overline{ECS}$ is driven low. This will cause the μPB8214 to accept incoming interrupts only on the basis of their priority to each other.

Priority Comparator

The priority comparator circuitry compares the level of the interrupt accepted by the priority encoder and request latch with the contents of the current status register. If the incoming request has a priority level higher than that of the current status register, the $\overline{INT}$ output is enabled. Note that this comparison can be disabled by loading the current status register with $\overline{SGS}$=0.

Expansion Control Signals

A microcomputer design may often require more than eight different interrupts. The μPB8214 is designed so that interrupt system expansion is easily performed via the use of three signals: ETLG (Enable This Level Group); ENLG (Enable Next Level Group); and $\overline{ELR}$ (Enable Level Read). A high input to ETLG indicates that the μPB8214 may accept an interrupt. In a typical system, the ENLG output from one μPB8214 is connected to the ETLG input of another μPB8214, etc. The ETLG of the μPB8214 with the highest priority is tied high. This configuration sets up priority among the cascaded μPB8214's. The ENLG output will be high for any device that does not have an interrupt pending, thereby allowing a device with lower priority to accept interrupts. The $\overline{ELR}$ input is basically a chip enable and allows hardware or software to selectively disable/enable individual μPB8214's. A low on the $\overline{ELR}$ input enables the device.

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FUNCTIONAL DESCRIPTION (CONT.)

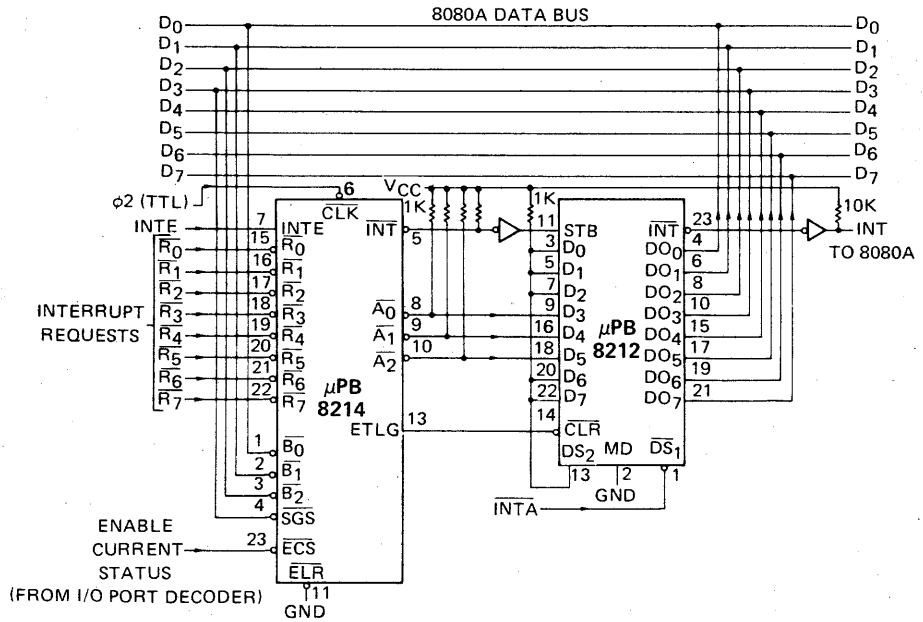
Interrupt Control Circuitry

The μPB8214 contains two flip-flops and several gates which determine whether an accepted interrupt request to the μPB8214 will generate a system interrupt to the 8080A. A condition gate drives the D input of the interrupt flip-flop whenever an interrupt request has been completely accepted. This requires that: the ETLG (Enable This Level Group) and INTE (Interrupt Enable) inputs to the μPB8214 are high; the $\overline{ELR}$ input is low; the incoming request must be of a higher priority than the contents of the current status register; and the μPB8214 must have been enabled to accept interrupt requests by the clearing of the interrupt disable flip-flop.

Once the condition gate drives the D input of the interrupt flip-flop high, a system interrupt ($\overline{INT}$) to the 8080A is generated on the next rising edge of the $\overline{CLK}$ input to the μPB8214. This $\overline{CLK}$ input is typically connected to the $\phi 2$ (TTL) output of an 8224 so that 8080A set-up time specifications are met. When $\overline{INT}$ is generated, it sets the interrupt disable flip-flop so that no additional system interrupts will be generated until it is reset. It is reset by driving $\overline{ECS}$ (Enable Current Status) low, thereby writing into the current status register.

It should be noted that the open collector $\overline{INT}$ output from the μPB8214 is active for only one clock period and thus must be externally latched for inputting to the 8080A. Also, because the $\overline{INT}$ output is open collector, when μPB8214's are cascaded, an $\overline{INT}$ output from any one will set all of the interrupt disable flip-flops in the array. Each μPB8214's interrupt disable flip-flop must then be cleared individually in order to generate subsequent system interrupts.

TYPICAL μPB8214 CIRCUITRY



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C
All Output and Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +5.5 Volts
Output Currents	100 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

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DC CHARACTERISTICS $T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Clamp Voltage (all inputs)	V_C			-1.0	V	I_C=-5mA
Input Forward Current: ETLG input	I_F		-.15	-0.5	mA	V_F=0.45V
all other inputs			-.08	-0.25	mA	
Input Reverse Current: ETLG input	I_R			80	μA	V_R=5.25V
all other inputs				40	μA	
Input LOW Voltage: all inputs	V_{IL}			0.8	V	V_{CC}=5.0V
Input HIGH Voltage: all inputs	V_{IH}	2.0			V	V_{CC}=5.0V
Power Supply Current	I_{CC}		90	130	mA	②
Output LOW Voltage: all outputs	V_{OL}		.3	.45	V	I_{OL}=10mA
Output HIGH Voltage: ENLG output	V_{OH}	2.4	3.0		V	I_{OH}=-1mA
Short Circuit Output Current: ENLG output	I_{OS}	-20	-35	-55	mA	V_{OS}=0V, V_{CC}=5.0V
Output Leakage Current: $\overline{INT}$ and $\overline{A_0}$–$\overline{A_2}$	I_{CEX}			100	μA	V_{CEX}=5.25V

CAPACITANCE ③ $T_a = 25°C$

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		5	10	pF	V_{BIAS}=2.5V
Output Capacitance	C_{OUT}		7	12	pF	V_{CC}=5V f=1mHz

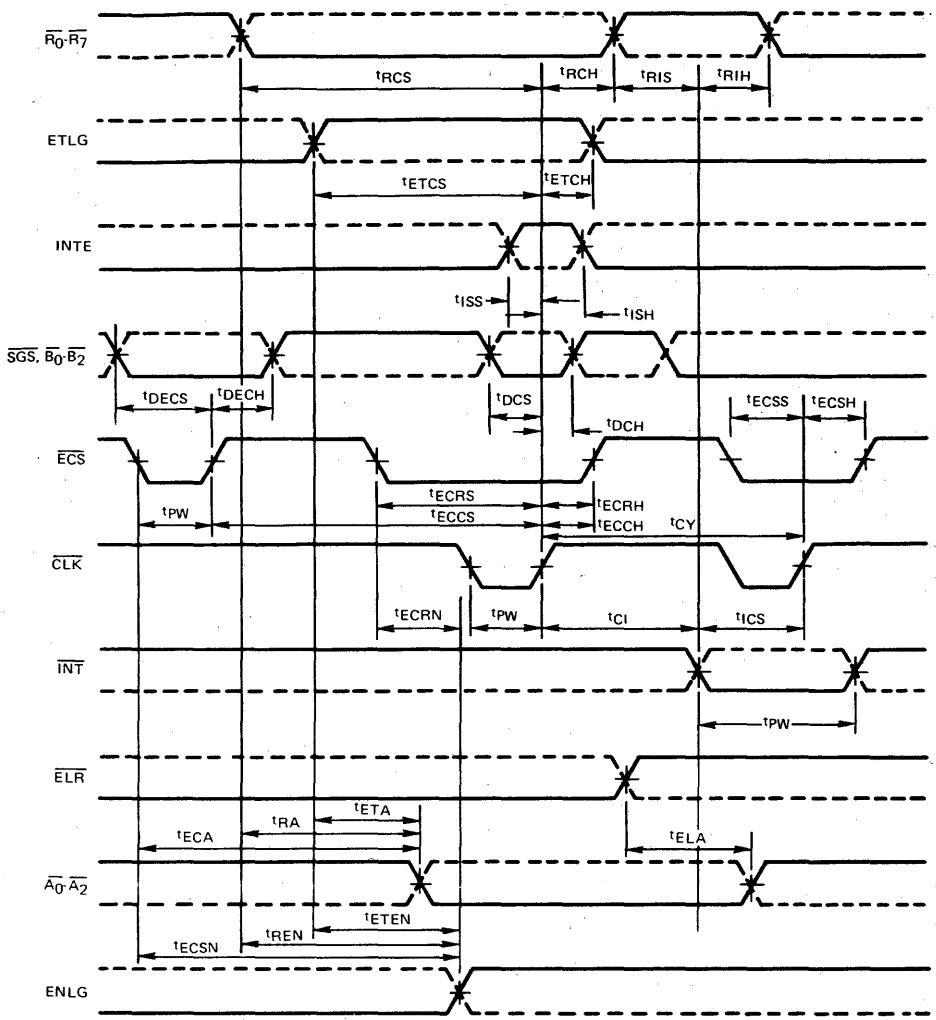
AC CHARACTERISTICS $T_a = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

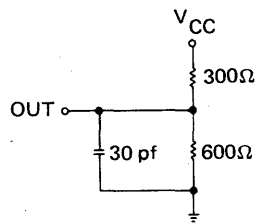
PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
$\overline{CLK}$ Cycle Time	t_{CY}	80	50		ns	Input pulse amplitude: 2.5 Volts
$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	t_{PW}	25	15		ns	
INTE Setup Time to $\overline{CLK}$	t_{ISS}	16	12		ns	
INTE Hold Time after $\overline{CLK}$	t_{ISH}	20	10		ns	
ETLG Setup Time to $\overline{CLK}$	t_{ETCS}④	25	12		ns	Input rise and fall times: 5 ns between 1 and 2 Volts
ETLG Hold Time After $\overline{CLK}$	t_{ETCH}④	20	10		ns	
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECCS}④	80	50		ns	
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECCH}⑤	0			ns	
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECRS}⑤	110	70		ns	
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECRH}⑤	0				Output loading of 15 mA and 30 pF.
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECSS}④	75	70		ns	
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECSH}④	0			ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Setup Time to $\overline{CLK}$	t_{DCS}④	70	50		ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Hold Time After $\overline{CLK}$	t_{DCH}④	0			ns	Speed measurements taken at the 1.5 Volts levels.
$\overline{R_0}$–$\overline{R_7}$ Setup Time to $\overline{CLK}$	t_{RCS}⑤	90	55		ns	
$\overline{R_0}$–$\overline{R_7}$ Hold Time After $\overline{CLK}$	t_{RCH}⑤	0			ns	
$\overline{INT}$ Setup Time to $\overline{CLK}$	t_{ICS}	55	35		ns	
$\overline{CLK}$ to $\overline{INT}$ Propagation Delay	t_{CI}		15	25	ns	
$\overline{R_0}$–$\overline{R_7}$ Setup Time to $\overline{INT}$	t_{RIS}⑥	10	0		ns	
$\overline{R_0}$–$\overline{R_7}$ Hold Time After $\overline{INT}$	t_{RIH}⑥	35	20		ns	
$\overline{R_0}$–$\overline{R_7}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{RA}		80	100	ns	
$\overline{ELR}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{ELA}		40	55	ns	
$\overline{ECS}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{ECA}		100	120	ns	
ETLG to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{ETA}		35	70	ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Setup Time to $\overline{ECS}$	t_{DECS}⑥	15	10		ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Hold Time After $\overline{ECS}$	t_{DECH}⑥	15	10		ns	
$\overline{R_0}$–$\overline{R_7}$ to ENLG Propagation Delay	t_{REN}		45	70	ns	
ELTG to ENLG Propagation Delay	t_{ETEN}		20	25	ns	
$\overline{ECS}$ to ENLG Propagation Delay	t_{ECRN}		85	90	ns	
$\overline{ECS}$ to ENLG Propagation Delay	t_{ECSN}		35	55	ns	

Notes:
① Typical values are for T_a=25°C, V_{CC}=5.0V
② $\overline{B_0}$–$\overline{B_2}$, $\overline{SGS}$, $\overline{CLK}$, $\overline{R_0}$–$\overline{R_4}$ grounded, all other inputs and all outputs open.
③ This parameter is periodically sampled and not 100% tested.
④ Required for proper operation if INTE is enabled during next clock pulse.
⑤ These times are not required for proper operation but for desired change in interrupt flip-flop.
⑥ Required for new request or status to be properly loaded.

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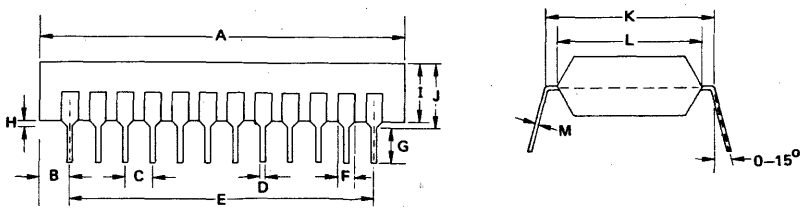
TIMING WAVEFORMS





TEST CIRCUIT

PACKAGE OUTLINE μPB8214C



ITEM	MILLIMETERS	INCHES
A	33 MAX.	1.28
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	3.2 MIN.	0.125 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	0.25 ± 0.1	0.01 ± 0.004

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CLOCK GENERATOR AND DRIVER FOR 8080A PROCESSORS

DESCRIPTION

The μPB8224 is a single chip clock generator and driver for 8080A processors. The clock frequency is determined by a user specified crystal and is capable of meeting the timing requirements of the entire 8080A family of processors. MOS and TTL level clock outputs are generated.

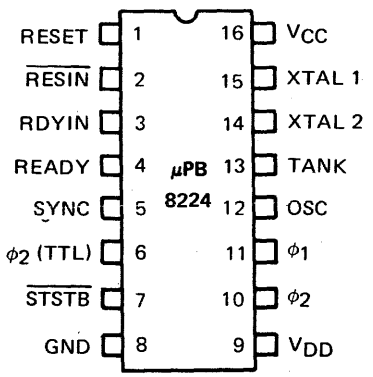
Additional logic circuitry of the μPB8224 provides signals for power-up reset, an advance status strobe and properly synchronizes the ready signal to the processor. This greatly reduces the number of chips needed for 8080A systems.

The μPB8224 is fabricated using NEC's Schottky bipolar process.

FEATURES

- Crystal Controlled Clocks
- Oscillator Output for External Timing
- MOS Level Clocks for 8080A Processor
- TTL Level Clock for DMA Activities
- Power-up Reset for 8080A Processor
- Ready Synchronization
- Advanced Status Strobe
- Reduces System Package Count
- Available in 16-pin Cerdip and Plastic Packages

PIN CONFIGURATION



PIN NAMES

$\overline{RESIN}$	Reset Input
RESET	Reset Output
RDYIN	Ready Input
READY	Ready Output
SYNC	Sync Input
$\overline{STSTB}$	Status STB Output
φ1	Processor Clocks
φ2	
XTAL 1	Crystal Connections
XTAL 2	
TANK	Used With Overtone Crystal
OSC	Oscillator Output
φ2 (TTL)	φ2 CLK (TTL Level)
V_{CC}	+5V
V_{DD}	+12V
GND	0V

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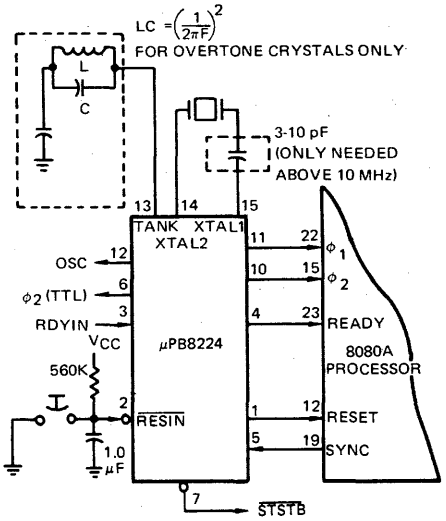
Clock Generator

The clock generator circuitry consists of a crystal controlled oscillator and a divide-by-nine counter. The crystal frequency is a function of the 8080A processor speed and is basically nine times the processor frequency, i.e.:

$$\text{Crystal frequency} = \frac{9}{t_{CY}}$$

where t_{CY} is the 8080A processor clock period.

A series resonant fundamental mode crystal is normally used and is connected across input pins XTAL1 and XTAL2. If an overtone mode crystal is used, an additional LC network, AC coupled to ground, must be connected to the TANK input of the μPB8224 as shown in the following figure.



The formula for the LC network is:

$$LC = \left(\frac{1}{2\pi F}\right)^2$$

where F is the desired frequency of oscillation.

The output of the oscillator is input to the divide-by-nine counter. It is also buffered and brought out on the OSC pin, allowing this stable, crystal controlled source to be used for derivation of other system timing signals. The divide-by-nine counter generates the two non-overlapping processor clocks, ϕ_1 and ϕ_2, which are buffered and at MOS levels, a TTL level ϕ_2 and internal timing signals.

The ϕ_1 and ϕ_2 high level outputs are generated in a 2-5-2 digital pattern, with ϕ_1 being high for two oscillator periods, ϕ_2 being high for five oscillator periods, and then neither being high for two oscillator periods. The TTL level ϕ_2,ϕ_2 (TTL), is normally used for DMA activities by gating the external device onto the 8080A bus once a Hold Acknowledge (HLDA) has been issued.

Additional Logic

In addition to the clock generator circuitry, the μPB8224 contains additional logic to aid the system designer in the proper timing of several interface signals.

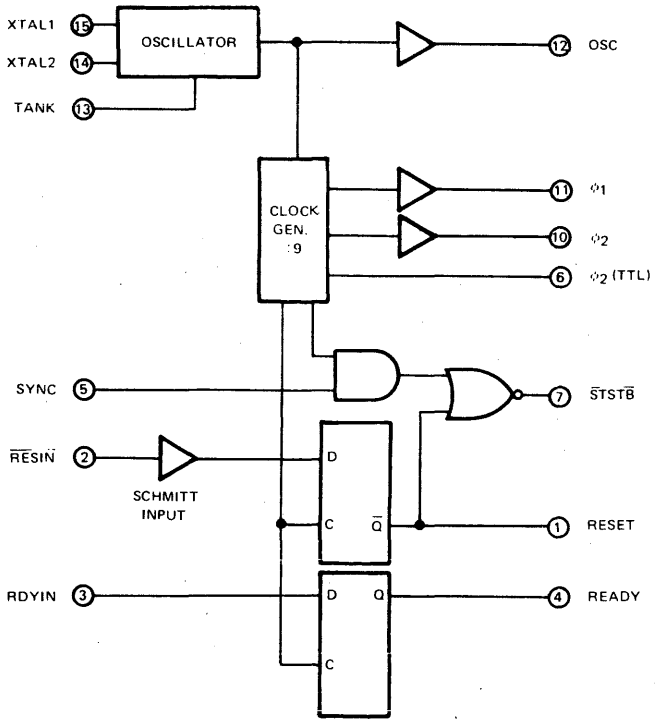
The $\overline{\text{STSTB}}$ signal indicates, at the earliest possible moment, when the status signals output from the 8080A processor are stable on the data bus. $\overline{\text{STSTB}}$ is designed to connect directly to the μPB8228 System Controller and automatically resets the μPB8228 during power-on Reset.

The $\overline{\text{RESIN}}$ input to the μPB8224 is used to automatically generate a RESET signal to the 8080A during power initialization. The slow rise of the power supply voltage in an external RC network is sensed by an internal Schmitt Trigger. The output of the Schmitt Trigger is gated to generate an 8080A compatible RESET. An active low manual switch may also be attached to the RC circuit for manual system reset.

The RDYIN input to the μPB8224 accepts an asynchronous "wait request" and generates a READY output to the 8080A that is fully synchronized to meet the 8080A timing requirements.

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output Voltages (TTL)	−0.5 to +7 Volts
All Output Voltages (MOS)	−1.0 to +13.5 Volts
All Input Voltages	−1.5 to +7 Volts
Supply Voltage V_{CC}	−0.5 to +7 Volts
Supply Voltage V_{DD}	−0.5 to +13.5 Volts
Output Currents	100 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ±5%; V_{DD} = +12V ±5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Current Loading	I_F			−0.25	mA	V_F = 0.45V
Input Leakage Current	I_R			10	μA	V_R = 5.25V
Input Forward Clamp Voltage	V_C			−1.0	V	I_C = −5 mA
Input "Low" Voltage	V_{IL}			0.8	V	V_{CC} = 5.0V
Input "High" Voltage	V_{IH}	2.6			V	Reset Input
		2.0				All Other Inputs
RESIN Input Hysteresis	V_{IH}-V_{IL}	0.25			V	V_{CC} = 5.0V
Output "Low" Voltage	V_{OL}			0.45	V	(ϕ_1, ϕ_2), Ready, Reset, STSTB
						I_{OL} = 2.5 mA
				0.45	V	All Other Inputs
						I_{OL} = 15 mA
Output "High" Voltage	V_{OH}					
ϕ_1, ϕ_2		9.4			V	I_{OH} = −100 μA
READY, RESET		3.6			V	I_{OH} = −100 μA
All Other Outputs		2.4			V	I_{OH} = −1 mA
Output Short Circuit Current (All Low Voltage Outputs Only)	I_{SC} ①	−10		−60	mA	V_O = 0V, V_{CC} = 5.0V
Power Supply Current	I_{CC}			115	mA	
Power Supply Current	I_{DD}			15	mA	

Note: ① Caution, ϕ_1 and ϕ_2 output drivers do not have short circuit protection

CAPACITANCE①

T_a = 25°C; f = 1 MHz; V_{CC} = 5V; V_{DD} = 12V; V_{BIAS} = 2.5V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			8	pF	

Note: ① This parameter is periodically sampled and not 100% tested.

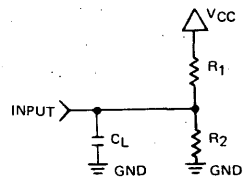
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AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ±5%; V_{DD} = +12V ±5%

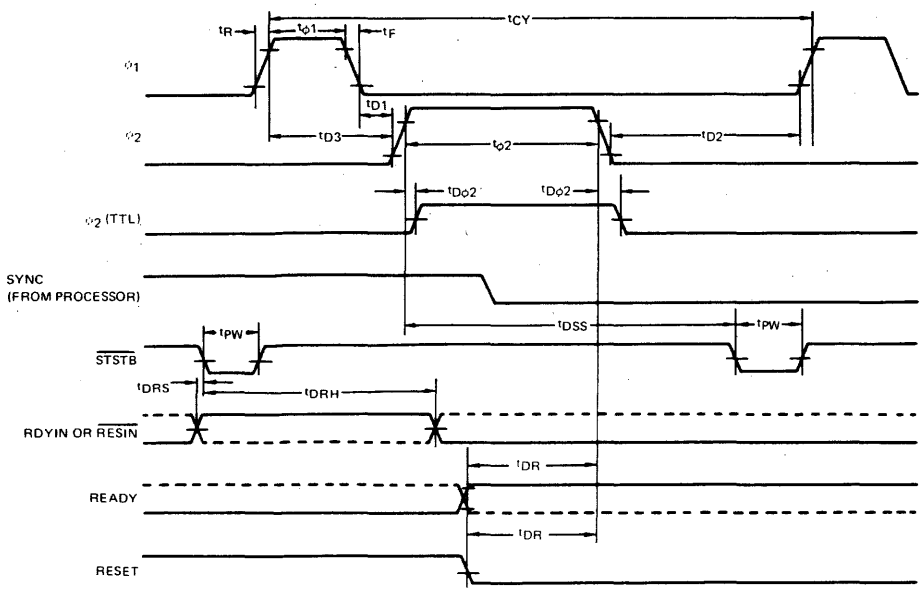
PARAMETER	SYMBOL	LIMITS ①			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
ϕ_1 Pulse Width	$t_{\phi 1}$	$\frac{2t_{CY}}{9}$ −20 ns			ns	C_L = 20 pF to 50 pF
ϕ_2 Pulse Width	$t_{\phi 2}$	$\frac{5t_{CY}}{9}$ −35 ns				
ϕ_1 to ϕ_2 Delay	t_{D1}	0				
ϕ_2 to ϕ_1 Delay	t_{D2}	$\frac{2t_{CY}}{9}$ −14 ns				
ϕ_1 to ϕ_2 Delay	t_{D3}	$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}$ +20 ns		
ϕ_1 and ϕ_2 Rise Time	t_R			20		
ϕ_1 and ϕ_2 Fall Time	t_F			20		
ϕ_2 to ϕ_2 (TTL) Delay	$t_{D\phi 2}$	−5		+15	ns	ϕ_2 TTL, CL = 30 pF R_1 = 300Ω R_2 = 600Ω
ϕ_2 to $\overline{STSTB}$ Delay	t_{DSS}	$\frac{6t_{CY}}{9}$ −30 ns		$\frac{6t_{CY}}{9}$	ns	$\overline{STSTB}$, CL = 15 pF R_1 = 2K R_2 = 4K
$\overline{STSTB}$ Pulse Width	t_{PW}	$\frac{t_{CY}}{9}$ −15 ns			ns	
RDYIN Setup Time to $\overline{STSTB}$	t_{DRS}	50 ns − $\frac{4t_{CY}}{9}$				
RDYIN Hold Time After $\overline{STSB}$	t_{DRH}	$\frac{4t_{CY}}{9}$				
READY or RESET to ϕ_2 Delay	t_{DR}	$\frac{4t_{CY}}{9}$ −25 ns			ns	Ready and Reset CL = 10 pF R_1 = 2K R_2 = 4K
Crystal Frequency	f_{CLK}		$\frac{9}{t_{CY}}$		MHz	
Maximum Oscillating Frequency	f_{MAX}			27	MHz	

Note: ① t_{CY} represents the processor clock period



TEST CIRCUIT

TIMING WAVEFORMS



Voltage Measurement Points: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V.
All other signals measured at 1.5V.

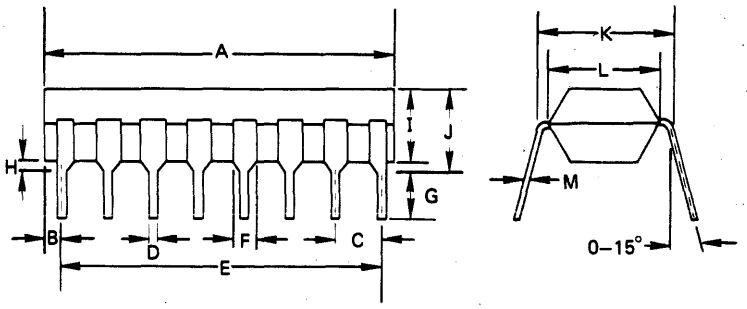
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CRYSTAL REQUIREMENTS

Tolerance	0.005% at 0°C–70°C
Resonance	Series (Fundamental) ①
Load Capacitance	20-35 pF
Equivalent Resistance	75-20 ohms
Power Dissipation (Min)	4 mW

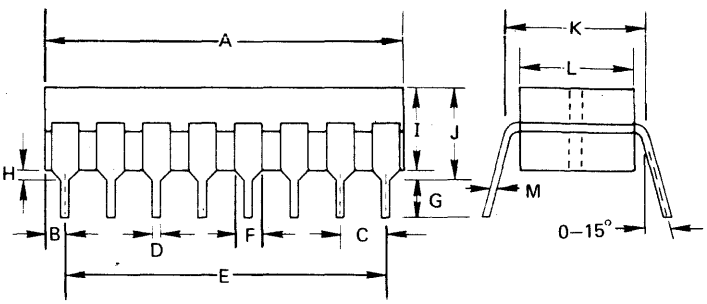
Note: ① With tank circuit use 3rd overtone mode.

PACKAGE OUTLINE μPB8224C/D



μPB8224C (Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{0.05}$	0.01



μPB8224D (Cerdip)

ITEM	MILLIMETERS	INCHES
A	19.9 MAX.	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{0.05}$	$0.0098^{+0.0039}_{0.0019}$

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8080A SYSTEM CONTROLLER AND BUS DRIVER

DESCRIPTION

The μPB8228/8238D is a single chip controller and bus driver for 8080A based systems. All the required interface signals necessary to connect RAM, ROM and I/O components to a μPD8080A are generated.

The μPB8228/8238D provides a bi-directional three-state bus driver for high TTL fan-out and isolation of the processor data bus from the system data bus for increased noise immunity.

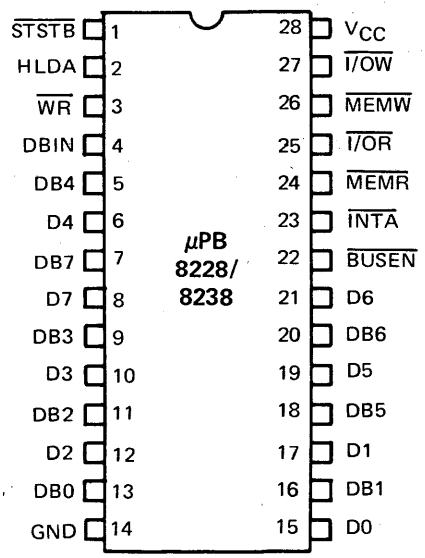
The system controller portion of the μPB8228/8238D consists of a status latch for definition of processor machine cycles and a gating array to decode this information for direct interface to system components. The controller can enable gating of a multi-byte interrupt onto the data bus or can automatically insert a RESTART 7 onto the data bus without any additional components.

Two devices are provided. The μPB8228D for small systems without tight write timing constraints and the μPB8238D for larger systems.

FEATURES

- System Controller for 8080A Systems
- Bi-Directional Data Bus for Processor Isolation
- 3.60V Output High Voltage for Direct Interface to 8080A Processor
- Three State Outputs on System Data Bus
- Enables Use of Multi-Byte Interrupt Instructions
- Generates RST 7 Interrupt Instruction
- μPB8228 for Small Memory Systems
- μPB8238 for Large Memory Systems
- Reduces System Package Count
- Schottky Bipolar Technology

PIN CONFIGURATION



NC: No Connection

PIN NAMES

D7-D0	Data Bus (Processor Side)
DB7-DB0	Data Bus (System Side)
$\overline{I/OR}$	I/O Read
$\overline{I/OW}$	I/O Write
$\overline{MEMR}$	Memory Read
$\overline{MEMW}$	Memory Write
DBIN	DBIN (From Processor)
$\overline{INTA}$	Interrupt Acknowledge
HLDA	HLDA (From Processor)
$\overline{WR}$	WR (From Processor)
$\overline{BUSEN}$	Bus Enable Input
$\overline{STSTB}$	Status Strobe (From μPB8224)
V_{CC}	+5V
GND	0 Volts

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FUNCTIONAL DESCRIPTION

Bi-Directional Bus Driver

The eight bit, bi-directional bus driver provides buffering between the processor data bus and the system data bus. On the processor side, the μPB8228/8238D exceeds the minimum input voltage requirements (3.0V) of the μPD8080A. On the system side, the driver is capable of adequate drive current (10 mA) for connection of a large number of memory and I/O devices to the bus. Signal flow in the bus driver is controlled by the gating array and its outputs can be forced into a high impedance state by use of the $\overline{\text{BUSEN}}$ input.

Status Latch

The Status Latch in the μPB8228/8238D stores the status information placed on the data bus by the 8080A at the beginning of each machine cycle. The information is latched when $\overline{\text{STSTB}}$ goes low and is then decoded by the gating array for the generation of control signals.

Gating Array

The Gating Array generates "active low" control signals for direct interfacing to system components by gating the contents of the status latch with control signals from the 8080A.

$\overline{\text{MEM/R}}$, $\overline{\text{I/OR}}$ and $\overline{\text{INTA}}$ are generated by gating the DBIN signal from the processor with the contents of the status latch. $\overline{\text{I/OR}}$ is used to enable an I/O input onto the system data bus. $\overline{\text{MEM/R}}$ is used to enable a memory input.

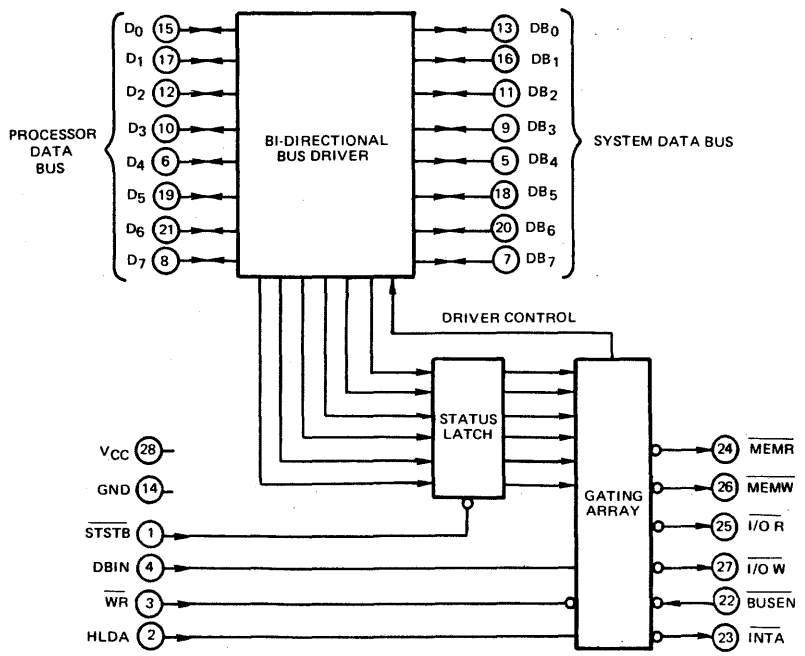
$\overline{\text{INTA}}$ is normally used to gate an interrupt instruction onto the system data bus. When used with the μPD8080A processor, the μPB8228/8238D will decode an interrupt acknowledge status word during all three machine cycles for a multi-byte interrupt instruction. For 8080A type processors that do not generate an interrupt acknowledge status word during the second and third machine cycles of a multi-byte interrupt instruction, the μPB8228/8238 will internally generate an $\overline{\text{INTA}}$ pulse for those machine cycles.

The μPB8228/8238D also provides the designer the ability to place a single interrupt instruction onto the bus without adding additional components. By connecting the +12 volt supply to the $\overline{\text{INTA}}$ output (pin 23) of the μPB8228/8238D through a 1K ohm series resistor, RESTART 7 will be gated onto the processor data bus when DBIN is active during an interrupt acknowledge machine cycle.

$\overline{\text{MEM/W}}$ and $\overline{\text{I/OW}}$ are generated by gating the $\overline{\text{WR}}$ signal from the processor with the contents of the status latch. $\overline{\text{I/OW}}$ indicates that an output port write is about to occur. $\overline{\text{MEM/W}}$ indicates that a memory write will occur.

The data bus output buffers and control signal buffers can be asynchronously forced into a high impedance state by placing a high on the $\overline{\text{BUSEN}}$ pin of the μPB8228/8238. Normal operation is performed with $\overline{\text{BUSEN}}$ low.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.5 to 5.5 Volts
Output Currents	100 mA

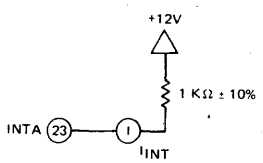
COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Input Clamp Voltage, All Inputs	V_C			−1.0	V	V_{CC} = 4.75V; I_{CC} = −5 mA
Input Load Current, $\overline{STSTB}$	I_F			500	μA	V_{CC} = 5.25V V_F = 0.45V
D_2 and D_6				750	μA	
D_0, D_1, D_4, D_5, and D_7				250	μA	
All Other Inputs				250	μA	
Input Leakage Current, $\overline{STSTB}$	I_R			100	μA	V_{CC} = 5.25V V_R = 5.0V
DB_0 through DB_7				20	μA	
All Other Inputs				100	μA	
Input Threshold Voltage, All Inputs	V_{TH}	0.8		2.0	V	V_{CC} = 5V
Power Supply Current	I_{CC}			190	mA	V_{CC} = 5.25V
Output Low Voltage, D_0 through D_7	V_{OL}			0.45	V	V_{CC} = 4.75V; I_{OL} = 2 mA
All Other Outputs				0.48	V	I_{OL} = 10 mA
Output High Voltage, D_0 through D_7	V_{OH}	3.6			V	V_{CC} = 4.75V; I_{OH} = −10 μA
All Other Outputs		2.4			V	I_{OH} = −1 mA
Short Circuit Current, All Outputs	I_{OS}	15		90	mA	V_{CC} = 5V
Off State Output Current, All Control Outputs	$I_{O(off)}$			100	μA	V_{CC} = 5.25V; V_O = 5.0V
				−100	μA	V_O = 0.45V
INTA Current	I_{INT}			5	mA	(See Figure below)



INTA TEST CIRCUIT

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			12	pF	V_{BIAS} = 2.5V,
Output Capacitance Control Signals	C_{OUT}			15	pF	V_{CC} = 5.0V,
I/O Capacitance (D or DB)	$C_{I/O}$			15	pF	f = 1 MHz

NOTE: This parameter is periodically sampled and not 100% tested.

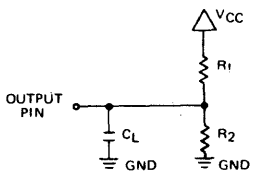
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AC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5V ± 5%

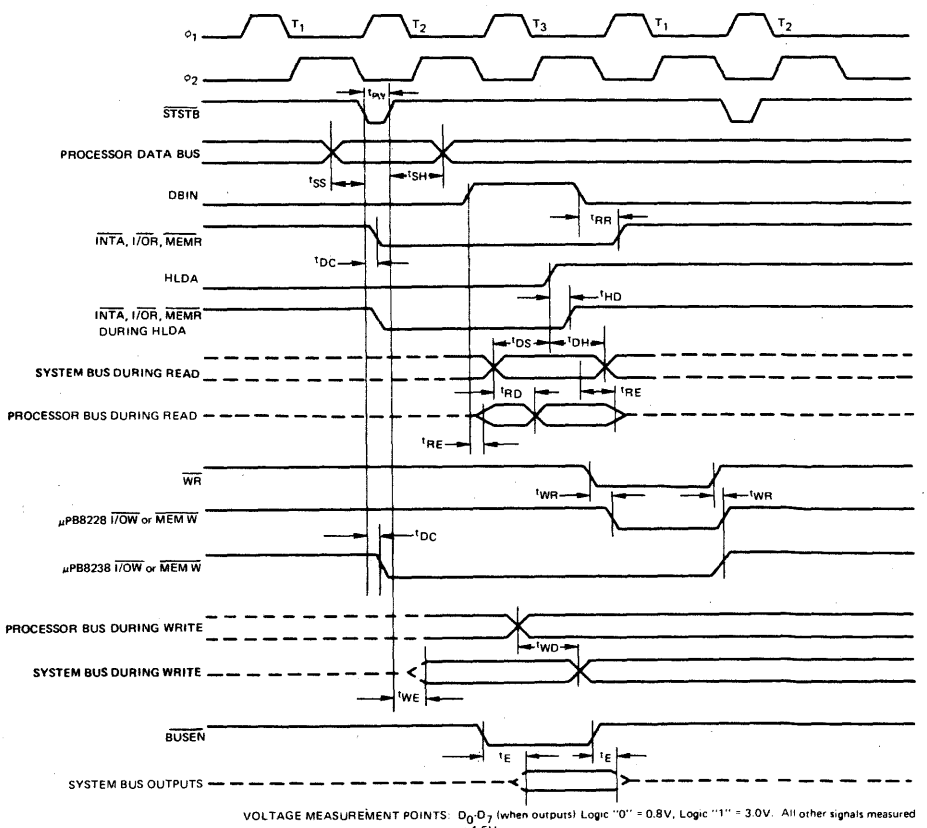
PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Width of Status Strobe	t_{PW}	22			ns	
Setup Time, Status Inputs D_0-D_7	t_{SS}	8			ns	
Hold Time, Status Inputs D_0-D_7	t_{SH}	5			ns	
Delay from $\overline{STSTB}$ to any Control Signal	t_{DC}	20		60	ns	C_L = 100 pF
Delay from DBIN to Control Outputs	t_{RR}			30	ns	C_L = 100 pF
Delay from DBIN to Enable/ Disable 8080A Bus	t_{RE}			45	ns	C_L = 25 pF
Delay from System Bus to 8080A Bus during Read	t_{RD}			30	ns	C_L = 25 pF
Delay from $\overline{WR}$ to Control Outputs	t_{WR}	5		45	ns	C_L = 100 pF
Delay to Enable System Bus DB_0-DB_7 after $\overline{STSTB}$	t_{WE}			30	ns	C_L = 100 pF
Delay from 8080A Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	t_{WD}	5		40	ns	C_L = 100 pF
Delay from $\overline{\text{System Bus Enable}}$ to System Bus DB_0-DB_7	t_E			30	ns	C_L = 100 pF
HLDA to Read Status Outputs	t_{HD}			25	ns	
Setup Time, System Bus Inputs to HLDA	t_{DS}	10			ns	
Hold Time, System Bus Inputs to HLDA	t_{DH}	20			ns	C_L = 100 pF

For D_0-D_7: R_1 = 4 KΩ, R_2 = ∞Ω, C_L = 25 pF. For all other outputs: R_1 = 500Ω, R_2 = 1 KΩ, C_L = 100 pF.



TEST CIRCUIT

TIMING WAVEFORMS



VOLTAGE MEASUREMENT POINTS: D_0-D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

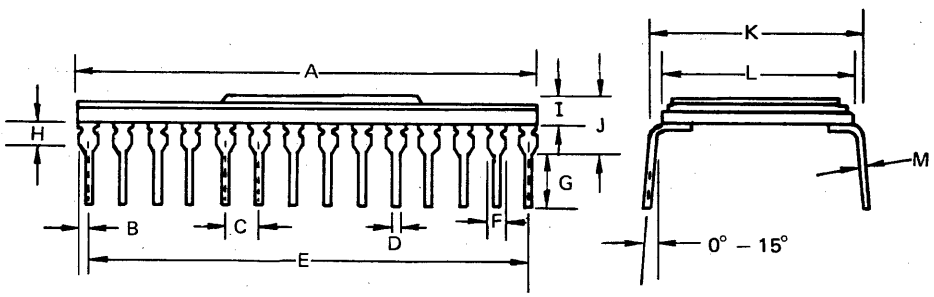
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STATUS WORD CHART

DATA BUS BIT	STATUS INFORMATION	INSTRUCTION FETCH	MEMORY READ	MEMORY WRITE	STACK READ	STACK WRITE	INPUT READ	OUTPUT WRITE	INTERRUPT ACKNOWLEDGE (M_1)	INT. ACK. (M_2, M_3)	HALT ACKNOWLEDGE	INT. ACK. WHILE HALT	
		(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	← (N) STATUS WORD
D_0	INTA	0	0	0	0	0	0	0	1	1	0	1	
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1	1	
D_2	STACK	0	0	0	1	1	0	0	0	0	0	0	
D_3	HLTA	0	0	0	0	0	0	0	0	0	1	0	
D_4	OUT	0	0	0	0	0	0	1	0	0	0	0	μPD8080A OUTPUT
D_5	M_1	1	0	0	0	0	0	0	1	0	0	1	
D_6	INP	0	0	0	0	0	1	0	0	0	0	0	
D_7	MEMR	1	1	0	1	0	0	0	0	0	0	0	
24	$\overline{MEMR}$	0	0	1	0	1	1	1	1	1	1	1	
26	$\overline{MEMW}$	1	1	0	1	0	1	1	1	1	1	1	μPB8228/8238 OUTPUT
25	$\overline{I/OR}$	1	1	1	1	1	0	1	1	1	1	1	
27	$\overline{I/OW}$	1	1	1	1	1	1	0	1	1	1	1	
23	$\overline{INTA}$	1	1	1	1	1	1	1	0	0	1	0	
PIN NO.		SIGNAL STATUS											
		μPB8228/8238 CONTROL SIGNALS											

PACKAGE OUTLINE μPB8228/8238D



ITEM	MILLIMETERS	INCHES
A	36.0 MAX.	1.42 MAX.
B	1.5 MAX.	0.59 MAX.
C	2.54	0.1
D	0.50 ± 0.1	0.02 ± 0.004
E	33.0	1.30
F	1.27	0.05
G	3.2 MIN.	0.13 MIN.
H	1.9	0.07
I	3.3 MAX.	0.13 MAX.
J	5.2 MAX.	0.20 MAX.
K	15.3	0.60
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

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MAGNETIC TAPE CASSETTE/ CARTRIDGE CONTROLLER

DESCRIPTION

The NEC μPD371 is a high performance N-Channel LSI tape cassette/cartridge controller designed to interface between most cassette or cartridge tape drives and most microprocessors or minicomputers.

The μPD371 converts 8-bit parallel data into serial phase encoded data to be written on tape and converts phase encoded data read from tape into 8-bit parallel data, calculates the CRC during write operations, verifies the CRC during read operations, informs the processor program when to send data bytes during write operations and when to read bytes during read operations, converts tape drive status signals into register bit levels which may be read by the processor program and converts software commands into signals which may be understood by the tape drive(s).

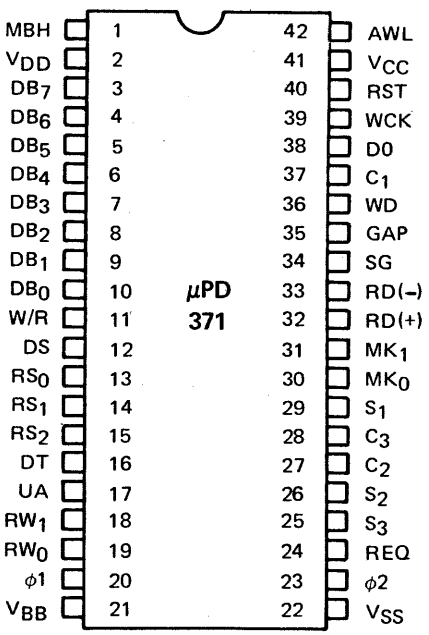
The μPD371 read and write data paths are completely separate to allow read-after-write data verification.

The μPD371 places no limitation on the selection of tape speed since the μPD371 maximum data transfer rate is considerably faster than that of the fastest cassette or cartridge drive.

FEATURES

- Compatible with ANSI, ECMA and ISO standard
- Also compatible with most other standards
- Hardware CRC generation and verification
- Read-after-write capability
- High speed file search
- Multiple drive capability
- May read or write on one drive while rewinding or file searching on another
- Maximum Data Transfer rate of 375K bits/sec equivalent to 468 IPS at 800 BPI

PIN CONFIGURATION



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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−40°C to +125°C
All Output Voltages	−1 to +8 Volts ①
All Input Voltages	−1 to +8 Volts ①
Clock Voltages	−1 to +16 Volts ①
Supply Voltage V_{DD}	−1 to +16 Volts ①
Supply Voltage V_{CC}	−1 to +8 Volts ①
Supply Voltage V_{BB}	−10 to 0 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

Note: ① V_{BB} = −5V ± 5%. All voltages measured with respect to GND.

DC CHARACTERISTICS

T_a = 0 − 70°C V_{DD} = +12V ± 5% V_{CC} = +5V ± 5% V_{BB} = −5V ± 5% V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	+3.0		V_{CC}	V	
Input Low Voltage	V_{IL}	0		+0.8	V	
Output High Voltage	V_{OH}	+3.5			V	I_{OH} = −1 mA
Output Low Voltage	V_{OL}			+0.4	V	I_{OL} = +1.7 mA
Clock Input High Voltage	V_{OH}	+9		V_{DD}	V	
Clock Input Low Voltage	V_{OL}	0		+0.65	V	
Input Leakage Current	I_{LIH}			+10	μA	V_I = +3.0V
Input Leakage Current: $DB_0 - DB_7$	$I_{LIL\,1}$			−10	μA	V_I = +0.8V
Input Leakage Current: All Except $DB_0 - DB_7$ (~25K Internal Pull-ups)	$I_{LIL\,2}$			−1.0	mA	V_I = +0.4V
Clock Input Leakage Current	I_{LOH}			+20	μA	V_O = +9.0V
Clock Input Leakage Current	I_{LOL}			−20	μA	V_O = +0.65V
Output Leakage Current	I_{LOH}			+10	μA	V_O = +3.5V
Output Leakage Current	I_{LOL}			−10	μA	V_O = +0.4V
Power Supply Current (V_{DD})	I_{DD}		+20		mA	
Power Supply Current (V_{CC})	I_{CC}		+30		mA	
Power Supply Current (V_{BB})	I_{BB}			−2	mA	

CAPACITANCE

T_a = 25°C, V_{DD} = V_{CC} = V_{SS} = 0V, V_{BB} = −5V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Capacitance	C_O			35	pF	fc = 1 MHz. All pins except measuring pin are grounded.
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

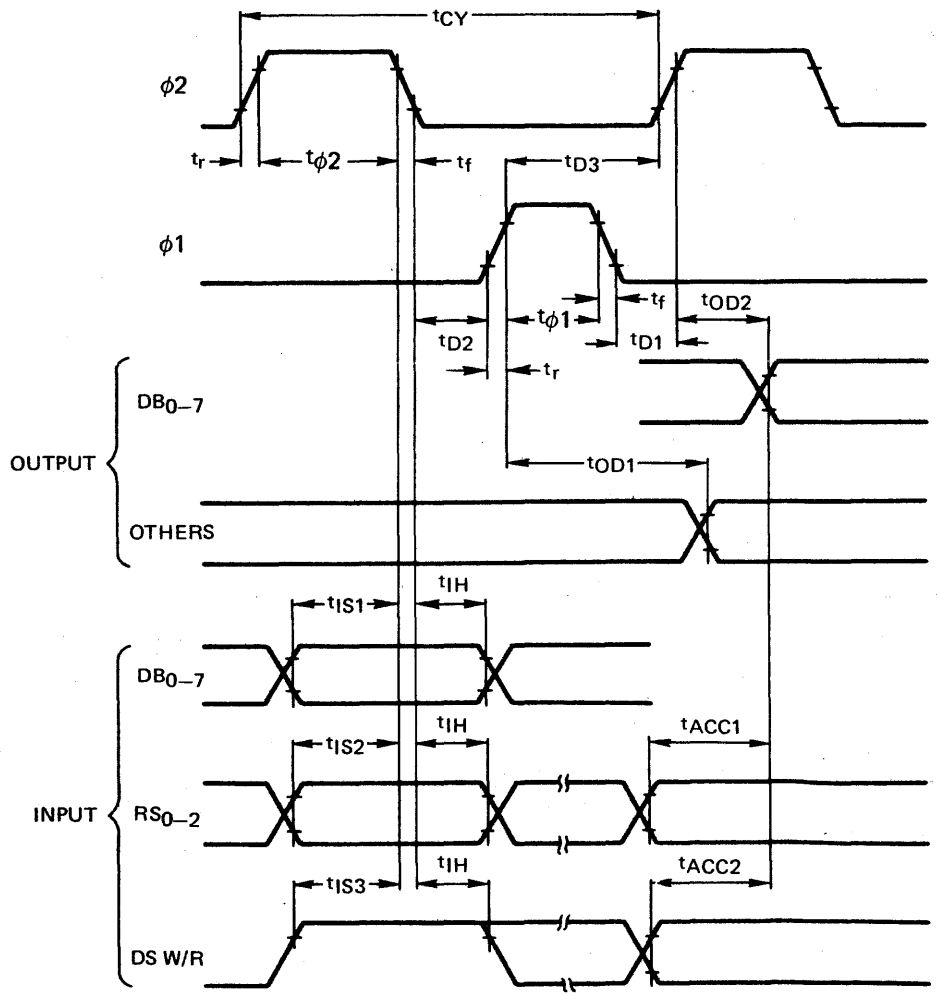
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AC CHARACTERISTICS

$T_a = 0 - 70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = CU$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Clock Period	t_{cy}	480		5000	ns	
Clock Rise and Fall Times	t_r, t_f	0		50	ns	
$\phi1$ Pulse Width	$t_{\phi1}$	60			ns	
$\phi2$ Pulse Width	$t_{\phi2}$	220			ns	
$\phi1$ to $\phi2$ Delay	t_{D1}	0			ns	
$\phi2$ to $\phi1$ Delay	t_{D2}	70			ns	
Delay $\phi1$ to $\phi2$ Lead Edges	t_{D3}	80			ns	
Data Out Delay from $\phi1$	t_{OD1}			480	ns	1TTL & CL = 30 pF
Data Out Delay from $\phi1$	t_{OD2}			260	ns	1TTL & CL = 30 pF
$RS_0 - RS_2$ to Output Delay	t_{ACC1}			300	ns	1TTL & CL = 30 pF
DS, W/R to Output Delay	t_{ACC2}			200	ns	1TTL & CL = 30 pF
$DB_0 - DB_7$ to $\phi2$ Setup Time	t_{IS1}	250			ns	
$RS_0 - RS_2$ to $\phi2$ Setup Time	t_{IS2}	350			ns	
DS, W/R to $\phi2$ Setup Time	t_{IS3}	150			ns	
Input Hold Time from $\phi2$	t_{IH}	30			ns	

TIMING WAVEFORMS



Note: Timing Measurement Levels:
Clock High/Low Voltage = 9.0V/0.65V
Input High/Low Voltage = 3.0V/0.8V
Output High/Low Voltage = 2.0V/0.8V

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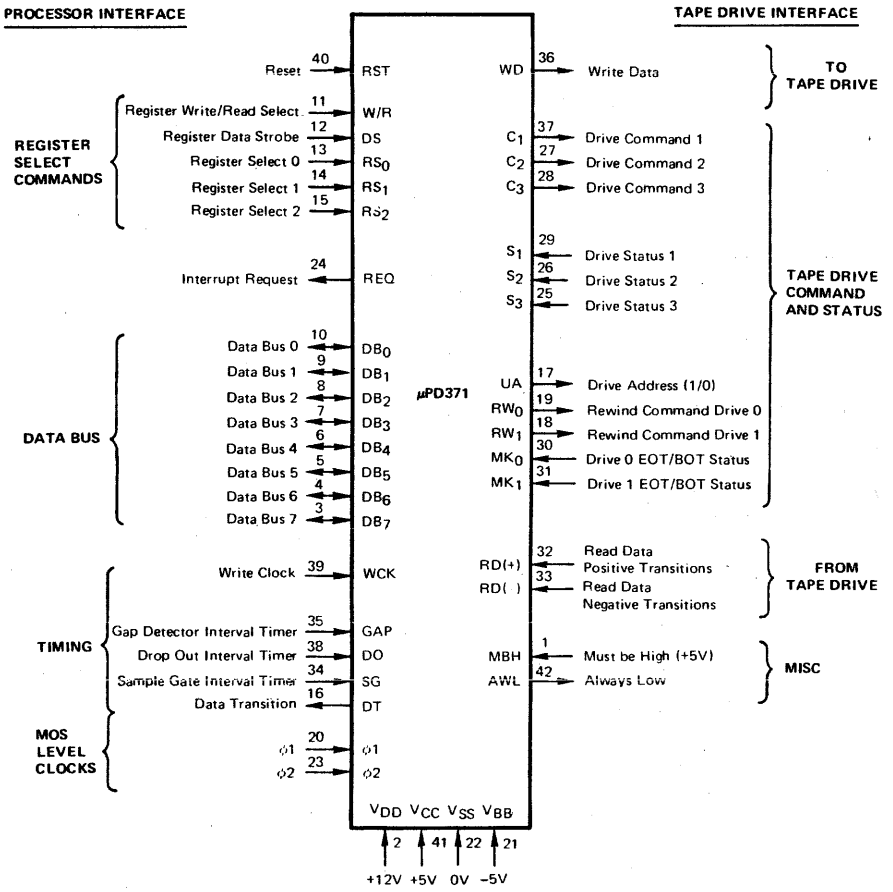
PIN IDENTIFICATION①

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
RESET			
40	RST	Reset	A logic one at this pin causes a general reset of the μPD371.
REGISTER SELECT COMMANDS AND DATA BUS			
11	W/R		W/R, DS and $RS_0 - RS_2$ control Data Bus transfers between the μPD371 and the processor as follows: Writing into a μPD371 register: When W/R is a logic one, information the processor places on $DB_0 - DB_7$ is written into the μPD371 WRITE REGISTER selected by $RS_0 - RS_2$. The information is strobed into the register by a logic one at DS. Reading from a μPD371 register: When W/R is a logic zero, information from the μPD371 READ REGISTER selected by $RS_0 - RS_2$ is placed on $DB_0 - DB_7$ to be read by the processor. The information remains on $DB_0 - DB_7$ as long as DS is a logic one.
12	DS		
13 – 15	$RS_0 - RS_2$		
3 – 10	$DB_0 - DB_7$	Data Bus	
INTERRUPT REQUEST			
24	REQ		The μPD371 may be operated with either interrupt or polling techniques. If the interrupt technique is chosen, REQ should be connected to the interrupt request input of the processor. There are three sources of interrupt: READ BUFFER FULL, WRITE BUFFER EMPTY and GAP DETECTION.
TIMING			The user must provide four timing signals to the μPD371 — one for write operations and three for read operations. Each is defined in terms of T, where T is the period between successive data transitions in the phase encoded data written onto or read from tape.
39	WCK		WCK determines the WRITE DATA (WD, pin 36) transfer rate. WCK should have a period of 0.5T. DT is a pulse provided by the μPD371 to be used in the generation of the three read timing signals — SG, DO, and GAP. DT occurs at each data transition in the data read from tape. The internal read data sample gate is closed following each data transition and is reopened by a positive transition at SG 0.75T μsec after each DT pulse. A positive transition should be made at DO whenever a DT pulse stream ceases for a period of 1.5T μsec. A positive transition should be made at GAP whenever a DT pulse stream ceases for a period of 4T μsec. $\phi 1$ and $\phi 2$ are MOS level (12V) clock pulses. The timing of $\phi 1$ and $\phi 2$ is shown in the Timing Diagram.
16	DT		
34	SG		
38	DO		
35	GAP		
20	$\phi 1$		
23	$\phi 2$		
WRITE DATA			
36	WD		Phase encoded data to be written on tape leaves the μPD371 at pin 36.
TAPE DRIVE COMMAND AND STATUS			
37	C_1		C_1, C_2 and C_3 are general purpose tape drive commands. C_1, C_2 and C_3 are set and reset by the software manipulation of bits 5, 6 and 7, respectively, in Write Register 3. Since C_1, C_2 and C_3 are defined by software, they may be configured for any purpose. Typical uses for C_1, C_2 and C_3 are WRITE ENABLE, FORWARD and REVERSE.
27	C_2		
28	C_3		
29	S_1		S_1, S_2 and S_3 are general purpose tape drive status inputs. Their logic levels are indicated by bits 3, 4 and 7 of Read Register 1, respectively. Typical tape drive status signals are WRITE PERMIT, CASSETTE IN PLACE and SIDE. The μPD371 can adapt to any tape drive status signal set with a slight change in software.
26	S_2		
25	S_3		
DUAL TAPE DRIVE SYSTEM COMMAND AND STATUS			
17	UA	Unit Address	Selects Drive 0 when low and Drive 1 when high.
19	RW_0	Rewind 0	Rewind Command for Drive 0.
18	RW_1	Rewind 1	Rewind Command for Drive 1.
30	MK_0	Marker 0	EOT/BOT status from Drive 0.
31	MK_1	Marker 1	EOT/BOT status from Drive 1.
READ DATA			
32	RD(+)	Read Data (+)	A positive pulse from the tape drive at each positive transition in the read data.
33	RD(–)	Read Data (–)	A positive pulse from the tape drive at each negative transition in the read data.
MISCELLANEOUS			
1	MBH		MBH must be tied to the V_{CC} (+5V) supply.
42	AWL		AWL is a logic low output under all normal operating conditions of the μPD371.
POWER SUPPLY VOLTAGES			
2	V_{DD}		+12V
41	V_{CC}		+5V
22	V_{SS}		Ground
21	V_{BB}		–5V

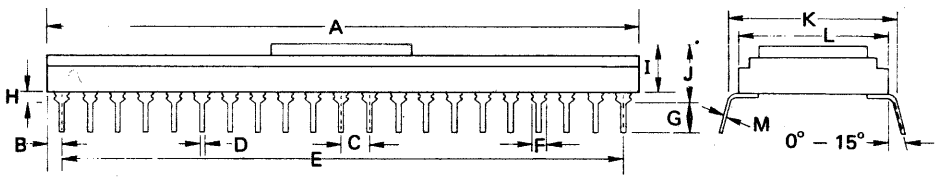
Note: ① Refer to diagram on following page.

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PIN IDENTIFICATION (CONT.)



PACKAGE OUTLINE μPD371



ITEM	MILLIMETERS	INCHES
A	53.5 MAX	2.1 MAX
B	1.35	0.05
C	2.54	0.10
D	50.80	2.0
F	1.27	0.05
G	2.54 MAX	0.10 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.21 MAX
K	15.24	0.60
L	13.50	0.53
M	0.3	0.012

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ADDRESSABLE INTERNAL REGISTERS

From the point of view of the processor program, the μPD371 makes the tape drive (or multiple drive system) appear as ten addressable registers. The program controls the drive(s) and transmits data to be written on tape by manipulating bits in the six μPD371 Write Registers. The program senses the status of the drive(s) and reads data stored on tape by reading bits from the four μPD371 Read Registers.

REGISTER ADDRESS				REGISTER NAME	BIT NUMBERS							
W/R	RS_2	RS_1	RS_0		7	6	5	4	3	2	1	0
				WRITE REGISTERS								
1	0	0	0	WR_0	RST	MBL	SRS	WME	WCR	X	WMD	GNT
1	0	0	1	WR_1	WRR	RRR	X	RRE	RRD	GRE	GRD	X
1	0	1	0	WR_2	WD_7	WD_6	WD_5	WD_4	WD_3	WD_2	WD_1	WD_0
1	0	1	1	WR_3	C_3	C_2	C_1	RRI	RW	X	X	X
1	1	0	1	WR_5	X	X	X	RME	RMD	X	X	X
1	1	1	0	WR_6	X	X	X	X	X	X	X	UA
				READ REGISTERS								
0	0	0	0	RR_0	AWH	AWL	C_2	C_3	RDF	GRQ	WRQ	RRQ
0	0	0	1	RR_1	S_3	MK	MKF	S_2	S_1	RW	C_1	UA
0	0	1	0	RR_2	RD_7	RD_6	RD_5	RD_4	RD_3	RD_2	RD_1	RD_0
0	0	1	1	RR_3	WD	GPF	REC	CRE	DOE	COR	NBR	NAR

X = NOT USED

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ADDRESSABLE INTERNAL REGISTER BIT IDENTIFICATION

BIT	SYMBOL	NAME
WRITE REGISTER 0		
0	GNT	Gap Noise Tolerance
1	WMD	Write Mode Disable
2	–	Not used
3	WCR	Write CRC
4	WME	Write Mode Enable
5	SRS	Status Reset
6	MBL	Must Be Low
7	RST	Reset
WRITE REGISTER 1		
0	–	Not used
1	GRD	Gap Request Disable
2	GRE	Gap Request Enable
3	RRD	Read Request Disable
4	RRE	Read Request Enable
5	–	Not used
6	RRR	Read Request Reset
7	WRR	Write Request Reset
WRITE REGISTER 2		
0 – 7	WD_0 – WD_7	Write Buffer Register
WRITE REGISTER 3		
0	–	Not used
1	–	Not used
2	–	Not used
3	RW	Rewind
4	RRI	Rewind Reset Inhibit
5	C_1	Command One
6	C_2	Command Two
7	C_3	Command Three
WRITE REGISTER 4		
–	–	Not used
WRITE REGISTER 5		
0	–	Not used
1	–	Not used
2	–	Not used
3	RMD	Read Mode Disable
4	RME	Read Mode Enable
5	–	Not used
6	–	Not used
7	–	Not used

BIT	SYMBOL	NAME
WRITE REGISTER 6		
0	UA	Unit Address
1 – 7	–	Not used
READ REGISTER 0		
0	RRQ	Read Request
1	WRQ	Write Request
2	GRQ	Gap Request
3	RDF	Read Flag
4	C_3	Command 3
5	C_2	Command 2
6	AWL	Always Low
7	AWH	Always High
READ REGISTER 1		
0	UA	Unit Address
1	C_1	Command 1
2	RW	Rewind
3	S_1	Status 1
4	S_2	Status 2
5	MKF	Marker Flag
6	MK	Marker
7	S_3	Status 3
READ REGISTER 2		
0 – 7	RD_0 – RD_7	Read Buffer Register
READ REGISTER 3		
0	NAR	Noise After Record
1	NBR	Noise Before Record
2	COR	Command Overrun
3	DOE	Drop Out Error
4	CRE	CRC Error
5	REC	Record Detection
6	GPF	Gap Flag
7	WD	Write Data

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FLOPPY DISK CONTROLLER

DESCRIPTION

The μPD372D is a single LSI floppy disk controller chip which contains the circuitry to read, write, track seek, load and unload the head, generate and detect CRC characters, and perform all other floppy disk operations. It is completely compatible with the IBM, Minifloppy*TM, hard sector, and other formats and controls up to 4 floppy disk drives. The μPD372D may be interfaced directly to a host processor; or to a controller processor first, which in turn is interfaced to the host. These processors do not necessarily have to be of the 8080A type.

Data transfers to and from the μPD372D are done through addressable internal registers. These internal regsiters allow a large variety of system architectures to be configured; they provide status information on the drive, as well as perform data transfers between the drive and the processor.

The μPD372D issues interrupts to the processor upon detection of an address mark and then when each subsequent data byte is available during either reading or writing. An 8-bit bi-directional data bus and 5 register select lines provide access to the 9 internal registers' contents. An internal interval timer is provided which facilitates performing such drive timing functions as: stepping rate, head settling time, track settling time, etc.

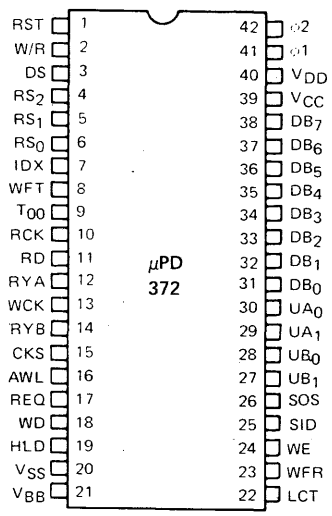
*TMShugart Associates.

FEATURES

- Compatible with IBM 3740 format
- Also compatible with other formats including Minifloppy and hard sector
- Controls up to four floppy disk drives
- Can perform overlap seeks
- Input and output TTL compatible (except for $\phi 1$ and $\phi 2$)
- Interfaces to most microprocessors including 8080A
- Standard power supplies (+12V, +5V and –5V)
- Controls most floppy disk drives including:

CALCOMP 140, 142	ORBIS 74, 76/77
CDC BR803	PERSCI 70, 75
INNOVEX 210, 410	REMEX RFS 7400
PERTEC FD400	SHUGART SA400 (Minifloppy)
POTTER DD4740	WANGCO 82 (Minifloppy)
SHUGART SA900, SA800	GSI MDD50 (Minifloppy)
GSI 110	

PIN CONFIGURATION



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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70°C
Storage Temperature	-40°C to +125°C
All Output Voltages	-1.0 to +8 Volts①
All Input Voltages	-1.0 to +8 Volts①
Clock Voltage	-1.0 to +16 Volts①
Supply Voltage V_{DD}	-1.0 to +16 Volts①
Supply Voltage V_{CC}	-1.0 to +8 Volts①
Supply Voltage V_{BB}	-10 to +0 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

Note: ① $V_{BB} = -5V \pm 5\%$

DC CHARACTERISTICS

$T_a = -70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
High Level Input Voltage	V_{IH}	+3.0		V_{CC}	V	
Low Level Input Voltage	V_{IL}	0		+0.8	V	
High Level Output Voltage	V_{OH}	+3.5			V	$I_{OH} = -1.0$ mA
Low Level Output Voltage	V_{OL1}①			+0.5	V	$I_{OL} = +1.7$ mA
	V_{OL2}②			+0.5	V	$I_{OL} = +3.3$ mA
High Level Clock Voltage	$V_{\phi H}$	+9		V_{DD}	V	
Low Level Clock Voltage	$V_{\phi L}$	0		+0.8	V	
High Level Input Leakage Current	I_{LIH}			+10	μA	$V_I = +3.0V$
Low Level Input Leakage Current	I_{LIL}			−10	μA	$V_I = +0.8V$
High Level Clock Leakage Current	$I_{L\phi H}$			+10	μA	$V_\phi = +9.0V$
Low Level Clock Leakage Current	$I_{L\phi L}$			−10	μA	$V_\phi = +0.8V$
High Level Output Leakage Current	I_{LOH}			+10	μA	$V_O = +3.5V$
Low Level Output Leakage Current	I_{LOL}			−10	μA	$V_O = +0.5V$
Power Supply Current (V_{DD})	I_{DD}		+20		mA	
Power Supply Current (V_{CC})	I_{CC}		+23		mA	
Power Supply Current (V_{BB})	I_{BB}			−2	mA	

Notes: ① CKS, REQ, UA_0, UA_1, UB_0, UB_1, DB_0–DB_7.
② WD, HLD, LCT, WE, WFR, SOS, SID.

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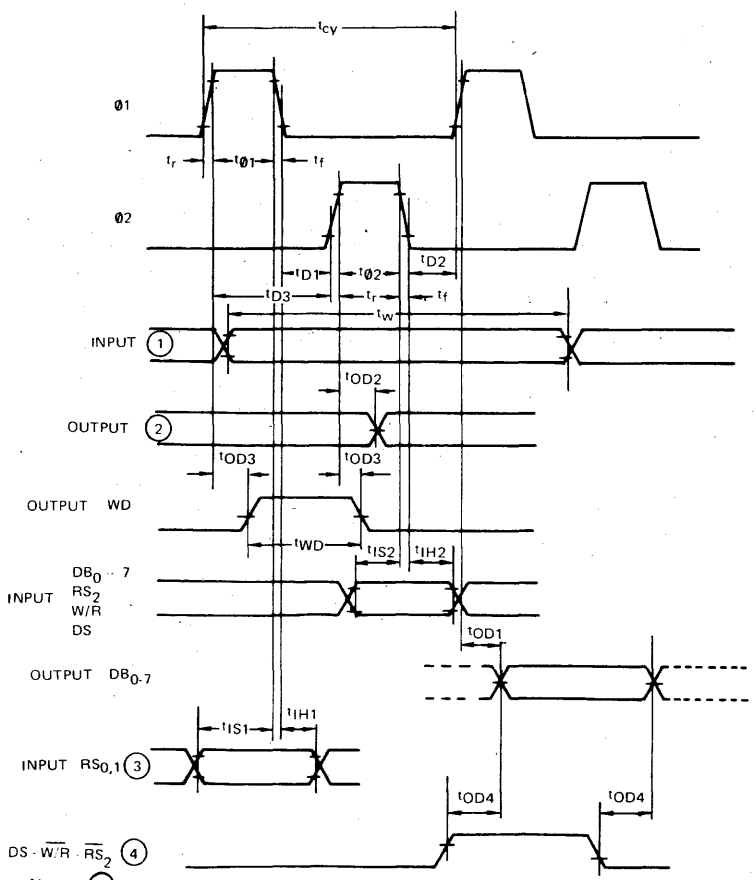
AC CHARACTERISTICS

T_a = 0 −70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY}	480		2000	ns	
Clock Rise and Fall Times	t_r, t_f	0		50	ns	
ϕ_1 Pulse Width	$t_{\phi 1}$	60			ns	
ϕ_2 Pulse Width	$t_{\phi 2}$	90			ns	
ϕ_1 to ϕ_2 Delay	t_{D_1}	0			ns	
ϕ_2 to ϕ_1 Delay	t_{D_2}	70			ns	
Delay ϕ_1 to ϕ_2 Leading Edges	t_{D_3}	100			ns	
Data Out Delay from ϕ_1	T_{OD_1}			90	ns	1 TTL and C_i = 30 pF
Data Out Delay from ϕ_2 ①	t_{OD_2}			200	ns	1 TTL and C_i = 30 pF
Data Out Delay from ϕ_2 ②	t_{OD_2}			200	ns	2 TTL and C_i = 50 pF
WD Delay Time	t_{OD_3}			120	ns	2 TTL and C_i = 50 pF
Data Out Delay from DS · $\overline{W/R}$ · $\overline{RS_2}$	t_{OD_4}			200	ns	
Data Setup Time to ϕ_1	t_{IS_1}	150			ns	
Data Setup Time to ϕ_2	t_{IS_2}	120			ns	
Data Hold Time from ϕ_1	t_{IH_1}	10			ns	
Data Hold Time from ϕ_2	t_{IH_2}	10			ns	
WD pulse width	t_{WD}	t_{D3}-40	t_{D_3}		ns	
Input pulse width ③	t_W	t_{CY}+150			ns	

Notes: ① CKS, AWL, REQ, UA_0, UA_1, UB_0, UB_1
② HLD, LCT, WFR, WE, SOS, SID.
③ IDX, RYA, RYB, RST, WFT, T_{00}, WCK, RCK.

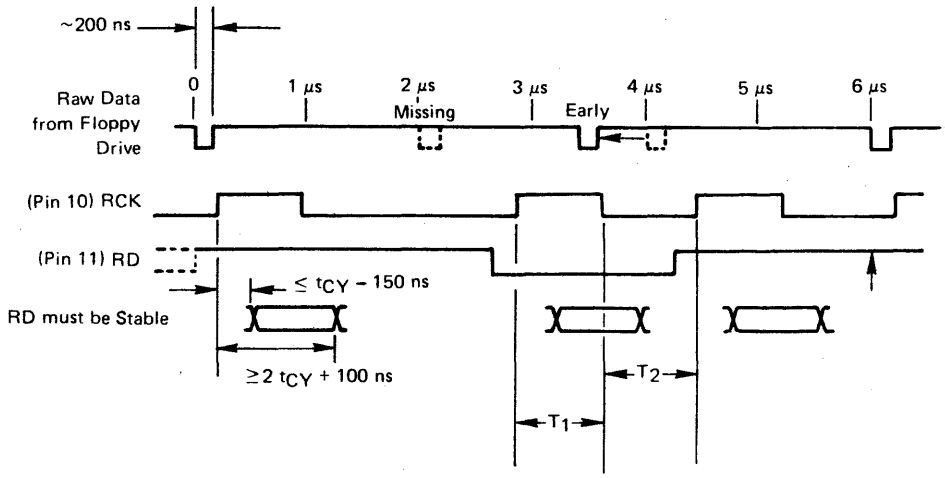
TIMING WAVEFORMS



Notes: ① IDX, RYA, RYB, RST, WFT, T_{OO}, WCK, RCK.
② CKS, WFR, SOS, SID, REQ, HLD, $UA_{\phi,1}$, $UB_{\phi,1}$, WE, LCT.
③ RS_O, RS_1 input must not make level transition within t_{IS1} and t_{IH1} times, or register contents may be modified.
④ The logic condition which places μPD372 information on DB_{0-7} is DS · $\overline{W/R}$ · $\overline{RS_2}$. Care must be taken to insure that this condition is not met inadvertently if DS, W/R and RS_2 are allowed to change state asynchronously.

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READ CLOCK (RCK) AND READ DATA (RD) REQUIRED BY μPD372



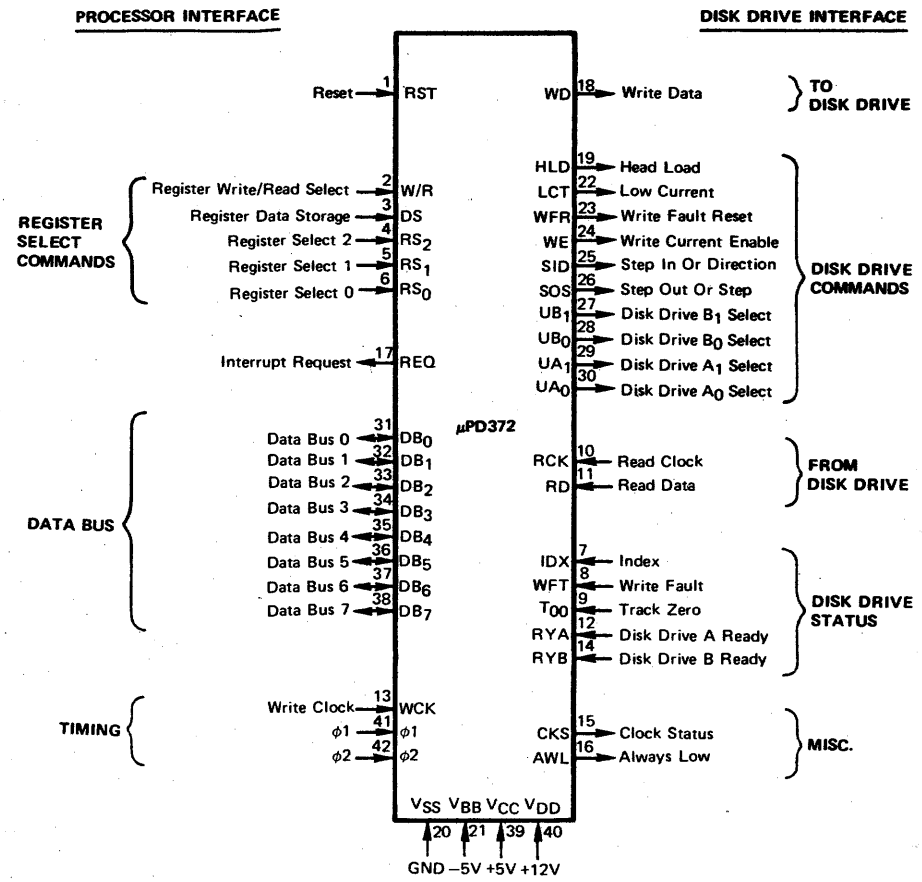
Notes: ① $t_{CY} = \phi 1$ Clock Period
② $T_1 \geq t_{CY} + 160$ ns
③ $T_2 \geq t_{CY} + 160$ ns

PIN IDENTIFICATION

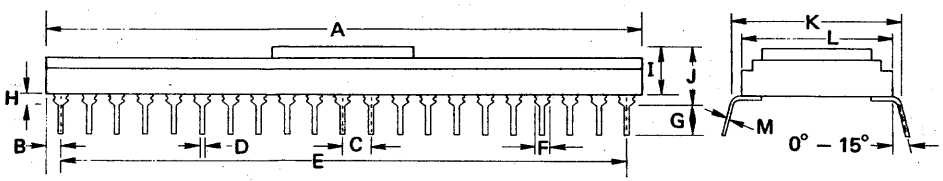
PIN NO.	PIN SYMBOL	PIN NAME	INPUT/ OUTPUT	CONNECTION	FUNCTION
1	RST	Reset	Input	Processor	Initializes internal registers, counters and F/F's
2	W/R	Register Write/ Read Select			W/R = 1 implies DB_{0-7} data written into μPD372 registers
3	DS	Data Strobe			DB_{0-7} Write and read strobe
4-6	RS_ϕ RS_1 RS_2	Register Select			Internal Register Select
7	IDX	Index		FDD	Pulse Signal that indicates start of Disk track
8	WFT	Write Fault			Write Fault Signal
9	T_{00}	Track 00			Indicates that Head is positioned on Track 00
10	RCK	Read Clock			
11	RD	Read Data			
12	RYA	Ready A			Indicates that FDD A is Ready
13	WCK	Write Clock		Processor	
14	RYB	Ready B		FDD	Indicates that FDD B is Ready
15	CKS	Clock States	Output		
16	AWL	Always Low			Always a logic zero
17	REQ	Request		Processor	Interrupt Request
18	WD	Write Data		FDD	Serial Write Data (Clock & Data Bits)
19	HLD	Head Load			Command which causes R/W head to contact disk
22	LCT	Low Current			Command to lower write current for inner tracks
23	WFR	Write Fault Reset			Signal to reset write fault latch
24	WE	Write Enable			
25	SID	Step In or Direction			R/W head step control
26	SOS	Step Out or Step			R/W head step control
27-30	UA_0, UA_1 UB_0, UB_1	FDD Select			FDD Unit Select
31-38	DB_{0-7}	Data Bus	Input/ Output	Processor	Bi-directional data bus

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PIN IDENTIFICATION (CONT.)



PACKAGE OUTLINE μPD372D



ITEM	MILLIMETERS	INCHES
A	53.5 MAX	2.1 MAX
B	1.35	0.05
C	2.54	0.10
D	50.80	2.0
F	1.27	0.05
G	2.54 MAX	0.10 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.21 MAX
K	15.24	0.60
L	13.50	0.53
M	0.3	0.012

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INTERNAL REGISTER IDENTIFICATION

BIT	SYMBOL	NAME	FUNCTION
		WRITE REGISTER 0	
0		Not Used	
1	WFR	Write Fault Reset	Resets Pin 23 to Zero
2	LCT	Low Current	Sets Pin 22, Should be Zero for TRKS > 43
3	HLD	Head Load	Sets Pin 19, Loading FDD Head
4		Not Used	
5		Not Used	
6	MBL	Must Be Low	
7	RST	Reset	Software Reset, Same Effect as Pin 1
		WRITE REGISTER 1	
0	UA_0	Unit A_0 Select	Device Select Pin 30
1	UA_1	Unit A_1 Select	Device Select Pin 29
2	UAS	Unit A Strobe	Strobe for Enabling UA_0 and OA_1 to be Loaded
3	CB_3	Clock Bit 3	Enables Clock Pulse #3 to be Written
4	CB_4	Clock Bit 4	Enables Clock Pulse #4 to be Written
5	CB_5	Clock Bit 5	Enables Clock Pulse #5 to be Written
6		Not Used	
7	CBS	Clock Bit Strobe	Enables Clock Bits to be Loaded
		WRITE REGISTER 2	
0	WD_0	Write Data Bit 0	
1	WD_1	Write Data Bit 1	
2	WD_2	Write Data Bit 2	
3	WD_3	Write Data Bit 3	
4	WD_4	Write Data Bit 4	
5	WD_5	Write Data Bit 5	
6	WD_6	Write Data Bit 6	
7	WD_7	Write Data Bit 7	
		WRITE REGISTER 3	
0	CCW	Cyclic Check Words	One During R/W, Zero for CRC Reset
1	CCG	Cyclic Check Generator Start	Starts CRC Generator in Write Mode
2	WER	Write Enable Reset	Resets Pin 24 to Zero
3	IXS	Index Start	Enable Index Hole Detection
4	WES	Write Enable Set	Sets Pin 24 to One
5	STT	Start	Enables Read and Write Operations to Occur
6	WCS	Write Clock Set	Write Clock Selected
7	RCS	Read Clock Set	Read Clock Selected
		WRITE REGISTER 4	
0	UB_0	Unit B_0 Select	Device Select Pin 28
1	UB_1	Unit B_1 Select	Device Select Pin 27
2	UBS	Unit B Strobe	Strobe for Enabling UB_0, UB_1 to be Loaded
3		Not Used	
4		Not Used	
5	SOS	Step Out or Step	Sets Pin 26 to One
6	SID	Step In or Direction	Sets Pin 25 to One
7	STS	Step Strobe	Enables SOS and SID to be Loaded
		WRITE REGISTER 5	
0–7		This Register Not Used	
		WRITE REGISTER 6	
0	DRR	Data Register Reset	Resets DRQ (RR_0 Bit 0)
1	IRR	Index Request Reset	Resets IRQ (RR_0 Bit 1)
2	TRR	Timer Request Reset	Resets TRQ (RR_0 Bit 2)
3		Not Used	
4		Not Used	
5		Not Used	
6		Not Used	
7		Not Used	

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INTERNAL REGISTER IDENTIFICATION (CONT.)

BIT	SYMBOL	NAME	FUNCTION
		READ REGISTER 0	
0	DRQ	Data Request	Read Data Byte from RR_2 or Write Data Byte into WR_2
1	IRQ	Index Request	Set by Physical Index Pulse
2	TRQ	Timer Request	Set by Every 512th Write CLK Pulse
3	ERR	Error	Logical OR of WFT + RYA + COR
4	UB_0	Drive B_0 Selected	
5	UB_1	Drive B_1 Selected	
6	RYB	Drive B Ready	Ready Signal from Pin 14
7	ALH	Always High	Always Contains a Logical One
		READ REGISTER 1	
0	UA_0	Drive A_0 Selected	
1	UA_1	Drive A_1 Selected	
2	WFT	Write Fault	Indicates Status of Pin 8
3	RYA	Drive A Ready	Indicates Status of Pin 12
4	COR	Command Overrun	Processor Did Not Respond in Time to a DRQ
5	DER	Data Error	CRC Error During Read
6	T_{00}	Track Zero	Indicates Status of Pin 9
7	WRT	Write Mode	Indicates which Clock WCK or RCK has been Selected
		READ REGISTER 2	
0	RD_0	Read Data Bit 0	
1	RD_1	Read Data Bit 1	
2	RD_2	Read Data Bit 2	
3	RD_3	Read Data Bit 3	
4	RD_4	Read Data Bit 4	
5	RD_5	Read Data Bit 5	
6	RD_6	Read Data Bit 6	
7	RD_7	Read Data Bit 7	

ADDRESSABLE INTERNAL REGISTERS

Data is transferred to the μPD372's internal addressable registers by signals W/R (Write=1, Read=0), DS (Data Strobe) and RS_0–RS_2 (Register Select 0, 1 and 2). Timing constraints for these signals are shown in the Timing Diagram. Diagram below shows register allocations and functional content.

REGISTER ADDRESS				REGISTER NAME	BIT NUMBERS							
W/R	RS_2	RS_1	RS_0		7	6	5	4	3	2	1	0
				WRITE REGISTERS								
1	0	0	0	WR_0	RST	MBL	X	X	HLD	LCT	WFR	X
1	0	0	1	WR_1	CBS	X	CB_5	CB_4	CB_3	UAS	UA_1	UA_0
1	0	1	0	WR_2	WD_7	WD_6	WD_5	WD_4	WD_3	WD_2	WD_1	WD_0
1	0	1	1	WR_3	RCS	WCS	STT	WES	TXS	WER	CCG	CCW
1	1	0	0	WR_4	STS	SID	SOS	X	X	UBS	UB_1	UB_0
1	1	1	0	WR_6	X	X	X	X	X	TRR	IRR	DRR
				READ REGISTERS								
0	0	0	0	RR_0	ALH	RYB	UB_1	UB_0	ERR	TRQ	IRQ	DRQ
0	0	0	1	RR_1	WRT	T_{00}	DER	COR	RYA	WFT	UA_1	UA_0
0	0	1	0	RR_2	RD_7	RD_6	RD_5	RD_4	RD_3	RD_2	RD_1	RD_0

X = NOT USED

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SYNCHRONOUS RECEIVER/TRANSMITTER

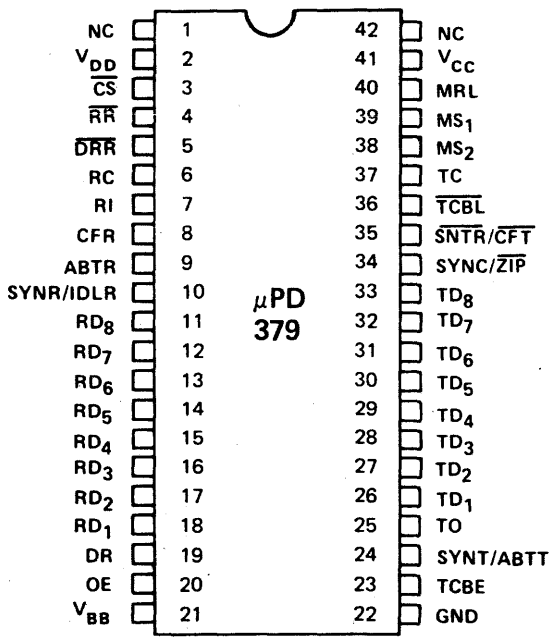
DESCRIPTION

The μPD379 Synchronous Receiver/Transmitter is an MOS LSI monolithic circuit that performs all the receiving and transmitting functions associated with Basic and High Level Data Link Control Procedures. This circuit is fabricated using N-channel AL-Gate MOS technology, allowing all inputs and outputs to be directly TTL compatible. The operation mode, baud rate and synchronous character are changeable through the use of external control. The μPD379 is packaged in a 42 pin Dual-in-line ceramic package.

FEATURES

- Suitable for Synchronous Basic and High Level Data Link Control Procedures (BiSync or SDLC)
- Full or Half Duplex Operation
- Fully Double Buffered Transmit and Receive
- Directly TTL Compatible
- Three-State Data Outputs
- Programmable Sync Word
- Detection/Rejection of Flag, Abort and Idle Patterns
- Zero Insertion and Rejection
- Indication of Overrun and Underrun Errors
- 800K Bits/Sec Operating Speed

PIN CONFIGURATION



NC: NO CONNECTION

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Basic Sync Mode Transmission

The Sync character may be 16 in hexadecimal or it may be set to any other pattern in the Closed Mode. When the mode control register is loaded with MS_1 = high and MS_2 = low, the μPD379 enters the Basic Sync mode from the Closed Mode. The Sync character is continuously transmitted until a transmission data character is loaded. After a data character is loaded, it is serialized and transmitted out from the TO (Transmitter Output) line. If an underrun occurs, Sync character(s) are again transmitted automatically until the next data character is loaded. Transmission data is sent out from LSB (TD_1) first to MSB (TD_8) last on the TO line.

Basic Sync Mode Receive

The RI (Receiver Input) line first searches for Sync characters. Once an 8-bit Sync character has been detected, the following received bits are treated as data characters and outputted on lines $RD_1 - RD_8$ in parallel.

When device operation is started, the receiver section should be first brought into Closed mode or should be reset in order to ensure synchronization.

SDLC Mode Transmission

Until a data character is loaded, the Flag pattern (7E in hexadecimal) is automatically transmitted continuously. After a data character is loaded, it is serialized and transmitted out from LSB (TD_1) to MSB (TD_8) on the TO line. In transmitting data characters, a dummy bit 0 is automatically inserted immediately following five (5) successive 1's. This is called Zero-Insertion and is performed in order to maintain synchronization with the receiver and to avoid duplication of Flag pattern in data characters. (Zero-Insertion may be prohibited optionally with the $\overline{ZIP}$ command, if necessary.) If an underrun occurs while data characters are being transmitted, an Abort pattern (FF in hexadecimal) and then a Flag pattern are automatically transmitted. After that, the Flag pattern is again automatically transmitted until the next data character is loaded.

If a low level is placed on the $\overline{CFT}$ (Closing Flag Transmit) line while a data character is being transmitted, a Closing Flag will be transmitted immediately following transmission of the current data character.

SDLC Mode Receive

First, the Flag pattern is searched for on the RI line. Once a Flag pattern is detected, inserted zero's are rejected from all the following characters except Flag, Abort (7 to 14 successive 1's) and Idle (15 successive 1's) patterns, and then deserialized and output on the $RD_1 - RD_8$ lines in parallel.

If an overrun occurs, all the following data inputs are neglected and the μPD379 goes back to the first stage to search for the next Flag pattern.

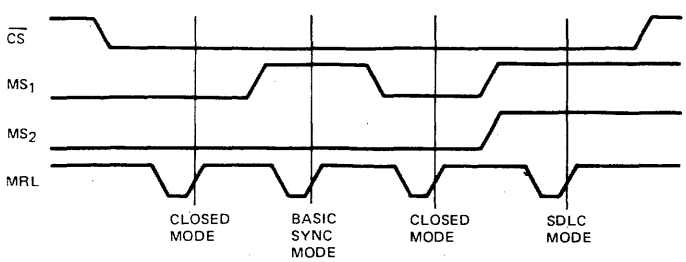
Closed Mode

When there is a change of mode, it must pass through the closed mode. In the closed mode, the following input signals may be used:

$\overline{CS}$, SYNC, $\overline{TCBL}$, MS1, MS2, MRL, $TD_1 - TD_8$

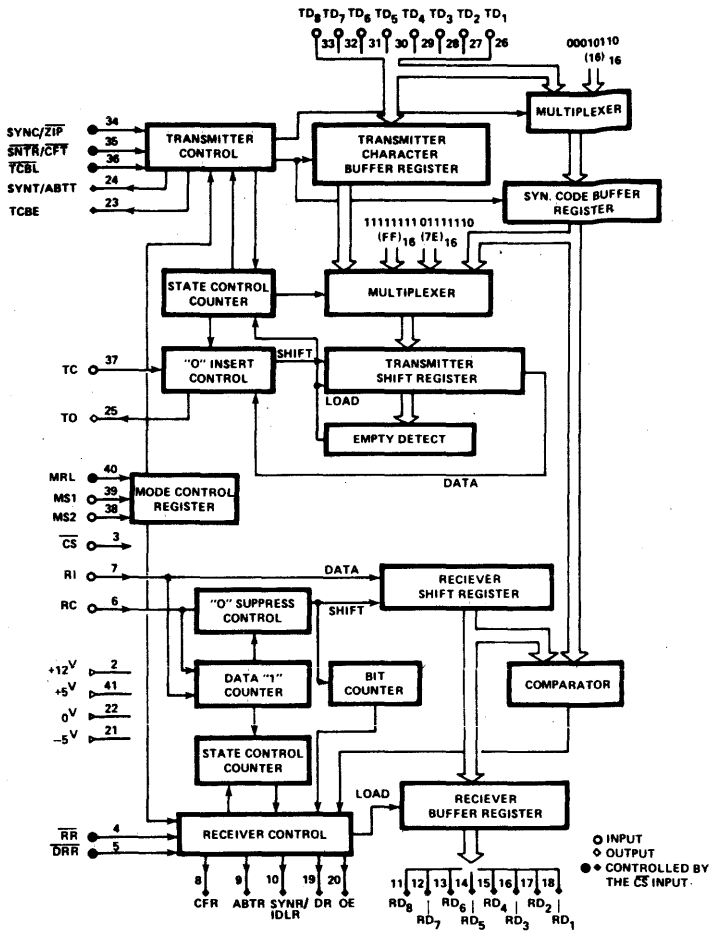
After leaving the closed mode, Sync characters are transmitted synchronously with the rising edge of TC. The receiver operates synchronously with the falling edge of RC, after $\overline{RR}$ = 1.

The following timing diagram shows how mode changes may be accomplished.



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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70°C
Storage Temperature	-40°C to +125°C
All Output Voltages	0V to +8.0V ①
All Input Voltages	0V to +8.0V ①
Supply Voltage V_{CC}	0V to +8.0V ①
Supply Voltage V_{DD}	0V to +16.0V ①
Supply Voltage V_{BB}	-10.0V to 0V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

Note: ① V_{BB} = -5 ± 5%

AC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Frequency	f_c	DC		800	KHz	TC, RC
Pulse Width	t_{PW}					TC, RC
		250			ns	MRL
		250			ns	$\overline{TCBL}$
		250			ns	$\overline{SNTR/CFT}$
		250			ns	$\overline{ZIP}$
		400			ns	$\overline{RR}$
		250			ns	$\overline{DRR}$
Setup Time	$t_{SET\ UP}$	250			ns	
Hold Time	t_{HOLD}	150			ns	
Rise Time	t_r			150	ns	
Fall Time	t_f			150	ns	
Pulse Interval	t_{cc}	100			ns	
Output Delay Time	t_{pd1}		180	270	ns	C_L = 20 pf
	t_{pd2}		410	600	ns	1 TTL Load
Fan Out	N			1		Standard TTL Load

*50% Duty Cycle

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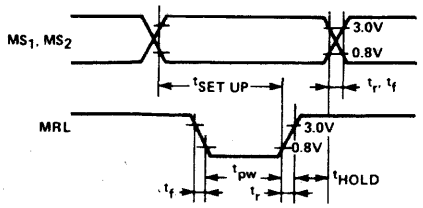
PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION: BASIC SYNC MODE	FUNCTION: SDLC MODE
1	NC	No Connection	
2	V_{DD}	+12V Power Supply	
3	$\overline{CS}$	Chip Select – When "1", the following inputs are disabled and the outputs are put into the high impedance state: (Input Disabled) $\overline{RR}$, $\overline{DRR}$, SYNC/$\overline{ZIP}$, $\overline{SNTR}$/$\overline{CFT}$, $\overline{TCBL}$, MRL; (Output-High Impedance) CFR, ABTR, SYNR/IDLR, RD_1 – RD_8, DR, OE, TCBE, CYNT/ABTT	
4	$\overline{RR}$	Receiver Reset – Receiver portion is reset with a "0" and operation is stopped RD_1 – RD_8 ~ – – – "1" CFR, ABTR, SYNR/IDLR, AR, OE – – – – "0"	
5	$\overline{DRR}$	Data Received Reset – Resets DR flag to "0"	
6	RC	Receiver Clock – Receiver clock input. Trailing edge of clock is located in the center of receiver input bits (RI).	
7	RI	Receiver Input – Received data serial input	
8	CFR	(Normally "0")	Closing Flag Received – Goes high whenever a Flag has been received during data reception. Goes low on the rising edge of DR or OE commands
9	ABTR	("0" Constant)	Abort Received – Becomes "1" when 7 – 14 continuous "1"s are received, after receiving the flag. Goes low on the rising edge of DR or OE commands.
10	SYNR / $\overline{IDLR}$	Sync Character Received – Goes high when synchronization has occurred, or whenever the contents of the Sync Character Buffer and the contents of the Receiver Character Buffer coincide. Goes low when DR goes high and the RD_1 – RD_8 outputs are different from the Sync Character.	Idle Pattern Received – Becomes "1" (Idle) when it receives 15 consecutive "1"s. Goes low on the rising edge of DR or OE outputs.
11 – 18	RD_8 – RD_1	Receiver Data Outputs – Received character output terminal (RD_1:LSB RD_8:MSB)	
19	DR	Data Received – Goes high when the received character has been transferred from the Receiver Shift Register to the Receiver Buffer Register	
		DR does not go high for the first Sync Character input. It is reset when DRR is driven low.	DR does not go high for Flag, Abort or Idle Patterns. It is reset when (1) $\overline{DRR}$ = "0", (2) On the rising edge of OE, (3) Seven (7) successive "1"s have been received.
20	OE	Overrun Error – OE = "1" shows that DR was still high when the received character is moved from the receiving shift register to the receiving buffer register	
		OE is reset if DR is low when the received character is transferred from the Receiver Shift Register to the Receiver Buffer Register	It is reset on the rising edge of DR
21	V_{BB}	–5V Power Supply	
22	V_{SS}	Ground	
23	TCBE	Transmitter Character Buffer Register Empty – TCBE = "1" when the transmitter character buffer is empty.	
		TCBE is reset when $\overline{TCBL}$ is driven low	It is reset when: (1) $\overline{TCBL}$ = "0", (2) When $\overline{CFT}$ = "0" in the data transmission mode, (3) One-half bit before ABTT goes high.
24	SYNT / ABTT	SYNC Character Transmit – SYNT = "1" when a synchronous character is being transmitted. It is reset when: (1) $\overline{SNTR}$ = "0", (2) when transmission of data commences	Abort Pattern Transmit – ABTT = "1" when an Abort Pattern is being transmitted
25	TO	Transmitter Output – Transmitter data output. TO = "1" in the closed mode.	
26 – 33	TD_1 – TD_8	Transmitter Data Inputs – Transmitter character input. (TD_1 = LSB, TD_8 = MSB)	
34	SYNC / $\overline{ZIP}$	SYNC Character – In the Closed Mode, the SYNC line is used to select a SYNC character to be loaded into the SYNC Character Buffer. The selected SYNC character is loaded into the buffer on the rising edge of TCBL and is selected as follows: (1) When SYNC = "0", the character placed on the TD_1 – TD_8 inputs is loaded, (2) When SYNC = "1", 16 Hexadecimal is loaded.	Zero Insertion Prohibit – When $\overline{ZIP}$ is driven low, zero-insertion will be prohibited for all subsequent data characters until a Closing Flag or an Abort Pattern is transmitted.
35	$\overline{SNTR}$ / $\overline{CFT}$	SYNC Character Transmit Reset – When $\overline{SNTR}$ is driven low, SYNT is reset to "0".	Closing Flag Transmit – During transmission, $\overline{CFT}$ low causes the following operations to occur: (1) TCBE Output is reset to "0", (2) The Closing Flag will be transmitted after the end of transmission of the current data character.
36	$\overline{TCBL}$	Transmitter Character Buffer Load – (1) In the closed Mode: the SYNC Character Buffer is loaded on the rising edge of $\overline{TCBL}$. If the SYNC input is low, the buffer is loaded with the data on the TD_1 – TD_8 inputs; if SYNC is high, the buffer is loaded with (16) Hex. (2) In the Basic SYNC or SDLC Modes: When $\overline{TCBL}$ is driven low (a) TCBE is reset to "0" and (b) the data character on the TD_1 – TD_8 inputs is loaded into the Transmitter Character Buffer. The loaded character is latched on the rising edge of $\overline{TCBL}$.	
37	TC	Transmitter Clock – Clock input for transmission.	
38	MS_2	Mode Select 2	
39	MS_1	Mode Select 1 Used to select one of three modes. MS_1 MS_2 MODE L L Closed Mode L H Closed Mode H L Basic Synchronous Mode H H SDLC Synchronous Mode In the closed mode TO and RD_1 – RD_8 are high, all other outputs are low.	
40	MRL	Mode Control Register Load – When MRL is low, the operational mode is selected by the current status of MS_1 and MS_2. When MRL goes high, the operational mode is latched based upon the status of MS_1 and MS_2.	
41	V_{CC}	+5V Power Supply	
42	NC	No Connection	

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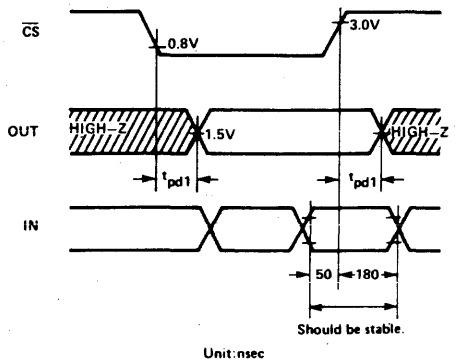
TIMING WAVEFORMS

MODE SELECT



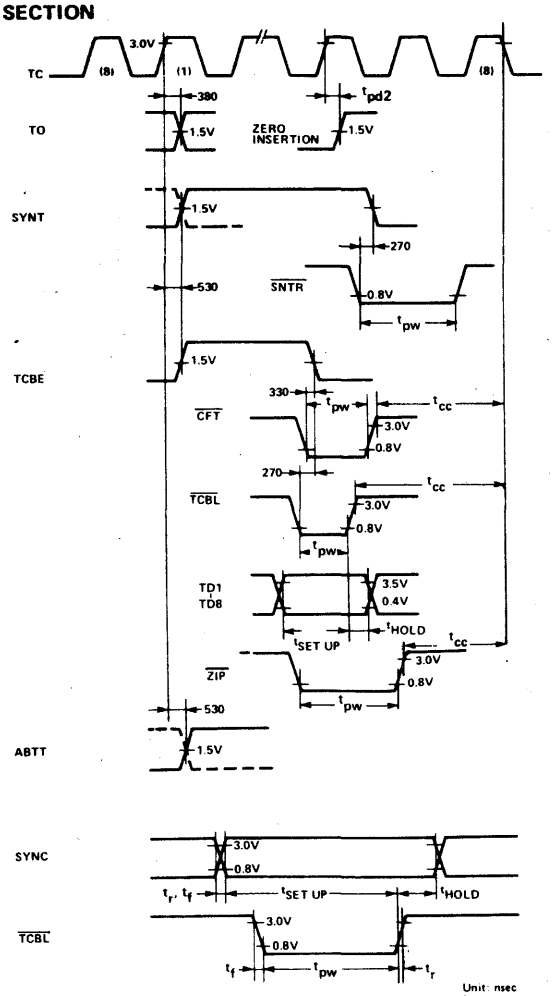
MODE	MS_1	MS_2	MRL
Closed	0	0 or 1	⌐¬
Basic Sync	1	1	⌐¬
SDLC	1	1	⌐¬

CHIP SELECT



Unit: nsec

TRANSMITTER SECTION

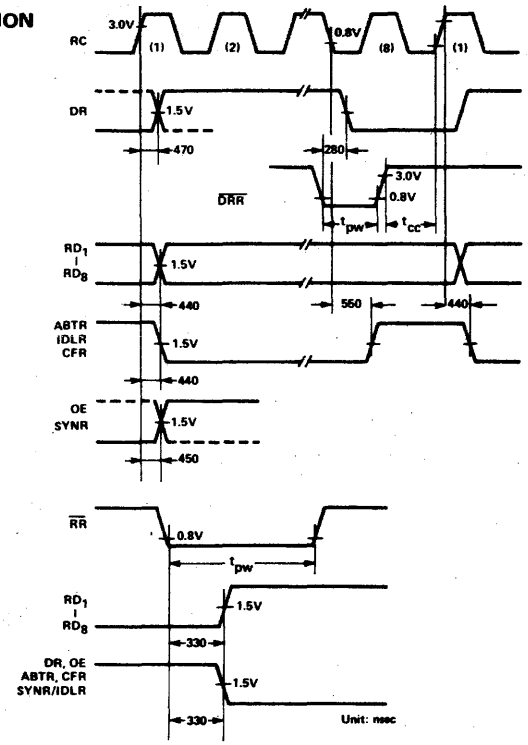


Unit: nsec

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TIMING WAVEFORMS (CONT.)

RECEIVER SECTION



DC CHARACTERISTICS

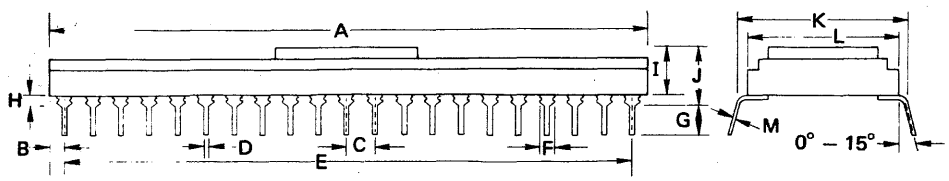
$T_a = 0°C$ to $+70°C$, $V_{DD} = 12V + 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	3.0		V_{DD}	V	With Built-in
Input Low Voltage	V_{IL}			0.8	V	pull-up resistors
Output Leakage Current	I_{OL}	−20		20	μA	V_O = 0.4 to 3.5V (CS)= 3.5V
Output High Voltage	V_{OH}	3.5			V	$I_{OH} = -100\mu A$
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 1.6mA
Input Low Current	I_{IL}			−1.4	mA	V_{IL} = 0.4V
V_{DD} Supply Current	I_{DD}		15	20	mA	
V_{CC} Supply Current	I_{CC}		40	65	mA	
V_{BB} Supply Current	I_{BB}		−0.2	−2.0	mA	
Fan-out	N			1		Standard TTL Load

CAPACITANCE

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}			20	pf	f = 1 MHz
Output Capacitance	C_{OUT}			20	pf	f = 1 MHz

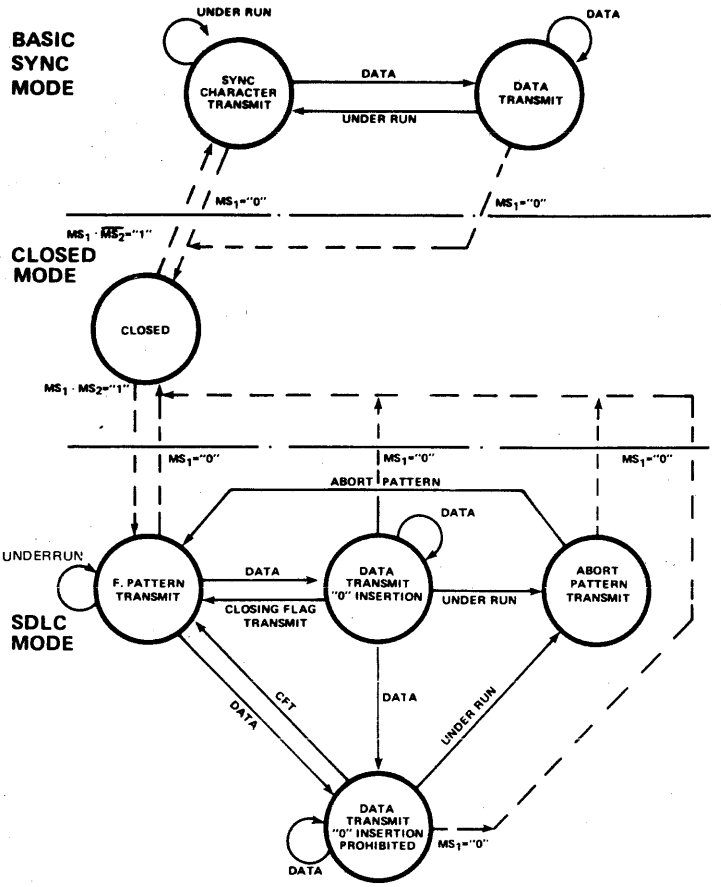
PACKAGE OUTLINE μPD379D



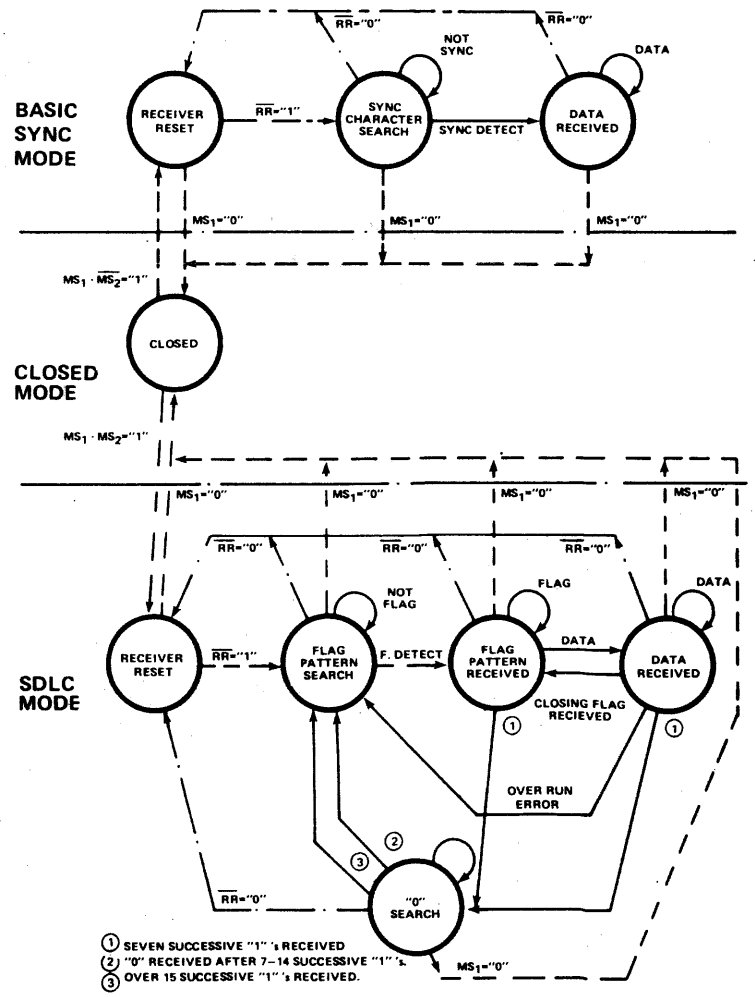
ITEM	MILLIMETERS	INCHES
A	53.5 MAX	2.1 MAX
B	1.35	0.05
C	2.54	0.10
D	50.80	2.0
F	1.27	0.05
G	2.54 MAX	0.10 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.21 MAX
K	15.24	0.60
L	13.50	0.53
M	0.3	0.012

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TRANSMITTER STATE DIAGRAM



RECEIVER STATE DIAGRAM



SP379-8-77-GN-CAT

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PRINTER CONTROLLER

DESCRIPTION

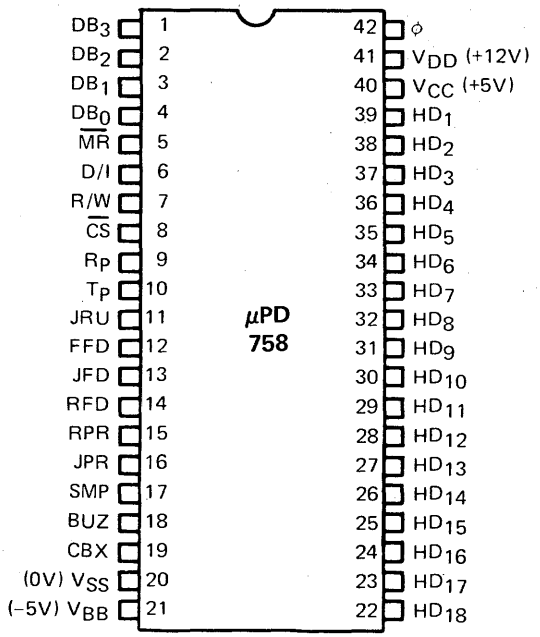
The μPD758 is a digital LSI device designed to control SEIKO 101 Series drum-type impact printers. It can be used with either single or double printer systems. The μPD758, ideally suited for low-cost Electronic Cash Register (ECR) systems, frees the processor from direct control of the printer and simplifies the peripheral circuitry.

Using a few of the possible 18 instructions, the controlling processor need only load the μPD758 with the characters to be printed, and issue the appropriate print instruction. The μPD758 then assumes control of the printer, keeping track of the printer drum position and generating hammer drive signals at the approproate time. The μPD758 also has separate output drives that are under software control. These are typically used to drive the STAMP input to the printer and to provide discrete drives for BUZZER and CASH BOX functions of the ECR system.

FEATURES

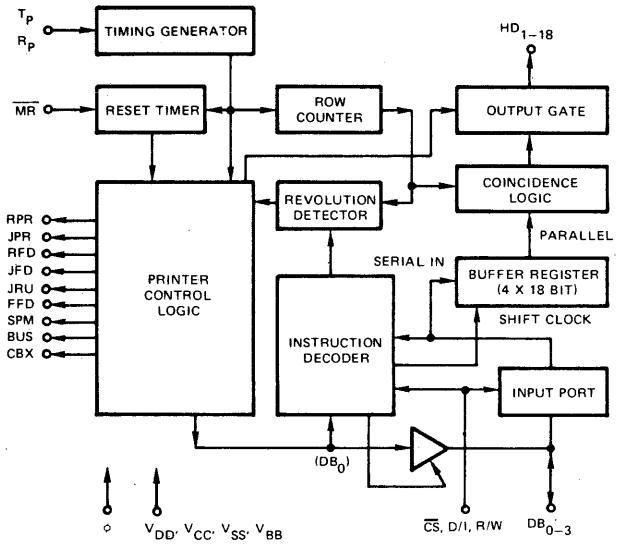
- Usable with SEIKO 101 Series Printers (CR101T[d], EP101S) and equivalents
- ECR Printer and Line Feed Control Capability
- 18 Powerful Instructions
- Controls up to 18 columns
- Controls up to 16 characters
- Input/Output TTL Compatible
- N-Ch MOS
- 42 Pin Plastic DIP
- Power Supplies, +12V, +5V and -5V

PIN CONFIGURATION



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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
All Input and Output Voltages	−1 to +7 Volts ①
Clock Voltage	−1 to +7 Volts ①
Supply Voltage V_{DD}	−1 to +15 Volts
Supply Voltage V_{CC}	−1 to +7 Volts
Supply Voltage V_{BB}	−2 to −8 Volts

Note: ① Relative to V_{BB}.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10 to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{SS} = 0V, V_{BB} = −5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	+3.0		V_{CC}	V	
Input Low Voltage	V_{IL}	−0.5		+0.8	V	
Output High Voltage	V_{OH}	+3.5			V	I_{OH} = −1.0 mA
Output Low Voltage	V_{OL}			+0.5	V	I_{OL} = +1.7 mA
High Level Clock Voltage	$V_{\phi H}$	+3.0		V_{CC}	V	
Low Level Clock Voltage	$V_{\phi L}$	−0.5		+0.8	V	
High Level Input Leakage Current	I_{LIH}			+10	μA	V_I = +3.0V
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_I = +0.8V
High Level Output Leakage Current	I_{LOH}			+10	μA	V_O = +3.5V
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_O = +0.5V
Supply Current	I_{BB}			−300	μA	V_{BB} = −5.25V
Supply Current	I_{DD}		17		mA	
Supply Current	I_{CC}		27		mA	

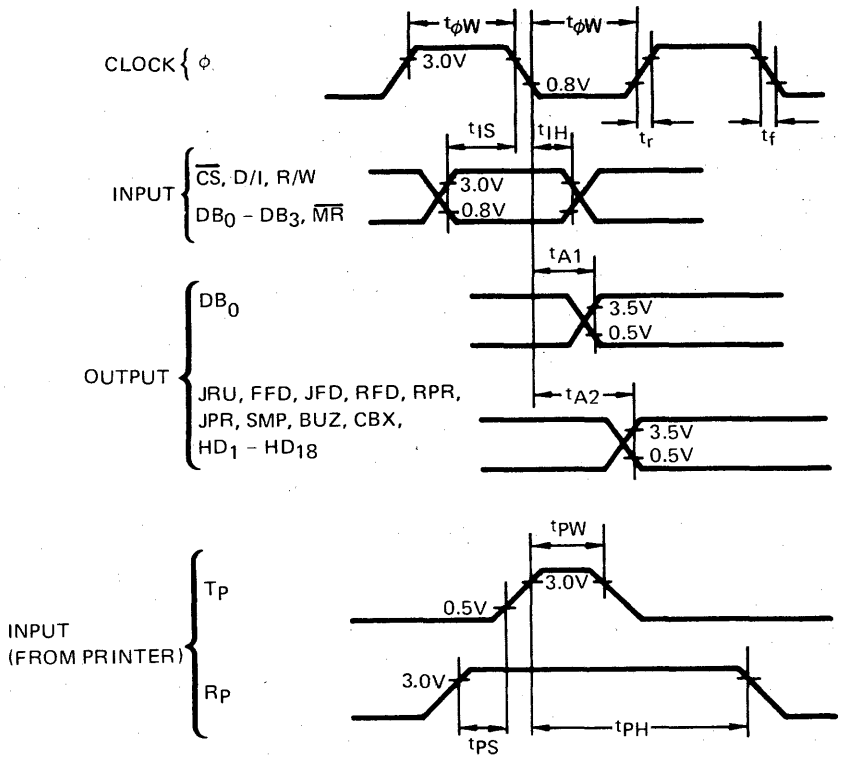
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CAPACITANCE

T_a = −10 to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{SS} = 0V, V_{BB} = −5V ± 5%

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Capacitance	C_{IN}			10	pF	f = 1 MHz
Output Capacitance	C_{OUT}			10	pF	f = 1 MHz

TIMING WAVEFORMS



AC CHARACTERISTICS

T_a = −10 to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{SS} = 0V, V_{BB} = −5V ± 5%

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Clock Rise and Fall Time	t_r, t_f			50	ns	
Clock Pulse Width	$t_{\phi W}$	0.45		2.0	μs	
Output Delay Time	t_{A1}			430	ns	$1T^2L$ & C_L = 100 pF
	t_{A2}			700	ns	$1T^2L$ & C_L = 100 pF
Input Setup Time	t_{IS}	400			ns	
Input Hold Time	t_{IH}	40			ns	
Pulse Width for T_P Input	t_{PW}	2			clock period	
R_P Input Setup Time	t_{PS}	0			clock period	
R_P Input Hold Time	t_{PH}	3			clock period	

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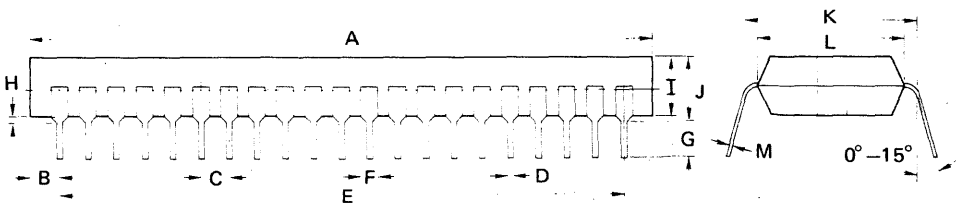
INSTRUCTION TABLE

INST. NO.	OPERATION	BUSY	D/I	R/W	DB			
					3	2	1	0
1	CHECK DB0 FOR BUSY FLAG STATUS	BF①	X②	0	X	X	X	BF
2	STORE DATA (dddd) INTO BUFFER REGISTER	0	0	1	d③	d	d	d
3a	NO OPERATION	1	0	1	X	X	X	X
3b		1	1	1	0	X	X	X
3c		1	1	1	1	1	X	X
3d		0	1	1	0	0	0	0
4	PRINT BUFFER REGISTER CONTENTS TO JOURNAL	0	1	1	0	0	0	1
5	PRINT BUFFER REGISTER CONTENTS TO RECEIPT	0	1	1	0	0	1	0
6	PRINT BUFFER REGISTER CONTENTS TO JOURNAL AND RECEIPT	0	1	1	0	0	1	1
7	FAST FEED AND STAMP RECEIPT	0	1	1	0	1	0	0
8	PRINT STORED DATA ONTO JOURNAL AND FEED ONE LINE	0	1	1	0	1	0	1
9	PRINT STORED DATA ONTO RECEIPT AND FEED ONE LINE	0	1	1	0	1	1	0
10	PRINT STORED DATA ONTO RECEIPT AND JOURNAL AND FEED BOTH ONE LINE	0	1	1	0	1	1	1
11	DRIVE CASH BOX OUTPUT	X	1	1	1	0	0	0
12	DRIVE BUZZER OUTPUT FOR FOUR CHARACTER PERIODS	X	1	1	1	0	0	1
13	RESET BUZZER OUTPUT	X	1	1	1	0	1	0
14	DRIVE BUZZER OUTPUT UNTIL RESET	X	1	1	1	0	1	1
15	DRIVE STAMP OUTPUT	0	1	1	1	1	0	0
16	FEED JOURNAL ONE LINE	0	1	1	1	1	0	1
17	FEED RECEIPT ONE LINE	0	1	1	1	1	1	0
18	FEED BOTH RECEIPT AND JOURNAL ONE LINE	0	1	1	1	1	1	1

Notes: ① BF = Busy Flag
② X = Don't Care
③ d = Data

PACKAGE OUTLINE

μPD758C



ITEM	MILLIMETERS	INCHES
A	56.0 MAX	2.2 MAX
B	2.6 MAX	0.1 MAX
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 MIN	0.126 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.20 MAX
J	5.72 MAX	0.22 MAX
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004

SP758-8-77-GN-CAT
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PRINTER CONTROLLER

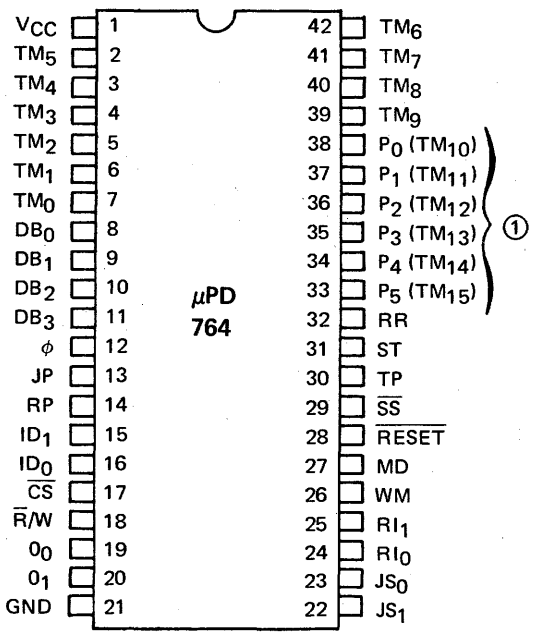
DESCRIPTION

The μPD764 is a digital LSI device designed to control SEIKO CR-330 or M-310 rolling contact printers. The μPD764, which is ideally suited for low-cost Electronic Cash Register (ECR) systems, frees the processor from direct control of the printer and simplifies the peripheral circuitry.

The processor need only load the μPD764 with the characters to be printed and issue the appropriate print command. The μPD764 then assumes control of the printer – positioning the print wheels, initiating the rolling contact print process, feeding paper and feeding ribbon automatically without further processor intervention.

FEATURES

- Compatible with SEIKO CR-330 and M-310 Printers.
- Simple Interface to 4-Bit, 8-Bit and 16-Bit Microprocessors.
- 23 Powerful Instructions.
- 4-Bit Data Bus for Print Data and Instruction Inputs.
- 16 Digit Data Buffer.
- 16 Trigger Magnet Drive Outputs for the M-310 and 10 for the CR-330.
- Single Phase Clock Input. 300, 400 or 500 kHz Selectable.
- Input/Output and Clock TTL Compatible.
- N-Channel MOS.
- Single +5V Power Supply.



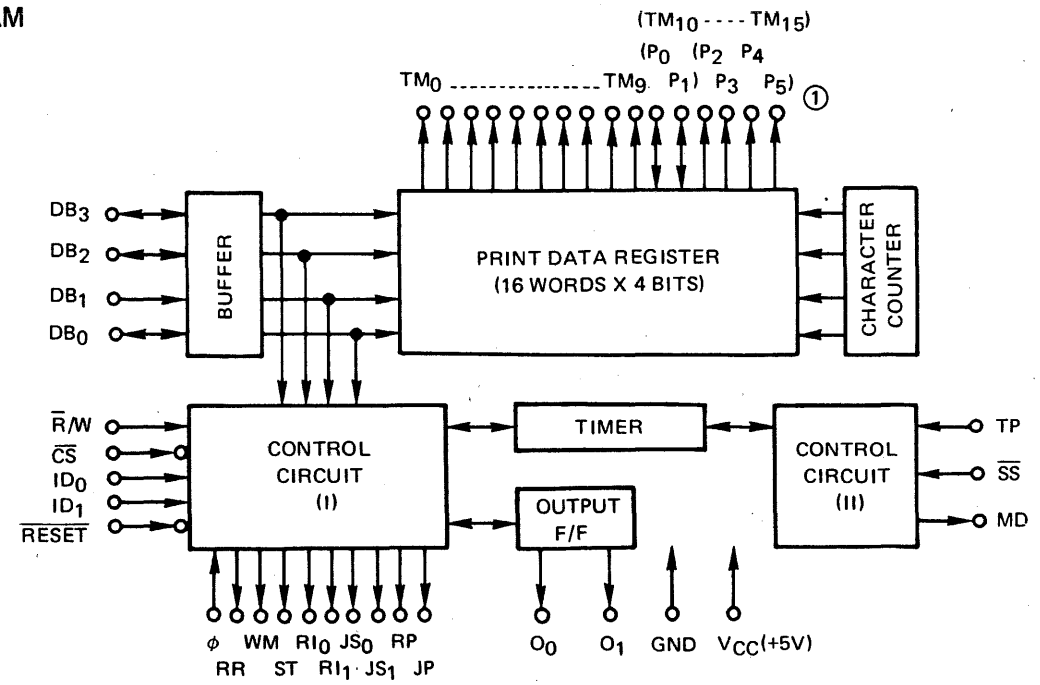
Note: ① $P_0 - P_{15}$ for CR-330 Printer
$TM_{10} - TM_{15}$ for M-310 Printer

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PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	INPUT/ OUTPUT	FUNCTION
7 – 2 42 – 39	$TM_0 - TM_9$	O	Trigger Magnet Drive
8, 10, 11 9	DB_0, DB_2, DB_3 DB_1	I/O I	Data Bus
12	ϕ	I	Single Phase Clock (TTL Level)
13	JP	O	Journal Print Drive
14	RP	O	Receipt Print Drive
16, 15	$ID_0 - ID_1$	I	Instruction/Data Selector
17	$\overline{CS}$	I	Chip Select (Active Low)
18	$\overline{R}/W$	I	Read/Write Control – "0" = Read, "1" = Write
19, 20	O_0, O_1	O	Output F/F
23	JS_0	O	Journal Stop Plunger Drive
22	JS_1	O	Journal Stop Plunger Hold Current Control
24	RI_0	O	Receipt Issue Plunger Drive
25	RI_1	O	Receipt Issue Plunger Hold Current Control
26	WM	O	Journal Wind Motor Drive
27	MD	O	Motor Drive
28	$\overline{RESET}$	1	Reset Input (Active Low) O_0, O_1: Reset to "0". ϕ: Set to 300 kHz Mode $DB_0 - DB_3$: Set to Hi-Z State Instruction Register: cleared Busy Flag: cleared Character Counter: Set to F in Hexidecimal $P_0 - P_1$: Set as Input Port $P_2 - P_5$: Set as Output Port (Output all "0")
29	$\overline{SS}$	I	Stop Signal from Printer
30	TP	I	Timing Pulse from Printer
31	ST	O	Stamp Plunger Drive
32	RR	O	Red Ribbon Select Control
36 – 33	$P_2 - P_5$ or $TM_{12} - TM_{15}$	O O	4-Bit Parallel Output Port when reset or specified with an instruction. Trigger Magnet Drive (for M-310 Printer) when specified with an instruction.
38, 37	$P_0 - P_1$ or $TM_{10} - TM_{11}$	I O	2-Bit Parallel Input Port when reset or specified with an instruction. Trigger Magnet Drive (for M-310 Printer) when specified with an instruction.

BLOCK DIAGRAM



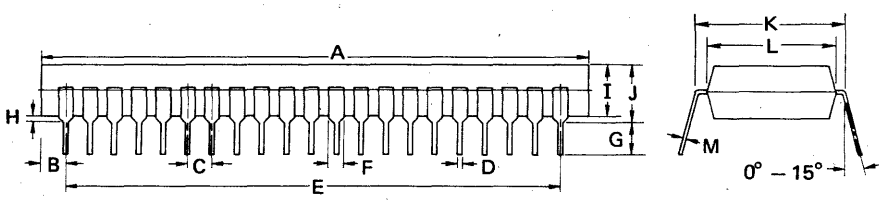
Note: ① $P_0 - P_{15}$ for CR-330 Printer
$TM_{10} - TM_{15}$ for M-310 Printer

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INSTRUCTION SET

NO.	MNEMONIC	FUNCTION	DB				ID	
			3	2	1	0	1	0
1	RS	Receipt – Stamp	0	0	0	1	1	1
2	RFF	Receipt – Fast Feed	0	0	1	0	1	1
3	RFPS	Receipt – Fast Feed, Print and Stamp	0	0	1	1	1	1
4	JPF	Journal – Print and Paper Feed	0	1	0	0	1	1
5	JP	Journal – Print	0	1	0	1	1	1
6	JF	Journal – Feed	0	1	1	0	1	1
7	RPF	Receipt – Print and Feed	1	0	0	0	1	1
8	RP	Receipt – Print	1	0	0	1	1	1
9	RF	Receipt – Feed	1	0	1	0	1	1
10	JRPF	Journal and Receipt – Print and Feed	1	1	0	0	1	1
11	JRP	Journal and Receipt – Print	1	1	0	1	1	1
12	JRF	Journal and Receipt – Feed	1	1	1	0	1	1
13	RR	Set Red Ribbon	0	0	0	1	0	1
14	RTM	Set $P_0 - P_1$ as Input Port and $P_2 - P_5$ as Output Port	0	0	1	0	0	1
15	STM	Set $P_0 - P_5$ as $TM_{10} - TM_{15}$	0	0	1	1	0	1
16	SFM	Set to ϕ = 400 kHz Operation Mode	0	1	0	0	0	1
17	SFH	Set to ϕ = 500 kHz Operation Mode	0	1	0	1	0	1
18	RSO	Reset Output F/F 0 (O_0)	0	1	1	0	0	1
19	STO	Set Output F/F 0 (O_0)	0	1	1	1	0	1
20	RS1	Reset Output F/F 1 (O_1)	1	0	1	0	0	1
21	ST1	Set Output F/F 1 (O_1)	1	0	1	1	0	1
22	RSB	Reset Output F/Fs 0 and 1 (O_0 and O_1)	1	1	1	0	0	1
23	STB	Set Output F/Fs 0 and 1 (O_0 and O_1)	1	1	1	1	0	1

PACKAGE OUTLINE μPD764C



ITEM	MILLIMETERS	INCHES
A	56.0 MAX	2.2 MAX
B	2.6 MAX	0.1 MAX
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 MIN	0.126 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.20 MAX
J	5.72 MAX	0.22 MAX
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004

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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −40°C to +125°C
All Inputs and Outputs . . . . . −0.5 to +7 Volts
V_{CC} . . . . . −0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10 to +70°C

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	+2.2			V	
Input Low Voltage	V_{IL}			+0.6	V	
Output High Voltage	V_{OH}	V_{CC} −2.45			V	I_{OH} = −100 μA
Output Low Voltage	V_{OL1}			0.4	V	I_{OL} = +1.1 mA
	V_{OL2}			0.6	V	I_{OL} = +1.7 mA
High Level Input Leakage Current	I_{LIH}			+10	μA	V_I = +2.2V
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_I = +0.6V
High Level Output Leakage Current	I_{LOH}			+10	μA	$V_O = V_{CC}$ −2.45V
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_O = +0.4V
Supply Current	I_{CC}		45		mA	

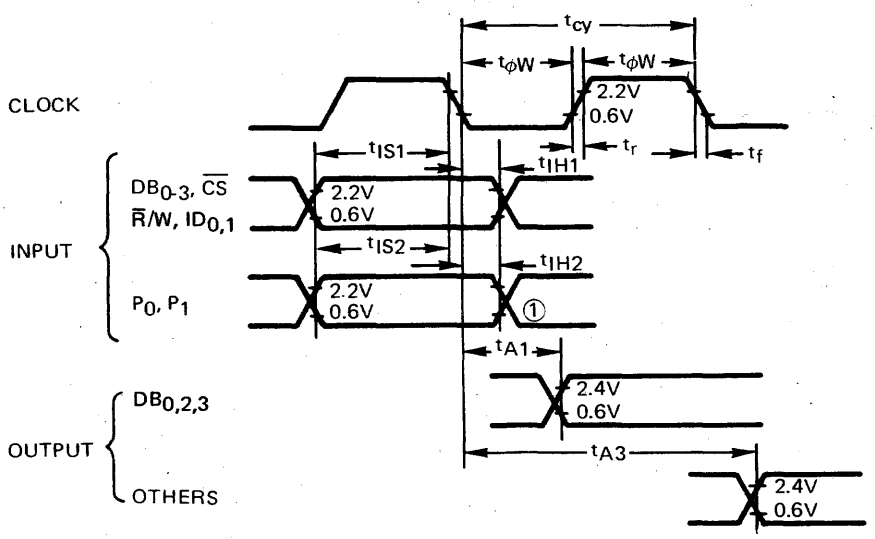
AC CHARACTERISTICS

T_a = −10 to +70°C

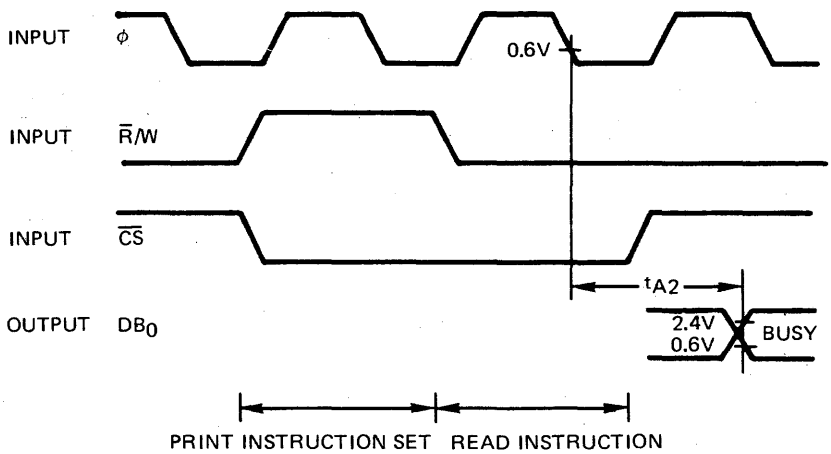
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Clock Cycle Time	t_{CY}	2		5	μs	
Clock Rise and Fall Time	t_r, t_f			70	ns	
Clock Pulse Width	$t_{\phi W}$	0.45			μs	
Output Delay Time	t_{A1}			430	ns	
	t_{A2}			800	ns	$1T^2$ L & C_L = 100 pF
	t_{A3}			2.0	μs	
Input Setup Time	t_{IS_1}	400			ns	
	t_{IS_2}	400			ns	
Input Hold Time	t_{IH_1}	40			ns	
	t_{IH_2}	100			ns	
Pulse Width for Tp Input	t_{TP}	5			t_{CY}	
$\overline{SS}$ Input Pulse Width	t_{SS}	5			t_{CY}	
$\overline{RESET}$ Input Pulse Width	t_{RES}	5			t_{CY}	

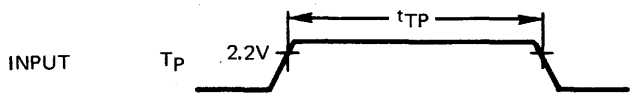
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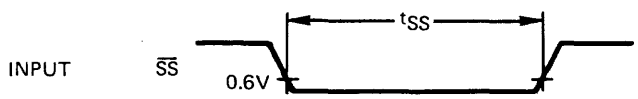
TIMING WAVEFORMS

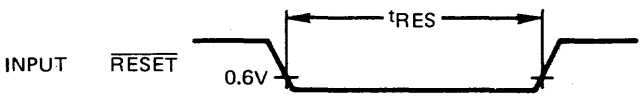


Note: ① If a Read instruction is performed just following an instruction that sets Busy Flag, the output delay of DB_0 (Busy) is t_{A2} as follows.









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EIGHT-BIT INPUT/OUTPUT PORT

DESCRIPTION

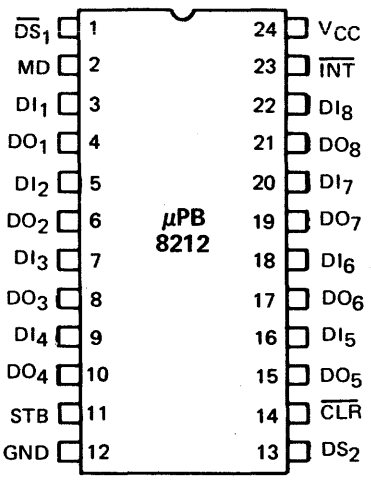
The μPB8212 input/output port consists of an 8-bit latch with three-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the control and generation of interrupts to the microprocessor.

The device is multimode in nature and can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

FEATURES

- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current – 0.25 mA Max.
- Three State Outputs
- Outputs Sink 15 mA
- 3.65V Output High Voltage for Direct Interface to 8080A Processor
- Asynchronous Register Clear
- Replaces Buffers, Latches and Multiplexers in Microcomputer Systems
- Reduces System Package Count
- Available in 24-pin Plastic and Cerdip Packages

PIN CONFIGURATION



PIN NAMES

$DI_1 - DI_8$	Data In
$DO_1 - DO_8$	Data Out
$\overline{DS}_1$, DS_2	Device Select
MD	Mode
STB	Strobe
$\overline{INT}$	Interrupt (Active Low)
$\overline{CLR}$	Clear (Active Low)

Rev/1

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Data Latch

The 8 flip-flops that compose the data latch are of a "D" type design. The output (Q) of the flip-flop follows the data input (D) while the clock input (C) is high. Latching occurs when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$).
(Note: Clock (C) Overrides Reset ($\overline{CLR}$).)

Output Buffer

The output of the data latch (Q) are connected to three-state, non-inverting output buffers. These buffers have a common control line (EN); enabling the buffer to transmit the data from the outputs of the data latch (Q) or disabling the buffer, forcing the output into a high impedance state (three-state).

This high-impedance state allows the designer to connect the μPB8212 directly to the microprocessor bi-directional data bus.

Control Logic

The μPB8212 has four control inputs: $\overline{DS}_1$, DS_2, MD and STB. These inputs are employed to control device selection, data latching, output buffer state and the service request flip-flop.

$\overline{DS}_1$, DS_2 (Device Select)

These two inputs are employed for device selection. When $\overline{DS}_1$ is low and DS_2 is high ($\overline{DS}_1 \cdot DS_2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

Service Request Flip-Flop (SR)

The (SR) flip-flop is employed to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output (Q) of the (SR) flip-flop is connected to an inverting input of a "NOR" gate. The other input of the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS}_1 \cdot DS_2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.

MD (Mode)

This input is employed to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is in the output mode (high) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS}_1 \cdot DS_2$).

When MD is in the input mode (low) the output buffer state is determined by the device selection logic ($\overline{DS}_1 \cdot DS_2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

STB is employed as the clock (C) to the data latch for the input mode (MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop triggers on the negative edge of STB which overrides $\overline{CLR}$.

ABSOLUTE MAXIMUM RATINGS*

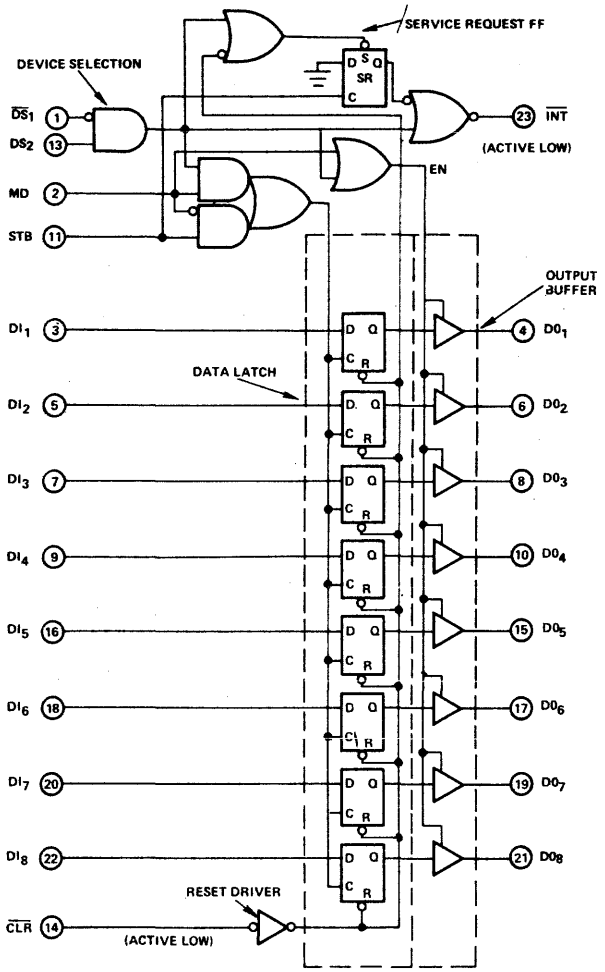
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +5.5 Volts
Output Currents	125 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

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BLOCK DIAGRAM



STB	MD	$(\overline{DS_1} \cdot DS_2)$	DATA OUT EQUALS
0	0	0	Three-State
1	0	0	Three-State
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

$\overline{CLR}$	$(\overline{DS_1} \cdot DS_2)$	STB	SR ②	$\overline{INT}$
0	0	0	1	1
0	1	0	1	0
1	0	0	③	③
1	↓	0	1	1
1	0	↓	0	0
1	1	0	1	0
1	1	↓	0	0

Notes: ① $\overline{CLR}$ resets data latch sets SR flip-flop. (No effect on output buffer)
② Internal SR flip-flop
③ Previous data remains

DC CHARACTERISTICS

$T_a = 0°C$ to $70°C$; $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current ACK, DS_2, CR, $DI_1 - DI_8$ Inputs	I_F		−0.14	−0.25	mA	$V_F = 0.45V$
Input Load Current MD Input	I_F		−0.25	−0.75	mA	$V_F = 0.45V$
Input Load Current $\overline{DS_1}$ Input	I_F		−0.26	−1.0	mA	$V_F = 0.45V$
Input Leakage Current ACK, DS, CR, $DI_1 - DI_8$ Inputs	I_R			10	μA	$V_R = 5.25V$
Input Leakage Current MD Input	I_R			30	μA	$V_R = 5.25V$
Input Leakage Current $\overline{DS_1}$ Input	I_R			40	μA	$V_R = 5.25V$
Input Forward Voltage Clamp	V_C		−0.85	−1.3	V	$I_C = -5$ mA
Input "Low" Voltage	V_{IL}			0.85	V	
Input "High" Voltage	V_{IH}	2.0			V	
Output "Low" Voltage	V_{OL}		0.26	0.45	V	$I_{OL} = 15$ mA
Output "High" Voltage	V_{OH}	3.65	4.0		V	$I_{OH} = -1$ mA
Short Circuit Output Current	I_{SC}	−15	−38	−75	mA	$V_O = 0V$
Output Leakage Current High Impedance State	I_O			20	μA	$V_O = 0.45V/5.25V$
Power Supply Current	I_{CC}		103	130	mA	

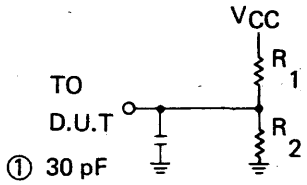
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AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Pulse Width	t_{pw}	30			ns	Input Pulse Amplitude = 2.5V
Data To Output Delay	t_{pd}		20	30	ns	
Write Enable To Output Delay	t_{we}			40	ns	Input Rise and Fall Times = 5 ns
Data Setup Time	t_{set}	15			ns	
Data Hold Time	t_h	20			ns	Between 1V and 2V Measurement made at 1.5V with 15 mA and 30 pF Test Load
Reset to Output Delay	t_r			40	ns	
Set To Output Delay	t_s			30	ns	
Output Enable/Disable Time	t_e/t_d			45	ns	①
Clear To Output Delay	t_c			55	ns	②

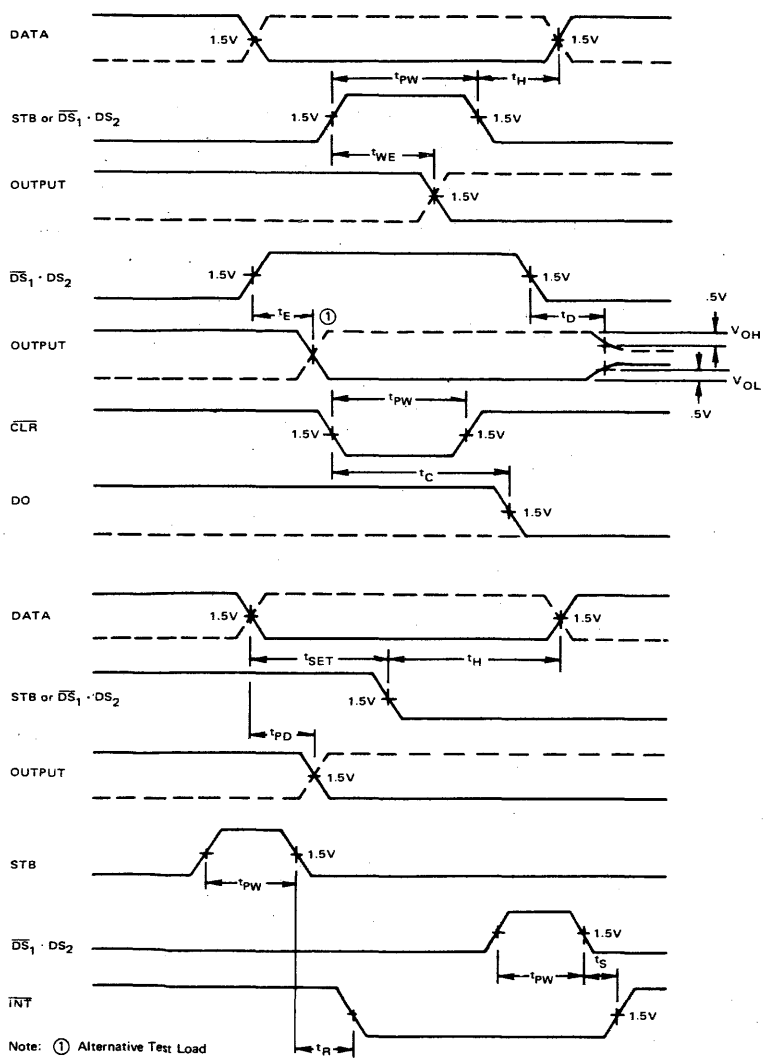
Notes: ① R_1 = 300Ω/10KΩ; R_2 = 600Ω/1KΩ
② R_1 = 300Ω; R_2 = 600Ω



TEST CIRCUIT

Note: ① Including Jig and Probe Capacitance

TIMING WAVEFORMS



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CAPACITANCE ①

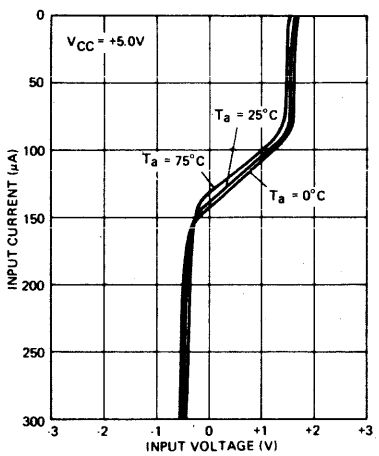
T_a = 25°C; V_{CC} = +5V; V_{BIAS} = 2.5V; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		7	12	pF	$\overline{DS_1}$, MD
Input Capacitance	C_{IN}		4	9	pF	DS_2, CLR, STB, $DI_1 - DI_8$
Output Capacitance	C_{OUT}		6	12	pF	$DO_1 - DO_8$

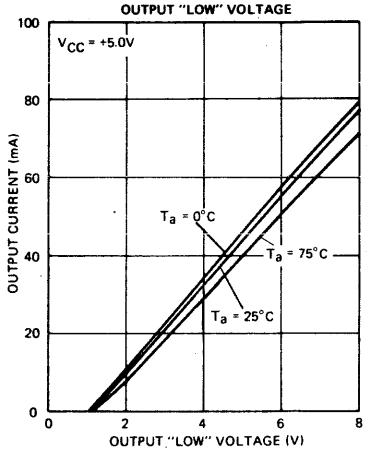
Note: ① This parameter is periodically sampled and not 100% tested

TYPICAL CHARACTERISTICS

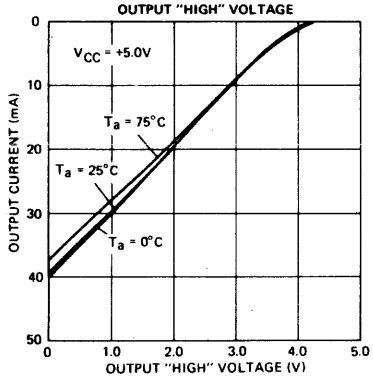
INPUT CURRENT VS. INPUT VOLTAGE



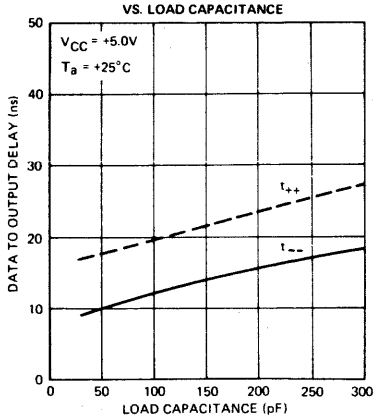
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



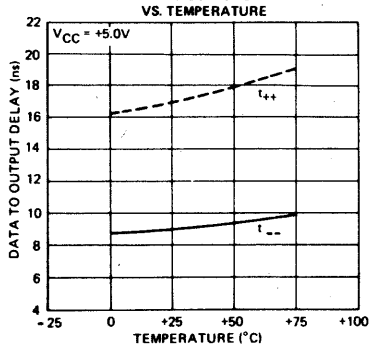
OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



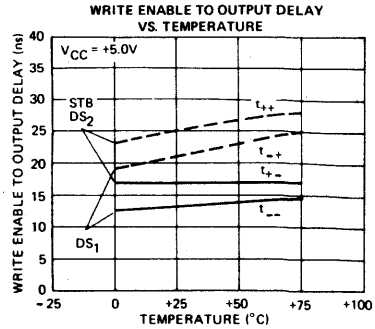
DATA TO OUTPUT DELAY VS. LOAD CAPACITANCE



DATA TO OUTPUT DELAY VS. TEMPERATURE

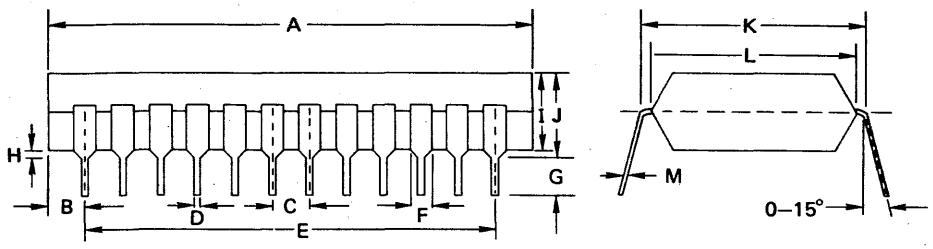


WRITE ENABLE TO OUTPUT DELAY VS. TEMPERATURE



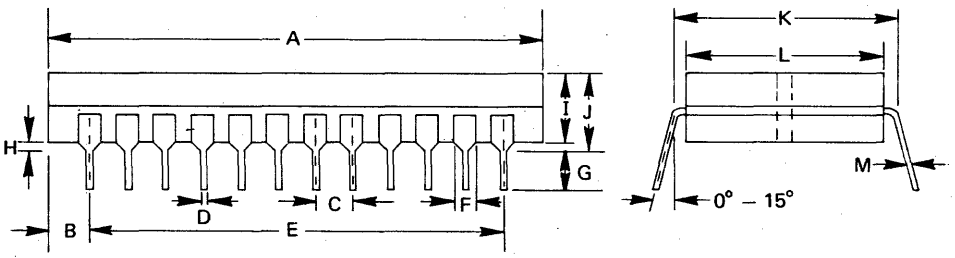
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PACKAGE OUTLINE
μPB8212C/D



μPB8212C (Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



μPB8212D (Cerdip)

ITEM	MILLIMETERS	INCHES
A	33.5 MAX.	1.32 MAX.
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.019 MIN.
I	4.58 MAX.	0.181 MAX.
J	5.08 MAX.	0.2 MAX.
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

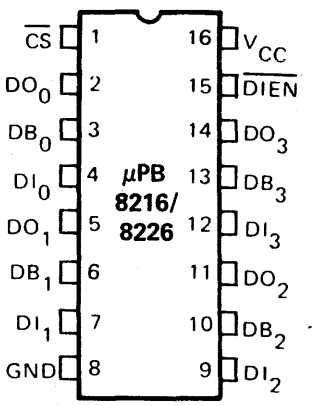
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4 BIT PARALLEL BIDIRECTIONAL BUS DRIVER

DESCRIPTION All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.65V (V_{OH}), and for high capacitance terminated bus structures, the DB outputs provide a high 55 mA (I_{OL}) capability.

FEATURES
- Data Bus Buffer Driver for μCOM-8 Microprocessor Family
- Low Input Load Current — 0.25 mA Maximum
- High Output Drive Capability for Driving System Data Bus
- 3.65V Output High Voltage for Direct Interface to μCOM-8 Microprocessor Family
- Three State Outputs
- Reduces System Package Count
- Available in 16 pin packages: Cerdip and Plastic

PIN CONFIGURATION



PIN NAMES

DB_0 - DB_3	Data Bus Bi Directional
DI_0 - DI_3	Data Input
DO_0 - DO_3	Data Output
$\overline{DIEN}$	Data in Enable Direction Control
$\overline{CS}$	Chip Select

Rev/2

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FUNCTIONAL DESCRIPTION

Microprocessors like the 8080A are MOS devices and are generally capable of driving a single TTL load. This also applies to MOS memory devices. This type of drive is sufficient for small systems with a few components, but often it is necessary to buffer the microprocessor and memories when adding components or expanding to a multi-board system.

The μPD8216/8226 is a four bit bi-directional bus driver specifically designed to buffer microcomputer system components.

Bi-Directional Driver

Each buffered line of the four bit driver consists of two separate buffers. They are three state in nature to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this is used to interface to the system side components such as memories, I/O, etc. Its interface is directly TTL compatible and it has high drive (55 mA). For maximum flexibility on the other side of the driver the inputs and outputs are separate. They can be tied together so that the driver can be used to buffer a true bi-directional bus such as the 8080A Data Bus. The DO outputs on this side of the driver have a special high voltage output drive capability (3.65V) so that direct interface to the 8080A processor is achieved with an adequate amount of noise immunity (650 mV worst case).

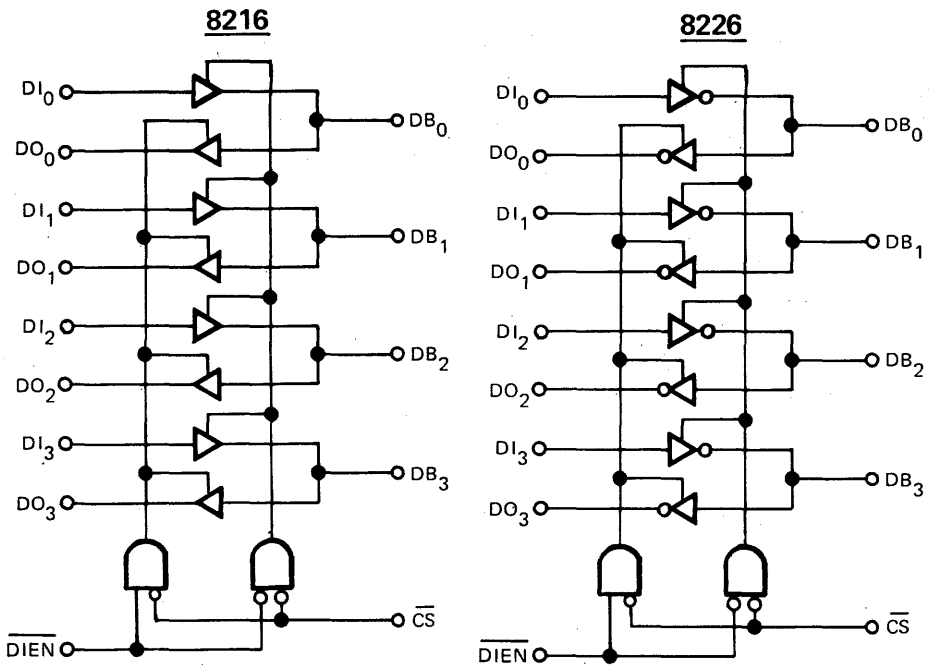
Control Gating $\overline{CS}$, $\overline{DIEN}$

The $\overline{CS}$ input is used for device selection. When $\overline{CS}$ is "high" the output drivers are all forced to their high-impedance state. When it is "low" the device is selected (enabled) and the data flow direction is determined by the $\overline{DIEN}$ input.

The $\overline{DIEN}$ input controls the data flow direction (see Block Diagrams for complete truth table). This directional control is accomplished by forcing one of the pair of buffers to its high impedance state. This allows the other to transmit its data. This is accomplished by a simple two gate circuit.

The μPB8216/8226 is a device that will reduce component count in microcomputer systems and at the same time enhance noise immunity to assure reliable, high performance operation.

BLOCK DIAGRAMS



$\overline{DIEN}$	$\overline{CS}$	RESULT
0	0	DI → DB
1	0	DB → DO
0	1	High Impedance
1	1	

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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to 70°C
Storage Temperature (Cerdip)	−65°C to +150°C
(Plastic)	−65°C to +125°C
All Output and Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.3 to +5.5 Volts
Output Currents	125 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = +5V±5%

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current $\overline{DIEN}$, $\overline{CS}$		I_{F1}			−0.5	mA	V_F = 0.45
Input Load Current All Other Inputs		I_{F2}			−0.25*	mA	V_F = 0.45
Input Leakage Current $\overline{DIEN}$, $\overline{CS}$		I_{R1}			20	μA	V_R = 5.25V
Input Leakage Current DI Inputs		I_{R2}			10	μA	V_R = 5.25V
Input Forward Voltage Clamp		V_C			−1.3	V	I_C = −5 mA
Input "Low" Voltage		V_{IL}			0.95	V	
Input "High" Voltage		V_{IH}	2.0			V	
Output Leakage Current (3-State)	DO	I_O			20	μA	V_O = 0.45/5.25V
	DB	I_O			100		
Power Supply Current	8216	I_{CC}			130	mA	
	8226	I_{CC}			120	mA	
Output "Low" Voltage		V_{OL1}			0.45	V	DO Outputs I_{OL} = 15 mA DB Outputs I_{OL} = 25 mA
Output "Low" Voltage	8216	V_{OL2}			0.6	V	DB Outputs I_{OL} = 55 mA
	8226	V_{OL2}			0.6	V	DB Outputs I_{OH} = 50 mA
Output "High" Voltage		V_{OH1}	3.65			V	DO Outputs I_{OH} = −1 mA
Output "High" Voltage		V_{OH2}	2.4			V	DB Outputs I_{OH} = −10 mA
Output Short Circuit Current		I_{OS}	−15 −30		−65 −120	mA mA	DO Outputs V_O = 0V DB Outputs V_{CC} = 5.0V

Note: ① Typical values are for T_a = 25°C, V_{CC} = 5.0V.

CAPACITANCE ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			8	pF	V_{BIAS} = 2.5V V_{CC} = 5V T_a = 25°C f = 1 MHz
Output Capacitance	C_{OUT1}			10 ②	pF	
Output Capacitance	C_{OUT2}			18 ③	pF	

Notes: ① This parameter is periodically sampled and not 100% tested.
② DO Output.
③ DB Output.

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AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V±5%

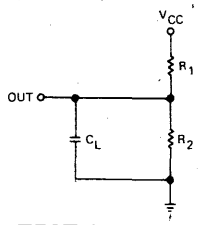
PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input to Output Delay DC Outputs		t_{PD1}			25	ns	C_L = 30 pF, R_1 = 300Ω, R_2 = 600Ω ④
Input to Output Delay DB Outputs	8216	t_{PD2}			30	ns	C_L = 300 pF, R_1 = 90Ω,
	8226	t_{PD2}			25	ns	R_2 = 180Ω ④
Output Enable Time	8216	t_E			65	ns	② ④
	8226	t_E			54	ns	
Output Disable Time		t_D			35	ns	③ ④

Notes: ① Typical values are for T_a = 25°C, V_{CC} = 5.0V

② DO Outputs, C_L = 30 pF, R_1 = 300/10 KΩ, R_2 = 600/1 KΩ,
DB Outputs, C_L = 300 pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.

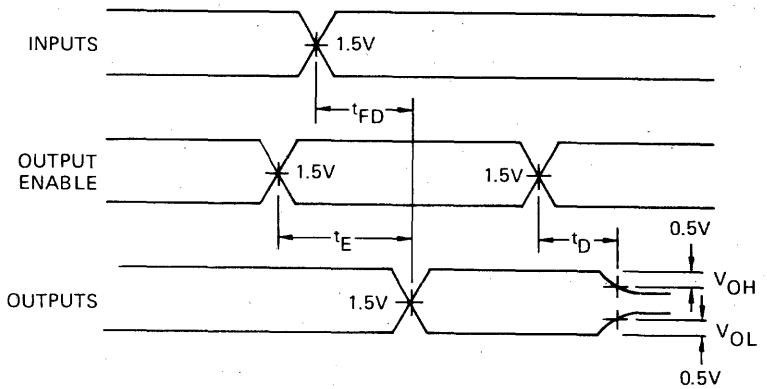
③ DO Outputs, C_L = 5 pF, R_1 = 300/10 KΩ, R_2 = 600/1 KΩ,
DB Outputs, C_L = 5 pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.

④ Input pulse amplitude: 2.5V
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 volt levels.

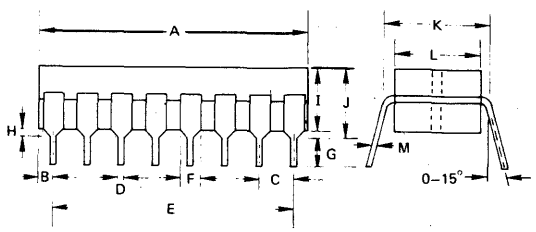


TEST CIRCUIT

TIMING WAVEFORMS

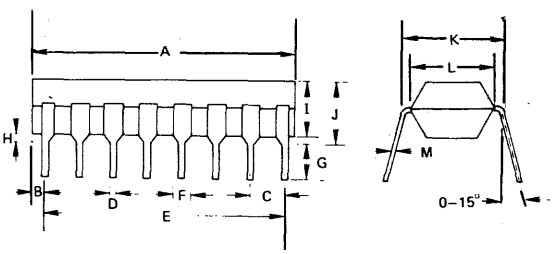


PACKAGE OUTLINE
μPB8216C/D
μPB8226C/D



μPB8216/8226D (Cerdip)

ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{0.05}$	$0.0098^{+0.0039}_{0.0019}$



μPB8216/8226C (Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX	0.76 MAX
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN
H	0.5 MIN	0.02 MIN
I	4.05 MAX	0.16 MAX
J	4.55 MAX	0.18 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{0.05}$	0.01

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PROGRAMMABLE COMMUNICATION INTERFACE

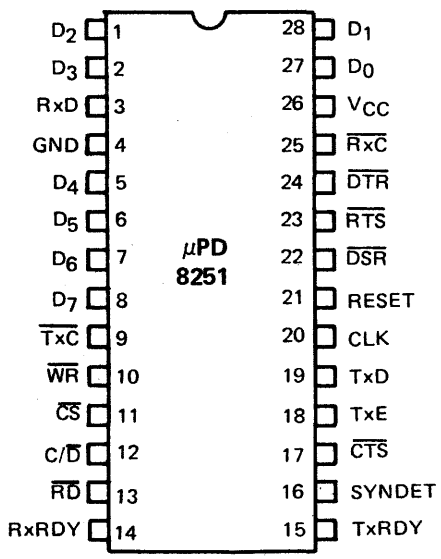
DESCRIPTION

The μPD8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is designed for microcomputer systems data communications. The USART is used as a peripheral and is programmed by the μPD8080 or other processor to communicate in commonly used serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART STATUS including data format errors and control signals such as TxE and SYNDET is available to the processor at any time.

FEATURES

- Asynchronous or Synchronous Operation
  - Asynchronous:
    - 5-8 Bit Characters
    - Clock Rate – 1, 16 or 64 x Baud Rate
    - Break Character Generation
    - Select 1, 1-1/2, or 2 Stop Bits
    - False Start Bit Detector
  - Synchronous:
    - 5-8 Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
    - Single or Double Sync Characters
- Baud Rate – Synchronous – DC to 56K Baud
  – Asynchronous – DC to 9.6K Baud
- Full Duplex, Double Buffered Transmitter and Receiver
- Parity, Overrun and Framing Flags
- Fully Compatible with 8080
- All Inputs and Outputs are TTL Compatible
- Single +5 Volt Supply
- Separate Device, Receive and Transmit TTL Clocks
- 28 Pin Plastic DIP Package
- N-Channel MOS Technology

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock (TTL)
TxD	Transmitter Data
RxC	Receiver Clock (TTL)
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

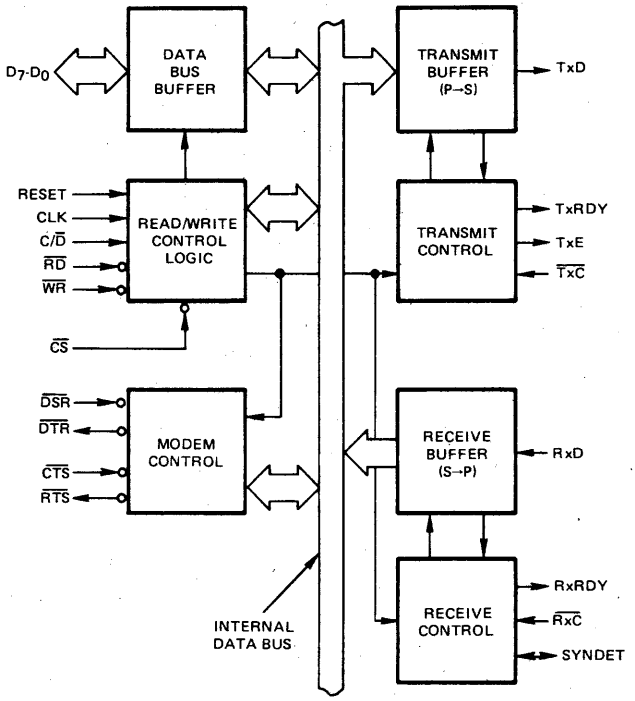
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FUNCTIONAL DESCRIPTION

The μPD8251 Universal Synchronous/Asynchronous Receiver/Transmitter is designed specifically for 8080 microcomputer systems but works with most 8-bit processors. Operation of the 8251, like other I/O devices in the 8080 family, is programmed by system software for maximum flexibility.

In the receive mode, a communication interface device must convert incoming serial format data into parallel data and make certain format checks on the data. And in the transmit mode, the device must format data into serial data. The device must also supply or remove characters or bits that are unique to the communication format in use. By performing conversion and formatting services automatically, the USART appears to the processor as a simple or "transparent" input or output of byte-oriented parallel data.

BLOCK DIAGRAM



BASIC OPERATION

C/D	RD	WR	CS	
0	0	1	0	8251 → Data Bus
0	1	0	0	Data Bus → 8251
1	0	1	0	Status → Data Bus
1	1	0	0	Data Bus → Control
X	X	X	1	Data Bus → 3-State
X	1	1	0	

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C
All Output Voltages	−0.5 to +7 Volts
All Input Voltages	−0.5 to +7 Volts
Supply Voltages	−0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

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DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 5%; GND = 0V

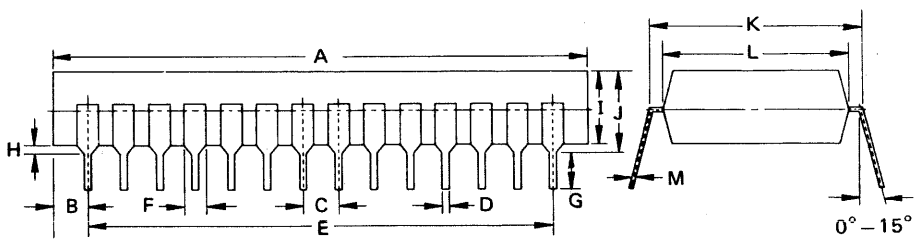
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	GND –.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.7 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = –100 μA
Data Bus Leakage	I_{DL}			–50	μA	V_{OUT} = 0.45V
				10		V_{OUT} = V_{CC}
Input Load Current	I_{IL}			10	μA	@5.5V
Power Supply Current	I_{CC}		45	80	mA	

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

PACKAGE OUTLINE μPD8251C



ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

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AC CHARACTERISTICS

BUS PARAMETERS: ①

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 5%; GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
READ						
Address Stable before $\overline{READ}$, ($\overline{CS}$, C/$\overline{D}$)	t_{AR}	50			ns	
Address Hold Time for $\overline{READ}$, ($\overline{CS}$, $\overline{CD}$)	t_{RA}	5			ns	
$\overline{READ}$ Pulse Width	t_{RR}	430			ns	
Data Delay from $\overline{READ}$	t_{RD}			350	ns	C_L = 100 pF
$\overline{READ}$ to Data Floating	t_{DF}			200	ns	C_L = 100 pF
		25				C_L = 15 pF
Recovery Time Between WRITES ②	t_{RV}	6			t_{CY}	
WRITE						
Address Stable before $\overline{WRITE}$	t_{AW}	20			ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	20			ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400			ns	
Data Set-Up Time for $\overline{WRITE}$	t_{DW}	200			ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	40			ns	
OTHER TIMING						
Clock Period ③	t_{CY}	.420		1.35	μs	
Clock Pulse Width	$t_{\phi W}$	220		0.7t_{CY}	ns	
Clock Rise and Fall Time	$t_{R,tF}$	0		50	ns	
TxD Delay from Falling Edge of $\overline{TxC}$	t_{DTx}			1	μs	C_L = 100 pF
Rx Data Set-Up Time to Sampling Pulse	t_{SRx}	2			μs	C_L = 100 pF
Rx Data Hold Time to Sampling Pulse	t_{HRx}	2			μs	C_L = 100 pF
Transmitter Input Clock Frequency	f_{Tx}					
1X Baud Rate		DC		56	KHz	
16X and 64X Baud Rate		DC		520	KHz	
Transmitter Input Clock Pulse Width	t_{TPW}					
1X Baud Rate		12			t_{CY}	
16X and 64X Baud Rate		1			t_{CY}	
Transmitter Input Clock Pulse Delay	t_{TPD}					
1X Baud Rate		15			t_{CY}	
16X and 64X Baud Rate		3			t_{CY}	
Receiver Input Clock Frequency	f_{Rx}					
1X Baud Rate		DC		56	KHz	
16X and 64X Baud Rate		DC		520	KHz	
Receiver Input Clock Pulse Width	t_{RPW}					
1X Baud Rate		12			t_{CY}	
16X and 64X Baud Rate		1			t_{CY}	
Receiver Input Clock Pulse Delay	t_{RPD}					
1X Baud Rate		15			t_{CY}	
16X and 64X Baud Rate		3			t_{CY}	
TxRDY Delay from Center of Data Bit	t_{Tx}			16	t_{CY}	C_L = 50 pF
RxRDY Delay from Center of Data Bit	t_{Rx}			20	t_{CY}	
Internal Syndet Delay from Center of Data Bit	t_{IS}			25	t_{CY}	
External Syndet Set-Up Time before Falling Edge of $\overline{RxC}$	t_{ES}	16		16	t_{CY}	
TxEMPTY Delay from Center of Data Bit	t_{TxE}			16	t_{CY}	C_L = 50 pF
Control Delay from Rising Edge of WRITE (TxE, $\overline{DTR}$, $\overline{RTS}$)	t_{WC}				t_{CY}	
Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)	t_{CR}	16			t_{CY}	

Notes: ① AC timings measured at V_{OH} = 2.0, V_{OL} = 0.8, and with load circuit of Figure 1.

② This recovery time is for initialization only, when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.

③ The TxC and RxC frequencies have the following limitations with respect to CLK.
For 1X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$
For 16X and 64X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(4.5\ t_{CY})$

④ Reset Pulse Width = 6 t_{CY} minimum.

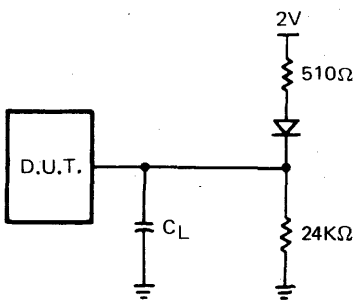
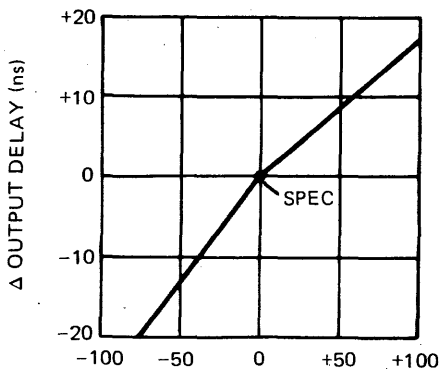


Figure 1.

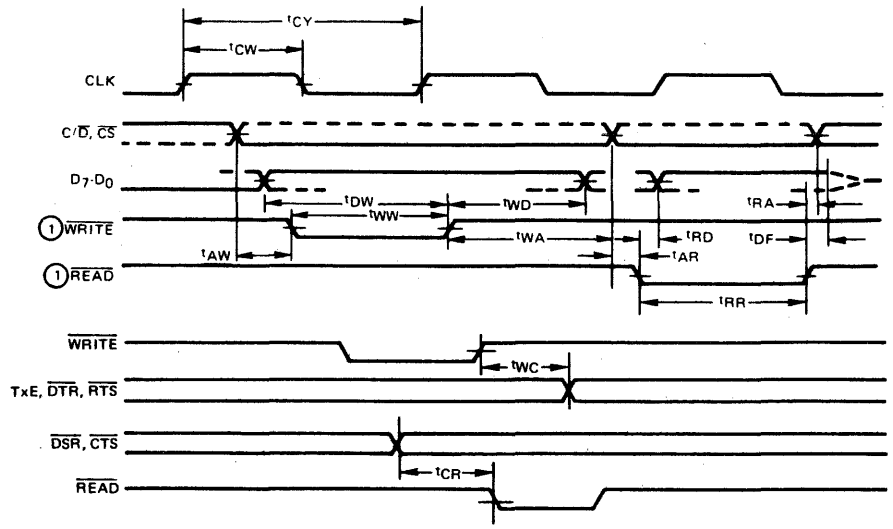
TEST LOAD CIRCUIT



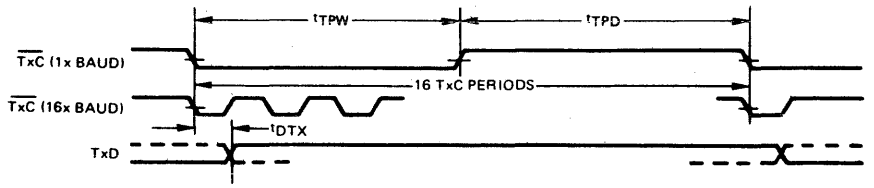
Typical Δ Output Delay Versus Δ Capacitance (pF)

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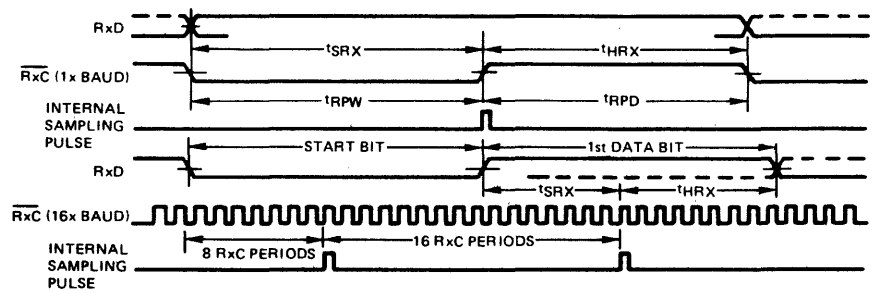
TIMING WAVEFORMS



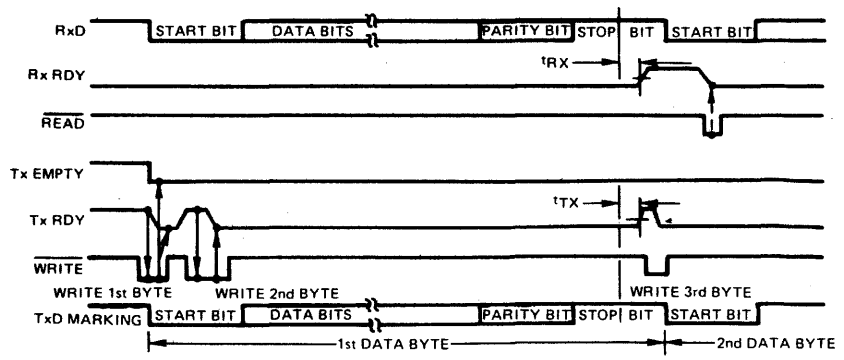
READ AND WRITE TIMING



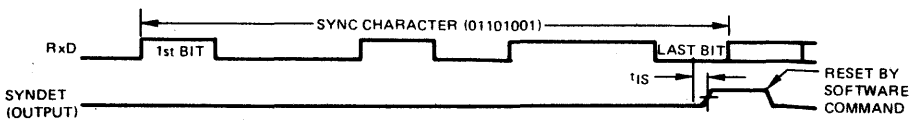
TRANSMITTER CLOCK AND DATA



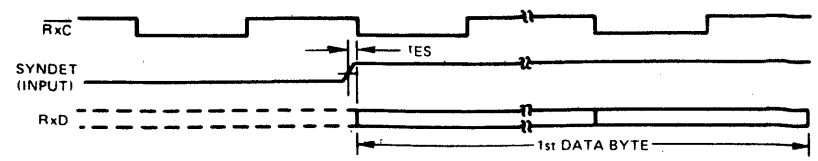
RECEIVER CLOCK AND DATA



TxRDY AND RxRDY TIMING (ASYNC MODE)



INTERNAL SYNC DETECT



EXTERNAL SYNC DETECT

Note: (1) Write and Read pulses have no timing limitation with respect to CLK.

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PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1, 2, 27, 28 5 – 8	$D_7 - D_0$	Data Bus Buffer	An 8-bit, 3-state bi-directional buffer used to interface the 8251 to the processor data bus. Data is transmitted or received by the buffer in response to input/output or Read/Write instructions from the processor. The Data Bus Buffer also transfers Control words, Command words, and Status.
26	V_{CC}	V_{CC} Supply Voltage	+5 volt supply
4	GND	Ground	Ground
Read/Write Control Logic			This logic block accepts inputs from the processor Control Bus and generates control signals for overall USART operation. The Mode Instruction and Command Instruction registers that store the control formats for device functional definition are located in the Read/ Write Control Logic.
21	RESET	Reset	A "one" on this input forces the USART into the "Idle" mode where it will remain until reinitialized with a new set of control words. Minimum RESET pulse width is t_{CY}.
20	CLK	Clock Pulse	The CLK input provides for internal device timing and is usually connected to the Phase 2 (TTL) output of the μPB8224 Clock Generator. External inputs and outputs are not referenced to CLK, but the CLK frequency must be 30 times the Receiver or Transmitter clocks in the synchronous mode and 4.5 times for the asynchronous mode.
10	$\overline{WR}$	Write Data	A "zero" on this input instructs the μPD8251 to accept the data or control word which the processor is writing out to the USART via the data bus.
13	$\overline{RD}$	Read Data	A "zero" on this input instructs the μPD8251 to place the data or status information onto the Data Bus for the processor to read.
12	C/$\overline{D}$	Control/Data	The Control/Data input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs USART to accept or provide either a data-character, control word or status information via the Data Bus. 0 = Data; 1 = Control.
11	$\overline{CS}$	Chip Select	A "zero" on this input enables the USART for reading and writing to the processor.
Modem Control			The μPD8251 has a set of control inputs and outputs which may be used to simplify the interface to a Modem.
22	$\overline{DSR}$	Data Set Ready	The Data Set Ready input can be tested by the processor via Status information. The $\overline{DSR}$ input is normally used to test Modem Data Set Ready condition.
24	$\overline{DTR}$	Data Terminal Ready	The Data Terminal Ready output can be controlled via the Command word. The $\overline{DTR}$ output is normally used to drive Modem Data Terminal Ready or Rate Select lines.
23	$\overline{RTS}$	Request to Send	The Request to Send output can be controlled via the Command word. The $\overline{RTS}$ output is normally used to drive the Modem Request to Send line.
17	$\overline{CTS}$	Clear to Send	A "zero" on the Clear to Send input enables the USART to transmit serial data if the TxEN bit in the Command Instruction register is enabled (one).

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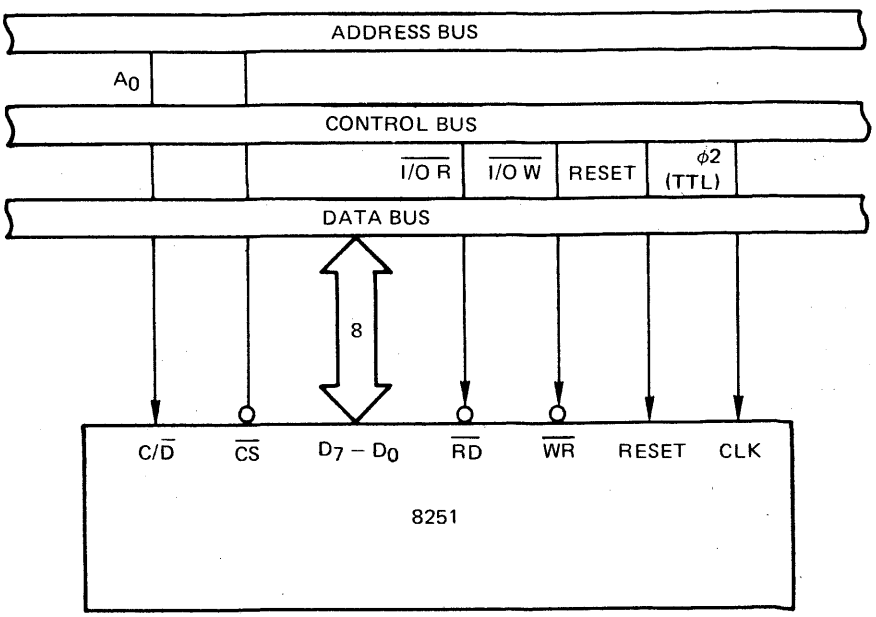
TRANSMIT BUFFER/ CONVERTER

The Transmit Buffer/Converter receives parallel data from the Data Bus Buffer via the internal data bus, converts parallel to serial data, inserts the necessary characters or bits needed for the programmed communication format and outputs composite serial data on the TxD output.

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Transmit Control Logic			The Transmit Control Logic accepts and outputs all external and internal signals necessary for serial data transmission.
15	TxRDY	Transmitter Ready	Transmitter Ready signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the Status information for Polled operation. Loading a character from the processor automatically resets TxRDY.
18	TxE	Transmitter Empty	The Transmitter Empty output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal end of a transmission and request the processor to "turn the line around." The TxEn bit in the command instruction does not effect TxE. In the Synchronous mode, a "one" on this output indicates that a Sync character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded.
9	$\overline{TxC}$	Transmitter Clock	The Transmitter Clock controls the serial character transmission rate. In the Asynchronous mode, the $\overline{TxC}$ frequency is a multiple of the actual Baud Rate. Two bits of the Mode Instruction select the multiple to be 1x, 16x, or 64x the Baud Rate. In the Synchronous mode, the $\overline{TxC}$ frequency is automatically selected to equal the actual Baud Rate. Note that for both Synchronous and Asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{TxC}$.
19	TxD	Transmitter Data	The Transmit Control Logic outputs the composite serial data stream on this pin.

8251 INTERFACE TO 8080 STANDARD SYSTEM BUS



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RECEIVER BUFFER

The Receiver Buffer accepts serial data input at the $\overline{RxD}$ pin and converts the data from serial to parallel format. Bits or characters required for the specific communication technique in use are checked and then an eight-bit "assembled" character is readied for the processor. For communication techniques which require less than eight bits, the μPD8251 sets the extra bits to "zero."

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Receiver Control Logic			This block manages all activities related to incoming data.
14	RxRDY	Receiver Ready	The Receiver Ready output indicates that the Receiver Buffer is ready with an "assembled" character for input to the processor. For Polled operation, the processor can check RxRDY using a Status Read or RxRDY can be connected to the processor interrupt structure. Note that reading the character to the processor automatically resets RxRDY.
25	$\overline{RxC}$	Receiver Clock	The Receiver Clock is the rate at which the incoming character is received. In the Asynchronous mode, the $\overline{RxC}$ frequency may be 1,16 or 64 times the actual Baud Rate but in the Synchronous mode the $\overline{RxC}$ frequency must equal the Baud Rate. Two bits in the mode instruction select Asynchronous at 1x, 16x or 64x or Synchronous operation at 1x the Baud Rate. Unlike $\overline{TxC}$, data is sampled by the μPD8251 on the rising edge of $\overline{RxC}$. (1)
3	RxD	Receiver Data	A composite serial data stream is received by the Receiver Control Logic on this pin.
16	SYNDET	Sync Detect	The SYNC Detect pin is only used in the Synchronous mode. The μPD8251 may be programmed through the Mode Instruction to operate in either the internal or external Sync mode and SYNDET then functions as an output or input respectively. In the internal Sync mode, the SYNDET output will go to a "one" when the μPD8251 has located the SYNC character in the Receive mode. If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second SYNC character. SYNDET is automatically reset to "zero" upon a Status Read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input will cause the μPD8251 to start assembling data character on the next falling edge of $\overline{RxC}$. The length of the SYNDET input should be at least one $\overline{RxC}$ period, but may be removed once the μPD8251 is in SYNC.

Note: (1) Since the μPD8251 will frequently be handling both the reception and transmission for a given link, the Receive and Transmit Baud Rates will be same. $\overline{RxC}$ and $\overline{TxC}$ then require the same frequency and may be tied together and connected to a single clock source or Baud Rate Generator.

Examples:

If the Baud Rate equals 110 (Async):
- $\overline{RxC}$ or $\overline{TxC}$ equals 110 Hz (1x)
- $\overline{RxC}$ or $\overline{TxC}$ equals 1.76 KHz (16x)
- $\overline{RxC}$ or $\overline{TxC}$ equals 7.04 KHz (64x)

If the Baud Rate equals 300:
- $\overline{RxC}$ or $\overline{TxC}$ equals 300 Hz (1x) A or S
- $\overline{RxC}$ or $\overline{TxC}$ equals 4800 Hz (16x) A only
- $\overline{RxC}$ or $\overline{TxC}$ equals 19.2 KHz (64x) A only

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OPERATIONAL DESCRIPTION

A set of control words must be sent to the μPD8251 to define the desired mode and communications format. The control words will specify the BAUD RATE FACTOR (1x, 16x, 64x), CHARACTER LENGTH (5 to 8), NUMBER OF STOP BITS (1, 1-1/2, 2), ASYNCHRONOUS or SYNCHRONOUS MODE, SYNDET (IN or OUT), PARITY, etc.

After receiving the control words, the μPD8251 is ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. When the processor writes a character to the USART, TxRDY is automatically reset.

Concurrently, the μPD8251 may receive serial data; and after receiving an entire character, the RxRDY output is raised to indicate a completed character is ready for the processor. The processor fetch will automatically reset RxRDY.

Note: The μPD8251 may provide faulty RxRDY for the first read after power-on or for the first read after receive is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. But this is not the case for the first read after hardware or software reset after the device operation has once been established.

The μPD8251 cannot transmit until the TxEN (Transmitter Enable) bit has been set by a Command Instruction and until the $\overline{CTS}$ (Clear to Send) input is a "zero". TxD is held in the "marking" state after Reset awaiting new Command Words.

μPD8251 PROGRAMMING

The USART must be loaded with a group of two to four control words provided by the processor before data reception and transmission can begin. A Reset (internal or external) must immediately proceed the control words which are used to program the complete operational description of the communications interface. If an external RESET is not available, three successive 00 Hex or two successive 80 Hex command instructions ($C/\overline{D}$ = 1) followed by a software reset command instruction (40 Hex) can be used to initialize the 8251.

There are two control word formats:

1. Mode Instruction
2. Command Instruction

MODE INSTRUCTION

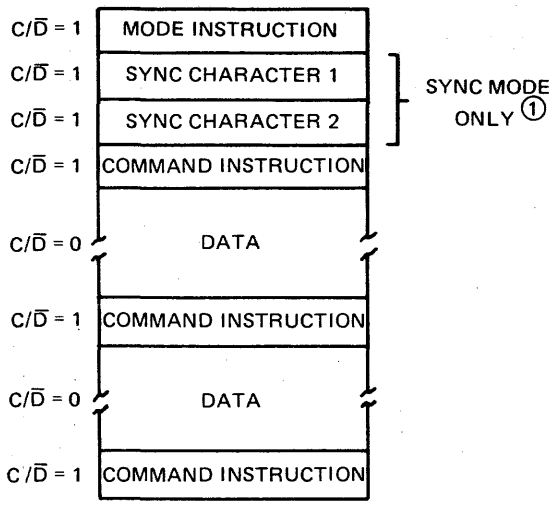
This control word specifies the general characteristics of the interface regarding the SYNCHRONOUS or ASYNCHRONOUS MODE, BAUD RATE FACTOR, CHARACTER LENGTH, PARITY, and NUMBER OF STOP BITS. Once the Mode Instruction has been received, SYNC characters or Command Instructions may be inserted depending on the Mode Instruction content.

COMMAND INSTRUCTION

This control word will be interpreted as a SYNC character definition if immediately preceded by a Mode Instruction which specified a Synchronous format. After the SYNC character(s) are specified or after an Asynchronous Mode Instruction, all subsequent control words will be interpreted as an update to the Command Instruction. Command Instruction updates may occur at any time during the data block. To modify the Mode Instruction, a bit may be set in the Command Instruction which causes an internal Reset which allows a new Mode Instruction to be accepted.

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TYPICAL DATA BLOCK



NOTE ① The second SYNC character is skipped if MODE instruction has programmed the 8251 to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the 8251 to ASYNC mode.

MODE INSTRUCTION DEFINITION

The μPD8251 can operate in either Asynchronous or Synchronous communication modes. Understanding how the Mode Instruction controls the functional operation of the USART is easiest when the device is considered to be two separate components, one asynchronous and the other synchronous, which share the same support circuits and package. Although the format definition can be changed at will or "on the fly", the two modes will be explained separately for clarity.

ASYNCHRONOUS TRANSMISSION

When a data character is written into the μPD8251, the USART automatically adds a START bit (low level or "space") and the number of STOP bits (high level or "mark") specified by the Mode Instruction. If Parity has been enabled, an odd or even Parity bit is inserted just before the STOP bits(s), as specified by the Mode Instruction. Then, depending on $\overline{CTS}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of $\overline{TxC}$ at $\overline{TxC}$, $\overline{TxC}$/16 or $\overline{TxC}$/64, as defined by the Mode Instruction.

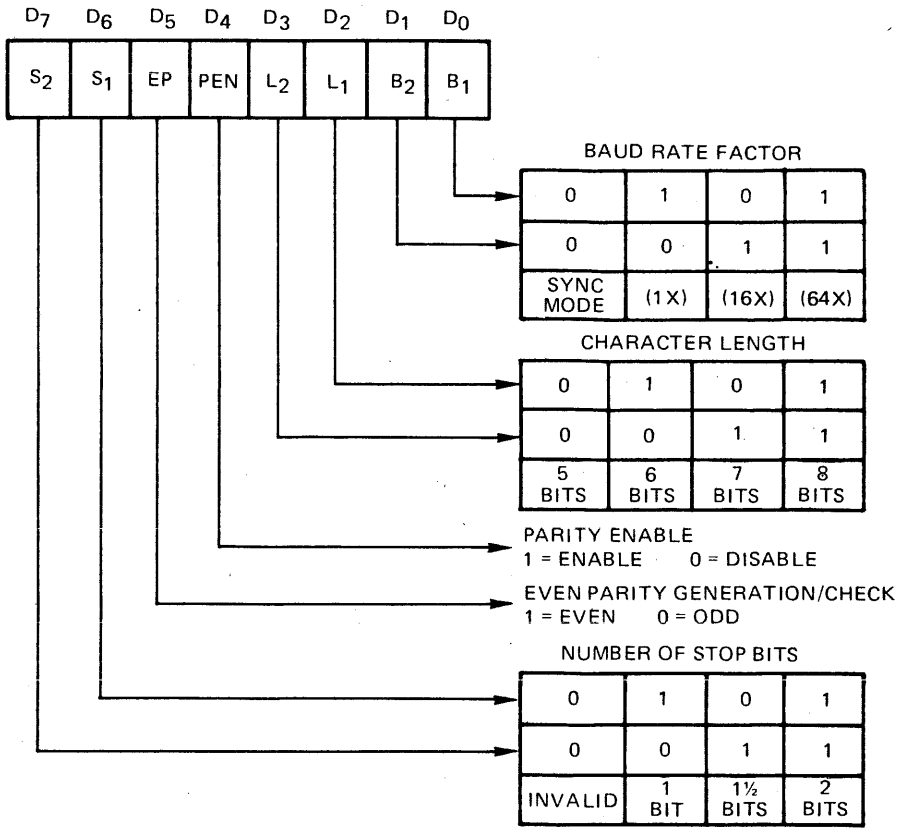
If no data characters have been loaded into the μPD8251, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the START bit of the next character provided by the processor. TxD may be forced to send a BREAK (continuously low) by setting the correct bit in the Command Instruction.

ASYNCHRONOUS RECEIVE

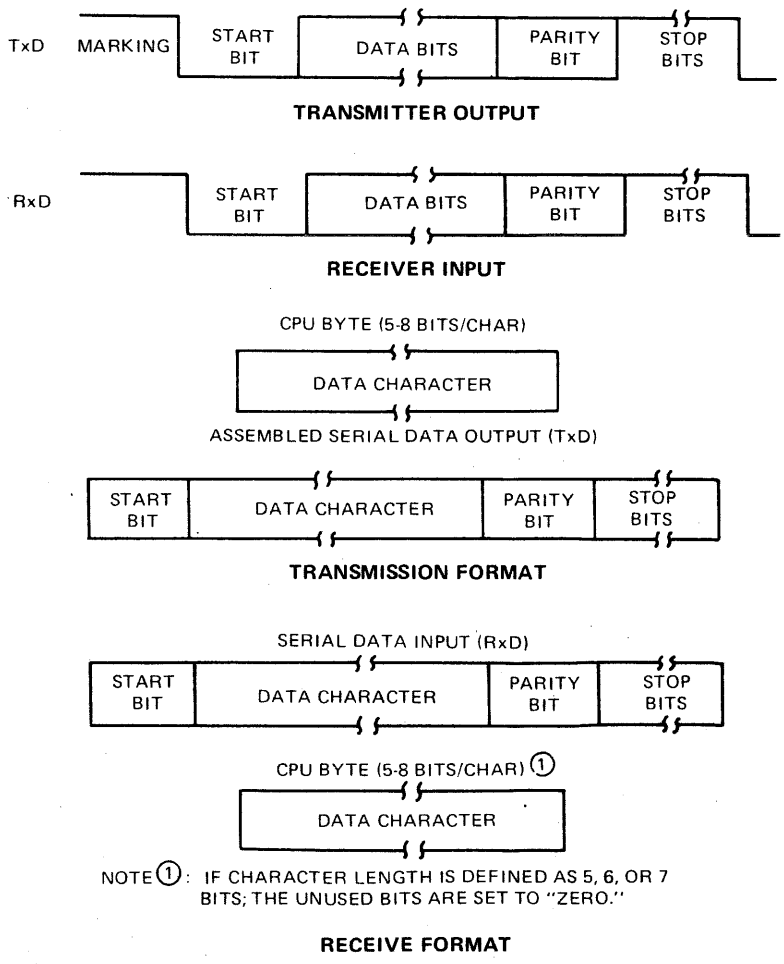
The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge at RxD signals the possible beginning of a START bit and a new character. The START bit is checked by testing for a "low" at its nominal center as specified by the BAUD RATE. If a "low" is detected again, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and STOP bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{RxC}$. If a high is not detected for the STOP bit, which normally signals the end of an input character, a framing error (FE) will be set. After a valid STOP bit, the input character is loaded into the parallel Data Bus Buffer of the μPD8251 and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and the overrun flag (OE) is set. All the error flags can be reset by setting a bit in the Command Instruction. Error flag conditions will not stop subsequent USART operation.

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MODE INSTRUCTION FORMAT ASYNCHRONOUS MODE



TRANSMIT/RECEIVE FORMAT ASYNCHRONOUS MODE



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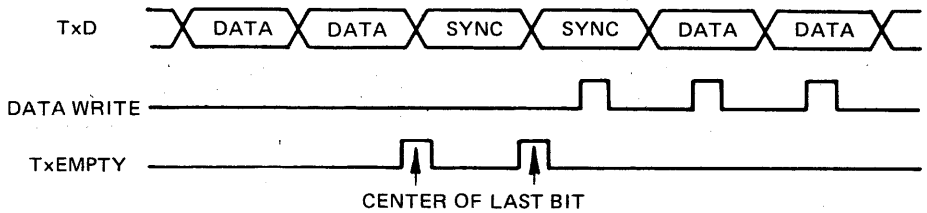
SYNCHRONOUS TRANSMISSION

As in Asynchronous transmission, the TxD output remains "high" (marking) until the μPD8251 receives the first character from the processor which is usually a SYNC character. After a Command Instruction has set TxEN and after Clear to Send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ and the same rate as $\overline{TxC}$.

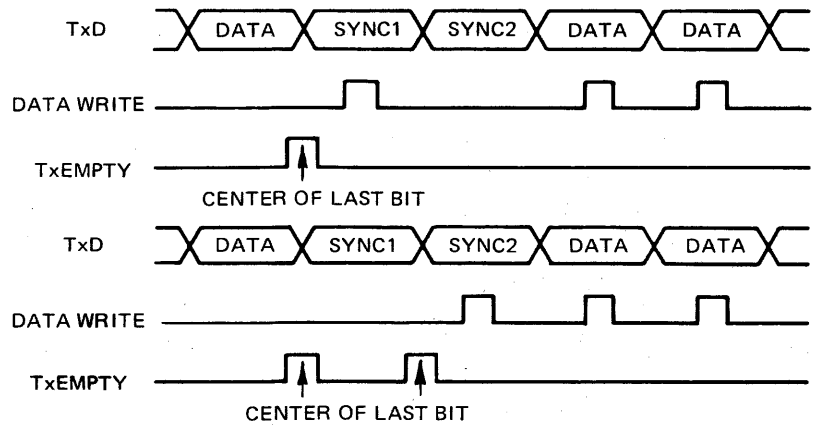
Once transmission has started, Synchronous Mode format requires that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the μPD8251 Transmitter Buffer becomes empty, the SYNC character(s) loaded directly following the Mode Instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until new data characters are available for transmission. If the μPD8251 becomes empty, and must send the SYNC character(s), the TxEMPTY output is raised to signal the processor that the Transmitter Buffer is empty and SYNC characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

TxEMPTY go high at the middle of the last data bit when the Transmit Register is EMPTY. TxEMPTY goes low again as sync characters are transmitted. See figure below.

FOR SINGLE SYNC CHARACTER OPERATION



FOR DOUBLE SYNC CHARACTER OPERATION (BISYNC)



SYNCHRONOUS RECEIVE

In Synchronous Receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, and the Enter HUNT (EH) bit has been set by a Command Instruction, the receiver goes into the HUNT mode.

Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the Receiver Buffer is compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the SYNC character(s) programmed have been detected, the μPD8251 leaves the HUNT mode and is in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a STATUS READ.

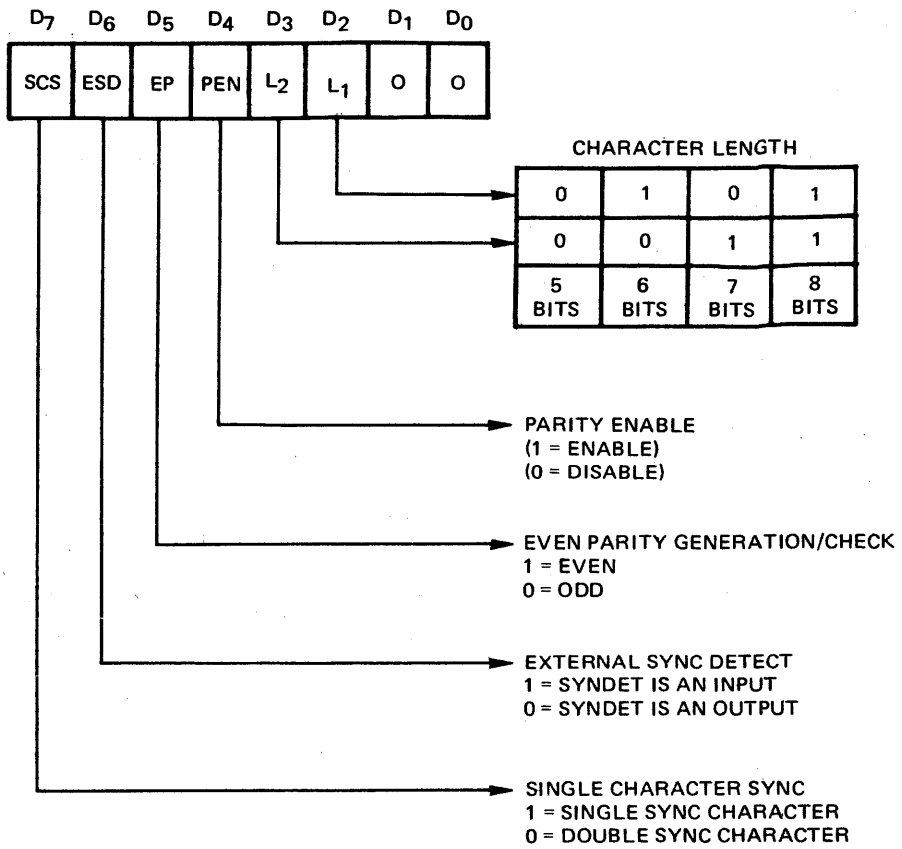
If external SYNC has been specified in the Mode Instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

Parity and Overrun Errors are treated the same in the Synchronous as in the Asynchronous Mode. Framing errors do not apply in the Synchronous format.

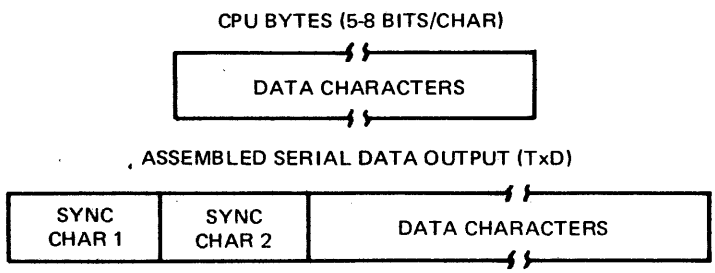
The processor may command the receiver to enter the HUNT mode with a Command Instruction which sets Enter HUNT (EH) if synchronization is lost.

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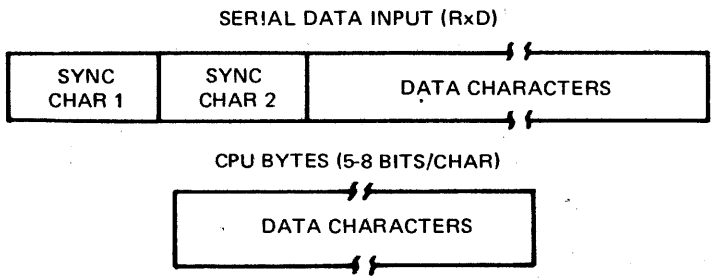
MODE INSTRUCTION FORMAT SYNCHRONOUS MODE



TRANSMIT/RECEIVE FORMAT SYNCHRONOUS MODE



TRANSMIT FORMAT



RECEIVE FORMAT

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COMMAND INSTRUCTION FORMAT

After the functional definition of the μPD8251 has been specified by the Mode Instruction and the SYNC character(s) have been entered, if in SYNC mode, the USART is ready to receive Command Instructions and begin communication. A Command Instruction is used to control the specific operation of the format selected by the Mode Instruction. Enable Transmit, Enable Receive, Error Reset and Modem Controls are controlled by the Command Instruction.

After the Mode Instruction and the SYNC character(s), as needed, are loaded, all subsequent "control writes" ($C/\overline{D} = 1$) will load or overwrite the Command Instruction register. A Reset operation (internal via CMD IR or external via the RESET input) will cause the μPD8251 to interpret the next "control write", which must immediately follow the reset, as a Mode Instruction.

STATUS READ FORMAT

It is frequently necessary for the processor to examine the "status" of an active interface device to determine if errors have occurred or to notice other conditions which require a response from the processor. The μPD8251 has features which allow the processor to "read" the device status at any time. A data fetch is issued by the processor while holding the $C/\overline{D}$ input "high" to obtain device Status Information. Many of the bits in the status register are copies of external pins. This dual status arrangement allows the μPD8251 to be used in both Polled and interrupt driven environments. Status update can have a maximum delay of a 16 clock period.

PARITY ERROR

When a parity error is detected, the PE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. PE being set does not inhibit USART operation.

OVERRUN ERROR

If the processor fails to read a data character before the one following is available, the OE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. Although OE being set does not inhibit USART operation, the previously received character is overwritten and lost.

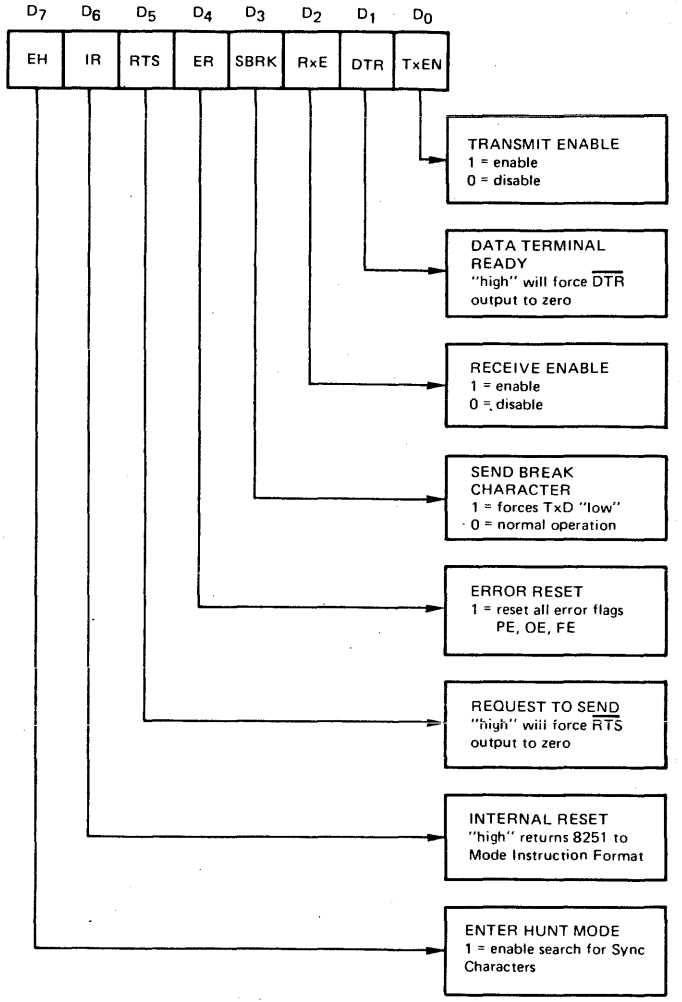
FRAMING ERROR ①

If a valid STOP bit is not detected at the end of a character, the FE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. FE being set does not inhibit USART operation.

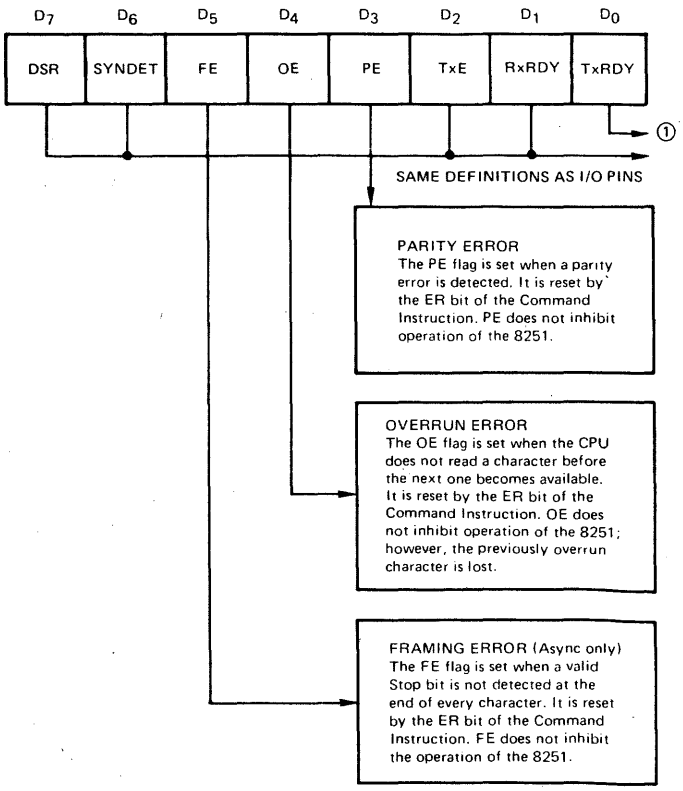
Note: ① ASYNC mode only.

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COMMAND INSTRUCTION FORMAT



STATUS READ FORMAT



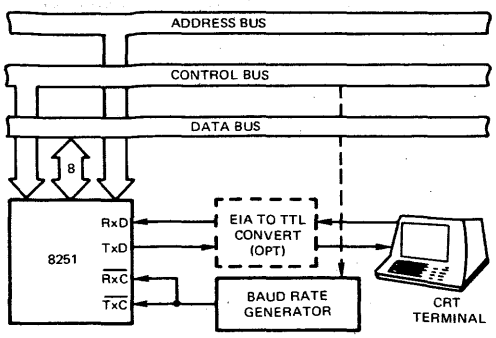
Note: ① TxRDY status bit is not totally equivalent to the TxRDY output pin, the relationship is as follows:

TxRDY status bit = DB Buffer Empty

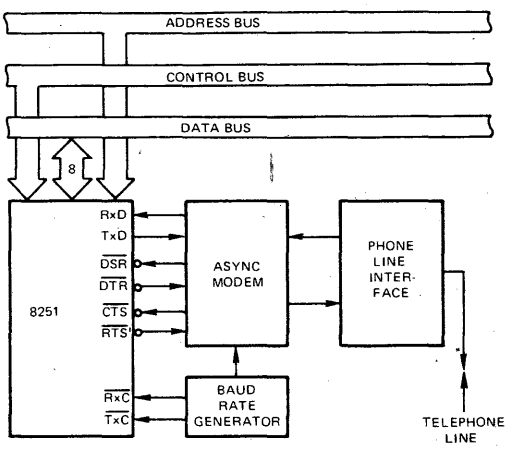
TxRDY (pin 15) = DB Buffer Empty • CTS • TxEn

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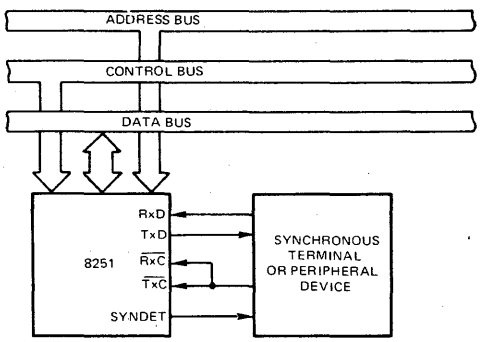
APPLICATION OF THE μPD8251



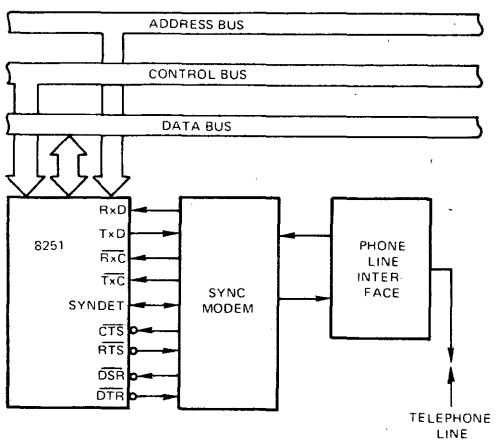
ASYNCHRONOUS SERIAL INTERFACE TO CRT TERMINAL, DC to 9600 BAUD



ASYNCHRONOUS INTERFACE TO TELEPHONE LINES



SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES

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PROGRAMMABLE PERIPHERAL INTERFACE

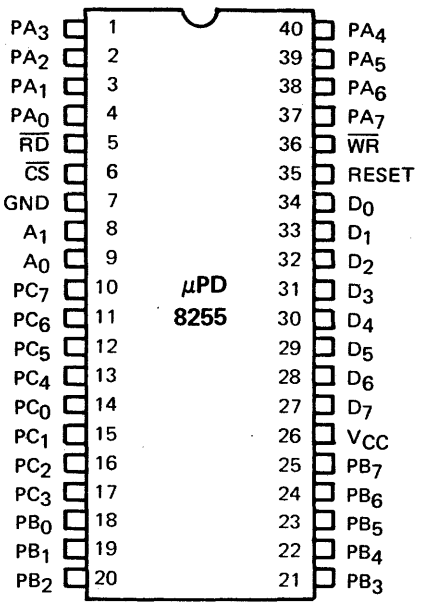
DESCRIPTION

The μPD8255 is a general purpose programmable INPUT/OUTPUT device designed for use with the 8080A microprocessor. Twenty-four (24) I/O lines may be programmed in two groups of twelve (group I and group II) and used in three major modes of operation. In the Basic mode, (MODE 0), each group of twelve I/O pins may be programmed in a set of 8 and a set of 4 to be input or output. In the Strobed mode, (MODE 1), each group may be programmed to have 8 lines of input or output. Three of the remaining four pins in each group are used for handshaking strobes and interrupt control signals. The Bidirectional Bus mode, (MODE 2), uses the 8 lines of Port A for a bidirectional bus, and five lines from Port C for bus control signals. The μPD8255 is packaged in a 40 pin plastic DIP.

FEATURES

- Fully Compatible with the 8080A Microprocessor Family
- All Inputs and Outputs TTL Compatible
- 24 Programmable I/O Pins
- Direct Bit SET/RESET Eases Control Application Interfaces
- 8 – 2 mA Darlington Drive Outputs for Printers and Displays
- LSI Drastically Reduces System Package Count
- Standard 40 Pin Dual-In-Line Plastic Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (Bi-Directional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7-PA_0	Port A (Bit)
PB_7-PB_0	Port B (Bit)
PC_7-PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

Rev/1

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FUNCTIONAL DESCRIPTION

General

The μPD8255 Programmable Peripheral Interface (PPI) is designed for use in 8080A microprocessor systems. Peripheral equipment can be effectively and efficiently interfaced to the 8080A data and control busses with the μPD8255. The μPD8255 is functionally configured to be programmed by system software to avoid external logic for peripheral interfaces.

Data Bus Buffer

The 3-state, bidirectional, eight bit Data Bus Buffer (D_0-D_7) of the μPD8255 can be directly interfaced to the 8080A system Data Bus (D_0-D_7). The Data Bus Buffer is controlled by execution of IN and OUT instructions by the 8080A. Control Words and Status information are also transmitted via the Data Bus Buffer.

Read/Write and Control Logic

This block manages all of the internal and external transfers of Data, Control and Status. Through this block, the processor Address and Control busses can control the peripheral interfaces.

Chip Select, $\overline{CS}$, pin 6

A Logic Low, V_{IL}, on this input enables the μPD8255 for communication with the 8080A.

Read, $\overline{RD}$, pin 5

A Logic Low, V_{IL}, on this input enables the μPD8255 to send Data or Status to the processor via the Data Bus Buffer.

Write, $\overline{WR}$, pin 36

A Logic Low, V_{IL}, on this input enables the Data Bus Buffer to receive Data or Control Words from the processor.

Port Select 0, A_0, pin 9

Port Select 1, A_1, pin 8

These two inputs are used in conjunction with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ to control the selection of one of three ports on the Control Word Register. A_0 and A_1 are usually connected to A_0 and A_1 of the processor Address Bus.

Reset, pin 35

A Logic High, V_{IH}, on this input clears the Control Register and sets ports A, B, and C to the input mode, The input latches in ports A, B, and C are not cleared.

Group I and Group II Controls

Through an OUT instruction in System Software from the processor, a control word is transmitted to the μPD8255. Information such as "MODE," "Bit SET," and "Bit RESET" is used to initialize the functional configuration of each I/O port.

Each group (I and II) accepts "commands" from the Read/Write Control Logic and "control words" from the internal data bus and in turn controls its associated I/O ports.

Group I – Port A and upper Port C (PC_7-PC_4)

Group II – Port B and lower Port C (PC_3-PC_0)

While the Control Word Register can be written into, the contents can not be read back to the processor.

Ports A, B, and C

The three 8-bit I/O ports (A, B, and C) in the μPD8255 can all be configured to meet a wide variety of functional requirements through system software. The effectiveness and flexibility of the μPD8255 is further enhanced by special features unique to each of the ports.

Port A = An 8-bit data output latch/buffer and data input latch.

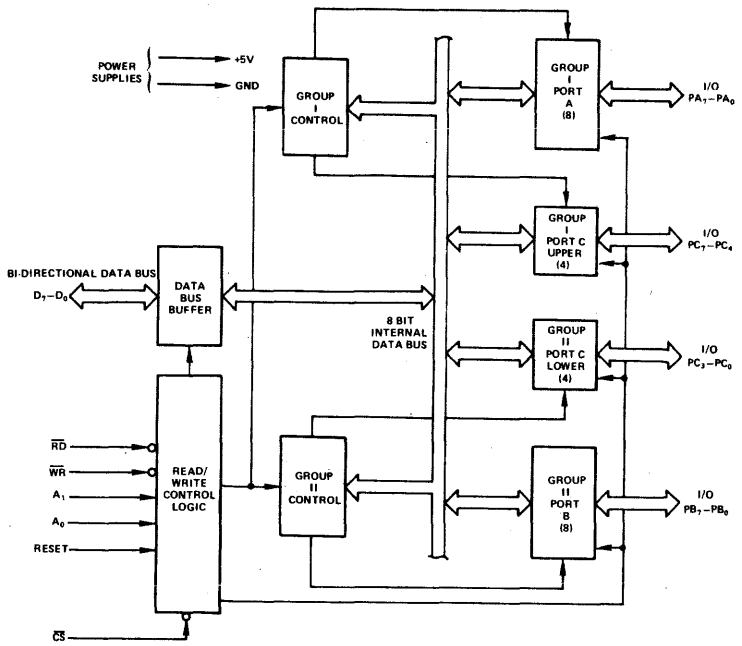
Port B = An 8-bit data input/output latch/buffer and an 8-bit data input buffer.

Port C = An 8-bit output latch/buffer and a data input buffer (input not latched).

Port C may be divided into two independent 4 bit control and status ports for use with Ports A & B.

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +125°C
All Output Voltages ①	-0.5 to +7 Volts
All Input Voltages ①	-0.5 to +7 Volts
Supply Voltages ①	-0.5 to +7 Volts

Note: ① With respect to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = +5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	V_{SS}-.5		0.8	V	
Input High Voltage	V_{IH}	2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 1.7 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = 50 μA (- 100 μA for D. B. Port)
Darlington Drive Current	I_{OH} ①	1	2	4	mA	V_{OH} = 1.5V, R_{EXT} = 750Ω
Power Supply Current	I_{CC}		40	120	mA	V_{CC} = +5V, Output Open
Input Leakage Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Input Leakage Current	I_{LIL}			-10	μA	V_{IN} = 0.4V
Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}; $\overline{CS}$ = 2.0V
Output Leakage Current	I_{LOL}			-10	μA	V_{OUT} = 0.4V, $\overline{CS}$ = 2.0V

Note: ① Any set of eight (8) outputs from either Port A, B, or C can source 2 mA into 1.5 volts.

CAPACITANCE

T_a = 25°C; V_{CC} = V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to V_{SS}

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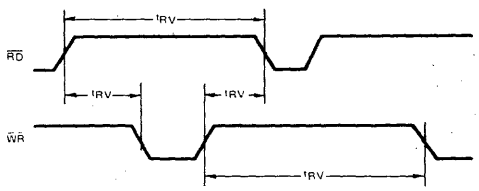
AC CHARACTERISTICS

8080 BUS PARAMETERS:
T_a = 0°C to +70°C; V_{CC} = +5V ± 5%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
READ						
Address Stable Before $\overline{READ}$	t_{AR}	50			ns	
Address Stable After $\overline{READ}$	t_{RA}	0			ns	
$\overline{READ}$ Pulse Width	t_{RR}	405			ns	
Data Valid From $\overline{READ}$	t_{RD}			295	ns	CL = 100 pF
Data Float After $\overline{READ}$	t_{DF}			150	ns	CL = 100 pF
		10			ns	CL = 15 pF
Time Between $\overline{READS}$ and/or $\overline{WRITES}$	t_{RV}	850			ns	②
WRITE						
Address Stable Before $\overline{WRITE}$	t_{AW}	20			ns	
Address Stable After $\overline{WRITE}$	t_{WA}	20			ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400			ns	
Data Valid To $\overline{WRITE}$ (L.E.)	t_{DW}	10			ns	
Data Valid After $\overline{WRITE}$	t_{WD}	35			ns	
OTHER TIMING						
$\overline{WR}$ = 0 To Output	t_{WB}			500	ns	CL = 50 pF
Peripheral Data Before $\overline{RD}$	t_{IR}	0			ns	
Peripheral Data After $\overline{RD}$	t_{HR}	50			ns	
$\overline{ACK}$ Pulse Width	t_{AK}	500			ns	
$\overline{STB}$ Pulse Width	t_{ST}	350			ns	
Per. Data Before T.E. Of $\overline{STB}$	t_{PS}	60			ns	
Per. Data After T.E. Of $\overline{STB}$	t_{PH}	150			ns	
$\overline{ACK}$ = 0 To Output	t_{AD}			400	ns	CL = 50 pF
$\overline{ACK}$ = 0 To Output Float	t_{KD}			300	ns	CL = 50 pF
		20				CL = 15 pF
$\overline{WR}$ = 1 To $\overline{OBF}$ = 0	t_{WOB}			300	ns	CL = 50 pF
$\overline{ACK}$ = 0 To $\overline{OBF}$ = 1	t_{AOB}			450	ns	CL = 50 pF
$\overline{STB}$ = 0 To IBF = 1	t_{SIB}			450	ns	CL = 50 pF
$\overline{RD}$ = 1 To IBF = 0	t_{RIB}			360	ns	CL = 50 pF
$\overline{RD}$ = 0 To INTR = 0	t_{RIT}			450	ns	CL = 50 pF
$\overline{STB}$ = 1 To INTR = 1	t_{SIT}			400	ns	CL = 50 pF
$\overline{ACK}$ = 1 To INTR = 1	t_{AIT}			400	ns	CL = 50 pF
$\overline{WR}$ = 0 To INTR = 0	t_{WIT}			850	ns	CL = 50 pF

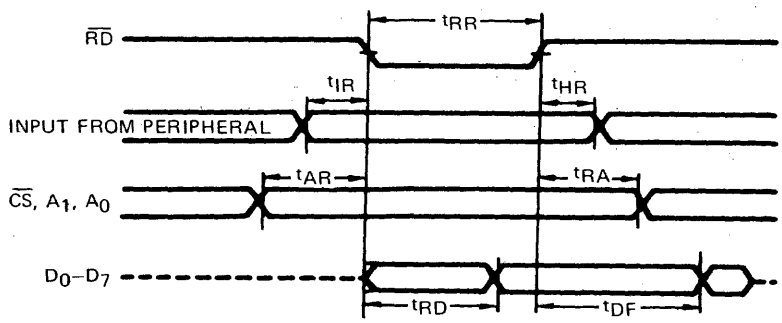
Notes: ① Period of Reset pulse must be at least 50 μs during or after power on. Subsequent Reset pulse can be 500 ns min.

②

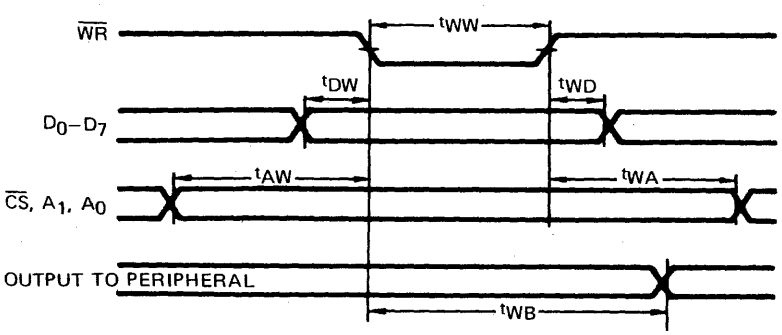


TIMING WAVEFORMS

MODE 0



BASIC INPUT

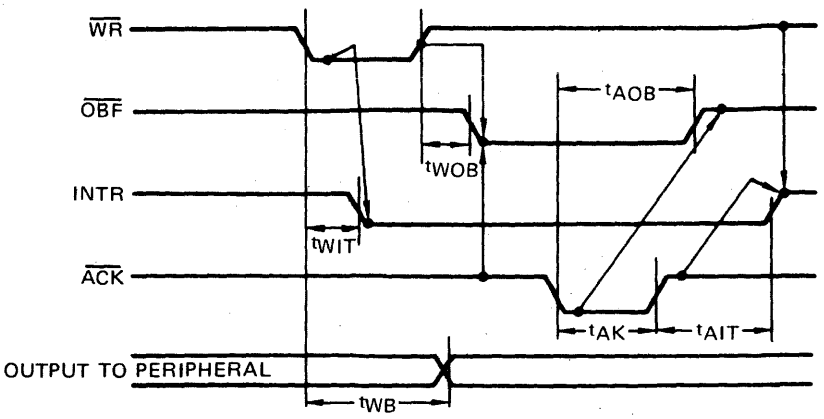


BASIC OUTPUT

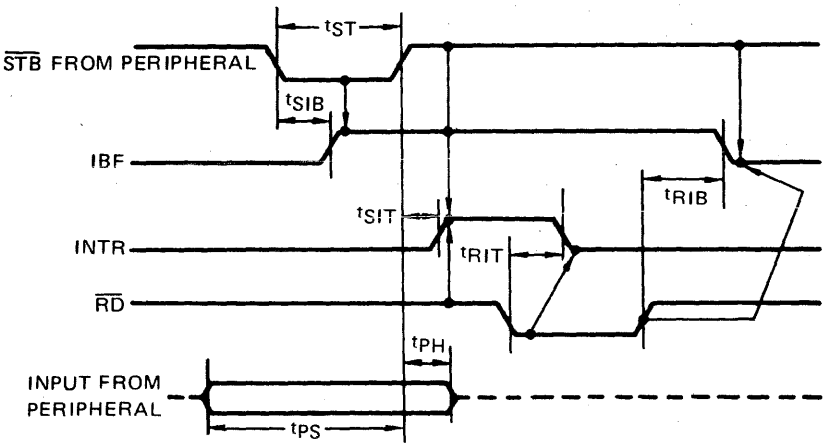
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TIMING WAVEFORMS (CONT.)

MODE 1

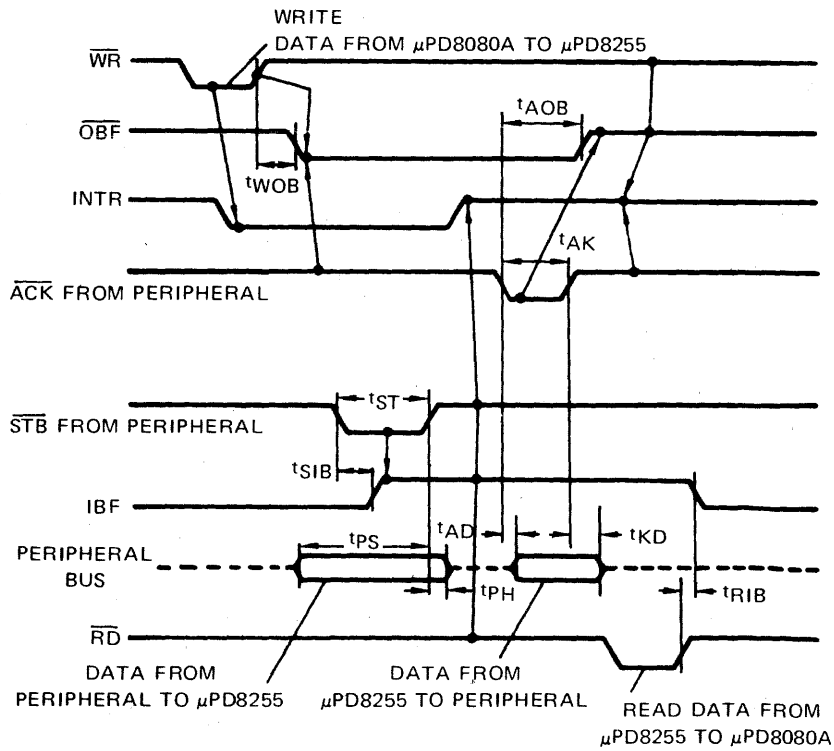


STROBED OUTPUT



STROBED INPUT

MODE 2



BI-DIRECTIONAL

Note: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
($INTR = IBF \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR}$)

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NEC Microcomputers

The μPD8255 can be operated in modes (0, 1 or 2) which are selected by appropriate control words and are detailed below.

MODES

MODE 0

- MODE 0 provides for basic Input and Output operations through each of the ports A, B, and C. Output data is latched and input data follows the peripheral. No "handshaking" strobes are needed.
- 16 different configurations in MODE 0
- Two 8-bit ports and two 4-bit ports
- Inputs are not latched
- Outputs are latched

MODE 1

- MODE 1 provides for Strobed Input and Output operations with data transferred through Port A or B and handshaking through Port C.
- Two I/O Groups (I and II)
- Both groups contain an 8-bit data port and a 4-bit control/data port
- Both 8-bit data ports can be either Latched Input or Latched Output

MODE 2

- MODE 2 provides for Strobed bidirectional operation using PA_{0-7} as the bidirectional latched data bus. PC_{3-7} is used for interrupts and "handshaking" bus flow controls similar to Mode 1. Note that PB_{0-7} and PC_{0-2} may be defined as Mode 0 or 1, input or output in conjunction with Port A in Mode 2.
- An 8-bit latched bidirectional bus port (PA_{0-7}) and a 5-bit control port (PC_{3-7})
- Both inputs and outputs are latched
- An additional 8-bit input or output port with a 3-bit control port

BASIC OPERATION

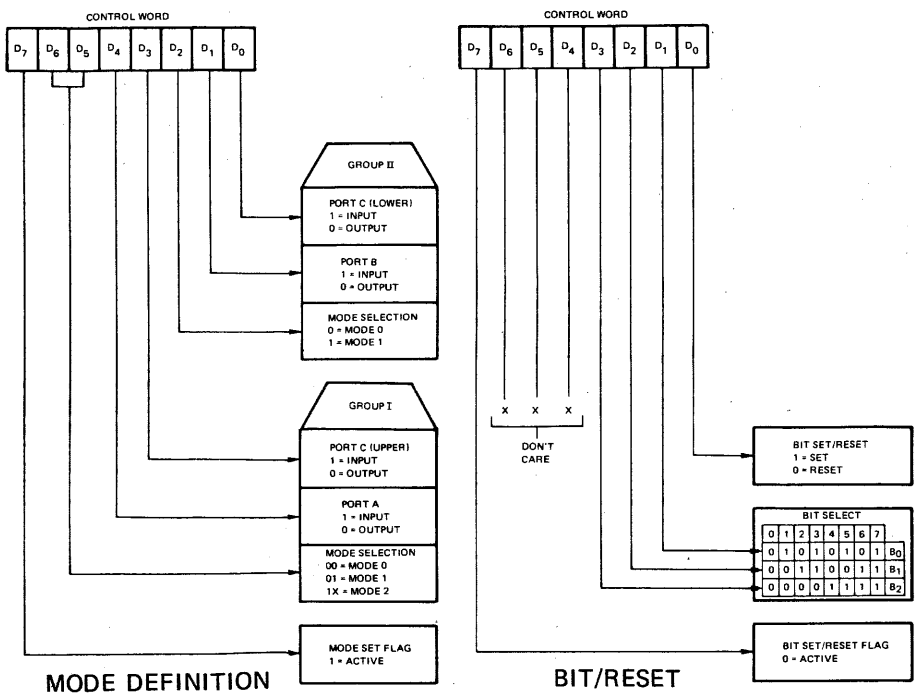
INPUT OPERATION (READ)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS

OUTPUT OPERATION (WRITE)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL

DISABLE FUNCTION					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
X	X	X	X	1	DATA BUS → HIGH Z STATE
X	X	1	1	0	DATA BUS → HIGH Z STATE

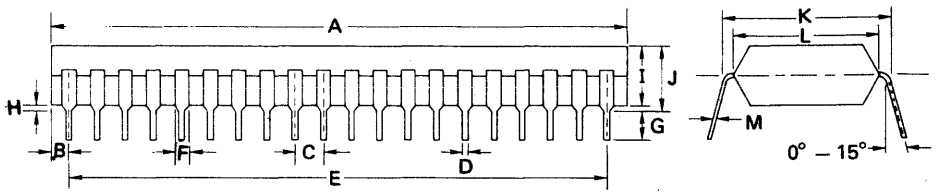
NOTES: ① X means "DO NOT CARE."
② All conditions not listed are illegal and should be avoided.

FORMATS



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PACKAGE OUTLINE
μPB8255C



μPD8255C
(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.5 MIN	0.06 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

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PROGRAMMABLE DMA CONTROLLER

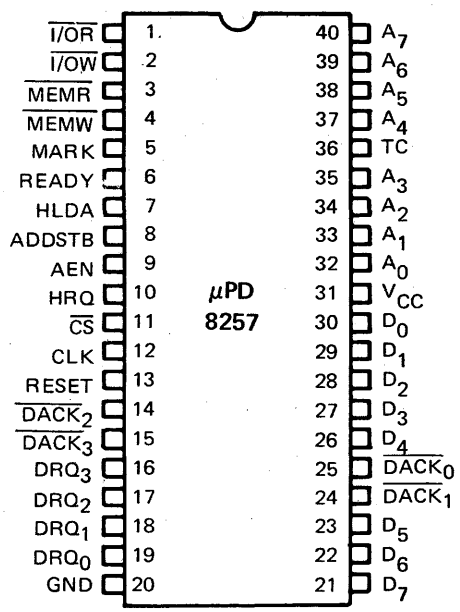
DESCRIPTION

The μPD8257 is a programmable four-channel Direct Memory Access (DMA) controller. It is designed to simplify high speed transfers between peripheral devices and memories. Upon a peripheral request, the 8257 generates a sequential memory address, thus allowing the peripheral to read or write data directly to or from memory. Peripheral requests are prioritized within the 8257 so that the system bus may be acquired by the generation of a single HOLD command to the 8080. DMA cycle counts are maintained for each of the four channels, and a control signal notifies the peripheral when the preprogrammed member of DMA cycles has occurred. Output control signals are also provided which allow simplified sectored data transfers and expansion to other 8257 devices for systems requiring more than four DMA channels.

FEATURES

- Four Channel DMA Controller
- Priority DMA Request Logic
- Channel Inhibit Logic
- Terminal Count and Modulo 128 Outputs
- Automatic Load Mode
- Single TTL Clock
- Single +5V Supply
- Expandable
- 40 Pin Plastic Dual-In-Line Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus
A_7-A_0	Address Bus
$\overline{I/OR}$	I/O Read
$\overline{I/OW}$	I/O Write
$\overline{MEMR}$	Memory Read
$\overline{MEMW}$	Memory Write
CLK	Clock Input
RESET	Reset Input
READY	Ready
HRQ	Hold Request (to 8080A)
HLDA	Hold Acknowledge (from 8080A)
AEN	Address Enable
ADSTB	Address Strobe
TC	Terminal Count
MARK	Modulo 128 Mark
DRQ_3-DRQ_0	DMA Request Input
$\overline{DACK_3}$-$\overline{DACK_0}$	DMA Acknowledge Out
$\overline{CS}$	Chip Select
V_{CC}	+5 Volts
GND	Ground

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FUNCTIONAL DESCRIPTION

The 8257 is a programmable, Direct Memory Access (DMA) device and when used with an 8212 I/O port device, it provides a complete four-channel DMA controller for use in 8080 based systems. Once initialized by an 8080 CPU, the 8257 will block transfer up to 16,364 bytes of data between memory and a peripheral device without any attention from the CPU, and it will do this on all 4-DMA channels. After receiving a DMA transfer request from a peripheral, the following sequence of events occur within the 8257.

- It acquires control of the system bus (placing 8080 in hold mode).
- Resolves priority conflicts if multiple DMA requests are made.
- A 16 bit memory address word is generated with the aid of an 8212 in the following manner:

  The 8257 outputs the least significant eight bits (A_0-A_7) which go directly onto the address bus.

  The 8257 outputs the most significant eight bits (A_8-A_{15}) onto the data bus where they are latched into an 8212 and then sent to the high order bits on the address bus.
- The appropriate memory and I/O read/write control signals are generated allowing the peripheral to receive or deposit a data byte directly from or to the appropriate memory location.

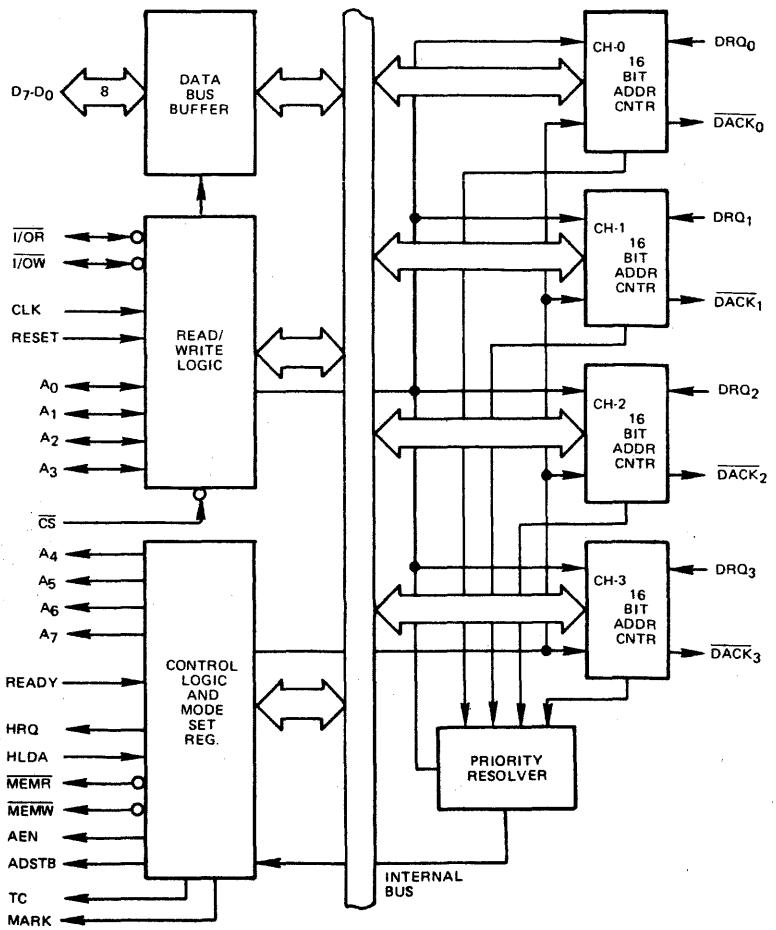
Block transfer of data (e.g., a sector of data on a floppy disk) either to or from a peripheral may be accomplished as long as the peripheral maintains its DMA Request (DRQ_n). The 8257 retains control of the system bus as long as DRQ_n remains high or until the Terminal Count (TC) is reached. When the Terminal Count occurs, TC goes high, informing the CPU that the operation is complete.

There are three different modes of operation:

- DMA read; which causes data to be transferred from memory to a peripheral;
- DMA write; which causes data to be transferred from a peripheral to memory; and ,
- DMA verify; which does not actually involve the transfer of data.

The DMA read and write modes are the normal operating conditions for the 8257. The DMA verify mode responds in the same manner as read/write except no memory or I/O read/write control signals are generated, thus preventing the transfer of data. The peripheral gains control of the system bus and obtains DMA Acknowledgements for its requests, thus allowing it to access each byte of a data block for check purposes or accumulation of a CRC (Cyclic Redundancy Code) checkword. In some applications it is necessary for a block of DMA read or write cycles to be followed by a block of DMA verify cycles to allow the peripheral to verify its newly acquired data.

BLOCK DIAGRAM



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AC CHARACTERISTICS PERIPHERAL (SLAVE) MODE

BUS PARAMETERS

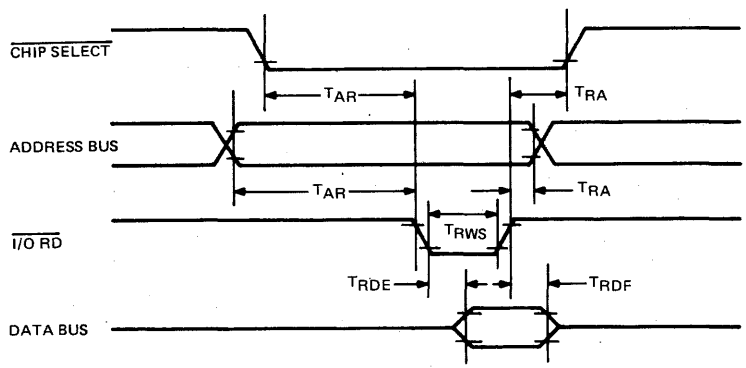
T_a = 0°C to 70°C; V_{CC} = 5V ± 5%; GND = 0V ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
READ						
Adr or $\overline{CS}$↓ Setup to $\overline{Rd}$↓	T_{AR}	50			ns	
Adr or $\overline{CS}$↑ Hold from $\overline{Rd}$↑	T_{RA}	0			ns	
Data Access from $\overline{Rd}$↓	T_{RDE}	0		300	ns	C_L = 100pF
DB→Float Delay from $\overline{Rd}$↑	T_{RDF}			150	ns	C_L = 100pF
		20			ns	C_L = 15pF
$\overline{Rd}$ Width	T_{RW}	300			ns	
WRITE						
$\overline{CS}$↓ Setup to $\overline{Wr}$↓	T_{CW}	300			ns	
$\overline{CS}$↑ Hold from $\overline{Wr}$↑	T_{WC}	20			ns	
Adr Setup to $\overline{Wr}$↓	T_{AW}	20			ns	
Adr Hold from $\overline{Wr}$↑	T_{WA}	20			ns	
Data Setup to $\overline{Wr}$↓	T_{DW}	200			ns	
Data Hold from $\overline{Wr}$↑	T_{WD}	35			ns	
Wr Width	T_{WWS}	200			ns	
OTHER TIMING						
Reset Pulse Width	T_{RSTW}	300			ns	
Power Supply↑(V_{CC}) Setup to Reset↓	T_{RSTD}	500			μs	
Signal Rise Time	T_r			20	ns	
Signal Fall Time	T_f			20	ns	
Reset to First $\overline{IOWR}$	T_{RSTS}	2			t_{CY}	

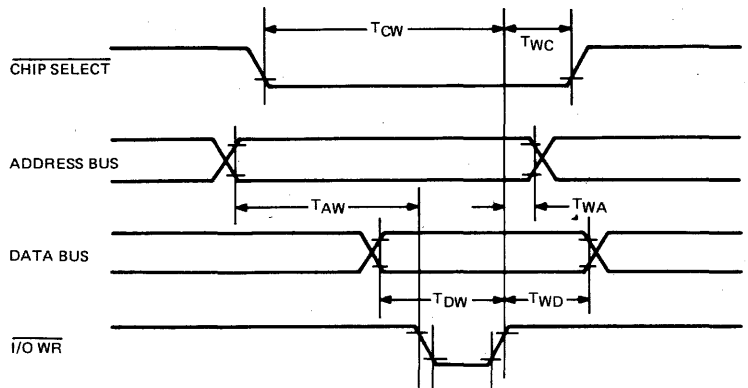
Note: ① All timing measurements are made at the following reference voltages unless specified otherwise: Input "1" at 2.0V, "0" at 0.8V, Output "1" at 2.0V, "0" at 0.8V.

TIMING WAVEFORMS PERIPHERAL (SLAVE) MODE

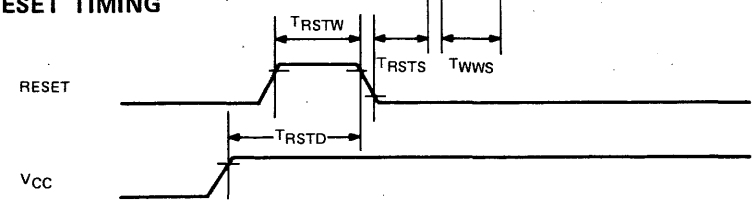
READ TIMING



WRITE TIMING



RESET TIMING



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AC CHARACTERISTICS DMA (MASTER) MODE

T_a = 0°C to 70°C; V_{CC} = +5V ±5%; GND = 0V

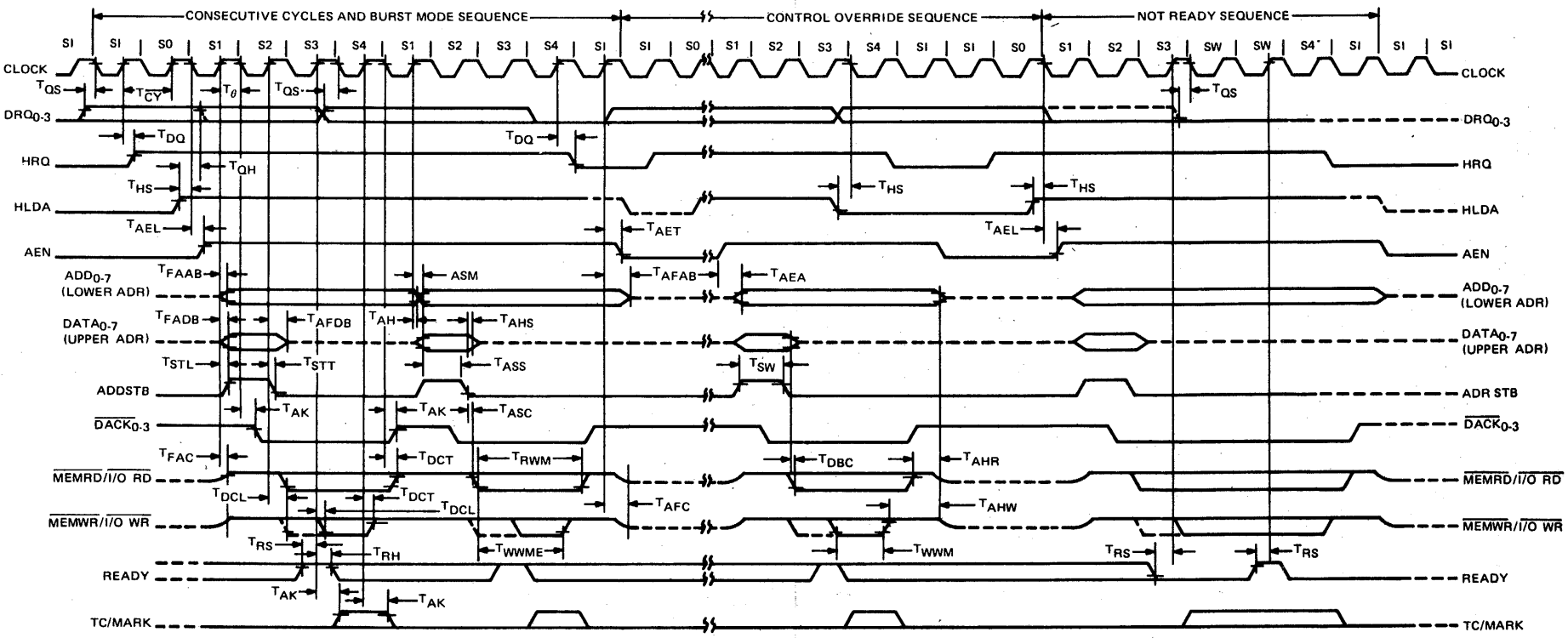
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Cycle Time (Period)	T_{CY}	0.330		4	μs	
Clock Active (High)	T_θ	150		.8T_{CY}	ns	
DRQ↑ Setup to θ↓ (SI, S4)	T_{QS}	120				
DRQ↓ Hold from HLDA↑	T_{QH}	0				④
HRQ↑ or ↓Delay from θ↑ (SI, S4) (measured at 2.0V)	T_{DQ}			160	ns	①
HRQ↑ or ↓Delay from θ↑ (SI, S4) (measured at 3.3V)	T_{DQ1}			250	ns	③
HLDA↑ or ↓Setup to θ↓ (SI, S4)	T_{HS}	100			ns	
AEN↑ Delay from θ↓ (S1)	T_{AEL}			300	ns	①
AEN↓ Delay from θ↑ (SI)	T_{AET}			200	ns	①
Adr (AB) (Active) Delay from AEN↑ (S1)	T_{AEA}	20			ns	④
Adr (AB) (Active) Delay from θ↑ (S1)	T_{FAAB}			250	ns	②
Adr (AB) (Float) Delay from θ↑ (SI)	T_{AFAB}			150	ns	②
Adr (AB) (Stable) Delay from θ↑ (S1)	T_{ASM}			250	ns	②
Adr (AB) (Stable) Hold from θ↑ (S1)	T_{AH}	T_{ASM}−50				②
Adr (AB) (Valid) Hold from $\overline{Rd}$↑ (S1,SI)	T_{AHR}	60			ns	④
Adr (AB) (Valid) Hold from $\overline{Wr}$↑ (S1, SI)	T_{AHW}	300			ns	④
Adr (DB) (Active) Delay from θ↑ (S1)	T_{FADB}			300	ns	②
Adr (DB) (Float) Delay from θ↑ (S2)	T_{AFDB}	T_{STT}+20		250	ns	②
Adr (DB) Setup to Adr Stb↓ (S1-S2)	T_{ASS}	100			ns	④
Adr (DB) (Valid) Hold from Adr Stb↓ (S2)	T_{AHS}	50			ns	④
Adr Stb↑ Delay from θ↑ (S1)	T_{STL}			200	ns	①
Adr Stb↓ Delay from θ↑ (S2)	T_{STT}			140	ns	①
Adr Stb Width (S1-S2)	T_{SW}	T_{CY}−100			ns	④
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from Adr Stb↓ (S2)	T_{ASC}	70			ns	④
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from Adr (DB) (Float) (S2)	T_{DBC}	20			ns	④
DACK↑ or ↓Delay from θ↓ (S2, S1) and TC/Mark↑ Delay from θ↑ (S3) and TC/Mark↓ Delay from θ↑ (S4)	T_{AK}			250	ns	①⑤
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from θ↑ (S2) and $\overline{Wr}$↓ Delay from θ↑ (S3)	T_{DCL}			200	ns	②⑥
$\overline{Rd}$↑ Delay from θ↓ (S1, SI) and $\overline{Wr}$↑ Delay from θ↑ (S4)	T_{DCT}			200	ns	②⑦
$\overline{Rd}$ or $\overline{Wr}$ (Active) from θ↑ (S1)	T_{FAC}			300	ns	②
$\overline{Rd}$ or $\overline{Wr}$ (Float) from θ↑ (SI)	T_{AFC}			150	ns	②
$\overline{Rd}$ Width (S2-S1 or SI)	T_{RWM}	$2T_{CY}$ + T_θ−50			ns	④
$\overline{Wr}$ Width (S3-S4)	T_{WWM}	T_{CY}−50			ns	④
$\overline{Wr}$ (Ext) Width (S2-S4)	T_{WWME}	$2T_{CY}$−50			ns	④
READY Set Up Time to θ↑ (S3, Sw)	T_{RS}	30			ns	
READY Hold Time from θ↑ (S3, Sw)	T_{RH}	20			ns	

Notes:
① Load = 1 TTL
② Load = 1 TTL + 50pF
③ Load = 1 TTL + (R_L = 3.3K), V_{OH} = 3.3V
④ Tracking Specification
⑤ $\Delta T_{AK} < 50$ ns
⑥ $\Delta T_{DCL} < 50$ ns
⑦ $\Delta T_{DCT} < 50$ ns

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TIMING WAVEFORMS
DMA (MASTER) MODE



DMA OPERATION

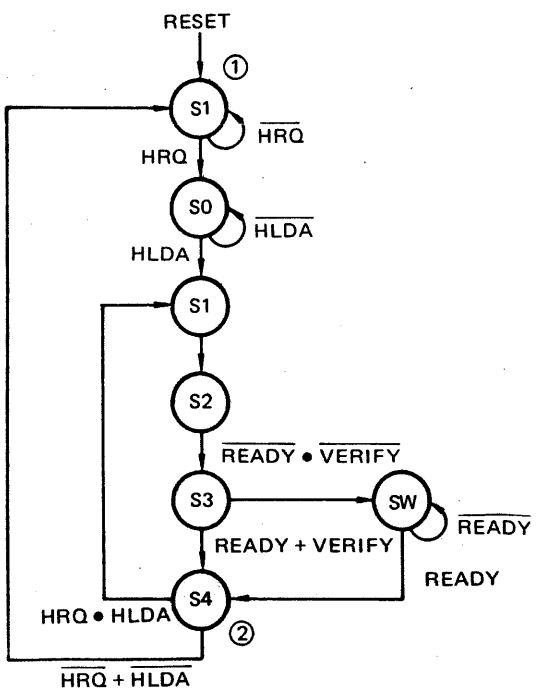
Internally the 8257 contains six different states (S0, S1, S2, S3, S4 and SW), the duration of each state is determined by the input clock. In the idle state, (S1), no DMA operation is being executed. A DMA cycle is started upon receipt of one or more DMA Requests (DRQ_n), then the 8257 enters the S0 state. During state S0 a Hold Request (HRQ) is sent to the 8080 and the 8257 waits in S0 until the 8080 issues a Hold Acknowledge (HLDA) back. During S0, DMA Requests are sampled and DMA priority is resolved (based upon either the fixed or priority scheme). After receipt of HLDA, the DMA Acknowledge line ($\overline{DACK}_n$) with the highest priority is driven low selecting that particular peripheral for the DMA cycle. The DMA Request line (DRQ_n) must remain high until either a DMA Acknowledge ($\overline{DACK}_n$) or both $\overline{DACK}_n$ and TC (Terminal Count) occur, indicating the end of a block or sector transfer (burst mode).

The DMA cycle consists of four internal states; S1, S2, S3 and S4. If the access time of the memory or I/O device is not fast enough to return a Ready command to the 8257 after it reaches state S3, then a Wait state is initiated (SW). One or more than one Wait state occurs until a Ready signal is received, and the 8257 is allowed to go into state S4. Either the extended write option or the DMA Verify mode may eliminate any Wait state.

If the 8257 should lose control of the system bus (i.e., HLDA goes low) then the current DMA cycle is completed, the device goes into the S1 state, and no more DMA cycles occur until the bus is reacquired. Ready setup time (t_{RS}), write setup time (t_{DW}), read data access time (t_{RD}) and HLDA setup time (t_{QS}) should all be carefully observed during the handshaking mode between the 8257 and the 8080.

During DMA write cycles, the I/O Read ($\overline{I/O\ R}$) output is generated at the beginning of state S2 and the Memory Write ($\overline{MEMW}$) output is generated at the beginning of S3. During DMA read cycles, the Memory Read ($\overline{MEMR}$) output is generated at the beginning of state S2 and the I/O Write ($\overline{I/O\ W}$) goes low at the beginning of state S3. No Read or Write control signals are generated during DMA verify cycles.

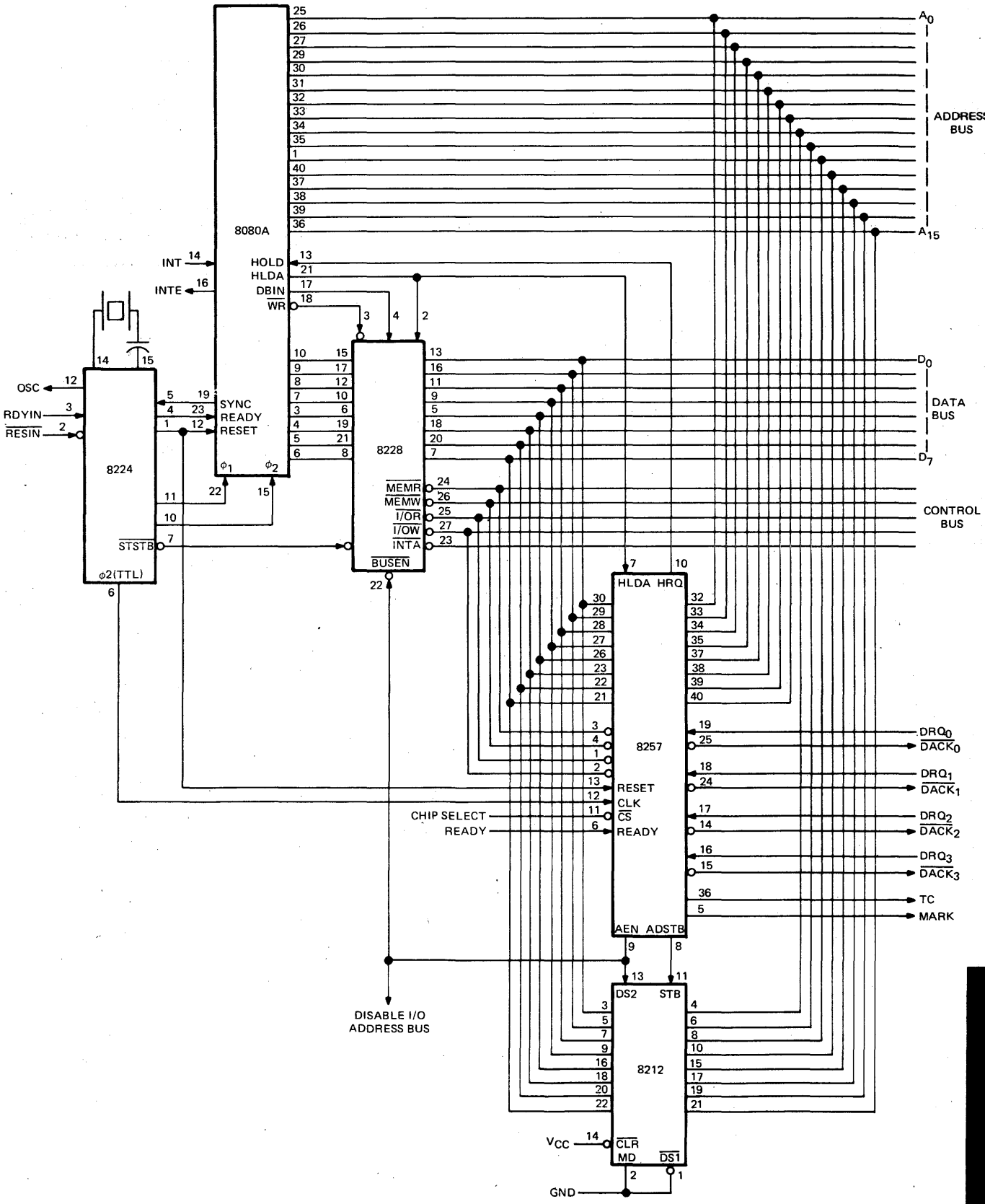
DMA OPERATION STATE DIAGRAM



Notes: ① HRQ is set if DRQ_n is active.
② HRQ is reset if DRQ_n is not active.

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TYPICAL 8257
SYSTEM INTERFACE SCHEMATIC



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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−0.5 to +7 Volts ①
Power Dissipation	1 Watt

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%; GND = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Low Voltage	V_{IL}	−0.5		0.8	Volts	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	Volts	
Output Low Voltage	V_{OL}			0.45	Volts	I_{OL} = 1.6 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	Volts	I_{OH} = −150 μA for AB, DB and AEN I_{OH} = −80 μA for others
HRQ Output High Voltage	V_{HH}	3.3		V_{CC}	Volts	I_{OH} = −80 μA
V_{CC} Current Drain	I_{CC}			120	mA	
Input Leakage	I_{IL}			10	μA	V_{IN} = V_{CC}
Output Leakage During Float	I_{OFL}			10	μA	V_{OUT} ①

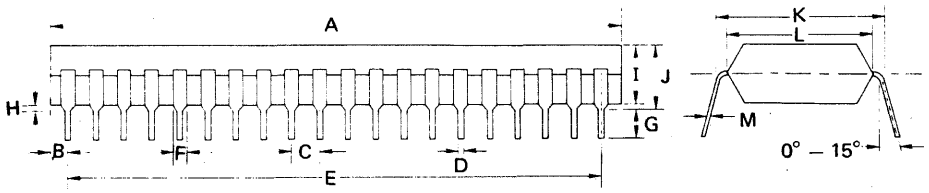
Note: ① $V_{CC} > V_{OUT} >$ GND + 0.45V

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

PACKAGE OUTLINE



ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

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PROGRAMMABLE INTERVAL TIMER

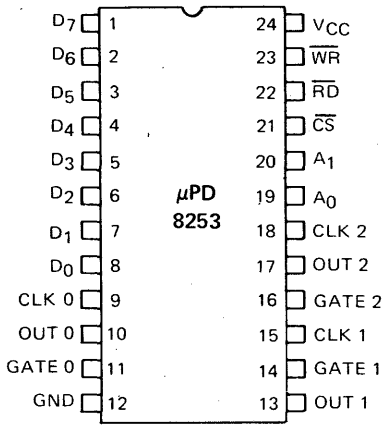
DESCRIPTION

The NEC μPD8253 is a fully programmable, multi-mode, 16-bit counter/timer. It is designed as a general purpose device capable of interfacing directly to an 8080 microprocessor system as an array of I/O ports. The μPD8253 can generate accurate time delays under the control of system software. It contains three independent 16-bit counters which can be clocked at rates from DC to 2 MHz.

FEATURES

- Three Independent 16-Bit Counters
- DC to 2 MHz
- Programmable Counter Modes
- Count Binary or BCD
- Single +5V Supply
- 24 Pin Dual-In-Line Package
- +5V NMOS Technology

PIN CONFIGURATION



PROGRAMMABLE PERIPHERAL INTERFACE

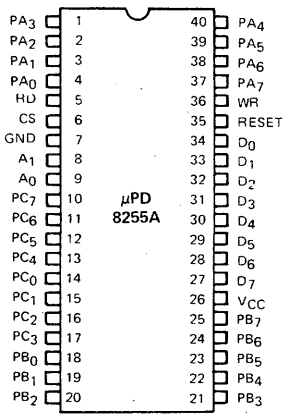
DESCRIPTION

The NEC μPD8255A is a programmable peripheral interface device having 24 programmable I/O pins. It is directly compatible with the 8080 microprocessor system, and normally no extra logic is required to interface to the 8080A. The system software can individually program each of the 24 I/O pins into two groups of twelve for the three major modes of operation.

FEATURES

- Completely TTL Compatible
- Fully Compatible with NEC μP Families
- Direct Bit Set/Reset Capabilities Easing Control Application Interface
- 40 Pin Dual-In-Line Package
- Reduces System Package Count
- Capabilities to Drive Darlington Pairs

PIN CONFIGURATION



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PROGRAMMABLE INTERRUPT CONTROLLER

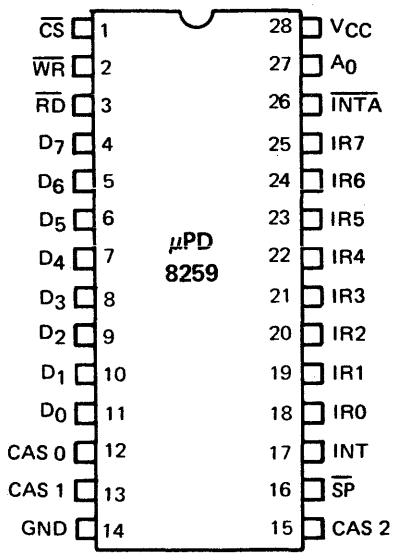
DESCRIPTION

The NEC μPD8259 is a programmable interrupt controller which can handle up to eight vectored priority interrupts in an 8080 microprocessor system. It can be cascaded to extend the vectored priority interrupt capability to 64 without extra circuitry. It is system software programmable with a selection of priority algorithms available which can be dynamically changed at any time.

FEATURES

- Eight Level Priority Controller
- Expandable to 64 Levels
- Programmable Interrupt Algorithms
- Individual Request Mask Capability
- Single +5V Supply
- Static Circuitry (No Clock)

PIN CONFIGURATION



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NEC microcomputers, inc.

PRELIMINARY

μPD8085

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

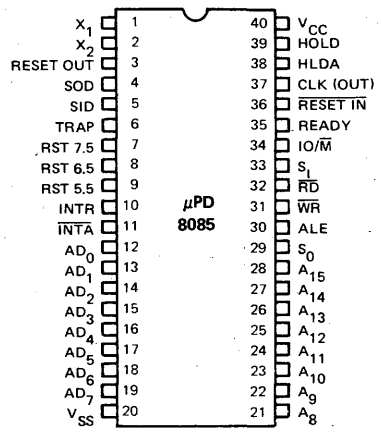
DESCRIPTION

The NEC μPD8085 is the next generation single chip 8-bit microprocessor. It provides full software compatibility with the 8080A but with an improved, higher system speed. The μPD8085's higher level of system integration allows the functions of the μPD8224 (clock generator) and the μPD8228 (system controller) to be incorporated into its design. Together with the μPD8155/8156 (2K RAM) and the μPD8355/8755 (16K ROM/EPROM) a minimum system can be configured using just three IC's. The DATA BUS of the μPD8085 multiplexes the 8-bit address bus and the 8-bit data bus to achieve greater system throughput. The μPD8155/8156 and the μPD8355/8755 memory products have on-chip address latches which provide direct interfacing to the μPD8085.

FEATURES

- Single +5V Supply
- 1.3 μs Instruction Cycle
- On-Chip System Controller
- 100% Software Compatibility with the μCOM-8 Family
- On-Chip Clock Generator (with External Crystal or RC Network)
- Four Vectored Interrupts (One is Non-Maskable)
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Direct Addressing Capability to 64K Bytes of Memory

PIN CONFIGURATION



NEC microcomputers, inc.

PRELIMINARY

μPD8155

μPD8156

2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

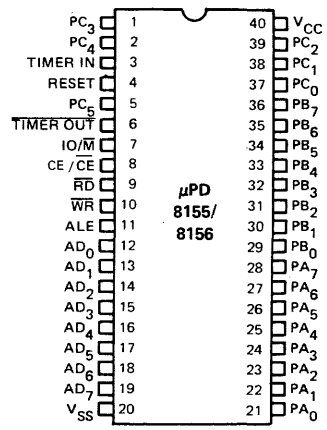
DESCRIPTION

The NEC μPD8155 and μPD8156 2048-bit Static Random Access Memories are organized as 256 x 8 and are fully compatible with the μPD8085 microprocessor system. Three I/O pins allow programmable status and handshaking capabilities with the processor. The on-chip 14 bit counter timer is fully programmable by the system software.

FEATURES

- 256 Words x 8 Bits Organization
- 400 ns Access Time (No Wait States Required)
- Multiplexed Address and Data Bus
- Programmable 14 Bit Binary Counter/Timer
- 1 Programmable 6 Bit I/O Port
- 2 Programmable 8 Bit I/O Ports

PIN CONFIGURATION



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μPD8355
μPD8755

16,384 BIT ROM WITH I/O / 16,384 BIT EPROM WITH I/O

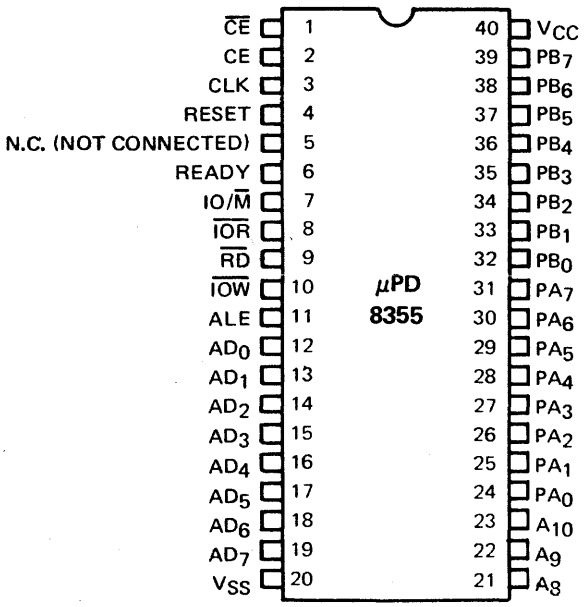
DESCRIPTION

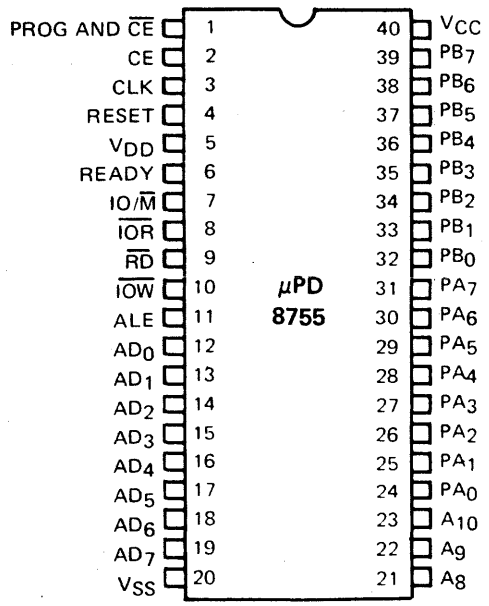
The NEC μPD8355 is a 16,384 bit Read Only Memory with I/O organized as 2048 words x 8 bits. The μPD8755 is a 16,384 bit erasable and electrically programmable Read Only Memory. Access time for both devices is 400 ns so no wait state are required in the processor. There are two separately programmable, 8 bit wide I/O ports for interfacing to the processor.

FEATURES

- 2048 Words x 8 Bits
- Single +5V Power Supply
- Internal Address Latch
- 2 General Purpose 8 Bit I/O Ports
- Multiplexed Address and Data Bus
- Direct Compatibility with μPD8085 and μPD8048

PIN CONFIGURATIONS





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PRELIMINARY

μPD8048
μPD8748
μPD8035

SINGLE COMPONENT 8-BIT MICROCOMPUTER

DESCRIPTION

The NEC μPD8048/8748/8035 are complete, single-chip, NMOS microcomputers requiring only a single +5V power supply. There are three interchangeable microcomputers in this family to allow the user maximum freedom in systems implementation. In addition, if system expansion is necessary, the μPD8048/8748/8035 are fully compatible with NEC's family of 8080A peripherals including memory devices.

The on-chip features of the μPD8048 include 1K x 8 bits of Read Only Memory for firm program storage, 64 x 8 bits of Random Access Memory which can be used as a scratch pad, 27 I/O lines, an 8-bit counter/timer and clock, oscillator and clock driver circuitry requiring only an off-the-chip crystal.

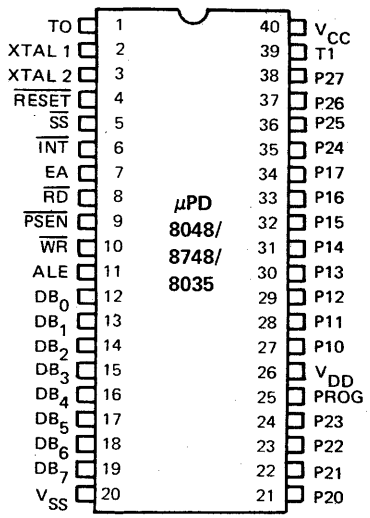
The μPD8035 is functionally and pin-for-pin compatible with the μPD8048 but without the 1K x 8 bit ROM, which is intended for use with external memory.

The μPD8748 is also fully compatible with both the μPD8048 and μPD8035. In this device the 1K x 8 bit ROM has been replaced with a 1K x 8 bit erasable, electrically programmable ROM to provide the user with the flexibility of changing the program memory contents.

FEATURES

- 8 Bit Parallel Processor, ROM, RAM, I/O in Single Package
- Interchangeable ROM and EPROM Versions
- Single +5V Supply
- 2.5 μsec and 5.0 μsec Cycle Versions
  All Instructions 1 or 2 Cycles
- Over 90 Instructions: 70% Single Byte
  None Over Two Bytes
- 1K x 8 ROM/EPROM, 64 x 8 RAM,
  27 I/O Lines
- Programmable Counter/Timer
- Easily Expandable Memory and I/O
- Single Level Interrupt
- Compatible with μCOM-8 Series Peripherals

PIN CONFIGURATION



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μPB2901 4-BIT MICROPROCESSOR SLICE

DESCRIPTION

The NEC μPB2901 is a four-bit microprocessor slice, with an expandable bus structure extending interface capabilities to all other members of the μPB2900 series family. The internal functions of the μPB2901 include an eight-function ALU, sixteen addressable registers using separate read and read/write address busses, an auxiliary register and shifting logic.

Other members of the μPB2900 series family are:

μPB2902 . . . . . 4-Bit Carry Look-Ahead
μPB2909 . . . . . 4-Bit Microprogram Sequencer
μPB2911 . . . . . 4-Bit Microprogram Sequencer
μPB2905 . . . . . OC Bus Transceiver with Tri-State Receiver
μPB2906 . . . . . OC Bus Transceiver with Parity
μPB2907 . . . . . OC Bus Transceiver with Parity and Tri-State Receiver
μPB2915 . . . . . Tri-State Bus Transceiver with Tri-State Receiver
μPB2916 . . . . . Tri-State Transceiver with Parity
μPB2917 . . . . . Tri-State Bus Receiver with Parity and Tri-State Receiver
μPB2918 . . . . . 4-Bit D-Register with Standard and Tri-State Output

FEATURES

- 4-Bit CPU Slice
- Standard 40 Pin Dual-In-Line Package
- Register-to-Register, Read/Modify/Write Time of 150 ns (Worst Case)
- 8 Function ALU
- 16 Working Registers
- Auxiliary Register
- Shifting Logic

SINGLE CHIP 8-BIT MICROPROCESSOR

DESCRIPTION

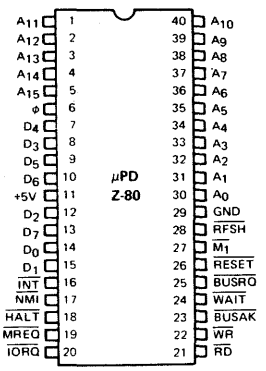
The NEC μPDZ-80 is a third generation, N-Channel microprocessor providing many advancements over second generation microprocessors. The μPDZ-80 processor offers a savings in systems throughput and reduced memory requirements through its expanded 158 software instruction set, while maintaining software compatibility with the 8080A. The expanded instruction set allows for a higher level of system operation by providing for memory-to-memory block transfers, bit manipulation and sampling in any register or memory location, enhanced 16-bit and BCD arithmetic, new I/O features such as I/O block transfers and expanded addressing modes (indexed and relative).

The μPDZ-80 provides all the control and refresh control signals for interfacing with most 4K static or dynamic memories. Only an external address decoder is needed for the static memories' chip selects. In addition, seventeen registers and 208 bits of programmer usable Read/Write memory on-chip all contribute to the power and versatility of this device.

FEATURES

- 158 Instructions (Including all 78 Instructions of the 8080A)
- 17 Internal Register
- Three Modes of Fast Interrupt Response and a Non-Maskable Interrupt
- Direct Interface with Standard Speed Dynamic or Static Memories
- 1.6 μs Instruction Execution Time
- Single +5V Supply
- Single-Phase TTL Clock
- TTL Compatible Tri-State Address and Data Busses

PIN CONFIGURATION



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DESCRIPTION

The 4-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPUs, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the 2901-1 will allow efficient emulation of almost any digital computing machine.

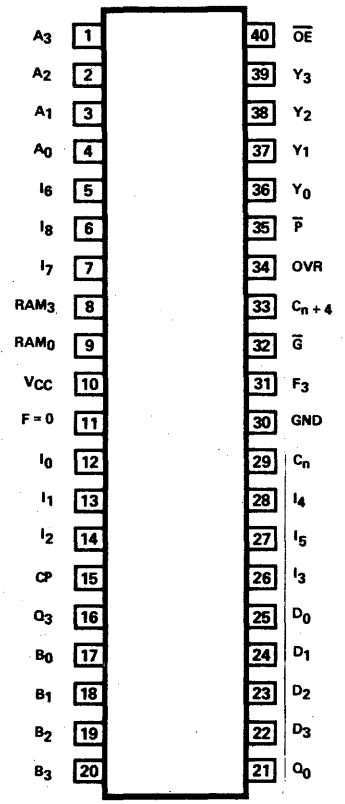
The device, as shown in the block diagram below, consists of a 16-word by 4-bit 2-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The 9-bit microinstruction word is organized into 3 groups of 3 bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip.

FEATURES

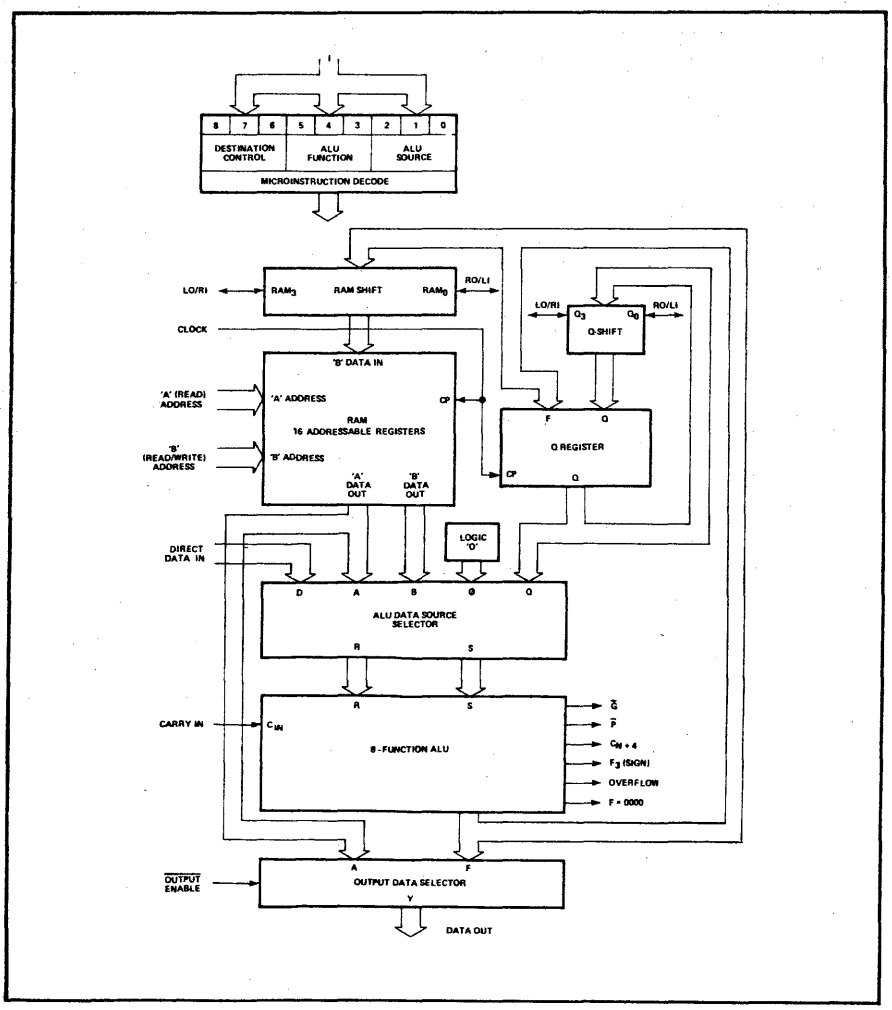
- **80ns cycle time**
- **2-address architecture**
  Independent simultaneous access to 2 working registers saves machine cycles
- **8-function ALU**
  Performs addition, 2 subtraction operations, and 5 logic functions on 2 source operands
- **Flexible data source selection**
  ALU data is selected from 5 source ports for a total of 203 source operand pairs for every ALU function
- **Left/right shift independent of ALU**
  Add and shift operations take only 1 cycle
- **4 status flags**
  Carry, overflow, zero, and negative
- **Expandable**
  Connect any number of 2901-1's together for longer word lengths
- **Microprogrammable**
  3 groups of 3 bits each for source operand, ALU function, and destination control

PIN CONFIGURATION

I PACKAGE



BLOCK DIAGRAM



Signetics

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PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-4	A_0-A_3	**A Address** The 4 address inputs to the register stack used to select 1 register whose contents are displayed through the A port. A_0 is the LSB.	Active high
17-20	B_0-B_3	**B Address** The 4 address inputs to the register stack used to select 1 register whose contents are displayed through the B port and into which new data can be written when the clock goes LOW. B_0 is the LSB.	Active high
12-14, 26-28, 5-7	I_0-I_8	**Instruction Control** The 9 instruction control lines to the 2901-1 used to determined what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q register or the register stack (I_{678}).	Active high
8 16	RAM_3 Q_3	**Shift Line** A shift line at the MSB of the Q register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the 2901-1. When the destination code on I_{678} indicates a left (up) shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are off (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a right (down) shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).	Three-state Active high
9 21	RAM_0 Q_0	**Shift Line** Shift lines similar to Q_3 and RAM_3, at the LSB of the Q register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device and are used to transfer data between devices for left and right shifts of the Q register and ALU data.	Active high
22-25	D_0-D_3	**Direct Data Inputs** A 4-bit data field which may be selected as one of the ALU data sources for entering data into the 2901-1. D_0 is the LSB.	Active high
36-39	Y_0-Y_3	**Data Out** The 4 data outputs of the 2901-1. These are three-state output lines. When enabled, they display either the 4 outputs of the ALU or the data on the A port of the register stack, as determined by the destination code I_{678}. Y_0 is the LSB.	Three-state Active high
40	$\overline{OE}$	**Output Enable** When $\overline{OE}$ is High, the Y outputs are disabled; when $\overline{OE}$ is Low, the Y outputs are active (high or low).	Active low
32, 35	$\overline{G}$, $\overline{P}$	**Carry Generate, Propagate** The carry generate and propagate outputs of the 2901-1. These signals are used with the N74S182 for carry-lookahead. See Table 7 for the logic equations.	Active low
34	OVR	**Overflow** This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit. See Table 7 for logic equation.	Active high
11	F = 0	**F = 0** This is an open collector output which goes High (off) if the data on the 4 ALU outputs F_{0-3} are all low. In positive logic, it indicates the result of an ALU operation is zero.	Active high
29	C_n	**Carry In**	Active high
33	C_{n+4}	**Carry Out** (See Table 7 for logic equations.)	Active high
15	CP	**Clock** The Q register and register stack outputs change on the clock Low-to-High transition. The clock Low time is internally the write enable to the 16X4 RAM which comprises the "master" latches of the register stack. While the clock is Low, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.	Active high

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SYSTEM DESCRIPTION

A detailed block diagram of the bipolar microprogrammable microprocessor structure is shown in Figure 1. The circuit is a 4-bit slice cascadable to any number of bits. Therefore, all data paths within the circuit are 4 bits wide. The two key elements in the Figure 1 block diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 16 words of the RAM as defined by the B address field input can be simultaneously read from the B port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A port and B port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This 3-input multiplexer scheme allows the data to be shifted up (left) 1 bit position, shifted down (right) 1 bit position, or not shifted in either direction.

The RAM A port data outputs and RAM B port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is low. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform 3 binary arithmetic and 5 logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 1, the ALU R-input multiplexer has the RAM A port and the direct data inputs (D) connected as inputs. Likewise, the ALU S input multiplexer has the RAM A port, the RAM B port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These 5 inputs, when taken 2 at a time, result in 10 possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent that AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only 7 completely non-redundant source operand pairs for the ALU. The 2901-1 microprocessor implements 8 of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the 8 source operand combinations are as shown in Table 1. Also shown is the octal code for each selection.

DETAILED 2901-1 BLOCK DIAGRAM

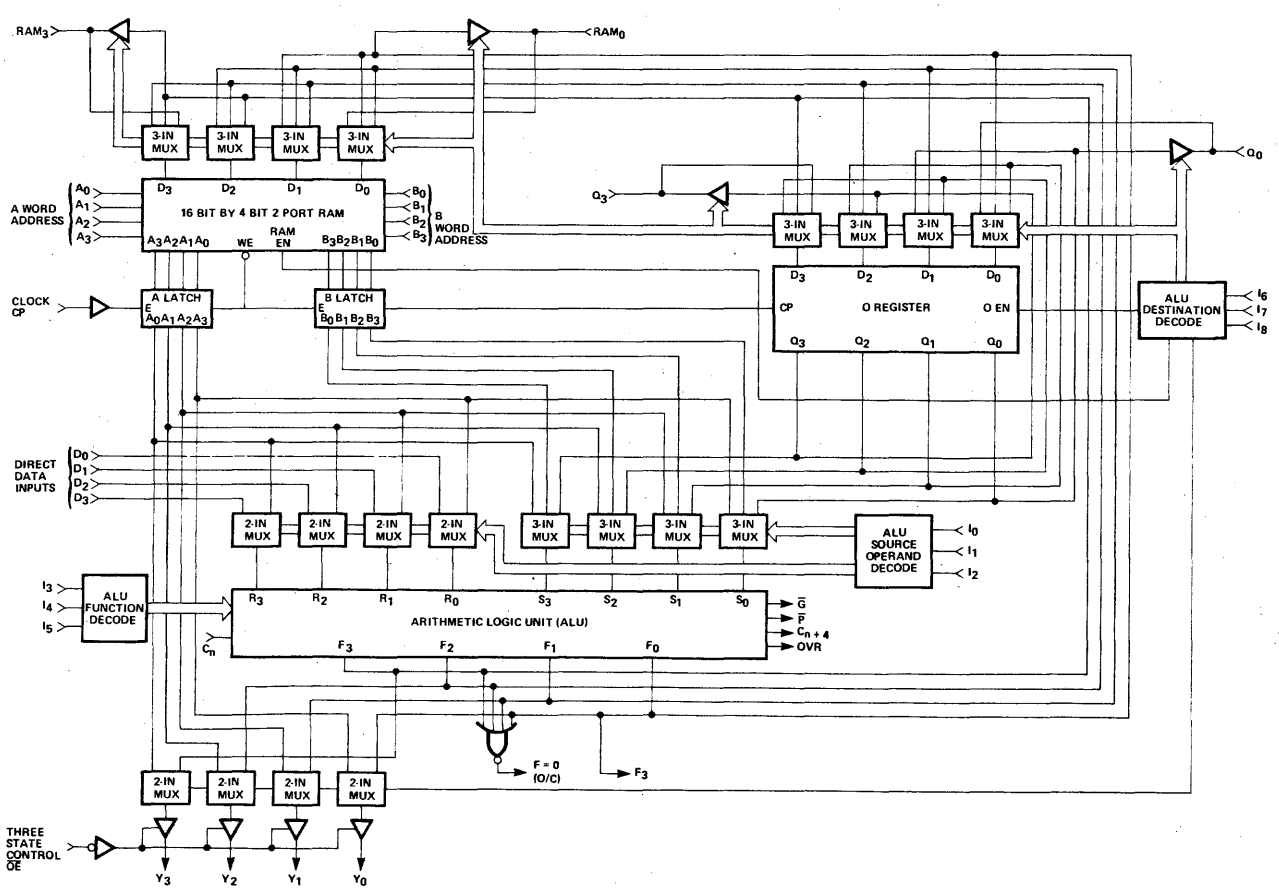


Figure 1

MICRO CODE				ALU SOURCE OPERANDS	
I_2	I_1	I_0	Octal Code	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	0	Q
L	H	H	3	0	B
H	L	L	4	0	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	0

Table 1 ALU SOURCE OPERAND CONTROL

The 2 source operands not fully described as yet are the D input and Q input. The D input is the 4-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing 3 binary arithmetic and 5 logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Table 2. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, G, and carry propagate, P, are outputs of the device for use with a carry-look-ahead-generator such as the N74S182. A carry-out, C_{n+4}, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active high.

MICRO CODE				ALU	
I_5	I_4	I_3	Octal Code	Function	Symbol
L	L	L	0	R Plus S	R + S
L	L	H	1	S Minus R	S - R
L	H	L	2	R Minus S	R - S
L	H	H	3	R OR S	R $\vee$ S
H	L	L	4	R AND S	R $\wedge$ S
H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
H	H	L	6	R EX-OR S	R $\forall$ S
H	H	H	7	R EX-NOR S	$\overline{R \forall S}$

Table 2 ALU FUNCTION CONTROL

The ALU has three other status-oriented outputs. These are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y_3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is high when all F outputs are low. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is high when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstructon inputs. These combinations are shown in Table 3.

MICRO CODE				RAM FUNCTION		Q REGISTER FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0 LO/RI	RAM_3 LI/RO	Q_0 LO/RI	Q_3 LI/RO
L	L	L	0	X	None	None	F → Q	F	X	X	X	X
L	L	H	1	X	None	X	None	F	X	X	X	X
L	H	L	2	None	F → B	X	None	A	X	X	X	X
L	H	H	3	None	F → B	X	None	F	X	X	X	X
H	L	L	4	Right (Down)	F/2 → B	Right (Down)	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
H	L	H	5	Right (Down)	F/2 → B	X	None	F	F_0	IN_3	Q_0	X
H	H	L	6	Left (Up)	2F → B	Left (Up)	2Q → Q	F	IN_0	F_3	IN_0	Q_3
H	H	H	7	Left (Up)	2F → B	X	None	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.

Table 3 ALU DESTINATION CONTROL

The 4-bit data output field (Y) features three-state outputs and can be directly bus organized. An output control ($\overline{OE}$) is used to enable the three-state outputs. When $\overline{OE}$ is high, the Y outputs are in the high-impedance state.

A 2-input multiplexer is also used at the data output such that either the A port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 microinstruction inputs. Refer to Table 3 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a 3-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up (left) one position (X2) or shifted down (right) one position (÷2). The shifter has 2 ports; one is labeled RAM_0 and the other is labeled RAM_3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the RAM_3 buffer is enabled and the RAM_0 multiplexer input is enabled. Likewise, in the shift down mode, the RAM_0 buffer and RAM_3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I_6, I_7, and I_8 microinstruction inputs as defined in Table 3.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has 2 ports; one is labeled Q_0 and the other is Q_3. The operation of these 2 ports is similar to the RAM shifter and is also controlled from I_6, I_7, and I_8 as shown in Table 3.

The clock input to the 2901-1 controls the RAM, the Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the low-to-high transition of the clock. When the clock input is high, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is low, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B address field when the clock input is low.

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SOURCE OPERANDS AND ALU FUNCTIONS

There are eight source operand pairs available to the ALU as selected by the I_0, I_1, and I_2 instruction inputs. The ALU can perform eight functions; five logic and three arithmetic. The I_3, I_4, and I_5 instruction inputs control this function selection. The carry input, C_n, also affects the ALU results when in the arithmetic mode. The C_n input has no effect in the logic mode. When I_0 through I_5 and C_n are viewed together, the matrix of Table 4 results. This matrix fully defines the ALU/source operand function for each state.

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode, the carry will affect the function performed while in the logic mode, the carry will have no bearing on the ALU output. Table 5 defines the various logic operations that the 2901-1 can perform and Table 6 shows the arithmetic functions of the device. Both carry-in low (C_n = 0) and carry-in high (C_n = 1) are defined in these operations.

OCTAL I_{543}, I_{210}	GROUP	FUNCTION
4 0	AND	A ∧ Q
4 1		A ∧ B
4 5		D ∧ A
4 6		D ∧ Q
3 0	OR	A ∨ Q
3 1		A ∨ B
3 5		D ∨ A
3 6		D ∨ Q
6 0	EX-OR	A ∀ Q
6 1		A ∀ B
6 5		D ∀ A
6 6		D ∀ Q
7 0	EX-NOR	$\overline{A \forall Q}$
7 1		$\overline{A \forall B}$
7 5		$\overline{D \forall A}$
7 6		$\overline{D \forall Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A}$ ∧ Q
5 1		$\overline{A}$ ∧ B
5 5		$\overline{D}$ ∧ A
5 6		$\overline{D}$ ∧ Q

Table 5 ALU LOGIC MODE FUNCTIONS (C_n Irrelevant)

OCTAL I_5 I_4 I_3	I_{210} OCTAL	0	1	2	3	4	5	6	7
	ALU Source / ALU Function	A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L R Plus S	A + Q	A + B	Q	B	A	D + A	D + Q	D
	C_n = H	A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	C_n = L S Minus R	Q-A-1	B-A-1	Q-1	B-1	A-1	A-D-1	Q-D-1	-D-1
	C_n = H	Q-A	B-A	Q	B	A	A-D	Q-D	-D
2	C_n = L R Minus S	A-Q-1	A-B-1	-Q-1	-B-1	-A-1	D-A-1	D-Q-1	D-1
	C_n = H	A-Q	A-B	-Q	-B	-A	D-A	D-Q	D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ∀ Q	A ∀ B	Q	B	A	D ∀ A	D ∀ Q	D
7	R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

+ = Plus; - = Minus, ∨= OR; ∧= AND, ∀= EX-OR

Table 4 SOURCE OPERAND AND ALU FUNCTION MATRIX

OCTAL	C_n = 0 (LOW)		C_n = 1 (HIGH)	
I_{543}, I_{210}	Group	Function	Group	Function
0 0	ADD	A + Q	ADD plus one	A + Q + 1
0 1		A + B		A + B + 1
0 5		D + A		D + A + 1
0 6		D + Q		D + Q + 1
0 2	PASS	Q	Increment	Q + 1
0 3		B		B + 1
0 4		A		A + 1
0 7		D		D + 1
1 2	Decrement	Q - 1	PASS	Q
1 3		B - 1		B
1 4		A - 1		A
2 7		D - 1		D
2 2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2 3		-B - 1		-B
2 4		-A - 1		-A
1 7		-D - 1		-D
1 0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1 1		B - A - 1		B - A
1 5		A - D - 1		A - D
1 6		Q - D - 1		Q - D
2 0		A - Q - 1		A - Q
2 1		A - B - 1		A - B
2 5		D - A - 1		D - A
2 6		D - Q - 1		D - Q

Table 6 ALU ARITHMETIC MODE FUNCTIONS

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LOGIC FUNCTIONS FOR $\overline{G}$, $\overline{P}$, C_{n+4}, AND OVR

The four signals $\overline{G}$, $\overline{P}$, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the 2901-1 is in the add or subtract mode. Table 7 indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Table 1.

I_{543}	FUNCTION	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S - R	← Same as R+S equations, but substitute $\overline{R}_i$ for R_i in definitions →			
2	R - S	← Same as R+S equations, but substitute $\overline{S}_i$ for S_i in definitions →			
3-7	All logic operations	High	Low	High	High

Table 7 LOGIC EQUATIONS

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$
$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$
$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$
$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$

$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant +70°C$, 4.75V, $V_{CC} \leqslant 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
V_{OH}	High level output voltage	V_{CC} = 4.75V, I_{OH} = 1.6mA	2.4			V
I_{CEX}	Output leakage current for F = 0 output	V_{CC} = 4.75V, V_{OH} = 5.25V, $V_{IN} = V_{IH}$ or V_{IL}			250	μA
V_{OL}	Low level output voltage	V_{CC} = 4.75V				
	Y	I_{OL} = 20mA			0.5	V
	$\overline{G}$	I_{OL} = 16mA			0.5	V
	C_{n+4}, F = 0, OVR, $\overline{P}$, F_3	I_{OL} = 10mA			0.5	V
	$RAM_{3,0}$, $Q_{3,0}$	I_{OL} = 6mA			0.5	V
V_{IH}	High level input voltage		2.0			V
V_{IL}	Low level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_I = -18mA			-1.5	V
I_I	High level input current at maximum input voltage	V_{CC} = 5.25V, V_I = 5.5V			1.0	mA
I_{IH}	High level input current	V_{CC} = 5.25V, V_I = 2.7V				
	Clock, $\overline{OE}$, A, B, D, I, C_n				20	μA
	$RAM_{3,0}$, $Q_{3,0}$ (Note 1)				20	μA
I_{IL}	Low level input current	V_{CC} = 5.25V, V_I = 0.5V				
	Clock, DE, A, B, D, I, C_n				50	μA
	$RAM_{3,0}$, $Q_{3,0}$ (Note 1)				-100	μA
I_{OS}	Short circuit output current (Note 2)	V_{CC} = 5.25V	-10		-40	mA
I_{OZ}	High-Z state output current $Y_0 - Y_3$	V_0 = 2.4V			50	μA
		V_0 = 0.5V			-50	μA
	$RAM_{3,0}$ $Q_{3,0}$	V_0 = 2.4V			100	μA
		V_0 = 0.5V			-100	μA
I_{CC}	Supply current	V_{CC} = 5.25V		165	265	mA

NOTES

1. LO/RI and RO/LI are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I_{678} in a state such that the three-state output is OFF.
2. Not more than 1 output should be shorted at a time. Duration of the short-circuit test should not exceed 1 second.

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ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-state output voltage	+5.5	Vdc
T_A	Operating temperature range	0° to +70°	°C
T_{STG}	Storage temperature range	-65° to +150°C	°C

AC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
	Clock Times[1]				
t_{CY}	Clock cycle time	80	65		ns
t_{RMW}	Ready-modify-write cycle	70	55		ns
f_Q	Clock frequency to shift Q register	25	30		MHz
t_{CL}	Clock low period	30	22		ns
t_{CH}	Clock high period	30	13		ns
	Hold Times[1]				
t_H	Any input	0	-3		ns
	Setup Times[1]				
t_{SAB}	A, B, setup time[2, 3, 4]	90	65		ns
		t_{CL} + 30	t_{CL} + 15		ns
t_{SBD}	B destination setup time[2, 3, 4]	t_{CL} + 15	t_{CL} + 5		ns
t_{SD}	D input setup time	60	45		ns
t_{SCn}	Cn input setup time	50	35		ns
t_{SI012}	ALU source control setup time	80	60		ns
t_{SI345}	ALU function setup time	75	58		ns
t_{SI678}	ALU destination control setup time[5]	t_{CL} + 25	t_{CL} + 15		ns
t_{SS}	$RAM_{3,0}$, input setup time	30	20		ns
	$Q_{3,0}$	15	10		

NOTES

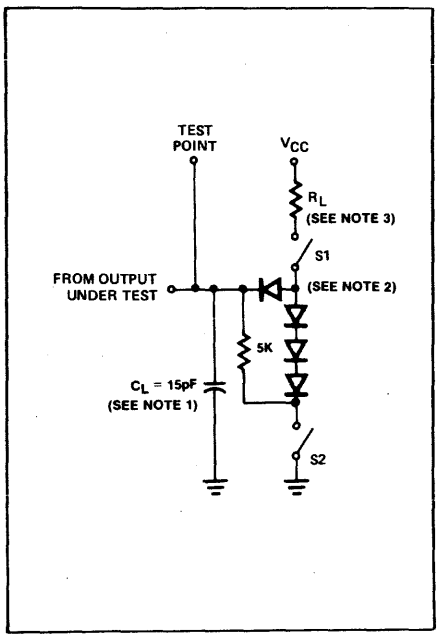
1. Setup and hold times are defined relative to the clock low-to-high edge. Inputs must be steady at all times from the setup time prior to the clock until the hold after the clock. The setup times allow sufficient time to perform the correct operation on the correct operation on the correct data so that the correct ALU data can be written into one of the registers.
2. If the B address is used as a source operand, allow for the A, B source setup time; if it is used only for the destination address, use the B dest. setup time.
3. Where 2 numbers are shown, both must be met.
4. t_{CL} is the clock low time.

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PROPAGATION DELAYS (ns) C_L = 15pF T_A = 0° to +70°C, V_{CC} = 5.0V ± 5%

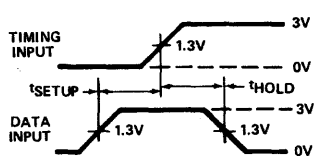
From Input \ To Output	Y	F_3	C_{n+4}	$\overline{G}$, $\overline{P}$	F = 0 RL = 470	OVR	SHIFT OUTPUTS	
							RAM	Q
Clock	60	55	45	50	65	50	65	45
A, B	75	65	60	70	80	60	80	—
D (arithmetic mode)	40	30	30	40	55	40	55	—
D(I = X37, logic mode)	40	30	—	—	55	—	55	—
C_n	40	25	25	—	45	30	50	—
I_{012}	60	50	45	50	60	45	65	—
I_{345}	55	40	40	50	50	45	60	—
I_{678}	30	—	—	—	—	—	45	45
$\overline{OE}$ Enable/Disable	25/30	—	—	—	—	—	—	—
A bypassing ALU (I = 2xx)	45	—	—	—	—	—	—	—

TEST LOAD CIRCUIT

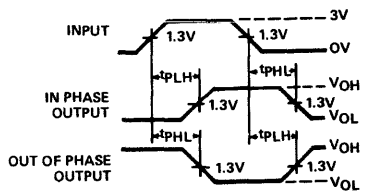


VOLTAGE WAVEFORMS

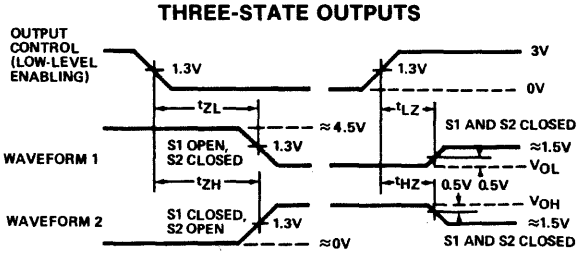
SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES THREE-STATE OUTPUTS



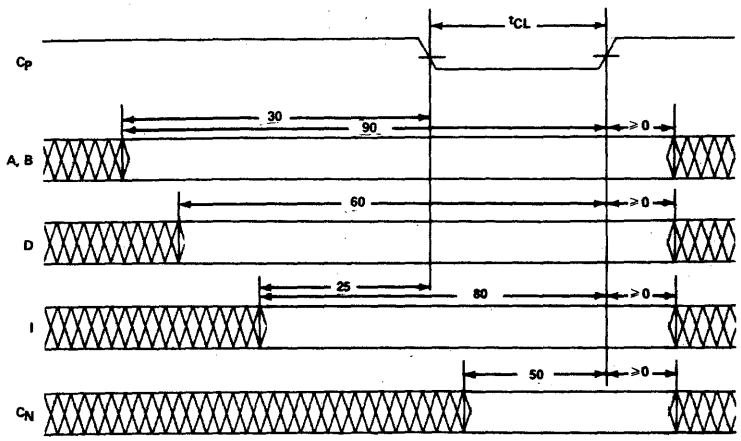
NOTES

1. C_L includes probe and jig capacitance.
2. All diodes 1N916 or 1N3064.
3. R_L = 2K

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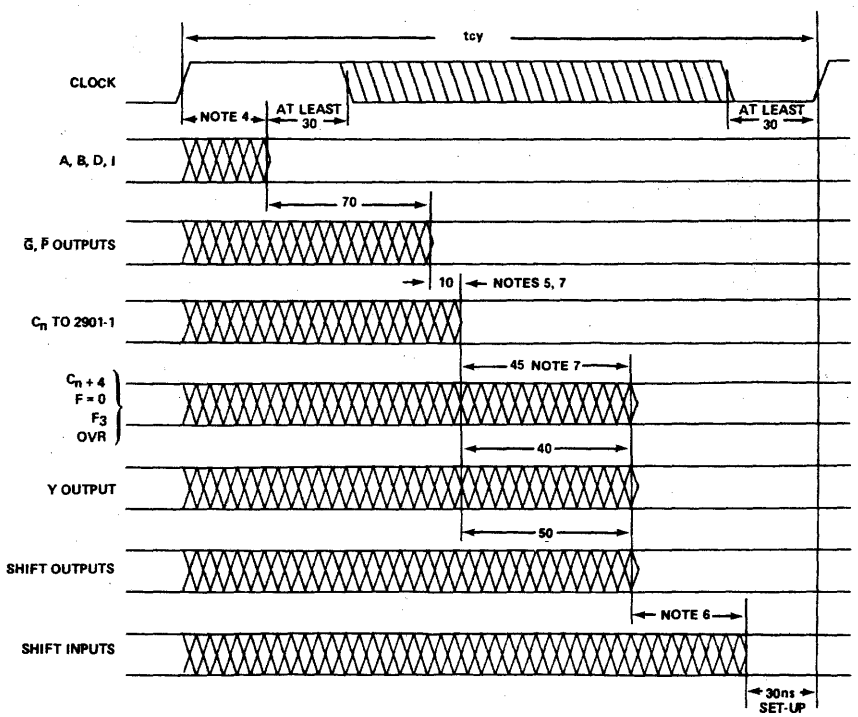
VOLTAGE WAVEFORMS (Cont'd) $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$

MINIMUM CYCLE TIMES FROM INPUTS



Numbers Shown Are Minimum Data Stable Times for 2901-1, DC, in ns.

SWITCHING WAVEFORMS FOR 16-BIT SYSTEM



Assuming A, B, D, and I are all Driven from Registers with the same Propagation Delay, Clocked by the 2901-1 Clock.

NOTES

4. This delay is the max. tpd of the register containing A, B, D, and I.
5. 10ns for lookahead carry. For ripple carry over 16 bits use 2 x (Cn →Cn + 4).
6. This is the delay associated with the multiplexer between the shift outputs and shift inputs on the 2901-1s. Normally applicable only for double length or circular shifts.
7. Not applicable for logic operations.

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S/N3001-I

DESCRIPTION

The S/N3001 MCU is 1 element of a bipolar microcomputer set. When used with the S/N3002, 54/74S182, ROM or PROM memory, a powerful microprogrammed computer can be implemented.

The 3001 MCU controls the fetch sequence of microinstructions from the microprogram memory. Functions performed by the 3001 include:

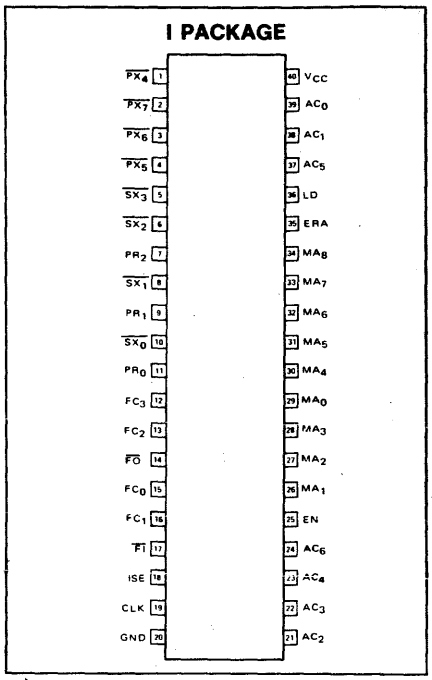
- Maintenance of microprogram address register
- Selection of next microinstruction address
- Decoding and testing of data supplied via several input buses
- Saving and testing of carry output data from the central processing (CP) array
- Control of carry/shift input data to the CP array
- Control of microprogram interrupts

FEATURES

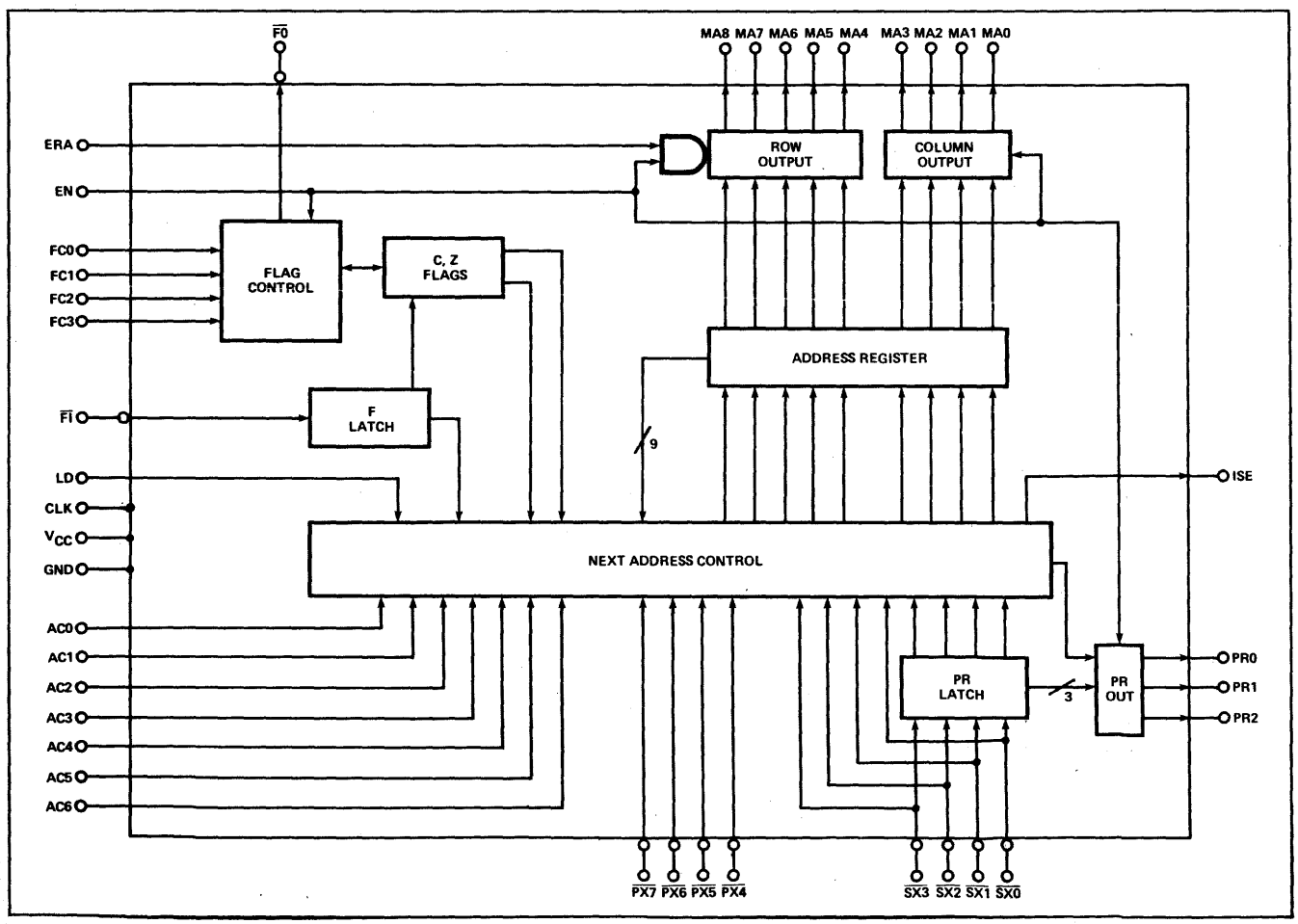
- **Schottky TTL process**
- **45ns cycle time (typ.)**
- **Direct addressing of standard bipolar PROM or ROM**
- **512 microinstruction addressability**
- **Advanced organization:**
  - **9-bit microprogram address register and bus organized to address memory by row and column**
  - **4-bit program latch**
  - **2-flag registers**
- **11 address control functions:**
  - **3 jump and test latch function**
  - **16 way jump and test instruction**
- **8 flag control functions:**
  - **4 flag input functions**
  - **4 flag output functions**

PIN CONFIGURATION

I PACKAGE



BLOCK DIAGRAM



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PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-4	$\overline{PX_4}$-$\overline{PX_7}$	Primary Instruction Bus Inputs Data on the primary instruction bus is tested by the JPX function to determine the next microprogram address.	Active low
5,6,8,10	$\overline{SX_0}$-$\overline{SX_3}$	Secondary Instruction Bus Inputs Data on the secondary instruction bus is synchronously loaded into the PR-latch while the data on the PX-bus is being tested (JPX). During a subsequent cycle, the contents of the PR-latch may be tested by the JPR, JLL, or JRL functions to determine the next microprogram address.	Active low
7,9,11	PR_0-PR_2	PR-Latch Outputs The PR-latch outputs (SX_0-SX_2) are synchronously enabled by the JCE function. They can be used to modify microinstructions at the outputs of the microprogram memory or to provide additional control lines.	Open Collecto
12,13 15,16	FC_0-FC_3	Flag Logic Control Inputs The flat logic control inputs are used to cross-switch the flags (C and Z) with the flag logic input (FI) and the flag logic output (FO).	Active high
14	$\overline{FO}$	Flag Logic Output The outputs of the flags (C and Z) are multiplexed internally to form the common flag logic output. The output may also be forced to a logical 0 or logical 1.	Active low Three-state
17	$\overline{FI}$	Flag Logic Input The flag logic input is demultiplexed internally and applied to the inputs of the flags (C and Z). Note: The flag input data is saved in the F-latch when the clock input (CLK) is low.	Active low
18	ISE	Interrupt Strobe Enable Output The interrupt strobe enable output goes to logical 1 when one of the JZR functions are selected (see Functional Description). It can be used to provide the strobe signal required by interrupt circuits.	Active high
19	CLK	Clock Input	
20	GND	Ground	
21-24 37-39	AC_0-AC_6	Next Address Control Function Inputs All jump functions are selected by these control lines.	Active high
25	EN	Enable Input When in the high state, the enable input enables the microprogram address, PR-latch and flag outputs.	
26-29	MA_0-MA_3	Microprogram Column Address Outputs	Three-state
30-34	MA_4-MA_8	Microprogram Row Address Outputs	Three-state
35	ERA	Enable Row Address Input When in the low state, the enable row address input independently disables the microprogram row address outputs. It can be used to facilitate the implementation of priority interrupt systems.	Active high
36	LD	Microprogram Address Load Input When the active high state, the microprogram address load input inhibits all jump functions and synchronously loads the data on the instruction buses into the microprogram address register. However, it does not inhibit the operation of the PR-latch or the generation of the interrupt strobe enable.	Active high
40	V_{CC}	+5 Volt supply	

THEORY OF OPERATION

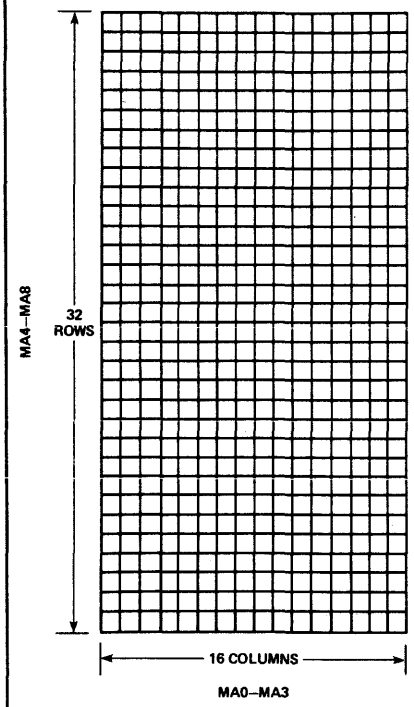
The MCU controls the sequence of microinstructions in the microprogram memory. The MCU simultaneously controls 2 flip-flops (C, Z) which are interactive with the carry-in and carry-out logic of an array of CPEs.

The functional control of the MCU provides both unconditional jumps to new memory locations and jumps which are dependent on the state of MCU flags or the state of the "PR" latch. Each instruction has a "jump set" associated with it. This "jump set" is the total group of memory locations which can be addressed by that instruction.

The MCU utilizes a two-dimensional addressing scheme in the microprogram memory. Microprogram memory is organized as 32 rows and 16 columns for a total of 512 words. Word length is variable according to application. Address is accomplished by a 9-bit address organized as a 5-bit row and 4-bit column address.

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ADDRESSING ORGANIZATION



FUNCTIONAL DESCRIPTION

The following is a description of each of the eleven address control functions. The symbols shown below are used to specify row and column addresses.

MNEMONIC	FUNCTION
row_n	5-bit next row address where n is the decimal row address.
col_n	4-bit next column address where n is the decimal column address.

Unconditional Address Control (Jump) Functions

The jump functions use the current microprogram address (i.e., the contents of the microprogram address register prior to the rising edge of the clock) and several bits from the address control inputs (AC0-AC6) to generate the next microprogram address.

Flag Conditional Address Control (Jump Test) Functions

The jump/test flag functions use the current microprogram address, the contents of the selected flag or latch, and several bits from the address control function to generate the next microprogram address.

JUMP FUNCTION TABLE

MNEMONIC	NAME AND FUNCTION
JCC	Jump in current column. AC_0-AC_4 are used to select 1 of 32 row addresses in the current column, specified by MA_0-MA_3, as the next address.
JZR	Jump to zero row. AC_0-AC_3 are used to select 1 of 16 column addresses in row_0, as the next address.
JCR	Jump in current row. AC_0-AC_3 are used to select 1 of 16 addresses in the current row, specified by MA_4-MA_8, as the next address.
JCE	Jump in current column/row group and enable PR-latch outputs. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7-MA_8, as the next row address. The current column is specified by MA_0-MA_3. The PR-latch outputs are asynchronously enabled.

JUMP/TEST FUNCTION TABLE

MNEMONIC	NAME AND FUNCTION
JFL	Jump/test F-latch. AC_0-AC_3 are used to select 1 of 16 row addresses in the current row group, specified by MA_8, as the next row address. If the current column group, specified by MA_3, is col_0-col_7, the F-latch is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group col_8-col_{15}, the F-latch is used to select col_{10} or col_{11} as the next column address.
JCF	Jump/test C-flag. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. If the current column group specified by MA_3 is col_0-col_7, the C-flag is used to select col_2 or col_3 as the next column address. If MA_3 specifies column group col_8-col_{15}, the C-flag is used to select col_{10} or col_{11} as the next column address.
JZF	Jump/test Z-flag. Identical to the JCF function described above, except that the Z-flag, rather than the C-flag, is used to select the next column address.
JPR	Jump/test PR-latch. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. The 4 PR-latch bits are used to select 1 of 16 possible column addresses as the next column address.
JLL	Jump/test leftmost PR-latch bits. AC_0-AC_2 are used to select 1 of 8 row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_2 and PR_3 are used to select 1 of 4 column addresses in col_4 through col_7 as the next column address.
JRL	Jump/test rightmost PR-latch bits. AC_0 and AC_1 are used to select 1 of 4 high-order row addresses in the current row group, specified by MA_7 and MA_8, as the next row address. PR_0 and PR_1 are used to select 1 of 4 possible column addresses in col_{12} through col_{16} as the next column address.
JPX	Jump/test PX-bus and load PR-latch. AC_0 and AC_1 are used to select 1 of 4 row addresses in the current row group, specified by MA_6-MA_8, as the next row address. PX_4-PX_7 are used to select 1 of 16 possible column addresses as the next column address. SX_0-SX_3 data is locked in the PR-latch at the rising edge of the clock.

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PX-Bus and PR-Latch Conditional Address Control (Jump/Test) Functions

The PX-bus jump/test function uses the data on the primary instruction bus (PX_4-PX_7), the current microprogram address, and several selection bits from the address control function to generate the next microprogram address. The PR-latch jump/test functions use the data held in the PR-latch, the current microprogram address, and several selection bits from the address control function to generate the next microprogram address.

Flag Control Functions

The flag control functions of the MCU are selected by the 4 input lines designated FC_0-FC_3. Function code formats are given in "Flag Control Function summary."

The following is a detailed description of each of the 8 flag control functions.

Flag Input Control Functions

The flag input control functions select which flag or flags will be set to the current value of the flag input ($\overline{FI}$) line.

Data on $\overline{FI}$ is stored in the F-latch when the clock is low. The content of the F-latch is loaded into the C and/or Z flag on the rising edge of the clock.

Flag Output Control Functions

The flag output control functions select the value to which the flag output ($\overline{FO}$) line will be forced.

FLAG CONTROL FUNCTION TABLE

MNEMONIC	FUNCTION DESCRIPTION
SCZ	Set C-flag and Z-flag to FI. The C-flag and the Z-flag are both set to the value of FI.
STZ	Set Z-flag to FI. The Z-flag is set to the value of FI. The C-flag is unaffected.
STC	Set C-flag to FI. The C-flag is set to the value of FI. The Z-flag is unaffected.
HCZ	Hold C-flag and Z-flag. The values in the C-flag and Z-flag are unaffected.

FLAG OUTPUT CONTROL FUNCTION TABLE

MNEMONIC	FUNCTION DESCRIPTION
FF0	Force FO to 0. FO is forced to the value of logical 0.
FFC	Force FO to C. FO is forced to the value of the C-flag.
FFZ	Force FO to Z. FO is forced to the value of the Z-flag.
FF1	Force FO to 1. FO is forced to the value of logical 1.

FLAG CONTROL FUNCTION SUMMARY

TYPE	MNEMONIC	DESCRIPTION	FC_1	0
Flag Input	SCZ	Set C-flag and Z-flag to f	0	0
	STZ	Set Z-flag to f	0	1
	STC	Set C-flag to f	1	0
	HCZ	Hold C-flag and Z-flag	1	1

TYPE	MNEMONIC	DESCRIPTION	FC_3	2
Flag Output	FF0	Force FO to 0	0	0
	FFC	Force FO to C-flag	1	0
	FFZ	Force FO to Z-flag	0	1
	FF1	Force FO to 1	1	1

LOAD FUNCTION	NEXT ROW					NEXT COL				
LD	MA_8	7	6	5	4	MA_3	2	1	0	
0	See Address Control Function Summary									
1	0	X_3	X_2	X_1	X_0	X_7	X_6	X_5	X_4	

NOTE

f = Contents of the F-latch xn = Data on PX- or SX-bus line n (active low)

ADDRESS CONTROL FUNCTION SUMMARY

MNEMONIC	DESCRIPTION	FUNCTION							NEXT ROW					NEXT COL			
		AC_6	5	4	3	2	1	0	MA_8	7	6	5	4	MA_3	2	1	0
JCC	Jump in current column	0	0	d_4	d_3	d_2	d_1	d_0	d_4	d_3	d_2	d_1	d_0	m_3	m_2	m_1	m_0
JZR	Jump to zero row	0	1	0	d_3	d_2	d_1	d_0	0	0	0	0	0	d_3	d_2	d_1	d_0
JCR	Jump in current row	0	1	1	d_3	d_2	d_1	d_0	m_8	m_7	m_6	m_5	m_4	d_3	d_2	d_1	d_0
JCE	Jump in column/enable	1	1	1	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	m_2	m_1	m_0
JFL	Jump/test F-latch	1	0	0	d_3	d_2	d_1	d_0	m_8	d_3	d_2	d_1	d_0	m_3	0	1	f
JCF	Jump/test C-flag	1	0	1	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	0	1	c
JZF	Jump/test Z-flag	1	0	1	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	m_3	0	1	Z
JPR	Jump/test PR-latch	1	1	0	0	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	p_3	p_2	p_1	p_0
JLL	Jump/test left PR bits	1	1	0	1	d_2	d_1	d_0	m_8	m_7	d_2	d_1	d_0	0	1	p_3	p_2
JRL	Jump/test right PR bits	1	1	1	1	1	d_1	d_0	m_8	m_7	1	d_1	d_0	1	1	p_1	p_0
JPX	Jump/test PX-bus	1	1	1	1	0	d_1	d_0	m_8	m_7	m_6	d_1	d_0	x_7	x_6	x_5	x_4

NOTE

dn = Data on address control line n
mn = Data in microprogram address register bit n
Pn = Data in PR-latch bit n
xn = Data on PX-bus line n (active low)
f,c,z = Contents of F-latch, C-flag, or Z-flag, respectively

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STROBE FUNCTIONS

The load function of the MCU is controlled by the input line designated LD. If the LD line is active high at the rising edge of the clock, the data on the primary and secondary instruction buses, PX_4-PX_7 and SX_0-SX_3, is loaded into the microprogram address register. PX_4-PX_7 are loaded into MA_0-MA_7 and SX_0-SX_3 are loaded into MA_4-MA_7. The high-order bit of the microprogram address register MA_8 is set to a logical 0. The bits from the primary instruction bus select 1 of 16 possible column addresses. Likewise, the bits from the secondary instruction bus select 1 of the first 16 row addresses.

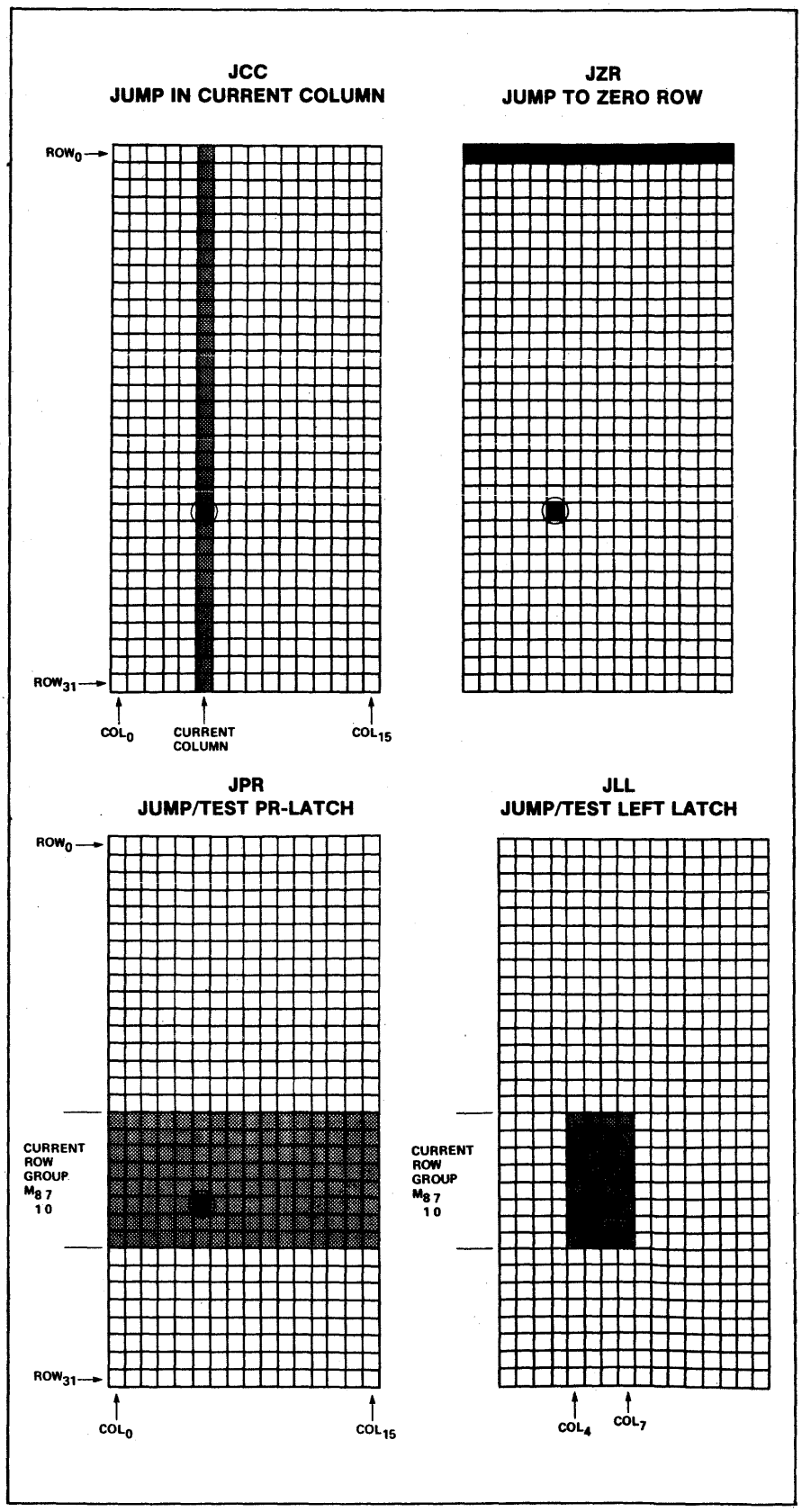
The MCU generates an interrupt strobe enable on the output line designated ISE. The line is placed in the active high state whenever a JZR to col_{15} is selected as the address control function. Generally, the start of a macroinstruction fetch sequence is situated at row_0 and col_{15} so the interrupt control may be enabled at the beginning of the fetch/execute cycle. The interrupt control responds to the interrupt by pulling the enable row address (ERA) input line low to override the selected next row address from the MCU. Then by gating an alternative next row address on to the row address lines of the microprogram memory, the microprogram may be forced to enter an interrupt handling routine. The alternative row address placed on the microprogram memory address lines does not alter the contents of the microprogram address register. Therefore, subsequent jump functions will utilize the row address in the register, and not the alternative row address, to determine the next microprogram address.

Note, the load function always overrides the address control function on AC_0-AC_6. It does not, however, override the latch enable or load sub-functions of the JCE or JPX instruction, respectively. In addition, it does not inhibit the interrupt strobe enable or any of the flag control functions.

JUMP SET DIAGRAMS

The following 10 diagrams illustrate the jump set for each of the 11 jump and jump/test functions of the MCU. Location 341 indicated by the circled square, represents 1 current row (row_{21}) and current column (col_5) address. The dark boxes indicate the microprogram locations that may be selected by the particular function as the next address.

JUMP SET DIAGRAMS



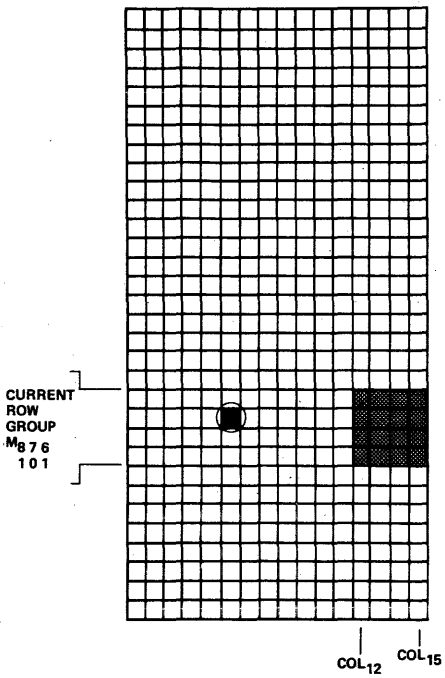
Signetics

MICROPROCESSOR

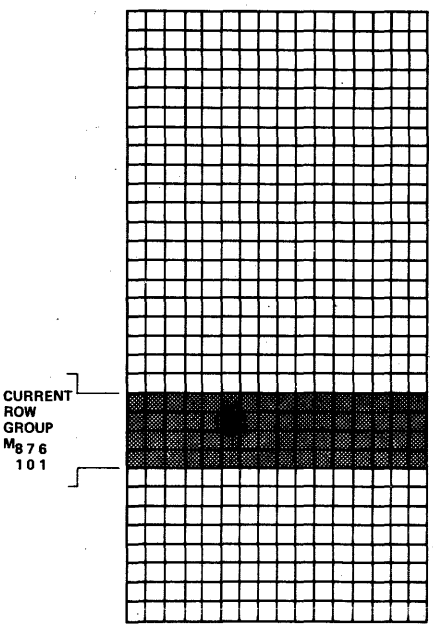
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JUMP SET DIAGRAMS (Cont'd)

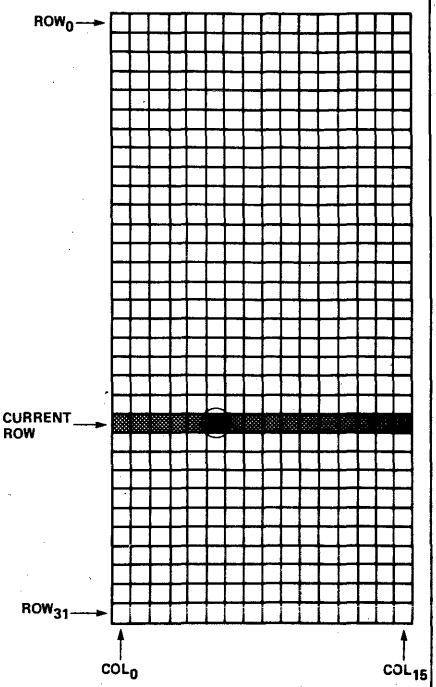
JRL
JUMP/TEST RIGHT LATCH



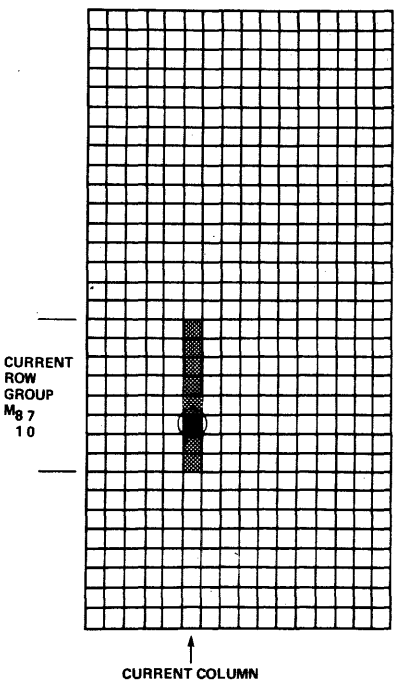
JPX
JUMP/TEST PX-BUS



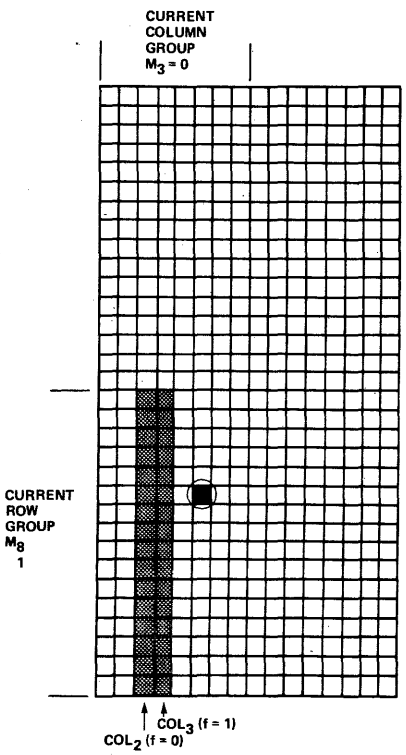
JCR
JUMP IN CURRENT ROW



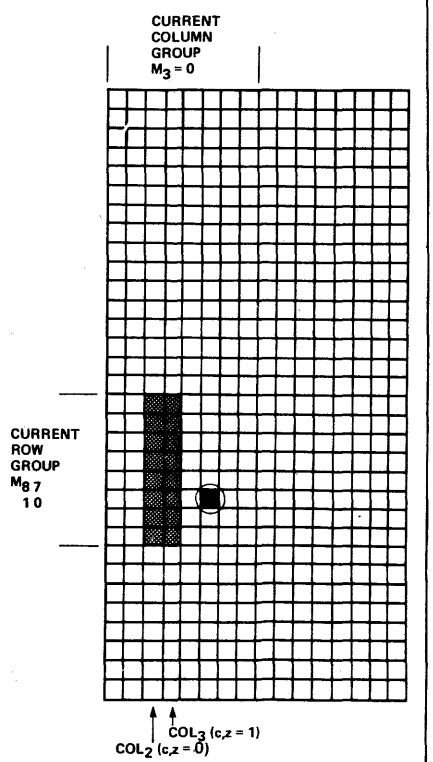
JCE
JUMP COLUMN/ENABLE



JFL
JUMP/TEST F-LATCH



JCF, JZF
JUMP/TEST C-FLAG
JUMP/TEST Z-FLAG



AC ELECTRICAL CHARACTERISTICS

N3001 T_A = 0°C to +70°C, V_{CC} = 5.0V, ± 5% S/N3001-I

S3001 T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

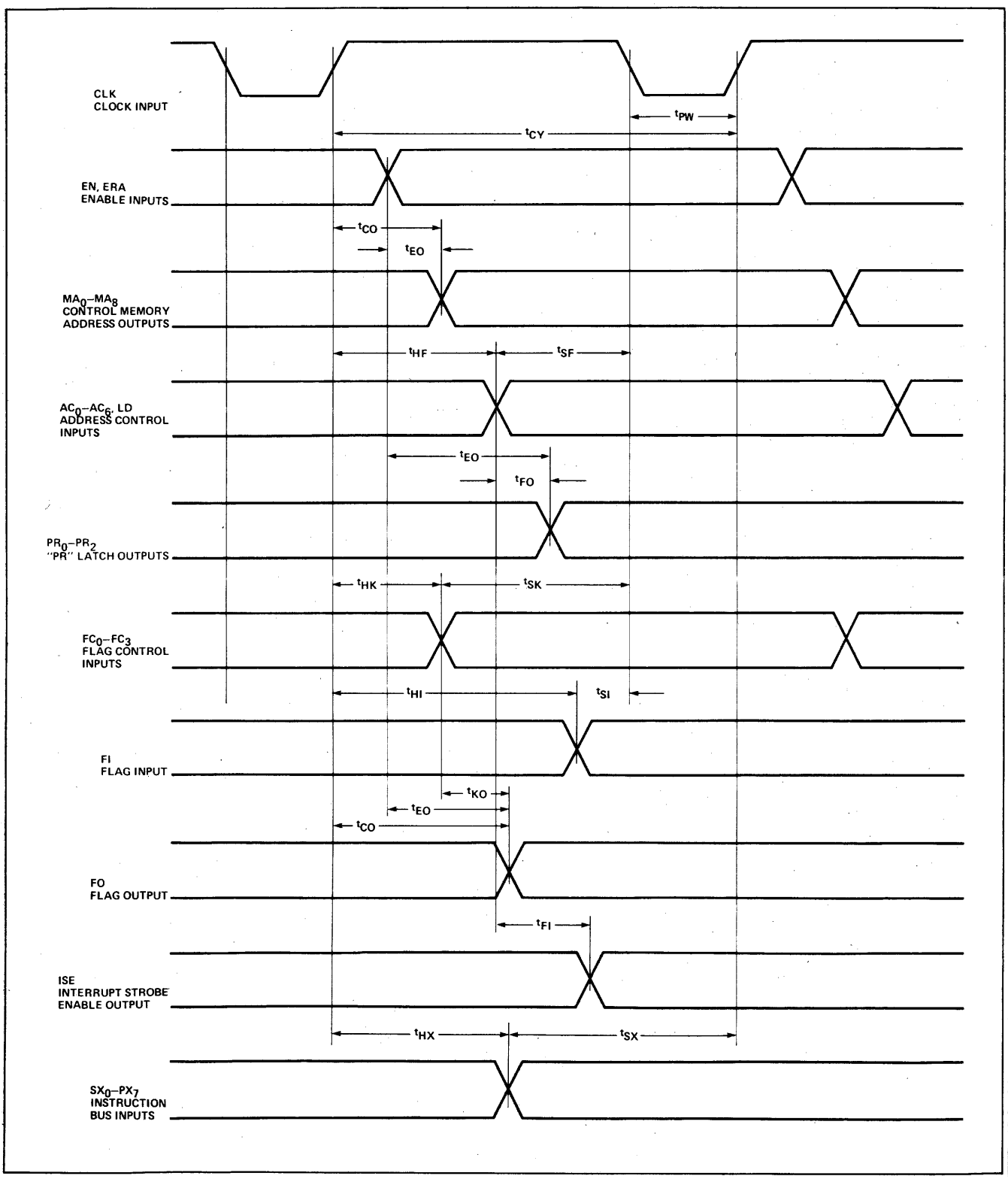
	PARAMETER	N3001			S3001			UNIT
		Min	Typ[1]	Max	Min	Typ[1]	Max	
t_{CY}	Cycle Time[2]	60	45		95	45		ns
t_{PW}	Clock Pulse Width	17	10		40	10		ns
	Control and Data Input Set-Up Times:							
t_{SF}	LD, AC_0-AC_6 (Set to "1"/"0")	20	3/14		20	3/14		ns
t_{SK}	FC_0, FC_1	7	5		10	5		ns
t_{SX}	PX_4-PX_7 (Set to "1"/"0")	28	4/13		35	4/13		ns
t_{SI}	FI (Set to "1"/"0")	12	-6/0		15	-6/10		ns
t_{SX}	SX_0-SX_3	15	5		35	5		ns
	Control and Data Input Hold Times:							
t_{HF}	LD, AC_0-AC_6 (Hold to "1"/"0")	4	-3/-14		5	-3/-14		ns
t_{HK}	FC_0, FC_1	4	-5		10	-5		ns
t_{HX}	PX_4-PX_7 (Hold to "1"/"0")	0	-4/-13		25	-4/-13		ns
t_{HI}	FI (Hold to "1"/"0")	16	6.5/0		22	6.5/0		ns
t_{HX}	SX_0-SX_3	0	-5		25	-5		ns
t_{CO}	Propagation Delay from Clock Input (CLK) to Outputs (mA_0-mA_8, FO) (tPHL/tPLH)		17/24	36	10	17/24	45	ns
t_{KO}	Propagation Delay from Control Inputs FC_2 and FC_3 to Flag Out (FO)		13	24		13	50	ns
t_{FO}	Propagation Delay from Control Inputs AC_0-AC_6 to Latch Outputs (PR_0-PR_2)		21	32		21	50	ns
t_{EO}	Propagation Delay from Enable Inputs EN and ERA to Outputs (mA_0-mA_8, FO, PR_0-PR_2)		17	26		17	35	ns
t_{FI}	Propagation Delay from Control Inputs AC_0-AC_6 to Interrupt Strobe Enable Output (ISE)		20	32		20	40	ns

NOTE

1. Typical values are for TA = 25°C and 5.0 supply voltage.
2. S3001: tCY = tWP + tSF + tCO

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VOLTAGE WAVEFORMS



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DESCRIPTION

The N3002 Central Processing Element (CPE) is one part of a bipolar microcomputer set. The N3002 is organized as a 2-bit slice and performs the logical and arithmetic functions required by microinstructions. A system with any number of bits in a data word can be implemented by using multiple N3002s, the N3001 microcomputer control unit, the N74S182 carry look-ahead unit and ROM or PROM memory.

FEATURES

- **45ns cycle time (typ)**
- **Easy expansion to multiple of 2 bits**
- **11 general purpose registers**
- **Full function accumulator**
- **Useful functions include:**
  - **2's complement arithmetic**
  - **Logical AND, OR, NOT, exclusive-NOR**
  - **Increment, decrement**
  - **Shift left/shift right**
  - **Bit testing and zero detection**
  - **Carry look-ahead generation**
  - **Masking via K-bus**
  - **Conditioned clocking allowing non-destructive testing of data in accumulator and scratchpad**
- **3 input buses**
- **2 output buses**
- **Control bus**

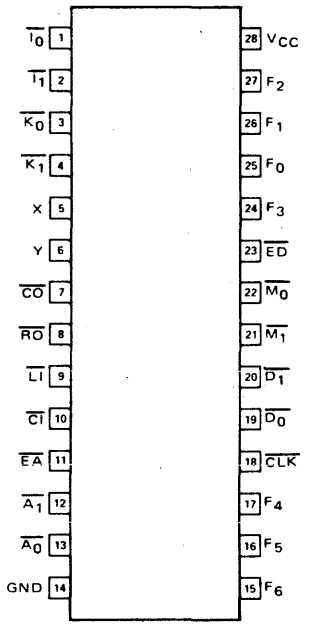
FUNCTION TRUTH TABLE

FUNCTION GROUP	F_6	F_5	F_4
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

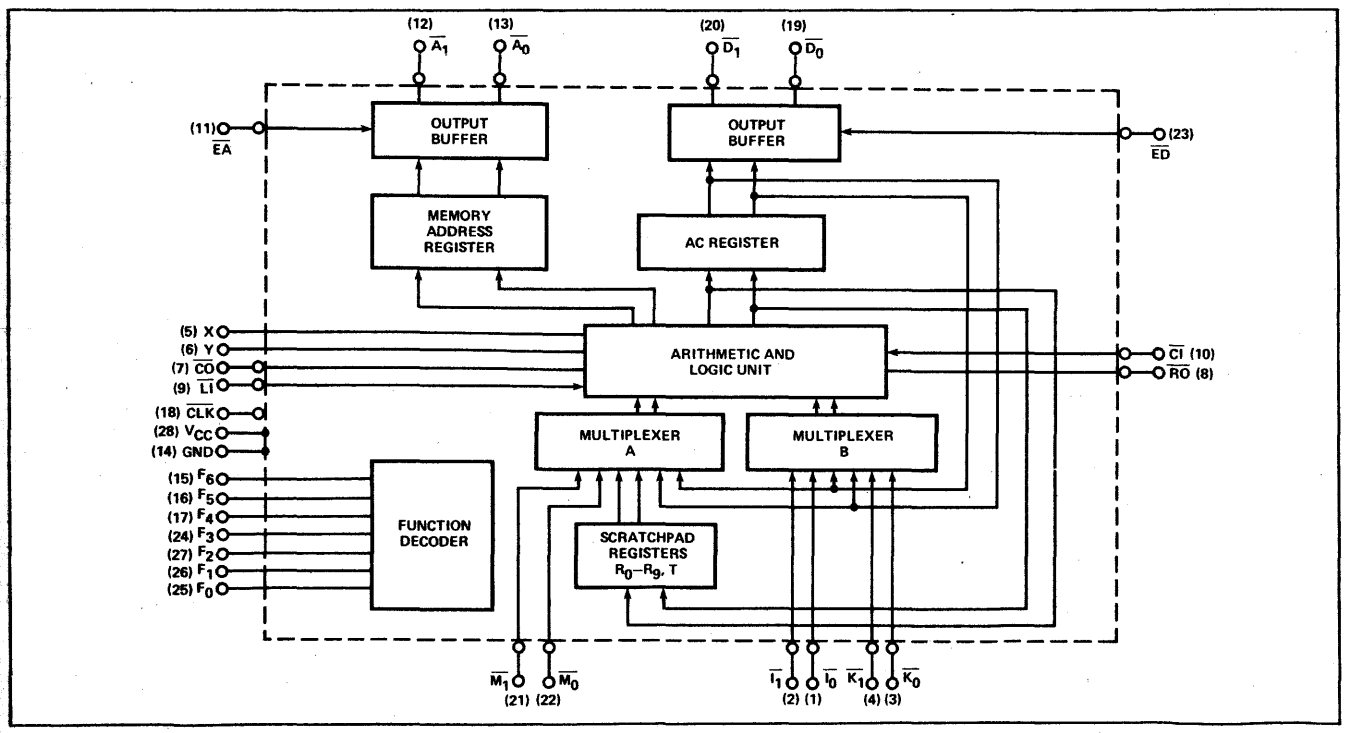
REGISTER GROUP	REGISTER	F_3	F_2	F_1	F_0
I	R_0	0	0	0	0
	R_1	0	0	0	1
	R_2	0	0	1	0
	R_3	0	0	1	1
	R_4	0	1	0	0
	R_5	0	1	0	1
	R_6	0	1	1	0
	R_7	0	1	1	1
	R_8	1	0	0	0
	R_9	1	0	0	1
	T	1	1	0	0
	AC	1	1	0	1
II	T	1	0	1	0
	AC	1	0	1	1
III	T	1	1	1	0
	AC	1	1	1	1

PIN CONFIGURATION

I,XL PACKAGE



BLOCK DIAGRAM



signetics

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PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1, 2	$\overline{I_0}$-$\overline{I_1}$	External Bus Inputs The external bus inputs provide a separate input port for external input devices.	Active low
3, 4	$\overline{K_0}$-$\overline{K_1}$	Mask Bus Inputs The mask bus inputs provide a separate input port from the microprogram memory, to allow mask or constant entry.	Active low
5, 6	X, Y	Standard Carry Look-Ahead Cascade Outputs The cascade outputs allow high speed arithmetic operations to be performed when they are used in conjunction with the 74S182 Look-Ahead Carry Generator	Active high
7	$\overline{CO}$	Ripple Carry Out The ripple carry output is only disabled during shift right operations.	Active low Three-state
8	$\overline{RO}$	Shift Right Output The shift right output is only enabled during shift right operations.	Active low Three-state
9	$\overline{LI}$	Shift Right Input	Active low
10	$\overline{CI}$	Carry Input	Active low
11	$\overline{EA}$	Memory Address Enable Input When in the low state, the memory address enable input enables the memory address outputs (A_0-A_1).	Active low
12-13	$\overline{A_0}$-$\overline{A_1}$	Memory Address Bus Outputs The memory address bus outputs are the buffered outputs of the memory address register (MAR).	Active low Three-state
14	GND	Ground	
14-17, 24-27	F_0-F_6	Micro-Function Bus Inputs The micro-function bus inputs control ALU function and register selection.	Active high
18	$\overline{CLK}$	Clock Input	
19-20	$\overline{D_0}$-$\overline{D_1}$	Memory Data Bus Outputs The memory data bus outputs are the buffered outputs of the full function accumulator register (AC).	Active low Three-state
21-22	$\overline{M_0}$-$\overline{M_1}$	Memory Data Bus Inputs The memory data bus inputs provide a separate input port for memory data.	Active low
23	$\overline{ED}$	Memory Data Enable Input When in the low state, the memory data enable input enables the memory data outputs (D_0-D_1).	Active low
28	V_{CC}	+5 Volt Supply	

SYSTEM DESCRIPTION

Microfunction Decoder and K-Bus

Basic microfunctions are controlled by a 7-bit bus (F_0-F_6) which is organized into 2 groups. The higher 3 bits (F_4-F_6) are designated as F-Group and the lower 4 bits (F_0-F_3) are designated as the R-Group. The F-Group specifies the type of operation to be performed and the R-Group specifies the registers involved.

The F-Bus instructs the microfunction decoder to:
- Select ALU functions to be performed
- Generate scratchpad register address
- Control A and B multiplexer

The resulting microfunction action can be:
- Data transfer
- Shift operations
- Increment and decrement
- Initialize stack
- Test for zero conditions
- 2's complement addition and subtraction
- Bit masking
- Maintain program counter

A and B Multiplexers

A and B multiplexers select the proper 2 operands to the ALU.

A multiplexer selects inputs from one of the following:
- M-bus (data from main memory)
- Scratchpad registers
- Accumulator

B multiplexer selects inputs from one of the following:
- I-bus (data from external I/O devices)
- Accumulator
- K-bus (literal or masking information from micro-program memory)

Scratchpad Registers

- Contains 11 registers (R_0-R_9, T)
- Scratchpad register outputs are multiplexed to the ALU via the A multiplexer
- Used to store intermediate results from arithmetic/logic operations
- Can be used as program counter

Arithmetic/Logic Unit (ALU)

The ALU performs the arithmetic and logic operations of the CPE.

Arithmetic operations are:
- 2's complement addition
- Incrementing
- Decrementing
- Shift left
- Shift right

Logical operations are:
- Transfer
- AND
- Inclusive-OR
- Exclusive-NOR
- Logic complement

ALU operation results are then stored in the accumulator and/or scratchpad registers. For easy expansion to larger arrays, carry look-ahead outputs (X and Y) and cascading shift inputs (LI, RO) are provided.

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Accumulator

- Stores results from ALU operations
- The output of accumulator is multiplexed into ALU via the A and B multiplexer as one of the operands

Input Buses

M-bus: Data bus from main memory
- Accepts 2 bits of data from main memory into CPE
- Is multiplexed into the ALU via the A multiplexer

I-bus: Data bus from input/output devices
- Accepts 2 bits of data from external input/output devices into CPE
- Is multiplexed into the ALU via the B multiplexer

K-bus: A special feature of the N3002 CPE
- During arithmetic operations, the K-bus can be used to **mask** portions of the field being operated on
- Select or remove accumulator from operation by placing K-bus in all "1" or all "0" state respectively
- During non-arithmetic operation, the carry circuit can be used in conjunction with the K-bus for word-wise-OR operation for bit testing
- Supply literal or constant data to CPE

Output Buses

A-bus and Memory Address Register
- Main memory address is stored in the memory address register (MAR)
- Main memory is addressed via the A-bus
- MAR and A-bus may also be used to generate device address when executing I/OO instruc-instructions
- A-bus has Tri-State outputs

D-bus: Data bus from CPE to main memory or to I/O devices
- Sends buffered accumulator outputs to main memory or the external I/O devices
- D-bus has Tri-State outputs

FUNCTION DESCRIPTION

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
0	I	XX	—	$R_n + (AC \wedge K) + CI \rightarrow R_n, AC$	**Logically AND AC with the K-bus.** Add the result to R_n and carry input (CI). Deposit the sum in AC and R_n.
		OO	ILR	$R_n + CI \rightarrow R_n, AC$	Conditionally increment R_n and load the result in AC. Used to load AC from R_n or to increment R_n and load a copy of the result in AC.
		11	ALR	$AC + R_n + CI \rightarrow R_n, AC$	Add AC and CI to R_n and load the result in AC. Used to add AC to a register. If R_n is AC, then AC is shifted left one bit position.
0	II	XX	—	$M + (AC \wedge K) + CI \rightarrow AT$	**Logically AND AC with the K-bus.** Add the result to CI and the M-bus. Deposit the sum in AC or T.
		OO	ACM	$M + CI \rightarrow AT$	Add CI to M-bus. Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.
		11	AMA	$M + AC + CI \rightarrow AT$	Add the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register.
0	III	XX	—	$AT_L \wedge (\overline{I_L \wedge K_L}) \rightarrow RO$ $LI \vee [(I_H \wedge K_H) \wedge AT_H] \rightarrow AT_H$ $[AT_L \wedge (I_L \wedge K_L)]$ $[AT_H \vee (I_H \wedge K_H)] \rightarrow AT_L$	None
		OO	SRA	$AT_L \rightarrow RO$ $AT_H \rightarrow AT_L$ $L_I \rightarrow AT_H$	Shift AC or T, as specified, right one bit position. Place the previous low order bit value on RO and fill the high order bit from the data on LI. Used to shift or rotate AC or T right one bit.
1	I	XX	—	$K \vee R_n \rightarrow MAR$ $R_n + K + CI \rightarrow R_n$	**Logically OR R_n with the K-bus.** Deposit the result in MAR. Add the K-bus to Rn and CI. Deposit the result in R_n.
		OO	LMI	$Rn \rightarrow MAR,\ Rn + CI \rightarrow Rn$	Load MAR from R_n. Conditionally increment R_n. Used to maintain a macro-instruction program counter.
		11	DSM	$11 \rightarrow MAR,\ Rn - 1 + CI \rightarrow Rn$	Set MAR to all ones. Conditionally decrement R_n by one. Used to force MAR to its highest address and to decrement Rn.
1	II	XX	—	$KVM \rightarrow MAR$ $M + K + CI \rightarrow AT$	**Logically OR the M-bus with the K-Bus.** Deposit the result in MAR. Add the K-bus to the M-bus and CI. Deposit the sum in AC or T.
		OO	LMM	$M \rightarrow MAR,\ M + CI \rightarrow AT$	Load MAR from the M-bus. Add CI to the M-bus. Deposit the result in AC or T. Used to load the address register with memory data for macro-instructions using indirect addressing.
		11	LDM	$11 \rightarrow MAR$ $M - 1 + CI \rightarrow AT$	Set MAR to all ones. Subtract one from the M-bus. Add CI to the difference and deposit the result in AC or T, as specified. Used to load decremented memory data in AC or T.

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FUNCTION DESCRIPTION (Cont'd)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
1	III	XX	—	$(\overline{AT} \vee K) + (AT \wedge K) + CI \rightarrow AT$	**Logically OR the K-bus with the complement of AC or T, as specified.** Add the result to the logical AND of specified register with the K-bus. Add the sum to CI. Deposit the result in the specified register.
		OO	CIA	$\overline{AT} + CI \rightarrow AT$	Add CI to the complement of AC or T, as specified. Deposit the result in the specified register. Used to form the 1's or 2's complement of AC or T.
		11	DCA	$\overline{AT} - 1 + CI \rightarrow AT$	Subtract one from AC or T, as specified. Add CI to the difference and deposit the sum in the specified register. Used to decrement AC or T.
2	I	XX	—	$(AC \wedge K) - 1 + CI \rightarrow R_n$	**Logically AND the K-bus with AC.** Subtract one from the result and add the difference to CI. Deposit the sum in R_n.
		OO	CSR	$CI - 1 \rightarrow R_n$ (See Note 1)	Subtract one from CI and deposit the difference in Rn. Used to conditionally clear or set R_n to all 0's or 1's, respectively.
		11	SDR	$AC - 1 + CI \rightarrow R_n$ (See Note 1)	Subtract one from AC and add the difference to CI. Deposit the sum in R_n. Used to store AC in R_n or to store the decremented value of AC in R_n.
2	II	XX	—	$(AC \wedge K) - 1 + CI \rightarrow AT$ (See Note 1)	**Logically AND the K-bus with AC.** Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.
		OO	CSA	$CI - 1 \rightarrow AT$ (See Note 1)	Subtract one from CI and deposit the difference in AC or T. Used to conditionally clear or set AC or T.
		11	SDA	$AC - 1 + CI \rightarrow AT$ (See Note 1)	Subtract one from AC and add the difference to CI. Deposit the sum in AC or T. Used to store AC in T, or decrement AC, or store the decremented value of AC in T.
2	III	XX	—	$(I \wedge K) - 1 + CI \rightarrow AT$ (See Note 1)	**Logically AND the data of the K-bus with the data on the I-bus.** Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.
		OO	CSA	$CI - 1 \rightarrow AT$	Subtract one from CI and deposit the difference in AC or T. Used to conditionally clear or set AC or T.
		11	LDI	$I - 1 + CI \rightarrow AT$	Subtract one from the data on the I-bus and add the difference to CI. Deposit the sum in AC or T, as specified. Used to load input bus data or decremented input bus data in the specified register.
3	I	XX	—	$R_n + (AC \wedge K) + CI \rightarrow R_n$	**Logically AND AC with the K-bus.** Add R_n and CI to the result. Deposit the sum in R_n.
		OO	INR	$R_n + CI \rightarrow R_n$	Add CI to R_n and deposit the sum in R_n. Used to increment R_n.
		11	ADR	$AC + R_n + CI \rightarrow R_n$	Add AC to R_n. Add the result to CI and deposit the sum in R_n. Used to add the accumulator to a register or to add the incremented value of the accumulator to a register.
3	II	XX	—	$M + (AC \wedge K) + CI \rightarrow AT$	**Logically AND AC with the K-bus.** Add the result to CI and the M-bus. Deposit the sum in AC or T.
		OO	ACM	$M + CI \rightarrow AT$	Add CI to M-bus. Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.
		11	AMA	$M + AC + CI \rightarrow AT$	Add the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register.

NOTE

1. 2's complement arithmetic adds 111 . . . 11 to perform subtraction of 000 . . . 01.

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FUNCTION DESCRIPTION (Cont'd)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
3	III	XX	—	AT + (I ∧ K) + CI → AT	**Logically AND the K-bus with the I-bus.** Add CI and the contents of AC or T, as specified, to the result. Deposit the sum in the specified register.
		OO	INA	AT + CI → AT	Conditionally increment AC or T. Used to increment AC or T.
		11	AIA	I + AT + CI → AT	Add the I-bus to AC or T. Add CI to the result and deposit the sum in the specified register. Used to add input data or incremented input data to the specified register.
4	I	XX	—	CI ∨ (R_n ∧ AC ∧ K) → CO R_n ∧ (AC ∧ K) → R_n	**Logically AND the K-bus with AC.** Logically AND the result with the contents of R_n. Deposit the final result in R_n. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR of the carry output (CO) line.
		OO	CLR	CI → CO, O → R_n	Clear R_n to all O's. Force CO to CI. Used to clear a register and force CO to CI.
		11	ANR	CI ∨ (R_n ∧ AC) → CO R_n ∧ AC → R_n	Logically AND AC with R_n. Deposit the result in R_n. Force CO to one if the result is non-zero. Used to AND the accumulator with a register and test for a zero result.
4	II	XX	—	CI ∨ (M ∧ AC ∧ K) → CO M ∧ (AC ∧ K) → AT	**Logically AND the K-bus with AC.** Logically AND the result with the M-bus. Deposit the final result in AC or T. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on CO.
		OO	CLA	CI → CO, O → AT	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	ANM	CI ∨ (M ∧ AC) → CO M ∧ AC → AT	Logically AND the M-bus with AC. Deposit the result in AC or T. Force CO to one if the result is non-zero. Used to AND M-bus data to the accumulator and test for a zero result.
4	III	XX	—	CI ∨ (AT ∧ 1 ∧ K) → CO AT ∧ (I ∧ K) → AT	**Logically AND the I-bus with the K-bus.** Logically AND the result with AC or T. Deposit the final result in the specified register. Logically OR CI with the word-wise OR of the final result. Place the value of the carry OR on CO.
		OO	CLA	CI → CO, O → AT	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	ANI	CI ∨ (AT ∧ I) → CO AT ∧ 1 → AT	Logically AND the I-bus with AC or T, as specified. Deposit the result in the specified register. Force CO to one if the result is non-zero. Used to AND the I-bus to the accumulator and test for a zero result.
5	I	XX	—	CI ∨ (R_n ∧ K) → CO K ∧ R_n → R_n	**Logically AND the K-bus with R_n.** Deposit the result in Rn. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLR	CI → CO, O → R_n	Clear Rn to all O's. Force CO to CI. Used to clear a register and force CO to CI.
		11	TZR	CI ∨ R_n → CO R_n → R_n	Force CO to one if Rn is non-zero. Used to test a register for zero. Also used to AND K-bus data with a register for masking and, optionally, testing for a zero result.
5	II	XX	—	CI ∨ (M ∧ K) → CO K ∧ M → AT	**Logically AND the K-bus with the M-bus.** Deposit the result in AC or T, as specified. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLA	CI → CO, O → AT	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	LTM	CI ∨ M → CO M → AT	Load AC or T, as specified, from the M-bus. Force CO to one if the result is non-zero. Used to load the specified register from memory and test for a zero result. Also used to AND the K-bus with the M-bus for masking and, optionally, testing for a zero result.

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FUNCTION DESCRIPTION (Cont'd)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
5	III	XX	—	CI ∨ (AT ∧ K) → CO K ∧ AT → AT	Logically AND the K-bus with AC or T, as specified. Deposit the result in the specified register. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLA	CI → CO, O → AT	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	TZA	CI ∨ AT → CO AT → AT	Force CO to one if AC or T, as specified, is non-zero. Used to test the specified register for zero. Also used to AND the K-bus to the specified register for masking and, optionally, testing for a zero result.
6	I	XX	—	CI ∨ (AC ∧ K) → CO R_n ∨ (AC ∧ K) → R_n	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus. Place the result of the carry OR on CO. Logically OR R_n with the logical AND of AC and the K-bus. Deposit the result in R_n.
		OO	NOP	CI → CO, R_n → R_n	Force CO to CI. Used as a null operation or to force CO to CI.
		11	ORR	CI ∨ AC → CO R_n ∨ AC → R_n	Force CO to one if AC is non-zero. Logically OR AC with R_n. Deposit the result in R_n. Used to OR the accumulator to a register and, optionally, test the previous accumulator value for zero.
6	II	XX	—	CI ∨ (AC ∧ K) → CO M ∨ (AC ∧ K) → AT	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus. Place the carry OR on CO. Logically OR the M-bus, with the logical AND of AC and the K-bus. Deposit the final result in AC or T.
		OO	LMF	CI → CO, M → AT	Load AC or T, as specified, from the M-bus. Force CO to CI. Used to load the specified register with memory data and force CO to CI.
		11	ORM	CI ∨ AC → CO M ∨ AC → AT	Force CO to one if AC is non-zero. Logically OR the M-bus with AC. Deposit the result in AC or T, as specified. Used to OR M-bus with the AC and, optionally, test the previous value of AC for zero.
6	III	XX	—	CI ∨ (I ∧ K) → CO AT ∨ (I ∧ I) → AT	Logical OR CI with the word-wise OR of the logical AND of the I-bus and the K-bus. Place the carry OR on CO. Logically AND the K-bus with the I-bus. Logically OR the result with AC or T, as specified. Deposit the final result in the specified register.
		OO	NOP	CI → CO, AT → AT	Force CO to CI. Used as a null operation or to force CO to CI.
		11	ORI	CI ∨ I → CO I ∨ AT → AT	Force CO to one if the data on the I-bus is non-zero. Logically OR the I-bus to AC or T, as specified. Deposit the result in the specified register. Used to OR I-bus data with the specified register and, optionally, test the I-bus data for zero.
7	I	XX	—	CI ∨ (R_n ∧ AC ∧ K) → CO R_n $\overline{\oplus}$ (AC ∧ K) → R_n	Logically OR CI with the word-wise OR of the logical AND of R_n and AC and the K-bus. Place the carry OR on CO. Logically AND the K-bus with AC. Exclusive-NOR the result with R_n. Deposit the final result in R_n.
		OO	CMR	CI → CO, Rn → Rn	Complement the contents of R_n. Force CO to CI.
		11	XNR	CI ∨ (R_n ∧ AC) → CO R_n $\overline{\oplus}$ AC → R_n	Force CO to one if the logical AND of AC and Rn is non-zero. Exclusive-NOR AC with R_n. Deposit the result in R_n. Used to exclusive-NOR the accumulator with a register.

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FUNCTION DESCRIPTION (Cont'd)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
7	II	XX	—	CI ∨ (M ∧ AC ∧ K) → CO M ⊕̄ (AC ∧ K) → AT	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus and M-bus. Place the carry OR on CO. Logically AND the K-bus with AC. Exclusive NOR the result with the M-bus. Deposit the final result in AC or T.
		OO	LCM	CI → CO, $\overline{M}$ → AT	Load the complement of the M-bus into AC or T, as specified. Force CO to CI.
		11	XNM	CI ∨ (M ∧ AC) → CO M ⊕̄ AC → AT	Force CO to one if the logical AND of AC and the M-bus is non-zero. Exclusive-NOR AC with the M-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR memory data with the accumulator.
7	III	XX	—	CI ∨ (AT ∧ I ∧ K) → CO AT ⊕̄ (I K) → AT	Logically OR CI with the word-wise OR of the logical AND of the specified register and the I-bus and K-bus. Place the carry OR on CO. Logically AND the K-bus with the I-bus. Exclusive-NOR the result with AC or T, as specified. Deposit the final result in the specified register.
		OO	CMA	CI → CO $\overline{AT}$ → AT	Complement AC or T, as specified. Force CO to CI.
		11	XNI	CI ∨ (AT ∧ I) → CO I ⊕̄ AT → AT	Force CO to one if the logical AND of the specified register and the I-bus is non-zero. Exclusive-NOR AC with the I-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR input data with the accumulator.

FUNCTION DESCRIPTION KEY

SYMBOL	MEANING
I,K,M	Data on the I, K, and M buses, respectively
CI,LI	Data on the carry input and left input, respectively
CO,RO	Data on the carry output and right output, respectively
Rn	Contents of register n including T and AC (R-Group I)
AC	Contents of the accumulator
AT	Contents of AC or T, as specified
MAR	Contents of the memory address register
L,H	As subscripts, designate low and high order bit, respectively
+	2's complement addition
-	2's complement subtraction
∧	Logical AND
∨	Logical OR
⊕	Exclusive-NOR
→	Deposit into

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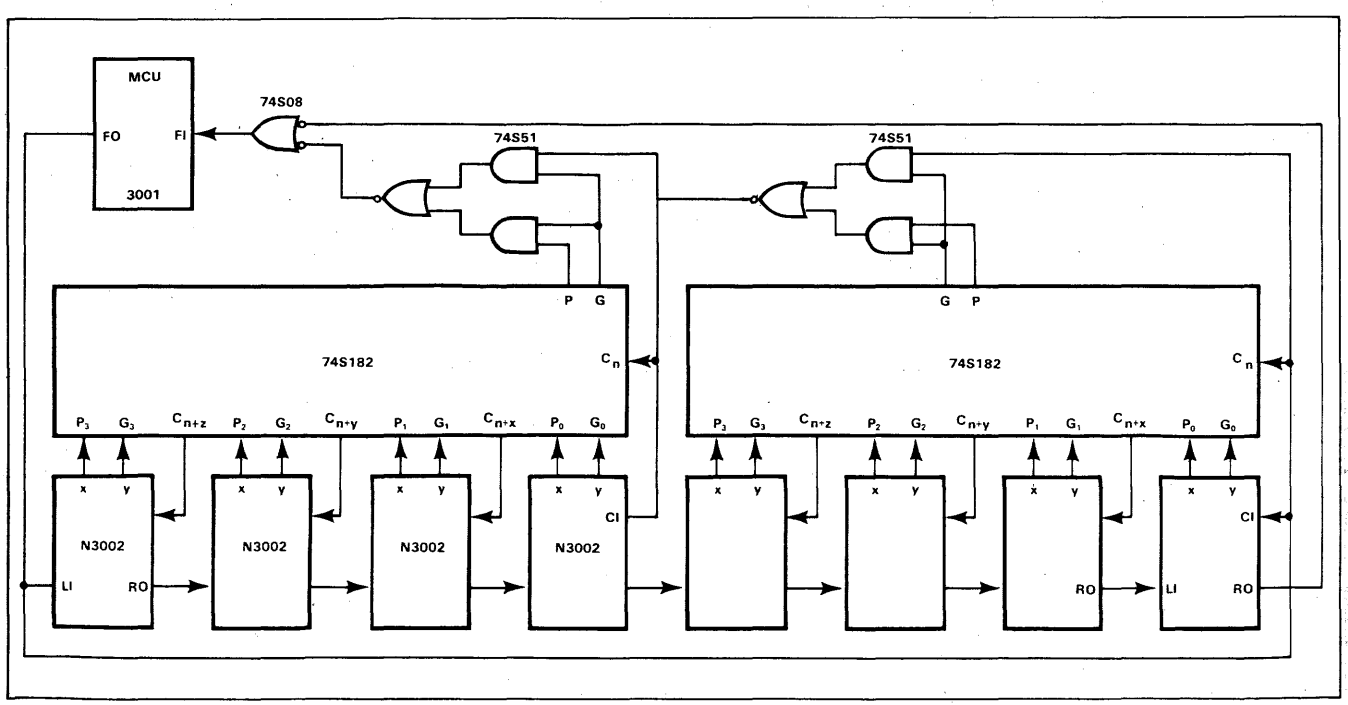
AC ELECTRICAL CHARACTERISTICS

N3001 = T_A = 0°C to +70°C, V_{CC} = 5V ± 5%
S3001 = T_A = -55°C to +125°C, V_{CC} = 5V ± 10%

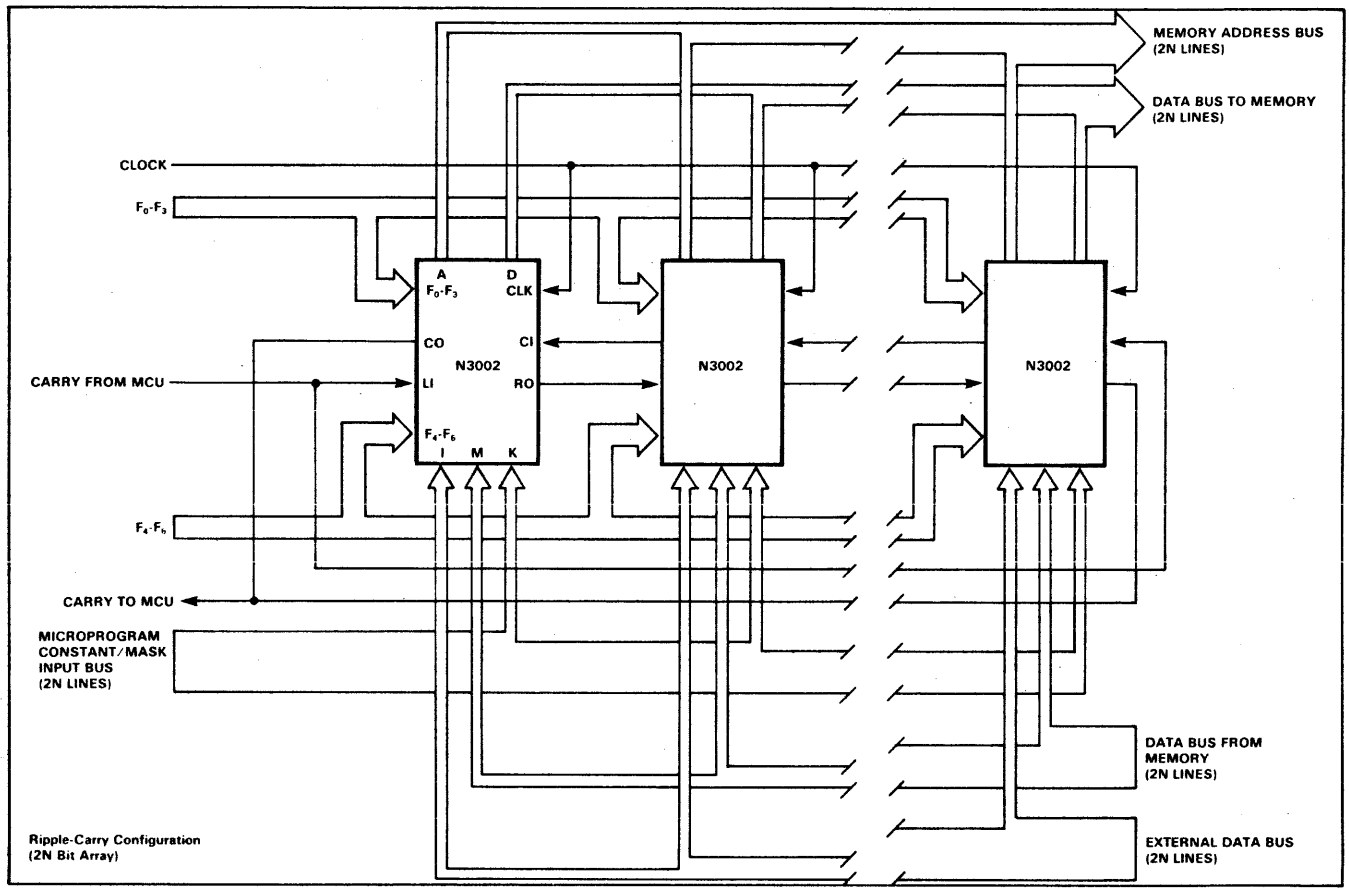
PARAMETER	N3002			S3002			UNIT
	Min	Typ*	Max	Min	Typ*	Max	
tCY Clock Cycle Time	70	45		120	45		ns
tWP Clock Pulse Width	17	10		42	10		ns
tFS Function Input Set-Up Time (F_0 through F_6)	48	-23 - 35		70	-23 - 35		ns
Data Set-Up Time:							
tDS I_0, I_1, M_0, M_1, K_0, K_1	40	12 - 29		60	12 - 29		ns
tSS LI, CI	21	0 - 7		30	0 - 7		ns
Data and Function Hold Time:							
tFH F_0 through F_6	4	0		5	0		ns
tDH 1_0, I_1, M_0, M_1, K_0, K_1	4	-28 - -11		5	-28 - -11		ns
tSH LI, CI	12	-7 - 0		15	-7 - 0		ns
Propagation Delay to X, Y, RO from:							
tXF Any Function Input		28	52		28	65	ns
tXD Any Data Input		16 - 20	33		16 - 20	65	ns
tXT Trailing Edge of CLK		33	48		33	75	ns
tXL Leading Edge of CLK	13	18 - 40	70	13	18 - 40	90	ns
Propagation Delay to CO from:							
tCL Leading Edge of CLK	16	24 - 44	70		24 - 44	90	ns
tCT Trailing Edge of CLK		30 - 40	56		30 - 40	100	ns
tCF Any Function Input		25 - 35	52		25 - 35	75	ns
tCD Any Data Input		17 - 23	55		17 - 23	65	ns
tCC CI (Ripple Carry)		9 - 13	20		9 - 13	30	ns
Propagation Delay to A_0, A_1, D_0, D_1 from:							
tDL Leading Edge of CLK		17 - 25	40		17 - 25	75	ns
tDE Enable Input ED, EA		10 - 12	20		10 - 12	35	ns

* NOTE
Typical values are for T_A = 25°C and typical supply voltage.

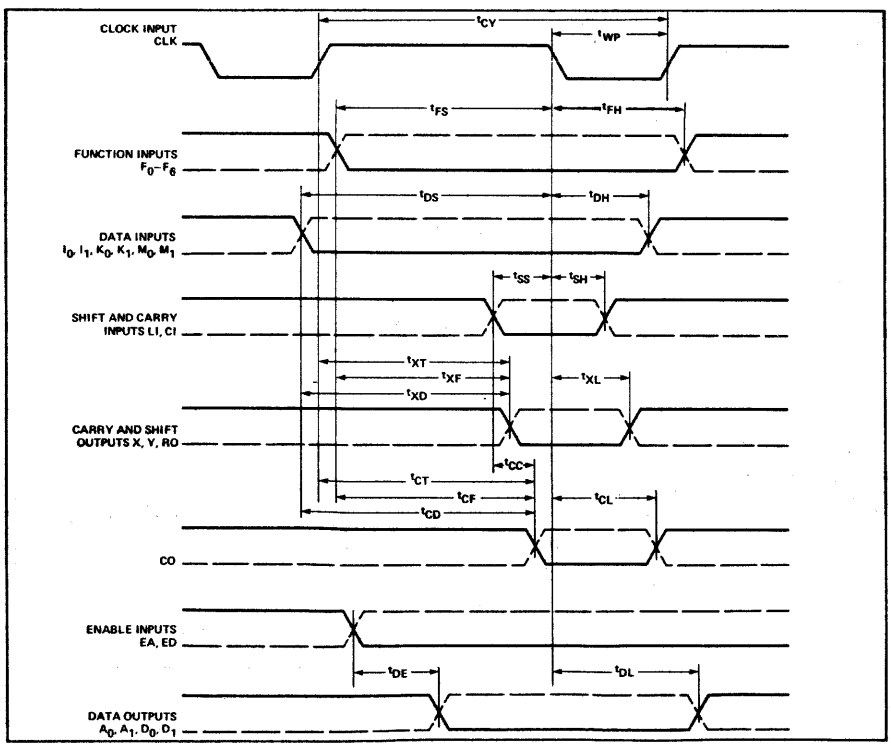
CARRY LOOK-AHEAD CONFIGURATION



TYPICAL CONFIGURATIONS



VOLTAGE WAVEFORMS



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PRELIMINARY SPECIFICATION 8X02-I,XL

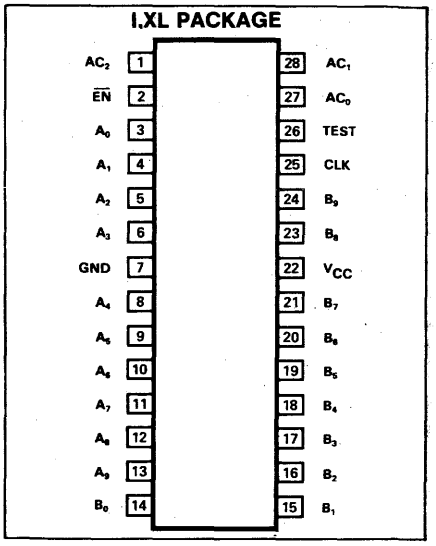
DESCRIPTION

The Signetics 8X02 is a low power Schottky LSI device intended for use in high performance microprogrammed systems to control the fetch sequence of microinstructions. When combined with standard ROM or PROM, the 8X02 forms a powerful microprogrammed control section for computers, controllers, or sequential logic.

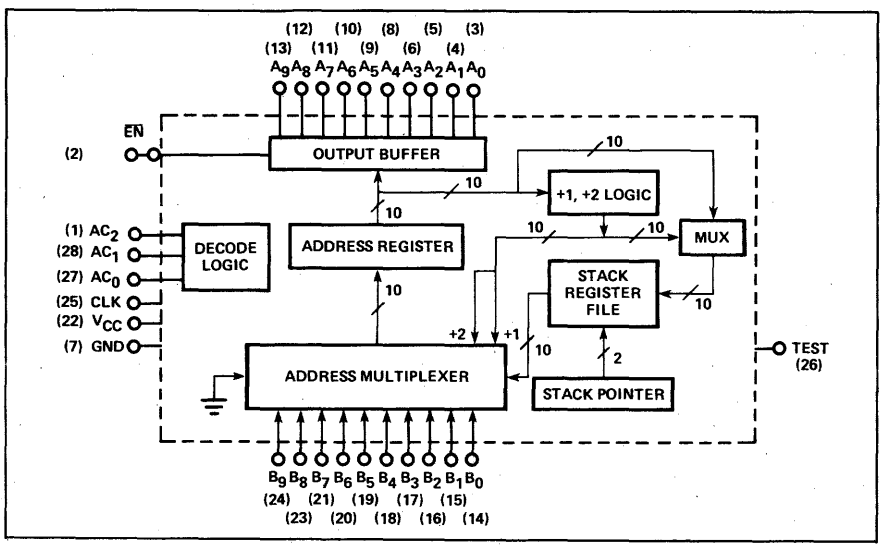
FEATURES

- **Low power Schottky process**
- **1024 microinstruction addressability**
- **N-way branch**
- **4-level stack register file (LIFO type)**
- **Automatic push/pop stack operation**
- **"Test and skip" operation on test input line**
- **3-bit command code**
- **Tri-state buffered outputs**
- **Auto-reset to address 0 during power-up**
- **Conditional branching, pop stack, and push stack**

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
5-6 8-13	A_0-A_9	Microprogram Address outputs	Three-state Active high
1,28,27	AC_0-AC_2	Next Address Control Function inputs All addressing control functions are selected by these command lines.	Active high
14-21 23-24	B_0-B_9	Branch Address inputs Determines the next address of an N-way branch when used with the BRANCH TO SUBROUTINE (BSR) or BRANCH ON TEST (BRT) command.	Active high
2	$\overline{EN}$	Enable input When in the low state, the Microprogram Address outputs are enabled.	Active low
25	CLK	Clock Input—High to Low transition for stack operations, Low to High transition for address modification.	⊓
26	TEST	Test input Used in conjunction with four NEXT ADDRESS CONTROL FUNCTION commands to effect conditional skips, branches, and stack operations.	Active high
7	GND	Ground	
22	V_{CC}	+5 Volt supply	

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FUNCTIONAL DESCRIPTION

The Signetics 8X02 Control Store Sequencer is an LSI device using low power Schottky technology and is intended for use in high performance microprogrammed applications. When used alone, the 8X02 is capable of addressing up to 1K words of microprogram. This may be expanded to any microprogram size by conventional paging techniques.

The Address Register consists of 10 D-type, edge-triggered flip-flops with a common clock. A new address is entered into the Address Register on the low-to-high transition of the clock. The next address to be entered into the Address Register is supplied via the Address Multiplexer.

The Address Multiplexer is a 5-input device that is used to select either the branch input, +1 adder, +2 adder, stack register file, or ground (all zeros) as the source of the next microinstruction address. The proper multiplexer channel is automatically selected via the Decode Logic according to the Address Control Function Input and Test Input line.

The +1, +2 logic is used to increment the present contents of the Address Register by 1 or 2, depending on the function input command. Thus, the next address to the Control Store ROM/PROM may be either the current address plus 1 (N+1) or the current address plus 2 (N+2). If the same Microprogram Address is to be used on successive occasions, the clock to the 8X02 must simply be disabled; therefore, no new address is loaded into the Address Register.

The Stack File Register is used to provide a return address linkage whenever a subroutine or loop is executed. The 4X10 stack operates in a last-in, first-out (LIFO) mode, with the stack pointer always pointing to the next address to be read. Operation of the stack pointer is automatically controlled by the Address Control Function Inputs. Since the stack is 4 words deep, up to 4 loops and/or subroutines may be nested.

The branch input is a 10-bit field of direct inputs to the multiplexer which can be selected as the next control store address. Using the appropriate branch command, an N-way branch is possible where N is the address of any microinstruction within the 1024 word microcode page. Likewise, the RESET command is a special case of an N-way branch in which the multiplexer selects an all zeros input, forcing the next microinstruction address to be zero.

The Test Input line is used in conjunction with the conditional execution of 4 Address Control Function commands. When the Test Input is false (low), the sequencer simply increments to the next address (N+1). When it is true (high), the sequencer executes a branch as defined by the input command, thereby transferring control to another portion of the microprogram.

All Address Output lines of the 8X02 are three-state buffered outputs with a common enable line ($\overline{EN}$). When the Enable line is high, all outputs are placed in a high-impedance state, and external access to the control store ROM/PROM is possible. This allows a preprogrammed set of microinstructions to be executed from external or built-in test equipment (BITE), vectored interrupts, and Writable Control Store if implemented.

NEXT ADDRESS CONTROL FUNCTION TABLE

MNEMONIC	DESCRIPTION	FUNCTION AC_2 1 0	TEST	NEXT ADDRESS	STACK	STACK POINTER
TSK	Test and skip	0 0 0	False True	Current + 1 Current + 2	N.C. N.C.	N.C. N.C.
INC	Increment	0 0 1	X	Current + 1	N.C.	N.C.
BLT	Branch to loop if test input true	0 1 0	False True	Current + 1 Stack reg file	X POP (read)	Decr Decr
POP	POP stack	0 1 1	X	Stack reg file	POP (read)	Decr
BSR	Branch to subroutine if test input true	1 0 0	False True	Current + 1 Branch address	N.C. PUSH (Curr + 1)	N.C. Incr
PLP	Push for looping	1 0 1	X	Current + 1	PUSH (Curr Addr)	Incr
BRT	Branch if test input true	1 1 0	False True	Current + 1 Branch address	N.C. N.C.	N.C. N.C.
RST	Set microprogram address output to zero	1 1 1	X	All O's	N.C.	N.C.

X = Don't care
N.C. = No change

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FUNCTIONAL DESCRIPTION

The following is a description of each of the eight Next Address Control Functions (AC_2-AC_0)

MNEMONIC	FUNCTION DESCRIPTION
TSK	AC_{2-0} = 000: TEST AND SKIP Perform test on Test Input Line. If test is False (Low): Next Address = Current Address + 1 Stack Pointer unchanged If test is True (High): Next Address = Current Address + 2 (i.e. Skip next microinstruction) Stack Pointer unchanged
INC	AC_{2-0} = 001: INCREMENT Next Address = Current Address + 1 Stack Pointer unchanged
BLT	AC_{2-0} = -010: BRANCH TO LOOP IF TEST CONDITION TRUE. Perform test on Test Input Line. If test is False (Low): Next Address = Current Address + 1 Stack Pointer decremented by 1 If test is True (High): Next Address = Address from Stack Register File (POP) Stack Pointer decremented by 1
POP	AC_{2-0} = 011: POP STACK Next Address = Address from Stack Register File (POP) Stack Pointer decremented by 1
BSR	AC_{2-0} = 100: BRANCH TO SUBROUTINE IF TEST CONDITION TRUE. Perform test on Test Input Line. If test is False (Low): Next Address = Current Address + 1 Stack Pointer unchanged If test is True (High): Next Address = Branch Address Input (B_{0-9}) Stack Pointer incremented by 1 PUSH (write) Current Address + 1 → Stack Register File
PLP	AC_{2-0} = 101: PUSH FOR LOOPING Next Address = Current Address + 1 Stack Pointer incremented by 1 PUSH (write) Current Address → Stack Register File
BRT	AC_{2-0} = 110: BRANCH ON TEST CONDITION TRUE Perform test on Test Input Line. If test is False (Low): Next Address = Current Address + 1 Stack Pointer unchanged If test is True (High): Next Address = Branch Address Input (B_{0-9}) Stack Pointer unchanged
RST	AC_{2-0} = 111: RESET TO ZERO Next Address = 0 Stack Pointer unchanged

ABSOLUTE MAXIMUM RATINGS

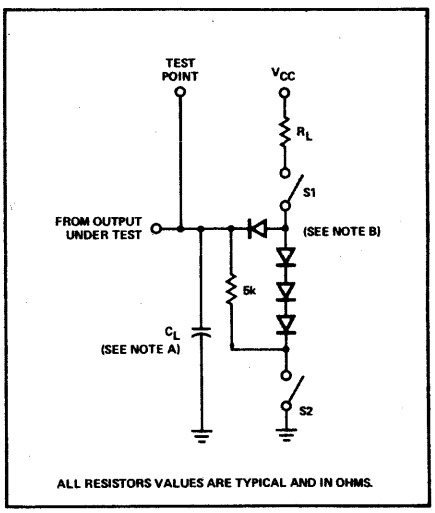
PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-State output voltage	+5.5	Vdc
T_A	Operating temperature range	0° to +70°	°C
T_{STG}	Storage temperature range	-65° to +150°	°C

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, 4.75 ≤ V_{CC} ≤ 5.25V

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[1]	Max	
V_{IH}	High level input voltage		2			V
V_{IL}	Low level input voltage				0.8	V
V_I	Input clamp voltage	V_{CC} = 4.75V, I_I = -18mA			-1.5	V
V_{OH}	High level output voltage	V_{CC} = 4.75V, I_{OH} = -2.6mA	2.4			V
V_{OL}	Low level output voltage	V_{CC} = 4.75V, I_{OL} = 8mA			0.5	V
I_I	Input current at maximum Input voltage	V_{CC} = 5.25V, V_I = 5.5V			100	μA
I_{IH}	High level input current	V_{CC} = 5.25V, V_I = 2.7V				
	AC_2-AC_0, $\overline{EN}$, TEST				40	μA
	B_9-B_0				20	μA
	CLK				60	μA
I_{IL}	Low level input current	V_{CC} = 5.25V, V_I = 0.4V				
	AC_2-AC_0, $\overline{EN}$, TEST				-0.72	mA
	B_9-B_0				-0.36	mA
	CLK				-1.08	mA
I_{OS}	Short-circuit output current	V_{CC} = 5.25V	-15		-100	mA
I_{OZH}	High-Z state output current	V_{OUT} = 2.7V			20	μA
I_{OZL}	High-Z state output current	V_{OUT} = 0.4V			-20	μA
I_{CC}	Supply current	V_{CC} = 5.25V		165	200	mA

NOTE
1. All typical values are at V_{CC} = 5V, T_A = 25°C.

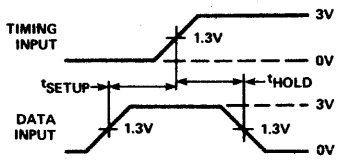
TEST LOAD CIRCUIT



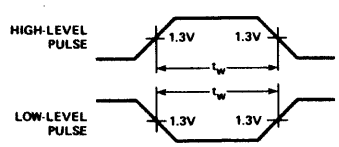
NOTES
A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. R_L = 2k, C = 15pF.

VOLTAGE WAVEFORMS

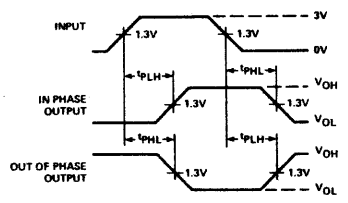
SETUP AND HOLD TIMES



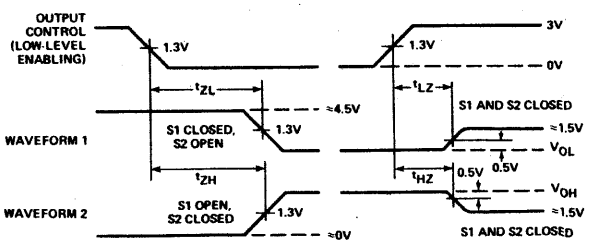
PULSE WIDTHS



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES THREE-STATE OUTPUTS



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AC ELECTRICAL CHARACTERISTICS T_A = 0° -70°C, V_{CC} = 5.0V ± 5%

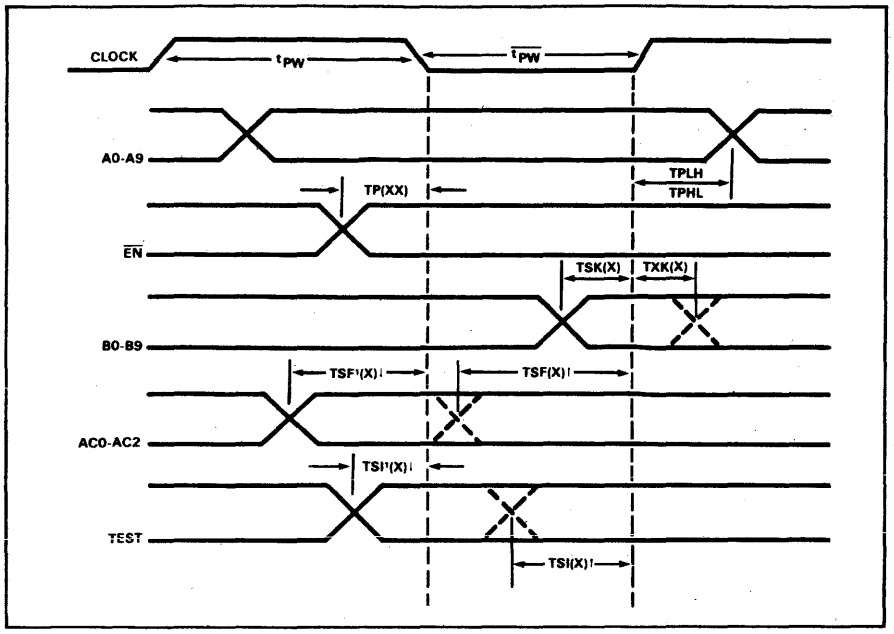
PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
t_{HI} (1)	Test			0	-10		ns
(0)				0	-24		
	Control and data input setup times with respect to CLK (↑) for stack related functions (BLT, POP, BSR, PLP) (2)						ns
t_{SF}[1] (1)	AC_0-AC_2			35	23		
(0)				35	22		
t_{SI}[1] (1)	Test			28	23		
(0)				28	22		
	Propagation delay	A_0-A_9	EN				ns
t_{PLZ}	Low to high Z				12	35	
t_{PHZ}	High to high Z				16	35	
t_{PZL}	High to low				14	25	
t_{PZH}	High Z to high				15	35	
	Propagation delay	A_0-A_9	Clock				
t_{PHL}	High to low				33	40	
t_{PLH}	Low to high				33	40	
	Clock pulse width						ns
t_{PW}	High			50	36		
$\overline{t}_{PW}$	Low			60	42		
	Control and data input setup times with respect to CLK (↑) for non-stack related functions (TSK, INC, BRT, RST)						ns
t_{SF} (1)	AC_0-AC_2			90	70		
(0)				90	70		
t_{SK} (1)	B_0-B_9[2]			27	22		
(0)				29	24		
t_{SI} (1)	Test			60	45		
(0)				60	45		
	Control and data input hold times with respect to CLK (↑)						ns
t_{HF} (1)	AC_0-AC_2			0	-7		
(0)				0	-12		
t_{HK} (1)	B_0-B_9[2]			0	-12		
(0)				0	-10		

NOTES

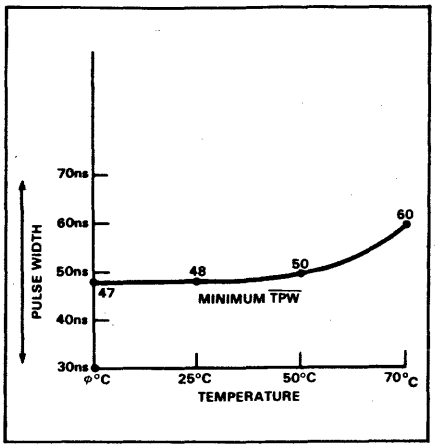
1. Typical values are to T_A = 25°C and V_{CC} = 5.0 volts
2. B_0-B_9 inputs are required to Clock (↑) only. See TSK (1) and TSK (0).

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TIMING WAVEFORM



PULSE WIDTH ($\overline{TPW}$) vs TEMPERATURE



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DESCRIPTION

The Signetics 8X300 Microcontroller is a monolithic, high-speed microprocessor implemented with bipolar Schottky technology. As the central processing unit, CPU, it allows 16-bit instructions to be fetched, decoded and executed in 250ns. A 250ns instruction cycle requires maximum memory access of 65ns, and maximum I/O device access of 35ns.

Microcontroller instructions operate on 8-bit, parallel data. Logic is distributed along the data path within the Microcontroller. Input data can be rotated and masked before being subject to an arithmetic or logical operation; and output data can be shifted and merged with the input data, before being output to external logic. This allows 1- to 8-bit I/O and data memory fields to be accessed and processed in a single instruction cycle.

PROGRAM STORAGE INTERFACE

Program Storage is typically connected to the A0-A12 (A12 is least significant bit) and I0-I15 signal lines. An address output on A0-A12 identifies one 16-bit instruction word in program storage. The instruction word is subsequently input on I0-I15 and defines the Microcontroller operations which are to follow.

The Signetics 82S115 PROM, or any TTL compatible memory, may be used for program storage.

I/O DEVICES INTERFACE

An 8-bit I/O bus, called the Interface Vector (IV) data bus, is used by the Microcontroller to communicate with 2 fields of I/O devices. The complementary $\overline{LB}$ and $\overline{RB}$ signals identify which field of the I/O devices is selected.

Both I/O data and I/O address information can be output on the IV bus. The SC and WC signals are typically used to distinguish between I/O data and I/O address information as follows:

SC	WC	
1	0	I/O address is being output on IV bus
0	1	I/O data is being output on IV bus
0	0	I/O data is expected on the IV, bus, as input to the Microcontroller
1	1	Not generated by the Microcontroller

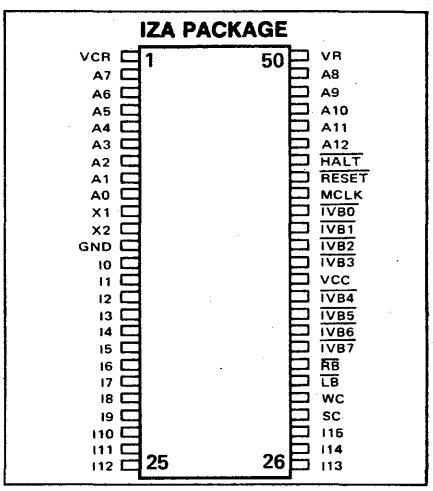
The Signetics 82SXXX series RAM, and the 8T32/33 may be attached to the IV bus.

FEATURES

- **185ns instruction decode and execute delay (with Signetics 8T32/33 I/O port)**
- **Eight 8-bit working registers**
- **Single instruction access to 1-bit, 2-bit, 3-bit or 8-bit field on I/O bus**
- **Separate instruction address, instruction, and I/O data buses**
- **On-chip oscillator**
- **Bipolar Schottky technology**
- **TTL inputs and outputs**
- **Tri-state output on I/O data bus**
- **+5 volt operation from 0° to 70°C**

PIN CONFIGURATION

IZA PACKAGE



PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
2-9, 45-49	A0-A12:	Instruction address lines. A high level equals "1." These outputs directly address up to 8192 words of program storage. A12 is least significant bit.	Active high
13-28	I0-I15:	Instruction lines. A high level equals "1." Receives instructions from Program Storage. I_{15} is least significant bit.	Active high
33-36, 38-41	$\overline{IVB0}$-$\overline{IVB7}$	Interface Vector (IV) Bus. A low level equals "1." Bidirectional tri-state lines to communicate with I/O devices. $\overline{IVB7}$ is least significant bit.	Three-state Active low
42	$\overline{MCLK}$:	Master Clock. Output to clock I/O devices, and/or provide synchronization for external logic	
30	WC:	Write Command. High level output indicates data is being output on the IV Bus.	Active high
29	SC:	Select Command. High level output indicates that an address is being output on the IV Bus.	Active high
31	$\overline{LB}$:	Left Bank. Low level output to enable one of two sets of I/O devices ($\overline{LB}$ is the complement of RB).	Active low
32	$\overline{RB}$:	Right Bank. Low level output to enable one of two sets of I/O devices ($\overline{RB}$ is the complement of $\overline{LB}$).	Active low
44	$\overline{HALT}$:	Low level is input to stop the Microcontroller.	Active low
43	$\overline{RESET}$:	Low level is input to initialize the Microcontroller.	Active low
10-11	X1, X2:	Inputs for an external frequency determining crystal. May also be interfaced to logic or test equipment.	
50	VR	Reference voltage to pass transistor.	
1	VCR	Regulated output voltage from pass transistor.	
37	V_{CC}:	5V power connection.	
12	GND:	Ground.	

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MICROCONTROLLER ARCHITECTURE

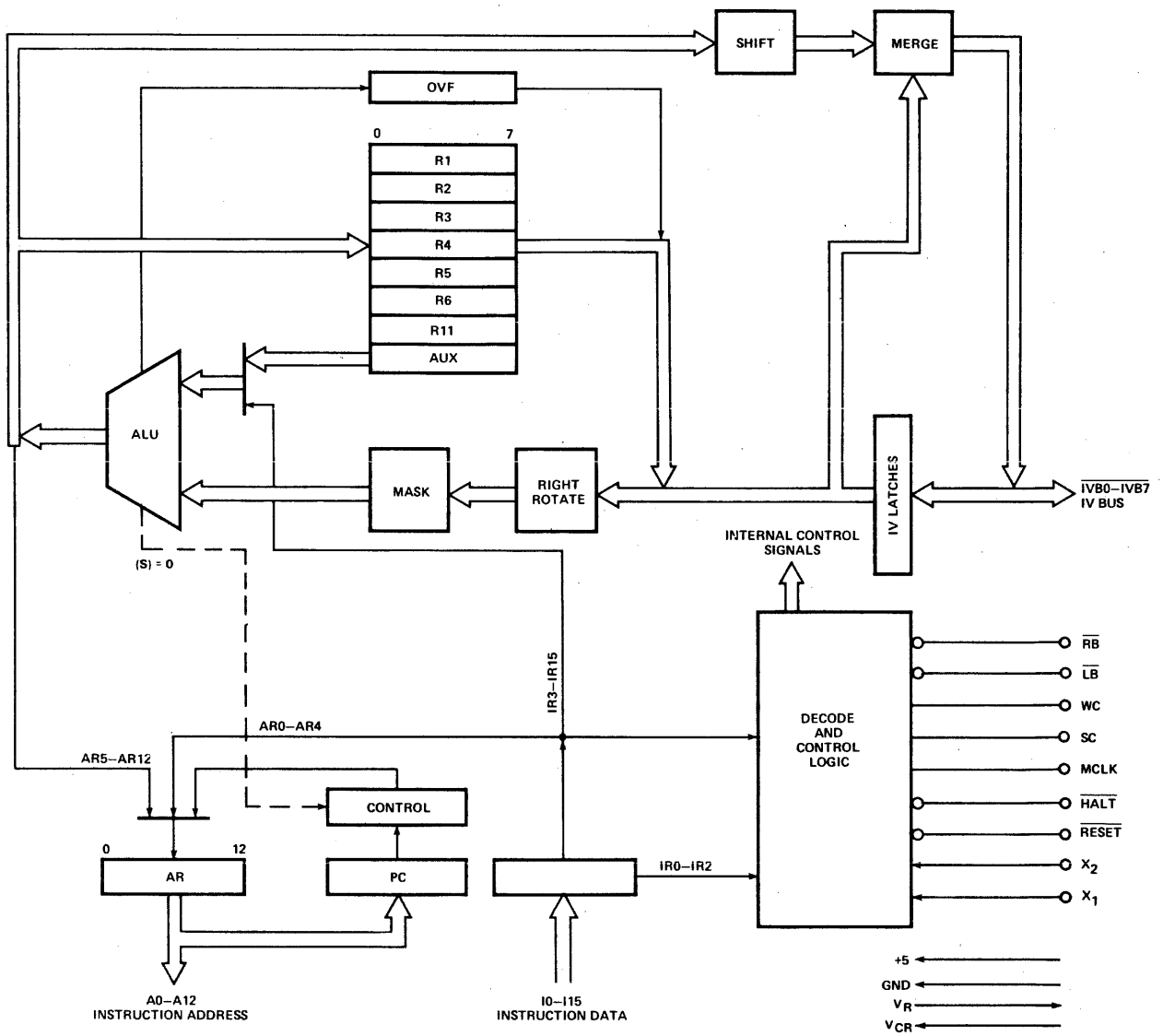


Figure 1

R1 — General working register
R2 — General working register
R3 — General working register
R4 — General working register
R5 — General working register
R6 — General working register
R11 — General working register
AUX — General working register. Contains second term for arithmetic or logical operations.

OVF — The least-significant bit of this register is used to reflect overflow status resulting from the most recent ADD operation (see Instruction Set Summary).

Instruction Register (IR)
— Holds the 16-bit instruction word currently being executed.

Program Counter (PC)
— Normally contains the address of the current instruction and is incremented to obtain the next instruction address.

Address Register (AR)
— A 13-bit register containing the address of the current instruction.

Table 1 INTERNAL REGISTERS

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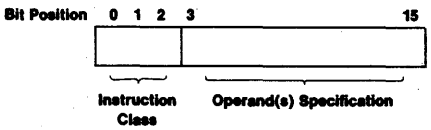
INSTRUCTION CYCLE

Each Microcontroller operation is executed in 1 instruction cycle, which may be as short as 250ns. The Microcontroller generates MCLK to synchronize external logic to the instruction cycle. Instruction cycles are subdivided into quarter cycles. MCLK is an output during the last quarter cycle.

During the third quarter cycle of an instruction, an address is output on A0-A12, identifying the location in program storage of the next instruction word. This instruction word defines the next instruction, which must be input on I0-I15 during the first quarter cycle of the next instruction cycle (see Table 2).

Instruction Set Summary

The 16-bit instruction word input on I0-I15 is decoded by the instruction decode logic to implement events that are to occur during the remainder of the instruction cycle. Generally the 16-bit instruction word is decoded as follows:



A detailed usage of the 13 "operand(s) specification" bits is given in following sections.

Three operation code bits allow for 8 instruction classes. The 8 instruction classes are summarized in Table 3. Each entry is referred to as an "instruction class" because the unique architecture of the Interpreter allows a number of powerful variations to be specified by the 13 operand(s) specification bits. A complete description of instruction formats and some instruction examples are provided in the Microprocessor Applications manual.

Data Processing

The Microcontroller architecture includes eight 8-bit working registers, an arithmetic logic unit (ALU), an overflow register, and the 8-bit IV Bus. Internal 8-bit data paths connect the registers and IV Bus to the ALU inputs, and the ALU output to the registers and IV Bus. Data processing logic is distributed along these internal 8-bit data paths. Rotate and mask logic precedes the ALU on the data entry path. Shift and merge logic follows the ALU on the data output path. All 4 sets of logic can operate on 8 data bits in a single instruction cycle (See Figure 1).

When less than 8 bits of data are specified for output to the IV bus by the ALU, the data field (shifted if necessary) is inserted into the prior contents of the IV bus latches. The IV bus latches contain data input at the start of an instruction. This data in the IV bus latches will be specified in the instruction as a) IV bus source data or b) data from an automatic read when the IV bus is specified as a destination. Therefore, IV bus bit positions outside an inserted bit field are unmodified.

Data Addressing

Sources and destinations of data are specified using a 5-bit octal number. The source and/or destination of data to be operated upon is specified in a single instruction word.

Referring to Figure 1, the Auxiliary register (address 00) is the implied source of the second argument for ADD, AND or XOR operations.

IVL and IVR are write-only registers used only as a destination. They have addresses and are treated as registers, but in reality they do not exist. When IVL is specified as a destination or the D field = $20\text{-}27_8$, then LB = 'low', RB = 'high' are generated; when IVR is specified as a destination or the D field = $30\text{-}37_8$, then RB = low, LB = 'high' are generated.

When IVL or IVR is specified as the destination in an instruction, SC is also activated and data is placed on the IV bus. If IVL or IVR is specified as a source of data, the source data is all zeroes.

TYPICAL SYSTEM CONFIGURATION

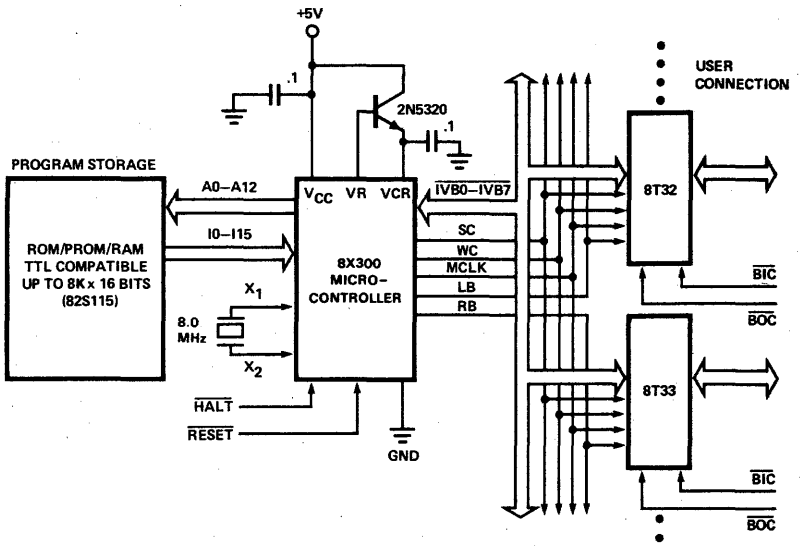


Figure 2

INSTRUCTION AND IV BUS DATA INPUT	DATA PROCESSING	ADDRESS AND IV BUS CHANGING	ADDRESS AND IV BUS DATA VALID MCLK=HIGH
← ¼ cycle →	← ¼ cycle →	← ¼ cycle →	← ¼ cycle →

Table 2 INSTRUCTION CYCLE

INSTRUCTION SEQUENCE CONTROL

The Address Register and Program Counter are used to generate addresses for accessing an instruction. The Address Register is used to form the instruction address, and in all but 3 instructions (XEC, NZT, and JMP) the address is copied into the Program Counter. The instruction address is formed in 1 of 3 ways:

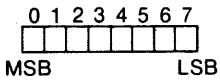
1. For all instructions but the JMP, XEC, and a satisfied NZT, the Program Counter is incremented by 1 and placed in the Address Register.
2. For the JMP instruction, the full 13-bit address field from the JMP instruction is placed into the Address Register and copied into the Program Counter.
3. For the XEC and NZT instructions, the high order 5- or 8-bits of the Program Counter are combined with 8- or 5-lower-order bits of ALU output (XEC or NZT) and placed in the Address Register. For the NZT instruction, it is also copied into the Program Counter.

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INSTRUCTION SET

The 8X300 Microcontroller has a repertoire of 8 instruction classes which allow the user to test input status lines, set or reset output control lines, and perform high speed input/output data transfers. All instructions are 16 bits in length and each is fetched, decoded and executed in 250ns.

Data is respresented as an 8-bit byte; bit positions are numbered from left to right, with the least significant bit in position 7.



Within the 8X300, all operations are performed on 8-bit bytes. Arithmetic operations use 8-bit, unsigned 2's complement arithmetic.

INSTRUCTION FORMATS

The general 8X300 instruction format is:

0 1 2	3 4 5 6 7 8 9 10 11 12 13 14 15
Op Code	Operand(s)

All instructions are specified by a 3-bit Operation (Op Code) field. The operand may consist of the following fields: Source (S) field, Destination (D) field, Rotate/Length (R/L) field, Immediate (I) field, or (Program Storage) Address (A) field.

The instructions are divided into 5 format types, based on the Op Code and the Operand(s), as shown in Figure 3.

OPERATION	FORMAT	RESULT	NOTES
MOVE	I,II	Content of data field specified by {S, R/L} replaces data in field specified by {D, R/L.}	If S and D both are registers, then R/L specifies a right rotate of the register specified by S.
ADD	I,II	Sum of AUX and data specified by {S, R/L} replaces data in field specified by {D, R/L}.	
AND	I,II	Logical AND of AUX and data specified by {S, R/L} replaces data in field specified by {D, R/L.}	
XOR	I,II	Logical exclusive OR of AUX and data specified by {S, R/L} replaces data in field specified by {D, R/L.}	
XMIT	III,IV	The literal value I replaces the data in the field specified by {S,L.}	If S is an I/O address then I is limited to range 00-37. Otherwise I is limited to range 000-377.
NZT	III,IV	If the data in the field specified by {S, L} equals zero, perform the next instruction in sequence. If the data specified by {S,L} is not equal to zero, execute the instruction at address determined by using the literal I as an offset to the Program Counter.	If S is an I/O address then I is limited to range 00-37. Otherwise I is limited to range 000-377.
XEC	III,IV	Perform the instruction at address determined by applying the sum of the literal I and the data specified by {S, L} as an offset to the Program Counter. If that instruction does not transfer control, the program sequence will continue from the XEC instruction location.	The offset operation is performed by reducing the value of PC to the nearest multiple of 32 (if I = 00-37) or 256 (if I = 000-377) and adding the offset.
JMP	V	The address value A replaces contents of the Program Counter.	A limited to the range $0\text{-}17777_8$.

Table 3 8X300 INSTRUCTION SUMMARY

INSTRUCTION FORMATS

OPERATIONS
(REGISTER TO REGISTER)
MOVE AND
ADD XOR

0 1 2	3 4 5 6 7	8 9 10	11 12 13 14 15
OP CODE	S	R (ROTATE)	D

Type I

OPERATIONS
(REGISTER TO I/O, I/O TO REGISTER, I/O TO I/O)
MOVE ADD
AND XOR

0 1 2	3 4 5 6 7	8 9 10	11 12 13 14 15
OP CODE	S	L (LENGTH)	D

Type II

OPERATIONS

XEC XMIT*
NZT

0 1 2	3 4 5 6 7	8 9 10 11 12 13 14 15
OP CODE	S	I

Type III

OPERATIONS

XEC XMIT*
NZT

0 1 2	3 4 5 6 7	8 9 10	11 12 13 14 15
OP CODE	S	L (LENGTH)	I

Type IV

OPERATIONS

JMP

0 1 2	3 4 5 6 7 8 9 10 11 12 13 14 15
OP CODE	A

Type V

*NOTE
If XMIT, S actually represents the destination.

Figure 3

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INSTRUCTION FIELDS

Op Code Field (3-Bit Field)

The Op Code field is used to specify 1 or 8 8X300 instructions as shown in Table 4.

OP CODE OCTAL VALUE	INSTRUCTION	
0	MOVE	S,R/L,D
1	ADD	S,R/L,D
2	AND	S,R/L,D
3	XOR	S,R/L,D
4	XEC	I,R/L,S or I,S
5	NZT	I,R/L,S or I,S
6	XMIT	I,R/L,D or I,D
7	JMP	A

Table 4 OP CODE FIELD OCTAL ASSIGNMENTS

S,D Fields (5-Bit Fields)

The S and D fields specify the source and destination of data for the operation defined by the Op Code field. The Auxiliary Register is an implied second source for the instructions ADD, AND and XOR, each of which require two source fields. That is, instructions of the form,

ADD X, Y

imply a third operand, say Z, located in the Auxiliary Register so that the operation which takes place is actually X + Z, with the result stored in Y.

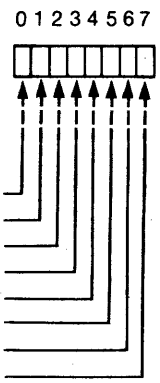
The S and/or D fields may specify a register, or a 1 to 8-bit I/O field. S and D field value assignments in octal are shown in Table 5.

0_8-17_8 is used to specify 1 of 7 working registers (R1-R6, R11), the Auxiliary Register, the Overflow Register, or IVL and IVR write-only registers.

OCTAL VALUE		OCTAL VALUE	
00	AUX-Auxiliary Register	10	OVF-Overflow register-Used only as a source
01	R1	11	R11
02	R2	12	Unassigned
03	R3	13	Unassigned
04	R4	14	Unassigned
05	R5	15	Unassigned
06	R6	16	Unassigned
07	IVL Register-Left Bank I/O address register. Used only as a destination.	17	IVR Register-Right Bank I/O address register. Used only as a destination.

a. Register Specification

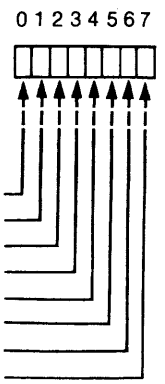
20_8-27_8 is used to specify the least significant bit of a variable length field within the I/O Port previously selected by the IVL register. The length of the field is determined by R/L.



OCTAL VALUE	
20	Field within previously selected Port; position of LSB = 0
21	Field within previously selected Port; position of LSB = 1
22	Field within previously selected Port; position of LSB = 2
23	Field within previously selected Port; position of LSB = 3
24	Field within previously selected Port; position of LSB = 4
25	Field within previously selected Port; position of LSB = 5
26	Field within previously selected Port; position of LSB = 6
27	Field within previously selected Port; position of LSB = 7

b. Left Bank I/O Field Specification

30_8-37_8 is used to specify the least significant bit of a variable length field within the I/O Port previously selected by the IVR Register. The length of the field is determined by R/L.



OCTAL VALUE	
30	Field within previously selected Port; position of LSB = 0
31	Field within previously selected Port; position of LSB = 1
32	Field within previously selected Port; position of LSB = 2
33	Field within previously selected Port; position of LSB = 3
34	Field within previously selected Port; position of LSB = 4
35	Field within previously selected Port; position of LSB = 5
36	Field within previously selected Port; position of LSB = 6
37	Field within previously selected Port; position of LSB = 7

c. Right Bank I/O Field Specification

Table 5 S AND D FIELD OCTAL ASSIGNMENTS

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R/L Field (3-Bit Field)

The R/L field performs one of two functions, specifying either a field length (L) or a right rotation (R). The function it specifies for a given instruction depends upon the contents of the S and D fields:

A. When both S and D specify registers, the R/L field is used to specify a right rotation of the data specified by the S field. (Rotation occurs on the bus and not in the source register.) The register source data is right rotated within one instruction cycle time independent of the number of bit positions specified in the R/L field.
B. When either or both the S and D fields specify a variable length I/O data field, the R/L field is used to specify the length of that data field.
C. R/L field assignments are shown in Table 6.

R/L FIELD OCTAL VALUE	SPECIFICATION
0	Field Length = 8 Bits
1	Field Length = 1 Bit
2	Field Length = 2 Bits
3	Field Length = 3 Bits
4	Field Length = 4 Bits
5	Field Length = 5 Bits
6	Field Length = 6 Bits
7	Field Length = 7 Bits

Table 6 R/L FIELD OCTAL ASSIGNMENTS

I Field (5/8-Bit Field)

The I field is used to load a literal value (contained in the instruction) into a register, or a variable I/O data field, or to modify the low order bits of the Program Counter.

The length of the I field is based on the S field in XEC, NZT, and XMIT instructions, as follows:

A. When S specifies a register, the literal I is an 8-bit field (Type III format).
B. When S specifies variable I/O data field, the literal I is a 5-bit field (Type IV format).

A Field (13-Bit Field)

The A field is a 13-bit Program Storage address field. This allows the 8X300 to directly address 8192 instructions.

REGISTER OPERATIONS

When a register is specified as the source and a variable I/O data field is specified as the destination, the low order bits of the results of the instructions MOVE, ADD, XOR are merged with the original destination data.

When an I/O data field of 1 to 8 bits is specified as the source, and a register as the destination, the 8-bit result of the operations MOVE, ADD, AND, XOR is stored in the register. The operations ADD, AND, XOR actually use the I/O data field (1 to 8 bits) with leading zeros to obtain 8-bit source data for use with the 8-bit AUX data during the operation.

IVL and IVR are write-only pseudo registers, and therefore can be specified as destination fields only. Operations involving IVL and IVR as sources are not possible. For example, it is not possible to increment IVR or IVL in a single instruction, and the contents of IVL or IVR cannot be transferred to a working register, or I/O Port.

The OVF (Overflow) Register can only be used as a source field; it is set or reset *only* by the ADD instruction.

ADDRESSING DATA ON THE INTERFACE VECTOR

I/O data fields are implemented via general purpose 8-bit I/O registers called Interface Vector (IV) Bytes. The IV registers serve to select IV bytes. In order for an instruction to access (read or write) an I/O data field, the address must be output to the IVL or IVR registers.

Thus, two instructions are required to operate on an Interface Vector byte.

```
XMIT    ADDRESS, IVL
MOVE    LB, RB
```

Each of the two IV registers (IVL and IVR) may be set to select an IV byte, therefore two I/O ports may be active at one time—one on the Right Bank (IVR) and one on the Left Bank (IVL). Data may be input and output in one instruction following the selection of IV bytes:

```
XMIT    ADDRESS1, IVL·
XMIT    ADDRESS2, IVR
ADD     LB, RB
```

Once the IV byte is selected (addressed) it will remain selected until another address is output to the same IV register. Since an IV register (IVL, IVR) can be used only as a destination field of an instruction, any instruction sending data to IVL or IVR can be used to select an IV byte.

From the user's standpoint, however, all IV byte outputs can be read by an external device regardless of whether they are selected or not.

The address range of IVL and IVR is $0\text{-}255_{10}$.

INSTRUCTION DESCRIPTIONS

The following instruction descriptions employ MCCAP (the 8X300 Cross Assembly Program) programming notation. This notation varies somewhat from the instruction descriptions provided in Tables 3 through 5. Thus, for example, explicit L field definition, as shown in Table 3 and Table 4 is not required by MCCAP instructions; MCCAP can create appropriate variable field addresses from information contained in Data Declaration statements which may be provided by the programmed at the beginning of his program.

The 8X300 instruction set is described below with examples shown in Figures 4 through 11.

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MOVE S,D or MOVE S(R),D

Format: Type I, Type II

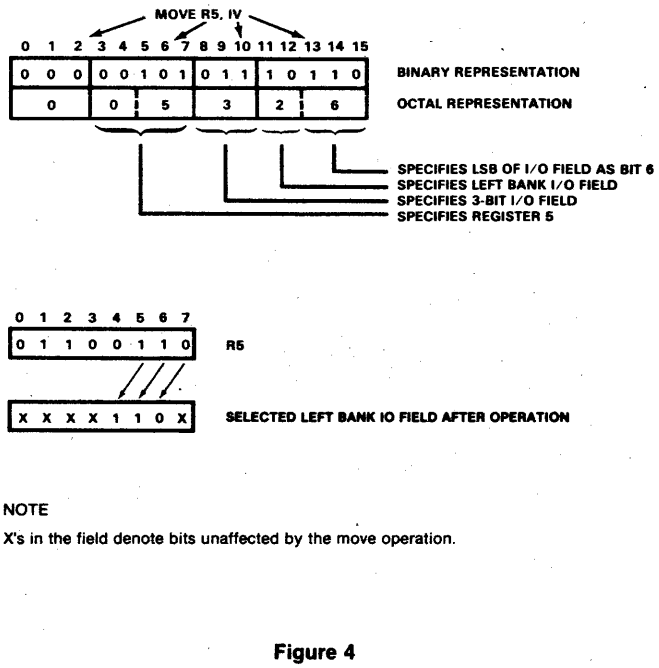
Operation: (S)➔(D)

Description

Move data. The contents of S are transferred to D; the contents of S are unaffected. If both S and D are registers, R/L specifies a right rotate of the source data before the move. Otherwise, R/L specifies the length of the source and/or destination I/O data field. If the MOVE is between Left Bank and Right Bank I/O field, an 8-bit field must always be moved.

Example

Store the least significant 3 bits of register 5 (R5) in bits 4, 5 and 6 of the I/O Port previously addressed by the IVL register. See Figure 4.



NOTE

X's in the field denote bits unaffected by the move operation.

Figure 4

ADD S,D or ADD S(R),D

Format: Type I, Type II

Operation: (S) + (AUX)⟶D
Carry⟶OVF

Description

Unsigned 2's complement 8-bit addition. The contents of S are added to the contents of the Auxiliary Register. The result is stored in D; OVF is set to the value of the carry. If both S and D are registers, R/L specifies a right rotate of the source (S) data before the operation. Otherwise, R/L specifies the length of the source and/or destination I/O data fields. S and AUX are unaffected unless specified as the destination.

Example

Add the contents of R1 rotated 4 places to AUX and store the result in R3. See Figure 5.

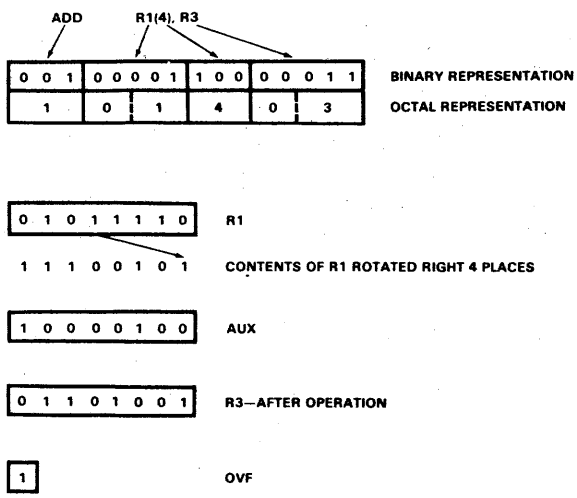


Figure 5

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AND S,D or AND S(R),D

Format: Type I, Type II

Operation: (S) ∧ (AUX)➔D

Description

Logical AND. The AND of the source field and the Auxiliary Register is stored into the destination. If both S and D are registers, R/L specifies a right rotate of the source (S) data before the AND operation. Otherwise R/L specifies the length of the source and/or destination I/O data fields. S and AUX are unaffected unless specified as a destination.

Example

Store the AND of the selected right bank I/O field and AUX in R4. The right bank data field is called WSBCD and is 4 bits long and located in bits 2, 3, 4 and 5. See Figure 6.

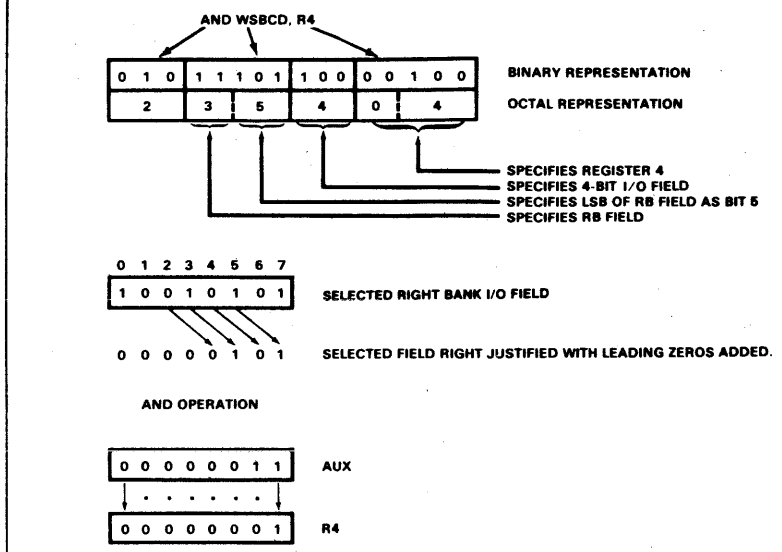


Figure 6

XOR S,D or XOR S(R),D

Format: Type I, Type II

Operation: (S) ⊕ (AUX)➔D

Description

Exclusive-OR. The Exclusive-OR of the source field and the Auxiliary Register is stored in the destination. If both S and D are registers, R/L specifies a right rotate of the source (S) data before the XOR operation. Otherwise R/L specifies the length of the source and/or destination I/O data fields. S and AUX are unaffected unless specified as a destination.

Example

Replace the selected I/O data field with the XOR of the field and AUX. The I/O data field is called STATUS and is 5 bits in length and located in bits 3, 4, 5, 6 and 7 of left bank. See Figure 7.

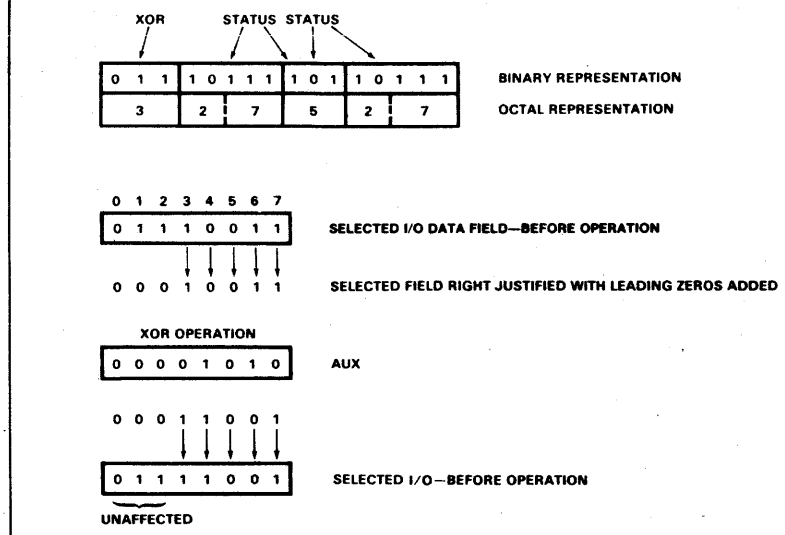


Figure 7

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XEC I(S)

Format: Type III, Type IV

Operation

Execute instruction at the address specified by the Address Register with lower 5 or 8 bits replaced by (S) + I.

Description

Execute the instruction at the address determined by replacing the low order bits of the Address Register (AR) with the low order bits of the sum of the literal I and the contents of the source field. If S is a register, the low order 8 bits of AR are replaced; if S is an I/O data field, the low order 5 bits of AR are replaced, resulting in an execute range of 256 and 32 respectively. The Program Counter is not affected unless the instruction executed is a JMP or NZT (whose branch is taken).

Example

Execute one of n JMPs in a table of JMP instructions determined by the value of the selected I/O data field on the left bank. The table follows immediately after the XEC instruction and the I/O field is called INTERPT and is a 3-bit field located in bits 4, 5 and 6. See Figure 8.

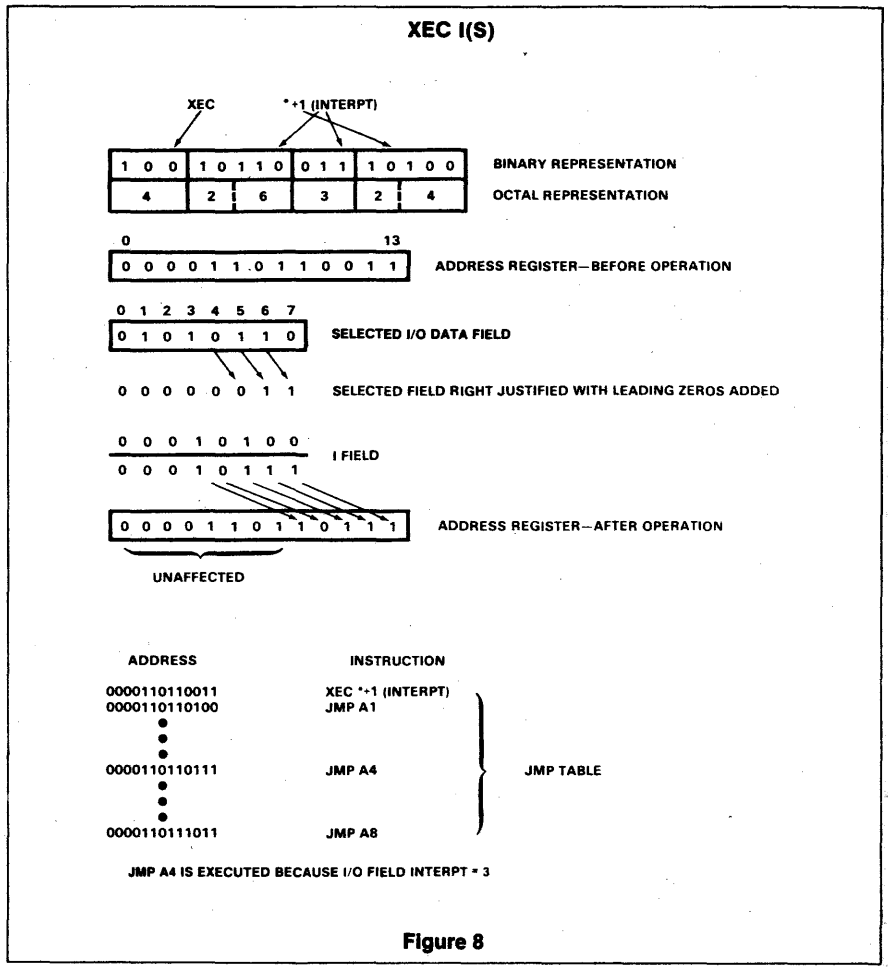


Figure 8

XMIT I,D

Format: Type III, Type IV

Operation: I→(D)

Description

Transmit literal. The literal field I is stored in D. If D is a register, an 8-bit field is transferred; if D is an I/O data field, up to a 5-bit field is transferred.

Example

Store the bit pattern 110 in the selected I/O data field on the right bank. The field name is VALUE and is located in bits 3, 4 and 5. See Figure 9.

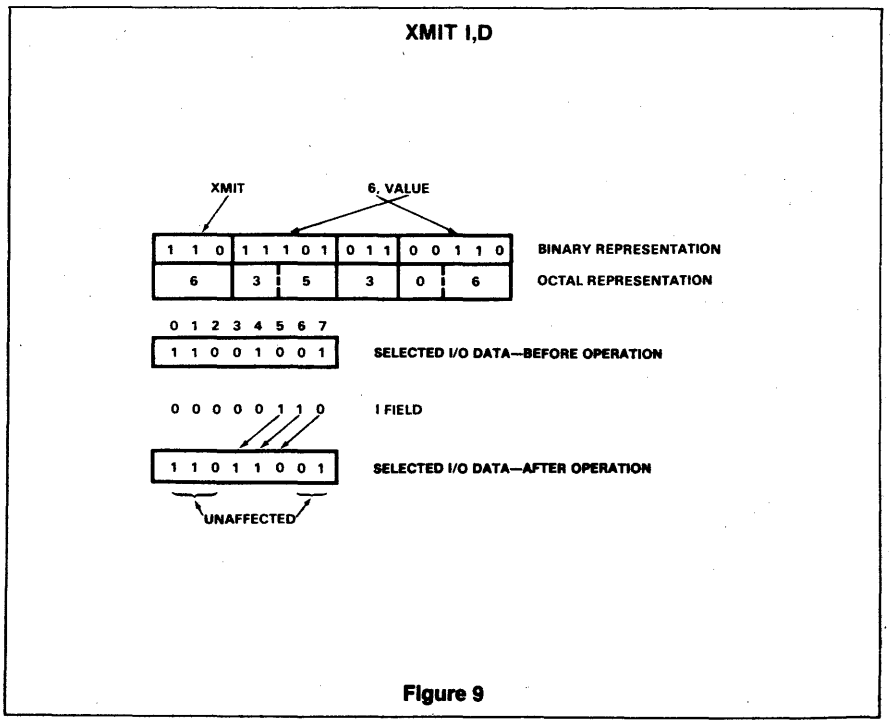


Figure 9

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NZT S,I

Format: Type III, Type IV

Operation:

Non-Zero Transfer. If (S) ≠ 0, PC offset by I → PC; otherwise PC + 1 → PC.

Description

If the data specified by the S field is non-zero, replace the low order bits of the Program Counter with I. Otherwise, processing continues with the next instruction in sequence. If S is a register, the low order 8 bits of the PC are replaced; if S is an I/O data field, the low order 5 bits of the PC are replaced, resulting in an NZT range of 256 and 32 respectively.

Example

Jump to Program Address ALPHA if the selected right bank I/O field is non-zero. The field name is OVERFLO and it is a 1-bit field located in bit 3. See Figure 10.

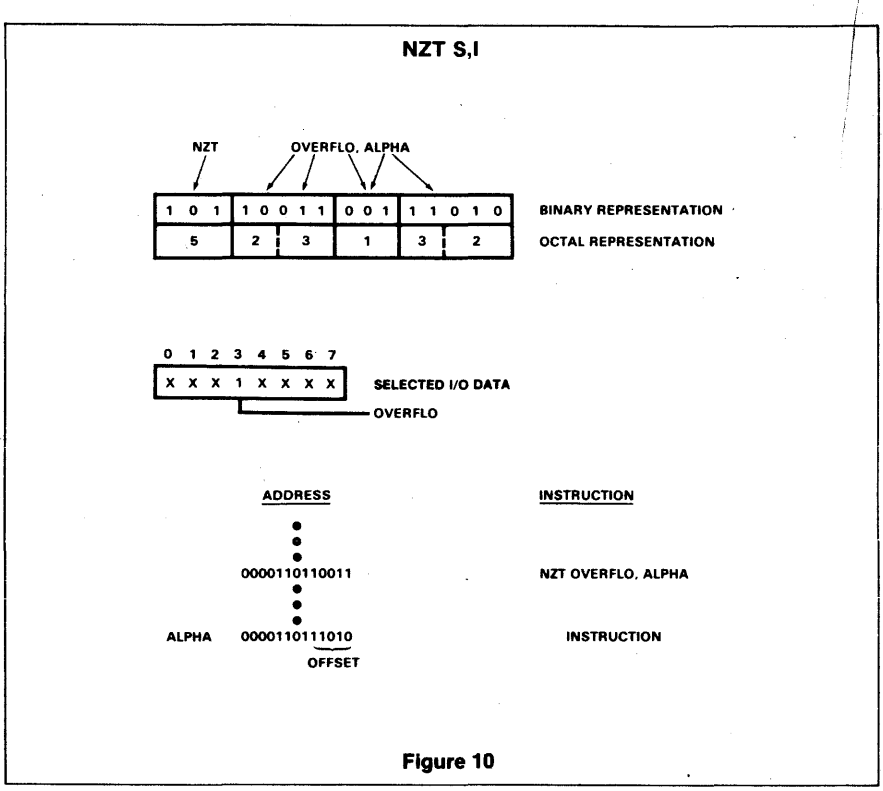


Figure 10

JMP A

Format: Type V

Operation: A → PC

Description

The literal value A is placed in the Program Counter and Address Register, and processing continues at location A. A has a range of 0-17777$_8$ (0-8191).

Example

Jump to location ALPHA (0000101110001). See Figure 11.

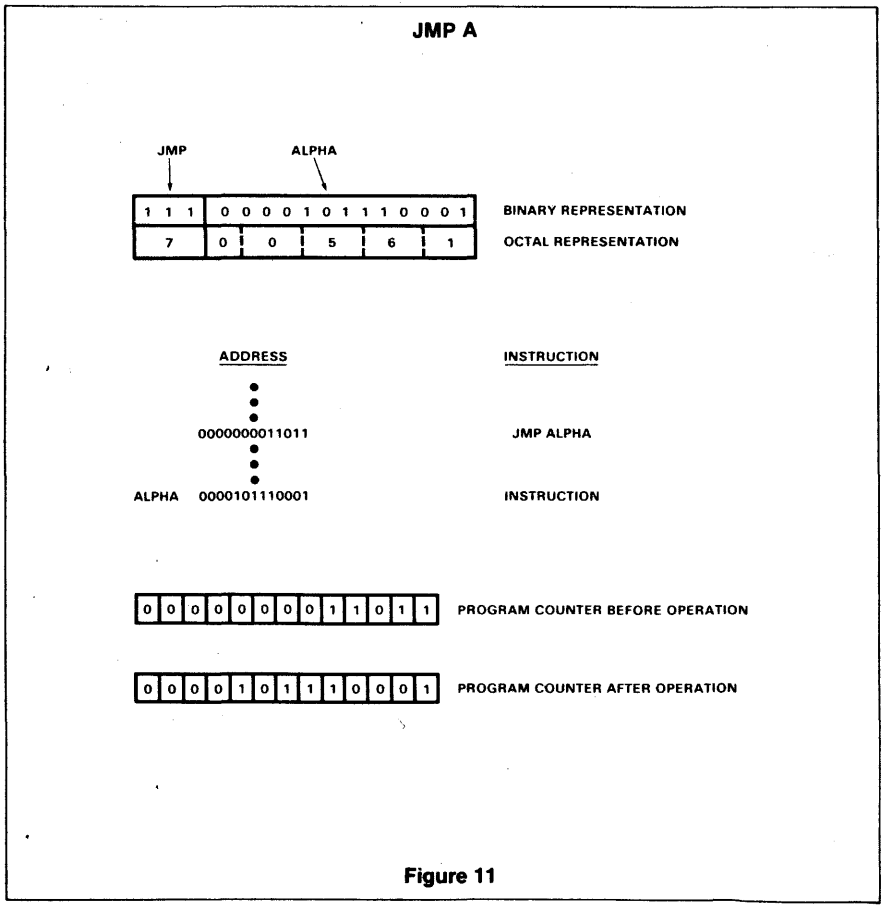


Figure 11

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SYSTEM DESIGN USING THE 8X300 MICROCONTROLLER

Designing hardware around the 8X300 Interpreter reduces to selecting a program storage devicer (ROM, PROM, etc.), selecting I/O devices (IV byte, multiplexers, RAM, etc.), selecting clock mode (system driven or crystal controlled) and interfacing the Microcontroller to these components.

A specific example of a control system using the 8X300 Microcontroller is shown in Figure 12. Only 8 components—four 8T32 I/O Ports, one 82S208 RAM, two 82S215 ROMs, and an 8X300 are required to build this system which contains 512 words of program storage, 32 TTL I/O connection points, 256 bytes of working storage, and operates at a 250ns instruction cycle time.

Halt, Reset Signals

$\overline{\text{HALT}}$:
A low level at the $\overline{\text{HALT}}$ input stops internal operation of the Microcontroller at the start of the next instruction after $\overline{\text{HALT}}$ is applied (quarter cycle after MCLK). Since $\overline{\text{HALT}}$ is sampled at the start of each instruction cycle it is possible to prevent a cycle by applying $\overline{\text{HALT}}$ early in that cycle. $\overline{\text{HALT}}$ does not inhibit MCLK or affect any internal registers. Normal operation begins with the next complete cycle after the $\overline{\text{HALT}}$ input goes high.

$\overline{\text{RESET}}$:
A low level at the $\overline{\text{RESET}}$ input sets the program counter and address register to zero. While $\overline{\text{RESET}}$ is low MCLK is inhibited. If $\overline{\text{RESET}}$ is applied during the last 2 quarter cycles, the MCLK during that cycle may be shortened. $\overline{\text{RESET}}$ should be applied for 1 full instruction cycle time to assure proper operation. When $\overline{\text{RESET}}$ input goes high an MCLK occurs prior to the resumption of normal processing. $\overline{\text{RESET}}$ does not affect the other internal registers.

SYSTEM TIMING

In systems with fast instruction cycle times, most Microcontroller delays are strictly determined by internal gate propagation delays.

EXAMPLE OF CONTROL SYSTEM

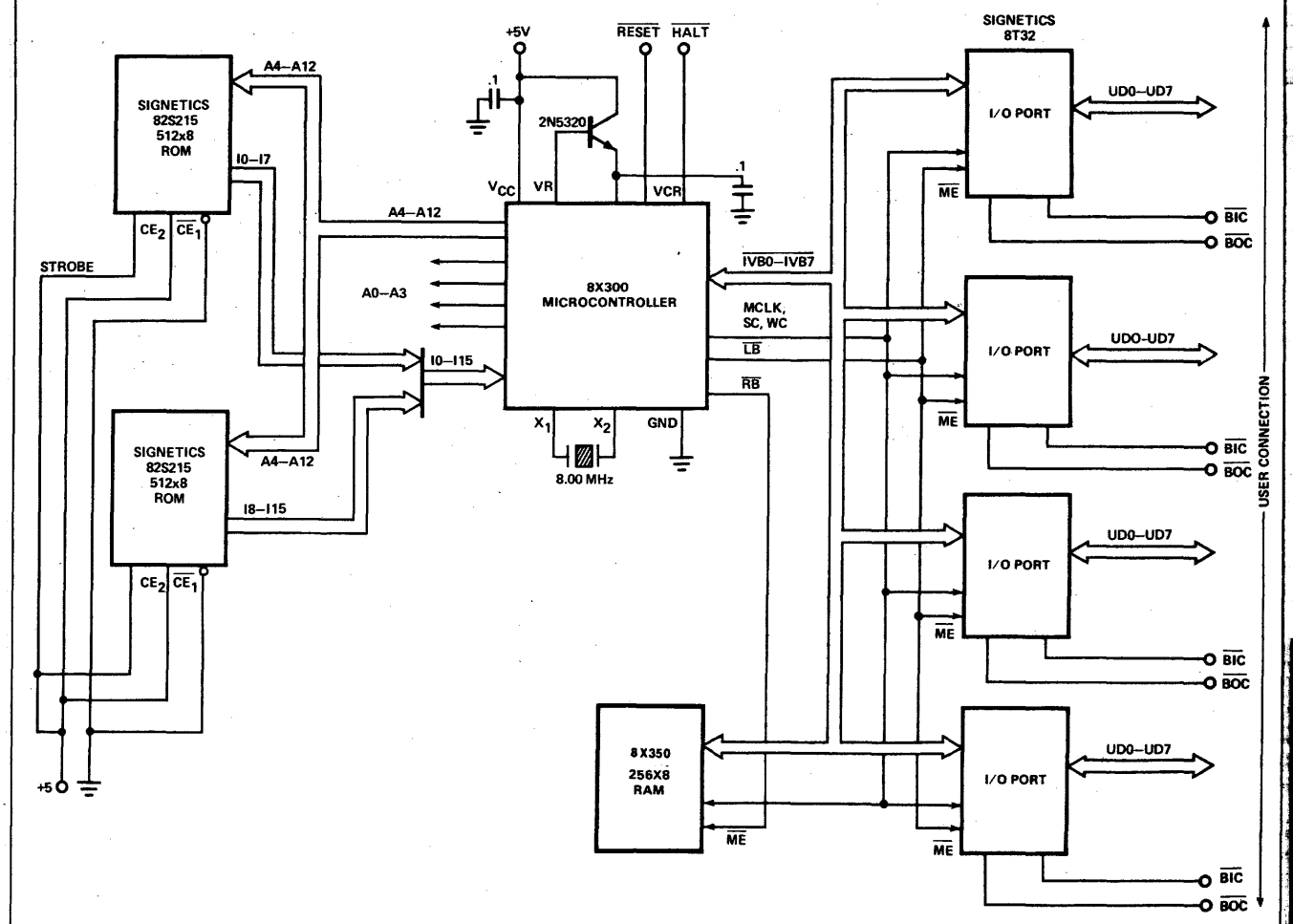


Figure 12

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Since some events are constrained to occur in certain quarter cycles, as system cycle times become slower, the delays will appear to increase due to gating with internal clocks. In the table of AC Electrical Characteristics, 2 columns are used: 1 to denote times which occur due to internal clock intervention and 1 to denote minimum delays for fast cycle times.

When using Signetics 8T32 I/O Ports, selection of instruction cycle time involves calculating the maximum program storage access time. Assuming the instruction is available when MCLK falls, the I/O control lines are stable 35ns later. Signetics 8T32's require another 35ns to disable a previously selected port and enable the desired port (assumes a change in bank signals). A 10ns margin has been added to the 8T32 enable for this evaluation to reflect the fact that most systems will have more capacitive loading than the 50pF test condition in the 8T32 specification and to allow for line delays.

The system instruction cycle time for normal systems such as shown in Figure 12 is determined by Microcontroller propagation delays, program storage access time, and port output enable times. Instruction cycle time is normally constrained by one or more of the following conditions:

1. Instruction to LB/RB (input phase) and I/O Port output enable:
   $T_{OE} \leq \frac{1}{2}$ cycle - 55ns (Figure 13).
2. Program storage access time and instruction to LB/RB (input phase) and I/O Port output enable and IV data (input phase) to address ≤ instruction cycle time (Figure 14).
3. Program storage access time and instruction to address ≤ instruction cycle time (Figure 15).

The first constraint can be used to determine the minimum cycle time. Using the inequality 35ns + 35ns ≤ ½ cycle - 55ns implies ½ cycle ≥ 125ns or an instruction time of 250ns.

Program storage access time for a 250ns instruction cycle can be calculated from the second constraint. Noting that the specification for IV data (input phase) to address is 115ns: Program storage access time + 35ns + 35ns + 115ns ≤ 250ns implies program storage access time ≤ 65ns.

The third constraint can be used to verify the maximum program storage access time. Noting that the specification for instruction to address is 185ns: Program storage access time + 185ns ≤ 250ns confirms that program storage access time 65ns is satisfactory.

SYSTEM INSTRUCTION CYCLE TIME

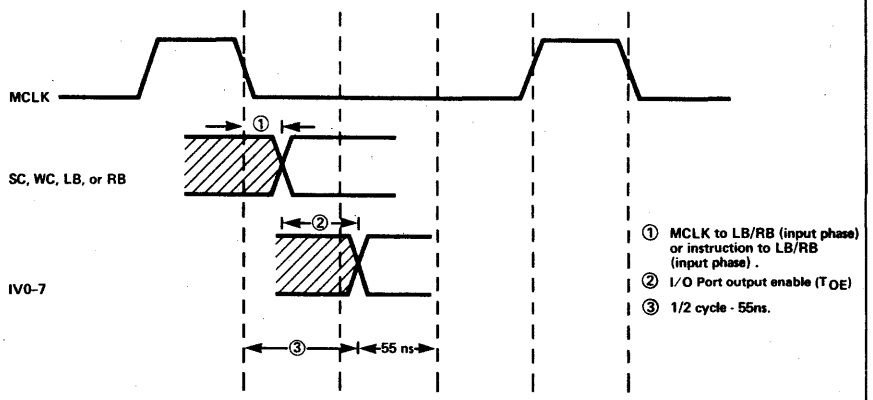


Figure 13

SYSTEM INSTRUCTION CYCLE TIME

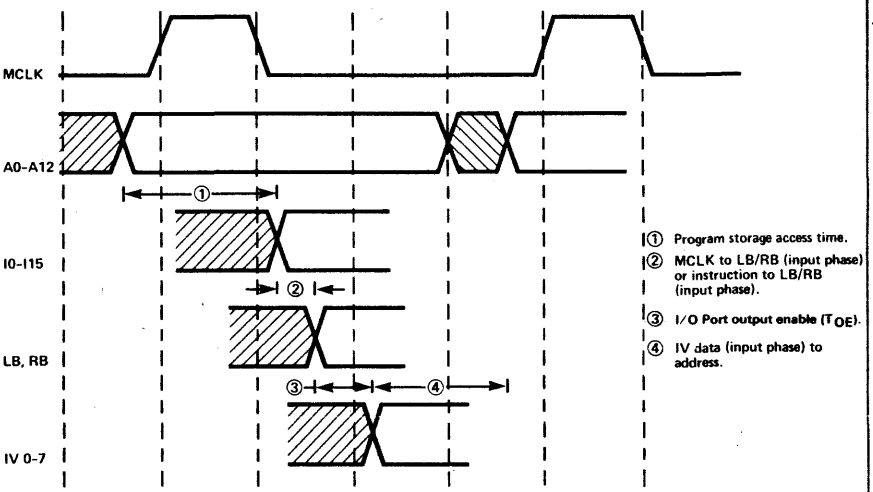


Figure 14

SYSTEM INSTRUCTION CYCLE TIME

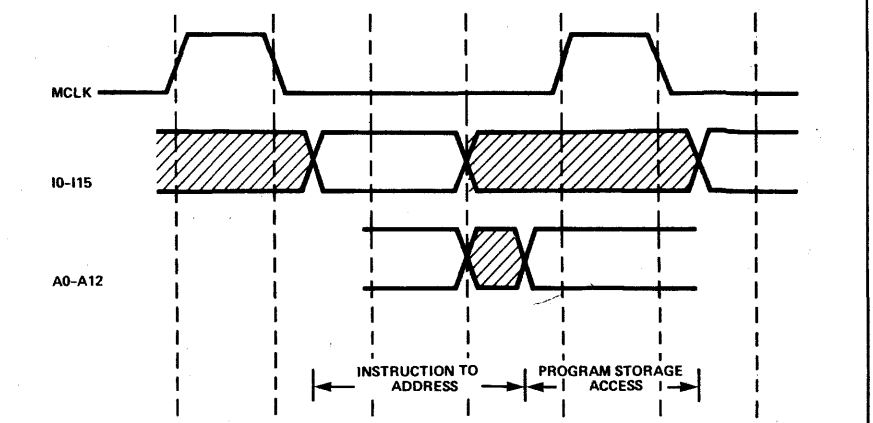


Figure 15

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System Clock

The Micrcontroller has an integrated oscillator which generates all necessary clock signals. The oscillator is designed to connect directly to a series resonant quartz crystal via pins X1 and X2. The crystal resonant frequency, f, is related to the desired cycle time, T, by the relationship f = 2/T. For a 250ns system, f = 8.00MHz.

Type:	Fundamental mode, series resonant
Impedance at Fundamental:	35 ohms maximum
Impedance at harmonics and spurs:	50 ohms minimum

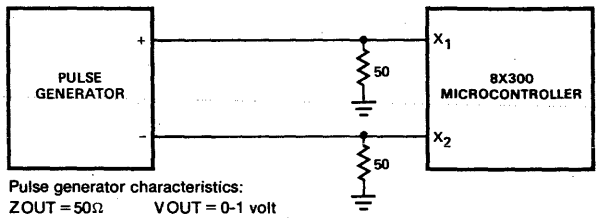
Table 7 CRYSTAL CHARACTERISTICS

In lower speed applications where the cycle time need not be precisely controlled, a capacitor may be connected between X1 and X2 to drive the oscillator. Approximate capacitor values are given in Table 8. If cycle time is to be varied, X1 and X2 should be driven from complementary outputs of a pulse generator. Figure 16 shows a typical configuration. For systems where the Interpreter is to be driven from a master clock the X1 and X2 lines may be interfaced to TTL logic as shown in Figure 17.

Cx,pF	
100	300ns
200	500ns
500	1.1μs
1000	2.0μs

Table 8 CLOCK CAPACITOR VALVES

CLOCKING WITH A PULSE GENERATOR

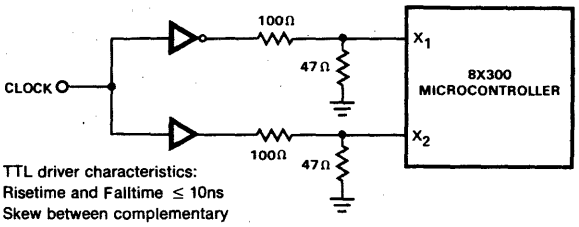


Pulse generator characteristics:
ZOUT = 50Ω VOUT = 0-1 volt
Risetime ≤ 10ns ≤ Skew ≤ 10ns
Complementary outputs

NOTE: All resistors values are typical and in ohms.

Figure 16

CLOCKING WITH TTL



TTL driver characteristics:
Risetime and Falltime ≤ 10ns
Skew between complementary outputs ≤ 10ns

Figure 17

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5% and 0°C ≤ T_A < 70°C

DELAY DESCRIPTION	PROPAGATION DELAY TIME	CYCLE TIME LIMIT
X1 falling edge to MCLK (driven from external pulse generator)	75ns	
MCLK to SC/WC falling edge (input phase)	25ns	
MCLK to SC/WC rising edge (output phase)		½ cycle + 25ns
MCLK to LB/RB (input phase)	35ns	
Instruction to LB/RB output (input phase)	35ns	
MCLK to LB/RB (output phase)		¼ cycle + 35ns
MCLK to IV data (output phase)	185ns	½ cycle + 60ns
IV data (input phase) to IV data (output phase)	115ns	
Instruction to Address	185ns	½ cycle + 40ns
MCLK to Address	185ns	½ cycle + 40ns
IV data (input phase) to Address	115ns	
MCLK to IV data (input phase)		½ cycle - 55ns
MCLK to Halt falling edge to prevent current cycle		¼ cycle - 40ns
Reset rising edge to first MCLK		0 to 1 cycle

NOTE
1. Reference to MCLK is to the falling edge when loaded with 300pF.
2. Loading on Address lines is 150pF.

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TYPICAL INSTRUCTION CYCLE TIMING

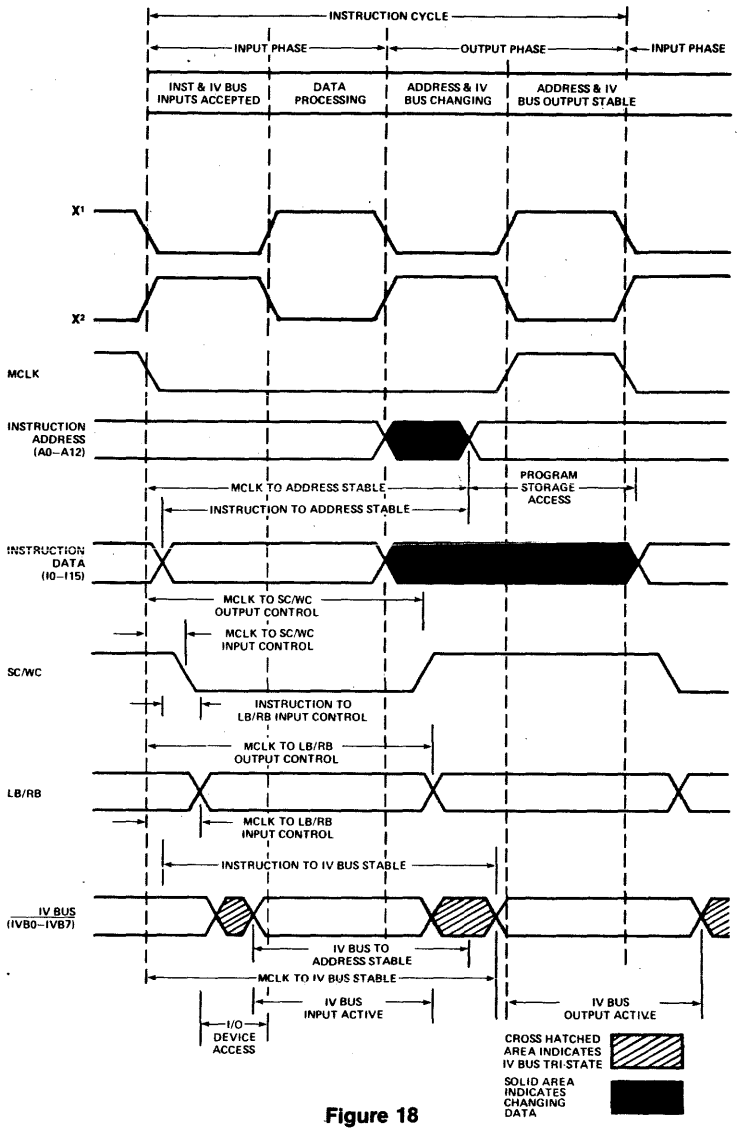


Figure 18

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DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{IH} High level input voltage					
X1,X2		.6			V
All others		2			V
V_{IL} Low level input voltage					
X1,X2				.4	V
All others				.8	V
V_{IC} Input clamp voltage (Note 1)	V_{CC} = 4.75V, I_I = -10mA			-1.5	V
I_{IH} High level input current					
X1,X2	V_{CC} = 5.25V, V_{IH} = .6V		2700		μA
All others	V_{CC} = 5.25V, V_{IH} = 4.5V		<1	50	μA
I_{IL} Low level input current					
X1,X2	V_{CC} = 5.25V, V_{IL} = .4V		-2500		μA
$\overline{IVBO}$-7			-140	-200	μA
IO-I15	V_{CC} = 5.25V, V_{IL} = .4V		-880	-1600	μA
$\overline{HALT}$, $\overline{RESET}$	V_{CC} = 5.25V, V_{IL} = .4V		-230	-400	μA
V_{OL} Low level output voltage					
A0-A12	V_{CC} = 4.75V, I_{OL} = 4.25mA		.35	.55	V
All others	V_{CC} = 4.75V, I_{OL} = 16mA		.35	.55	V
V_{OH} High level output voltage	V_{CC} = 4.75V, I_{OH} = 3mA	2.4			V
I_{OS} Short circuit output current (Note 2)	V_{CC} = 5.25V	-30		-140	mA
V_{CC} Supply voltage		4.75	5	5.25	V
I_{CC} Supply current	V_{CC} = 5.25V			1.60	mA
I_{REG} Regulator control	V_{CC} = 5.0V	-14		-21	mA
I_{CR} Regulator current (Note 3)				290	mA
V_{CR} Regulator voltage (Note 3)		2.2		3.2	V

NOTES
1. Crystal inputs X1 and X2 do not have clamp diodes.
2. Only one output may be grounded at a time.
3. (Limits apply for V_{CC} = 5V ± 5% and 0°C < T_A < 70°C unless specified otherwise.)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC} Supply voltage	7	V
Logic input voltage	5.5	V
Crystal input voltage	2	V

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8T31-N/F

DESCRIPTION

The I/O Port is an 8-bit bidirectional data register designed to function as an I/O interface element in microprocessor systems. It contains 8 clocked data latches accessible from either a microprocessor port or a user port. Separate I/O control is provided for each port. The 2 ports operate independently, except when both are attempting to input data into the I/O Port. In this case, the user port has priority.

A master enable (ME) is provided that enables or disables the μP bus regardless of the state of the other inputs, but has no effect on the user bus.

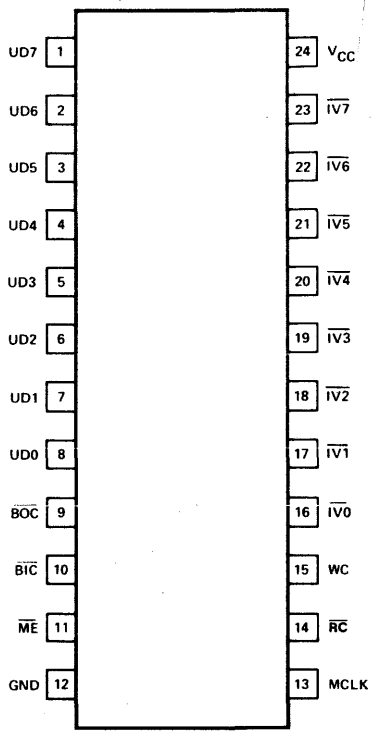
A unique feature of this family is its ability to start up in a predetermined state. If the clock is maintained at a voltage less than .8V until the power supply reaches 3.5V, the user port will always be all logic 1 levels, while the microprocessor port will be all logic 0 levels.

FEATURES

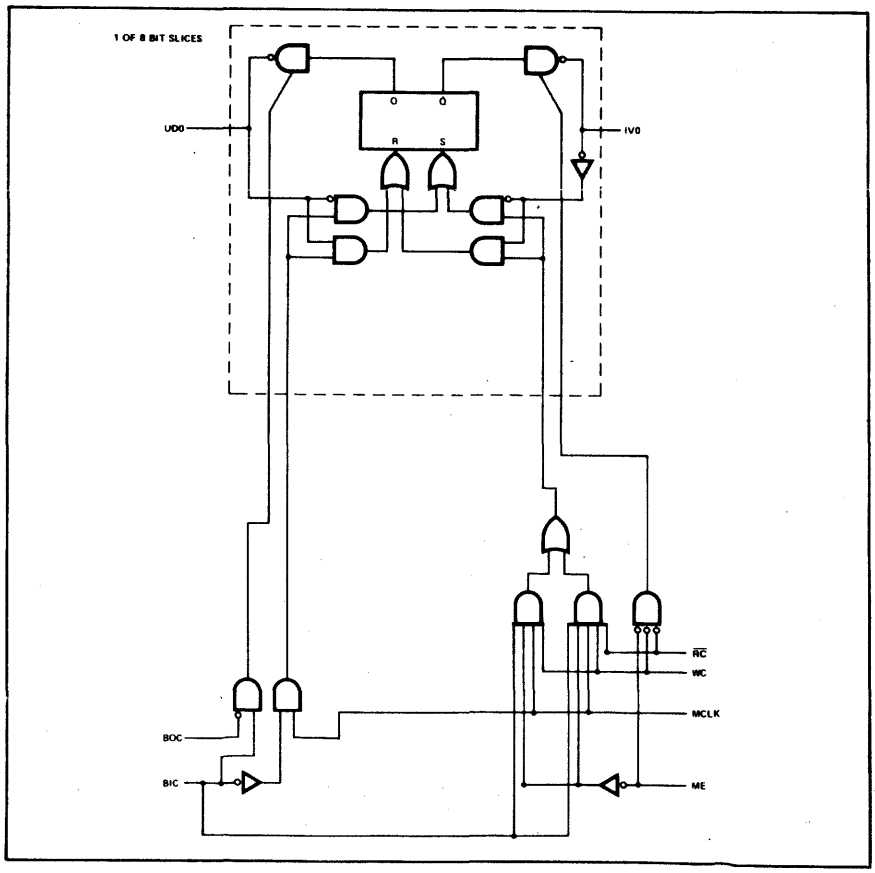
- **Each device has 2 ports, one to the user, the other to a microprocessor. I/O Ports are completely bidirectional**
- **Ports are independent, with the user port having priority for data entry**
- **User data input synchronous**
- **The user data bus is available with tri-state (8T32, 8T36) or open collector (8T33, 8T35) outputs**
- **At power up, the user port outputs are high**
- **Tri-state TTL outputs for high drive capability**
- **Directly compatible with the 8X300 Microcontroller**
- **Operates from a single 5V power supply over a temperature range of 0°C to +70°C**

PIN CONFIGURATION

F,NA PACKAGE



BLOCK DIAGRAM



signetics

Signetics MICROPROCESSOR

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PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-8	UD0-UD7:	User Data I/O Lines. Bidirectional data lines to communicate with user's equipment.	Acitve high three-state
16-23	$\overline{IV0}$-$\overline{IV7}$:	Microprocessor Bus. Bidirectional data lines to communicate with controlling digital system.	Active low three-state
10	$\overline{BIC}$:	Input Control. User input to control writing into the I/O Port from the user data lines.	Active low
9	$\overline{BOC}$:	Output Control. User input to control reading from the I/O Port onto the user data lines.	Active low
11	$\overline{ME}$:	Master Enable. System input to enable or disable all other system inputs and outputs. It has no effect on user inputs and outputs.	Active low
15	WC:	Write Command. When WC is high, stores contents of IV0-IV7 as data.	Active high
14	$\overline{RC}$	Read Command. When RC is low, data is presented on IV0-IV7.	Active low
13	MCLK:	Master Clock. Input to strobe data into the latches. See function tables for details.	Active high
24	V_{CC}:	5V power connection.	
12	GND:	Ground.	

$\overline{BIC}$	$\overline{BOC}$	MCLK	USER DATA BUS FUNCTION
H	L	X	Output Data
L	X	H	Input Data
H	H	X	Inactive

H = High Level L = Low Level X = Don't care

Table 1 USER PORT CONTROL FUNCTION

$\overline{ME}$	$\overline{RC}$	WC	MCLK	$\overline{BIC}$	MICROPROCESSOR BUS FUNCTION
L	L	L	X	X	Output Data
L	X	H	H	H	Input Data
X	H	L	X	X	Inactive
X	X	H	X	L	Inactive
H	X	X	X	X	Inactive

Table 2 MICROPROCESSOR PORT CONTROL FUNCTION

USER DATA BUS CONTROL

The activity of the user data bus is controlled by the BIC and BOC inputs as shown in Table 1.

The user data input is a synchronous function with MCLK. A low level on the BIC input allows data on the user data bus to be written into the data latches only if MCLK is at a high level. A low level on the BIC input allows data on the user data bus to be latched regardless of the level of the MCLK input.

To avoid conflicts at the data latches, input from the microprocessor port is inhibited when BIC is at a low level. Under all other conditions the 2 ports operate independently.

MICROPROCESSOR BUS CONTROL

As is shown in Table 2, the activity of the microprocessor port is controlled by the ME, RC, WC and BIC inputs, as well as the state of an internal status latch. BIC is included to show user port priority over the microprocessor port for data input.

BUS OPERATION

Data written into the I/O Port from one port will appear inverted when read from the other port. Data written into the I/O Port from one port will not be inverted when read from the same port.

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DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5%, 0°C ≤ TA ≤ 70°C unless otherwise specified.

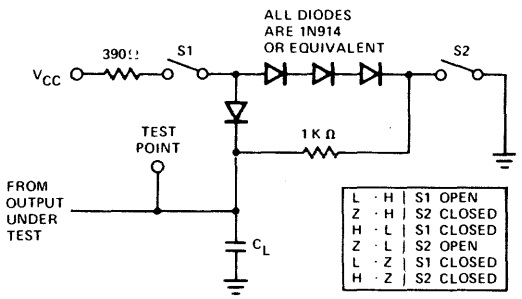
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Min	
	Input voltage					V
V_{IH}	High		2.0			
V_{IL}	Low				.8	
V_{IC}	Clamp	I_I = -5mA			-1	
	Output voltage	V_{CC} = 4.75V				V
V_{OH}	High		2.4			
V_{OL}	Low				.55	
	Input current[1]	V_{CC} = 5.25V				μA
I_{IH}	High	V_{IH} = 5.25V		<10	100	
I_{IL}	Low	V_{IL} = .5V		-350	-550	
	Output current[2]					mA
I_{OS}	Short circuit	V_{CC} = 4.75V				
	UD bus		10			
	IV bus		20			
I_{CC}	VCC supply current	V_{CC} = 5.25V		100	150	mA

NOTES

1. The input current includes the tri-state/open collector leakage current of the output driver on the data lines.
2. Only one output may be shorted at a time.

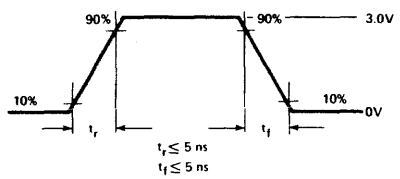
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT FOR TRI-STATE OUTPUTS

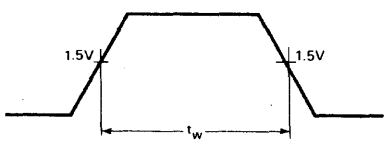


NOTE: C_L includes fixture capacitance.

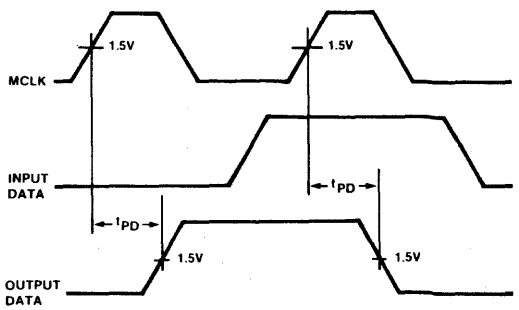
INPUT WAVEFORM



CLOCK PULSE WIDTH



DATA DELAY TIMES
Clock Referenced



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AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 5\%$

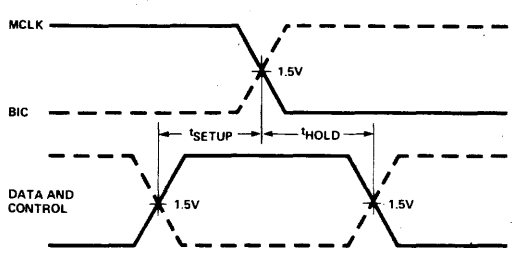
PARAMETER		INPUT	TEST CONDITION	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
t_{PD}	User data delay[1]	UDX	$C_L = 50pF$		25	38	ns
		MCLK			45	61	ns
t_{OE}	User output enable	BOC	$C_L = 50pF$	18	26	47	ns
t_{OD}	User output disable	BIC	$C_L = 50pF$	18	28	35	ns
		BOC		16	23	33	ns
t_{PD}	μP data delay[1]	IVBX	$C_L = 50pF$		38	53	ns
		MCLK			48	61	ns
t_{OE}	μP output enable	ME RC WC	$C_L = 50pF$	14	19	25	ns
t_{OD}	μP output disable	ME RC WC	$C_L = 50pF$	13	17	32	ns
t_W	Minimum pulse width	MCLK		40			ns
t_{SETUP}	Minimum setup time[2]	UDX[3]		15			ns
		BIC		25			
		IVX		55			
		ME		30			
		RC		30			
		WC		30			
t_{HOLD}	Minimum hold time[2]	UDX[3]		25			ns
		BIC		10			
		IVX		10			
		ME		5			
		RC		5			
		WC		5			

NOTES

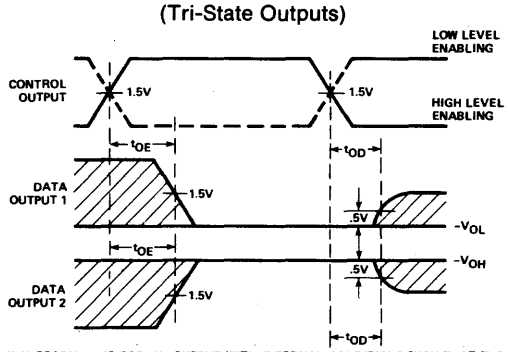
1. Data delays referenced to the clock are valid only if the input data is stable at the arrival of the clock and the hold time requirement is met.
2. Set up and hold times given are for "normal" operation. BIC setup and hold times are for a user write operation. RC setup and hold times are for an I/O Port select operation. ME and WC setup and hold times are for a microprocessor bus write operation.
3. Times are referenced to MCLK

VOLTAGE WAVEFORMS

SETUP AND HOLD TIMES



OUTPUT ENABLE AND DISABLE TIMES
(Tri-State Outputs)



WAVEFORM #1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW WHEN THE TRI-STATE DRIVER IS ENABLED. WAVEFORM #2 IS FOR THE OPPOSITE CONDITION.

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8T32/8T33/8T35/8T36-F,NA

TYPES

8T32 Tri-State, Synchronous User Port
8T33 Open Collector, Synchronous User Port
8T35 Open Collector, Asynchronous User Port
8T36 Tri-State, Asynchronous User Port

DESCRIPTION

The Addressable I/O Port is an 8-bit bidirectional data register designed to function as an I/O interface element in microprocessor systems. It contains 8 data latches accessible from either a microprocessor port or a user port. Separate I/O control is provided for each port. The 2 ports operate independently, except when both are attempting to input data into the I/O Port. In this case, the user port has priority.

A unique feature of the I/O Port is the way in which it is addressed. Each device has an 8-bit, field programmable address, which is used to enable the microprocessor port. When the SC control signal is high, data at the microprocessor port is treated as an address. If the address matches the I/O Port's internally programmed address, the microprocessor port is enabled, allowing data transfer through it.

The port remains enabled until an address which does not match is presented, at which time the port is disabled (data transfer is inhibited). A Master Enable input (ME) can serve as a ninth address bit, allowing 512 I/O Ports to be individually selected on a bus, without decoding. The user port is accessible at all times, independent of whether or not the microprocessor port is selected.

A unique feature of this family is their ability to start up in a predetermined state. If the clock is maintained at a voltage less than .8V until the power supply reaches 3.5V, the user port will always be all logic 1 levels, while the port will be all logic 0 levels.

ORDERING

The 8T32/33/35/36 may be ordered in preaddressed form. To order a preaddressed device use the following part number format:

N8TYY-XXX P

- -P = F Ceramic package, NA Plastic package
- XXX = Any address from 000 through 255 (decimal) - 256 available addresses
- YY = I/O Port version (32, 33, 35, 36)

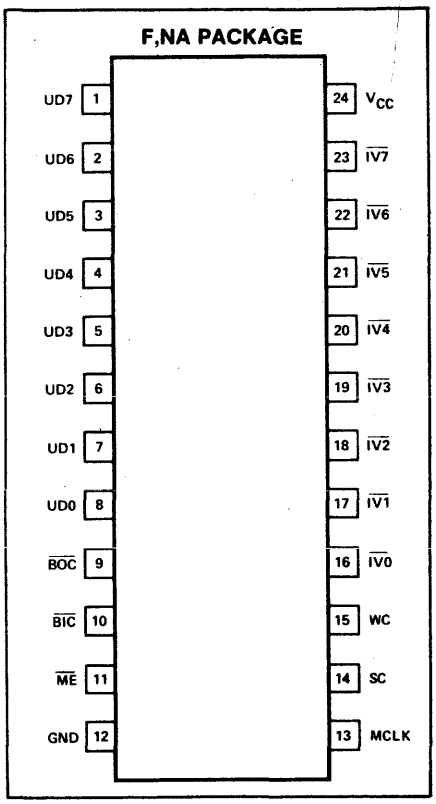
A stock of 8T32s and 8T36s with addresses 1 through 10 will be maintained. A small quantity of addresses 11 through 50 will also be available with a longer lead time.

FEATURES

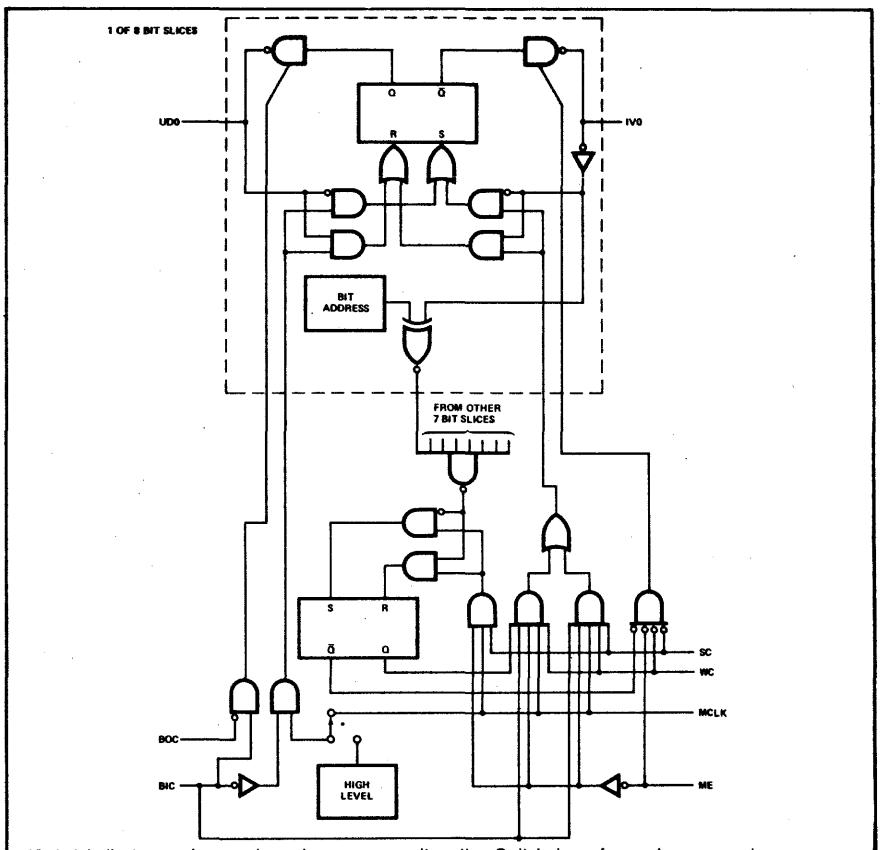
- **A field-programmable address allows 1 of 512 I/O Ports on a bus to be selected, without decoders.**
- **Each device has 2 ports, one to the user, the other to a microprocessor.**
- **Completely bidirectional.**
- **Ports are independent, with the user port having priority for data entry.**
- **A selected I/O Port de-selects itself when another I/O Port address is sensed.**
- **User data input available as synchronous (8T32, 8T33) or as asynchronous (8T35, 8T36) function.**
- **The user data bus is available with tri-state (8T32, 8T36) or open collector (8T33, 8T35) outputs.**
- **At power up, the I/O Port is not selected and the user port outputs are high.**
- **Tri-state TTL outputs for high drive capability.**
- **Directly compatible with the 8X300 Microcontroller.**
- **Operates from a single 5V power supply over a temperature range of 0° C to 70° C.**

PIN CONFIGURATION

F,NA PACKAGE



BLOCK DIAGRAM



*Switch indicates synchronous/asynchronous user write option. Switch shown for synchronous version.

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PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-8	UD0-UD7:	User Data I/O Lines. Bidirectional data lines to communicate with user's equipment. Either tri-state or open collector outputs are available.	Active high
16-23	$\overline{IV0}$-$\overline{IV7}$:	Microprocessor Bus. Bidirectional data lines to communicate with controlling digital system (microprocessor).	Active low three-state
10	$\overline{BIC}$:	Input Control. User input to control writing into the I/O Port from the user data lines.	Active low
9	$\overline{BOC}$:	Output Control. User input to control reading from the I/O Port onto the user data lines.	Active low
11	$\overline{ME}$:	Master Enable. System input to enable or disable all other system inputs and outputs. It has no effect on user inputs and outputs.	Active low
15	WC:	Write Command. When WC is high and SC is low, I/O Port, if selected, stores contents of IV0-IV7 as data.	Active high
14	SC:	Select Command. When SC is high and WC is low, data on IV0-IV7 is interpreted as an address. I/O Port selects itself if its address is identical to μP bus data; it de-selects itself otherwise.	Active high
13	MCLK:	Master Clock. Input to strobe data into the latches. See function tables for details.	Active high
24	VCC:	5V power connection.	
12	GND:	Ground.	

$\overline{BIC}$	$\overline{BOC}$	MCLK	USER DATA BUS FUNCTION	
			8T32, 8T33	8T35, 8T36
H	L	X	Output Data	Output Data
L	X	H	Input Data	Input Data
L	X	L	Inactive	Input Data
H	H	X	Inactive	Inactive

H = High Level L = Low Level X = Don't care

Table 1 USER PORT CONTROL FUNCTION

$\overline{ME}$	SC	WC	MCLK	$\overline{BIC}$	STATUS LATCH	I/O PORT FUNCTION
L	L	L	X	X	SET	Output Data
L	L	H	H	H	SET	Input Data
L	H	L	H	X	X	Input Address
L	H	H	H	L	X	Input Address
L	H	H	H	H	X	Input Data and Address
L	X	H	L	X	X	Inactive
L	H	X	L	X	X	Inactive
L	L	H	H	L	X	Inactive
L	L	X	X	X	Not Set	Inactive
H	X	X	X	X	X	Inactive

Table 2 MICROPROCESSOR PORT CONTROL FUNCTION

signetics

USER DATA BUS CONTROL

The activity of the user data bus is controlled by the BIC and BOC inputs as shown in Table 1.

For the 8T32 and 8T33, user data input is a synchronous function with MCLK. A low level on the BIC input allows data on the user data bus to be written into the data latches only if MCLK is at a high level. For the 8T35 and 8T36, user data input is an asynchronous function. A low level on the BIC input allows data on the user data bus to be latched regardless of the level of the MCLK input. Note that when 8T35 or 8T36 are used with the 8X300 Microcontroller care must be taken to insure that the Microprocessor bus is stable when it is being read by the 8X300 Microcontroller.

To avoid conflicts at the Data Latches, input from the Microprocessor Port is inhibited when BIC is at a low level. Under all other conditions the 2 ports operate independently.

MICROPROCESSOR BUS CONTROL

As is shown in Table 2, the activity of the microprocessor port is controlled by the ME, SC, WC and BIC inputs, as well as the state of an internal status latch. BIC is included to show user port priority over the microprocessor port for data input.

Each I/O Port's status latch stores the result of the most recent I/O Port select; it is set when the I/O Port's internal address matches the Microprocessor Bus. It is cleared when an address that differs from the internal address is presented on the Microprocessor Bus.

In normal operation, the state of the status latch acts like a master enable; the microprocessor port can transfer data only when the status latch is set.

When SC and WC are both high, data on the Microprocessor Bus is accepted as data, whether or not the I/O Port was selected. The data is also interpreted as an address. The I/O Port sets its select status if its address matches the data read when SC and WC were both high; it resets its select status otherwise.

BUS OPERATION

Data written into the I/O Port from one port will appear inverted when read from the other port. Data written into the I/O Port from one port will not be inverted when read from the same port.

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AC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 5\%$

PARAMETER	INPUT	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
t_{PD} User data delay (Note 1)	UDX	C_L = 50pF		25	38	ns
	MCLK*			45	61	
	BIC†			40	55	
t_{OE} User output enable	BOC	C_L = 50pF	18	26	47	ns
t_{OD} User output disable	BIC	C_L = 50pF	18	28	35	ns
	BOC		16	23	33	
t_{PD} µP data delay (Note 1)	IVBX	C_L = 50pF		38	53	ns
	MCLK			48	61	
t_{OE} µP output enable	ME SC WC	C_L = 50pF	14	19	25	ns
t_{OD} µP output disable	ME SC WC	C_L = 50pF	13	17	32	ns
t_W Minimum pulse width	MCLK		40			ns
	BIC†		35			
t_{SETUP} Minimum setup time	UDX□	(Note 2)	15			ns
	BIC*		25			
	IVX		55			
	ME		30			
	SC		30			
	WC		30			
t_{HOLD} Minimum hold time	UDX□	(Note 2)	25			ns
	BIC*		10			
	IVX		10			
	ME		5			
	SC		5			
	WC		5			

* Applies for 8T32 and 8T33 only.
† Applies for 8T35 and 8T36 only.
□ Times are referenced to MCLK for 8T32 and 8T33, and are referenced to BIC for 8T35 and 8T36.

NOTES:

1. Data delays referenced to the clock are valid only if the input data is stable at the arrival of the clock and the hold time requirement is met.
2. Set up and hold times given are for "normal" operation. BIC setup and hold times are for a user write operaton. SC setup and hold times are for an I/O Port select operation. WC setup and hold times are for an Microprocessor Bus write operation. ME setup and hold times are for both IV write and select operations.

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DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 5\%$

PARAMETER		TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				.8	V
V_{CL}	Input clamp voltage	$I_I = -5mA$			-1	V
I_{IH}	High-level input current[1]	$V_{CC} = 5.25V$ $V_{IH} = 5.25V$		<10	100	μA
I_{IL}	Low level input current[1]	$V_{CC} = 5.25V$ $V_{IL} = .5V$		-350	-550	μA
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$ $I_{OL} = 16mA$			.55	V
V_{OH}	High-level output voltage	$V_{CC} = 4.75V$ $I_{OH} = -3.2mA$	2.4			V
I_{OS}	Short-circuit output current[2] UD bus IV bus	 $V_{CC} = 4.75V$ $V_{CC} = 4.75V$	 10 20			 mA mA
I_{CC}	Supply current	$V_{CC} = 5.25V$		100	150	mA

NOTES

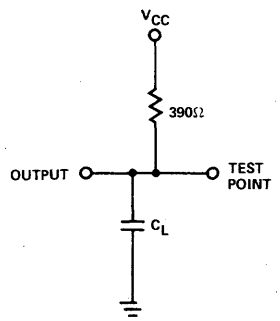
1. The input current includes the Tri-state/Open Collector leakage current of the output driver on the data lines.
2. Only one output may be shorted at a time.
3. These limits do not apply during address programming.

Absolute Maximum Ratings:

Supply voltage[3] 7V

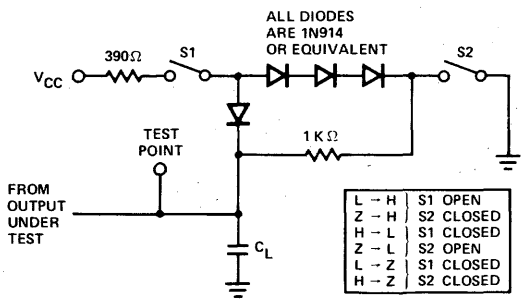
Input voltage[3] 5.5V

TEST LOAD CIRCUIT (OPEN COLLECTOR OUTPUTS)



NOTE: C_L includes fixture capacitance.

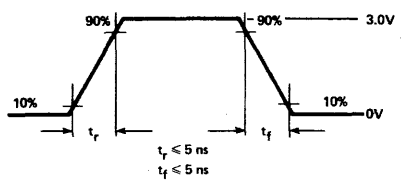
TEST LOAD CIRCUIT (TRI-STATE OUTPUTS)



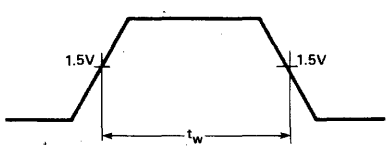
NOTE: C_L includes fixture capacitance.

VOLTAGE WAVEFORMS

INPUT WAVEFORM



CLOCK PULSE WIDTH



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ADDRESS PROGRAMMING

The I/O Port is manufactured such that an address of all high levels (>2V) on the Microprocessor Bus inputs matches the Port's internal address. To program a bit so a low-level input (<0.8V) matches, the following procedure should be used:

1. Set all control inputs to their inactive state (BIC = BOC = ME = V_{CC}, SC = WC = MCLK = GND). Leave all Microprocessor Bus I/O pins open.
2. Raise V_{CC} to 7.75V ± .25V.
3. After V_{CC} has stabilized, apply a single programming pulse to the user data bus bit where a low-level match is desired. The voltage should be limited to 18V; the current should be limited to 75mA. Apply the pulse as shown in Figure 1.
4. Return V_{CC} to 0V. (Note 1).
5. Repeat this procedure for each bit where a low-level match is desired.
6. Verify that the proper address is programmed by setting the Port's status latch (IV0-IV7 = desired address, ME = WC = L, SC = MCLK = H). If the proper address has been programmed, data presented at the μP bus will appear inverted on the user bus outputs. (Use normal V_{CC} and input voltage for verification.)

After the desired address has been programmed, a second procedure must be followed to isolate the address circuitry. The procedure is:

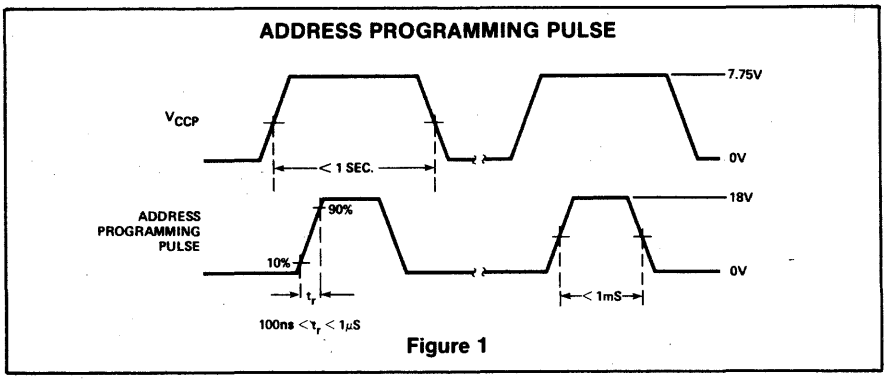


Figure 1

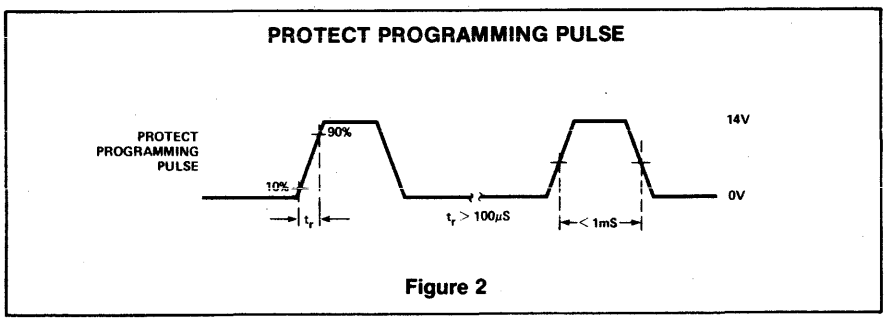


Figure 2

1. Set V_{CC} and all control inputs to 0V. (V_{CC} = BIC = BOC = ME = SC = WC = MCLK = 0V). Leave all Microprocessor Bus I/O pins open.
2. Apply a protect programming pulse to every user data bus pin, one at a time. The voltage should be limited to 14V; the current should be limited to 150mA. Apply the pulse as shown in Figure 2.
3. Verify that the address circuitry is isolated by applying 7V to each user data bus pin and measuring less than 1mA of input current. The conditions should be the same as in step 1 above. The rise time on the verification voltage must be slower than 100μs.

PROGRAMMING SPECIFICATIONS[1]

PARAMETER		TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
V_{CCP}	Programming supply voltage					
	Address		7.5		8.0	V
	Protect			0		V
I_{CCP}	Programming supply current	V_{CCP} = 8.0V			250	mA
	Max time V_{CCP} > 5.25V				1.0	s
	Programming voltage					
	Address		17.5		18.0	V
	Protect		13.5		14.0	V
	Programming current					
	Address				75	mA
	Protect				150	mA
	Programming pulse rise time					
	Address		.1		1	μs
	Protect		100			μs
	Programming pulse width		.5		1	ms

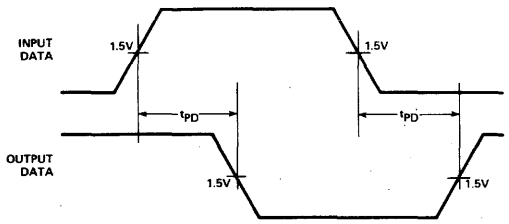
NOTE

1. If all programming can be done in less than 1 second, V_{CC} may remain at 7.75V for the entire programming cycle.

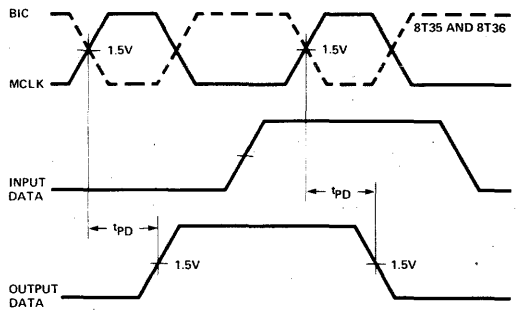
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VOLTAGE WAVEFORMS (Cont'd)

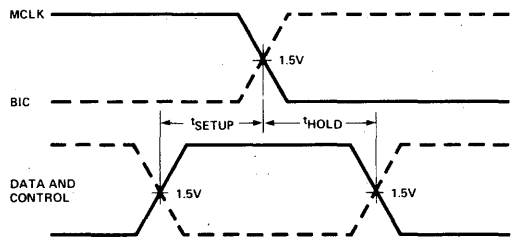
DATA DELAY TIMES
Input Data Reference



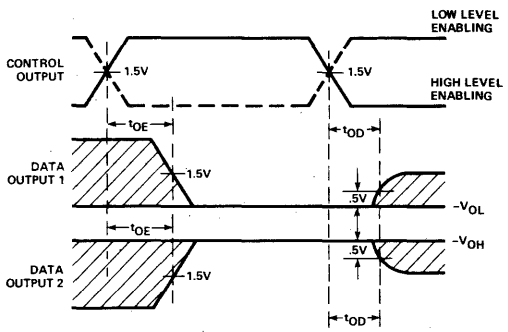
DATA DELAY TIMES
Clock Referenced



SETUP AND HOLD TIMES



OUTPUT ENABLE AND DISABLE TIMES
(Tri-State Outputs)



Waveform #1 is for an output with internal conditions such that the output is Low when the tri-state driver is enabled. Waveform #2 is for the opposite condition.

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APPLICATIONS

Figure 3 shows some of the various ways to use the I/O Port in a system. By controlling the BIC and BOC lines, the device may be used for the input and output of data, control, and status signals. I/O Port 1 functions bidirectionally for data transfer and I/O Port 2 provides a similar function for discrete status and control lines. I/O Ports 3 and 4 serve as dedicated output and input ports, respectively.

8T32 APPLICATIONS

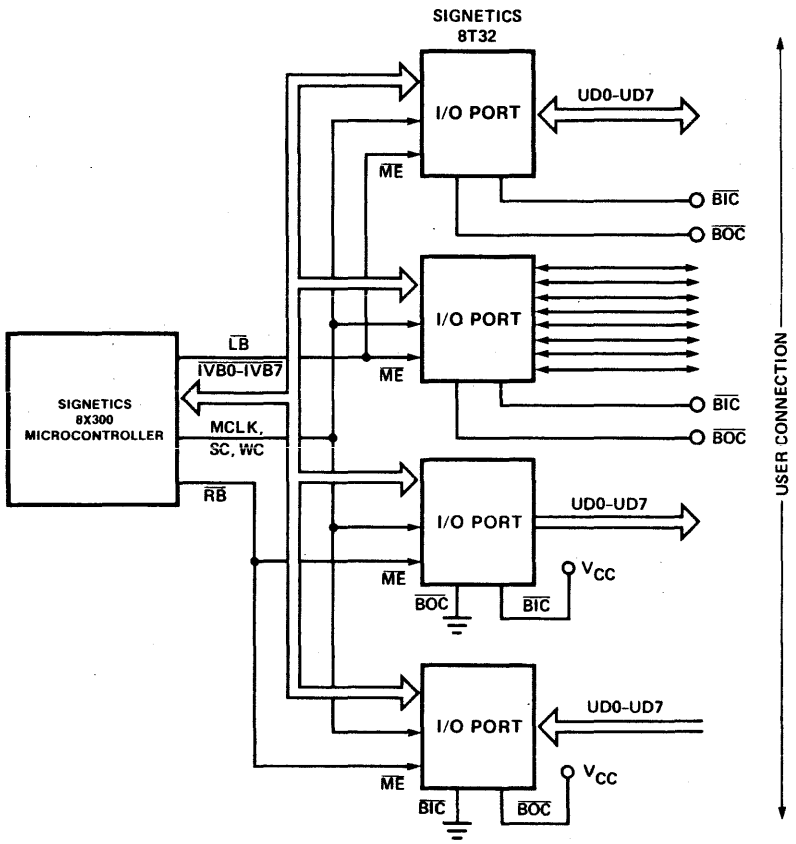


Figure 3

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PRELIMINARY SPECIFICATION 8T39-I,XL

DESCRIPTION

The Bus Expander is specifically designed to increase the I/O capability of 8X300 systems previously limited by fanout considerations. The bus expander serves as a buffer between the 8X300 and blocks of I/O devices. Each bus expander can buffer a block of 16 I/O ports while only adding a single load to the 8X300.

FEATURES

- **15ns max propagation delay**
- **Bidirectional**
- **Three-state outputs on both ports**
- **Pre-programmed address range**

APPLICATIONS

The 8T39 Bus Expander is designed to be used with the 8X300 microprocessor to allow increased I/O capability in those systems previously limited by fanout considerations. Figure 1 shows a typical arrangement of the bus expander in an 8X300 system. Each expander services I/O ports whose address is within the range of the expander. Other I/O ports or working storage may be directly connected to the bus as shown.

The bus expander is not limited to use with the 8X300, but may be applied in any system which uses a combined address/data bus.

8T39 ADDRESSING

During normal operation of the 8X300 when an I/O port address is being sent on the IV Bus (SC is high), the I/O port will examine all eight bits of the microprocessor bus for an address compare. Since the 8T39 is used to buffer blocks of I/O ports, only the four most significant bits are examined by the 8T39 for an address compare.

Note that redundant addresses are not programmed into separate devices. Rather, a discrete device (such as the 8T39-03) may be wired for any address requiring two 1 bits and two 0 bits in the address. The various address ranges for this same device are obtained by permuting the high order (DI0 and DO0 are MSB) data lines accordingly. Both input and output lines must be redefined in order to maintain data and address integrity on the extended bus. Table 1 summarizes the 8T39 addressing.

Address functions are specified with the convention that bit 0 is the MSB and bit 7 is the LSB. The DI microprocessor bus address decoding is active low.

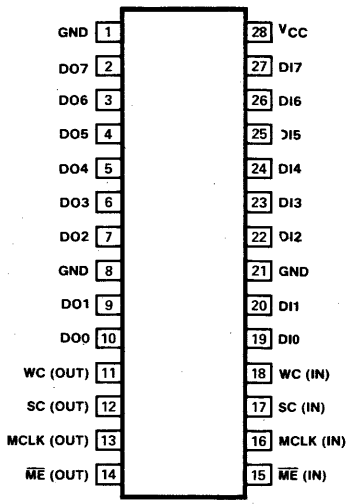
FUNCTIONAL DESCRIPTION

The Bus Expander contains eight sets of non-inverting bidirectional tri-state drivers for the bus data bits, four non-inverting unidirectional drivers for I/O port control, and necessary control logic. The control logic is required to maintain the proper directional transfer of bus data as dictated by the states of the I/O port control signals and the currently enabled I/O port. Each bus expander is programmed during manufacturing to respond to a specific block of I/O port addresses. Only I/O ports with addresses in the range of a given bus expander may be connected to that expander. A bus expander may be used on either left bank or right bank. Multiple expanders on the same bank must have different address ranges; however, expanders with the same address range can be connected if they are on different banks. Systems may be configured with I/O ports connected directly to the 8X300, as well as I/O ports connected through a bus expander; however, no unbuffered I/O port may have an address within the span of a bus expander on the same bank.

Addition of bus expanders may impact system cycle time due to the added delay in the data path. For the purposes of calculating allowable cycle time as described in the 8X300 data sheet, the bus expander delays may be considered additive to the I/O port delays so that a buffered I/O port simply appears as a slower I/O port.

PIN CONFIGURATION

I,XL PACKAGE



PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION	TYPE
2-7,9,10	DO0-DO7	I/O port data bus	Active low, three-state
11	WC(OUT)	Write command output	Active high
12	SC(OUT)	Select command output	Active high
13	MCLK(OUT)	Master clock output	Acitve high
14	$\overline{ME}$(OUT)	Master enable output	Active low
15	$\overline{ME}$(IN)	Master enable input	Active low
16	MCLK(IN)	Master clock input	Active high
17	SC(IN)	Select command output	Active high
18	WC(IN)	Write command output	Active high
19,20,22-27	DI0-DI7	Microprocessor data bus	Active low, three-state
1,8,21	GND	Ground	
28	V_{CC}	+5 volt supply	

PART TYPE	ADDRESS PATTERN MSB(0) LSB(7)	ADDRESS BLOCKS Octal
8T39-00	0000XXXX	0-17
8T39-01	0001XXXX	20-37, 40-57, 100-117, 200-217
8T39-03	0011XXXX	60-77, 120-137, 220-237, 140-157, 240-257, 300-317
8T39-07	0111XXXX	160-177, 260-277, 320-337, 340-357
8T39-17	1111XXXX	360-377

Table 1 8T39 ADDRESSING SUMMARY

signetics

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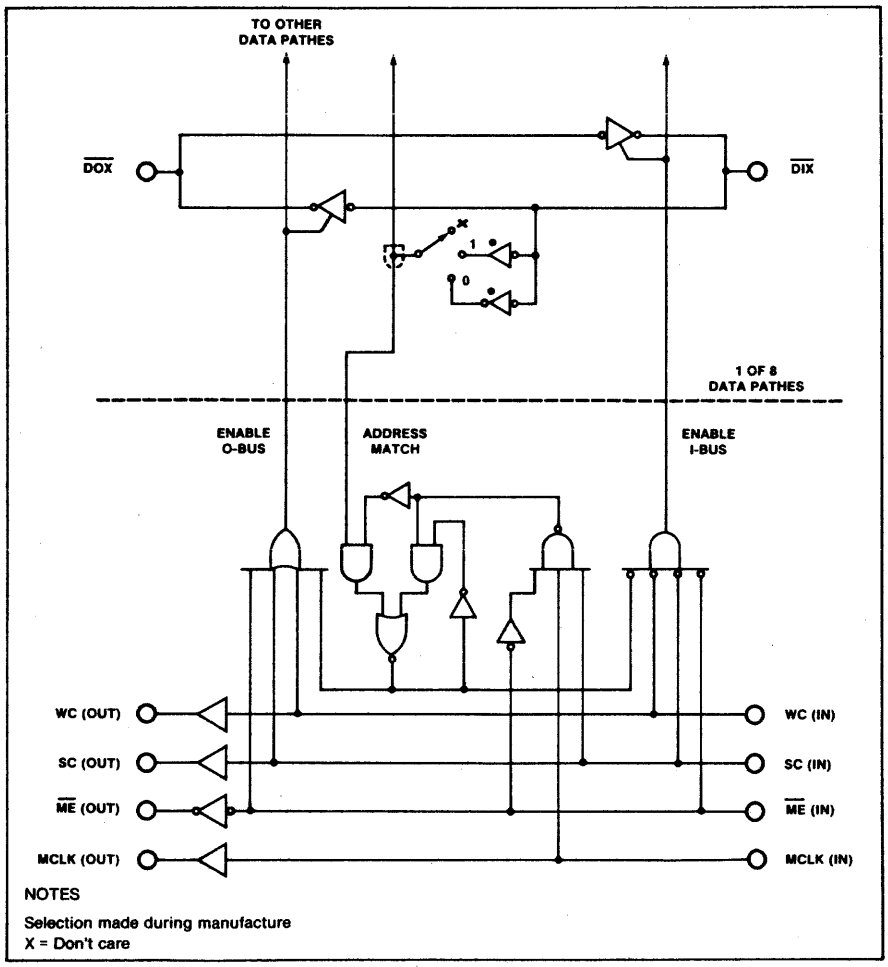
TRUTH TABLE

$\overline{ME}$	SC	WC	MCLK	SELECT LATCH	DATA TRANSFER DIRECTION	ADDRESS* COMPARISON
L	L	L	X	Set	DI Bus ← DO Bus	No
L	L	L	X	Not set	DI Bus → DO Bus	No
L	L	H	X	X	DI Bus → DO Bus	No
L	H	X	L	X	DI Bus → DO Bus	No
L	H	X	H	X	DI Bus → DO Bus	Yes
H	X	X	X	X	DI Bus → DO Bus	No

NOTES

*When an address comparison is made, the select latch is set if the data on the DI Bus is within the manufactured address range of the IV Bus Expander. Otherwise, the select latch is cleared.

FUNCTIONAL BLOCK DIAGRAM



NOTES

Selection made during manufacture
X = Don't care

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PRELIMINARY SPECIFICATION 8T39-I,XL

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-state output voltage	+5.5	Vdc
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

ORDERING INFORMATION

The Bus Expander is ordered by specifying the following part number:

N8T39-XX P

P = { I - Ceramic Package; XL - Epoxy Package

XX = Address Range As Determined From Table 1

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5%, 0°C ≤ T_A ≤ 70°C

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	Input voltage					V
V_{IL}	Low	-5mA at V_{CC} min			.8	
V_{IH}	High		2.0			
V_{IC}	Clamp				-1	
	Output voltage	V_{CC} = 4.75V				V
V_{OL}	Low	I_{OL} = 16mA			.55	
V_{OH}	High	I_{OH} = -3.2mA	2.4			
	Input current	V_{CC} = 5.25V				uA
I_{IL}	Low*	V_{IL} = .5V			-250	
I_{IH}	High*	V_{IH} = 5.25V		< 10	100	
I_{OS}	Short circuit output current	V_{CC} = 4.75V	-40			mA
I_{CC}	Supply current	V_{CC} = 5.25V			200	mA

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5%, 0°C ≤ T_A ≤ 70°C, CL^1 = 300pF[2]

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
t_{pd}	Propagation Delay Data	DOX DIX	DIX DOX				15	ns
t_{pd}	Control Propagation Delay	$\overline{ME}$ (out) MCLK (out) SC (out) WC (out)	$\overline{ME}$ (in) MCLK (in) SC (in) WC (in)				15	
t_{oe}	Data Output Enable	DIX DOX	$\overline{ME}$ (in) SC (in) WC (in)		28		56	ns
t_{od}	Data Output Disable	DIX DOX	$\overline{ME}$ (in) SC (in) WC (in)		15			ns
t_{setup}	Adverse Setup Time[3]	DIX DOX	DIX $\overline{ME}$ (in) MCLK (in) SC (in) WC (in)		54			ns
t_{hold}	Address Hold Time[3]	DIX DOX	DIX $\overline{ME}$ (in) MCLK (in) SC (in) WC (in)		3			ns

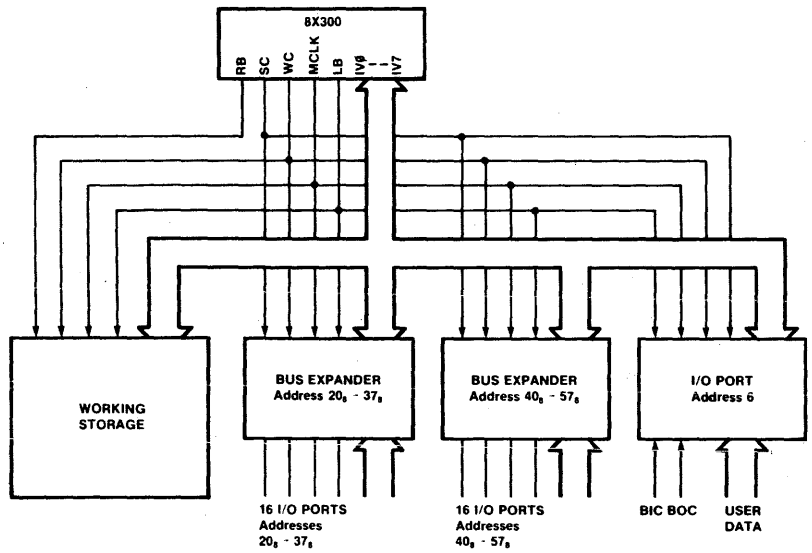
NOTES

1. Includes tri-state leakage.
2. Minimum clock width ≈ 50ns.
3. All set up and hold times are referenced to the trailing edge of the clocking input MCLK.

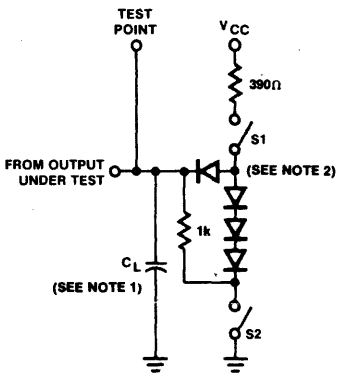
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TYPICAL APPLICATIONS

USING 2 BUS EXPANDERS TO GIVE 33 I/O PORTS PLUS WORKING STORAGE



TEST LOAD CIRCUIT



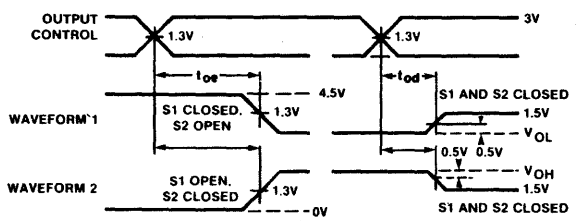
All resistors values are typical and in ohms.

NOTES

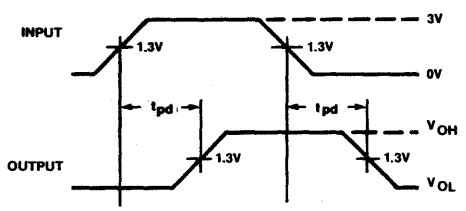
1. C_L includes probe and jig capacitance.
2. All diodes are 1N916 or 1N3064.

VOLTAGE WAVEFORMS

PROPAGATION DELAY TO THREE-STATE OUTPUTS



PROPAGATION DELAY TIMES



PRELIMINARY SPECIFICATION
Manufacturer reserves the right to make design changes and improvements.

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NE5018-F,N

DESCRIPTION

The NE5018 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches,controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

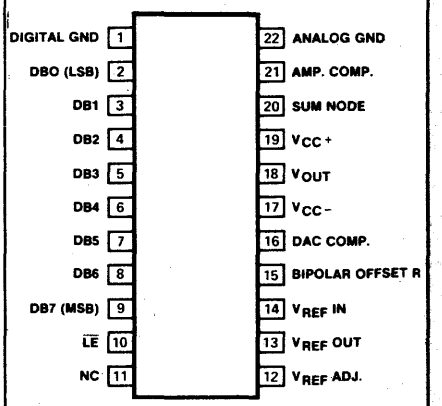
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± 1/2 LSB**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 2650, 8080 and many other μP's.**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**

PIN CONFIGURATION

F,N PACKAGE



SE5018 available in F package only.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	-18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at V_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
I_{REF}	Reference input current	5	mA
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5018	-55 to +125	°C
	NE5018	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTE

For N package, derate at 120°C/W above 35°C
For F package, derate at 75°C/W above 75°C

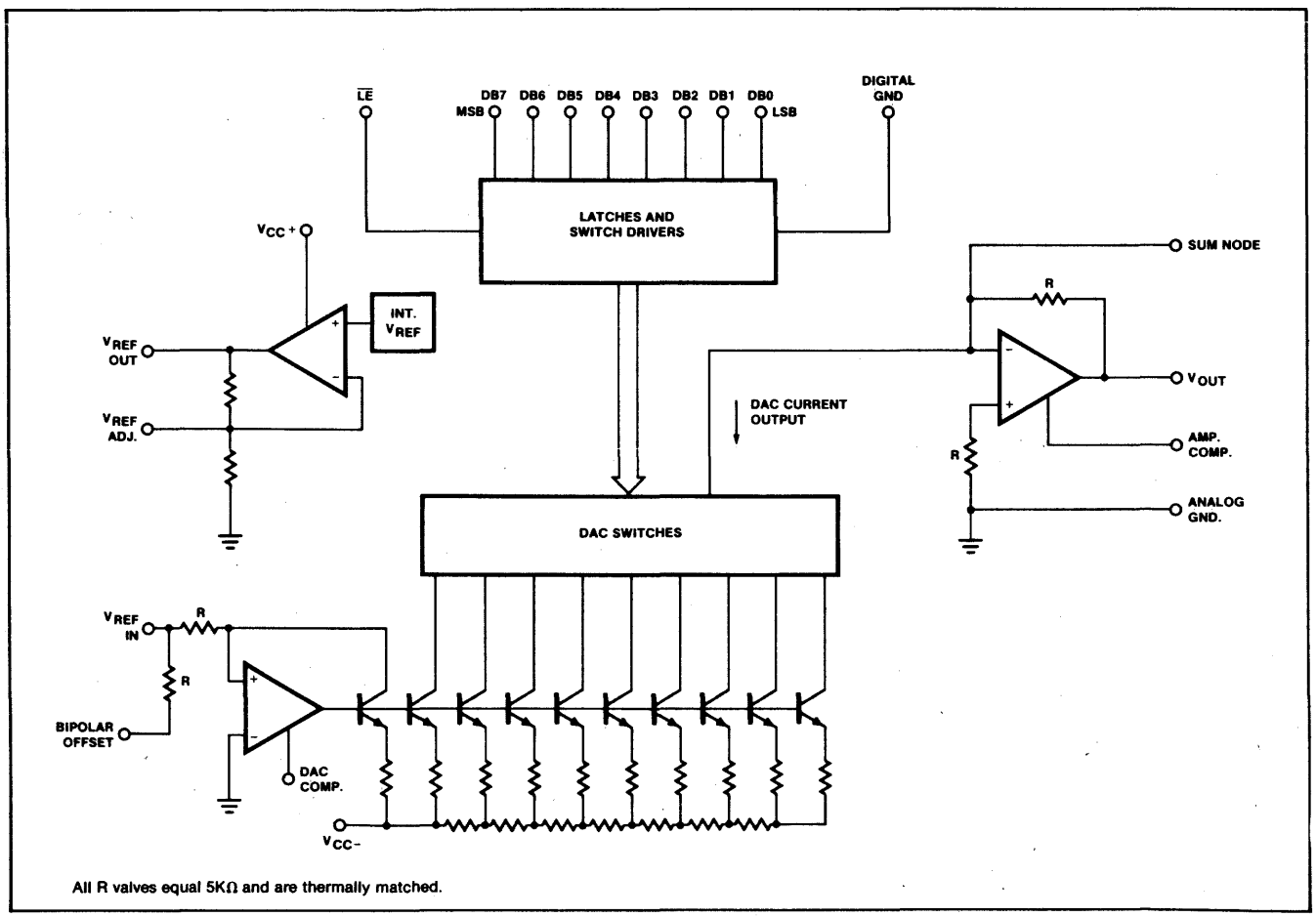
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DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = 15V$, $V_{CC}- = -15V$, SE5018. $-55°C \leq T_A \leq 125°C$, NE5018. $0°C \leq T_A \leq 70°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SE5018			NE5018			UNITS
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}+$	Positive supply voltage			15			15		V
$V_{CC}-$	Negative supply voltage			-15			-15		V
	Resolution			8			8		bits
	Relative accuracy				±0.19			±0.19	%
T_S	Settling time	To ± 1/2LSB, 10V step		2			2		μs
PSRR	Power supply Rejection ratio	$V_{CC}+$ +12 to +18V $V_{CC}-$ -12 to -18V		±1			±1		mV/V
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		8			8		mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		-10			-10		mA
$I_{IN}(0)$	Logic "0" input current	$V_{IN} = 0V$		5			5		μA
$V_{IN}(0)$	Logic "0" input voltage				0.8			0.8	V
$V_{IN}(1)$	Logic "1" input voltage		2.0			2.0			V
T_{PWLE}	Latch enable pulse width			400			400		ns

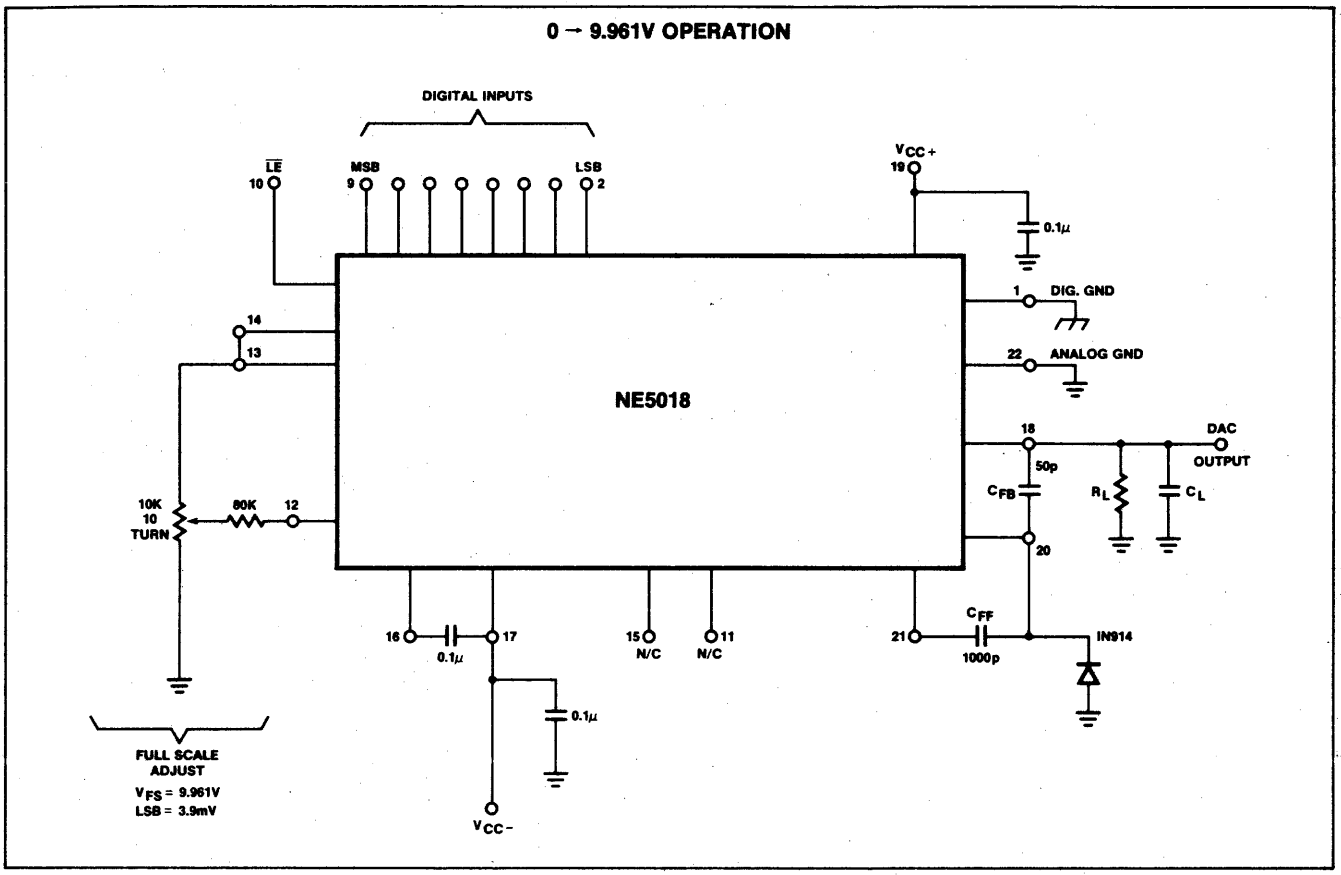
BLOCK DIAGRAM



All R valves equal 5KΩ and are thermally matched.

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EQUIVALENT SCHEMATIC

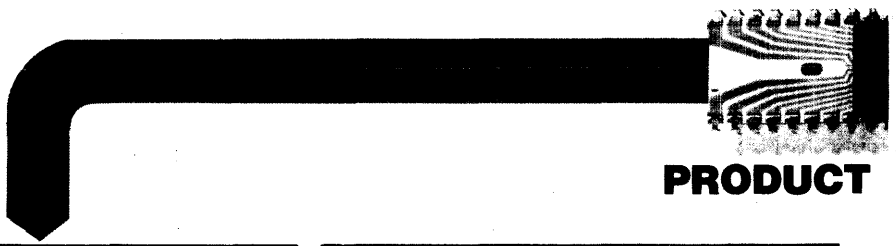


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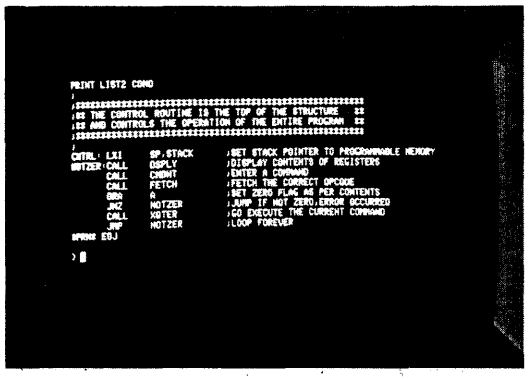
PRODUCT

PROGRAM DESIGN

Prepare detailed flow charts for optimum microprocessor operation.

CODE

Code detailed flow charts into assembly language using 8002 Microprocessor Lab's editing capabilities.



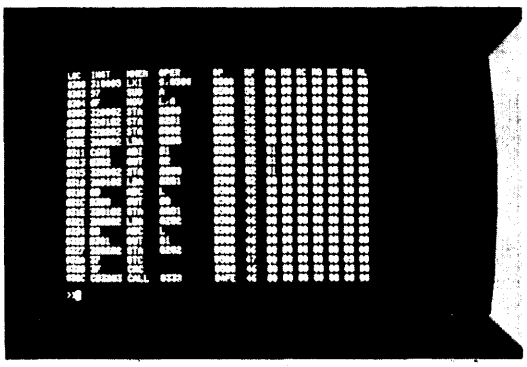
Software creation is made easy with the 8002 Microprocessor Lab's editing capabilities. TEKDOS maintains files while you concentrate on entering and revising the program.

ASSEMBLE

Assemble coded programs into machine language using 8002 Microprocessor Lab's universal assembler processor.

DEBUG

Trace and debug programs using 8002 or 8001 program emulation and debugging capabilities.



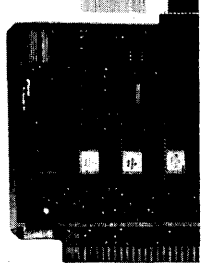
The software is executed and debugged on the prototype with the addition of the appropriate emulator processor. This dynamic trace capability enables you to trace program execution, set breakpoints, and examine memory and register contents.

CHANGE PROGRAM

NO **OK** **YES**

NO

8002/8001 Microprocessor Lab



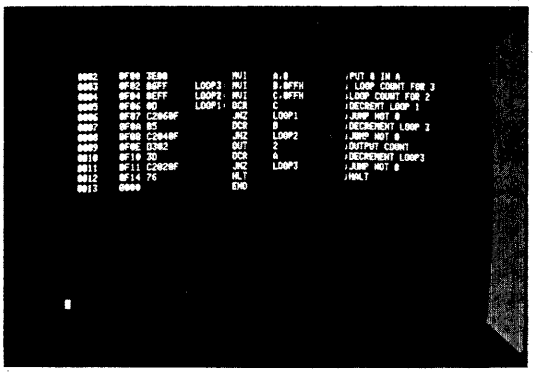
Tektronix

MICROPROCESSOR

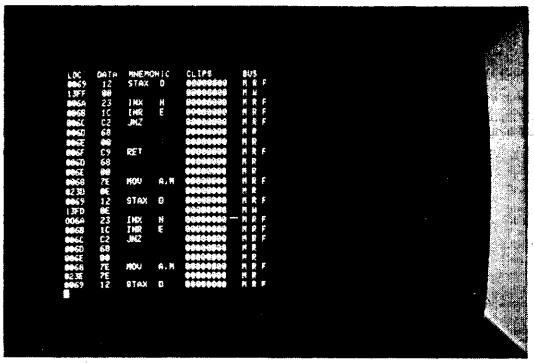
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with the 8002/8001 Microprocessor Labs

DEFINITION



Assembly into executable object code is accomplished rapidly. Corrections can be made and reassembled on the spot, too.



The real-time prototype analysis option, which enables you to fully debug hardware and software as a working unit, at operating speed, rounds out the picture.

LOGIC DESIGN

Design hardware, selecting microprocessor-support circuitry and implementing hard-wired logic functions.

BREADBOARD

Build and troubleshoot wire-wrapped breadboard using 8002 or 8001 emulator processor and prototype control probe with real-time prototype analyzer.

PROTOTYPE

Integrate hardware and software. Execute application program on prototype from 8002 or 8001 program memory using prototype control probe.

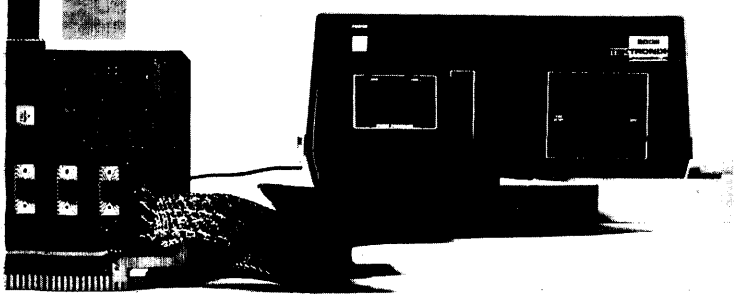
DEBUG

Verify system operation. Load program into PROM, then trace and debug system behavior using real-time prototype analyzer.

YES OK NO

WIRE LIST CHANGES

NO

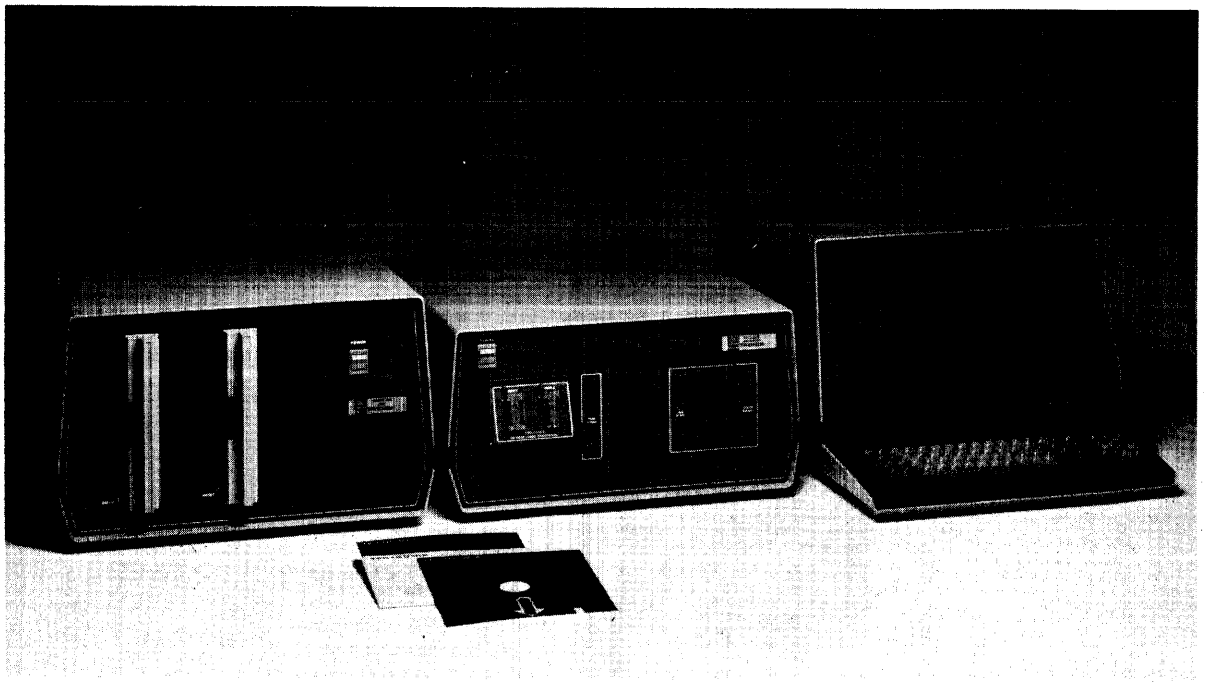


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MICROPROCESSOR

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8002 Microprocessor Lab

- **Multiple Microprocessor Support**
- **A Complete Software Development System**
- **Real-Time Trace Option**

The 8002 Microprocessor Lab consists of the 8002 Mainframe; the dual flexible disc unit; a system terminal (TEKTRONIX CT8100 or CT8101 recommended); and two sets of assembler software for two different microprocessors, chosen from the microprocessors supported at time of purchase. An emulator processor module for each microprocessor the system supports, and its associated prototype control probe, are offered as options.

The 8002 Microprocessor Lab is a complete software development system for the design of microprocessor-based products. A key feature is its ability to support many microprocessor chips, including the Intel 8085 and 8080, Motorola 6800, Texas Instruments 9900, and Zilog Z-80. The system will support other microprocessors in the future.

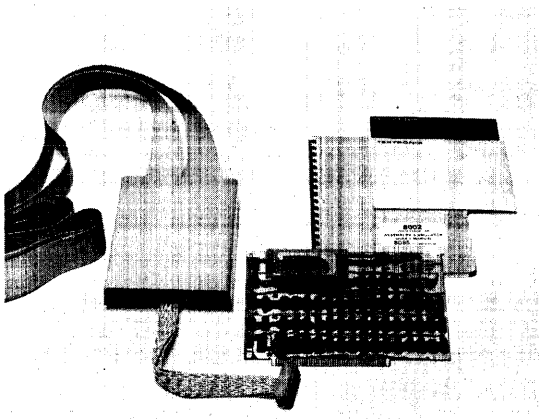
In addition to multiple microprocessor support, the 8002 offers a superior operating system and powerful text editor, assembler, and debugging programs; three optional levels of emulation for software debugging, partial and full emulation; and a real-time prototype analyzer option with all the capabilities of a microprocessor analyzer plus eight channels of external input.

Software development and debugging

In a typical design sequence, software is developed using all the resources of TEKDOS, the disc-operating system software for the 8002 Microprocessor Lab. TEKDOS performs flexible disc and file utility functions, data transfer functions, and system/peripheral device control functions. In addition to relieving the user of these housekeeping chores, TEKDOS also supervises the text editor, assembler, and linker programs and the optional emulation support, debugging system and PROM programming routines.

Program entry and editing may be accomplished module by module. The line-oriented text editor provides 150 60-character lines of buffer workspace, and offers several convenience features for preparing, correcting, and modifying the program quickly and easily. The macro assembler allows a multiple-step routine to be defined by a single command. At the end of each work session, file space is allocated by TEKDOS; duplicate files of important material may be readily created. When program entry has been completed, all program files may be merged with a single TEKDOS command.

The assembler processor, with the appropriate disc inserted in the flexible disc drive, performs program assembly functions for each microprocessor supported by the 8002.



After an error-free assembly listing has been obtained, the resulting object code may be executed in system emulation (mode 0) on the optional emulator processor. The emulator processor is identical to the microprocessor that will finally be installed in the user's prototype. Execution is performed under control of the debugging system; during execution, program steps can be traced, software breakpoints can be set, and memory can be examined and changed as required. Should an error be discovered, that portion of the program can be corrected at the source level using the text editor. It can then be reassembled and executed again. This procedure continues until the program is clean.

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Partial and Full Emulation

After the software has been partially debugged, it may be exercised on the prototype circuitry in the partial emulation mode (mode 1). During partial emulation, control may be released from the 8002 to the prototype in stages. The developmental software runs using 8002 memory space and prototype I/O and clock. The 8002 memory mapping feature allows memory to be gradually mapped over to the prototype by any combination of 128-byte address blocks. Throughout partial emulation, the user has access to prototype circuitry through the debugging system, which enables him, as before, to trace, set breakpoints, examine and change memory and register contents.

In full emulation (mode 2) the program is run on the now stand-alone prototype, but program execution is still under complete control of the debugging system. All I/O and timing functions are directed by the prototype; all memory has been mapped over to the prototype; and only the prototype control probe is still in place, emulating the target microprocessor. Although the prototype is effectively freestanding, then, the user may still direct program activity from the 8002.

Hardware Trace Option

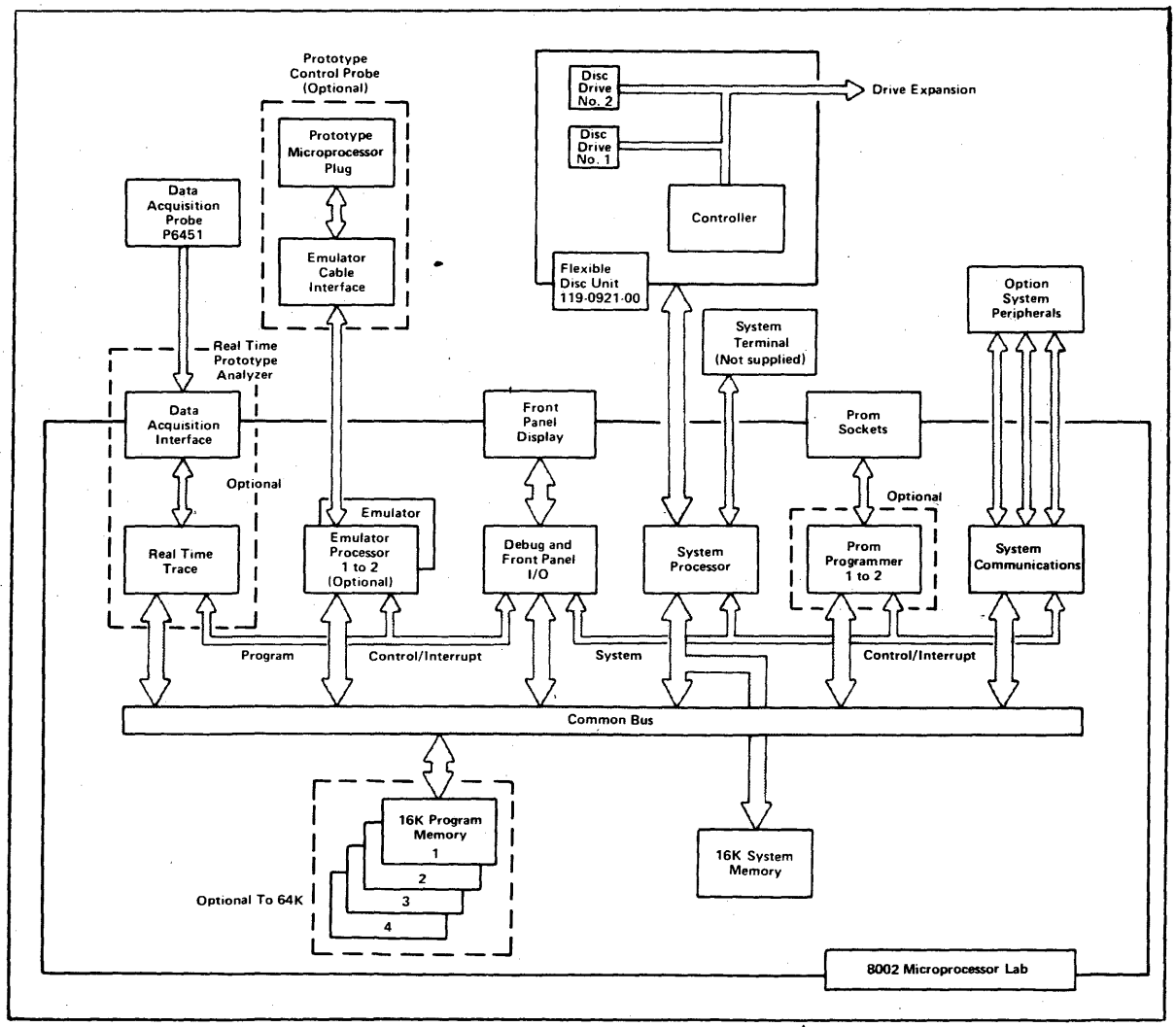
The optional real-time prototype analyzer enables the user to dynamically monitor the prototype address bus, data bus, and up to eight other locations on the prototype circuit board. Prototype activity is monitored at full speed, without stopping or slowing up the working microprocessor. This enables the designer to locate critical timing problems and hardware/software sequence problems during partial and full emulation.

In summary, then, each of the three emulation modes supports a specific phase of the product development cycle. Beginning with program entry, editing, and assembly, the designer proceeds from software debugging (mode 0), to the sequential integration of program and circuit (mode 1), to the final integration and test of the stand-alone product (mode 2). The real-time prototype analyzer enhances modes 1 and 2 by allowing the user to monitor and access prototype activity in real time.

8002 CHARACTERISTICS

The 8002 Microprocessor Lab is a modular system whose mainframe houses up to 20 plug-in circuit boards. The system includes System Processor, Debug and Front-Panel I/O; System Memory; Program Memory; System Communications; and Assembler Processor modules. A system terminal is necessary but not supplied.

Available as options are an Emulator Processor module and associated Prototype Control Probe for the microprocessor of choice to support three progressive levels of emulation. The Real-Time Prototype Analyzer module, additional 16K byte Program Memory modules, and ePROM Programmer modules for the 1702 or 2704/2708 are also available as options. Optional peripherals include the TEKTRONIX CT8100 Crt Terminal, CT 8101 TTY Terminal, and LP8200 Line Printer.



8002 SIMPLIFIED BLOCK DIAGRAM

8002 PHYSICAL CHARACTERISTICS

Dimensions	
Height	24.66 cm (9.62 in)
Width	48.31 cm (18.842 in)
Length	57.3 cm (22.347 in)
Weight	30 Kg (66 lb)

8002 ENVIRONMENTAL CHARACTERISTICS

Temperature	
Operating	0°C to +35°C (+32°F to 95°F)
Storage	Not available.
Humidity	To 90° relative noncondensing.
Altitude	
Operating	To 15,000 feet max.
Storage	To 50,000 feet max.

8002 ELECTRICAL CHARACTERISTICS

AC Input Voltages	115 V ac ±10% or 230 V ac ±10%
Frequency Range	60 Hz (50 Hz special order).
Outputs	
Dual Supply V dc	−12 V dc/+12 V dc ±5% at 3.4 A each
Single Voltage	+5.2 V dc ±5% at 25 A each
Line Regulation	
Dual Supply	±0.05% for a 10% line change.
Single Supply	±0.01% for a 10% line change.
Load Regulation	
Dual Supply	±0.05% for a 50% load change.
Single Supply	±0.05% for a 50% load change.
Output Ripple	
Dual Supply	1.5 mv p-p, 0.4 mV rms.
Single Supply	1.5 mv p-p, 0.4 mV rms.
Transient Response	
Dual Supply	30 μs for a 50% load change.
Single Supply	30 μs for a 50% load change.
Overload Protection	Automatic current limit foldback.
Adjustments	
Dual Supply	For −12 to −15, For +12 to +15 } Factory Set
Single Supply	Factory Set

Fuses	Amps	at	Volts AC
Primary	6		115
	3		230
60 V ac second.	0.5		
50 V ac second.	0.5		
±12 V dc primary.	2		115
	1		230

8002 DUAL FLEXIBLE DISC CHARACTERISTICS

Flexible Disc Unit

The Flexible Disc Unit consists of two disc drives, a controller, and power supplies. The two disc drives are designated as drive 0 and drive 1. Drive 0 is the default system drive. System programs are placed in this drive, including disc-operating system programs, the text editor, and the debugging routines peculiar to a specific Emulator Processor. Drive 1 may be used for storing user files, for modifying user files, or as a scratch data area. Drive 1 can also be designated as the system drive.

Disc Organization

Each disc contains 77 concentric tracks. Each quarter track, or block, is split into eight sectors, and each sector can contain 128 bytes. Due to directory limitations, a maximum of 72 files can be contained on one disc. The disc operating system reserves track 0 for the disc directory; tracks one through four are normally automatically reserved for system programs.

Write Protection

Each disc has a write protect slot. If the slot is covered, the disc is write enabled; if the slot is not covered, the disc is write protected. If an attempt is made to write to a write-protected disc, an error message will be displayed on the appropriate peripheral.

ENVIRONMENTAL CHARACTERISTICS

Temperature	
Operating	+10°C to +35°C (+50°F to +104°F).
Storage	Not available.
Altitude	
Operating	To 15,000 feet max.
Storage	To 50,000 feet max.
Humidity	
Operating	20%-80% relative noncondensing.
Storage	Not available.

PHYSICAL CHARACTERISTICS

Size	
Height	27 cm (10.5 in)
Width	44 cm (17.5 in)
Length	60 cm (23.62 in)
Weight	38.63 Kg (85 lb)

ELECTRICAL CHARACTERISTICS

Line Voltage	Voltage	Current
	115 V ac ±10%	3.5 A
	230 V ac ±10%	2.0 A
Line Frequency	60 Hz (50 Hz Special Order)	

Fuses	Amps	at	Volts AC
#1	4		115
	2		230
#2		Spare	
#3	2.5		115
	1.5		230
#4		Spare	

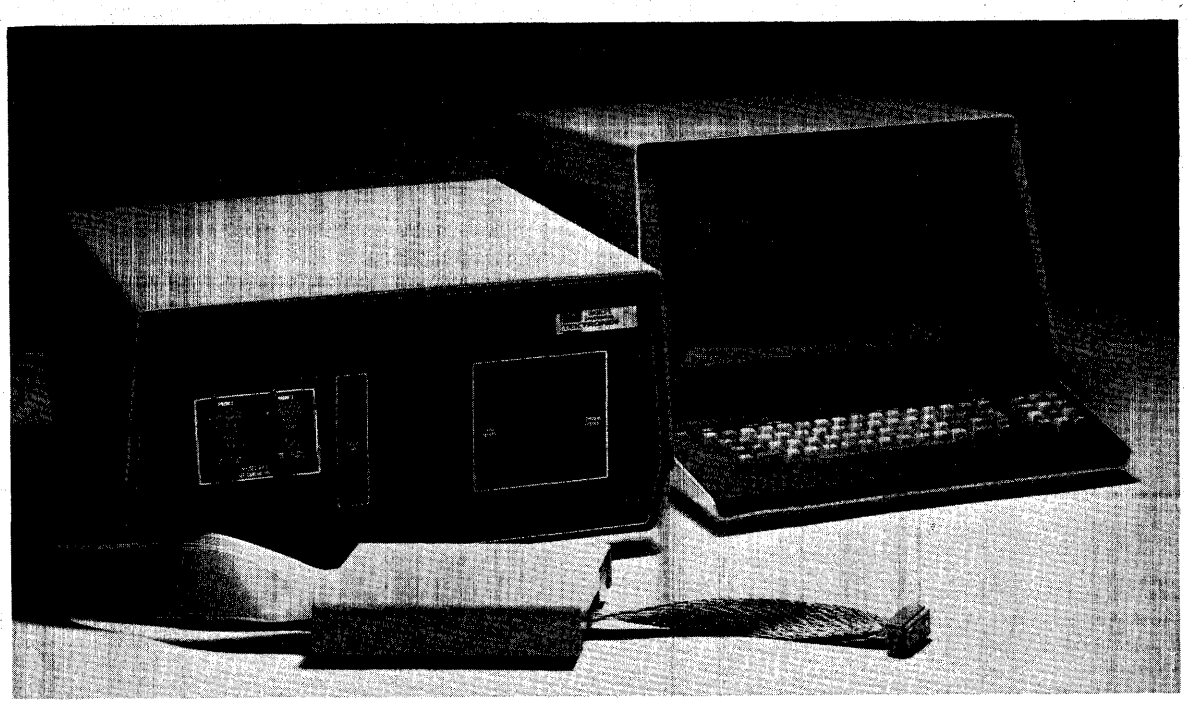
Supplies, Regulated	Current	Ripple	Regulation Within
5 V dc	6 A	1.5 mV p-p, 0.4 mV rms	±.05% for a 50% load change
24 V dc	4.8 A	4.8 mV p-p, 2.4 mV rms	±.05% for a 50% load change

Stability	±0.3% for 24 hours after warmup.
Temperature Rating of Supplies	0°-50°C full rated, derated linearly to 40% at 70°C.

FLEXIBLE DISC UNIT CHARACTERISTICS

Capacity		Bits	Bytes
Per Disc	77 x 32 x 128 x 8 bits =	2,523,136	315,392
Per Track	32 x 128 x 8 bits =	32,768	4,096
Per Sector	128 x 8 bits =	1,204	128
Access Time	10 ms/track		

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8001 Microprocessor Lab

- **Multiple Microprocessor Support**
- **A Total Hardware Debugging Environment**
- **Real-Time Trace Option**

The 8001 Microprocessor Lab consists of the 8001 Mainframe; a system terminal (TEKTRONIX CT8100 or CT8101 recommended); and a Microprocessor Support Package for the microprocessor selected. A support package includes an emulator ROM, an emulator processor, and a prototype control probe.

The 8001 Microprocessor Lab is a total hardware debugging environment for the design of microprocessor-based products. A key feature is its ability to support many microprocessor chips, including the Intel 8085 and 8080, Motorola 6800, Texas Instruments 9900, and Zilog Z-80. The system will support other microprocessors in the future.

In addition to multiple microprocessor support, the 8001 offers three emulation modes for software debugging, partial and full emulation, as well as a real-time prototype analyzer option with all the capabilities of a microprocessor analyzer plus eight channels of external input.

Three Emulation Modes

In a typical design sequence, software is first developed independently using time-sharing, a minicomputer, or some other means. It is then downloaded to the 8001. At this point the in-prototype emulation and software/hardware integration capabilities of the 8001 come into play.

In emulation mode 0, the software runs only on the emulator processor. This enables the program to be debugged on a microprocessor identical to the one that will ultimately be used in the completed product. In emulation modes 1 and 2, the prototype control probe is connected to the emulator processor at one end and plugged into the empty microprocessor socket in prototype circuitry at the other.

Partial emulation (mode 1) lets the user release control in methodical steps from the 8001 to the prototype. The developmental software runs using 8001 memory space and prototype I/O and clock. The 8001 memory mapping feature allows memory to be gradually mapped over to the prototype by address blocks. Throughout partial emulation, the user has access to prototype circuitry via the powerful 8001 debugging system software, which enables him to trace, set breakpoints, examine and change memory and register contents.

Full emulation (mode 2) lets the user exercise the program on the now stand-alone prototype while still maintaining complete control through the Microprocessor Lab. All I/O and timing functions are directed by the prototype; all memory has been mapped over to the prototype; and only the prototype control probe is still in place, emulating the target microprocessor. Although the prototype is effectively freestanding, then, the user may still direct program activity from the Microprocessor Lab.

Hardware Trace Option

The optional real-time prototype analyzer enables the user to dynamically monitor the prototype address bus, data bus, and up to eight other locations on the prototype circuit board. Prototype activity is monitored at full speed, without stopping or slowing up the working microprocessor. This enables the designer to locate critical timing problems and hardware/software sequence problems during partial and full emulation.

In summary, then, each of the three emulation modes supports a specific phase of the product development cycle. Beginning with assembled source language, the designer proceeds from software debugging (mode 0), to the sequential integration of program and circuit (mode 1), to the final integration and test of the stand-alone product (mode 2). The real-time prototype analyzer enhances modes 1 and 2 by allowing the user to monitor and access prototype activity in real time.

8001 CHARACTERISTICS

The 8001 Microprocessor Lab is a modular system whose mainframe houses up to 20 plug-in circuit boards. The system includes System Processor, Debug and Front-Panel I/O, Program Memory, System Communications, and System Memory modules. Also provided are an Emulator Processor module for the microprocessor of choice, its associated prototype control probe, and a ROM-based software module. Additional emulator processor packages are available as options for each microprocessor the system supports. A system terminal is necessary but not supplied.

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The Real-Time Prototype Analyzer module, additional 16K byte Program Memory modules, and ePROM Programmer modules for the 1702 or 2704/2708 are available as options. Optional peripherals include the TEKTRONIX CT8100 Crt Terminal, CT8101 TTY Terminal, and LP8200 Line Printer.

8001 PHYSICAL CHARACTERISTICS

Dimensions	
Height	24.66 cm (9.62 in)
Width	48.31 cm (18.842 in)
Length	57.3 cm (22.347 in)
Weight	30 Kg (66 lb)

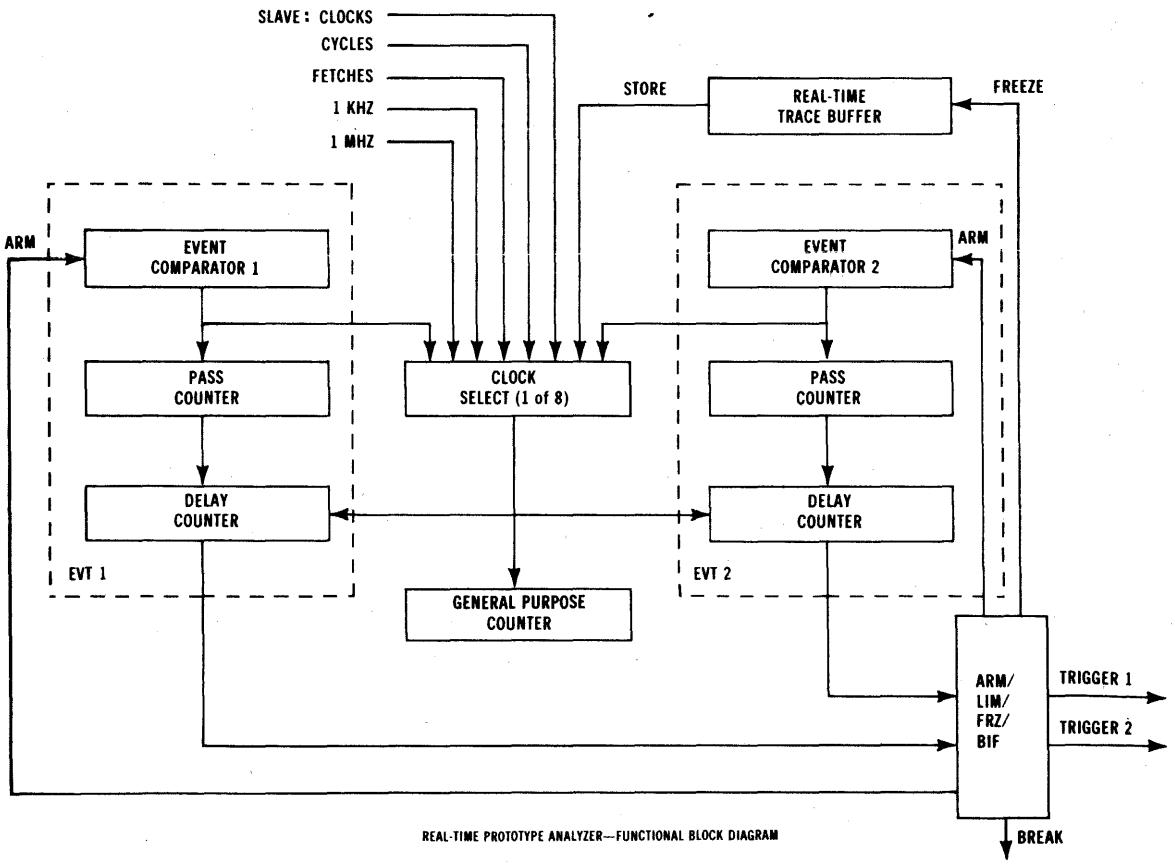
8001 ENVIRONMENTAL CHARACTERISTICS

Temperature	
Operating	0°C to +35°C (+32°F to 95°F)
Storage	Not available.
Humidity	To 90° relative noncondensing.
Altitude	
Operating	To 15,000 feet max.
Storage	To 50,000 feet max.

8001 ELECTRICAL CHARACTERISTICS

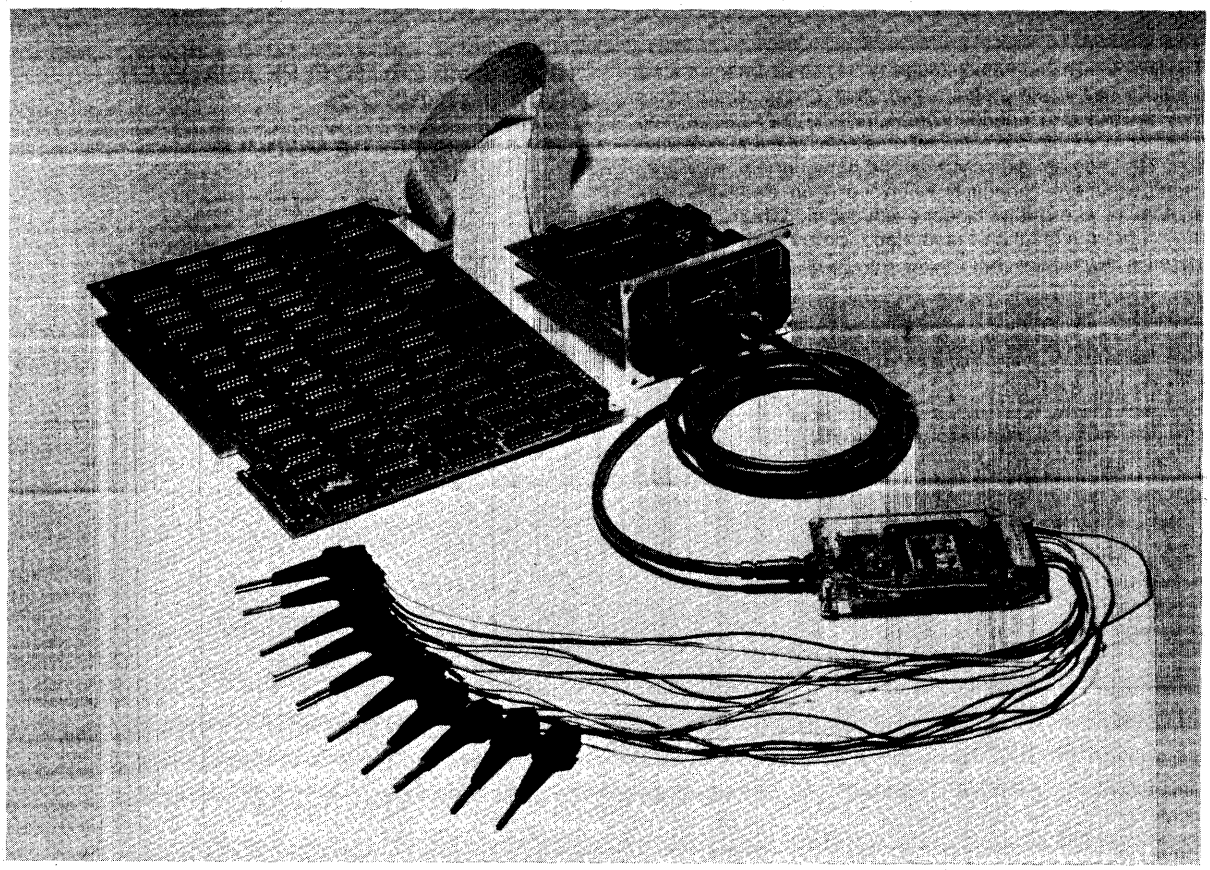
AC Input Voltages	115 V ac ±10% or 230 V ac ±10%
Frequency Range	60 Hz (50 Hz special order).
Outputs	
Dual Supply Vdc	−12 V dc to +12 V dc ±5%
Dual Supply Adc	3.4/3.4 A
Single Voltage	+5.2 V dc ±5%
Single Current	25 A
Line Regulation	
Dual Supply	±0.05% for a 10% line change.
Single Supply	±0.01% for a 10% line change.
Load Regulation	
Dual Supply	±0.05% for a 50% load change.
Single Supply	±0.05% for a 50% load change.
Output Ripple	
Dual Supply	1.5 mv p-p, 0.4 mV rms.
Single Supply	1.5 mv p-p, 0.4 mV rms.
Transient Response	
Dual Supply	30 μs for 50% load change.
Single Supply	30 μs for 50% load change.
Overload Protection	Automatic current limit foldback.
Adjustments	
Dual Supply	For −12 to −15, For +12 to +15 } Factory Set
Single Supply	None.

Fuses	Amps	at	Volts AC
Primary	6		115
	3		230
60 V ac second.	0.5		
50 V ac second.	0.5		
±12 V dc primary.	2		115
	1		230



REAL-TIME PROTOTYPE ANALYZER—FUNCTIONAL BLOCK DIAGRAM

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REAL-TIME PROTOTYPE ANALYZER

The Real-Time Prototype Analyzer, Option 46 for the 8002 and 8001 Microprocessor Labs, is comprised of the Real-Time Trace Module, Data Acquisition Interface, and 8-Channel Data Acquisition Probe. This option provides a real-time trace of the user program executing on the emulator processor, plus eight concurrent channels from any location on the user hardware probe input. The emulator address bus, data bus, control bus, and the eight external signals in the prototype circuit may be monitored without stopping or slowing up the working microprocessor.

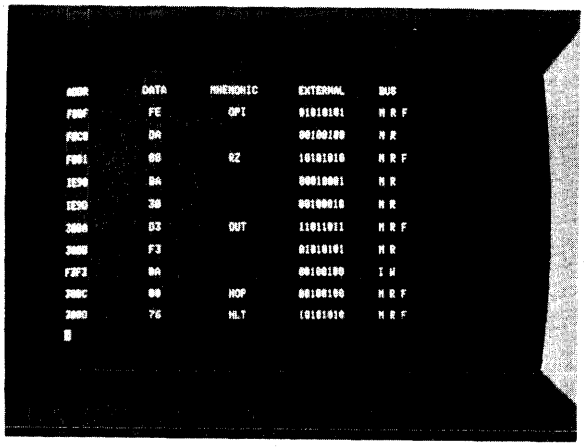
The analyzer module is a separate plug-in circuit card that may be inserted into either the 8002 or 8001 System Mainframe. The P6451 Probe connects to the prototype circuitry and permits data transference from the prototype to the analyzer. Data from the prototype is buffered and driven by the probe to the data acquisition interface, and then loaded into the analyzer module's real-time trace buffer.

As the user program is executed by the emulator processor, 48-bit data words are sequentially acquired from the prototype and loaded into the real-time trace buffer. Each data word contains 16-bit data from the address bus; 8-bit or 16-bit data from the data bus; 8-bit data from the test probe; 3-bit data identifying cycle type (read, write, I/O, memory, or instruction fetch); and 5-bit data used internally to identify last start/stop of the emulator. The analyzer will continue to acquire these sequential cycles of logic input until the processor is stopped or the real-time trace buffer is frozen by a specified trigger occurrence. The real-time trace buffer can retain up to 128 data words in pre, variable center, or post trigger modes; thus enabling the storage of pertinent program bus transactions.

A general-purpose delay counter times program execution in clock or event cycles to enable the analysis of critical timing measurements. Count units may be designated as bus instruction fetches, bus cycles, real-time trace stores, microseconds, milliseconds, or any event trigger. As the program executes, the counter keeps track of the number of count units which take place. The current count value may be displayed after the processor is stopped by entering the CNT command from the system terminal.

The Real-Time Prototype Analyzer offers expanded breakpoints to aid in efficient location of prototype problems. Two event comparators located within the analyzer module can be utilized to halt program execution and stop real-time trace. A trigger may be generated on any specific data occurrence in the address bus, data bus, test probe input, and instruction cycle type. Triggering may be immediate; delayed by counting the number of passes; or delayed by counting the number of clock select outputs (clock select may be by microseconds, milliseconds, emulator clocks, etc.). In addition, an output pulse may be generated, via the data acquisition interface, to trigger a logic analyzer or an oscilloscope.

The two event comparators (triggers) may be set to designate a break or halt in the program execution. These comparators may be used as independent breakpoints; or they may be used together to enable a breakpoint on a specific event combination. The program execution can be halted when two trigger events occur simultaneously; when one trigger event precedes another; or when either trigger event occurs. When a break in the program execution takes place, program transactions stored in the real-time trace buffer may be displayed or printed.



Data stored in the real-time trace buffer is displayed sequentially in the order it was acquired from the prototype. Buffer content may be displayed in whole or in part. Optional command parameters are available to limit the storing of data to any specific transaction type, such as memory reads only. If the total buffer contents are displayed, a blank line will separate data sequence associated with each program starting point.

The Real-Time Prototype Analyzer features a convenient and easy-to-understand display format. With this format the address location, data, probe input, and control bus data of each acquired transaction are displayed. If the transaction was an instruction fetch, the instruction is also disassembled into the appropriate memonic readout unique to the emulator type being used.

The Real-Time Prototype Analyzer functions in all emulation modes and operates with all commercial microprocessors supported by the 8002 and 8001 Microprocessor Labs.

REAL-TIME PROTOTYPE ANALYZER CHARACTERISTICS

REAL-TIME TRACE MODULE

ELECTRICAL CHARACTERISTICS

Voltage	Current.
+5.2 V dc	2.4 A typical.
Dissipation	Approx 12.5 W.

ENVIRONMENTAL CHARACTERISTICS

Ambient Air Temperature	
Operational	0° C to +70°C (+32°F to +158°F)
Storage	−55°C to +80°C (−67°F to +167°F)
Humidity	To 90% relative noncondensing.
Altitude	
Storage	To 50,000 feet max.
Operating	To 15,000 feet max.

DATA ACQUISITION INTERFACE

ELECTRICAL CHARACTERISTICS

Power	Typical	Max.
+12V dc	20 mA	—
−12V dc	—	400 mA with P6451 Data Acquisition Probe attached. 125 mA without P6451 Data Acquisition Probe.
+5.2 Fdc	—	400 mA
Dissipation	Approx 7 W.	

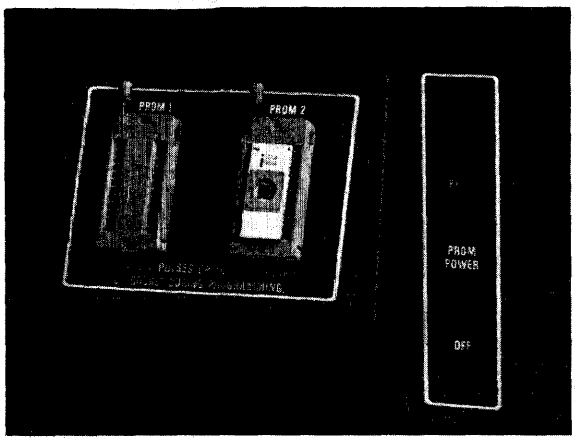
PHYSICAL CHARACTERISTICS

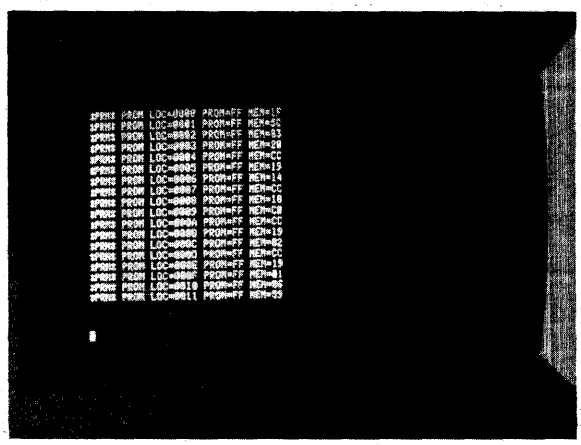
Dimensions	
Circuit Board	10.5 cm x 12.14 cm (4.09 in x 4.83 in)
Overall Length	12 cm (4.68 in)
Rear Panel	11.2 cm x 6.1 cm (4.36 in x 2.37 in)
Cable Length	50 cm (19.5 in)

INPUT/OUTPUT CHARACTERISTICS

Variable Threshold Range	>+10 V dc to <−10 v dc
Preset TTL Voltage	+1.4 V dc ± 200 mV
Event Trigger Out	High level voltage out (when Vcc = min, Vi = 0.5, Ro = 50 Ω to GND) is >2 V dc.
Adjustments	Variable threshold may be adjusted from >+10 V dc to <−10 V dc with a screwdriver adjustment accessible at the rear panel of the Microprocessor Lab. This voltage must be monitored with a voltmeter having an input impedance of at least 10 MΩ.
Jumpers	With the internal jumper in position '0-3' the clock threshold is designated to be the same as channels 0-3. In position '4-7' the jumper designates the clock threshold to be the same channels 4-7.

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PROM PROGRAMMER

The 1702 and 2704/2708 PROM Programmer options, each consisting of a circuit card module and supporting software, provide the ability to program either 1702A or 2704/2708 erasable PROM chips. When the module is installed in an 8002 or 8001 Microprocessor Lab mainframe, the PROM Programmer software enables communication between 8001 or 8002 program memory and the PROM installed in the front-panel PROM programming porch.

Before programming the 1702A PROM, all bits are set to 0. Programming is performed by writing Is to selected bits. Address and data are applied to the appropriate pins and each address is cycled through the write sequence until the PROM is completely programmed.

Programming a 2704/2708 PROM is identical to the procedure for the 1702A PROM, except that bit settings are reversed. Programming is accomplished by setting selected bits to 0.

After programming, the PROM can only be erased by exposure to an ultraviolet light source. The transparent PROM cover allows ultraviolet light to reset all bits to their original setting, high or low. The PROM can then be programmed again.

1702A or 2704/2708 PROM Programmer software transfers one data byte at a time, and actual addresses are assigned. Data may be written from 8002 or 8001 program memory (WPROM); read from PROM into program memory (RPROM); or compared on the system terminal (CPROM).

For a write operation (WPROM), the data for each byte to be written is sent to either the 1702 or 2704/2708 PROM Programmer from the program memory module. The PROM Programmer then executes a programming sequence for that byte.

The RPROM command allows the programmed PROM to be read into program memory and dumped onto a console display.

The CPROM compare function performs an address-by-address comparison between the PROM and the program under development. When an inequality between PROM bytes and memory bytes occurs, the memory address, memory byte content, and PROM byte content are displayed on the system console. A successful comparison between designated PROM and memory bytes is indicated by an End of Job message on the console.

1702A PROM PROGRAMMER CHARACTERISTICS

Power	Typical	Maximum
+5 V dc	0.9 A	1.2 A
+12 V dc	60 mA	90 mA
−12 V dc	40 mA	70 mA
50 V ac		0.3 A peak
Dissipation	Approx. 15 W	
Fuses		
50 V ac	0.5 A 250 V located on the rear panel of the Microprocessor Lab	
Adjustments	+47 V dc is adjusted with a potentiometer located on the top edge PROM Programmer module	
Ambient Air Temperature		
Operational	0°C to +70°C (32°F to +158°F).	
Storage	−55°C to +80°C (−67°F to +167°F).	
Humidity	To 90% relative noncondensing.	
Altitude		
Storage	To 50,000 ft max.	
Operating	To 15,000 ft max.	

2704/2708 PROM PROGRAMMER CHARACTERISTICS

Power	Typical	Maximum
+5.2	1.09 A	1.2 A
+12 V dc	36 mA	50 mA
−12 V dc	70 mA	90 mA
30 V ac	68 mA	85 mA
15 V ac	105 mA	150 mA
Dissipation	Approx. 7 W	
Ambient Air Temperature		
Operational	0°C to +70°C (+32°F to +58°F)	
Storage	−55°C to +80°C (−67°F to +167°F)	
Humidity	To 90% relative noncondensing.	
Altitude		
Operating	To 50,000 ft max.	
Storage	To 15,000 ft max.	

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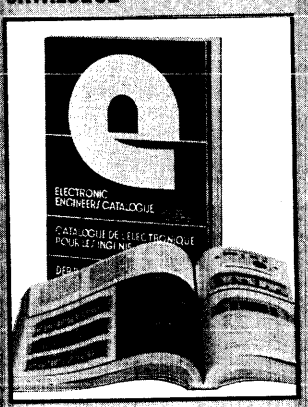
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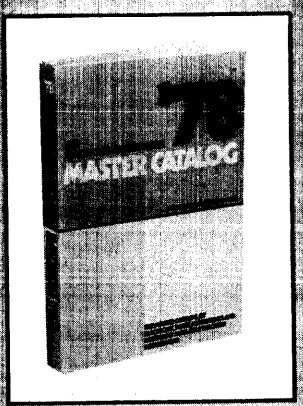
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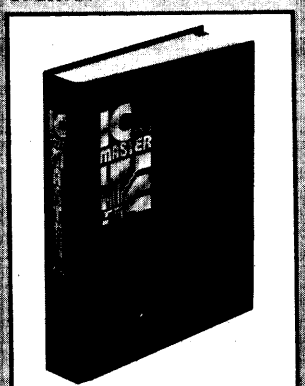
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how to use the alternate source directory

The second column of this Alternate Source Directory shows devices which are replacements for those in the first column. Devices listed in **BOLD FACE** type have technical data in the Master Selection Guide. This information begins on the page listed to the right of the **BOLD FACE** part numbers. Products preceded by a ♦ have been discontinued by the manufacturer. This section does include devices not listed in the Master Selection Guide; e.g., discontinued items, DTL and 54L devices.

This list is compiled from manufacturers' recommendations. Since there is a tendency for every company to only show itself as an alternate to the prominent manufacturers, and for the larger ones to ignore the little ones, not every device is referenced both ways to every other one. Therefore, if you are looking for alternates to a lesser known company's device, take the replacements you find, especially if they are made by prominent companies and look them up to see if you can find any other sources.

In order to maintain this list within some reasonable bounds, the A and B suffixes indicating improved versions generally have been dropped. If this weren't done, for example, every higher speed selection conjured up by a memory manufacturer would result in a device that could replace many equal or slower competitors and this directory would become highly involved in slight performance variations. Moreover, improved performance is only important if your circuits take advantage of it.

One of the difficulties with any cross reference is that devices meant to be alternates do not necessarily perform the same in all circuits. Thus, it will be necessary for you to check specifications, or even to check circuit performance before deciding which alternates are right for you. A major benefit of this list is that it gives you more alternatives to study. But if you don't find what you need here, it may be possible to find additional alternates by locating the device in the Master Selection Guide. Particularly for digital circuits, the other products grouped with it will normally offer similar or identical performance.

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Advanced Micro Devices

Manufacturer Device	Replacement Source	Device	IC Master Page
♦AM2071	Signetics	82S07	
AM25LS07	Motorola	SN74LS378	
	TI	SN54LS378	
		SN74LS378	
AM25LS08	Motorola	SN74LS379	
	TI	SN54LS379	
		SN74LS379	
AM25LS09	Motorola	SN74LS399	
	TI	SN54LS399	
		SN74LS399	
AM25LS138	National	DM54LS138	
		DM74LS138	
	Raytheon	25LS138	
AM25LS139	National	DM54LS139	
		DM74LS139	
	Raytheon	25LS139	
AM25LS14	Motorola	SN74LS384	
	Raytheon	**25LS14**	**293**
AM25LS15	Motorola	SN74LS385	
	Raytheon	**25LS15**	**295**
AM25LS151	National	DM54LS151	
		DM74LS151	
	Raytheon	25LS151	
AM25LS153	National	DM54LS153	
		DM74LS153	
	Raytheon	25LS153	
AM25LS157	National	DM54LS157	
		DM74LS157	
	Raytheon	25LS157	
AM25LS158	National	DM54LS158	
		DM74LS158	
	Raytheon	25LS158	
AM25LS160	National	DM54LS160	
		DM74LS160	
	Raytheon	25LS160	
AM25LS161	National	DM54LS161	
		DM74LS161	
	Raytheon	25LS161	
AM25LS162	National	DM54LS162	
		DM74LS162	
	Raytheon	25LS162	
AM25LS163	National	DM54LS163	
		DM74LS163	
	Raytheon	25LS163	
AM25LS164	National	DM54LS164	
		DM74LS164	
AM25LS170	Raytheon	25LS170	
AM25LS174	National	DM54LS174	
		DM74LS174	
	Raytheon	25LS174	
AM25LS175	National	DM54LS175	
		DM74LS175	
	Raytheon	25LS175	
AM25LS181	National	DM54181	
		DM74181	
	Raytheon	25LS181	
AM25LS190	National	DM54LS190	
		DM74LS190	
	Raytheon	25LS190	
AM25LS191	National	DM54LS191	
		DM74LS191	
AM25LS192	Raytheon	25LS192	
AM25LS193	National	DM54LS193	
		DM74LS193	
	Raytheon	25LS193	
AM25LS194A	Raytheon	25LS194A	
AM25LS195	Raytheon	25LS195	
AM25LS22	Motorola	SN74LS322	
	Raytheon	**25LS22**	**297**
	TI	SN54LS322	
		SN74LS322	
AM25LS23	Motorola	SN74LS323	
	Raytheon	**25LS23**	**300**
	TI	SN54LS323	
		SN74LS323	
AM25LS241	Raytheon	25LS241	
AM25LS251	Raytheon	25LS251	
AM25LS2518	Motorola	SN74LS388W	♦
AM25LS253	Raytheon	25LS253	
AM25LS257	National	DM54LS257	
		DM74LS257	
AM25LS258	National	DM54LS258	
		DM74LS258	
AM25LS258	Raytheon	25LS258	
AM25LS299	Raytheon	25LS299	
AM25LS670	Raytheon	25LS670	
AM25L02	National	DM2502	
AM25L03	National	DM2503	
AM25L04	National	DM2504	
AM2502	Intersil	2502	
	National	DM2502	
AM2503	Intersil	2503	
	National	DM2503	
AM2504	Intersil	2504	
	National	DM2504	
AM2505	Raytheon	RC2505	
		RM2505	
	Signetics	2505	
AM26LS31	TI	AM26LS31	
AM26LS32	TI	AM26LS32	
AM26L02	National	DM8602	
		DM9602	
AM26L123	National	DM54L123	
		DM74L123	
AM26S02	National	DM8602	
		DM9602	
AM26S10	Fairchild	9640	
	Motorola	MC26S10	
	Raytheon	26S10	
	TI	AM26S10	
AM26S11	Fairchild	9641	
	Motorola	MC26S11	
	Raytheon	26S11	
	TI	AM26S11	
AM2602	National	DM8602	
		DM9602	
AM26123	National	DM54123	
		DM74123	
	TI	SN54123	
		SN74123	
AM27LS00	Fairchild	93421	
	National	DM54S200	
		DM74S200	
	NEC Micro	μPB2202	
		μPD2200	
	TI	SN74LS200	
AM27LS01	Fairchild	93411	
	National	**DM54S206**	**1297**
		DM74S206	**1297**
	NEC Micro	μPB2206	
AM27LS10	Fairchild	93416	
	Harris	HPROM1024	
	Intel	3601	
	NEC Micro	**μPB403**	**1462**
AM27S02	Fairchild	93404	
	MMI	5560	
		6560	
	National	DM54S289	
		DM74S289	
	NEC Micro	μPB2089	
	TI	SN54S289	
		SN74S289	
AM27S03	Fairchild	93405	
	MMI	5561	
		6561	
	National	**DM54S189**	**1292**
		DM74S189	**1292**
		DM7599	
		DM8599	
	TI	SN54S189	
		SN74S189	
AM27S06	**Harris**	**HM7602**	**1192**
	National	DM7577	
		DM8577	
	Signetics	82S23	
	TI	SN54S288	
		SN74S288	
AM27S10	**Harris**	**HM7610**	**1192**
		HM7610A	**1200**
	Intel	M3601	
		3601	
	National	**DM54S387**	**1264**
		DM74S387	**1264**
AM27S10	**NEC Micro**	**μPB403**	**1462**
	TI	SN54S387	
		SN74S387	
AM27S11	**Harris**	**HM7611**	**1192**
		HM7611A	**1200**
	Intel	M3621	
		3621	
	National	**DM54S287**	**1264**
		DM74S287	**1264**
	NEC Micro	μPB423	
	TI	SN54S287	
		SN74S287	
AM27S80	**NEC Micro**	**μPB408**	**1491**
AM27S81	**NEC Micro**	**μPB428**	**1491**
AM2700	Fairchild	93421	
	MMI	6531	
	Signetics	N82S16	
		82S06	
	TI	SN54S201	
		SN74S200A	
		SN74S201	
AM2701	Fairchild	93411	
	MMI	6530	
	Signetics	82S17	
	TI	SN54S301	
		SN74S300	
		SN74S301	
AM2802	Synertek	SY2802	
AM2803	Synertek	SY2803	
AM2804	Synertek	SY2804	
AM2806	Signetics	2512	
AM2807	Signetics	2524	
AM2808	Signetics	2525	
AM2809	Signetics	2521	
AM2814	TI	TMS3114	
AM2825	Synertek	SY2825	
AM2826	Synertek	SY2826	
AM2827	Synertek	SY2827	
AM2833	Signetics	2533	
	Synertek	SY2833	
AM2901A	Fairchild	F2901	
		9409	
	Motorola	MC2901	
	National	**IDM2901A**	
			1656,1680
	NEC Micro	**μPB2901**	**1850**
	Raytheon	AM2901A	
	Signetics	**N2901**	**1851**
AM2902	Motorola	MC2902	
	National	IDM2902	
	NEC Micro	**μPB2902**	**1850**
	Raytheon	AM2902	
AM2905	Motorola	MC2905	
	Raytheon	AM2905	
AM2906	Motorola	MC2906	
	Raytheon	AM2906	
AM2907	Motorola	MC2907	
	Raytheon	AM2907	
AM2909	Motorola	MC2909	
	National	IDM2909	
	NEC Micro	**μPB2909**	**1850**
	Raytheon	AM2909	
AM2911	Motorola	MC2911	
	National	IDM2911	
	NEC Micro	**μPB2911**	**1850**
	Raytheon	AM2911	
AM2915	Motorola	MC2915	
	NEC Micro	**μPB2915**	**1850**
AM2916	Motorola	MC2916	
	NEC Micro	**μPB2916**	**1850**
AM2917	Motorola	MC2917	
	NEC Micro	**μPB2917**	**1850**
AM2918	Motorola	MC2918	
	NEC Micro	**μPB2918**	**1850**
	Raytheon	AM2918	
DAC-08	Datel	DAC-08B	
	PMI	**DAC-08**	**919**
DM7820	Signetics	DS7820	
DM7820A	Signetics	DS7820A	
	TI	SN55182	
DM7830	Signetics	DS7830	
	TI	SN55183	
DM7831	TI	DS7831	
DM7832	TI	DS7832	
DM8820A	TI	SN75182	
DM8830	Signetics	DS8830	
DM8830	TI	SN75183	
DM8831	TI	DS7831	
DM8832	TI	DS7832	
LF155	Fairchild	μAF155	
	Intersil	LF155	
	Motorola	LF155	
	National	**LF155**	**786**
	PMI	**PM155**	**871**
	Raytheon	LF155	
	Signetics	LF155	
	TI	LF155	
LF156	Fairchild	μAF156	
	Intersil	LF156	
	Motorola	LF156	
	National	**LF156**	**786**
	PMI	**PM156**	**877**
	Raytheon	LF156	
	Signetics	LF156	
	TI	LF156	
LF157	Fairchild	μAF157	
	Intersil	LF157	
	Motorola	LF157	
	National	**LF157**	**786**
	PMI	**PM157**	**882**
	Raytheon	LF157	
	Signetics	LF157	
	TI	LF157	
LF255	Fairchild	μAF255	
	Intersil	LF255	
	Motorola	LF255	
	National	**LF255**	**786**
	PMI	**PM255**	**871**
	Raytheon	LF255	
	Signetics	LF255	
	TI	LF255	
LF256	Fairchild	μAF256	
	Intersil	LF256	
	Motorola	LF256	
	National	**LF256**	**786**
	PMI	**PM256**	**877**
	Raytheon	LF256	
	Signetics	LF256	
	TI	LF256	
LF257	Fairchild	μAF257	
	Intersil	LF257	
	Motorola	LF257	
	National	**LF257**	**786**
	PMI	**PM257**	**882**
	Raytheon	LF257	
	Signetics	LF257	
	TI	LF257	
LF355	Fairchild	μAF355	
	Intersil	LF355	
	Motorola	LF355	
	National	**LF355**	**786**
	PMI	**PM355**	**871**
	Raytheon	LF355	
	Signetics	LF355	
	TI	LF355	
LF356	Fairchild	μAF356	
	Intersil	LF356	
	Motorola	LF356	
	National	**LF356**	**786**
	PMI	**PM356**	**877**
	Raytheon	LF356	
	Signetics	LF356	
	TI	LF356	
LF357	Fairchild	μAF357	
	Intersil	LF357	
	Motorola	LF357	
	National	**LF357**	**786**
	PMI	**PM357**	**882**
	Raytheon	LF357	
	Signetics	LF357	
	TI	LF357	
LM101	AD	AD101	
	Fairchild	μA101	
	Intersil	LM101	
	Motorola	LM101	
	National	LM101	
	RCA	CA101	
	Signetics	LM101	
	Silicon G	SG101	
LM102	Fairchild	μA102	
LM105	Fairchild	μA105	
	Intersil	LM105	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Advanced Micro Devices (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
LM105	Motorola	LM105	
	National	LM105	
	Raytheon	LM105	
	Silicon G	SG105	
LM107	Fairchild	μA107	
	Intersil	LM107	
	Motorola	LM107	
	National	LM107	
	Raytheon	LM107	
	RCA	CA107	
	Silicon G	SG107	
LM108	AD	AD108	
	Fairchild	μA108	
	Intersil	LM108	
	Motorola	LM108	
	National	LM108	
	Raytheon	LM108	
	RCA	CA108	
	Signetics	LM108	
	Silicon G	SG108	
LM110	Fairchild	μA110	
	Intersil	LM110	
	Motorola	LM110	
	National	LM110	
	Silicon G	SG110	
LM111	Fairchild	μA111	
	Intersil	LM111	
	Motorola	LM111	
	National	LM111	
	Raytheon	LM111	
	RCA	CA111	
	Signetics	LM111	
	Silicon G	SG111	
LM118	AD	AD518	
	National	LM118	
	Raytheon	LM118	
LM139	Fairchild	μA139	
~~LM148~~	~~Exar~~	~~XR4741~~	
	Raytheon	LM148	
LM201	AD	AD201	
	Fairchild	μA201	
	Intersil	LM201	
	Motorola	LM201	
	National	LM201	
	RCA	CA201	
	Signetics	LM201	
	Silicon G	SG201	
LM202	Motorola	LM210	
	Silicon G	SG202	
LM205	Intersil	LM205	
	Motorola	LM205	
	Raytheon	LM205	
	Silicon G	SG205	
LM207	Fairchild	μA207	
	Intersil	LM207	
	Motorola	LM207	
	Raytheon	LM207	
	RCA	CA207	
	Silicon G	SG207	
LM208	AD	AD208	
	Fairchild	μA208	
	Intersil	LM208	
	Motorola	LM208	
	Raytheon	LM208	
	RCA	CA208	
	Silicon G	SG208	
LM210	Intersil	LM210	
	Motorola	LM210	
	Silicon G	SG210	
LM211	Intersil	LM211	
	Motorola	LM211	
	Raytheon	LM211	
	RCA	CA211	
	Signetics	LM211	
	Silicon G	SG211	
LM218	AD	AD518	
	Raytheon	LM218	
LM248	Exar	XR4741	
	Raytheon	LM248	
LM301	AD	AD301	
	Fairchild	μA301	
	Intersil	LM301	
LM301	Motorola	LM301	
	Raytheon	LM301	
	RCA	CA301	
	Signetics	LM301	
	Silicon G	SG301	
LM302	Fairchild	μA302	
LM305	Fairchild	μA305	
	Intersil	LM305	
	Motorola	LM305	
	Raytheon	LM305	
	Silicon G	SG305	
LM307	Fairchild	μA307	
	Intersil	LM307	
	Motorola	LM307	
	Raytheon	LM307	
	RCA	CA307	
	Signetics	LM307	
	Silicon G	SG307	
LM308	AD	AD308	
	Fairchild	μA308	
	Intersil	LM308	
	Motorola	LM308	
	Raytheon	LM308	
	RCA	CA308	
	Signetics	LM308	
	Silicon G	SG308	
LM310	Fairchild	μA310	
	Intersil	LM310	
	Motorola	LM310	
	Silicon G	SG310	
LM311	Fairchild	μA311	
	Intersil	LM311	
	Motorola	LM311	
	Raytheon	LM311	
	RCA	CA311	
	Signetics	LM311	
	Silicon G	SG311	
LM318	AD	AD518	
	Raytheon	LM318	
LM339	Fairchild	μA339	
LM348	Exar	XR4741	
	~~Raytheon~~	~~LM348~~	
NE555	Exar	XR555	
		XR555M	
	Fairchild	μA555	
	Motorola	MC1455	
	National	LM555	
	Silicon G	SG555	
NE556	Exar	XR556	
	Fairchild	μA556	
SE555	Exar	XR555	
SE556	Exar	XR556M	
SN54LS123	National	DM54LS123	
	Raytheon	**54LS123**	**275**
	TI	SN54LS123	
SN54LS138	Motorola	SN54LS138	
	Raytheon	54LS138	
SN54LS139	Fairchild	54LS139	
	Motorola	SN54LS139	
	National	DM54LS139	
	Raytheon	54LS139	
	Signetics	74LS139	
	TI	SN54LS139	
SN54LS148	TI	SN54LS148	
SN54LS151	Fairchild	54LS151	
	Motorola	SN54LS151	
	National	DM54LS151	
	Raytheon	54LS151	
	Signetics	54LS151	
	TI	SN54LS151	
SN54LS153	Fairchild	54LS153	
	Motorola	SN54LS153	
	National	DM54LS153	
	Raytheon	54LS153	
	Signetics	54LS153	
	TI	SN54LS153	
SN54LS157	Fairchild	54LS157	
	Motorola	SN54LS157	
	National	DM54LS157	
	Raytheon	54LS157	
	Signetics	54LS157	
	TI	SN54LS157	
SN54LS158	Motorola	SN54LS158	
	Raytheon	54LS158	
SN54LS160	Fairchild	54LS160	
	Motorola	SN54LS160	
SN54LS160	National	DM54LS160	
	Raytheon	54LS160	
	TI	SN54LS160	
SN54LS161	Fairchild	54LS161	
	Motorola	SN54LS161	
	National	DM54LS161	
	Raytheon	54LS161	
	Signetics	54LS161	
	TI	SN54LS161	
SN54LS162	Fairchild	54LS162	
	Motorola	SN54LS162	
	National	DM54LS162	
	Raytheon	54LS162	
	TI	SN54LS162	
SN54LS163	Fairchild	54LS163	
	Motorola	SN54LS163	
	National	DM54LS163	
	Raytheon	54LS163	
	Signetics	54LS163	
	TI	SN54LS163	
SN54LS164	Fairchild	54LS164	
	Motorola	SN54LS164	
	National	DM54LS164	
	Raytheon	**54LS164**	**272**
	Signetics	54LS164	
	TI	SN54LS164	
SN54LS168	Fairchild	54LS168	
	National	DM54LS168	
	TI	SN54LS168	
SN54LS169	Fairchild	54LS169	
	National	DM54LS169	
	TI	SN54LS169	
SN54LS170	Fairchild	54LS170	
	Motorola	SN54LS170	
	National	DM54LS170	
	Raytheon	54LS170	
	Signetics	54LS170	
	TI	SN54LS170	
SN54LS174	Fairchild	54LS174	
	Motorola	SN54LS174	
	National	DM54LS174	
	Raytheon	54LS174	
	Signetics	54LS174	
	TI	SN54LS174	
SN54LS175	Fairchild	54LS175	
	Motorola	SN54LS175	
	National	DM54LS175	
	Raytheon	54LS175	
	Signetics	54LS175	
	TI	SN54LS175	
SN54LS181	Fairchild	54LS181	
	Motorola	SN54LS181	
	Raytheon	54LS181	
	Signetics	54LS181	
	TI	SN54LS181	
SN54LS190	Fairchild	54LS190	
	Motorola	SN54LS190	
	National	DM54LS190	
	Raytheon	54LS190	
	Signetics	54LS190	
	TI	SN54LS190	
SN54LS191	Fairchild	54LS191	
	Motorola	SN54LS191	
	National	DM54LS191	
	Raytheon	54LS191	
	Signetics	54LS191	
	TI	SN54LS191	
SN54LS192	Fairchild	54LS192	
	Motorola	SN54LS192	
	National	DM54LS192	
	Raytheon	54LS192	
	Signetics	54LS192	
	TI	SN54LS192	
SN54LS193	Fairchild	54LS193	
	Motorola	SN54LS193	
	National	DM54LS193	
	Raytheon	54LS193	
	Signetics	54LS193	
	TI	SN54LS193	
SN54LS194A	Fairchild	54LS194	
	Motorola	SN54LS194	
	Raytheon	54LS194A	
	TI	SN54LS194A	
SN54LS195A	Fairchild	54LS195	
	Motorola	SN54LS195	
	Raytheon	54LS195A	
SN54LS195A	Signetics	54LS195A	
	TI	SN54LS195A	
SN54LS240	Fairchild	54LS240	
	MMI	54LS240	
	TI	SN54LS240	
SN54LS241	Fairchild	54LS241	
	MMI	54LS241	
	TI	SN54LS241	
SN54LS242	**Raytheon**	**54LS242**	**282**
	TI	SN54LS242	
SN54LS243	**Raytheon**	**54LS243**	**282**
	TI	SN54LS243	
SN54LS251	Fairchild	54LS251	
	Motorola	SN54LS251	
	Raytheon	54LS251	
	Signetics	54LS251	
	TI	SN54LS251	
SN54LS253	Fairchild	54LS253	
	Motorola	SN54LS253	
	National	DM54LS253	
	Raytheon	54LS253	
	Signetics	54LS253	
	TI	SN54LS253	
SN54LS257	Motorola	SN54LS257	
	Raytheon	54LS257	
SN54LS258	Fairchild	54LS258	
	Motorola	SN54LS258	
	Raytheon	54LS258	
	TI	SN54LS258	
SN54LS273	Motorola	SN54LS273	
	TI	SN54LS273	
SN54LS299	Fairchild	54LS299	
	Motorola	SN54LS299	
	Raytheon	54LS299	
	TI	SN54LS299	
SN54LS322	TI	SN54LS322	
SN54LS323	TI	SN54LS323	
SN54LS374	MMI	54LS374	
	Motorola	SN54LS374	
	TI	SN54LS374	
SN54LS377	Motorola	SN54LS377	
	TI	SN54LS377	
SN54LS378	TI	SN54LS378	
SN54LS379	TI	SN54LS379	
SN54LS381	TI	SN54LS381	
SN54LS384	TI	SN54LS384	
SN54LS385	TI	SN54LS385	
SN54LS399	TI	SN54LS399	
SN54LS424	TI	SN54LS424	
SN54LS670	Fairchild	54LS670	
	Motorola	SN54LS670	
	National	DM54LS670	
	Raytheon	54LS670	
	Signetics	54LS670	
	TI	SN54LS670	
SN54S138	Fairchild	54S138	
	TI	SN54S138	
SN54S139	Fairchild	54S139	
	Signetics	54S139	
	TI	SN54S139	
SN54S140	Signetics	54S140	
	TI	SN54S140	
SN54S151	Fairchild	54S151	
	Signetics	54S151	
	TI	SN54S151	
SN54S153	Fairchild	54S153	
	Signetics	54S153	
	TI	SN54S153	
SN54S157	Fairchild	54S157	
	Signetics	54S157	
	TI	SN54S157	
SN54S158	Fairchild	54S158	
	Signetics	54S158	
	TI	SN54S158	
SN54S174	Fairchild	54S174	
	TI	SN54S174	
SN54S175	Fairchild	54S175	
	TI	SN54S175	
SN54S181	Fairchild	54S181	
	Signetics	54S181	
	TI	SN54S181	
SN54S189	TI	SN54S189	
SN54S194	Fairchild	54S194	
	TI	SN54S194	
SN54S195	Fairchild	54S195	
	TI	SN54S195	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN54S240	**MMI**	**54S240**	**462**
	Raytheon	54S240	
	TI	SN54S240	
SN54S241	**MMI**	**54S241**	**462**
	Raytheon	54S241	
	TI	SN54S241	
SN54S244	**MMI**	**54S244**	**462**
	Raytheon	54S244	
SN54S251	Fairchild	54S251	
	Signetics	54S251	
	TI	SN54S251	
SN54S253	Fairchild	54S253	
	Signetics	54S253	
SN54S257	Fairchild	54S257	
	Signetics	54S257	
	TI	SN74S257	
SN54S258	Fairchild	54S258	
	Signetics	54S258	
	TI	SN54S258	
SN54123	Fairchild	54123	
	ITT	ITT54123	
	Motorola	MC54123	
	National	DM54123	
	Raytheon	54123	
	Signetics	54123	
	TI	SN54123	
SN54154	Fairchild	54154	
	Motorola	MC54154	
	National	DM54154	
	Raytheon	54154	
	Signetics	54154	
	TI	SN54154	
SN54157	Fairchild	54157	
	ITT	ITT54157	
	Motorola	MC54157	
	National	DM54157	
	Raytheon	54157	
	Signetics	54157	
	TI	SN54157	
SN54160	Fairchild	54160	
	ITT	ITT54160	
	Motorola	MC54160	
	National	DM54160	
	Raytheon	54160	
	Signetics	54160	
	TI	SN54160	
SN54161	Fairchild	54161	
	ITT	ITT54161	
	Motorola	MC54161	
	National	DM54161	
	Raytheon	54161	
	Signetics	54161	
	TI	SN54161	
SN54162	Fairchild	54162	
	ITT	ITT54162	
	Motorola	MC54162	
	National	DM54162	
	Raytheon	54162	
	Signetics	54162	
	TI	SN54162	
SN54163	Fairchild	54163	
	ITT	ITT54163	
	Motorola	MC54163	
	National	DM54163	
	Raytheon	54163	
	Signetics	54163	
	TI	SN54163	
SN54164	Fairchild	54164	
	ITT	ITT54164	
	National	DM54164	
	Raytheon	54164	
	Signetics	54164	
	TI	SN54164	
SN54175	Fairchild	54175	
	Motorola	MC54175	
	National	DM54175	
	Raytheon	54175	
	Signetics	54175	
	TI	SN54175	
SN54181	Fairchild	54181	
		9341	
	Motorola	MC54181	
SN54181	National	DM54181	
	Raytheon	54181	
	Signetics	54181	
	TI	SN54181	
		SN74181	
SN54182	Fairchild	54182	
		9342	
	ITT	ITT54182	
	Motorola	MC54182	
	National	DM54182	
	Raytheon	54182	
	Signetics	54182	
	TI	SN54182	
		SN74182	
SN54192	Fairchild	54192	
	ITT	ITT54192	
	Motorola	MC54192	
	National	DM54192	
	Raytheon	54192	
	Signetics	54192	
	TI	SN54192	
SN54193	Fairchild	54193	
	ITT	ITT54193	
	Motorola	MC54193	
	National	DM54193	
	Raytheon	54193	
	Signetics	54193	
	TI	SN54193	
SN54194	Fairchild	54194	
	ITT	ITT54194	
	Motorola	MC54194	
	National	DM54194	
	Signetics	54194	
	TI	SN54194	
SN54195	Fairchild	54195	
	ITT	ITT54195	
	Motorola	MC54195	
	National	DM54195	
	Raytheon	54195	
	Signetics	54195	
	TI	SN54195	
SN54259	TI	SN54259	
SN5489	MMI	5560	
	Raytheon	5489	
SN55107	Fairchild	55107	
	TI	SN55107	
SN55108	Fairchild	55108	
	TI	SN55108	
SN55109	Fairchild	55109	
	TI	SN55109	
SN55110	Fairchild	55110	
	TI	SN55110	
SN5520	Fairchild	5520	
SN5521	Fairchild	5521	
SN55234	Fairchild	55234	
	TI	SN55234	
SN55235	Fairchild	55235	
	TI	SN55235	
SN55238	Fairchild	55238	
	TI	SN55238	
SN55239	Fairchild	55239	
	TI	SN55239	
SN5524	Fairchild	5524	
SN5525	Fairchild	5525	
SN55325	Fairchild	55325	
	TI	SN55325	
SN74LS123	ITT	ITT74LS123	
	National	DM74LS123	
	Raytheon	**74LS123**	**275**
	TI	SN74LS123	
SN74LS138	Fairchild	74LS138	
	ITT	ITT74LS138	
	Motorola	SN74LS138	
	National	DM74LS138	
	NEC America	μPB74LS138	
	Raytheon	74LS138	
	Signetics	74LS138	
	TI	SN74LS138	
SN74LS139	Fairchild	74LS139	
	ITT	ITT74LS139	
	Motorola	SN74LS139	
	National	DM74LS139	
	NEC America	μPB74LS139	
	Raytheon	74LS139	
	Signetics	74LS139	
	TI	SN74LS139	
SN74LS148	TI	SN74LS148	
SN74LS151	Fairchild	74LS151	
	ITT	ITT74LS151	
	Motorola	SN74LS151	
	National	DM74LS151	
	NEC America	μPB74LS151	
	Raytheon	74LS151	
	Signetics	74LS151	
	TI	SN74LS151	
SN74LS153	Fairchild	74LS153	
	ITT	ITT74LS153	
	Motorola	SN74LS153	
	National	DM74LS153	
	NEC America	μPB74LS153	
	Raytheon	74LS153	
	Signetics	74LS153	
	TI	SN74LS153	
SN74LS157	Fairchild	74LS157	
	ITT	ITT74LS157	
	Motorola	SN74LS157	
	National	DM74LS157	
	NEC America	μPB74LS157	
	Raytheon	74LS157	
	Signetics	74LS157	
	TI	SN74LS157	
SN74LS158	Fairchild	74LS158	
	ITT	ITT74LS158	
	Motorola	SN74LS158	
	National	DM74LS158	
	Raytheon	74LS158	
	Signetics	74LS158	
	TI	SN74LS158	
SN74LS160	Fairchild	74LS160	
	ITT	ITT74LS160	
	Motorola	SN74LS160	
	National	DM74LS160	
	Raytheon	74LS160	
	Signetics	74LS160	
	TI	SN74LS160	
SN74LS161	Fairchild	74LS161	
	ITT	ITT74LS161	
	Motorola	SN74LS161	
	National	DM74LS161	
	NEC America	μPB74LS161	
	Raytheon	74LS161	
	Signetics	74LS161	
	TI	SN74LS161	
SN74LS162	Fairchild	74LS162	
	ITT	ITT74LS162	
	Motorola	SN74LS162	
	National	DM74LS162	
	Raytheon	74LS162	
	Signetics	74LS162	
	TI	SN74LS162	
SN74LS163	Fairchild	74LS163	
	ITT	ITT74LS163	
	Motorola	SN74LS163	
	National	DM74LS163	
	Raytheon	74LS163	
	Signetics	74LS163	
	TI	SN74LS163	
SN74LS164	Fairchild	74LS164	
	ITT	ITT74LS164	
	Motorola	SN74LS164	
	National	DM74LS164	
	NEC America	μPB74LS164	
	Raytheon	**74LS164**	**272**
	Signetics	74LS164	
	TI	SN74LS164	
SN74LS168	Fairchild	74LS168	
	National	DM74LS168	
	TI	SN74LS168	
SN74LS169	Fairchild	74LS169	
	National	DM74LS169	
	TI	SN74LS169	
SN74LS170	Fairchild	74LS170	
	ITT	ITT74LS170	
	Motorola	SN74LS170	
	National	DM74LS170	
	Raytheon	74LS170	
	Signetics	74LS170	
	TI	SN74LS170	
SN74LS174	Fairchild	74LS174	
	ITT	ITT74LS174	
	Motorola	SN74LS174	
	National	DM74LS174	
SN74LS174	Raytheon	74LS174	
	Signetics	74LS174	
	TI	SN74LS174	
SN74LS175	Fairchild	74LS175	
	ITT	ITT74LS175	
	Motorola	SN74LS175	
	National	DM74LS175	
	NEC America	μPB74LS175	
	Raytheon	74LS175	
	Signetics	74LS175	
	TI	SN74LS175	
SN74LS181	Fairchild	74LS181	
	Motorola	SN74LS181	
	Raytheon	74LS181	
	Signetics	74LS181	
	TI	SN74LS181	
SN74LS190	Fairchild	74LS190	
	ITT	ITT74LS190	
	Motorola	SN74LS190	
	National	DM74LS190	
	Raytheon	74LS190	
	Signetics	74LS190	
	TI	SN74LS190	
SN74LS191	Fairchild	74LS191	
	ITT	ITT74LS191	
	Motorola	SN74LS191	
	National	DM74LS191	
	Raytheon	74LS191	
	Signetics	74LS191	
	TI	SN74LS191	
SN74LS192	Fairchild	74LS192	
	ITT	ITT74LS192	
	Motorola	SN74LS192	
	National	DM74LS192	
	NEC America	μPB74LS192	
	Raytheon	74LS192	
	Signetics	74LS192	
	TI	SN74LS192	
SN74LS193	Fairchild	74LS193	
	ITT	ITT74LS193	
	Motorola	SN74LS193	
	National	DM74LS193	
	NEC America	μPB74LS193	
	Raytheon	74LS193	
	Signetics	74LS193	
	TI	SN74LS193	
SN74LS194A	Fairchild	74LS194	
	ITT	ITT74LS194A	
	Motorola	SN74LS194	
	NEC America	μPB74LS194	
	Raytheon	74LS194A	
	Signetics	74LS194A	
	TI	SN74LS194A	
SN74LS195A	Fairchild	74LS195	
	ITT	ITT74LS195A	
	Motorola	SN74LS195	
	NEC America	μPB74LS195	
	Raytheon	74LS195A	
	Signetics	74LS195A	
	TI	SN74LS195A	
SN74LS240	Fairchild	74LS240	
	ITT	ITT74LS240	
	MMI	74LS240	
	Motorola	SN74LS240	
	Raytheon	**74LS240**	**279**
	Signetics	74LS240	
	TI	SN74LS240	
SN74LS241	Fairchild	74LS241	
	ITT	ITT74LS241	
	MMI	74LS241	
	Motorola	SN74LS241	
	Raytheon	**74LS241**	**279**
	Signetics	74LS241	
	TI	SN74LS241	
SN74LS242	Fairchild	74LS242	
	ITT	ITT74LS242	
	Motorola	SN74LS242	
	Raytheon	**74LS242**	**282**
	Signetics	74LS242	
	TI	SN74LS242	
SN74LS243	Fairchild	74LS243	
	ITT	ITT74LS243	
	Motorola	SN74LS243	
	Raytheon	**74LS243**	**282**
	Signetics	74LS243	
	TI	SN74LS243	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN74LS244	Fairchild	74LS244	
	ITT	ITT74LS244	
	MMI	74LS244	
	Motorola	SN74LS244	
	Raytheon	**74LS244**	**279**
	Signetics	74LS244	
	TI	SN74LS244	
SN74LS251	Fairchild	74LS251	
	ITT	ITT74LS251	
	Motorola	SN74LS251	
	National	DM74LS251	
	NEC America	μPB74LS251	
	Raytheon	74LS251	
	Signetics	74LS251	
	TI	SN74LS251	
SN74LS253	Fairchild	74LS253	
	ITT	ITT74LS253	
	Motorola	SN74LS253	
	National	DM74LS253	
	NEC America	μPB74LS253	
	Raytheon	74LS253	
	Signetics	74LS253	
	TI	SN74LS253	
SN74LS257	Fairchild	74LS257	
	ITT	ITT74LS257	
	Motorola	SN74LS257	
	National	DM74LS257	
	NEC America	μPB74LS257	
	Raytheon	74LS257	
	Signetics	74LS257	
	TI	SN74LS257	
SN74LS258	Fairchild	74LS258	
	ITT	ITT74LS258	
	Motorola	SN74LS258	
	National	DM74LS258	
	NEC America	μPB74LS258	
	Raytheon	74LS258	
	Signetics	74LS258	
	TI	SN74LS258	
SN74LS273	Fairchild	74LS273	
	ITT	ITT74LS273	
	Motorola	SN74LS273	
	Signetics	74LS273	
	TI	SN74LS273	
SN74LS299	Fairchild	74LS299	
	ITT	ITT74LS299	
	Motorola	SN74LS299	
	Raytheon	74LS299	
	TI	SN74LS299	
SN74LS322	TI	SN74LS322	
SN74LS323	ITT	ITT74LS323	
	Raytheon	74LS323	
	TI	SN74LS323	
SN74LS373	Fairchild	74LS373	
	ITT	ITT74LS373	
	MMI	74LS373	
	Raytheon	**74LS373**	**288**
	Signetics	74LS373	
	TI	SN74LS373	
SN74LS374	Fairchild	74LS374	
	ITT	ITT74LS374	
	MMI	74LS374	
	Motorola	SN74LS374	
	Raytheon	**74LS374**	**288**
	TI	SN74LS374	
SN74LS377	Fairchild	74LS377	
	ITT	ITT74LS377	
	Motorola	SN74LS377	
	Raytheon	**74LS377**	**288**
	Signetics	74LS377	
	TI	SN74LS377	
SN74LS378	Fairchild	74LS378	
	ITT	ITT74LS378	
	Signetics	74LS378	
	TI	SN74LS378	
SN74LS379	TI	SN74LS379	
SN74LS381	ITT	ITT74LS381	
	TI	SN74LS381	
SN74LS384	TI	SN74LS384	
SN74LS385	TI	SN74LS385	
SN74LS399	TI	SN74LS399	
SN74LS424	TI	SN74LS424	
SN74LS670	Fairchild	74LS670	
	Motorola	SN74LS670	
	National	DM74LS670	
	Raytheon	74LS670	
	Signetics	74LS670	
	TI	SN74LS670	
SN74S138	Fairchild	74S138	
	Mitsubishi	M5S138	
	National	DM74S138	
	Signetics	74S138	
	TI	SN74S138	
SN74S139	Fairchild	74S139	
	National	DM74S139	
	Signetics	74S139	
	TI	SN74S139	
SN74S151	Fairchild	74S151	
	Hitachi	HD74S151	
	Mitsubishi	M5S151	
	National	DM74S151	
	Signetics	74S151	
	TI	SN74S151	
SN74S153	Fairchild	74S153	
	Mitsubishi	M5S153	
	National	DM74S153	
	Signetics	74S153	
	TI	SN74S153	
SN74S157	Fairchild	74S157	
	Mitsubishi	M5S157	
	National	DM74S157	
	Signetics	74S157	
	TI	SN74S157	
SN74S158	Fairchild	74S158	
	Mitsubishi	M5S158	
	National	DM74S158	
	Signetics	74S158	
	TI	SN74S158	
SN74S160	Fairchild	93S10	
SN74S161	Fairchild	93S16	
SN74S174	Fairchild	74S174	
	Hitachi	HD74S174	
	Mitsubishi	M5S174	
	National	DM74S174	
	Signetics	74S174	
	TI	SN74S174	
SN74S175	Fairchild	74S175	
	Hitachi	HD74S175	
	Mitsubishi	M5S175	
	National	DM74S175	
	Signetics	74S175	
	TI	SN74S175	
SN74S181	Fairchild	74S181	
	Hitachi	HD74S181	
	Mitsubishi	M5S181	
	Signetics	74S181	
	TI	SN74S181	
SN74S194	Fairchild	74S194	
	Signetics	74S194	
	TI	SN74S194	
SN74S195	Fairchild	74S195	
	National	DM74S195	
	Signetics	74S195	
	TI	SN74S195	
SN74S240	**MMI**	**74S240**	**462**
	Raytheon	74S240	
	TI	SN74S240	
SN74S241	**MMI**	**74S241**	**462**
	Raytheon	74S241	
	TI	SN74S241	
SN74S244	**MMI**	**74S244**	**462**
	Raytheon	74S244	
SN74S251	Fairchild	74S251	
	Hitachi	HD74S251	
	Mitsubishi	M5S251	
	National	DM74S251	
	Signetics	74S251	
	TI	SN74S251	
SN74S253	Fairchild	74S253	
	National	DM74S253	
	Signetics	74S253	
SN74S257	Fairchild	74S257	
	Mitsubishi	M5S257	
	National	DM74S257	
	Signetics	74S257	
	TI	SN74S257	
SN74S258	Fairchild	74S258	
	Mitsubishi	M5S258	
SN74S258	Signetics	74S258	
	TI	SN74S258	
SN74S289	NEC Micro	μPB2289	
SN74123	Fairchild	74123	
	ITT	ITT74123	
	Mitsubishi	M53323	
	Motorola	MC74123	
	National	DM74123	
	NEC America	μPB74123	
	Raytheon	74123	
	Signetics	74123	
	TI	SN74123	
	TRW	74123	
SN74154	Fairchild	74154	
	Mitsubishi	M53354	
	Motorola	MC74154	
	National	DM74154	
	NEC America	μPB74154	
	Raytheon	74154	
	Signetics	74154	
	TI	SN74154	
	TRW	74154	
SN74157	Fairchild	74157	
	Hitachi	HD74157	
	ITT	ITT74157	
	Mitsubishi	M53357	
	Motorola	MC74157	
	National	DM74157	
	NEC America	μPB74157	
	Raytheon	74157	
	Signetics	74157	
	TI	SN74157	
SN74160	Fairchild	74160	
	Hitachi	HD74160	
	ITT	ITT74160	
	Mitsubishi	M53360	
	Motorola	MC74160	
	National	DM74160	
	Raytheon	74160	
	Signetics	74160	
	TI	SN74160	
	TRW	74160	
SN74161	Fairchild	74161	
	Hitachi	HD74161	
	ITT	ITT74161	
	Mitsubishi	M53361	
	Motorola	MC74161	
	National	DM74161	
	NEC America	μPB74161	
	Raytheon	74161	
	Signetics	74161	
	TI	SN74161	
	TRW	74161	
SN74162	Fairchild	74162	
	Hitachi	HD74162	
	ITT	ITT74162	
	Mitsubishi	M53362	
	Motorola	MC74162	
	National	DM74162	
	Raytheon	74162	
	Signetics	74162	
	TI	SN74162	
	TRW	74162	
SN74163	Fairchild	74163	
	Hitachi	HD74163	
	ITT	ITT74163	
	Mitsubishi	M53363	
	Motorola	MC74163	
	National	DM74163	
	Raytheon	74163	
	Signetics	74163	
	TI	SN74163	
	TRW	74163	
SN74174	Fairchild	54174	
		74174	
	Hitachi	HD74174	
	Mitsubishi	M53374	
	Motorola	MC54174	
		MC74174	
	National	DM54174	
		DM74174	
	Raytheon	54174	
		74174	
	Signetics	54174	
		74174	
	TI	SN54174	
SN74174	TI	SN74174	
SN74175	Fairchild	74175	
	Hitachi	HD74175	
	Mitsubishi	M53375	
	Motorola	MC74175	
	National	DM74175	
	NEC America	μPB74175	
	Raytheon	74175	
	Signetics	74175	
	TI	SN74175	
SN74181	Fairchild	74181	
	Mitsubishi	M53381	
	Motorola	MC74181	
	National	DM74181	
	NEC America	μPB74181	
	Raytheon	74181	
	Signetics	74181	
	TI	SN74181	
SN74182	Fairchild	74182	
	ITT	ITT74182	
	Mitsubishi	M53382	
	Motorola	MC74182	
	National	DM74182	
	NEC America	μPB74182	
	Raytheon	74182	
	Signetics	74182	
	TI	SN74182	
SN74192	Fairchild	74192	
	ITT	ITT74192	
	Mitsubishi	M53392	
	Motorola	MC74192	
	National	DM74192	
	NEC America	μPB74192	
	Raytheon	74192	
	Signetics	74192	
	TI	SN74192	
SN74193	Fairchild	74193	
	ITT	ITT74193	
	Mitsubishi	M53393	
	Motorola	MC74193	
	National	DM74193	
	NEC America	μPB74193	
	Raytheon	74193	
	Signetics	74193	
	TI	SN74193	
SN74194	Fairchild	74194	
	Hitachi	HD74194	
	ITT	ITT74194	
	Motorola	MC74194	
	National	DM74194	
	Signetics	74194	
	TI	SN74194	
SN74195	Fairchild	74195	
	ITT	ITT74195	
	Motorola	MC74195	
	National	DM74195	
	NEC America	μPB74195	
	Raytheon	74195	
	Signetics	74195	
	TI	SN74195	
SN74259	TI	SN74259	
SN7489	Fairchild	7489	
	Mitsubishi	M53289	
	National	**DM7489**	**1287**
	NEC Micro	μPB2089	
	TI	SN7489	
	TRW	7489	
SN75107	Fairchild	75107	
	TI	SN75107	
SN75108	Fairchild	75108	
	TI	SN75108	
SN75109	Fairchild	75109	
	TI	SN75109	
SN75110	Fairchild	75110	
	TI	SN75110	
SN7520	Fairchild	7520	
SN75207	Fairchild	75207	
	TI	SN75207	
SN75208	Fairchild	75208	
	TI	SN75208	
SN7521	Fairchild	7521	
SN75234	Fairchild	75234	
	TI	SN75234	
SN75235	Fairchild	75235	
	TI	SN75235	
SN75238	Fairchild	75238	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN75238	TI	SN75238	
SN75239	Fairchild	75239	
SN7524	Fairchild	7524	
SN7525	Fairchild	7525	
SN75325	Fairchild	75325	
	TI	SN75325	
SSS1408	Datel	DAC-IC8BC	
	PMI	SSS1408	
SSS1508	Datel	DAC-IC8BM	
	PMI	SSS1508	
SSS725	**PMI**	**SSS725**	**849**
SSS741	**PMI**	**OP-02**	**839**
		SSS741	**839**
SSS747	**PMI**	**OP-04**	**844**
		SSS747	**844**
TMS2812	Plessey	MP2812	
0026	TI	SN75369	
1002	Mostek	MK1002	
1101	Intersil	IM7501	
		IM7511	
	Mostek	MK4007	
1402	National	MM1402	
	Nortec	1402	
	Signetics	2502	
	Synertek	SY1402	
1403	National	MM1403	
	Nortec	1403	
	Signetics	2503	
	Synertek	SY1403	
1404	National	MM1404	
	Nortec	1404	
	Signetics	2504	
	Synertek	SY1404	
1406	Signetics	2506	
1407	Signetics	2517	
1408	PMI	SSS1408	
1458	Exar	XR1458	
	Fairchild	µA1458	
1488	Exar	XR1488	
	Motorola	MC1488	
	National	DS1488	
	Raytheon	RC1488	
	Signetics	MC1488	
	Silicon G	SG1488	
	TI	SN75188	
1489	Exar	XR1489	
	National	DS1489	
	Raytheon	RC1489	
	Signetics	MC1489	
	Silicon G	SG1489	
	TI	SN75189	
1489A	TI	SN75189A	
1500	Intersil	AM1500	
1501	Intersil	AM1501	
1506	Signetics	2506	
1507	Signetics	2506	
1508	PMI	SSS1508	
1558	Exar	XR1558	
	Fairchild	µA1558	
1660	**Intersil**	**AM166039**	
1702	Intel	1702A	
	Mostek	MK3702	
2101	EA	EA2101	
	Intel	2101	
	Intersil	7101	
	National	MM2101	
	NEC Micro	µPD2101	
	Signetics	2101	
	Synertek	SY2101	
2102	Mostek	MK4102	
	National	**MM2102**	**1300**
	NEC Micro	µPD2102	
	Signetics	2102	
2111	EA	EA2111	
	Intel	2111	
	National	MM2111	
	NEC Micro	µPD2111	
	Signetics	2111	
	Synertek	SY2111	
2112	EA	EA2112	
	Intel	2112	
	Intersil	7112	
2112	National	MM2112	
	Signetics	2112	
	Synertek	SY2112	
2401	Synertek	SY2401	
25LS240	Raytheon	25LS240	
25LS373	Raytheon	25LS373	
2702	Synertek	SY2102	
2708	EA	EA2708	
	Fujitsu	MB8518	
	Intel	2708	
	Mostek	MK2708	
	Motorola	MCM2708	
	National	MM2708	
	TI	TMS2708	
31L01	MMI	L5560	
		L6560	
	NEC Micro	µPB2089	
	Signetics	N82S25	
31L0101	Signetics	N8225	
3101	AMI	S1685	
	Fairchild	93403	
	NEC Micro	µPB2089	
	Signetics	82S25	
	TI	SN7489	
3101A	Signetics	3101A	
	TI	SN54S289	
		SN74S289	
3114	TI	TMS3114	
4102	Mostek	MK4102	
5889	Fairchild	5489	
	National	**DM5489**	**1287**
	TI	SN5489	
715	Fairchild	µA715	
723	Fairchild	µA723	
	Intersil	723	
	Motorola	MC1723	
	Raytheon	RC723	
		RM723	
	RCA	CA723	
	Signetics	µA723	
	Silicon G	SG723	
725	Fairchild	µA725	
	PMI	**SSS725**	**849**
733	Fairchild	µA733	
	Motorola	MC1733	
	Silicon G	SG733	
741	Fairchild	µA741	
	Intersil	741	
	Motorola	MC1741	
	PMI	**OP-02**	**839**
		SSS741	**839**
	Raytheon	RC741	
		RM741	
	RCA	CA741	
	Silicon G	SG741	
74164	Fairchild	74164	
	Hitachi	HD74164	
	ITT	ITT74164	
	Mitsubishi	M53364	
	National	DM74164	
	NEC America	µPB74164	
	Raytheon	74164	
	Signetics	74164	
	TI	SN74164	
747	Fairchild	µA747	
	Motorola	MC1747	
	PMI	**OP-04**	**844**
		SSS747	**844**
	Raytheon	RC747	
		RM747	
	RCA	CA747	
	Silicon G	SG747	
748	Fairchild	µA748	
	Intersil	748	
	Motorola	MC1748	
	Raytheon	RC748	
		RM748	
	RCA	CA748	
	Silicon G	SG748	
7552	Mostek	MK4102	
8048	**Intel**	**8048**	**1648**
	NEC Micro	**µPD8085**	**1847**
	Signetics	8048	
8085	**Intel**	**8085**	**1644**
	NEC Micro	**µPD8085**	**1847**
8155	**NEC Micro**	**µPD8155**	**1847**
8212	**NEC Micro**	**µPB8212**	**1804**
8214	**NEC Micro**	**µPB8214**	**1758**
8216	**NEC Micro**	**µPB8216**	**1810**
8224	**NEC Micro**	**µPB8224**	**1764**
8226	**NEC Micro**	**µPB8226**	**1810**
8228	**NEC Micro**	**µPB8228**	**1769**
8238	**NEC Micro**	**µPB8238**	**1769**
8251	**NEC Micro**	**µPD8251**	**1814**
8255	**NEC Micro**	**µPD8255**	**1830**
8257	**NEC Micro**	**µPD8257**	**1837**
8355	**NEC Micro**	**µPD8355**	**1848**
9LS298	Fairchild	9LS298	
	Raytheon	9LS298	
9050	**NEC Micro**	**µPD418**	**1412**
	Synertek	SY4050	
	TI	TMS4050	
9060	Intersil	7280	
	NEC Micro	**µPD411**	**1375**
	Signetics	2680	
	TI	TMS4060	
9080	Intel	8080	
	National	**INS8080A**	
		1656,1670	
	NEC Micro	µPB8080A	
	TI	TMS8080	
9080A	Intel	8080A	
	National	**INS8080A**	
		1656,1670	
	NEC Micro	**µPD8080AF**	**1736**
	Signetics	MP8080A	
	TI	TMS8080A	
91A11	**NEC Micro**	**µPD2111AL**	**1433**
91L01	NEC Micro	µPB2101AL	
91L02	Fairchild	21L02	
	National	**MM2102**	**1300**
	NEC Micro	**µPD2102AL**	**1429**
	Signetics	21L02	
		2102	
9101	Intersil	7101	
	National	MM2101	
	NEC Micro	**µPD2101AL**	**1424**
9102	Fairchild	2102	
	Mostek	MK4102	
	National	**MM2102**	**1300**
	NEC Micro	**µPD2102AL**	**1429**
	Signetics	21F02	
		2102	
		2402	
	Synertek	SY2102	
	TI	TMS4033	
		TMS4034	
9107	**NEC Micro**	**µPD411**	**1375**
9111	Intersil	7111	
	National	MM2111	
	NEC Micro	**µPD2111AL**	**1433**
9112	Intersil	7112	
	National	MM2112	
9130	AMI	S9130	
9140	AMI	S9140	
9145	**Harris**	**HM6504**	**1176**
9151	TI	TMS4051	
9208	Fairchild	3508	
	Mostek	MK30000	
	NEC Micro	**µPD2308**	**1478**
9214	Mostek	MK2600	
9216	**NEC Micro**	**µPD2316E**	**1492**
93L00	Fairchild	93L00	
93L01	Fairchild	93L01	
93L08	Fairchild	93L08	
93L09	Fairchild	93L09	
93L10	Fairchild	93L10	
93L11	Fairchild	93L11	
93L12	Fairchild	93L12	
93L14	Fairchild	93L14	
93L16	Fairchild	93L16	
93L18	Fairchild	93L18	
93L21	Fairchild	93L21	
93L22	Fairchild	93L22	
93L24	Fairchild	93L24	
93L28	Fairchild	93L28	
93L34	Fairchild	93L34	
93L38	Fairchild	93L38	
93L40	Fairchild	93L40	
93L41	Fairchild	93L41	
93L60	Fairchild	93L60	
	National	DM75L60	
93L60	National	DM85L60	
93L66	Fairchild	93L66	
	National	DM75L63	
		DM85L63	
9300	Fairchild	9300	
	Raytheon	RM9300	
	TI	SN54195	
		SN74195	
9301	Fairchild	9301	
	TI	SN29301	
		SN39301	
9304	Fairchild	9304	
	Raytheon	RM9304	
9306	Fairchild	9306	
9308	Fairchild	9308	
	Raytheon	RM9308	
	TI	SN29308	
		SN39308	
9309	Fairchild	9309	
	TI	SN29309	
		SN39309	
9310	Fairchild	9310	
	Raytheon	RM9310	
	TI	SN54160	
		SN74160	
9311	Fairchild	9311	
	Raytheon	RM9311	
	TI	SN54154	
		SN74154	
9312	Fairchild	9312	
	Raytheon	RM9312	
	TI	SN29312	
		SN39312	
9314	Fairchild	9314	
9316	Fairchild	9316	
	Raytheon	RM9316	
	TI	SN54161	
		SN74161	
9318	Fairchild	9318	
	TI	SN54148	
		SN74148	
9321	Fairchild	9321	
9322	Fairchild	9322	
	Raytheon	RM9322	
	TI	SN54157	
		SN74157	
9324	Fairchild	9324	
9328	Fairchild	9328	
9334	Fairchild	9334	
	TI	SN54259	
		SN74259	
9338	Fairchild	9338	
9340	Fairchild	9340	
9341	Fairchild	9341	
	Raytheon	RM9341	
	TI	SN54181	
		SN74181	
93415	Intel	2115	
	NEC Micro	**µPB2205**	**1418**
	TI	SN54S314	
		SN74S314	
9342	Fairchild	9342	
	Raytheon	RM9342	
	TI	SN54182	
		SN74182	
9360	Fairchild	9360	
	Raytheon	RM9360	
9366	Fairchild	9366	
	Raytheon	RM9366	
9401	Synertek	SY2401	
96L02	Fairchild	96L02	
9600	Fairchild	9600	
9601	Fairchild	9601	
	Raytheon	RF9601	
	TI	SN29601	
9602	Fairchild	9602	
	Raytheon	RF9602	
9614	Fairchild	9614	
	TI	SN55114	
		SN75114	
9615	Fairchild	9615	
	TI	SN55115	
		SN75115	
9616	Fairchild	9616	
9617	Fairchild	9617	
9620	Fairchild	9620	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Manufacturer Device	Replacement Source	Device	IC Master Page
Advanced Micro Devices (cont'd)			
9621	Fairchild	9621	
	Raytheon	RM9621	
American Microsystems, Inc.			
S1103A	Intel	1103A	
	Rockwell	1103A	
	Synertek	1103A	
S1413	SSS	SCL5430	
S146	Intel	1103-146	
	Signetics	2146	
♦S1670	Motorola	MC1160	
S1757	GI	AY3-1014A	
		AY3-1015	
		AY5-1013A	
	SMC	COM2052	
	Western	TR1402	
S1883	SMC	COM2017	
	TI	TMS6011	
	Western	TR1602	
♦S2076	Intersil	IM7780	
♦S2102	Intersil	IM7552	
	Motorola	MCM6605	
S2181	Mostek	MK1002	
		MK4116	
S2182	SMC	SR5015	
S2183	SMC	SR5015	
S2185	SMC	SR5015	
S2222	Nortec	2222	
	Signetics	N2222	
		S2222	
	SSS	SCM5522	
S2350	SMC	COM2601	
S2470	GI	AY1-1006	
S2555	Nitron	NC1183	
S2556	Nitron	NC1184	
~~S2559~~	~~Mostek~~	~~MK5085~~	
♦S2566	Motorola	MC1182	
	Nitron	NC1182	
S2567	Nitron	NC1181	
S3102	SGS	M330	
	TI	TMS4035	
S3102A	TI	TMS4033	
S3102B	TI	TMS4034	
S3514	Mostek	MK2600	
♦S4006	Mostek	MK4006	
♦S4008	Mostek	MK4008	
S4021	TI	TMS4060	
♦S4096	EA	EA4096	
	EMM/Semi	RO3-4096	
	Fairchild	4096	
	Mostek	MK4096	
S5101	Harris	HM5101	
		HM6501	**1174**
S5232	Mostek	MK2500	
		MK2600	
	National	MM5232	
S6508	**Harris**	**HM6508**	**1180**
S6518	**Harris**	**HM6518**	**1181**
S68A00	Motorola	MC68A00	
S68A10	Motorola	MC68A10	
S68A21	Motorola	MC68A21	
S68B00	Motorola	MC68B00	
S68B10	Motorola	MC68B10	
S68B21	Motorola	MC68B21	
S6800	Fairchild	F6800	
	Hitachi	M6800	
	Motorola	M6800	
S6810	Motorola	MCM6810	
S6820	Motorola	MC6820	
♦S6830	Motorola	MCM6830	
S6831A	Mostek	MK31000	
S6831B	Mostek	MK34000	
S6850	Motorola	MC6850	
S8499	SMC	GG4103	
S8865	GI	RO5-8192	
S8996	EMM/Semi	RO3-16384	
	GI	RO3-16384	
	Nortec	8996	
S9900	TI	TMS9900	
S9901	TI	TMS9901	
S9902	TI	TMS9902	
S9903	TI	TMS9903	
S9940	TI	TMS9940	
S9980	TI	TMS9980	
Analog Devices			
AD101	AMD	LM101	
	Fairchild	μA101	
	Motorola	LM101	
	National	LM101	
	RCA	CA101	
	Signetics	LM101	
	Silicon G	SG101	
AD108	AMD	LM108	
	Fairchild	μA108	
	Motorola	LM108	
	National	LM108	
	Raytheon	LM108	
	RCA	CA108	
	Signetics	LM108	
	Silicon G	SG108	
AD111	Motorola	LM111	
	National	LM111	
	Raytheon	LM111	
	RCA	CA111	
	Signetics	LM111	
	Silicon G	SG111	
AD201	AMD	LM201	
	Fairchild	μA201	
	Motorola	LM201	
	National	LM201	
	RCA	CA201	
	Signetics	LM201	
	Silicon G	SG201	
AD208	AMD	LM208	
	Fairchild	μA208	
	National	LM208	
	Raytheon	LM208	
	RCA	CA208	
	Silicon G	SG208	
AD211	National	LM211	
	Raytheon	LM211	
	RCA	CA211	
	Signetics	LM211	
	Silicon G	SG211	
AD301	AMD	LM301	
	Fairchild	μA301	
	Motorola	LM301	
	National	LM301	
	Raytheon	LM301	
	RCA	CA301	
	Signetics	LM301	
	Silicon G	SG301	
AD308	AMD	LM308	
	Fairchild	μA308	
	Motorola	LM308	
	National	LM308	
	Raytheon	LM308	
	RCA	CA308	
	Signetics	LM308	
	Silicon G	SG308	
AD311	Motorola	LM311	
	National	LM311	
	Raytheon	LM311	
	RCA	CA311	
	Signetics	LM311	
	Silicon G	SG311	
AD503	National	LH0042	
AD506	National	LH0022	
AD507	Datel	AM-462-2	
	Harris	**HA-2620**	**692**
AD509	Datel	AM-452-2	
	Harris	**HA-2520**	**680**
AD510	**PMI**	**OP-07**	**853**
AD513	National	LH0042	
AD516	National	LH0022	
AD559	Datel	DAC-IC8BC	
	Motorola	MC1408	
		MC1508	
AD562	**Harris**	**HI562**	**444**
	PMI	**SSS562**	**955**
AD583	**Datel**	**SHM-IC-1**	**393**
	Harris	**HA-2425**	**746**
AD710	Motorola	MC1710	
AD710	National	LM710	
	Raytheon	RM710	
	Signetics	μA710	
	Silicon G	SG710	
AD711	Motorola	MC1711	
	National	LM711	
	Raytheon	RM711	
	Signetics	μA711	
	Silicon G	SG711	
AD741	AMD	741	
	Fairchild	μA741	
	Motorola	MC1741	
	National	LM741	
	PMI	**SSS741**	**839**
	Raytheon	RM741	
	RCA	CA741	
	Signetics	μA741	
AD7501	Micro Power	MPS7501	
AD7502	Micro Power	MPS7502	
	RCA	CD4052	
AD7503	Micro Power	MPS7503	
AD7505	Siliconix	DG507	
AD7506	**Harris**	**HI506**	**418**
	Micro Power	MPS7506	
	RCA	CD4067	
	Siliconix	DG506	
AD7507	**Harris**	**HI507**	**418**
	Micro Power	MPS7507	
	RCA	CD4097	
AD7510	Micro Power	MPS7510	
AD7511	Micro Power	MPS7511	
AD7512	Micro Power	MPS7512	
AD7513	Micro Power	MPS7513	
	Siliconix	DG200	
AD7516	Fairchild	F4016	
	Micro Power	MPS7516	
	Mitel	SIL4016	
	Motorola	MC14016	
	National	CD4016	
	RCA	CD4016	
	Solitron	CM4016	
	SSS	**SCL4016**	
	TI	TP4016	
AD7519	Micro Power	MPS7519	
AD7520	Datel	DAC-HA10B	
	Intersil	AD7520	
	Micro Power	MPS7520	
AD7521	Datel	DAC-HA12B	
	Intersil	AD7521	
	Micro Power	MPS7521	
AD7522	Micro Power	MPS7522	
AD7530	Datel	DAC-HA10B	
	Intersil	AD7530	
AD7531	Datel	DAC-HA12B	
	Intersil	AD7531	
AD7550	Micro Power	MPS7550	
AD7570	Micro Power	MPS7570	
Beckman Instruments, Helipot Division			
877-80	Datel	DAC-HZ12B	
	Micro Net	DAC85	
877-85	Datel	DAC-HZ12B	
	Micro Net	DAC85	
Burr-Brown Research			
ADC80	Micro Net	ADC80	
ADC84	Micro Net	MN5240	
ADC85	Datel	ADC-HZ12BGZ	
	Micro Net	ADC85	
		MN5240	
DAC12	AD	DAC12	
DAC80	Beckman	877-80	
	Datel	DAC-HZ12B	
	Micro Net	DAC80	
	National	DAC1280	
DAC85	Beckman	877-85	
	Datel	DAC-HZ12B	
	Micro Net	DAC85	
	National	DAC1285	
DAC85/CCD	National	DAC1287	
MPC16S	Datel	MX-1606	
MPC16S	**Harris**	**HI506A**	**424**
MPC4D	Datel	MXD-409	
	Harris	HI509A	
MPC8D	Datel	MXD-807	
	Harris	**HI507A**	**424**
MPC8S	Datel	MX-808	
	Harris	**HI508A**	**430**
SHC25	National	LH0023	
3500	AD	AD3500	
3503	AD	AD540	
	Intersil	ICL3503	
3505	Datel	AM-450-2	
	Harris	**HA-2505**	**672**
3506	Datel	AM-460-2	
	Harris	**HA-2605**	**688**
3507	AD	AD509	
	Datel	AM-452-2	
	Harris	**HA-2525**	**680**
3508	AD	AD507	
	Datel	AM-462-2	
	Harris	**HA-2625**	**692**
♦3524	Intersil	ICL3524	
3542	AD	AD3542	
4201	AD	AD530	
4205	AD	AD532	
4213	AD	AD532	
4550	Intersil	ICL4550	
Datel Systems			
ADC-EK10B	Teledyne S	8701	
ADC-EK12B	Teledyne S	8702	
ADC-EK12D	Teledyne S	8750	
ADC-EK8B	Teledyne S	8700	
ADC-HZ12B	Burr-Brown	ADC85	
	Micro Net	ADC85	
ADC-MZ12	Micro Net	MN5240	
AM-405	**Harris**	**HA-2055**	**660**
AM-406	**Harris**	**HA-2065**	**664**
AM-450	Burr-Brown	3505	
	Harris	HA-2505	672
AM-452	AD	AD509	
	Burr-Brown	3507	
	Harris	**HA-2525**	**680**
	Teledyne P	TP1322	
AM-460	Burr-Brown	3506	
	Harris	**HA-2605**	**688**
AM-462	AD	AD507	
	Burr-Brown	3508	
	Harris	**HA-2625**	**692**
	Teledyne P	TP1321	
AM-464	**Harris**	**HA-2645**	**700**
AM-490-2	**Harris**	**HA-2905**	**724**
AM-500	Teledyne P	TP1430	
DAC-HZ12B	Beckman	877-80	
	Burr-Brown	DAC80	
	Micro Net	DAC80	
DAC-HZ12BM	Beckman	877-85	
	Burr-Brown	DAC85	
	Micro Net	DAC85	
MX-1606	**Harris**	**HI506A**	**424**
MX-808	**Harris**	**HI508A**	**430**
MXD-409	Harris	HI509A	
MXD-807	**Harris**	**HI507A**	**424**
SHM-IC-1	AD	AD583	
	Harris	**HA-2425**	**746**
	Teledyne P	TP4856	
VFQ-1	Teledyne S	9400	
Electronic Arrays			
EA1009	AMI	S2181	
EA1206	AMI	S1685	
EA12065	AMI	S1685	
EA12105	AMI	S1685	
EA1212	AMI	S1685	
EA2102	Mostek	MK4102	
	TI	TMS4035	
EA2308	Mostek	MK3000	
EA2708	AMD	2708	
	Fairchild	**2708**	**1093**
	Fujitsu	MB8518	
	Intel	2708	
	Mostek	MK2708	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Electronic Arrays (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
EA2708	Motorola	MCM2708	
	National	MM2708	
	TI	TMS2708	
♦EA3000	AMI	S8773	
♦EA3001	AMI	S8773	
♦EA3100	AMI	S8773	
♦EA3101	AMI	S8773	
♦EA3132	AMI	S8773	
♦EA3300	AMI	S8772	
♦EA3307	AMI	S8772	
EA3800	AMI	S8773	
EA4000	AMI	S8771	
	GI	RO3-5120	
EA4004	**AMI**	S8771	
EA4015	AMI	S8771	
EA4016	AMI	S8771	
EA4096	EMM/Semi	RO3-4096	
	Mostek	MK4096	
	Rockwell	1604	
EA4600	**AMI**	**S6831C**	**1062,1560**
EA4800	TI	TMS4800	
EA4900	Mostek	MK28000	
	TI	TMS4800	
EA5316	AMI	S1998	

EMM Semi., Div. of Electronic Memories & Magnetics

♦RA3-4256	GI	RA3-4256	
RO3-16384	GI	RO3-16384	
RO3-4096	GI	RO3-4096	
RO3-5120	GI	RO3-5120	
RO3-8316A	Intel	8316A	
RO3-8316B	Intel	8316B	
♦1217	GI	RA3-1217	
♦1218	GI	RA3-1218	
2114	Intel	2114	
3539	Fairchild	3539	
4104A	Nitron	NC4104A	
4200	GI	RA3-4200	
	NEC Micro	**μPD410**	**1420**
4202	**NEC Micro**	**μPD410**	**1420**
4402	GI	RA3-4402	

Exar Integrated Systems

XR-A100	Interdesign	Monochip A	
XR-B100	Interdesign	Monochip B	
XR-D100	Interdesign	Monochip D	
XR1310	Motorola	MC1310	
	National	LM1310	
XR1448	National	DS1488	
XR1458	Fairchild	μA1458	
	Motorola	MC1458	
	National	LM1458	
	Signetics	MC1458	
	TI	MC1458	
XR146	**National**	**LM146**	**766**
XR1488	Fairchild	μA1488	
	Motorola	MC1488	
	Signetics	MC1488	
XR1489A	Fairchild	μA1489A	
	Motorola	MC1489A	
	National	DS1489A	
	Signetics	MC1489A	
XR1524	Silicon G	SG1524	
	TI	SG1524	
XR1558	Fairchild	μA1558	
	Motorola	MC1558	
	National	LM1558	
	Signetics	MC1558	
	TI	MC1558	
XR1800	National	LM1800	
XR2003	Signetics	NE5503	
		ULN2003	
XR2201	Fairchild	μA9665	
		9665	
	Motorola	ULN2001	
	SGS	L201	
	Signetics	NE5501	
XR2201	Signetics	ULN2001	
	Silicon G	SG2001	
	Sprague	ULN-2001	
		ULS-2201	
	TI	ULN2001	
XR2202	Fairchild	μA9666	
		9666	
	Motorola	ULN2002	
	SGS	L202	
	Signetics	NE5502	
		ULN2002	
	Silicon G	SG2002	
	Sprague	ULN-2002	
		ULS-2002	
	TI	ULN2002	
XR2203	Fairchild	μA9667	
		9667	
	Motorola	ULN2003	
	SGS	L203	
	Silicon G	SG2003	
	Sprague	ULN-2003	
		ULS-2003	
	TI	ULN2003	
XR2204	Fairchild	μA9668	
		9668	
	Motorola	ULN2004	
	Signetics	NE5504	
		ULN2004	
	Silicon G	SG2004	
	Sprague	ULN-2004	
		ULS-2004	
	TI	ULN2004	
XR2206	Silicon G	SG2206	
XR2207	Raytheon	XR2207	
XR2211	Raytheon	XR2211	
XR2240	Fairchild	μA7240	
		7240	
	Intersil	8240	
XR246	**National**	**LM246**	**766**
XR2524	TI	SG2524	
XR2567	Raytheon	RC2567	
		XR2567	
XR3403	Fairchild	μA3403	
	Motorola	MC3403	
	Raytheon	RC3403	
XR346	**National**	**LM346**	**766**
XR3503	Motorola	MC3503	
	Raytheon	RM3503	
XR3524	Silicon G	SG3524	
	TI	SG3524	
XR4136	Fairchild	μA4136	
	PMI	**PM4136**	**864**
	Raytheon	RC4136	
	TI	RC4136	
XR4151	Raytheon	RC4151	
		RM4151	
		RV4151	
XR4152	**Raytheon**	**RC4152**	**968**
		RM4152	**968**
		RV4152	**968**
XR4156	**Raytheon**	**RC4156**	**971**
		RM4156	**971**
		RV4156	**971**
XR4157	Raytheon	RC4151	
XR4194	Raytheon	RC4194	
XR4195	Raytheon	RC4195	
XR4212	**Harris**	**HA-4741**	**735**
	Motorola	MC4741	
XR4558	Fairchild	μA4558	
	Motorola	MC4558	
		RC4558	
	Raytheon	RC4558	
	TI	RC4558	
XR4734	Raytheon	RC4739	
XR4741	**Harris**	**HA-4741**	**735**
	Motorola	MC4741	
	Raytheon	HA4741	
XR555	Fairchild	μA555	
	Motorola	MC1455	
	National	LM555	
	Signetics	NE555	
	TI	NE555	
XR556	Fairchild	μA556	
	Motorola	MC3456	
	National	LM556	
	Raytheon	RC556	
XR556	Signetics	NE556	
XR567	National	LM567	
	Signetics	NE567	
XR742	Fairchild	μA742	
XR8038	Intersil	8038	

Fairchild

μAF155	AMD	LF155	
	Intersil	LF155	
	Motorola	LF155	
	National	**LF155**	**786**
	PMI	**PM155**	**871**
	Raytheon	LF155	
	Signetics	LF155	
	TI	LF155	
μAF156	AMD	LF156	
	Intersil	LF156	
	Motorola	LF156	
	National	**LF156**	**786**
	PMI	**PM156**	**877**
	Raytheon	LF156	
	Signetics	LF156	
	TI	LF156	
μAF157	AMD	LF157	
	Intersil	LF157	
	Motorola	LF157	
	National	**LF157**	**786**
	PMI	**PM157**	**882**
	Raytheon	LF157	
	Signetics	LF157	
	TI	LF157	
μAF255	AMD	LF255	
	Intersil	LF255	
	Motorola	LF255	
	National	**LF255**	**786**
	PMI	**PM255**	**871**
	Raytheon	LF255	
	Signetics	LF255	
	TI	LF255	
μAF256	AMD	LF256	
	Intersil	LF256	
	Motorola	LF256	
	National	**LF256**	**786**
	PMI	**PM256**	**877**
	Raytheon	LF256	
	Signetics	LF256	
	TI	LF256	
μAF257	AMD	LF257	
	Intersil	LF257	
	Motorola	LF257	
	National	**LF257**	**786**
	PMI	**PM257**	**882**
	Raytheon	LF257	
	Signetics	LF257	
	TI	LF257	
μAF355	AMD	LF355	
	Intersil	LF355	
	Motorola	LF355	
	National	**LF355**	**786**
	PMI	**PM355**	**871**
	Raytheon	LF355	
	Signetics	LF355	
	TI	LF355	
μAF356	AMD	LF356	
	Intersil	LF356	
	Motorola	LF356	
	National	**LF356**	**786**
	PMI	**PM356**	**877**
	Raytheon	LF356	
	Signetics	LF356	
	TI	LF356	
μAF357	AMD	LF357	
	Intersil	LF357	
	Motorola	LF357	
	National	**LF357**	**786**
	PMI	**PM357**	**882**
	Raytheon	LF357	
	Signetics	LF357	
	TI	LF357	
μA0801	Datel	DAC-08B	
μA0802	Datel	DAC-IC8B	
	Motorola	MC1408	
		MC1508	
	PMI	**DAC-08**	**919**
μA0802	PMI	SSS1408	
		SSS1508	
μA101	AMD	LM101	
	Intersil	LM101	
	Motorola	LM101	
	National	LM101	
	RCA	CA101	
	Signetics	LM101	
	Silicon G	SG101	
	TI	LM101	
μA102	AMD	LM102	
	Intersil	LM102	
	Motorola	LM110	
	National	LM102	
	Silicon G	SG102	
μA104	Motorola	LM104	
	National	LM104	
	Raytheon	LM104	
	Silicon G	SG104	
	TI	LM104	
μA105	AMD	LM105	
	Intersil	LM105	
	Motorola	LM105	
	National	LM105	
	Raytheon	LM105	
	Silicon G	SG105	
	TI	LM105	
μA107	AMD	LM107	
	Intersil	LM107	
	Motorola	LM107	
	Silicon G	SG107	
μA108	AMD	LM108	
	Intersil	LM108	
	Motorola	LM108	
	National	LM108	
	PMI	**PM108**	**858**
	Raytheon	LM108	
	RCA	CA108	
	Signetics	LM108	
	Silicon G	SG108	
μA109	Motorola	LM109	
	National	LM109	
	Raytheon	LM109	
	Signetics	LM109	
	Silicon G	SG109	
	TI	LM109	
μA110	AMD	LM110	
	Intersil	LM110	
	Motorola	LM110	
	National	LM110	
	Silicon G	SG110	
μA111	AMD	LM111	
	Intersil	LM111	
	Raytheon	LM111	
	RCA	CA111	
	Signetics	LM111	
	Silicon G	SG111	
	TI	LM111	
μA1312	Motorola	MC1312	
μA139	AMD	LM139	
	RCA	CA139	
	Silicon G	SG139	
	TI	LM139	
μA1391	Motorola	MC1391	
	RCA	CA1391	
μA1394	Motorola	MC1394	
	RCA	CA1394	
μA1458	AMD	1458	
	Exar	XR1458	
	Harris	**HA-2655**	**704**
	Motorola	MC1458	
	National	LM1458	
	Raytheon	RC1458	
	RCA	CA1458	
	Signetics	MC1458	
	Silicon G	SG1458	
	TI	MC1458	
μA1488	Exar	XR1488	
	Signetics	MC1488	
	TI	SN75188	
μA1489	Signetics	MC1489	
	TI	SN85189	
μA1489A	Exar	XR1489A	
	Signetics	MC1489A	
	TI	SN75189A	
μA155	Motorola	LF155	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Fairchild (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
µA1558	AMD	1558	
	Exar	XR1558	
	Harris	**HA-2650**	**704**
	Motorola	MC1558	
	National	LM1558	
	Raytheon	RM1558	
	RCA	CA1558	
	Signetics	MC1558	
	Silicon G	SG1558	
	TI	MC1558	
µA156	Motorola	LF156	
µA157	Motorola	LF157	
µA201	AMD	LM201	
	Intersil	LM201	
	Motorola	LM201	
	National	LM201	
	RCA	CA201	
	Signetics	LM201	
	Silicon G	SG201	
	TI	LM201	
µA202	Intersil	LM202	
	Motorola	LM210	
	Silicon G	SG202	
µA204	Motorola	LM204	
	Silicon G	SG204	
	TI	LM204	
µA205	Intersil	LM205	
	Motorola	LM205	
	National	LM205	
	Raytheon	LM205	
	Silicon G	SG205	
	TI	LM205	
µA207	AMD	LM207	
	Intersil	LM207	
	Motorola	LM207	
	National	LM207	
	Raytheon	LM207	
	RCA	CA207	
	Signetics	LM207	
	Silicon G	SG207	
	TI	LM207	
µA208	AMD	LM208	
	Intersil	LM208	
	Motorola	LM208	
	National	LM208	
	PMI	PM208	
	Raytheon	LM208	
	RCA	CA208	
	Signetics	LM208	
	Silicon G	SG208	
µA209	Motorola	LM209	
	National	LM209	
	Raytheon	LM209	
	Signetics	LM209	
	Silicon G	SG209	
	TI	LM209	
µA210	Intersil	LM210	
	Motorola	MLM210	
	Silicon G	SG210	
µA211	Intersil	LM211	
	National	LM211	
	Raytheon	LM211	
	RCA	CA211	
	Signetics	LM211	
	Silicon G	SG211	
	TI	LM211	
µA2136	Motorola	MC1352	
µA2240	Exar	XR2240	
	TI	µA2240 ♦	
µA301	AMD	LM301	
	Intersil	LM301	
	Motorola	LM301	
	National	LM301	
	Raytheon	LM301	
	RCA	CA301	
	Signetics	LM301	
	Silicon G	SG301	
	TI	LM301	
µA3019	RCA	CA3019	
µA302	AMD	LM302	
	Intersil	LM302	
	Motorola	LM310	
	Silicon G	SG302	
µA3026	RCA	CA3026	
µA3036	RCA	CA3036	
µA3039	RCA	CA3039	
µA304	Motorola	LM304	
	National	LM304	
	Raytheon	LM304	
	Silicon G	SG304	
	TI	LM304	
µA3045	RCA	CA3045	
	Silicon G	SG3045	
µA3046	Motorola	MC3346	
	RCA	CA3046	
	Silicon G	SG3046	
µA305	AMD	LM305	
	Intersil	LM305	
	Motorola	LM305	
	National	LM305	
	Raytheon	LM305	
	Silicon G	SG305	
	TI	LM305	
µA3054	Motorola	CA3054	
	RCA	CA3054	
µA306	National	LM306	
	Raytheon	LM306	
µA3064	Motorola	MC1364	
	National	LM3064	
	RCA	CA3064	
	Sprague	ULN-2264	
µA3065	Motorola	MC1358	
	National	LM3065	
	RCA	CA3065	
	Sanyo	LA1365	
	Sprague	ULN-2165	
µA3066	RCA	CA3066	
µA3067	RCA	CA3067	
µA307	AMD	LM307	
	Intersil	LM307	
	Motorola	LM307	
	National	LM307	
	Raytheon	LM307	
	RCA	CA307	
	Signetics	LM307	
	Silicon G	SG307	
	TI	LM307	
µA3075	Motorola	MC1375	
	RCA	CA3075	
	Sprague	ULN-2129	
µA3076	RCA	CA3076	
µA308	AMD	LM308	
	Intersil	LM308	
	Motorola	LM308	
	National	LM308	
	PMI	PM308	
	Raytheon	LM308	
	RCA	CA308	
	Signetics	LM308	
	Silicon G	SG308	
µA3081	RCA	CA3018	
µA3086	Motorola	MC3386	
	RCA	CA3086	
	Silicon G	SG3886	
µA3089	RCA	CA3089	
	Siliconix	CA3089	
	Sprague	ULN-2289	
µA309	Motorola	LM309	
	Signetics	LM309	
	Silicon G	SG309	
	TI	LM309	
µA310	AMD	LM310	
	Intersil	LM310	
	Motorola	LM310	
	Silicon G	SG310	
µA311	AMD	LM311	
	Intersil	LM311	
	Motorola	LM311	
	Raytheon	LM311	
	RCA	CA311	
	Signetics	LM311	
	Silicon G	SG311	
	TI	LM311	
µA3301	Motorola	MC3301	
µA3302	Motorola	MC3302	
µA3303	Motorola	MC3303	
µA339	AMD	LM339	
	RCA	CA339	
	Silicon G	SG339	
µA3401	Motorola	MC3401	
	RCA	CA3401	
µA3403	Exar	XR3403	
	Motorola	MC3403	
	Raytheon	RC3403	
µA3503	Exar	XR3503	
	Motorola	MC3503	
	Raytheon	RM3503	
µA376	TI	LM376	
µA4136	Exar	XR4136	
	Raytheon	RC4136	
	TI	RC4136	
µA4558	Exar	XR4558	
	Motorola	MC4558	
µA555	Exar	XR555	
	Motorola	MC1455	
	Raytheon	RC555	
	Signetics	NE555	
	Silicon G	SG555	
	TI	NE555	
µA556	Exar	XR556	
	Motorola	MC3456	
	Raytheon	RC556	
	Signetics	NE556	
	Silicon G	SG556	
	TI	NE556	
µA702	Motorola	MC1712	
	Raytheon	RC702	
		RM702	
	TI	µA702	
µA703	National	LM703	
µA705	Sprague	ULN-2278	
µA706	SGS	TBA641	
µA709	Motorola	MC1709	
	National	LM709	
	Raytheon	RC709	
		RM709	
	Signetics	µA709	
	TI	µA709	
µA710	Motorola	MC1710	
	National	LM710	
	Raytheon	RC710	
		RM710	
	Signetics	µA710	
	Silicon G	SG710	
	TI	µA710	
µA711	Motorola	MC1711	
	National	LM711	
	Raytheon	RC711	
		RM711	
	Signetics	µA711	
	Silicon G	SG711	
	TI	µA711	
µA715	AMD	715	
µA720	RCA	CA3123	
	Sprague	ULN-2137	
µA723	AMD	723	
	Intersil	723	
	Motorola	MC1723	
	National	LM723	
	Raytheon	RC723	
		RM723	
	RCA	CA723	
	SGS	L123	
	Signetics	µA723	
	Silicon G	SG723	
	TI	µA723	
µA7240	Exar	XR2240	
µA725	AMD	725	
	PMI	**PM725**	**849**
		SSS725	**849**
	Raytheon	RC725	
		RM725	
µA732	National	LM1305	
µA733	AMD	733	
	Intersil	µA733	
	Motorola	MC1733	
	National	LM733	
	Raytheon	RC733	
		RM733	
	Signetics	µA733	
	Silicon G	SG733	
	TI	µA733	
µA734	Intersil	734	
µA739	Exar	XR4739	
	SGS	TBA231	
µA740	Intersil	µA740	
		LH0042	
	Signetics	µA740	
µA741	AMD	741	
	Intersil	741	
	Motorola	MC1741	
	National	LM741	
	PMI	**OP-02**	**839**
		PM741	**839**
		SSS741	**839**
	Raytheon	RC741	
		RM741	
	RCA	CA741	
	Signetics	µA741	
	Silicon G	SG741	
	TI	µA741	
µA742	Exar	XR742	
µA746	National	LM746	
	RCA	CA3072	
	Sprague	ULN-2114	
µA747	AMD	747	
	Motorola	MC1747	
	National	LM747	
	PMI	**OP-04**	**844**
		PM747	**844**
		SSS747	**844**
	Raytheon	RC747	
		RM747	
	RCA	CA747	
	Signetics	µA747	
	Silicon G	SG747	
	TI	µA747	
µA748	AMD	748	
	Intersil	748	
	Motorola	MC1748	
	National	LM101	
		LM201	
		LM748	
	Plessey	µA748	
	Raytheon	RC748	
		RM748	
	RCA	CA748	
	Signetics	µA748	
	Silicon G	SG748	
	TI	µA748	
µA749	Exar	XR4739	
µA753	Sprague	ULN-2209	
µA754	National	LM1596	
µA758	Exar	XR1800	
	Plessey	µA758	
	RCA	CA758	
	Signetics	µA758	
	Sprague	ULN-2244	
µA760	National	LM160	
µA763	National	LM1496	
µA775	Motorola	LM139	
µA776	**Harris**	**HA-2720**	**712**
	Motorola	MC1776	
	Silicon G	SG3250	
µA777	Intersil	777	
	Silicon G	SG777	
	TI	µA777	
µA78C05	Signetics	µA78M05	
µA78G	Signetics	µA78G	
µA78L02	Motorola	MC78L02	
µA78L05	Motorola	MC78L05	
	National	LM78L05	
	Plessey	SL8L05	
	Signetics	µA78L05	
	TI	µA78L05	
µA78L06	Motorola	MC78L06	
	National	LM78L06	
	Plessey	SL78L06	
µA78L08	Motorola	MC78L08	
	Plessey	SL78L08	
	TI	µA78L08	
µA78L09	TI	µA78L09	
µA78L10	TI	µA78L10	
µA78L12	Motorola	MC78L12	
	National	LM78L12	
	Plessey	SL78L12	
	Signetics	µA78L12	
	TI	µA78L12	
µA78L15	Motorola	MC78L15	
	National	LM78L15	
	Plessey	SL78L15	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
μA78L15	Signetics	μA78L15	
	TI	μA78L15	
μA78L18	Plessey	SL78L18	
μA78L20	Plessey	SL78L20	
		SL78L30	
	TI	μA78L20	
μA78L24	Plessey	SL78L24	
	Signetics	μA78L24	
μA78L26	Motorola	MC78L02	
		MC7802	
	Signetics	μA78L26	
	TI	μA78L02	
μA78L30	Plessey	SL78L30	
μA78L62	Signetics	μA78L06	
	TI	μA78L06	
μA78MG	Signetics	μA78MG	
μA78M05	Motorola	MC78M05	
	National	LM18M05	
	Plessey	SL78M05	
	Signetics	μA78M05	
	Silicon G	SG7805	
	TI	μA78M05	
μA78M06	Motorola	MC78M06	
	National	LM18M06	
	Plessey	SL78M06	
	Signetics	μA78M06	
	Silicon G	SG7806	
	TI	μA78M06	
μA78M08	Motorola	MC78M08	
	National	LM18M08	
	Plessey	SL78M08	
	Signetics	μA78M08	
	TI	μA78M08	
μA78M12	Motorola	MC78M12	
	Nitron	LM18M12	
	Plessey	SL78M12	
	Signetics	μA78M12	
	Silicon G	SG7812	
	TI	μA78M12	
μA78M15	Motorola	MC78M15	
	National	LM18M15	
	Plessey	SL78M15	
	Signetics	μA78M15	
	Silicon G	SG7815	
	TI	μA78M15	
μA78M18	Motorola	MC78M18	
	National	LM18M18	
		LM78M18	
	Plessey	SL78M18	
μA78M20	Motorola	MC78M20	
	Plessey	SL78M20	
	TI	μA78M20	
μA78M24	Motorola	MC78M24	
	National	LM18M24	
	Plessey	SL78M24	
	Signetics	μA78M24	
	Silicon G	SG7824	
	TI	μA78M24	
μA78M30	Plessey	SL78M30	
μA780	RCA	CA3070	
	Sprague	ULN-2124	
μA7805	Motorola	MC7805	
	National	**LM340-5**	**806**
		LM7805	
	Plessey	SL7805	
	Signetics	μA7805	
	Silicon G	SG7805	
	TI	μA7805	
μA7806	Motorola	MC7806	
	National	**LM340-6**	**806**
		LM7806	
	Plessey	μA7806	
	Signetics	μA7806	
	Silicon G	SG7806	
	TI	μA7806	
μA7808	Motorola	MC7808	
	National	**LM340-8**	**806**
		LM7808	
	Plessey	μA7808	
	Signetics	μA7808	
	Silicon G	SG7808	
	TI	μA7808	
μA781	RCA	CA3071	
μA781	Sprague	ULN-2127	
μA7812	Motorola	MC7812	
	National	**LM340-12**	**806**
		LM7812	
	Plessey	μA7812	
	Signetics	μA7812	
	Silicon G	SG7812	
	TI	μA7812	
μA7815	Motorola	MC7815	
	National	**LM340-15**	**806**
		LM7815	
	Plessey	μA7815	
	Signetics	μA7815	
	Silicon G	SG7815	
	TI	μA7815	
μA7818	Motorola	MC7818	
	National	**LM340-18**	**806**
		LM7818	
	Plessey	μA7818	
	Signetics	μA7818	
	Silicon G	SG7818	
	TI	μA7818	
μA7822	TI	μA7822	
μA7824	Motorola	MC7824	
	National	**LM340-24**	**806**
		LM7824	
	Plessey	μA7824	
	Signetics	μA7824	
	Silicon G	SG7824	
	TI	μA7824	
μA7830	Plessey	μA7830	
μA786	SGS	TAA630	
μA787	RCA	CA3126	
μA7885	TI	μA7885	
μA79G	Signetics	μA79G	
μA79MG	Signetics	μA79MG	
μA79M05	National	LM79M05	
	Signetics	μA79M05	
	TI	μA79M05	
μA79M06	National	LM79M06	
	Signetics	μA79M06	
	TI	μA79M06	
μA79M08	National	LM79M08	
	Signetics	μA79M08	
	TI	μA79M08	
μA79M12	National	LM79M12	
	Signetics	μA79M12	
	TI	μA79M12	
μA79M15	National	LM79M15	
	Signetics	μA79M15	
	TI	μA79M15	
μA79M18	National	LM79M18	
μA79M20	TI	μA79M20	
μA79M24	National	LM79M24	
	Signetics	μA79M24	
	TI	μA79M24	
μA7902	Motorola	MC7902	
μA7905	Motorola	MC7905	
	National	LM7905	
	Signetics	μA7905	
	Silicon G	SG120-5	
	TI	μA7905	
μA7906	Motorola	MC7906	
	National	LM7906	
	Signetics	μA7906	
μA7908	Motorola	MC7908	
	National	LM7908	
	Signetics	μA7908	
	TI	μA7908	
μA7912	Motorola	MC7912	
	National	LM7912	
	Signetics	μA7912	
	Silicon G	SG120-12	
	TI	μA7912	
μA7915	Motorola	MC7915	
	National	LM7915	
	Signetics	μA7915	
	Silicon G	SG120-15	
	TI	μA7915	
μA7918	Motorola	MC7918	
	National	LM7918	
	Signetics	μA7918	
	TI	μA7918	
μA7924	Motorola	MC7924	
	National	LM7924	
	Signetics	μA7924	
μA7924	TI	μA7924	
μA795	Motorola	MC1495	
		MC1595	
μA7952	TI	μA7952	
μA796	Motorola	MC1496	
		MC1596	
	Signetics	MC1496	
	Silicon G	SG1496	
		SG1596	
μA798	Motorola	MC3458	
		MC3558	
μA8T13	TI	SN55121	
		SN75121	
μA8T14	TI	SN55122	
		SN75122	
μA8T23	TI	SN75123	
μA8T24	TI	SN75124	
μA9665	Exar	XR2201	
μA9666	Exar	XR2202	
μA9667	Exar	XR2203	
μA9668	Exar	XR2204	
FQ3724	RCA	CA3724	
FQ3725	RCA	CA3725	
F10100	Motorola	MC10100	
	NEC America	μPB10100	
	Plessey	SP10100	
	Signetics	10100	
F10101	Hitachi	HD10101	
	Motorola	MC10101	
	NEC America	μPB10101	
	Plessey	SP10101	
	Signetics	10101	
F10102	Hitachi	HD10102	
	Motorola	MC10102	
	NEC America	μPB10102	
	Plessey	SP10102	
	Signetics	10102	
F10103	Motorola	MC10103	
	NEC America	μPB10103	
	Plessey	SP10103	
	Signetics	10103	
F10104	Hitachi	HD10104	
	Motorola	MC10104	
	Plessey	SP10104	
	Signetics	10104	
F10105	Hitachi	HD10105	
	Motorola	MC10105	
	National	DM10105	
	NEC America	μPB10105	
	Plessey	SP10105	
	Signetics	10105	
F10106	Hitachi	HD10106	
	Motorola	MC10106	
	National	DM10106	
	NEC America	μPB10106	
	Plessey	SP10106	
	Signetics	10106	
F10107	Hitachi	HD10107	
	Motorola	MC10107	
	NEC America	μPB10107	
	Plessey	SP10107	
	Signetics	10107	
F10109	Hitachi	HD10109	
	Motorola	MC10109	
	National	DM10109	
	NEC America	μPB10109	
	Plessey	SP10109	
	Signetics	10109	
F10110	Hitachi	HD10110	
	Motorola	MC10110	
	NEC America	μPB10110	
	Plessey	SP10110	
	Signetics	10110	
F10111	Hitachi	HD10111	
	Motorola	MC10111	
	National	DM10111	
	NEC America	μPB10111	
	Plessey	SP10111	
	Signetics	10111	
F10113	Motorola	MC10113	
	Plessey	SP10113	
	Signetics	10113	
F10114	Motorola	MC10114	
	Plessey	SP10114	
	Signetics	10114	
F10115	Motorola	MC10115	
F10115	National	DM10115	
	NEC America	μPB10115	
	Plessey	SP10115	
	Signetics	10115	
F10116	Hitachi	HD10116	
	Motorola	MC10116	
	National	DM10116	
	Plessey	SP10116	
	Signetics	10116	
F10117	Hitachi	HD10117	
	Motorola	MC10117	
	National	DM10117	
	NEC America	μPB10117	
	Plessey	SP10117	
	Signetics	10117	
F10118	Hitachi	HD10118	
	Motorola	MC10118	
	National	DM10118	
	NEC America	μPB10118	
	Plessey	SP10118	
	Signetics	10118	
F10119	Hitachi	HD10119	
	Motorola	MC10119	
	National	DM10119	
	Plessey	SP10119	
	Signetics	10119	
F10121	Hitachi	HD10121	
	Motorola	MC10121	
	National	DM10121	
	Plessey	SP10121	
	Signetics	10121	
F10123	Motorola	MC10123	
	Plessey	SP10123	
	Signetics	10123	
F10124	Hitachi	HD10124	
	Motorola	MC10124	
	National	DM10124	
	NEC America	μPB10124	
	Plessey	SP10124	
	Signetics	10124	
F10125	Hitachi	HD10125	
	Motorola	MC10125	
	Plessey	SP10125	
	Signetics	10125	
F10130	Hitachi	HD10130	
	Motorola	MC10130	
	Plessey	SP10130	
	Signetics	10130	
F10131	Hitachi	HD10131	
	Motorola	MC10131	
	NEC America	μPB10131	
	Plessey	SP10131	
	Signetics	10131	
F10132	Hitachi	HD10132	
	Motorola	MC10132	
	Signetics	10132	
F10133	Hitachi	HD10133	
	Motorola	MC10133	
	NEC America	μPB10133	
	Plessey	SP10133	
	Signetics	10133	
F10134	Hitachi	HD10134	
	Motorola	MC10134	
	Plessey	SP10134	
	Signetics	10134	
F10135	Motorola	MC10135	
	Plessey	SP10135	
	Signetics	10135	
F10136	Hitachi	HD10136	
	Motorola	MC10136	
	Plessey	SP10136	
	Signetics	10136	
F10137	Motorola	MC10137	
	Plessey	SP10137	
	Signetics	10137	
F10141	Motorola	MC10141	
	Plessey	SP10141	
	Signetics	10141	
F10144	Signetics	10144	
F10145	Hitachi	HD10145	
	Motorola	MC10145	
	Plessey	SP10145	
	Signetics	10145	
F10153	Motorola	MC10153	
F10158	Motorola	MC10158	
	NEC America	μPB10158	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
F10158	Signetics	10158	
F10159	Motorola	MC10159	
	Signetics	10159	
F10160	Hitachi	HD10160	
	Motorola	MC10160	
	Plessey	SP10160	
	Signetics	10160	
F10161	Hitachi	HD10161	
	Motorola	MC10161	
	NEC America	μPB10161	
	Plessey	SP10161	
	Signetics	10161	
F10162	Hitachi	HD10162	
	Motorola	MC10162	
	NEC America	μPB10162	
	Plessey	SP10162	
	Signetics	10162	
F10164	Hitachi	HD10164	
	Motorola	MC10164	
	NEC America	μPB10164	
	Plessey	SP10164	
	Signetics	10164	
	TI	SN10164	
F10165	Hitachi	HD10165	
	Motorola	MC10165	
	Plessey	SP10165	
	Signetics	10165	
F10166	Motorola	MC10166	
F10168	Motorola	MC10168	
F10170	Motorola	MC10170	
	Signetics	10170	
F10171	Motorola	MC10171	
	Plessey	SP10171	
	Signetics	10171	
F10172	Motorola	MC10172	
	Plessey	SP10172	
	Signetics	10172	
F10173	~~Motorola~~	~~MC10173~~	
	Plessey	SP10173	
	Signetics	10173	
F10174	Hitachi	HD10174	
	Motorola	MC10174	
	NEC America	μPB10174	
	Plessey	SP10174	
	Signetics	10174	
	TI	SN10174	
F10175	Hitachi	HD10175	
	Motorola	MC10175	
	Plessey	SP10175	
	Signetics	10175	
F10176	Motorola	MC10176	
	Plessey	SP10176	
	Signetics	10176	
F10177	Motorola	MC10177	
F10179	Hitachi	HD10179	
	Motorola	MC10179	
	Plessey	SP10179	
	Signetics	10179	
F10180	Hitachi	HD10180	
	Motorola	MC10180	
	NEC America	μPB10180	
	Plessey	SP10180	
	Signetics	10180	
F10181	Hitachi	HD10181	
	Motorola	MC10181	
	NEC America	μPB10181	
	Plessey	SP10181	
	Signetics	10181	
F10186	Motorola	MC10186	
F10192	Signetics	10192	
F10212	Motorola	MC10212	
	Plessey	SP10212	
F10405	TI	SN10147	
F10410	Fujitsu	MBM10410	
	TI	SN10144	
F10415	Fujitsu	MBM10415	
	Signetics	10146	
F10415A	Fujitsu	MBM10415A	
F16K	Intel	2116	
	Intersil	7116	
	Mostek	MK4116	
	Motorola	MCM4116	
	NEC Micro	**μPD416**	**1402**
F16K	Signetics	2690	
	TI	TMS4116	
	Zilog	Z6116	
F2901A	AMD	AM2901A	
	Fairchild	9409	
	Motorola	MC2901	
	National	DM2901A	
	NEC Micro	**μPB2901**	**1850**
	Raytheon	AM2901A	
	Signetics	MP2901	
F4001	Mitel	SIL4001	
	Motorola	MC14001	
	National	CD4001	
	NEC America	μPD4001	
	RCA	CD4001	
	SGS	HBF4001	
	Solitron	CM4001	
	SSS	SCL4001	
	TI	TP4001	
	Toshiba	TC4001	
F4002	Mitel	SIL4002	
	Motorola	MC14002	
	National	CD4002	
	NEC America	μPD4002	
	RCA	CD4002	
	SGS	HBF4002	
	Solitron	CM4002	
	SSS	SCL4002	
	TI	TP4002	
	Toshiba	TC4002	
F4006	Motorola	MC14006	
	National	CD4006	
	NEC America	μPD4006	
	RCA	CD4006	
	Solitron	CM4006	
	SSS	SCL4006	
F4007	Mitel	SIL4007	
	Motorola	MC14007	
	National	CD4007	
	RCA	CD4007	
	~~SGS~~	~~HBF4007~~	
	Solitron	CM4007	
	SSS	SCL4007	
	TI	TP4007	
	Toshiba	TC4007	
F4008	Motorola	MC14008	
	National	CD4008	
	RCA	CD4008	
	SGS	HBF4008	
	Solitron	CM4008	
	SSS	SCL4008	
	TI	TP4008	
	Toshiba	TC4008	
F40083	RCA	CD4008	
F40085	Harris	HD74C85	
	National	MM74C85	
	RCA	CD4063	
F40089	**National**	**MM74C89**	**1352**
F40097	Harris	HD80C97	
	National	MM80C97	
F40098	National	MM80C98	
F4011	Mitel	SIL4011	
	Motorola	MC14011	
	National	CD4011	
	NEC America	μPD4011	
	RCA	CD4011	
	SGS	HBF4011	
	Solitron	CM4011	
	SSS	SCL4011	
	TI	TP4011	
	Toshiba	TC4011	
F4012	Mitel	SIL4012	
	Motorola	MC14012	
	National	CD4012	
	NEC America	μPD4012	
	RCA	CD4012	
	SGS	HBF4012	
	Solitron	CM4012	
	SSS	SCL4012	
	TI	TP4012	
	Toshiba	TC4012	
F4013	Mitel	SIL4013	
	Motorola	MC14013	
	National	CD4013	
	NEC America	μPD4013	
	RCA	CD4013	
F4013	SGS	HBF4013	
	Solitron	CM4013	
	SSS	SCL4013	
	TI	TP4013	
	Toshiba	TC4013	
F4014	Mitel	SIL4014	
	Motorola	MC14014	
	National	CD4014	
	NEC America	μPD4014	
	RCA	CD4014	
	SGS	HBF4014	
	Solitron	CM4014	
	SSS	SCL4014	
	TI	TP4014	
	Toshiba	TC4014	
F4015	Mitel	SIL4015	
	Motorola	MC14015	
	National	CD4015	
	NEC America	μPD4015	
	RCA	CD4015	
	SGS	HBF4015	
	Solitron	CM4015	
	SSS	SCL4015	
	TI	TP4015	
	Toshiba	TC4015	
F4016	AD	AD7516	
	Micro Power	MPS7516	
	Mitel	SIL4016	
	Motorola	MC14016	
	National	CD4016	
	RCA	CD4016	
	Solitron	CM4016	
	SSS	SCL4016	
	TI	TP4016	
F40160	Harris	HD54C160	
		HD74C160	
	National	CD40160	
		MM54C160	
		MM74C160	
	RCA	CD40160	
	~~SSS~~	~~SCL4160~~	
	TI	TP4360	
F40161	Harris	HD54C161	
		HD74C161	
	National	CD40161	
		MM54C161	
		MM74C161	
	RCA	CD40161	
	SSS	SCL4161	
	TI	TP4361	
F40162	Harris	HD54C162	
		HD74C162	
	National	CD40162	
		MM54C162	
		MM74C162	
	RCA	CD40162	
	SSS	SCL4162	
	TI	TP4362	
F40163	Harris	HD54C163	
		HD74C163	
	National	CD40163	
		MM54C163	
		MM74C163	
	RCA	CD40163	
	SSS	SCL4163	
	TI	TP4363	
F4017	Mitel	SIL4017	
	Motorola	MC14017	
	National	CD4017	
	NEC America	μPD4017	
	RCA	CD4017	
	SGS	HBF4017	
	Solitron	CM4017	
	SSS	SCL4017	
	TI	TP4017	
	Toshiba	TC4017	
F40174	Harris	HD54C174	
		HD74C174	
	National	CD40174	
		MM54C174	
		MM74C174	
	RCA	CD40174	
F40175	Harris	HD54C175	
		HD74C175	
	National	MM54C175	
		MM74C175	
F4018	Mitel	SIL4018	
	National	CD4018	
	RCA	CD4018	
	SGS	HBF4018	
	Solitron	CM4018	
	SSS	SCL4018	
	TI	TP4018	
	Toshiba	TC4018	
F4019	Mitel	SIL4019	
	National	CD4019	
	NEC America	μPD4019	
	RCA	CD4019	
	SGS	HBF4019	
	Solitron	CM4019	
	SSS	SCL4019	
	TI	TP4019	
	Toshiba	TC4019	
F40192	Harris	HD54C192	
		HD74C192	
	National	CD40192	
		MM54C192	
		MM74C192	
	RCA	CD40192	
F40193	Harris	HD54C193	
		HD74C193	
	National	CD40193	
		MM54C193	
		MM74C193	
	RCA	CD40193	
F40194	NEC America	μPD4194	
	RCA	CD40194	
F40195	National	MM74C195	
F4020	Mitel	SIL4020	
	Motorola	MC14020	
	National	CD4020	
	NEC America	μPD4020	
	RCA	CD4020	
	SGS	HBF4020	
	Solitron	CM4020	
	SSS	SCL4020	
	TI	TP4020	
	Toshiba	TC4020	
F4021	Mitel	SIL4021	
	Motorola	MC14021	
	National	CD4021	
	NEC America	μPD4021	
	RCA	CD4021	
	Solitron	CM4021	
	SSS	SCL4021	
	TI	TP4021	
	Toshiba	TC4021	
F4022	Mitel	SIL4022	
	Motorola	MC14022	
	National	CD4022	
	RCA	CD4022	
	SGS	HBF4022	
	Solitron	CM4022	
	SSS	SCL4022	
	TI	TP4022	
	Toshiba	TC4022	
F4023	Mitel	SIL4023	
	Motorola	MC14023	
	National	CD4023	
	NEC America	μPD4023	
	RCA	CD4023	
	SGS	HBF4023	
	Solitron	CM4023	
	SSS	SCL4023	
	TI	TP4023	
	Toshiba	TC4023	
F4024	Mitel	SIL4024	
	Motorola	MC14024	
	National	CD4024	
	NEC America	μPD4024	
	RCA	CD4024	
	SGS	HBF4024	
	Solitron	CM4024	
	SSS	SCL4024	
	TI	TP4024	
	Toshiba	TC4024	
F4025	Mitel	SIL4025	
	Motorola	MC14025	
	National	CD4025	
	NEC America	μPD4025	
	RCA	CD4025	
	SGS	HBF4025	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Fairchild (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
F4025	Solitron	CM4025	
	SSS	SCL4025	
	TI	TP4025	
	Toshiba	TC4025	
F4027	Mitel	SIL4027	
	Motorola	MC14027	
	National	CD4027	
	NEC America	μPD4027	
	RCA	CD4027	
	SGS	HBF4027	
	Solitron	CM4027	
	SSS	SCL4027	
	TI	TP4027	
	Toshiba	TC4027	
F4028	Mitel	SIL4028	
	Motorola	MC14028	
	National	CD4028	
	NEC America	μPD4028	
	RCA	CD4028	
	SGS	HBF4028	
	Solitron	CM4028	
	SSS	SCL4028	
	TI	TP4028	
	Toshiba	TC4028	
F4029	Mitel	SIL4029	
	National	CD4029	
	NEC America	μPD4029	
	RCA	CD4029	
	SGS	HBF4029	
	Solitron	CM4029	
	SSS	SCL4029	
	TI	TP4029	
	Toshiba	TC4029	
F4030	Mitel	SIL4030	
	National	CD4030	
	NEC America	μPD4030	
	RCA	CD4030	
		CD4070	
	SGS	HBF4030	
	Solitron	CM4030	
	SSS	SCL4030	
	TI	TP4030	
	Toshiba	TC4030	
F4031	National	CD4031	
	RCA	CD4031	
F4034	Motorola	MC14034	
	National	CD4034	
	RCA	CD4034	
	Solitron	CM4034	
	SSS	SCL4034	
	Toshiba	TC4034	
F4035	Mitel	SIL4035	
	Motorola	MC14035	
	National	CD4035	
	NEC America	μPD4035	
	RCA	CD4035	
	SGS	HBF4035	
	Solitron	CM4035	
	SSS	SCL4035	
	TI	TP4035	
	Toshiba	TC4035	
F4040	Mitel	SIL4040	
	National	CD4040	
	NEC America	μPD4040	
	RCA	CD4040	
	Solitron	CM4040	
	SSS	SCL4040	
	TI	TP4040	
	Toshiba	TC4040	
F4041	National	CD4041	
	RCA	CD4041	
	Solitron	CM4041	
	SSS	CL4041	
		SCL4041	
F4042	Mitel	SIL4042	
	Motorola	MC14042	
	National	CD4042	
	NEC America	μPD4042	
	RCA	CD4042	
	SGS	HBF4042	
	Solitron	CM4042	
	SSS	SCL4042	
	TI	TP4042	
F4042	Toshiba	TC4042	
F4043	Mitel	SIL4043	
	Motorola	MC14043	
	National	CD4043	
	NEC America	μPD4043	
	RCA	CD4043	
	Solitron	CM4043	
	SSS	SCL4043	
	TI	TP4043	
	Toshiba	TC4043	
F4044	Mitel	SIL4044	
	Motorola	MC14044	
	National	CD4044	
	NEC America	μPD4044	
	RCA	CD4044	
	Solitron	CM4044	
	SSS	SCL4044	
	TI	TP4044	
	Toshiba	TC4044	
F4046	Mitel	SIL4046	
	Motorola	MC14046	
	National	CD4046	
	RCA	CD4046	
	Solitron	CM4046	
	SSS	SCL4046	
F4047	RCA	CD4047	
	Solitron	CM4047	
	TI	TP4047	
	Toshiba	TC4047	
F4049	Mitel	SIL4049	
	Motorola	MC14049	
	National	CD4049	
	NEC America	μPD4049	
	RCA	CD4049	
	SGS	HBF4049	
	Solitron	CM4049	
	SSS	SCL4049	
	TI	TP4049	
	Toshiba	TC4049	
F4050	Mitel	SIL4050	
	Motorola	MC14050	
	National	CD4050	
	NEC America	μPD4050	
	RCA	CD4050	
	SGS	HBF4050	
	Solitron	CM4050	
	SSS	SCL4050	
	TI	TP4050	
	Toshiba	TC4050	
F4051	Mitel	SIL4051	
	Motorola	MC14051	
	National	CD4051	
	NEC America	μPD4051	
	RCA	CD4051	
	Solitron	CM4051	
	SSS	SCL4051	
	TI	TP4051	
	Toshiba	TC4051	
F4052	Mitel	SIL4052	
	Motorola	MC14052	
	National	CD4052	
	NEC America	μPD4052	
	RCA	CD4052	
	Solitron	CM4052	
	SSS	SCL4052	
	TI	TP4052	
	Toshiba	TC4052	
F4053	Mitel	SIL4053	
	Motorola	MC14053	
	National	CD4053	
	NEC America	μPD4053	
	RCA	CD4053	
	Solitron	CM4053	
	SSS	SCL4053	
	Toshiba	TC4053	
F4066	Mitel	SIL4066	
	Motorola	MC14066	
	National	CD4066	
	NEC America	μPD4066	
	RCA	CD4066	
	SGS	HBF4066	
	Signetics	N4066	
	Solitron	CM4066	
	SSS	SCL4066	
	Toshiba	TC4066	
F4067	RCA	CD4067	
F4068	Mitel	SIL4068	
	Motorola	MC14068	
	NEC America	μPD4068	
	RCA	CD4068	
	Solitron	CM4068	
	SSS	SCL4068	
	TI	TP4068	
	Toshiba	TC4068	
F4069	Harris	HD74C04	
	Mitel	SIL4069	
	Motorola	MC14069	
	National	CD4069	
		MM74C04	
	NEC America	μPD4069	
	RCA	CD4069	
	Solitron	CM4069	
	SSS	SCL4069	
	TI	TP4069	
	Toshiba	TC4069	
F4070	Mitel	SIL4070	
	National	CD4070	
		MM74C86	
	RCA	CD4070	
	Solitron	CM4070	
	SSS	SCL4070	
F4071	Mitel	SIL4071	
	Motorola	MC14071	
	National	CD4071	
	NEC America	μPD4071	
	RCA	CD4071	
	Solitron	CM4071	
	SSS	SCL4071	
	TI	TP4071	
	Toshiba	TC4071	
F4072	Mitel	SIL4072	
	Motorola	MC14072	
	RCA	CD4072	
	SSS	SCL4072	
	TI	TP4072	
	Toshiba	TC4072	
F4073	Mitel	SIL4073	
	Motorola	MC14073	
	National	CD4073	
	NEC America	μPD4073	
	RCA	CD4073	
	Solitron	CM4073	
	SSS	SCL4073	
	TI	TP4073	
	Toshiba	TC4073	
F4075	Mitel	SIL4075	
	Motorola	MC14075	
	National	CD4075	
	NEC America	μPD4075	
	RCA	CD4075	
	SSS	SCL4075	
	TI	TP4075	
	Toshiba	TC4075	
F4076	Harris	HD74C173	
	Mitel	SIL4076	
	Motorola	MC14076	
	National	CD4076	
		MM74C173	
	RCA	CD4076	
	Solitron	CM4076	
	SSS	SCL4076	
F4077	Mitel	SIL4077	
	Motorola	MC14077	
	RCA	CD4077	
	Solitron	CM4077	
	SSS	SCL4077	
F4078	Mitel	SIL4078	
	Motorola	MC14078	
	NEC America	μPD4078	
	RCA	CD4078	
	Solitron	CM4078	
	SSS	SCL4078	
	Toshiba	TC4078	
F4081	Mitel	SIL4081	
	Motorola	MC14081	
	National	CD4081	
	NEC America	μPD4081	
	RCA	CD4081	
	Solitron	CM4081	
	SSS	SCL4081	
	TI	TP4081	
	Toshiba	TC4081	
F4082	Mitel	SIL4082	
	Motorola	MC14082	
	NEC America	μPD4082	
	RCA	CD4082	
	SSS	SCL4082	
	TI	TP4082	
	Toshiba	TC4082	
F4085	RCA	CD4085	
F4086	RCA	CD4086	
F4093	Motorola	MC14093	
	National	CD4093	
	NEC America	μPD4093	
	RCA	CD4093	
F4097	RCA	CD4097	
F4099	National	CD4099	
	NEC America	μPD4099	
	RCA	CD4099	
F4104	RCA	CD40104	
F4510	Mitel	SIL4510	
	Motorola	MC14510	
	National	CD4510	
	NEC America	μPD4510	
	RCA	CD40192	
		CD4510	
	SSS	SCL4510	
	Toshiba	TC4510	
F4511	Mitel	SIL4511	
	Motorola	MC14511	
	National	CD4511	
	NEC America	μPD4511	
	RCA	CD4511	
	Solitron	CM4511	
	SSS	SCL4511	
	TI	TP4511	
F4512	Mitel	SIL4512	
	Motorola	MC14512	
	National	CD4512	
	NEC America	μPD4512	
	SSS	SCL4512	
	TI	TP4512	
	Toshiba	TC4512	
F4514	Mitel	SIL4514	
	Motorola	MC14514	
	National	CD4514	
	NEC America	μPD4514	
	RCA	CD4514	
	Solitron	CM4514	
	SSS	SCL4514	
	Toshiba	TC4514	
F4515	Mitel	SIL4515	
	Motorola	MC14515	
	National	CD4515	
	NEC America	μPD4515	
	RCA	CD4515	
	SSS	SCL4515	
	Toshiba	TC4515	
F4516	Mitel	SIL4516	
	Motorola	MC14516	
	National	CD4516	
	NEC America	μPD4516	
	RCA	CD40193	
		CD4516	
	SSS	SCL4516	
	Toshiba	TC4516	
F4518	Mitel	SIL4518	
	Motorola	MC14518	
	National	CD4518	
	NEC America	μPD4518	
	RCA	CD4518	
	Solitron	CM4518	
	SSS	SCL4518	
	TI	TP4518	
	Toshiba	TC4518	
F4519	Motorola	MC14519	
	National	CD4519	
	NEC America	μPD4519	
	RCA	CD4019	
	TI	TP4519	
F4520	Mitel	SIL4520	
	Motorola	MC14520	
	National	CD4520	
	NEC America	μPD4520	
	RCA	CD4520	
	Solitron	CM4520	
	SSS	SCL4520	
	TI	TP4520	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Fairchild (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
F4520	Toshiba	TC4520	
F4522	Motorola	MC14522	
	National	CD4522	
	RCA	CD4018	
	SSS	SCL4522	
	TI	TP4522	
F4526	Motorola	MC14526	
	SSS	SCL4526	
	TI	TP4526	
F4527	RCA	CD4527	
	SSS	SCL4527	
F4528	Motorola	MC14528	
	National	CD4528	
	NEC America	μPD4528	
	RCA	CD4098	
		CD4528	
	SSS	SCL4528	
	Toshiba	TC4528	
F4531	Motorola	MC14531	
	RCA	CD40101	
	SSS	SCL4531	
	TI	TP4531	
F4532	Motorola	MC14532	
	RCA	CD4532	
	Toshiba	TC4532	
F4539	Motorola	MC14539	
	NEC America	μPD4539	
	Toshiba	TC4539	
F4553	Motorola	MC14553	
F4555	Motorola	MC14555	
	NEC America	μPD4555	
	RCA	CD4555	
	SSS	SCL4555	
F4556	Motorola	MC14556	
	NEC America	μPD4556	
	RCA	CD4556	
	SSS	SCL4556	
~~F4557~~	~~Motorola~~	~~MC14557~~	
	RCA	CD4031	
F4581	RCA	CD40181	
	SSS	SCL4581	
F4582	Motorola	MC14582	
	RCA	CD40182	
	SSS	SCL4582	
	TI	TP4582	
F4583	Motorola	MC14583	
	RCA	CD40100	
	Toshiba	TC4583	
F4585	RCA	CD4063	
	SSS	SCL4585	
F4702	**Harris**	**HD4702**	**1634**
F4703	RCA	CD40105	
F4710	RCA	CD4036	
		CD4039	
F4720	RCA	CD40061	
		CD4061	
F4731	RCA	CD4031	
F6800	**AMI**	**S6800**	**1538,1548**
	Hitachi	M6800	
	Motorola	MC6800	
F6820	**AMI**	**S6820**	**1556**
	Motorola	MC6820	
M4027	Mostek	MK4027	
	Motorola	MCM4027	
	NEC Micro	**μPD414**	**1395**
	Signetics	4027	
	TI	TMS4027	
SH3002	Siliconix	SI3002	
TBA810	RCA	CA810	
1103	AMI	S1103A	
1800	TI	SN151800	
		SN151900	
1802	TI	SN151802	
		SN151902	
1805	TI	SN151805	
		SN151905	
1806	TI	SN151806	
		SN151906	
1807	TI	SN151807	
		SN151907	
1808	TI	SN151808	
		SN151908	
1810	TI	SN151810	
1810	TI	SN151910	
1812	TI	SN151812	
		SN151912	
21L02	Signetics	21L02	
2102	Mostek	MK4102	
	NEC Micro	**μPD2102AL**	**1429**
	Signetics	21F02	
		2102	
2136	Motorola	MC1356	
	Sprague	ULN-2136	
3257	GI	RO5-2240S	
	Mostek	MK2302	
3260	AMI	S8564	
3329	AMI	S1685	
3330	AMI	S1685	
3331	AMI	S1685	
3337	AMI	S1685	
3341	AMD	3341	
3343	AMI	S2181	
	Signetics	2521	
3344	AMI	S2181	
	Signetics	2522	
3347	AMI	S2182	
	Intersil	IM7780	
	Signetics	2532	
	TI	TMS3120	
3349	Signetics	2518	
3355	Synertek	SY2833	
34XXX	Fairchild	F4XXX	
3501	AMI	S8457	
	National	MM3501	
	Rockwell	CRC3501	
3507	AMI	S8773	
3508	**NEC Micro**	**μPD2308**	**1478**
3512	AMI	S8773	
3513	AMI	S8773	
3514	AMI	S3514	
		S8772	
	Mostek	MK2600	
		MK2601	
	~~National~~	~~MM4233~~	
		MM5233	
3533	Signetics	2533	
3534	AMI	S2103	
3538	**NEC Micro**	**μPD2101AL**	**1424**
3539	**EMM/Semi**	**3539**	**1076**
3580	AMI	S8773	
3705	Siliconix	SI3705	
3730	AMI	S1757	
	GI	AY5-1013A	
3731	AMI	S1757	
3817	AMI	S1998	
3850	Mostek	MK3850	
3851	Mostek	MK3851	
3852	Mostek	MK3852	
3853	Mostek	MK3853	
3854	Mostek	MK3854	
3861	Mostek	MK3861	
3870	Mostek	MK3870	
4096	EA	EA4096	
	EMM/Semi	RO3-4096	
	Intersil	7005	
	Mostek	MK4096	
	NEC Micro	**μPD414**	**1395**
	Rockwell	1604	
54H00	ITT	ITT54H00	
	Motorola	MC54H00	
	National	DM54H00	
	Raytheon	54H00	
	Signetics	54H00	
	TI	SN54H00	
54H01	ITT	ITT54H01	
	Motorola	MC54H01	
	National	DM54H01	
	Raytheon	54H01	
	Signetics	54H01	
	TI	SN54H01	
54H04	ITT	ITT54H04	
	Motorola	MC54H04	
	National	DM54H04	
	Raytheon	54H04	
	Signetics	54H04	
	TI	SN54H04	
54H05	ITT	ITT54H05	
	Motorola	MC54H05	
	National	DM54H05	
54H05	Raytheon	54H05	
	Signetics	54H05	
	TI	SN54H05	
54H08	Motorola	MC54H08	
	National	DM54H08	
	Signetics	54H08	
54H10	ITT	ITT54H10	
	Motorola	MC54H10	
	National	DM54H10	
	Raytheon	54H10	
	Signetics	54H10	
	TI	SN54H10	
54H101	Motorola	MC54H101	
	Signetics	54H101	
	TI	SN54H101	
54H102	Motorola	MC54H102	
	Signetics	54H102	
	TI	SN54H102	
54H103	National	DM54H103	
	Signetics	54H103	
	TI	SN54H103	
54H106	National	DM54H106	
	Signetics	54H106	
	TI	SN54H106	
54H108	Motorola	MC54H108	
	National	DM54H108	
	Signetics	54H108	
	TI	SN54H108	
54H11	ITT	ITT54H11	
	Motorola	MC54H11	
	National	DM54H11	
	Raytheon	54H11	
	Signetics	54H11	
	TI	SN54H11	
54H15	Raytheon	54H15	
	TI	SN54H15	
54H183	TI	SN54H183	
54H20	ITT	ITT54H20	
	Motorola	MC54H20	
	National	DM54H20	
	~~Raytheon~~	~~54H20~~	
	Signetics	54H20	
	TI	SN54H20	
54H21	ITT	ITT54H21	
	Motorola	MC54H21	
	National	DM54H21	
	Signetics	54H21	
	TI	SN54H21	
54H22	Motorola	MC54H22	
	National	DM54H22	
	Raytheon	54H22	
	Signetics	54H22	
	TI	SN54H22	
54H30	ITT	ITT54H30	
	Motorola	MC54H30	
	National	DM54H30	
	Signetics	54H30	
	TI	SN54H30	
54H40	ITT	ITT54H40	
	Motorola	MC54H40	
	National	DM54H40	
	Raytheon	54H40	
	Signetics	54H40	
	TI	SN54H40	
54H50	ITT	ITT54H50	
	Motorola	MC54H50	
	National	DM54H50	
	Signetics	54H50	
	TI	SN54H50	
54H51	ITT	ITT54H51	
	Motorola	MC54H51	
	National	DM54H51	
	Signetics	54H51	
	TI	SN54H51	
54H52	Motorola	MC54H52	
	National	DM54H52	
	Signetics	54H52	
	TI	SN54H52	
54H53	ITT	ITT54H53	
	Motorola	MC54H53	
	National	DM54H53	
	Signetics	54H53	
	TI	SN54H53	
54H54	ITT	ITT54H54	
	Motorola	MC54H54	
	National	DM54H54	
54H54	Signetics	54H54	
	TI	SN54H54	
54H55	Motorola	MC54H55	
	National	DM54H55	
	Signetics	54H55	
	TI	SN54H55	
54H60	ITT	ITT54H60	
	Motorola	MC54H60	
	National	DM54H60	
	Signetics	54H60	
	TI	SN54H60	
54H61	Motorola	MC54H61	
	National	DM54H61	
	Signetics	54H61	
	TI	SN54H61	
54H62	Motorola	MC54H62	
	National	DM54H62	
	Signetics	54H62	
	TI	SN54H62	
54H71	Motorola	MC54H71	
	National	DM54H71	
	Signetics	54H71	
	TI	SN54H71	
54H72	Fairchild	54H73	
	ITT	ITT54H72	
	Motorola	MC54H72	
	National	DM54H72	
	Signetics	54H72	
	TI	SN54H72	
54H73	Fairchild	54H72	
	ITT	ITT54H72	
		ITT54H73	
	Motorola	MC54H73	
	National	DM54H72	
		DM54H73	
	Signetics	54H72	
		54H73	
	TI	SN54H72	
		SN54H73	
54H74	ITT	ITT54H74	
	~~Motorola~~	~~MC54H74~~	
	National	DM54H74	
	Raytheon	54H74	
	Signetics	54H74	
	TI	SN54H74	
54H76	National	DM54H76	
	Signetics	54H76	
	TI	SN54H76	
54H78	National	DM54H78	
	TI	SN54H78	
54LSO95	National	DM54LS395	
	Raytheon	**54LS395**	**291**
	Signetics	54LS395	
	TI	SN54LS395	
54LS00	Motorola	SN54LS00	
	National	DM54LS00	
	Raytheon	54LS00	
	Signetics	54LS00	
	TI	SN54LS00	
54LS01	National	DM54LS01	
	Raytheon	54LS01	
	Signetics	54LS01	
	TI	SN54LS01	
54LS02	Motorola	SN54LS02	
	National	DM54LS02	
	Raytheon	54LS02	
	Signetics	54LS02	
	TI	SN54LS02	
54LS03	Motorola	SN54LS03	
	National	DM54LS03	
	Raytheon	54LS03	
	Signetics	54LS03	
	TI	SN54LS03	
54LS04	Motorola	SN54LS04	
	National	DM54LS04	
	Raytheon	54LS04	
	Signetics	54LS04	
	TI	SN54LS04	
54LS05	Motorola	SN54LS05	
	National	DM54LS05	
	Raytheon	54LS05	
	Signetics	54LS05	
	TI	SN54LS05	
54LS08	Motorola	SN54LS08	
	National	DM54LS08	
	Raytheon	54LS08	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
54LS08	Signetics	54LS08	
	TI	SN54LS08	
54LS09	Motorola	SN54LS09	
	National	DM54LS09	
	Raytheon	54LS09	
	Signetics	54LS09	
	TI	SN54LS09	
54LS10	Motorola	SN54LS10	
	National	DM54LS10	
	Raytheon	54LS10	
	Signetics	54LS10	
	TI	SN54LS10	
54LS107	Motorola	SN54LS107	
	National	DM54LS107	
	Raytheon	54LS107	
	Signetics	54LS107	
	TI	SN54LS107	
54LS109	Motorola	SN54LS109	
	National	DM54LS109	
	Raytheon	54LS109	
	Signetics	54LS109	
	TI	SN54LS109	
54LS11	Motorola	SN54LS11	
	National	DM54LS11	
	Raytheon	54LS11	
	Signetics	54LS11	
	TI	SN54LS11	
54LS112	National	DM54LS112	
	Raytheon	54LS112	
	Signetics	54LS112	
	TI	SN54LS112	
54LS113	National	DM54LS113	
	Raytheon	54LS113	
	Signetics	54LS113	
	TI	SN54LS113	
54LS114	Motorola	SN54LS114	
	National	DM54LS114	
	Raytheon	54LS114	
	Signetics	54LS114	
	TI	SN54LS114	
54LS12	National	DM54LS12	
	Raytheon	54LS12	
	Signetics	54LS12	
	TI	SN54LS12	
54LS125	National	DM54LS125	
	Raytheon	54LS125	
	Signetics	54LS125	
	TI	SN54LS125	
54LS126	Motorola	SN54LS126	
	National	DM54LS126	
	Raytheon	54LS126	
	Signetics	54LS126	
	TI	SN54LS126	
54LS132	Motorola	SN54LS132	
	National	DM54LS132	
	Raytheon	**54LS132**	**264**
	Signetics	54LS132	
	TI	SN54LS132	
54LS136	Motorola	SN54LS136	
	Raytheon	54LS136	
	Signetics	54LS136	
	TI	SN54LS136	
54LS138	Motorola	SN54LS138	
	National	DM54LS138	
	Raytheon	54LS138	
	Signetics	54LS138	
	TI	SN54LS138	
54LS139	AMD	SN54LS139	
	Motorola	SN54LS139	
	National	DM54LS139	
	Raytheon	54LS139	
	Signetics	74LS139	
	TI	SN54LS139	
54LS14	Motorola	SN54LS14	
	National	DM54LS14	
	Raytheon	**54LS14**	**264**
	Signetics	54LS14	
	TI	SN54LS14	
54LS145	TI	SN54LS145	
54LS15	Motorola	SN54LS15	
	National	DM54LS15	
	Raytheon	54LS15	
	Signetics	54LS15	
54LS15	TI	SN54LS15	
54LS151	AMD	SN54LS151	
	Motorola	SN54LS151	
	National	DM54LS151	
	Raytheon	54LS151	
	Signetics	54LS151	
	TI	SN54LS151	
54LS152	Motorola	SN54LS152	
	Raytheon	54LS152	
	TI	SN54LS152	
54LS153	AMD	SN54LS153	
	Motorola	SN54LS153	
	National	DM54LS153	
	Raytheon	54LS153	
	Signetics	54LS153	
	TI	SN54LS153	
54LS155	Motorola	SN54LS155	
	National	DM54LS155	
	Raytheon	54LS155	
		74LS155	
	TI	SN54LS155	
54LS156	Motorola	SN54LS156	
	National	DM54LS156	
	Raytheon	54LS156	
	TI	SN54LS156	
54LS157	AMD	SN54LS157	
	Motorola	SN54LS157	
	National	DM54LS157	
	Raytheon	54LS157	
	Signetics	54LS157	
	TI	SN54LS157	
54LS158	Motorola	SN54LS158	
	National	DM54LS158	
	Raytheon	54LS158	
	Signetics	54LS158	
	TI	SN54LS158	
54LS160	AMD	SN54LS160	
	Motorola	SN54LS160	
	National	DM54LS160	
	Raytheon	54LS160	
	TI	SN54LS160	
54LS161	AMD	SN54LS161	
	Motorola	SN54LS161	
	National	DM54LS161	
	Raytheon	54LS161	
	Signetics	54LS161	
	TI	SN54LS161	
54LS162	AMD	SN54LS162	
	Motorola	SN54LS162	
	National	DM54LS162	
	Raytheon	54LS162	
	TI	SN54LS162	
54LS163	AMD	SN54LS163	
	Motorola	SN54LS163	
	National	DM54LS163	
	Raytheon	54LS163	
	Signetics	54LS163	
	TI	SN54LS163	
54LS164	AMD	SN54LS164	
	Motorola	SN54LS164	
	National	DM54LS164	
	Raytheon	**54LS164**	**272**
	Signetics	54LS164	
	TI	SN54LS164	
54LS165	TI	SN54LS165	
54LS168	AMD	SN54LS168	
	National	DM54LS168	
	TI	SN54LS168	
54LS169	AMD	SN54LS169	
	National	DM54LS169	
	TI	SN54LS169	
54LS170	AMD	AM54LS170	
	Motorola	SN54LS170	
	National	DM54LS170	
	Raytheon	54LS170	
	Signetics	54LS170	
	TI	SN54LS170	
54LS173	National	DM54LS173	
	Signetics	54LS173	
	TI	SN54LS173	
54LS174	AMD	SN54LS174	
	National	DM54LS174	
	Raytheon	54LS174	
	Signetics	54LS174	
	TI	SN54LS174	
54LS175	AMD	SN54LS175	
54LS175	Motorola	SN54LS175	
	National	DM54LS175	
	Raytheon	54LS175	
	Signetics	54LS175	
	TI	SN54LS175	
54LS181	AMD	SN54LS181	
	Motorola	SN54LS181	
	Raytheon	54LS181	
	Signetics	54LS181	
	TI	SN54LS181	
54LS190	AMD	SN54LS190	
	Motorola	SN54LS190	
	National	DM54LS190	
	Raytheon	54LS190	
	Signetics	54LS190	
	TI	SN54LS190	
54LS191	AMD	SN54LS191	
	Motorola	SN54LS191	
	National	DM54LS191	
	Raytheon	54LS191	
	Signetics	54LS191	
	TI	SN54LS191	
54LS192	AMD	SN54LS192	
	Motorola	SN54LS192	
	National	DM54LS192	
	Raytheon	54LS192	
	Signetics	54LS192	
	TI	SN54LS192	
54LS193	AMD	SN54LS193	
	Motorola	SN54LS193	
	National	DM54LS193	
	Raytheon	54LS193	
	Signetics	54LS193	
	TI	SN54LS193	
54LS194	AMD	SN54LS194A	
	Motorola	SN54LS194	
	Raytheon	54LS194A	
	TI	SN54LS194A	
54LS195	AMD	SN54LS195A	
	Motorola	SN54LS195	
	Raytheon	54LS195A	
	Signetics	54LS195A	
	TI	SN54LS195A	
54LS196	Motorola	SN54LS196	
	National	DM54LS196	
	Raytheon	54LS196	
	TI	SN54LS196	
54LS197	Motorola	SN54LS197	
	National	DM54LS197	
	Raytheon	54LS197	
	TI	SN54LS197	
54LS20	Motorola	SN54LS20	
	National	DM54LS20	
	Raytheon	54LS20	
	Signetics	54LS20	
	TI	SN54LS20	
54LS21	Motorola	SN54LS21	
	National	DM54LS21	
	Raytheon	54LS21	
	Signetics	54LS21	
	TI	SN54LS21	
54LS22	Motorola	SN54LS22	
	National	DM54LS22	
	Raytheon	54LS22	
	Signetics	54LS22	
	TI	SN54LS22	
54LS240	AMD	SN54LS240	
	MMI	54LS240	
	TI	SN54LS240	
54LS241	AMD	SN54LS241	
	MMI	54LS241	
	TI	SN54LS241	
54LS251	AMD	SN54LS251	
	Motorola	SN54LS251	
	Raytheon	54LS251	
	Signetics	54LS251	
	TI	SN54LS251	
54LS253	AMD	SN54LS253	
	Motorola	SN54LS253	
	National	DM54LS253	
	Raytheon	54LS253	
	Signetics	54LS253	
	TI	SN54LS253	
54LS255	Raytheon	54LS255	
54LS257	Motorola	SN54LS257	
	National	DM54LS257	
54LS257	Raytheon	54LS257	
	Signetics	54LS257	
	TI	SN54LS257	
54LS258	AMD	SN54LS258	
	Motorola	SN54LS258	
	Raytheon	54LS258	
	TI	SN54LS258	
54LS259	Motorola	SN54LS259	
	TI	SN54LS259	
54LS26	National	DM54LS26	
	Raytheon	54LS26	
	Signetics	54LS26	
	TI	SN54LS26	
54LS266	Motorola	SN54LS266	
	Raytheon	54LS266	
	Signetics	54LS266	
	TI	SN54LS266	
54LS27	Motorola	SN54LS27	
	National	DM54LS27	
	Raytheon	54LS27	
	Signetics	54LS27	
	TI	SN54LS27	
54LS279	Motorola	SN54LS279	
	National	DM54LS279	
	Raytheon	54LS279	
		74LS279	
	Signetics	54LS279	
	TI	SN54LS279	
54LS280	TI	SN54LS280	
54LS283	Motorola	SN54LS283	
	National	DM54LS283	
	Raytheon	54LS283	
	TI	SN54LS283	
54LS290	Signetics	54LS290	
	TI	SN54LS290	
54LS293	Signetics	54LS293	
	TI	SN54LS293	
54LS295	Motorola	SN54LS295	
	Raytheon	54LS295A	
	TI	SN54LS295B	
54LS298	Motorola	SN54LS298	
	Raytheon	54LS298	
	TI	SN54LS298	
54LS299	AMD	SN54LS299	
	Raytheon	54LS299	
	TI	SN54LS299	
54LS30	Motorola	SN54LS30	
	National	DM54LS30	
	Raytheon	54LS30	
	Signetics	54LS30	
	TI	SN54LS30	
54LS32	Motorola	SN54LS32	
	National	DM54LS32	
	Raytheon	54LS32	
	Signetics	54LS32	
	TI	SN54LS32	
54LS33	Raytheon	54LS33	
	Signetics	54LS33	
	TI	SN54LS33	
54LS352	National	DM54LS352	
	TI	SN54LS352	
54LS353	National	DM54LS353	
	TI	SN54LS353	
54LS365	Motorola	SN54LS365	
	Raytheon	**54LS365**	**286**
	Signetics	54LS365	
	TI	SN54LS365	
54LS366	Motorola	SN54LS366	
	Raytheon	**54LS366**	**286**
	Signetics	54LS366	
	TI	SN54LS366	
54LS367	Motorola	SN54LS367	
	Raytheon	**54LS367**	**286**
	Signetics	54LS367	
	TI	SN54LS367	
54LS368	Motorola	SN54LS368	
	Raytheon	**54LS368**	**286**
	Signetics	54LS368	
	TI	SN54LS368	
54LS37	Motorola	SN54LS37	
	National	DM54LS37	
	Raytheon	54LS37	
	Signetics	54LS37	
	TI	SN54LS37	
54LS38	Motorola	SN54LS38	
	National	DM54LS38	

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Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
54LS38	Raytheon	54LS38	
	Signetics	54LS38	
	TI	SN54LS38	
54LS390	TI	SN54LS390	
54LS393	TI	SN54LS393	
54LS40	Motorola	SN54LS40	
	National	DM54LS40	
	Raytheon	54LS40	
	Signetics	54LS40	
	TI	SN54LS40	
54LS42	Motorola	SN54LS42	
	National	DM54LS42	
	Raytheon	**54LS42**	**266**
	Signetics	54LS42	
	TI	SN54LS42	
54LS490	TI	SN54LS490	
54LS51	Motorola	SN54LS51	
	National	DM54LS51	
	Raytheon	54LS51	
	Signetics	54LS51	
	TI	SN54LS51	
54LS54	Motorola	SN54LS54	
	National	DM54LS54	
	Raytheon	54LS54	
	Signetics	54LS54	
	TI	SN54LS54	
54LS55	Motorola	SN54LS55	
	National	DM54LS55	
	Raytheon	54LS55	
	Signetics	54LS55	
	TI	SN54LS55	
54LS670	AMD	SN54LS670	
	Motorola	SN54LS670	
	National	DM54LS670	
	Raytheon	54LS670	
	Signetics	54LS670	
	TI	SN54LS670	
54LS73	~~Motorola~~	~~SN54LS73~~	
	National	DM54LS73	
	Raytheon	54LS73	
	Signetics	54LS73	
	TI	SN54LS73	
54LS74	Motorola	SN54LS74	
	National	DM54LS74	
	Raytheon	54LS74	
	Signetics	54LS74	
	TI	SN54LS74	
54LS75	National	DM54LS75	
	Raytheon	54LS75	
	Signetics	54LS75	
	TI	SN54LS75	
54LS77	Raytheon	54LS77	
	TI	SN54LS77	
54LS83	Motorola	SN54LS83	
	National	DM54LS83	
	Raytheon	54LS83A	
	TI	SN54LS83A	
54LS85	National	DM54LS85	
	Raytheon	54LS85	
	Signetics	54LS85	
	TI	SN54LS85	
54LS86	Motorola	SN54LS86	
	Raytheon	54LS86	
	Signetics	54LS86	
	TI	SN54LS86	
54LS90	Motorola	SN54LS90	
	National	DM54LS90	
	Raytheon	**54LS90**	**268**
	Signetics	54LS90	
	TI	SN54LS90	
54LS92	**Raytheon**	**54LS92**	**268**
54LS93	Motorola	SN54LS93	
	Raytheon	**54LS93**	**268**
	Signetics	54LS93	
	TI	SN54LS93	
54LS95B	Motorola	SN54LS95B	
	National	DM54LS95B	
	Raytheon	54LS95B	
	TI	SN54LS95B	
54S00	TI	SN54S00	
54S02	Signetics	54S02	
	TI	SN54S02	
54S03	TI	SN54S03	
54S04	Signetics	54S04	
	TI	SN54S04	
54S05	Signetics	54S05	
	TI	SN54S05	
54S08	Signetics	54S08	
	TI	SN54S08	
54S09	Signetics	54S09	
	TI	SN54S09	
54S10	TI	SN54S10	
54S11	Signetics	54S11	
	TI	SN54S11	
54S112	Motorola	SN54S112	
	TI	SN54S112	
54S113	Motorola	SN54S113	
	TI	SN54S113	
54S114	TI	SN54S114	
54S132	TI	SN54S132	
54S133	TI	SN54S133	
54S134	TI	SN54S134	
54S135	TI	SN54S135	
54S138	AMD	SN54S138	
	TI	SN54S138	
54S139	AMD	SN54S139	
	Signetics	54S139	
	TI	SN54S139	
54S15	Signetics	54S15	
	TI	SN54S15	
54S151	AMD	SN54S151	
	Signetics	54S151	
	TI	SN54S151	
54S153	AMD	SN54S153	
	Signetics	54S153	
	TI	SN54S153	
54S157	AMD	SN54S157	
	Signetics	54S157	
	TI	SN54S157	
54S158	AMD	SN54S158	
	Signetics	54S158	
	TI	SN54S158	
54S174	AMD	SN54S174	
	TI	~~SN54S174~~	
54S175	AMD	SN54S175	
	TI	SN54S175	
54S181	AMD	SN54S181	
	Signetics	54S181	
	TI	SN54S181	
54S182	TI	SN54S182	
54S194	AMD	SN54S194	
	TI	SN54S194	
54S195	AMD	SN54S195	
	TI	SN54S195	
54S20	TI	SN54S20	
54S22	National	DM54S22	
	Signetics	54S22	
	TI	SN54S22	
54S251	AMD	SN54S251	
	Signetics	54S251	
	TI	SN54S251	
54S253	AMD	SN54S253	
	Signetics	54S253	
54S257	AMD	SN54S257	
	Signetics	54S257	
	TI	SN74S257	
54S258	AMD	SN54S258	
	Signetics	54S258	
	TI	SN54S258	
54S30	TI	SN54S30	
54S32	Signetics	54S32	
	TI	SN54S32	
54S40	TI	SN54S40	
54S51	TI	SN54S51	
54S64	TI	SN54S64	
54S65	TI	SN54S65	
54S74	TI	SN54S74	
54S86	Signetics	54S86	
	TI	SN54S86	
5400	ITT	ITT5400	
	Motorola	MC5400	
	National	DM5400	
	Raytheon	5400	
	Signetics	5400	
	TI	SN5400	
5401	ITT	ITT5401	
	Motorola	MC5401	
	National	DM5401	
	Raytheon	5401	
5401	Signetics	5401	
	TI	SN5401	
5402	ITT	ITT5402	
	Motorola	MC5402	
	National	DM5402	
	Signetics	5402	
	TI	SN5402	
5403	ITT	ITT5403	
	Motorola	MC5403	
	National	DM5403	
	Raytheon	5403	
	Signetics	5403	
	TI	SN5403	
5404	ITT	ITT5404	
	Motorola	MC5404	
	National	DM5404	
	Raytheon	5404	
	Signetics	5404	
	TI	SN5404	
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	Motorola	MC5405	
	National	DM5405	
	Raytheon	5405	
	Signetics	5405	
	TI	SN5405	
5406	ITT	ITT5406	
	Motorola	MC5406	
	National	DM5406	
	Signetics	5406	
	TI	SN5406	
5407	ITT	ITT5407	
	Motorola	MC5407	
	National	DM5407	
	Signetics	5407	
	TI	SN5407	
5408	ITT	ITT5408	
	Motorola	MC5408	
	National	DM5408	
	Raytheon	5408	
	Signetics	5408	
	TI	SN5408	
5409	ITT	ITT5409	
	Motorola	MC5409	
	National	DM5409	
	Raytheon	5409	
	Signetics	5409	
	TI	SN5409	
5410	ITT	ITT5410	
	Motorola	MC5410	
	National	DM5410	
	Raytheon	5410	
	Signetics	5410	
	TI	SN5410	
54107	AMD	SN54107	
	ITT	ITT54107	
	Motorola	MC54107	
	National	DM54107	
	Signetics	54107	
	TI	SN54107	
5411	ITT	ITT5411	
	National	DM5411	
	Raytheon	5411	
	Signetics	5411	
	TI	SN5411	
54116	Signetics	54116	
	TI	SN54116	
5412	ITT	ITT5412	
	Motorola	MC5412	
	Raytheon	5412	
	Signetics	5412	
	TI	SN5412	
54121	ITT	ITT54121	
	Motorola	MC54121	
		MC9603	
	National	DM54121	
	Signetics	54121	
	TI	SN54121	
54122	ITT	ITT54122	
	Motorola	MC54122	
	TI	SN54122	
54123	AMD	SN54123	
	ITT	ITT54123	
	Motorola	MC54123	
	National	DM54123	
	Raytheon	54123	
	Signetics	54123	
54123	TI	SN54123	
54125	National	DM54125	
	Signetics	54125	
	TI	SN54125	
54126	National	DM54126	
	Signetics	54126	
	TI	SN54126	
5413	ITT	ITT5413	
	Motorola	MC5413	
	National	DM5413	
	Signetics	5413	
	TI	SN5413	
54132	Motorola	MC54132	
	National	DM54132	
	Signetics	54132	
	TI	SN54132	
54136	Raytheon	54136	
	TI	SN54136	
5414	Motorola	MC5414	
	National	DM5414	
	Signetics	5414	
	TI	SN5414	
54145	ITT	ITT54145	
	Motorola	MC54145	
		MC93145	
	National	DM54145	
	Raytheon	54145	
	Signetics	54145	
	TI	SN54145	
5415	Raytheon	5415	
54150	Motorola	MC54150	
		MC93150	
	National	DM54150	
	Raytheon	54150	
	Signetics	54150	
	TI	SN54150	
54151	ITT	ITT54151	
	Motorola	MC54151	
		MC93151	
	National	DM54151	
	Raytheon	54151	
	Signetics	54151	
	TI	SN54151	
		SN54151A	
54152	Motorola	MC54152	
		MC93152	
	Raytheon	54152	
	Signetics	54152	
	TI	SN54152A	
54153	AMD	SN54153	
	ITT	ITT54153	
	Motorola	MC54153	
		MC93153	
	National	DM54153	
	Raytheon	54153	
	Signetics	54153	
	TI	SN54153	
54154	AMD	SN54154	
	Motorola	MC54154	
		MC9311	
	National	DM54154	
	Raytheon	54154	
	Signetics	54154	
	TI	SN54154	
54155	ITT	ITT54155	
	Motorola	MC54155	
	National	DM54155	
	Raytheon	54155	
	Signetics	54155	
	TI	SN54155	
54156	ITT	ITT54156	
	Motorola	MC54156	
	National	DM54156	
	Raytheon	54156	
	Signetics	54156	
	TI	SN54156	
54157	AMD	SN54157	
	ITT	ITT54157	
	Motorola	MC54157	
		MC9322	
	National	DM54157	
	Raytheon	54157	
	Signetics	54157	
	TI	SN54157	
54158	Raytheon	54158	
54159	Raytheon	54159	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Fairchild (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
54159	TI	SN54159	
5416	ITT	ITT5416	
	Motorola	MC5416	
	National	DM5416	
	Signetics	5416	
	TI	SN5416	
54160	AMD	SN54160	
	ITT	ITT54160	
	Motorola	MC54160	
		MC9310	
	National	DM54160	
	Raytheon	54160	
	Signetics	54160	
	TI	SN54160	
54161	AMD	SN54161	
	ITT	ITT54161	
	Motorola	MC54161	
		MC9316	
	National	DM54161	
	Raytheon	54161	
	Signetics	54161	
	TI	SN54161	
54162	AMD	SN54162	
	ITT	ITT54162	
	Motorola	MC54162	
	National	DM54162	
	Raytheon	54162	
	Signetics	54162	
	TI	SN54162	
54163	AMD	SN54163	
	ITT	ITT54163	
	Motorola	MC54163	
	National	DM54163	
	Raytheon	54163	
	Signetics	54163	
	TI	SN54163	
54164	AMD	SN54164	
	ITT	ITT54164	
	National	DM54164	
	Raytheon	54164	
	Signetics	54164	
	TI	SN54164	
54165	Motorola	MC54165	
	National	DM54165	
	Raytheon	54165	
	Signetics	54165	
	TI	SN54165	
54166	National	DM54166	
	Raytheon	54166	
	Signetics	54166	
	TI	SN54166	
5417	ITT	ITT5417	
	Motorola	MC5417	
		MC9417	
	National	DM5417	
	Signetics	5417	
	TI	SN5417	
54170	National	DM54170	
	Raytheon	54170	
	Signetics	54170	
	TI	SN54170	
54173	National	DM54173	
	TI	SN54173	
54174	AMD	SN74174	
	Motorola	MC54174	
	National	DM54174	
	Raytheon	54174	
	Signetics	54174	
	TI	SN54174	
54175	AMD	SN54175	
	Motorola	MC54175	
	National	DM54175	
	Raytheon	54175	
	Signetics	54175	
	TI	SN54175	
54176	Motorola	MC54176	
		MC93176	
	National	DM54176	
	Signetics	54176	
	TI	SN54176	
54177	Motorola	MC54177	
		MC93177	
	National	DM54177	
54177	Signetics	54177	
	TI	SN54177	
54178	Motorola	MC93178	
	TI	SN54178	
54179	Motorola	MC93179	
	TI	SN54179	
54180	ITT	ITT54180	
	Motorola	MC54180	
		MC93180	
	National	DM54180	
	Raytheon	54180	
	Signetics	54180	
	TI	SN54180	
54181	AMD	SN54181	
	Motorola	MC54181	
		MC9341	
	National	DM54181	
	Raytheon	54181	
	Signetics	54181	
	TI	SN54181	
54182	AMD	SN54182	
	ITT	ITT54182	
	Motorola	MC54182	
		MC9342	
	National	DM54182	
	Raytheon	54182	
	Signetics	54182	
	TI	SN54182	
54190	ITT	ITT54190	
	Motorola	MC54190	
	National	DM54190	
	Raytheon	54190	
	Signetics	54190	
	TI	SN54190	
54191	ITT	ITT54191	
	Motorola	MC54191	
	National	DM54191	
	Raytheon	54191	
	Signetics	54191	
	TI	SN54191	
54192	AMD	SN54192	
	ITT	ITT54192	
	Motorola	MC54192	
		MC9360	
	National	DM54192	
	Raytheon	54192	
	Signetics	54192	
	TI	SN54192	
54193	AMD	SN54193	
	ITT	ITT54193	
	Motorola	MC54193	
		MC9366	
	National	DM54193	
	Raytheon	54193	
	Signetics	54193	
	TI	SN54193	
54194	AMD	SN54194	
	ITT	ITT54194	
	Motorola	MC54194	
	National	DM54194	
	Raytheon	54194	
	Signetics	54194	
	TI	SN54194	
54195	AMD	SN54195	
	ITT	ITT54195	
	Motorola	MC54195	
	National	DM54195	
	Raytheon	54195	
	Signetics	54195	
	TI	SN54195	
54196	Motorola	MC54196	
	National	DM54196	
	Signetics	54196	
	TI	SN54196	
54197	Motorola	MC54197	
	National	DM54197	
	Signetics	54197	
	TI	SN54197	
54198	National	DM54198	
	Raytheon	54198	
	Signetics	54198	
	TI	SN54198	
54199	National	DM54199	
	Raytheon	54199	
	Signetics	54199	
	TI	SN54199	
5420	ITT	ITT5420	
	Motorola	MC5420	
	National	DM5420	
	Raytheon	5420	
	Signetics	5420	
	TI	SN5420	
5421	ITT	ITT5421	
	Raytheon	5421	
	Signetics	5421	
5422	Raytheon	5422	
	TI	SN5422	
5423	Motorola	MC5423	
	National	DM5423	
	TI	SN5423	
5425	ITT	ITT5425	
	Motorola	MC5425	
	National	DM5425	
	TI	SN5425	
5426	ITT	ITT5426	
	Motorola	MC5426	
	National	DM5426	
	Signetics	5426	
	TI	SN5426	
5427	Motorola	MC5427	
	National	DM5427	
	TI	SN5427	
54279	Signetics	54279	
	TI	SN54279	
54283	Raytheon	54283	
	TI	SN54283	
54298	Motorola	MC54298	
	Signetics	54298	
	TI	SN54298	
5430	ITT	ITT5430	
	Motorola	MC5430	
	National	DM5430	
	Signetics	5430	
	TI	SN5430	
5432	ITT	ITT5432	
	National	DM5432	
	Signetics	5432	
	TI	SN5432	
5437	ITT	ITT5437	
	Motorola	MC5437	
	National	DM5437	
	Raytheon	5437	
	Signetics	5437	
	TI	SN5437	
5438	ITT	ITT5438	
	Motorola	MC5438	
	National	DM5438	
	Raytheon	5438	
	Signetics	5438	
	TI	SN5438	
5440	ITT	ITT5440	
	Motorola	MC5440	
	National	DM5440	
	Signetics	5440	
	TI	SN5440	
5441	National	DM5441	
5442	ITT	ITT5442	
	Motorola	MC5442	
		MC9352	
	National	DM5442	
	Raytheon	5442	
	Signetics	5442	
	TI	SN5442	
5443	ITT	ITT5443	
	Motorola	MC5443	
		MC9353	
	Raytheon	5443	
	Signetics	5443	
	TI	SN5443	
5444	ITT	ITT5444	
	Motorola	MC5444	
		MC9354	
	Raytheon	5444	
	Signetics	5444	
	TI	SN5444	
		SN5444A	
5445	ITT	ITT5445	
	Motorola	MC5445	
		MC9345	
	National	DM5445	
	Raytheon	5445	
	Signetics	5445	
5445	TI	SN5445	
		SN5445A	
5446	ITT	ITT5446	
	Motorola	MC5446	
		MC9357A	
	National	DM5446	
	Signetics	5446	
	TI	SN5446	
		SN5446A	
5447	ITT	ITT5447	
	Motorola	MC5447	
		MC9357B	
	National	DM5447	
	Signetics	5447	
	TI	SN5447	
		SN5447A	
5448	ITT	ITT5448	
	Motorola	MC5448	
		MC9358	
	National	DM5448	
	Signetics	5448	
	TI	SN5448	
5449	Motorola	MC5449	
		MC9359	
	TI	SN5449	
5450	ITT	ITT5450	
	Motorola	MC5450	
	National	DM5450	
	Signetics	5450	
	TI	SN5450	
5451	ITT	ITT5451	
	Motorola	MC5451	
	National	DM5451	
	Signetics	5451	
	TI	SN5451	
5453	ITT	ITT5453	
	Motorola	MC5453	
	National	DM5453	
	Signetics	5453	
	TI	SN5453	
5454	ITT	ITT5454	
	Motorola	MC5454	
	National	DM5454	
	Signetics	5454	
	TI	SN5454	
5460	Motorola	MC5460	
	National	DM5460	
	Signetics	5460	
	TI	SN5460	
5470	ITT	ITT5470	
	Motorola	MC5470	
	National	DM5470	
	Signetics	5470	
	TI	SN5470	
5472	ITT	ITT5472	
	Motorola	MC5472	
	National	DM5472	
	Signetics	5472	
	TI	SN5472	
5473	ITT	ITT5473	
	Motorola	MC5473	
	National	DM5473	
	Signetics	5473	
	TI	SN5473	
5474	ITT	ITT5474	
	Motorola	MC5474	
	National	DM5474	
	Raytheon	5474	
	Signetics	5474	
	TI	SN5474	
5475	ITT	ITT5475	
	Motorola	MC5475	
		MC9375	
	National	DM5475	
	Signetics	5475	
	TI	SN5475	
5476	ITT	ITT5476	
	Motorola	MC5476	
	National	DM5476	
	Signetics	5476	
	TI	SN5476	
5477	Motorola	MC5477	
		MC9377	
	Signetics	5477	
	TI	SN5477	
5480	ITT	ITT5480	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
5480	Motorola	MC5480	
		MC9380	
	Signetics	5480	
	TI	SN5480	
5481	Motorola	MC4304	
	TI	SN5481A	
5482	ITT	ITT5482	
	Motorola	MC5482	
		MC9382	
	TI	SN5482	
5483	Motorola	MC9383	
	Raytheon	5483	
	Signetics	5483A	
	TI	SN5483A	
5485	Motorola	MC5485	
	National	DM5485	
	Signetics	5485	
	TI	SN5485	
5486	ITT	ITT5486	
	Motorola	MC5486	
	National	DM5486	
	Raytheon	5486	
	Signetics	5486	
	TI	SN5486	
5488	Motorola	MCM4002	
	TI	SN5488A	
5489	AMD	SN5489	
		5889	
	Motorola	MC4064	
	National	**DM5489**	**1287**
	TI	SN5489	
5490	ITT	ITT5490	
	Motorola	MC5490	
		MC9390	
	National	DM5490	
	Signetics	5490	
	TI	SN5490	
		SN5490A	
5491	ITT	ITT5491	
	Motorola	MC5491	
		MC9391	
	National	DM5491	
	Signetics	5491	
	TI	SN5491	
		SN5491A	
5492	ITT	ITT5492	
	Motorola	MC5492	
		MC9392	
	National	DM5492	
	Signetics	5492	
	TI	SN5492	
		SN5492A	
5493	ITT	ITT5493	
	Motorola	MC5493	
		MC9393	
	National	DM5493	
	Signetics	5493	
	TI	SN5493	
		SN5493A	
5494	Motorola	MC5494	
		MC9394	
	Signetics	5494	
	TI	SN5494	
		SN5494A	
5495	ITT	ITT5495	
	Motorola	MC5495	
		MC9395	
	National	DM5495	
	Signetics	5495	
	TI	SN5495	
		SN5495A	
5496	ITT	ITT5496	
	Motorola	MC5496	
		MC9396	
	National	DM5496	
	Signetics	5496	
	TI	SN5496	
5497	Motorola	MC5497	
	TI	SN5497	
55107	AMD	SN55107B	
	Motorola	MC55107	
	National	**DS55107**	**504**
	Raytheon	RM55107	
55107	TI	SN55107	
55108	AMD	SN55108	
	Motorola	MC55108	
	National	**DS55108**	**504**
	Raytheon	RM55108	
	TI	SN55108	
55109	AMD	SN55109	
	Raytheon	RM55109	
	TI	SN55109	
55110	Raytheon	RM55110	
	TI	SN55110	
55121	TI	SN55121	
55122	TI	SN55122	
55232	TI	SN55232	
55233	TI	SN55232	
55234	TI	SN55234	
55235	Motorola	MC55325	
	TI	SN55234	
55238	TI	SN55238	
55239	TI	SN55239	
5524	Motorola	SN5524	
	National	DS5524	
	TI	SN5524	
5525	Motorola	SN5525	
	TI	SN5524	
5528	Motorola	MC5528	
	TI	SN5528	
5529	Motorola	MC5529	
	TI	SN5528	
55325	TI	SN55325	
55326	TI	SN55326	
55327	TI	SN55327	
5534	Motorola	MC5534	
5535	Motorola	MC5535	
5538	Motorola	MC5538	
5539	Motorola	MC5539	
55450	TI	SN55450	
55451	TI	SN55451	
55452	TI	SN55452	
55453	TI	SN55453	
55454	TI	SN55454	
55460	TI	SN55460	
55461	TI	SN55461	
55462	TI	SN55462	
55463	TI	SN55463	
55464	TI	SN55464	
55470	TI	SN55470	
55471	TI	SN55471	
55472	TI	SN55472	
55473	TI	SN55473	
55474	TI	SN55474	
6105	SSS	SCL5430	
74H00	Motorola	MC74H00	
	National	DM74H00	
	NEC America	μPB74H00	
	Raytheon	74H00	
	Signetics	74H00	
	TI	SN74H00	
74H01	ITT	ITT74H01	
	Motorola	MC74H01	
	National	DM74H01	
	NEC America	μPB74H01	
	Raytheon	74H01	
	Signetics	74H01	
	TI	SN74H01	
74H04	ITT	ITT74H04	
	Motorola	MC74H04	
	National	DM74H04	
	NEC America	μPB74H04	
	Raytheon	74H04	
	Signetics	74H04	
	TI	SN74H04	
74H05	ITT	ITT74H05	
	Motorola	MC74H05	
	National	DM74H05	
	Raytheon	74H05	
	Signetics	74H05	
	TI	SN74H05	
74H08	Motorola	MC74H08	
	National	DM74H08	
	Signetics	74H08	
74H10	ITT	ITT74H10	
	Motorola	MC74H10	
	National	DM74H10	
	NEC America	μPB74H10	
	Raytheon	74H10	
74H10	Signetics	74H10	
	TI	SN74H10	
74H101	Motorola	MC74H101	
	TI	SN74H101	
74H102	Motorola	MC74H102	
	Signetics	74H102	
	TI	SN74H102	
74H103	National	DM74H103	
	Signetics	74H103	
	TI	SN74H103	
74H105	Motorola	MC9001	
74H106	National	DM74H106	
	Signetics	74H106	
	TI	SN74H106	
74H108	Motorola	MC74H108	
	National	DM74H108	
	Signetics	74H108	
	TI	SN74H108	
74H11	ITT	ITT74H11	
	Motorola	MC74H11	
	National	DM74H11	
	Raytheon	74H11	
	Signetics	74H11	
	TI	SN74H11	
74H15	Raytheon	74H15	
	TI	SN74H15	
74H183	TI	SN74H183	
74H20	ITT	ITT74H20	
	Motorola	MC74H20	
	National	DM74H20	
	NEC America	μPB74H20	
	Raytheon	74H20	
	Signetics	74H20	
	TI	SN74H20	
74H21	ITT	ITT74H21	
	Motorola	MC74H21	
	National	DM74H21	
	Signetics	74H21	
	TI	SN74H21	
74H22	Motorola	MC74H22	
	National	DM74H22	
	Raytheon	74H22	
	Signetics	74H22	
	TI	SN74H22	
74H30	ITT	ITT74H30	
	Motorola	MC74H30	
	National	DM74H30	
	NEC America	μPB74H30	
	Signetics	74H30	
	TI	SN74H30	
74H40	ITT	ITT74H40	
	Motorola	MC74H40	
	National	DM74H40	
	NEC America	μPB74H40	
	Raytheon	74H40	
	Signetics	74H40	
	TI	SN74H40	
74H50	ITT	ITT74H50	
	Motorola	MC74H50	
	National	DM74H50	
	Signetics	74H50	
	TI	SN74H50	
74H51	ITT	ITT74H51	
	Motorola	MC74H51	
	National	DM74H51	
	NEC America	μPB74H51	
	Signetics	74H51	
	TI	SN74H51	
74H52	Motorola	MC74H52	
	National	DM74H52	
	Signetics	74H52	
	TI	SN74H52	
74H53	ITT	ITT74H53	
	Motorola	MC74H53	
	National	DM74H53	
	Signetics	74H53	
	TI	SN74H53	
74H54	ITT	ITT74H54	
	Motorola	MC74H54	
	National	DM74H54	
	Signetics	74H54	
	TI	SN74H54	
74H55	Motorola	MC74H55	
	National	DM74H55	
	Signetics	74H55	
	TI	SN74H55	
74H60	ITT	ITT74H60	
	Motorola	MC74H60	
	National	DM74H60	
	Signetics	74H60	
	TI	SN74H60	
74H61	Motorola	MC74H61	
	Signetics	74H61	
	TI	SN74H61	
74H62	Motorola	MC74H62	
	National	DM74H62	
	Signetics	74H62	
	TI	SN74H62	
74H71	Motorola	MC74H71	
	National	DM74H71	
	Signetics	74H71	
	TI	SN74H71	
74H72	ITT	ITT74H72	
	Motorola	MC74H72	
	National	DM74H72	
	Signetics	74H72	
	TI	SN74H72	
74H73	ITT	ITT74H73	
	Motorola	MC74H73	
	National	DM74H73	
	Signetics	74H73	
	TI	SN74H73	
74H74	ITT	ITT74H74	
	Motorola	MC74H74	
	National	DM74H74	
	Raytheon	74H74	
	Signetics	74H74	
	TI	SN74H74	
74H76	National	DM74H76	
	Signetics	74H76	
	TI	SN74H76	
74H78	National	DM74H78	
	TI	SN74H78	
74H87	Motorola	MC74H87	
	TI	SN74H87	
74LS00	ITT	ITT74LS00	
	Motorola	SN74LS00	
	National	DM74LS00	
	NEC America	μPB74LS00	
	Raytheon	74LS00	
	Signetics	74LS00	
	TI	SN74LS00	
74LS01	ITT	ITT74LS01	
	National	DM74LS01	
	Raytheon	74LS01	
	Signetics	74LS01	
	TI	SN74LS01	
74LS02	ITT	ITT74LS02	
	Motorola	SN74LS02	
	National	DM74LS02	
	NEC America	μPB74LS02	
	Raytheon	74LS02	
	Signetics	74LS02	
	TI	SN74LS02	
74LS03	ITT	ITT74LS03	
	Motorola	SN74LS03	
	National	DM74LS03	
	NEC America	μPB74LS03	
	Raytheon	74LS03	
	Signetics	74LS03	
	TI	SN74LS03	
74LS04	ITT	ITT74LS04	
	Motorola	SN74LS04	
	National	DM74LS04	
	NEC America	μPB74LS04	
	Raytheon	74LS04	
	Signetics	74LS04	
	TI	SN74LS04	
74LS05	ITT	ITT74LS05	
	Motorola	SN74LS05	
	National	DM74LS05	
	NEC America	μPB74LS05	
	Raytheon	74LS05	
	Signetics	74LS05	
	TI	SN74LS05	
74LS08	ITT	ITT74LS08	
	Motorola	SN74LS08	
	National	DM74LS08	
	NEC America	μPB74LS08	
	Raytheon	74LS08	
	Signetics	74LS08	
	TI	SN74LS08	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
74LS09	ITT	ITT74LS09	
	Motorola	SN74LS09	
	National	DM74LS09	
	Raytheon	74LS09	
	Signetics	74LS09	
	TI	SN74LS09	
74LS10	ITT	ITT74LS10	
	Motorola	SN74LS10	
	National	DM74LS10	
	NEC America	μPB74LS10	
	Raytheon	74LS10	
	Signetics	74LS10	
	TI	SN74LS10	
74LS107	ITT	ITT74LS107	
	National	DM74LS107	
	Raytheon	74LS107	
	Signetics	74LS107	
	TI	SN74LS107	
74LS109	ITT	ITT74LS109A	
	Motorola	SN74LS109	
	National	DM74LS109	
	NEC America	μPB74LS109	
	Raytheon	74LS109	
	Signetics	74LS109	
	TI	SN74LS109	
74LS11	ITT	ITT74LS11	
	Motorola	SN74LS11	
	National	DM74LS11	
	NEC America	μPB74LS11	
	Raytheon	74LS11	
	Signetics	74LS11	
	TI	SN74LS11	
74LS112	ITT	ITT74LS112	
	National	DM74LS112	
	NEC America	μPB74LS112	
	Raytheon	74LS112	
	Signetics	74LS112	
	TI	SN74LS112	
74LS113	ITT	ITT74LS113	
	National	DM74LS113	
	NEC America	μPB74LS113	
	Raytheon	74LS113	
	Signetics	74LS113	
	TI	SN74LS113	
74LS114	ITT	ITT74LS114	
	Motorola	SN74LS114	
	National	DM74LS114	
	Raytheon	74LS114	
	Signetics	74LS114	
	TI	SN74LS114	
74LS12	National	DM74LS12	
	Raytheon	74LS12	
	Signetics	74LS12	
	TI	SN74LS12	
74LS125	ITT	ITT74LS125	
	National	DM74LS125	
	Raytheon	74LS125	
	Signetics	74LS125	
	TI	SN74LS125	
		SN74LS125A	
74LS126	ITT	ITT74LS126	
	Motorola	SN74LS126	
	National	DM74LS126	
	Raytheon	74LS126	
	Signetics	74LS126	
	TI	SN74LS126	
		SN74LS126A	
74LS13	ITT	ITT74LS13	
	Motorola	SN74LS13	
	National	DM74LS13	
	Raytheon	**74LS13**	**264**
	Signetics	74LS13	
	TI	SN74LS13	
74LS132	ITT	ITT74LS132	
	Motorola	SN74LS132	
	National	DM74LS132	
	Raytheon	**74LS132**	**264**
	Signetics	74LS132	
	TI	SN74LS132	
74LS136	ITT	ITT74LS136	
	Motorola	SN74LS136	
	National	DM74LS136	
	Raytheon	74LS136	
74LS136	Signetics	74LS136	
	TI	SN74LS136	
74LS138	AMD	SN74LS138	
	ITT	ITT74LS138	
	Motorola	SN74LS138	
	National	DM74LS138	
	NEC America	μPB74LS138	
	Raytheon	74LS138	
	Signetics	74LS138	
	TI	SN74LS138	
74LS139	AMD	SN74LS139	
	ITT	ITT74LS139	
	Motorola	SN74LS139	
	National	DM74LS139	
	NEC America	μPB74LS139	
	Raytheon	74LS139	
	Signetics	74LS139	
	TI	SN74LS139	
74LS14	ITT	ITT74LS14	
	Motorola	SN74LS14	
	National	DM74LS14	
	Raytheon	**74LS14**	**264**
	Signetics	74LS14	
	TI	SN74LS14	
74LS145	Signetics	74LS145	
	TI	SN74LS145	
74LS15	ITT	ITT74LS15	
	Motorola	SN74LS15	
	National	DM74LS15	
	Raytheon	74LS15	
	Signetics	74LS15	
	TI	SN74LS15	
74LS151	AMD	SN74LS151	
	ITT	ITT74LS151	
	Motorola	SN74LS151	
	National	DM74LS151	
	NEC America	μPB74LS151	
	Raytheon	74LS151	
	Signetics	74LS151	
	TI	SN74LS151	
74LS152	Motorola	SN74LS152	
	Raytheon	74LS152	
74LS153	AMD	SN74LS153	
	ITT	ITT74LS153	
	Motorola	SN74LS153	
	National	DM74LS153	
	NEC America	μPB74LS153	
	Raytheon	74LS153	
	Signetics	74LS153	
	TI	SN74LS153	
74LS155	ITT	ITT74LS155	
	Motorola	SN74LS155	
	National	DM74LS155	
	NEC America	μPB74LS155	
	Raytheon	74LS155	
	Signetics	74LS155	
	TI	SN74LS155	
74LS156	ITT	ITT74LS156	
	Motorola	SN74LS156	
	National	DM74LS156	
	Raytheon	74LS156	
	Signetics	74LS156	
	TI	SN74LS156	
74LS157	AMD	SN74LS157	
	ITT	ITT74LS157	
	Motorola	SN74LS157	
	National	DM74LS157	
	NEC America	μPB74LS157	
	Raytheon	74LS157	
	Signetics	74LS157	
	TI	SN74LS157	
74LS158	AMD	SN74LS158	
	ITT	ITT74LS158	
	Motorola	SN74LS158	
	National	DM74LS158	
	Raytheon	74LS158	
	Signetics	74LS158	
	TI	SN74LS158	
74LS160	AMD	SN74LS160	
	ITT	ITT74LS160	
	Motorola	SN74LS160	
	National	DM74LS160	
	Raytheon	74LS160	
	Signetics	74LS160	
	TI	SN74LS160	
74LS161	AMD	SN74LS161	
74LS161	ITT	ITT74LS161	
	Motorola	SN74LS161	
	National	DM74LS161	
	NEC America	μPB74LS161	
	Raytheon	74LS161	
	Signetics	74LS161	
	TI	SN74LS161	
74LS162	AMD	SN74LS162	
	ITT	ITT74LS162	
	Motorola	SN74LS162	
	National	DM74LS162	
	Raytheon	74LS162	
	Signetics	74LS162	
	TI	SN74LS162	
74LS163	AMD	SN74LS163	
	ITT	ITT74LS163	
	Motorola	SN74LS163	
	National	DM74LS163	
	Raytheon	74LS163	
	Signetics	74LS163	
	TI	SN74LS163	
74LS164	AMD	SN74LS164	
	ITT	ITT74LS164	
	Motorola	SN74LS164	
	National	DM74LS164	
	NEC America	μPB74LS164	
	Raytheon	**74LS164**	**272**
	Signetics	74LS164	
	TI	SN74LS164	
74LS165	TI	SN74LS165	
74LS168	AMD	SN74LS168	
	National	DM74LS168	
	TI	SN74LS168	
74LS169	AMD	SN74LS169	
	National	DM74LS169	
	TI	SN74LS169	
74LS170	AMD	SN74LS170	
	ITT	ITT74LS170	
	Motorola	SN74LS170	
	National	DM74LS170	
	Raytheon	74LS170	
	Signetics	74LS170	
	TI	SN74LS170	
74LS173	National	DM74LS173	
	Signetics	74LS173	
	TI	SN74LS173	
74LS174	AMD	SN74LS174	
	ITT	ITT74LS174	
	Motorola	SN74LS174	
	National	DM74LS174	
	Raytheon	74LS174	
	Signetics	74LS174	
	TI	SN74LS174	
74LS175	AMD	SN74LS175	
	ITT	ITT74LS175	
	Motorola	SN74LS175	
	National	DM74LS175	
	NEC America	μPB74LS175	
	Raytheon	74LS175	
	Signetics	74LS175	
	TI	SN74LS175	
74LS181	AMD	SN74LS181	
	Motorola	SN74LS181	
	Raytheon	74LS181	
	Signetics	74LS181	
	TI	SN74LS181	
74LS190	AMD	SN74LS190	
	ITT	ITT74LS190	
	Motorola	SN74LS190	
	National	DM74LS190	
	Raytheon	74LS190	
	Signetics	74LS190	
	TI	SN74LS190	
74LS191	AMD	SN74LS191	
	ITT	ITT74LS191	
	Motorola	SN74LS191	
	National	DM74LS191	
	Raytheon	74LS191	
	Signetics	74LS191	
	TI	SN74LS191	
74LS192	AMD	SN74LS192	
	ITT	ITT74LS192	
	Motorola	SN74LS192	
	National	DM74LS192	
	NEC America	μPB74LS192	
	Raytheon	74LS192	
74LS192	Signetics	74LS192	
	TI	SN74LS192	
74LS193	AMD	SN74LS193	
	ITT	ITT74LS193	
	Motorola	SN74LS193	
	National	DM74LS193	
	NEC America	μPB74LS193	
	Raytheon	74LS193	
	Signetics	74LS193	
	TI	SN74LS193	
74LS194	AMD	SN74LS194A	
	ITT	ITT74LS194A	
	Motorola	SN74LS194	
	NEC America	μPB74LS194	
	Raytheon	74LS194A	
	Signetics	74LS194A	
	TI	SN74LS194A	
74LS195	AMD	SN74LS195A	
	ITT	ITT74LS195A	
	Motorola	SN74LS195	
	NEC America	μPB74LS195	
	Raytheon	74LS195A	
	Signetics	74LS195A	
	TI	SN74LS195A	
74LS196	ITT	ITT74LS196	
	Motorola	SN74LS196	
	National	DM74LS196	
	Raytheon	74LS196	
	Signetics	74LS196	
	TI	SN74LS196	
74LS197	ITT	ITT74LS197	
	Motorola	SN74LS197	
	National	DM74LS197	
	Raytheon	74LS197	
	Signetics	74LS197	
	TI	SN74LS197	
74LS20	ITT	ITT74LS20	
	Motorola	SN74LS20	
	National	DM74LS20	
	NEC America	μPB74LS20	
	Raytheon	74LS20	
	Signetics	74LS20	
	TI	SN74LS20	
74LS21	ITT	ITT74LS21	
	Motorola	SN74LS21	
	National	DM74LS21	
	NEC America	μPB74LS21	
	Raytheon	74LS21	
	Signetics	74LS21	
	TI	SN74LS21	
74LS22	ITT	ITT74LS22	
	Motorola	SN74LS22	
	National	DM74LS22	
	Raytheon	74LS22	
	Signetics	74LS22	
	TI	SN74LS22	
74LS221	ITT	ITT74LS221	
	Motorola	SN74LS221	
	National	DM74LS221	
	Raytheon	**74LS221**	**275**
	Signetics	74LS221	
	TI	SN74LS221	
74LS240	AMD	SN74LS240	
	ITT	ITT74LS240	
	MMI	74LS240	
	Motorola	SN74LS240	
	Raytheon	**74LS240**	**279**
	Signetics	74LS240	
	TI	SN74LS240	
74LS241	AMD	SN74LS241	
	ITT	ITT74LS241	
	MMI	74LS241	
	Motorola	SN74LS241	
	Raytheon	**74LS241**	**279**
	Signetics	74LS241	
	TI	SN74LS241	
74LS242	AMD	SN74LS242	
	ITT	ITT74LS242	
	Motorola	SN74LS242	
	Raytheon	**74LS242**	**282**
	Signetics	74LS242	
	TI	SN74LS242	
74LS243	AMD	SN74LS243	
	ITT	ITT74LS243	
	Motorola	SN74LS243	
	Raytheon	**74LS243**	**282**

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Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
74LS243	Signetics	74LS243	
	TI	SN74LS243	
74LS244	AMD	SN74LS244	
	ITT	ITT74LS244	
	MMI	74LS244	
	Motorola	SN74LS244	
	Raytheon	**74LS244**	**279**
	Signetics	74LS244	
	TI	SN74LS244	
74LS247	National	DM74LS247	
	TI	SN74LS247	
74LS248	National	DM74LS248	
	TI	SN74LS248	
74LS249	National	DM74LS249	
	TI	SN74LS249	
74LS251	AMD	SN74LS251	
	ITT	ITT74LS251	
	Motorola	SN74LS251	
	National	DM74LS251	
	NEC America	μPB74LS251	
	Raytheon	74LS251	
	Signetics	74LS251	
	TI	SN74LS251	
74LS253	AMD	SN74LS253	
	ITT	ITT74LS253	
	Motorola	SN74LS253	
	National	DM74LS253	
	NEC America	μPB74LS253	
	Raytheon	74LS253	
	Signetics	74LS253	
	TI	SN74LS253	
74LS255	Raytheon	74LS255	
74LS257	AMD	SN74LS257	
	ITT	ITT74LS257	
	Motorola	SN74LS257	
	National	DM74LS257	
	NEC America	μPB74LS257	
	Raytheon	74LS257	
	Signetics	74LS257	
	TI	SN74LS257	
74LS258	AMD	SN74LS258	
	ITT	ITT74LS258	
	Motorola	SN74LS258	
	National	DM74LS258	
	NEC America	μPB74LS258	
	Raytheon	74LS258	
	Signetics	74LS258	
	TI	SN74LS258	
74LS259	ITT	ITT74LS259	
	Motorola	SN74LS259	
	TI	SN74LS259	
74LS26	National	DM74LS26	
	Raytheon	74LS26	
	Signetics	74LS26	
	TI	SN74LS26	
74LS260	Signetics	74LS260	
74LS266	Fairchild	74LS266	
	ITT	ITT74LS266	
	Motorola	SN74LS266	
	Raytheon	74LS266	
	Signetics	74LS266	
	TI	SN74LS266	
74LS27	ITT	ITT74LS27	
	Motorola	SN74LS27	
	National	DM74LS27	
	NEC America	μPB74LS27	
	Raytheon	74LS27	
	Signetics	74LS27	
	TI	SN74LS27	
74LS273	AMD	SN74LS273	
	ITT	ITT74LS273	
	Signetics	74LS273	
	TI	SN74LS273	
74LS279	ITT	ITT74LS279	
	Motorola	SN74LS279	
	National	DM74LS279	
	NEC America	μPB74LS279	
	Raytheon	74LS279	
	Signetics	74LS279	
	TI	SN74LS279	
74LS28	ITT	ITT74LS28	
	Raytheon	74LS28	
	Signetics	74LS28	
74LS28	TI	SN74LS28	
74LS280	TI	SN74LS280	
74LS283	ITT	ITT74LS283	
	Motorola	SN74LS283	
	National	DM74LS283	
	Raytheon	74LS283	
	Signetics	74LS283	
	TI	SN74LS283	
74LS290	ITT	ITT74LS290	
	Motorola	SN74LS290	
	National	DM74LS290	
	Signetics	74LS290	
	TI	SN74LS290	
74LS293	ITT	ITT74LS293	
	Motorola	SN74LS293	
	National	DM74LS293	
	Signetics	74LS293	
	TI	SN74LS293	
74LS295	Motorola	SN74LS295	
	NEC America	μPB74LS295	
	Raytheon	74LS295A	
	Signetics	74LS295	
	TI	SN74LS295B	
74LS298	Motorola	SN74LS298	
	Raytheon	74LS298	
	Signetics	74LS298	
	TI	SN74LS298	
74LS299	AMD	SN74LS299	
	ITT	ITT74LS299	
	Raytheon	74LS299	
	TI	SN74LS299	
74LS30	ITT	ITT74LS30	
	Motorola	SN74LS30	
	National	DM74LS30	
	NEC America	μPB74LS30	
	Raytheon	74LS30	
	Signetics	74LS30	
	TI	SN74LS30	
74LS32	ITT	ITT74LS32	
	Motorola	SN74LS32	
	National	DM74LS32	
	NEC America	μPB74LS32	
	Raytheon	74LS32	
	Signetics	74LS32	
	TI	SN74LS32	
74LS352	National	DM74LS352	
	TI	SN74LS352	
74LS353	National	DM74LS353	
	TI	SN74LS353	
74LS365	ITT	ITT74LS365	
	Motorola	SN74LS365	
	National	DM74LS365	
	NEC America	μPB74LS365	
	Raytheon	**74LS365**	**286**
	Signetics	74LS365	
	TI	SN74LS365	
74LS366	ITT	ITT74LS366	
	Motorola	SN74LS366	
	National	DM74LS366	
	NEC America	μPB74LS366	
	Raytheon	**74LS366**	**286**
	Signetics	74LS366	
	TI	SN74LS366	
74LS367	ITT	ITT74LS367	
	Motorola	SN74LS367	
	National	DM74LS367	
	NEC America	μPB74LS367	
	Raytheon	**74LS367**	**286**
	Signetics	74LS367	
	TI	SN74LS367	
74LS368	ITT	ITT74LS368	
	Motorola	SN74LS368	
	National	DM74LS368	
	NEC America	μPB74LS368	
	Raytheon	**74LS368**	**286**
	Signetics	74LS368	
	TI	SN74LS368	
74LS37	ITT	ITT74LS37	
	Motorola	SN74LS37	
	National	DM74LS37	
	NEC America	μPB74LS37	
	Raytheon	74LS37	
	Signetics	74LS37	
	TI	SN74LS37	
74LS373	AMD	SN74LS373	
	ITT	ITT74LS373	
74LS373	MMI	74LS373	
	Raytheon	**74LS373**	**288**
	Signetics	74LS373	
	TI	SN74LS373	
74LS374	AMD	SN74LS374	
	ITT	ITT74LS374	
	MMI	74LS374	
	Raytheon	**74LS374**	**288**
	TI	SN74LS374	
74LS377	AMD	SN74LS377	
	ITT	ITT74LS377	
	Raytheon	**74LS377**	**288**
	Signetics	74LS377	
	TI	SN74LS377	
74LS378	AMD	SN74LS378	
	ITT	ITT74LS378	
	Signetics	74LS378	
	TI	SN74LS378	
74LS38	ITT	ITT74LS38	
	Motorola	SN74LS38	
	National	DM74LS38	
	NEC America	μPB74LS38	
	Raytheon	74LS38	
	Signetics	74LS38	
	TI	SN74LS38	
74LS386	ITT	ITT74LS386	
	Motorola	SN74LS386	
	National	DM74LS386	
	Raytheon	74LS386	
	Signetics	74LS386	
	TI	SN74LS386	
74LS390	TI	SN74LS390	
74LS393	TI	SN74LS393	
74LS395	National	DM74LS395	
	Raytheon	**74LS395**	**291**
	Signetics	74LS395	
	TI	SN74LS395	
74LS40	ITT	ITT74LS40	
	Motorola	SN74LS40	
	National	DM74LS40	
	NEC America	μPB74LS40	
	Raytheon	74LS40	
	Signetics	74LS40	
	TI	SN74LS40	
74LS42	ITT	ITT74LS42	
	Motorola	SN74LS42	
	National	DM74LS42	
	NEC America	μPB74LS42	
	Raytheon	**74LS42**	**266**
	Signetics	74LS42	
	TI	SN74LS42	
74LS490	TI	SN74LS490	
74LS51	ITT	ITT74LS51	
	Motorola	SN74LS51	
	National	DM74LS51	
	NEC America	μPB74LS51	
	Raytheon	74LS51	
	Signetics	74LS51	
	TI	SN74LS51	
74LS54	ITT	ITT74LS54	
	Motorola	SN74LS54	
	National	DM74LS54	
	NEC America	μPB74LS54	
	Raytheon	74LS54	
	Signetics	74LS54	
	TI	SN74LS54	
74LS55	Motorola	SN74LS55	
	National	DM74LS55	
	NEC America	μPB74LS55	
	Raytheon	74LS55	
	Signetics	74LS55	
	TI	SN74LS55	
74LS670	AMD	SN74LS670	
	Motorola	SN74LS670	
	National	DM74LS670	
	Raytheon	74LS670	
	Signetics	74LS670	
	TI	SN74LS670	
74LS73	ITT	ITT74LS73	
	Motorola	SN74LS73	
	National	DM74LS73	
	Raytheon	74LS73	
	Signetics	74LS73	
	TI	SN74LS73	
74LS74	ITT	ITT74LS74	
	Motorola	SN74LS74	
74LS74	National	DM74LS74	
	NEC America	μPB74LS74	
	Raytheon	74LS74	
	Signetics	74LS74	
	TI	SN74LS74	
74LS75	ITT	ITT74LS75	
	National	DM74LS75	
	Raytheon	74LS75	
	Signetics	74LS75	
	TI	SN74LS75	
74LS77	National	DM74LS77	
	Raytheon	54LS77	
74LS83	ITT	ITT74LS83A	
	Motorola	SN74LS83	
	National	DM74LS83	
		DM74LS83A	
	Raytheon	74LS83A	
	Signetics	74LS83	
	TI	SN74LS83A	
74LS85	ITT	ITT74LS85	
	Motorola	SN74LS85	
	National	DM74LS85	
	Raytheon	74LS85	
	Signetics	74LS85	
	TI	SN74LS85	
74LS86	ITT	ITT74LS86	
	Motorola	SN74LS86	
	NEC America	μPB74LS86	
	Raytheon	74LS86	
	Signetics	74LS86	
	TI	SN74LS86	
74LS90	ITT	ITT74LS90	
	Motorola	SN74LS90	
	Raytheon	**74LS90**	**268**
	Signetics	74LS90	
	TI	SN74LS90	
74LS92	Motorola	SN74LS92	
	Raytheon	**74LS92**	**268**
	Signetics	74LS92	
	TI	SN74LS92	
74LS93	ITT	ITT74LS93	
	Motorola	SN74LS93	
	Raytheon	**74LS93**	**268**
	Signetics	74LS93	
	TI	SN74LS93	
74LS95	ITT	ITT74LS95B	
	Motorola	SN74LS95	
	Raytheon	74LS95B	
	Signetics	74LS95B	
	TI	SN74LS95B	
74S00	Hitachi	HD74S00	
	Mitsubishi	M5S000	
	National	DM74S00	
	Signetics	74S00	
	TI	SN74S00	
74S02	National	DM74S02	
	Signetics	74S02	
	TI	SN74S32	
74S03	Hitachi	HD74S03	
	Mitsubishi	M5S003	
	National	DM74S03	
	Signetics	74S03	
	TI	SN74S03	
74S04	Hitachi	HD74S04	
	Mitsubishi	M5S004	
	National	DM74S04	
	Signetics	74S04	
	TI	SN74S04	
74S05	Hitachi	HD74S05	
	Mitsubishi	M5S005	
	National	DM74S05	
	Signetics	74S05	
	TI	SN74S05	
74S08	Signetics	74S08	
	TI	SN74S08	
74S09	Signetics	74S09	
	TI	SN74S09	
74S10	Hitachi	HD74S10	
	Mitsubishi	M5S010	
	National	DM74S10	
	Signetics	74S10	
	TI	SN74S10	
74S11	Hitachi	HD74S11	
	Mitsubishi	M5S011	
	National	DM74S11	
	Signetics	74S11	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
74S11	TI	SN74S11	
74S112	Hitachi	HD74S112	
	Mitsubishi	M5S112	
	Motorola	SN74S112	
	National	DM74S112	
	Signetics	74S112	
	TI	SN74S112	
74S113	Hitachi	HD74S113	
	Mitsubishi	M5S113	
	Motorola	SN74S113	
	National	DM74S113	
	Signetics	74S113	
	TI	SN74S113	
74S114	Hitachi	HD74S114	
	Mitsubishi	M5S114	
	National	DM74S114	
	Signetics	74S114	
	TI	SN74S114	
74S132	TI	SN74S132	
74S133	Hitachi	HD74S133	
	Mitsubishi	M5S133	
	National	DM74S133	
	Signetics	74S133	
	TI	SN74S133	
74S134	Hitachi	HD74S134	
	National	DM74S134	
	Signetics	74S134	
	TI	SN74S134	
74S135	Hitachi	HD74S135	
	National	DM74S135	
	Signetics	74S135	
	TI	SN74S135	
74S138	AMD	SN74S138	
	Mitsubishi	M5S138	
	National	DM74S138	
	Signetics	74S138	
	TI	SN74S138	
74S139	AMD	SN74S139	
	National	DM74S139	
	Signetics	74S139	
	TI	SN74S139	
74S140	Hitachi	HD74S140	
	National	DM74S140	
	Signetics	74S140	
	TI	SN74S140	
74S15	Hitachi	HD74S15	
	Mitsubishi	M5S015	
	National	DM74S15	
	Signetics	74S15	
	TI	SN74S15	
74S151	AMD	SN74S151	
	Hitachi	HD74S151	
	Mitsubishi	M5S151	
	National	DM74S151	
	Signetics	74S151	
	TI	SN74S151	
74S153	AMD	SN74S153	
	Mitsubishi	M5S153	
	National	DM74S153	
	Signetics	74S153	
	TI	SN74S153	
74S157	AMD	SN74S157	
	Mitsubishi	M5S157	
	National	DM74S157	
	Signetics	74S157	
	TI	SN74S157	
74S158	AMD	SN74S158	
	Mitsubishi	M5S158	
	National	DM74S158	
	Signetics	74S158	
	TI	SN74S158	
74S174	AMD	SN74S174	
	Hitachi	HD74S174	
	Mitsubishi	M5S174	
	National	DM74S174	
	Signetics	74S174	
	TI	SN74S174	
74S175	AMD	SN74S175	
	Hitachi	HD74S175	
	Mitsubishi	M5S175	
	National	DM74S175	
	Signetics	74S175	
	TI	SN74S175	
74S181	AMD	SN74S181	
	Hitachi	HD74S181	
	Mitsubishi	M5S181	
	Signetics	74S181	
	TI	SN74S181	
74S182	Mitsubishi	M5S182	
	National	DM74S182	
	Signetics	74S182	
	TI	SN74S182	
74S194	AMD	SN74S194	
	Signetics	74S194	
	TI	SN74S194	
74S195	AMD	SN74S195	
	National	DM74S195	
	Signetics	74S195	
	TI	SN74S195	
74S20	Hitachi	HD74S20	
	Mitsubishi	M5S020	
	National	DM74S20	
	Signetics	74S20	
	TI	SN74S20	
74S22	Hitachi	HD74S22	
	Mitsubishi	M5S22	
	National	DM74S22	
	Signetics	74S22	
	TI	SN74S22	
74S251	AMD	SN74S251	
	Hitachi	HD74S251	
	Mitsubishi	M5S251	
	National	DM74S251	
	Signetics	74S251	
	TI	SN74S251	
74S253	AMD	SN74S253	
	National	DM74S253	
	Signetics	74S253	
74S257	AMD	SN74S257	
	Mitsubishi	M5S257	
	National	DM74S257	
	Signetics	74S257	
	TI	SN74S257	
74S258	AMD	SN74S258	
	Mitsubishi	M5S258	
	Signetics	74S258	
	TI	SN74S258	
74S30	Mitsubishi	M5S030	
	National	DM74S30	
	TI	SN74S30	
74S32	Signetics	74S32	
74S40	Hitachi	HD74S40	
	Mitsubishi	M5S040	
	National	DM74S40	
	Signetics	74S40	
	TI	SN74S40	
74S51	Mitsubishi	M5S051	
	National	DM74S51	
	Signetics	74S51	
	TI	SN74S51	
74S64	Hitachi	HD74S64	
	National	DM74S64	
	Signetics	74S64	
	TI	SN74S64	
74S65	Hitachi	HD74S65	
	National	DM74S65	
	Signetics	74S65	
	TI	SN74S65	
74S74	Hitachi	HD74S74	
	Mitsubishi	M5S074	
	TI	SN74S74	
74S86	Hitachi	HD74S86	
	National	DM74S86	
	Signetics	74S86	
	TI	SN74S86	
7400	Hitachi	HD2503	
		HD7400	
	ITT	ITT7400	
	Mitsubishi	M53200	
	Motorola	MC7400	
	National	DM7400	
	NEC America	μPB7400	
	Raytheon	7400	
	Signetics	7400	
	TI	SN7400	
	Toshiba	TC7400	
	TRW	7400	
7401	Hitachi	HD2509	
	ITT	ITT7401	
7401	Mitsubishi	M53201	
	Motorola	MC7401	
	National	DM7401	
	Raytheon	7401	
	Signetics	7401	
	TI	SN7401	
	TRW	7401	
7402	Hitachi	HD2511	
		HD7402	
	ITT	ITT7402	
	Mitsubishi	M53202	
	Motorola	MC7402	
	National	DM7402	
	NEC America	μPB7402	
	Signetics	7402	
	TI	SN7402	
	TRW	7402	
7403	Hitachi	HD2528	
		HD7403	
	ITT	ITT7403	
	Mitsubishi	M53203	
	Motorola	MC7403	
	National	DM7403	
	Raytheon	7403	
	Signetics	7403	
	TI	SN7403	
	TRW	7403	
7404	Hitachi	HD2522	
		HD7404	
	ITT	ITT7404	
	Mitsubishi	M53204	
	Motorola	MC7404	
	National	DM7404	
	NEC America	μPB7404	
	Raytheon	7404	
	Signetics	7404	
	TI	SN7404	
	Toshiba	TC7404	
	TRW	7404	
7405	Hitachi	HD2523	
		HD7405	
	ITT	ITT7405	
	Mitsubishi	M53205	
	Motorola	MC7405	
	National	DM7405	
	NEC America	μPB7405	
	Raytheon	7405	
	Signetics	7405	
	TI	SN7405	
	TRW	7405	
7406	Hitachi	HD7406	
	ITT	ITT7406	
	Mitsubishi	M53206	
	Motorola	MC7406	
	National	DM7406	
	Signetics	7406	
	TI	SN7406	
	TRW	7406	
7407	Hitachi	HD7407	
	ITT	ITT7407	
	Mitsubishi	M53207	
	Motorola	MC7407	
	National	DM7407	
	Signetics	7407	
	TI	SN7407	
	TRW	7407	
7408	Hitachi	HD2550	
	ITT	ITT7408	
	Mitsubishi	M53208	
	Motorola	MC7408	
	National	DM7408	
	Raytheon	7408	
	Signetics	7408	
	TI	SN7408	
	Toshiba	TC7408	
	TRW	7408	
7409	Hitachi	HD7409	
	ITT	ITT7409	
	Mitsubishi	M53209	
	Motorola	MC7409	
	National	DM7409	
	Raytheon	7409	
	Signetics	7409	
	TI	SN7409	
	TRW	7409	
7410	Hitachi	HD7410	
	ITT	ITT7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
	National	DM7410	
	NEC America	μPB7410	
	Raytheon	7410	
	Signetics	7410	
	TI	SN7410	
		SN7427	
	Toshiba	TC7410	
	TRW	7410	
74105	NEC America	μPB74105	
74107	AMD	SN74107	
	Hitachi	HD2530	
		HD74107	
	ITT	ITT74107	
	Mitsubishi	M53307	
	Motorola	MC74H107	
		MC74107	
	National	DM74107	
	NEC America	μPB74107	
	Signetics	74107	
	TI	SN74107	
74109	National	DM74109	
	Signetics	74109	
	TI	SN74109	
7411	Hitachi	HD7411	
	ITT	ITT7411	
	National	DM7411	
	Raytheon	7411	
	Signetics	7411	
74116	Signetics	74116	
	TI	SN74116	
7412	Hitachi	HD7412	
	ITT	ITT7412	
	Raytheon	7412	
	Signetics	7412	
	TI	SN7412	
	TRW	7412	
74121	Hitachi	HD74121	
	ITT	ITT74121	
	Mitsubishi	M53321	
	Motorola	MC74121	
		MC8603	
	National	DM74121	
	Signetics	74121	
	TI	SN74121	
	TRW	74121	
74122	ITT	ITT74122	
	Mitsubishi	M53322	
	Motorola	MC74122	
	Signetics	74122	
	TI	SN74122	
74123	AMD	SN74123	
	ITT	ITT74123	
	Mitsubishi	M53323	
	Motorola	MC74123	
	National	DM74123	
	NEC America	μPB74123	
	Raytheon	74123	
	Signetics	74123	
	TI	SN74123	
	TRW	74123	
74125	Hitachi	HD74125	
	Mitsubishi	M53325	
	National	DM74125	
	Signetics	74125	
	TI	SN74125	
74126	Hitachi	HD74126	
	Mitsubishi	M53326	
	National	DM74126	
	Signetics	74126	
	TI	SN74126	
7413	ITT	ITT7413	
	Mitsubishi	M53213	
	Motorola	MC7413	
	National	DM7413	
	NEC America	μPB7413	
	Signetics	7413	
	TI	SN7413	
	TRW	7413	
74132	Hitachi	HD74132	
	Mitsubishi	M53332	
	Motorola	MC74132	
	National	DM74132	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
74132	Signetics	74132	
	TI	SN74132	
74136	Raytheon	74136	
	TI	SN74136	
7414	Hitachi	HD7414	
	Mitsubishi	M53214	
	Motorola	MC7414	
	National	DM7414	
	Signetics	7414	
	TI	SN7414	
74141	Motorola	MC74141	
	National	DM74141	
	NEC America	μPB74141	
	Signetics	74141	
	TI	SN74141	
74145	ITT	ITT74145	
	Mitsubishi	M53345	
	Motorola	MC74145	
		MC83145	
	National	DM74145	
	Raytheon	74145	
	Signetics	74145	
	TI	SN74145	
	TRW	74145	
7415	Raytheon	7415	
74150	Hitachi	HD74150	
	Mitsubishi	M53350	
	Motorola	MC74150	
		MC83150	
	National	DM74150	
	NEC America	μPB74150	
	Raytheon	74150	
	Signetics	74150	
	TI	SN74150	
	TRW	74150	
74151	Hitachi	HD74151	
	ITT	ITT74151	
	~~Mitsubishi~~	~~M53351~~	
	Motorola	MC74151	
		MC83151	
	National	DM74151	
	NEC America	μPB74151	
	Raytheon	74151	
	Signetics	74151	
	TI	SN74151	
		SN74151A	
	TRW	74151	
74152	Motorola	MC74152	
		MC83152	
	Raytheon	74152	
	TI	SN74152	
	TRW	74152	
74153	AMD	SN74153	
	ITT	ITT74153	
	Mitsubishi	M53353	
	Motorola	MC74153	
		MC83153	
	National	DM74153	
	NEC America	μPB74153	
	Raytheon	74153	
	Signetics	74153	
	TI	SN74153	
	TRW	74153	
74154	AMD	SN74154	
	Mitsubishi	M53354	
	Motorola	MC74154	
		MC8311	
	National	DM74154	
	NEC America	μPB74154	
	Raytheon	74154	
	Signetics	74154	
	TI	SN74154	
	TRW	74154	
74155	ITT	ITT74155	
	Mitsubishi	M53355	
	Motorola	MC74155	
	National	DM74155	
	NEC America	μPB74155	
	Raytheon	74155	
	Signetics	74155	
	TI	SN74155	
	TRW	74155	
74156	Hitachi	HD74156	
74156	ITT	ITT74156	
	Mitsubishi	M53356	
	Motorola	MC74156	
	National	DM74156	
	NEC America	μPB74156	
	Raytheon	74156	
	Signetics	74156	
	TI	SN74156	
	TRW	74156	
74157	AMD	SN74157	
	Hitachi	HD74157	
	ITT	ITT74157	
	Mitsubishi	M53357	
	Motorola	MC74157	
		MC8322	
	National	DM74157	
	NEC America	μPB74157	
	Raytheon	74157	
	Signetics	74157	
	TI	SN74157	
74158	Raytheon	74158	
74159	Raytheon	74159	
	TI	SN74159	
7416	Hitachi	HD7416	
	ITT	ITT7416	
	Mitsubishi	M53216	
	Motorola	MC7416	
	National	DM7416	
	Signetics	7416	
	TI	SN7416	
	TRW	7416	
74160	AMD	SN74160	
	Hitachi	HD74160	
	ITT	ITT74160	
	Mitsubishi	M53360	
	Motorola	MC74160	
		MC8310	
		MC8316	
	National	DM74160	
	Raytheon	74160	
	~~Signetics~~	~~74160~~	
	TI	SN74160	
	TRW	74160	
74161	AMD	SN74161	
	Hitachi	HD74161	
	ITT	ITT74161	
	Mitsubishi	M53361	
	Motorola	MC74161	
	National	DM74161	
	NEC America	μPB74161	
	Raytheon	74161	
	Signetics	74161	
	TI	SN74161	
	TRW	74161	
74162	AMD	SN74162	
	Hitachi	HD74162	
	ITT	ITT74162	
	Mitsubishi	M53362	
	Motorola	MC74162	
	National	DM74162	
	Raytheon	74162	
	Signetics	74162	
	TI	SN74162	
	TRW	74162	
74163	AMD	SN74163	
	Hitachi	HD74163	
	ITT	ITT74163	
	Mitsubishi	M53363	
	Motorola	MC74163	
	National	DM74163	
	Raytheon	74163	
	Signetics	74163	
	TI	SN74163	
	TRW	74163	
74164	AMD	SN74164	
		74164	
	Hitachi	HD74164	
	ITT	ITT74164	
	Mitsubishi	M53364	
	Motorola	MC83164	
	National	DM74164	
	NEC America	μPB74164	
	Raytheon	74164	
	Signetics	74164	
	TI	SN74164	
74165	Mitsubishi	M53365	
74165	Motorola	MC74165	
		MC83165	
	National	DM74165	
	Raytheon	74165	
	Signetics	74165	
	TI	SN74165	
74166	Hitachi	HD74166	
	Mitsubishi	M53366	
	National	DM74166	
	Raytheon	74166	
	Signetics	74166	
	TI	SN74166	
7417	Hitachi	HD7417	
	ITT	ITT7417	
	Mitsubishi	M53217	
	Motorola	MC7417	
	National	DM7417	
	Signetics	7417	
	TI	SN7417	
	TRW	7417	
74170	Mitsubishi	M53370	
	National	DM74170	
	NEC America	μPB74170	
	Raytheon	74170	
	Signetics	74170	
	TI	SN74170	
74173	National	DM74173	
	TI	SN74173	
74174	AMD	SN74174	
	Hitachi	HD74174	
	Mitsubishi	M53374	
	Motorola	MC74174	
	National	DM74174	
	Raytheon	74174	
	Signetics	74174	
	TI	SN74174	
74175	AMD	SN74175	
	Hitachi	HD74175	
	Mitsubishi	M53375	
	Motorola	MC74175	
	~~National~~	~~DM74175~~	
	NEC America	μPB74175	
	Raytheon	74175	
	Signetics	74175	
	TI	SN74175	
74176	Mitsubishi	M53376	
	Motorola	MC74176	
		MC83176	
	National	DM74176	
	Signetics	74176	
	TI	SN74176	
74177	Mitsubishi	M53377	
	Motorola	MC74177	
		MC83177	
	National	DM74177	
	Signetics	74177	
	TI	SN74177	
74178	Motorola	MC83178	
	TI	SN74178	
74179	Motorola	MC83179	
	TI	SN74179	
74180	Hitachi	HD74180	
	ITT	ITT74180	
	Mitsubishi	M53380	
	Motorola	MC74180	
		MC83180	
	National	DM74180	
	NEC America	μPB74180	
	Raytheon	74180	
	Signetics	74180	
	TI	SN74180	
	TRW	74180	
74181	AMD	SN74181	
	Mitsubishi	M53381	
	Motorola	MC74181	
		MC8341	
	National	DM74181	
	NEC America	μPB74181	
	Raytheon	74181	
	Signetics	74181	
	TI	SN74181	
74182	AMD	SN74182	
	ITT	ITT74182	
	Mitsubishi	M53382	
	Motorola	MC74182	
		MC8342	
74182	National	DM74182	
	NEC America	μPB74182	
	Raytheon	74182	
	Signetics	74182	
	TI	SN74182	
74190	Hitachi	HD74190	
	ITT	ITT74190	
	Mitsubishi	M53390	
	Motorola	MC74190	
	National	DM74190	
	Raytheon	74190	
	Signetics	74190	
	TI	SN74190	
74191	Hitachi	HD74191	
	ITT	ITT74191	
	Mitsubishi	M53391	
	Motorola	MC74191	
	National	DM74191	
	Raytheon	74191	
	Signetics	74191	
	TI	SN74191	
74192	AMD	SN74192	
	ITT	ITT74192	
	Mitsubishi	M53392	
	Motorola	MC74192	
		MC8360	
	National	DM74192	
	NEC America	μPB74192	
	Raytheon	74192	
	Signetics	74192	
	TI	SN74192	
74193	AMD	SN74193	
	ITT	ITT74193	
	Mitsubishi	M53393	
	Motorola	MC74193	
		MC8366	
	National	DM74193	
	NEC America	μPB74193	
	Raytheon	74193	
	Signetics	74193	
	~~TI~~	~~SN74193~~	
74194	AMD	SN74194	
	Hitachi	HD74194	
	ITT	ITT74194	
	Motorola	MC74194	
	National	DM74194	
	Raytheon	74194	
	Signetics	74194	
	TI	SN74194	
74195	AMD	SN74195	
	ITT	ITT74195	
	Motorola	MC74195	
	National	DM74195	
	NEC America	μPB74195	
	Raytheon	74195	
	Signetics	74195	
		7447	
	TI	SN74195	
		SN74447A	
74196	Motorola	MC74196	
	National	DM74196	
	Signetics	74196	
	TI	SN74196	
74197	Motorola	MC74197	
	National	DM74197	
	Signetics	74197	
	TI	SN74197	
74198	Hitachi	HD74198	
	Mitsubishi	M53398	
	National	DM74198	
	NEC America	μPB74198	
	Raytheon	74198	
	Signetics	74198	
	TI	SN74198	
74199	Mitsubishi	M53399	
	National	DM74199	
	Raytheon	74199	
	Signetics	74199	
	TI	SN74199	
7420	Hitachi	HD2504	
		HD7420	
	ITT	ITT7420	
	Mitsubishi	M53220	
	Motorola	MC7420	
	National	DM7420	
	NEC America	μPB7420	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Fairchild (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
7420	Raytheon	7420	
	Signetics	7420	
	TI	SN7420	
	Toshiba	TC7420	
	TRW	7420	
7421	ITT	ITT7421	
	Raytheon	7421	
	Signetics	7421	
7422	Hitachi	HD7422	
	Raytheon	7422	
	TI	SN7422	
7423	Motorola	MC7423	
	National	DM7423	
	TI	SN7423	
7425	ITT	ITT7425	
	Mitsubishi	M53225	
	Motorola	MC7425	
	National	DM7425	
	TI	SN7425	
7426	Hitachi	HD7426	
	ITT	ITT7426	
	Motorola	MC7426	
	National	DM7426	
	Signetics	7426	
	TI	SN7426	
	TRW	7426	
7427	Hitachi	HD7427	
	Mitsubishi	M53227	
	Motorola	MC7427	
	National	DM7427	
	Signetics	7427	
	TI	SN7427	
74279	Signetics	74279	
	TI	SN74279	
74283	Mitsubishi	M53483	
	NEC America	μPB74283	
	Raytheon	74283	
	TI	SN74283	
74290	Mitsubishi	M53490	
	Motorola	MC74290	
	TI	SN74290	
	TRW	74290	
74293	Mitsubishi	M53493	
	Motorola	MC74293	
	TI	SN74293	
	TRW	74293	
74298	Motorola	MC74298	
	Signetics	74298	
	TI	SN74298	
7430	Hitachi	HD2508	
		HD7430	
	ITT	ITT7430	
	Mitsubishi	M53230	
	Motorola	MC7430	
	National	DM7430	
	NEC America	μPB7430	
	Signetics	7430	
	TI	SN7430	
	TRW	7430	
7432	Hitachi	HD7432	
	ITT	ITT7432	
	National	DM7432	
	Signetics	7432	
	TI	SN7432	
7437	ITT	ITT7437	
	Mitsubishi	M53237	
	Motorola	MC7437	
	National	DM7437	
	NEC America	μPB7437	
	Raytheon	7437	
	Signetics	7437	
	TI	SN7437	
	TRW	7437	
7438	ITT	ITT7438	
	Mitsubishi	M53238	
	Motorola	MC7438	
	National	DM7438	
	NEC America	μPB7438	
	Raytheon	7438	
	Signetics	7438	
	TI	SN7438	
	TRW	7438	
7439	Signetics	7439	
7440	Hitachi	HD2501	
		HD7440	
	ITT	ITT7440	
	Mitsubishi	M53240	
	Motorola	MC7440	
	National	DM7440	
	NEC America	μPB7440	
	Signetics	7440	
	TI	SN7440	
	TRW	7440	
7441	Mitsubishi	M53241	
	Motorola	MC8315	
	National	DM7441	
	Signetics	7441	
	TI	SN74141	
7442	Hitachi	HD7442	
	ITT	ITT7442	
	Mitsubishi	M53242	
	Motorola	MC7442	
		MC8352	
	National	DM7442	
	NEC America	μPB7442	
	Raytheon	7442	
	Signetics	7442	
	TI	SN7442	
		SN7442A	
7443	Hitachi	HD7443	
	ITT	ITT7443	
	Mitsubishi	M53243	
	Motorola	MC7443	
		MC8353	
	Raytheon	7443	
	Signetics	7443	
	TI	SN7443	
		SN7443A	
7444	Hitachi	HD7444	
	ITT	ITT7444	
	Mitsubishi	M53244	
	Motorola	MC7444	
		MC8354	
	Raytheon	7444	
	Signetics	7444	
	TI	SN7444A	
7445	ITT	ITT7445	
	Mitsubishi	M53245	
	Motorola	MC7445	
		MC8345	
	National	DM7445	
	NEC America	μPB7445	
	Raytheon	7445	
	Signetics	7445	
	TI	SN7445	
	TRW	7445	
7446	ITT	ITT7446	
	Motorola	MC7446	
		MC8357	
	National	DM7446	
	Signetics	7446	
	TI	SN7446A	
7447	ITT	ITT7447	
	Mitsubishi	M53247	
	Motorola	MC7447	
		MC8357	
	National	DM7447	
	NEC America	μPB7447	
	Signetics	7447	
	TI	SN7447	
7448	ITT	ITT7448	
	Mitsubishi	M53248	
	Motorola	MC7448	
		MC8358	
	National	DM7448	
	Signetics	7448	
	TI	SN7448	
7449	Motorola	MC7449	
		MC8359	
	TI	SN7449	
7450	Hitachi	HD2506	
		HD7450	
	ITT	ITT7450	
	Mitsubishi	M53250	
	Motorola	MC7450	
	National	DM7450	
	NEC America	μPB7450	
	Signetics	7450	
	TI	SN7450	
7450	TRW	7450	
7451	Hitachi	HD2505	
		HD7451	
	ITT	ITT7451	
	Motorola	MC7451	
	National	DM7451	
	NEC America	μPB7451	
	Signetics	7451	
	TI	SN7451	
	TRW	7451	
7453	Hitachi	HD2512	
		HD7453	
	ITT	ITT7453	
	Mitsubishi	M53253	
	Motorola	MC7453	
	National	DM7453	
	NEC America	μPB7453	
	Signetics	7453	
	TI	SN7453	
	TRW	7453	
7454	Hitachi	HD2514	
		HD7454	
	ITT	ITT7454	
	Motorola	MC7454	
	National	DM7454	
	NEC America	μPB7454	
	Signetics	7454	
	TI	SN7454	
	TRW	7454	
7460	Hitachi	HD2502	
		HD7460	
	Mitsubishi	M53260	
	Motorola	MC7460	
	National	DM7460	
	NEC America	μPB7460	
	Signetics	7460	
	TI	SN7460	
	TRW	7460	
7470	Hitachi	HD2539	
	ITT	ITT7470	
	Mitsubishi	M53270	
	Motorola	MC7470	
	National	DM7470	
	Signetics	7470	
	TI	SN7470	
7472	Hitachi	HD2529	
		HD7472	
	ITT	ITT7472	
	Mitsubishi	M53272	
	Motorola	MC7472	
	National	DM7472	
	Signetics	7472	
	TI	SN7472	
	TRW	7472	
7473	Hitachi	HD2515	
	ITT	ITT7473	
	Mitsubishi	M53273	
	Motorola	MC7473	
	National	DM7473	
	NEC America	μPB7473	
	Signetics	7473	
	TI	SN7473	
7474	Hitachi	HD2510	
		HD7474	
	ITT	ITT7474	
	Mitsubishi	M53274	
	Motorola	MC7474	
	National	DM7474	
	NEC America	μPB7474	
	Raytheon	7474	
	Signetics	7474	
	TI	SN7474	
	TRW	7474	
7475	Hitachi	HD7475	
	ITT	ITT7475	
	Mitsubishi	M53275	
	Motorola	MC7475	
		MC8375	
	National	DM7475	
	Signetics	7475	
	TI	SN7475	
	TRW	7475	
7476	Hitachi	HD2516	
	ITT	ITT7476	
	Mitsubishi	M53276	
	Motorola	MC7476	
7476	National	DM7476	
	NEC America	μPB7476	
	Signetics	7476	
	TI	SN7476	
	TRW	7476	
7477	Motorola	MC7477	
		MC8377	
	Signetics	7477	
7480	ITT	ITT7480	
	Mitsubishi	M53280	
	Motorola	MC7480	
	NEC America	μPB7480	
	Signetics	7480	
	TI	SN7480	
7481	Motorola	MC4004	
	TI	SN7481A	
7482	Hitachi	HD2513	
	ITT	ITT7482	
	Motorola	MC7482	
		MC8382	
	TI	SN7482	
7483	ITT	ITT7483	
	Mitsubishi	M53283	
	Motorola	MC7483	
		MC8383	
	National	DM7483	
	Raytheon	7483	
	Signetics	7483	
	TI	SN7483	
		SN7483A	
7485	Hitachi	HD7485	
	Mitsubishi	M53285	
	Motorola	MC7485	
	National	DM7485	
	NEC America	μPB7485	
	Signetics	7485	
	TI	SN7485	
	TRW	7485	
7486	Hitachi	HD2526	
		HD7486	
	ITT	ITT7486	
	Mitsubishi	M53286	
	Motorola	MC7486	
	National	DM7486	
	NEC America	μPB7486	
	Raytheon	7486	
	Signetics	7486	
	TI	SN7486	
	TRW	7486	
7488	Motorola	MC4002	
	TI	SN7488A	
7489	AMD	SN7489	
	Mitsubishi	M53289	
	Motorola	MC4064	
	National	**DM7489**	**1287**
	NEC Micro	μPB2089	
	TI	SN7489	
	TRW	7489	
7490	Hitachi	HD2519	
		HD7490	
	ITT	ITT7490	
	Mitsubishi	M53290	
	Motorola	MC7490	
		MC8390	
	National	DM7490	
	Signetics	7490	
	TI	SN7490A	
	TRW	7490	
7491	Hitachi	HD2524	
	ITT	ITT7491	
	Mitsubishi	M53291	
	Motorola	MC7491	
		MC8391	
	National	DM7491	
	NEC America	μPB7491	
	Signetics	7491	
	TI	SN7491A	
7492	Hitachi	HD2521	
		HD7492	
	ITT	ITT7492	
	Mitsubishi	M53292	
	Motorola	MC7492	
		MC8392	
	National	DM7492	
	Signetics	7492	
	TI	SN7492	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Fairchild (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
7492	TI	SN7492A	
	TRW	7492	
7493	Hitachi	HD2520	
		HD7493	
	ITT	ITT7493	
	Mitsubishi	M53293	
	Motorola	MC7493	
		MC8393	
	National	DM7493	
	Signetics	7493	
	TI	SN7493A	
	TRW	7493	
7494	Motorola	MC7494	
		MC8394	
	Signetics	7494	
	TI	SN7494	
7495	Hitachi	HD2534	
	ITT	ITT7495	
	Mitsubishi	M53295	
	Motorola	MC7495	
		MC8395	
	National	DM7495	
	Signetics	7495	
	TI	SN7495	
		SN7495A	
7496	Hitachi	HD7496	
	ITT	ITT7496	
	Mitsubishi	M53296	
	Motorola	MC7496	
		MC8396	
	National	DM7496	
	Signetics	7496	
	TI	SN7496	
	TRW	7496	
7497	Motorola	MC7497	
	TI	SN7497	
75107	ITT	ITT75107	
	Motorola	MC75107	
	National	**DS75107**	**504**
	Raytheon	RC75107	
	TI	SN75107	
75108	ITT	ITT75108	
	Motorola	MC75108	
	National	**DS75108**	**504**
	Raytheon	RC75108	
	TI	SN75108	
75109	ITT	ITT75109	
	Raytheon	RC75109	
	TI	SN75109	
75110	ITT	ITT75110	
	Motorola	MC75110	
	Raytheon	RC75110	
	TI	SN75110	
75112	TI	SN75112	
75121	Motorola	MC8T13	
	TI	SN75121	
75122	Motorola	MC8T14	
	TI	SN75122	
75123	Motorola	MC8T23	
	TI	SN75123	
75124	Motorola	MC8T24	
	TI	SN75124	
75150	TI	SN75150	
75154	TI	SN75154	
75207	TI	SN75207	
75208	TI	SN75208	
75232	TI	SN75232	
75233	TI	SN75232	
75234	ITT	ITT75234	
	TI	SN75234	
75235	TI	SN75234	
75238	TI	SN75238	
75239	TI	SN75238	
7524	ITT	ITT7524	
	Motorola	MC7524	
	National	DS7524	
	Signetics	7524	
	TI	SN7524	
7525	Motorola	MC7525	
	National	DS7525	
	Signetics	7525	
	TI	SN7524	
7528	Motorola	MC7528	
7528	TI	SN7528	
7529	Motorola	MC7529	
75325	Motorola	MC75325	
	National	**DS75325**	**520**
	Signetics	75325	
	TI	SN75325	
75326	TI	SN75326	
75327	TI	SN75327	
7534	Motorola	MC7534	
7535	Motorola	MC7535	
7538	Motorola	MC7538	
7539	Motorola	MC7539	
75430	TI	SN75430	
75431	TI	SN75431	
75432	TI	SN75432	
75433	TI	SN75433	
75434	TI	SN75434	
75450	ITT	ITT75450	
	Motorola	MC75450	
	National	DS75450	
	Signetics	75450	
	Silicon G	SG75450	
	TI	SN75450	
75451	ITT	ITT75451	
	Motorola	MC75451	
	National	DS75451	
	Signetics	75451	
	TI	SN75451	
75452	ITT	ITT75452	
	Motorola	MC75452	
	National	DS75452	
	Signetics	75452	
	TI	SN75452	
75453	ITT	ITT75453	
	Motorola	MC75453	
	National	DS75453	
	Signetics	75453	
	TI	SN75453	
75454	ITT	ITT75454	
	Motorola	MC75454	
	National	DS75454	
	Signetics	75454	
	TI	SN75454	
75460	ITT	ITT75460	
	National	DS75460	
	Silicon G	SG75460	
	TI	SN75460	
75461	ITT	ITT75461	
	Motorola	MC75461	
	National	DS75461	
	TI	SN75461	
75462	ITT	ITT75462	
	Motorola	MC75462	
	National	DS75462	
	TI	SN75462	
75463	Motorola	MC75463	
	National	DS75463	
	TI	SN75463	
75464	ITT	ITT75464	
	Motorola	MC75464	
	National	DS75464	
	TI	SN75464	
75470	TI	SN75470	
75471	TI	SN75471	
75472	TI	SN75472	
75473	TI	SN75473	
75474	TI	SN75474	
75491	Motorola	MC75491	
	National	DS75491	
	TI	SN75491	
75492	Motorola	MC75492	
	National	DS75492	
	TI	SN75492	
8T13	Motorola	MC8T13	
	National	DS55121	
	TI	SN55121	
8T14	Motorola	MC8T14	
	National	DS55122	
	TI	SN55122	
8T23	Motorola	MC8T23	
	National	DS75123	
	TI	SN75123	
8T24	Motorola	MC8T24	
	National	DS75124	
	TI	SN75124	
9H00	Motorola	MC54H00	
9H00	Motorola	MC74H00	
	National	DM54H00	
		DM74H00	
	Signetics	54H00	
		74H00	
	TI	SN54H00	
		SN74H00	
9H01	Motorola	MC54H01	
		MC74H01	
	National	DM54H01	
	TI	SN54H01	
		SN74H01	
9H04	Motorola	MC54H04	
		MC74H04	
	National	DM54H04	
		DM74H04	
	Signetics	54H04	
		74H04	
	TI	SN54H04	
		SN74H04	
9H05	Motorola	MC54H05	
		MC74H05	
	National	DM54H05	
		DM74H05	
	Signetics	54H05	
		74H05	
	TI	SN54H05	
		SN74H05	
9H08	Motorola	MC54H08	
		MC74H08	
	National	DM54H08	
		DM74H08	
	Signetics	54H08	
		74H08	
9H10	Motorola	MC54H10	
		MC74H10	
	National	DM54H10	
		DM74H10	
	Signetics	54H10	
		74H10	
	TI	SN54H10	
		SN74H10	
9H101	Motorola	MC54H101	
		MC74H101	
	Signetics	54H101	
		74H101	
	TI	SN54H101	
		SN74H101	
9H102	Motorola	MC54H102	
		MC74H102	
	Signetics	54H102	
		74H102	
	TI	SN54H102	
		SN74H102	
9H103	National	DM54H103	
		DM74H103	
	TI	SN54H103	
		SN74H103	
9H106	National	DM54H106	
		DM74H106	
	Signetics	54H106	
		74H106	
	TI	SN54H106	
		SN54H107	
		SN74H106	
		SN74H107	
9H108	Motorola	MC54H108	
		MC74H108	
	National	DM54H108	
		DM74H108	
	Signetics	54H108	
		74H108	
	TI	SN54H108	
		SN74H108	
9H11	Motorola	MC54H11	
		MC74H11	
	National	DM54H11	
		DM74H11	
	Signetics	54H11	
		74H11	
	TI	SN54H11	
		SN74H11	
9H20	Motorola	MC54H20	
		MC74H20	
	National	DM54H20	
		DM74H20	
9H20	Signetics	54H20	
		74H20	
	TI	SN54H20	
		SN74H20	
9H21	Motorola	MC54H21	
		MC74H21	
	National	DM54H21	
		DM74H21	
	TI	SN54H21	
		SN74H21	
9H22	Motorola	MC54H22	
		MC74H22	
	National	DM54H22	
		DM74H22	
	Signetics	54H22	
		74H22	
	TI	SN54H22	
		SN74H22	
9H30	Motorola	MC54H30	
		MC74H30	
	National	DM54H30	
		DM74H30	
	Signetics	54H30	
		74H30	
	TI	SN54H30	
		SN74H30	
9H40	Motorola	MC54H40	
		MC74H40	
	National	DM54H40	
		DM74H40	
	Signetics	54H40	
		74H40	
	TI	SN54H40	
		SN74H40	
9H50	Motorola	MC74H50	
	National	DM54H50	
		DM74H50	
	Signetics	54H50	
		74H50	
	TI	SN54H50	
		SN74H50	
9H51	Motorola	MC54H51	
		MC74H51	
	National	DM54H51	
		DM74H51	
	Signetics	54H51	
		74H51	
	TI	SN54H51	
		SN74H51	
9H52	Motorola	MC54H52	
		MC74H52	
	National	DM54H52	
		DM74H52	
	TI	SN54H52	
		SN74H52	
9H53	Motorola	MC54H53	
		MC74H53	
	National	DM54H53	
		DM74H53	
	TI	SN54H53	
		SN74H53	
9H54	Motorola	MC54H54	
		MC74H54	
	National	DM54H54	
		DM74H54	
	TI	SN54H54	
		SN74H54	
9H55	Motorola	MC54H55	
		MC74H55	
	National	DM54H55	
		DM74H55	
	TI	SN54H55	
		SN74H55	
9H60	Motorola	MC54H60	
		MC74H60	
	National	DM54H60	
		DM74H60	
	TI	SN54H60	
		SN74H60	
9H61	Motorola	MC54H61	
		MC74H61	
	National	DM54H61	
		DM74H61	
	Signetics	54H61	
		74H61	
	TI	SN54H61	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Fairchild (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
9H61	TI	SN74H61	
9H62	Motorola	MC54H62	
		MC74H62	
	National	DM54H62	
		DM74H62	
	Signetics	54H62	
		74H62	
	TI	SN54H62	
		SN74H62	
9H71	Motorola	MC54H71	
		MC74H71	
	National	DM54H71	
		DM74H71	
	Signetics	54H71	
		74H71	
	TI	SN54H71	
		SN74H71	
9H72	Motorola	MC54H72	
	National	DM54H72	
		DM74H72	
	Signetics	54H72	
		74H72	
	TI	SN54H72	
		SN74H72	
9H73	Motorola	MC54H73	
	National	DM54H73	
		DM74H73	
	Signetics	54H73	
		74H73	
	TI	SN54H73	
		SN74H73	
9H74	Motorola	MC54H74	
		MC74H74	
	National	DM54H74	
		DM74H74	
	Signetics	54H74	
		74H74	
	TI	SN54H74	
		SN74H74	
9H76	National	DM54H76	
		DM74H76	
	Signetics	54H76	
		74H76	
	TI	SN54H76	
		SN74H76	
9H78	National	DM54H78	
		DM74H78	
	TI	SN54H78	
		SN74H78	
9LS00	National	DM54LS00	
		DM74LS00	
	Raytheon	9LS00	
9LS02	National	DM54LS02	
		DM74LS02	
	Raytheon	9LS02	
9LS03	National	DM54LS03	
		DM74LS03	
	Raytheon	9LS03	
9LS04	National	DM54LS04	
		DM74LS04	
	Raytheon	9LS04	
9LS05	National	DM54LS05	
		DM74LS05	
	Raytheon	9LS05	
9LS08	National	DM54LS08	
		DM74LS08	
	Raytheon	9LS08	
9LS09	National	DM54LS09	
		DM74LS09	
	Raytheon	9LS09	
9LS10	National	DM54LS10	
		DM74LS10	
	Raytheon	9LS10	
9LS109	National	DM54LS109	
		DM74LS109	
	Raytheon	9LS109	
9LS11	National	DM54LS11	
		DM74LS11	
	Raytheon	9LS11	
9LS112	National	DM54LS112	
		DM74LS112	
	Raytheon	9LS112	
9LS113	National	DM54LS113	
9LS113	National	DM74LS113	
	Raytheon	9LS113	
9LS114	National	DM54LS114	
		DM74LS114	
	Raytheon	9LS114	
9LS125	National	DM54LS125	
		DM74LS125	
9LS126	National	DM54LS126	
		DM74LS126	
9LS132	National	DM54LS132	
		DM74LS132	
	Raytheon	**9LS132**	**264**
9LS133	National	DM74S133	
9LS136	National	DM54LS136	
		DM74LS136	
	Raytheon	9LS136	
9LS138	National	DM54LS138	
		DM74LS138	
	Raytheon	9LS138	
9LS139	National	DM54LS139	
		DM74LS139	
	Raytheon	9LS139	
9LS14	National	DM54LS14	
		DM74LS14	
	Raytheon	**9LS14**	**264**
9LS15	National	DM54LS15	
		DM74LS15	
	Raytheon	9LS15	
9LS151	National	DM54LS151	
		DM74LS151	
	Raytheon	9LS151	
9LS152	Raytheon	9LS152	
9LS153	National	DM54LS153	
		DM74LS153	
	Raytheon	9LS153	
9LS155	National	DM54LS155	
		DM74LS155	
	Raytheon	9LS155	
9LS156	National	DM54LS156	
		DM74LS156	
	Raytheon	9LS156	
9LS157	National	DM54LS157	
		DM74LS157	
	Raytheon	9LS157	
9LS158	National	DM54LS158	
		DM74LS158	
	Raytheon	9LS158	
9LS160	National	DM54LS160	
		DM74LS160	
	Raytheon	9LS160	
9LS161	National	DM54LS161	
		DM74LS161	
	Raytheon	9LS161	
9LS162	National	DM54LS162	
		DM74LS162	
	Raytheon	9LS162	
9LS163	National	DM54LS163	
		DM74LS163	
	Raytheon	9LS163	
9LS164	National	DM54LS164	
		DM74LS164	
9LS170	National	DM54LS170	
		DM74LS170	
	Raytheon	9LS170	
9LS173	Raytheon	9LS173	
9LS174	National	DM54LS174	
		DM74LS174	
	Raytheon	9LS174	
9LS175	National	DM54LS175	
		DM74LS175	
	Raytheon	9LS175	
9LS181	National	DM54181	
		DM74181	
	Raytheon	9LS181	
9LS190	National	DM54LS190	
		DM74LS190	
	Raytheon	9LS190	
9LS191	National	DM54LS191	
		DM74LS191	
	Raytheon	9LS191	
9LS192	National	DM54LS192	
		DM74LS192	
	Raytheon	9LS192	
9LS193	National	DM54LS193	
		DM74LS193	
	Raytheon	9LS193	
9LS194	Raytheon	9LS194A	
9LS195	Raytheon	9LS195A	
9LS196	National	DM54LS196	
		DM74LS196	
	Raytheon	9LS196	
9LS197	National	DM54LS197	
		DM74LS197	
	Raytheon	9LS197	
9LS20	National	DM54LS20	
		DM74LS20	
	Raytheon	9LS20	
9LS21	National	DM54LS21	
		DM74LS21	
	Raytheon	9LS21	
9LS22	National	DM54LS22	
		DM74LS22	
	Raytheon	9LS22	
9LS251	Raytheon	9LS251	
9LS253	National	DM54LS253	
		DM74LS253	
	Raytheon	9LS253	
9LS257	National	DM54LS257	
		DM74LS257	
	Raytheon	9LS257	
9LS258	National	DM54LS258	
		DM74LS258	
	Raytheon	9LS258	
9LS259	National	DM8334	
		DM9334	
9LS266	National	DM54LS266	
		DM74LS266	
	Raytheon	9LS266	
9LS27	National	DM54LS27	
		DM74LS27	
	Raytheon	9LS27	
9LS279	National	DM54LS279	
		DM74LS279	
	Raytheon	9LS279	
9LS283	National	DM54LS283	
		DM74LS283	
	Raytheon	9LS283	
9LS295	Raytheon	9LS295A	
9LS298	AMD	9LS298	
	Raytheon	9LS298	
9LS30	National	DM54LS30	
		DM74LS30	
	Raytheon	9LS30	
9LS32	National	DM54LS32	
		DM74LS32	
	Raytheon	9LS32	
9LS365	National	DM54LS365	
		DM74LS365	
9LS366	National	DM54LS366	
		DM74LS366	
9LS367	National	DM54LS367	
		DM74LS367	
9LS368	National	DM54LS368	
		DM74LS368	
9LS37	National	DM54LS37	
		DM74LS37	
	Raytheon	9LS37	
9LS38	National	DM54LS38	
		DM74LS38	
	Raytheon	9LS38	
9LS40	National	DM54LS40	
		DM74LS40	
	Raytheon	9LS40	
9LS42	National	DM54LS42	
		DM74LS42	
	Raytheon	**9LS42**	**266**
9LS51	National	DM54LS51	
		DM74LS51	
	Raytheon	9LS51	
9LS54	National	DM54LS54	
		DM74LS54	
	Raytheon	9LS54	
9LS55	National	DM54LS55	
		DM74LS55	
	Raytheon	9LS55	
9LS670	National	DM54LS670	
		DM74LS670	
	Raytheon	9LS670	
9LS73	National	DM54LS73	
		DM74LS73	
9LS74	National	DM54LS74	
		DM74LS74	
9LS74	Raytheon	9LS74	
9LS83	National	DM54LS83	
		DM74LS83	
	Raytheon	9LS83A	
9LS86	National	DM54LS86	
		DM74LS86	
	Raytheon	9LS86	
9LS90	**Raytheon**	**9LS90**	**268**
9LS93	**Raytheon**	**9LS93**	**268**
9LS95	Raytheon	9LS95B	
9L00	National	DM54L00	
		DM74L00	
	TI	SN54LS00	
		SN74LS00	
9L04	National	DM54L04	
		DM74L04	
	TI	SN54LS04	
		SN74LS04	
9L24	National	DM8024	
		DM9024	
	TI	SN54LS109	
		SN74LS109	
9L54	National	DM54L54	
		DM74L54	
	TI	SN54LS54	
		SN74LS54	
9L86	National	DM5486	
		DM7486	
	TI	SN54LS86	
		SN74LS86	
9N00	Motorola	MC5400	
		MC7400	
	National	DM5400	
		DM7400	
	Signetics	5400	
		7400	
	TI	SN5400	
		SN7400	
9N01	Motorola	MC5401	
		MC7401	
	National	DM5401	
		DM7401	
	Signetics	5401	
		7401	
	TI	SN5401	
		SN7401	
9N02	Motorola	MC7402	
	National	DM5402	
		DM7402	
	Signetics	5402	
		7402	
	TI	SN5402	
		SN7402	
9N03	Motorola	MC5403	
		MC7403	
	National	DM5403	
		DM7403	
	Signetics	5403	
		7403	
	TI	SN5403	
		SN7403	
9N04	Motorola	MC5404	
		MC7404	
	National	DM5404	
		DM7404	
	Signetics	5404	
		7404	
	TI	SN5404	
		SN7404	
9N05	Motorola	MC5405	
		MC7405	
	National	DM5405	
		DM7405	
	Signetics	5405	
		7405	
9N06	Motorola	MC5406	
		MC7406	
	National	DM5406	
		DM7406	
	Signetics	5406	
		7406	
	TI	SN5406	
		SN7406	
9N07	Motorola	MC5407	
		MC7407	
	National	DM5407	

◆ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Fairchild (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
9N07	National	DM7407	
	Signetics	5407	
		7407	
	TI	SN5407	
		SN7407	
9N08	Motorola	MC5408	
		MC7408	
	National	DM5408	
		DM7408	
	Signetics	5408	
		7408	
	TI	SN5408	
		SN7408	
9N09	Motorola	MC5409	
		MC7409	
	National	DM5409	
		DM7409	
	Signetics	7409	
	TI	SN5409	
		SN7409	
9N10	Motorola	MC5410	
		MC7410	
	National	DM5410	
		DM7410	
	Signetics	5410	
	TI	SN5410	
		SN7410	
9N107	Motorola	MC54107	
		MC74H107	
	National	DM54107	
		DM74107	
	Signetics	54107	
		74107	
	TI	SN54107	
		SN74107	
9N11	National	DM5411	
		DM7411	
	Signetics	5411	
		7411	
9N12	Motorola	MC5412	
	National	DM54LS12	
		DM74LS12	
	TI	SN5412	
		SN7412	
9N122	National	DM54LS122	
		DM74LS122	
		DM74122	
	TI	SN54122	
		SN74122	
9N123	National	DM54123	
		DM74123	
	TI	SN54123	
		SN74123	
9N13	National	DM5413	
		DM7413	
	TI	SN5413	
		SN7413	
9N132	National	DM54132	
		DM74132	
	TI	SN54132	
		SN74132	
9N14	National	DM5414	
		DM7414	
	TI	SN5414	
		SN7414	
9N16	Motorola	MC5416	
		MC7416	
	National	DM5416	
		DM7416	
	TI	SN5416	
		SN7416	
9N17	Motorola	MC7417	
		MC9417	
	National	DM5417	
		DM7417	
	TI	SN5417	
		SN7417	
9N20	Motorola	MC5420	
		MC7420	
	National	DM5420	
		DM7420	
	Signetics	5420	
		7420	
9N20	TI	SN5420	
		SN7420	
9N21	National	DM54LS21	
		DM74LS21	
9N23	Motorola	MC5423	
		MC7423	
	National	DM5423	
		DM7423	
	TI	SN5423	
		SN7423	
9N25	Motorola	MC5425	
		MC7425	
	National	DM5425	
		DM7425	
	TI	SN5425	
		SN7425	
9N26	Motorola	MC5426	
		MC7426	
	National	DM5426	
		DM7426	
	Signetics	5426	
	TI	SN5426	
		SN7426	
9N27	Motorola	MC5427	
		MC7427	
	National	DM5427	
		DM7427	
	TI	SN5427	
		SN7427	
9N279	National	DM54LS279	
		DM74LS279	
	TI	SN54279	
		SN74279	
9N30	Motorola	MC5430	
		MC7430	
	National	DM5430	
		DM7430	
	Signetics	5430	
		7430	
	TI	SN5430	
		SN7430	
9N32	National	DM5432	
		DM7432	
	TI	SN5432	
		SN7432	
9N37	Motorola	MC5437	
		MC7437	
	National	DM5437	
		DM7437	
	TI	SN5437	
		SN7437	
9N38	Motorola	MC5438	
		MC7438	
	National	DM5438	
		DM7438	
	TI	SN5438	
		SN7438	
9N39	National	DM5401	
		DM7401	
9N40	Motorola	MC5440	
		MC7440	
	National	DM5440	
		DM7440	
	Signetics	5440	
		7440	
	TI	SN5440	
		SN7440	
9N50	Motorola	MC5450	
		MC7450	
	National	DM5450	
		DM7450	
	Signetics	5450	
		7450	
	TI	SN5450	
		SN7450	
9N51	Motorola	MC5451	
		MC7451	
	National	DM5451	
		DM7451	
	Signetics	5451	
		7451	
	TI	SN5451	
		SN7451	
9N53	Motorola	MC5453	
		MC7453	
	National	DM5453	
9N53	National	DM7453	
	Signetics	5453	
		7453	
	TI	SN5453	
		SN7453	
9N54	Motorola	MC5454	
		MC7454	
	National	DM5454	
		DM7454	
	Signetics	5454	
		7454	
	TI	SN5454	
		SN7454	
9N60	Motorola	MC5460	
		MC7460	
	National	DM5460	
		DM7460	
	Signetics	5460	
		7460	
	TI	SN5460	
		SN7460	
9N70	Motorola	MC5470	
		MC7470	
	National	DM5470	
		DM7470	
	Signetics	5470	
		7470	
	TI	SN5470	
		SN7470	
9N72	Motorola	MC5472	
		MC7472	
	National	DM5472	
		DM7472	
	Signetics	5472	
		7472	
	TI	SN5472	
		SN7472	
9N73	Motorola	MC5473	
		MC7473	
	National	DM5473	
		DM7473	
	Signetics	5473	
		7473	
	TI	SN5473	
		SN7473	
9N74	Motorola	MC5474	
		MC7474	
	National	DM5474	
		DM7474	
	Raytheon	5474	
	Signetics	5474	
		7474	
	TI	SN5474	
		SN7474	
9N75	Motorola	MC8375	
	TI	SN5475	
		SN7475	
9N76	Motorola	MC5476	
		MC7476	
	National	DM5476	
		DM7476	
	Signetics	5476	
		7476	
	TI	SN5476	
		SN7476	
9N86	National	DM5486	
		DM7486	
	Raytheon	5486	
	Signetics	5486	
		7486	
	TI	SN5486	
		SN7486	
9S00	National	DM74S00	
	Signetics	74S00	
	TI	SN54S00	
		SN74S00	
9S02	National	DM74S02	
	TI	SN54S02	
		SN74S02	
9S03	National	DM74S03	
	Signetics	74S03	
	TI	SN54S03	
		SN74S03	
9S04	National	DM74S04	
	Signetics	74S04	
	TI	SN54S04	
9S04	TI	SN74S04	
9S05	National	DM74S05	
	Signetics	74S05	
	TI	SN54S05	
		SN74S05	
9S08	National	DM74LS08	
	TI	SN54S08	
		SN74S08	
9S09	National	DM74LS09	
	TI	SN54S09	
		SN74S09	
9S10	National	DM74S10	
	TI	SN54S10	
		SN74S10	
9S109	National	DM74LS109	
9S11	National	DM74S11	
	TI	SN54S11	
		SN74S11	
9S112	National	DM74S112	
	TI	SN54S112	
		SN74S112	
9S113	National	DM74S113	
	TI	SN54S113	
		SN74S113	
9S114	National	DM74S114	
	TI	SN54S114	
		SN74S114	
9S132	National	DM54LS132	
		DM74LS132	
	TI	SN54S132	
		SN74S132	
9S133	National	DM74S133	
	TI	SN54S133	
		SN74S133	
9S134	National	DM74S134	
	TI	SN54S134	
		SN74S134	
9S135	National	DM74S135	
	TI	SN54S135	
		SN74S135	
9S140	National	DM74S140	
	TI	SN54S140	
		SN74S140	
9S15	National	DM74S15	
	TI	SN54S15	
		SN74S15	
9S20	National	DM74S20	
	Signetics	74S20	
	TI	SN54S20	
		SN74S20	
9S22	National	DM74S22	
	Signetics	74S22	
	TI	SN54S22	
		SN74S22	
9S30	National	DM74S30	
	TI	SN54S30	
		SN74S30	
9S32	National	DM74S32	
	TI	SN54S32	
		SN74S32	
9S40	National	DM75S40	
	Signetics	74S40	
	TI	SN54S40	
		SN74S40	
9S51	National	DM74S51	
	TI	SN54S51	
		SN74S51	
9S64	National	DM74S64	
	Signetics	74S64	
	TI	SN54S64	
		SN74S64	
9S65	National	DM74S65	
	Signetics	74S65	
	TI	SN54S65	
		SN74S65	
9S74	National	DM74S74	
	TI	SN54S74	
		SN74S74	
9S86	National	DM74S86	
	TI	SN54S86	
		SN74S86	
9000	TI	SN29000	
9001	ITT	ITT9001	
	Motorola	MC3052	
		MC9001	
	TI	SN29001	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
9002	ITT	ITT9002	
	Motorola	MC7400	
	National	DM9002C	
	TI	SN29002	
		SN5400	
		SN7400	
9003	ITT	ITT9003	
	Motorola	MC7410	
	National	DM9003C	
	TI	SN29003	
		SN5410	
		SN7410	
9004	ITT	ITT9004	
	Motorola	MC7420	
	National	DM9004C	
	TI	SN29004	
		SN5420	
		SN7420	
9005	ITT	ITT9005	
	Motorola	MC7450	
	National	DM9005C	
	TI	SN29005	
		SN5450	
		SN7450	
9006	Motorola	MC7460	
	National	DM9006C	
	TI	SN5460	
		SN7460	
9007	TI	SN29007	
9008	ITT	ITT9008	
	National	DM9008C	
	TI	SN29008	
9009	ITT	ITT9009	
	Motorola	MC7440	
	National	DM9009C	
	TI	SN29009	
		SN5440	
9012	ITT	ITT9012	
	National	DM9012C	
	TI	SN29012	
		SN5403	
		SN7403	
9016	ITT	ITT9016	
	Motorola	MC7404	
	National	DM9016C	
	TI	SN29016	
		SN5404	
		SN7404	
9017	TI	SN5405	
		SN7405	
9020	ITT	ITT9020	
9022	ITT	ITT9022	
9024	ITT	ITT9024	
	National	DM74109	
		DM8024	
		DM9024	
	Signetics	74109	
	TI	SN29024	
		SN54109	
		SN74109	
9031	Signetics	N8252	
9033	Hitachi	HM2501	
	TI	SN83433	
		SN93433	
9034	Motorola	MCM4002	
	Signetics	8224	
	TI	SN5488A	
		SN7488A	
9093	Hitachi	HD2211	
	National	DM9093	
	Raytheon	RM993	
	TI	SN158093	
		SN159093	
9094	National	DM9094	
	Raytheon	RM994	
	TI	SN158094	
		SN159094	
9097	National	DM9097	
	Raytheon	RM997	
	TI	SN158097	
		SN159097	
9099	Hitachi	HD2210	
	National	DM9099	
9099	Raytheon	RM999	
	TI	SN158099	
		SN159099	
9135	National	DM935	
9157	National	DM957	
9158	National	DM958	
93H00	TI	SN54S195	
		SN74S195	
93L00	AMD	93L00	
	National	DM74L00	
	TI	SN54LS195	
		SN74LS195	
93L01	AMD	93L01	
	National	DM8301	
		DM9301	
93L08	AMD	93L08	
93L09	National	DM8309	
		DM9309	
93L10	AMD	93L10	
	National	DM76L75	
		DM86L75	
93L11	AMD	93L11	
	National	DM54L154A	
		DM74L154A	
93L12	AMD	93L12	
	National	DM8312	
		DM9312	
93L14	AMD	93L14	
93L16	AMD	93L16	
	National	DM76L76	
		DM86L76	
93L18	AMD	93L18	
	National	DM8318	
		DM9318	
93L21	AMD	93L21	
	TI	SN54LS139	
		SN74LS139	
93L22	AMD	93L22	
	National	DM54L157A	
		DM74L157A	
93L24	AMD	93L24	
93L28	AMD	93L28	
93L34	AMD	93L34	
	National	DM8334	
		DM9334	
93L38	AMD	93L38	
93L40	AMD	93L40	
93L41	AMD	93L41	
	National	DM54181	
		DM74181	
93L60	AMD	93L60	
93L66	AMD	93L66	
93S00	National	DM74S195	
	TI	SN54S195	
		SN74S195	
93S10	AMD	93S10	
	National	DM54LS160	
		DM74LS160	
93S12	AMD	93S12	
	National	DM8312	
		DM9312	
93S138	National	DM74S138	
	TI	SN54S138	
		SN74S138	
93S139	National	DM74S139	
	TI	SN54S139	
		SN74S139	
93S151	National	DM74S151	
	TI	SN54S151	
		SN74S151	
93S153	National	DM74S153	
	TI	SN54S153	
		SN74S153	
93S157	National	DM74S157	
	TI	SN54S157	
		SN74S157	
93S158	National	DM74S158	
	TI	SN54S158	
		SN74S158	
93S16	AMD	93S16	
	National	DM54LS161	
		DM74LS161	
93S174	National	DM74S174	
	TI	SN54S174	
		SN74S174	
93S175	National	DM74S175	
93S175	TI	SN54S175	
		SN74S175	
93S194	National	DM74S194	
	TI	SN54S194	
		SN74S194	
93S21	AMD	93S21	
	National	DM74S139	
93S22	AMD	93S22	
	National	DM74S157	
		DM74S22	
	TI	SN54S157	
		SN74S157	
93S251	National	DM74S251	
	TI	SN54S251	
		SN74S251	
93S253	National	DM74S253	
93S257	National	DM74S257	
	TI	SN54S257	
		SN74S257	
93S258	National	DM74S258	
	TI	SN54S258	
		SN74S258	
93S41	National	DM54181	
		DM74181	
	TI	SN54S181	
		SN74S181	
93S42	National	DM74S182	
	TI	SN54S182	
		SN74S182	
93S46	National	DM7160	
		DM8160	
93S47	National	DM7160	
		DM74S47	
		DM8160	
93S48	AMD	93S48	
930	National	DM930	
9300	AMD	9300	
	ITT	ITT9300	
	Motorola	MC9300	
	National	DM8300	
		DM9300	
	Raytheon	RC9300	
		RM9300	
	TI	SN54195	
		SN74195	
9301	AMD	9301	
	ITT	ITT9301	
	Motorola	MC9301	
	National	DM8301	
		DM9301	
	TI	SN29301	
		SN39301	
9304	AMD	9304	
	ITT	ITT9304	
	Mitsubishi	M54304	
	Motorola	MC9304	
	Raytheon	RC9304	
		RM9304	
9306	AMD	9306	
	Motorola	MC9306	
9307	Motorola	MC9307	
	National	DM5448	
		DM7448	
	TI	SN5448A	
		SN7448A	
9308	AMD	9308	
	Motorola	MC9308	
	Raytheon	RC9308	
		RM9308	
	TI	SN29308	
		SN39308	
		SN54116	
		SN74116	
9309	AMD	9309	
	Motorola	MC9309	
	National	DM8309	
		DM9309	
	TI	SN29309	
		SN39309	
9310	AMD	9310	
	Motorola	MC8310	
		MC9310	
	National	DM74160	
		DM8310	
		DM9310	
	Raytheon	RC9310	
9310	Raytheon	RM9310	
	TI	SN29310	
		SN39310	
		SN54160	
		SN74160	
9311	AMD	9311	
	Motorola	MC8311	
		MC9311	
	National	DM8311	
		DM9311	
	Raytheon	RC9311	
		RM9311	
	TI	SN29311	
		SN39311	
		SN54154	
		SN74154	
9312	AMD	9312	
	ITT	ITT9312	
	Motorola	MC9312	
	National	DM8312	
		DM9312	
	Raytheon	RC9312	
		RM9312	
	Signetics	8230	
	TI	SN29312	
		SN39312	
9314	AMD	9314	
	Motorola	MC9314	
93141	National	DM54141	
		DM74141	
	TI	SN74141	
93145	ITT	ITT74145	
	Motorola	MC83145	
		MC93145	
	National	DM54145	
		DM74145	
	Raytheon	54145	
		74145	
	TI	SN54145	
		SN74145	
9315	Motorola	MC8315	
		MC9315	
	National	DM5441	
		DM7441A	
	Signetics	7441	
	TI	SN54141	
93150	Motorola	MC83150	
		MC93150	
	National	DM54150	
		DM74150	
	Raytheon	54150	
		74150	
	TI	SN54150	
		SN74150	
93151	ITT	ITT74151	
	Motorola	MC83151	
		MC93151	
	National	DM54151	
		DM74151	
	Raytheon	54151	
		74151	
	TI	SN54151A	
		SN74151A	
93152	Motorola	MC83152	
		MC93152	
	Raytheon	54152	
		74152	
	TI	SN54152A	
		SN74152	
93153	ITT	ITT74153	
	Motorola	MC83153	
		MC93153	
	National	DM54153	
		DM74153	
	Raytheon	54153	
		74153	
	TI	SN54153	
		SN74153	
93155	National	DM54155	
		DM74155	
	Raytheon	54155	
		74155	
	TI	SN54155	
		SN74155	
93156	National	DM54156	
		DM74156	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Fairchild (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
93156	Raytheon	54156	
		74156	
	TI	SN54156	
		SN74156	
93157	National	DM54157	
		DM74157	
	TI	SN54157	
		SN74157	
9316	AMD	9316	
	ITT	ITT9316	
	Motorola	MC8316	
		MC9316	
	National	DM8316	
		DM9316	
	Raytheon	RC9316	
		RM9316	
	TI	SN29316	
		SN39316	
		SN54161	
		SN74161	
93160	National	DM54160	
		DM74160	
	TI	SN54160	
		SN74160	
93161	National	DM54161	
		DM74161	
	TI	SN54161	
		SN74161	
93162	National	DM54162	
		DM74162	
	TI	SN54162	
		SN74162	
93163	National	DM54163	
		DM74163	
	Raytheon	54163	
		74163	
	TI	SN54163	
		SN74163	
93164	AMD	SN74164	
	Motorola	MC83164	
		MC93164	
	National	DM54164	
		DM74164	
	TI	SN54164	
		SN74164	
93165	Motorola	MC83165	
	National	DM54165	
		DM74165	
	Raytheon	54165	
		74165	
	TI	SN54165	
		SN74165	
93166	National	DM54166	
		DM74166	
	Raytheon	54166	
		74166	
	TI	SN54166	
		SN74166	
9317B	National	DM5447	
		DM7447	
	TI	SN5446A	
		SN7446A	
9317C	National	DM5446	
		DM7446	
	TI	SN29318	
		SN39318	
		SN5446A	
		SN7446A	
93170	National	DM74170	
	Raytheon	54170	
		74170	
	TI	SN54170	
		SN74170	
93174	AMD	SN74174	
	National	DM54174	
		DM74174	
	Raytheon	54174	
		74174	
	TI	SN54174	
		SN74174	
93175	AMD	SN74175	
	National	DM54175	
		DM74175	
93175	Raytheon	54175	
		74175	
	TI	SN54175	
		SN74175	
93176	Motorola	MC93176	
	National	DM54176	
		DM74176	
	TI	SN54176	
		SN74176	
93177	Motorola	MC83177	
		MC93177	
	National	DM54177	
		DM74177	
	TI	SN54177	
		SN74177	
93178	Motorola	MC83178	
		MC93178	
	TI	SN54178	
		SN74178	
93179	Motorola	MC83179	
		MC93179	
	TI	SN54179	
		SN74179	
9318	AMD	9318	
	Motorola	MC9318	
	National	DM8318	
		DM9318	
	TI	SN54148	
		SN74148	
93180	ITT	ITT74180	
	Motorola	MC83180	
		MC93180	
	National	DM54180	
		DM74180	
	Raytheon	54180	
		74180	
	TI	SN54180	
		SN74180	
93190	National	DM54190	
		DM74190	
	Raytheon	54190	
		74190	
	TI	SN54190	
		SN74190	
93191	National	DM54191	
		DM74191	
	Raytheon	54191	
		74191	
	TI	SN54191	
		SN74191	
93194	AMD	SN74194	
	National	DM54194	
		DM74194	
	Raytheon	54194	
		74194	
	TI	SN54194	
		SN74194	
93195	National	DM54195	
		DM74195	
	TI	SN54195	
		SN74195	
93196	Motorola	MC7280	
	National	DM54196	
		DM74196	
	TI	SN54196	
		SN74196	
93197	Motorola	MC8280	
	National	DM54197	
		DM74197	
	TI	SN54197	
		SN74197	
93198	Motorola	MC8316	
	National	DM54198	
		DM74198	
	Raytheon	54198	
		74198	
	Signetics	54198	
		74198	
	TI	SN54198	
		SN74198	
93199	National	DM54199	
		DM74199	
	Raytheon	54199	
		74199	
	TI	SN54199	
		SN74199	
932	National	DM932	
9321	AMD	9321	
	National	DM54LS139	
		DM74LS139	
	TI	SN54S139	
		SN74S139	
9322	AMD	9322	
	ITT	ITT9322	
	Motorola	MC8322	
		MC9322	
	National	DM74157	
		DM8322	
		DM9322	
	Raytheon	RC9322	
		RM9322	
		54157	
		74157	
	TI	SN29322	
		SN39322	
		SN54157	
		SN74157	
9324	AMD	9324	
	Motorola	MC9324	
9325	National	DM54141	
		DM74141	
	Signetics	54141	
		74141	
	TI	SN74141	
9328	AMD	9328	
	ITT	ITT9328	
	Motorola	MC9328	
	Signetics	N8277	
933	National	DM933	
9334	AMD	9334	
	Motorola	MC9334	
	National	DM9334	
	TI	SN54259	
		SN74259	
9338	AMD	9338	
9340	AMD	9340	
93400	Motorola	MCM4012	
♦93403	AMD	93403	
	Fairchild	7489	
	MMI	6560	
	Motorola	MCM4064	
		MC4064	
	National	**DM7489**	**1287**
	Signetics	N82S25	
	TI	SN54S289	
		SN74S289	
		SN7489	
93404	Signetics	82S25	
♦93406	Intersil	IM5603	
	MMI	**6200**	**1252**
	Motorola	MCM4006	
	Signetics	N82S226	
	TI	SN54187	
		SN74187	
93407	Motorola	MC4004	
		MC4304	
	TI	SN5481A	
		SN7481A	
9341	AMD	9341	
	Motorola	MC8341	
		MC9341	
	National	DM54181	
		DM74181	
	Raytheon	RC9341	
		RM9341	
		54181	
		74181	
	Signetics	54181	
		74181	
	TI	SN54181	
		SN74181	
♦93410	Motorola	MCM4056	
	Signetics	N93410	
		54S301	
		74S301	
	TI	SN54S300	
		SN54S301	
		SN74S300	
		SN74S301	
93411	MMI	5530	
		6530	
		6531	
93411	**National**	**DM54S206**	**1297**
		DM74S206	**1297**
	NEC Micro	μPB2206	
	Raytheon	RC5330	
		RM5330	
	Signetics	82S17	
	TI	SN54S200A	
		SN54S201	
		SN74S200A	
		SN74S201	
♦93412	Intersil	IM5600	
	TI	SN54S214	
		SN74S214	
93415	**AMI**	**S4015**	**1032**
	Fujitsu	MBM93415	
	Intel	2115	
	Motorola	MCM93415	
	NEC Micro	**μPB2205**	**1418**
	Raytheon	RC5500	
		RM5500	
	RCA	MWS5001	
		MWS5501	
	Signetics	N82S10	
	TI	SN54S314	
		SN74S314	
93415A	Fujitsu	MBM93415A	
	Intel	2115A	
	Signetics	93415A	
	TI	SN54S314A	
		SN74S314A	
93416	Harris	HPROM1024A	
	Intel	3601	
	Intersil	IM5603	
	MMI	**6300**	**1252**
	NEC Micro	μPD403	
	Signetics	N82S126	
	TI	SN54S387	
		SN74S387	
93417	**Harris**	**HM7610**	**1192**
		HM7610A	**1200**
	MMI	**5300**	**1248**
		6300	**1252**
	National	**DM54S387**	**1264**
		DM74S387	**1264**
	NEC Micro	**μPB403**	**1462**
	TI	SN54S387	
		SN74S387	
934183	TI	SN54H183	
		SN74H183	
9342	AMD	9342	
	ITT	ITT74182	
	Motorola	MC8342	
		MC9342	
	National	DM54182	
		DM74182	
	Raytheon	RM9342	
		54182	
		74182	
	Signetics	54182	
		74182	
	TI	SN54182	
		SN74182	
93421	MMI	5531	
		6531	
	National	DM54S200	
		DM74S200	
	Raytheon	RC5340	
		RM5340	
	Signetics	N82S16	
	TI	SN54S200A	
		SN54S201	
		SN74S200A	
		SN74S201	
93425	**AMI**	**S4025**	**1032**
	Intel	2125	
	RCA	MWS5001	
		MWS5501	
	TI	SN54S214	
93425A	Intel	2125A	
	Signetics	93425	
	TI	SN54S214A	
		SN74S214	
93426	Harris	HPROM1024	
	Intel	3621	
	Intersil	IM5623	
	MMI	**6301**	**1252**

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Manufacturer Device	Replacement Source	Device	IC Master Page
Fairchild (cont'd)			
93426	Signetics	N82S129	
	TI	SN54S287	
		SN74S287	
93427	**Harris**	**HM7611**	**1192**
		HM7611A	**1200**
	MMI	**5301**	**1248**
		6301	**1252**
	National	**DM54S287**	**1264**
		DM74S287	**1264**
	TI	SN54S287	
		SN74S287	
93433	Motorola	MC4004	
	TI	SN83433	
		SN93433	
♦93434	Intersil	IM5600	
	MMI	**5230**	**1252**
		6230	**1252**
	Motorola	MCM4002	
	National	DM5487	
		DM7488	
	Signetics	8223	
	TI	SN5488A	
		SN7488A	
93435	MMI	5560	
		6560	
	Motorola	MC4064	
	TI	SN7489	
93436	**Harris**	**HM7621**	**1192**
		HM7621A	**1202**
	Intel	3602	
	Intersil	IM5604	
	MMI	**5305**	**1248**
		6305	**1252**
	National	DM54S570	
		DM74S570	**1266**
	Signetics	82S130	
	TI	SN54S270	
		SN74S270	
93438	**Harris**	**HM7640**	**1192**
		HM7640A	**1204**
	MMI	**5340**	**1563**
		6340	**1252**
	National	**DM77S295**	**1270**
		DM87S295	**1270**
	NEC Micro	μPB405	
	TI	SN54S475	
		SN74S475	
93446	**Harris**	**HM7621**	**1192**
		HM7621A	**1202**
	Intel	3622	
	MMI	**5306**	**1248**
		6306	**1252**
	National	**DM54S571**	**1266**
		DM74S571	**1266**
	Signetics	82S131	
93448	**Harris**	**HM7641**	**1192**
		HM7641A	**1204**
	MMI	**5341**	**1563**
		6341	**1252**
	National	**DM77S296**	**1270**
		DM87S296	**1270**
	NEC Micro	**μPB425**	**1466**
	TI	SN54S474	
		SN74S474	
9345	ITT	ITT7445	
	Motorola	MC9345	
	National	DM5445	
		DM7445	
	Raytheon	5445	
		7445	
	Signetics	5445	
		7445	
	TI	SN5445A	
		SN7445A	
93452	**MMI**	**5352**	**1563**
		6352	**1252**
	National	**DM54S572**	**1268**
		DM74S572	**1268**
	NEC Micro	**μPB406**	**1470**
93453	**MMI**	**5353**	**1563**
		6353	**1252**
	National	**DM54S573**	**1268**
		DM74S573	**1268**
93453	**NEC Micro**	**μPB426**	**1470**
93487	TI	SN54H87	
		SN74H87	
9349	Raytheon	54180	
		74180	
	Signetics	54180	
		74180	
	TI	SN54180	
		SN74180	
935	National	DM935	
9350	TI	SN54290	
		SN74290	
9352	ITT	ITT7442	
	Motorola	MC8352	
		MC9352	
	National	DM5442	
		DM7442	
	Signetics	5442	
		7442	
	TI	SN5442	
		SN7442	
9353	ITT	ITT7443	
	Motorola	MC8353	
		MC9353	
	Signetics	5443	
		7443	
	TI	SN5443	
		SN7443	
9354	ITT	ITT7444	
	Motorola	MC8354	
		MC9354	
	Signetics	5444	
		7444	
	TI	SN5444A	
		SN7444A	
9355	Motorola	MC8355	
9356	TI	SN54293	
		SN74293	
9357	Motorola	MC8357	
		MC9357	
9357A	ITT	ITT7446A	
	Motorola	MC9357A	
	National	DM5446A	
		DM7446A	
	Signetics	7446	
	TI	SN5446A	
		SN7446A	
9357B	ITT	ITT7447A	
	Motorola	MC9357B	
	National	DM5447A	
		DM7447A	
	Signetics	7447	
	TI	SN5447A	
		SN7447A	
9358	ITT	ITT7448	
	Motorola	MC8358	
		MC9358	
	National	DM5448	
		DM7448	
	Signetics	7448	
	TI	SN5448	
		SN7448	
9359	Motorola	MC8359	
		MC9359	
	TI	SN54293	
936	National	DM936	
9360	AMD	9360	
	ITT	ITT74192	
	Motorola	MC8360	
		MC9360	
	National	DM54192	
		DM74192	
	Raytheon	RC9360	
		RM9360	
		54192	
		74192	
	Signetics	54192	
		74192	
	TI	SN54192	
		SN74192	
9366	AMD	9366	
	ITT	ITT74193	
	Motorola	MC8366	
		MC9366	
	National	DM54193	
		DM74193	
9366	Raytheon	RM9366	
		54193	
		74193	
	Signetics	54193	
		74193	
	TI	SN54193	
		SN74193	
9368	Mitel	MD4368	
937	National	DM937	
9375	ITT	ITT7475	
	Motorola	MC9375	
	National	DM5475	
		DM7475	
	Signetics	5475	
		7475	
	TI	SN5475	
		SN7475	
9377	Motorola	MC8377	
		MC9377	
	National	DM54LS77	
		DM74LS77	
	TI	SN5477	
		SN7477	
9380	ITT	ITT7480	
	Motorola	MC8380	
		MC9380	
	Signetics	5480	
		7480	
	TI	SN5480	
		SN7480	
9382	ITT	ITT7482	
	Motorola	MC8382	
		MC9382	
	National	DM7482	
	TI	SN5482	
		SN7482	
9383	ITT	ITT7483	
	Motorola	MC8383	
		MC9383	
	National	DM5483	
		DM7483	
	Signetics	5483	
		7483	
	TI	SN5483A	
		SN7483A	
9385	National	DM5485	
		DM7485	
9386	TI	SN54LS266	
		SN74LS266	
939	National	DM939	
9390	ITT	ITT7490	
	Motorola	MC8390	
		MC9390	
	National	DM5490	
		DM7490	
	Signetics	5490	
		7490	
	TI	SN5490A	
		SN7490A	
9391	ITT	ITT7491	
	Motorola	MC8391	
		MC9391	
	National	DM5491	
		DM7491	
	Signetics	5491	
		7491	
	TI	SN5491A	
		SN7491A	
9392	ITT	ITT7492	
	Motorola	MC8392	
		MC9392	
	National	DM5492	
		DM7492	
	Signetics	9392	
	TI	SN5492A	
		SN7492A	
9393	ITT	ITT7493	
	Motorola	MC8393	
		MC9393	
	National	DM5493	
		DM7493	
	Signetics	5493	
		7493	
	TI	SN5493	
		SN7493	
9394	Motorola	MC8394	
9394	Motorola	MC9394	
	Signetics	5494	
		7494	
	TI	SN5494	
		SN7494	
9395	ITT	ITT7495A	
	Motorola	MC8395	
		MC9395	
	National	DM5495	
		DM7495	
	Signetics	5495	
		7495	
	TI	SN5495A	
		SN7495A	
9396	ITT	ITT7496	
	Motorola	MC8396	
		MC9396	
	National	DM5496	
		DM7496	
	Signetics	5496	
		7496	
	TI	SN5496	
		SN7496	
9409	AMD	AM2901A	
	Fairchild	2901A	
	Motorola	MC2901	
	National	**IDM2901A**	**1656,1680**
	NEC Micro	**μPB2901**	**1850**
	Raytheon	AM2901A	
	Signetics	MP2901	
944	National	DM944	
945	National	DM945	
946	National	DM946	
948	National	DM948	
949	National	DM949	
95H90	Plessey	SP640	
95H91	Plessey	SP641	
95H92	Plessey	SP642	
95H93	Plessey	SP643	
96L02	National	DM9602	
96S02	National	DM8602	
		DM9602	
9600	AMD	9600	
9601	AMD	9601	
	ITT	ITT9601	
	Motorola	MC9601	
	National	DM8601	
		DM9601	
	Raytheon	RF8601	
		RF9601	
	TI	SN29601	
9602	AMD	9602	
	ITT	ITT9602	
	Motorola	MC9602	
	National	DM8602	
		DM9602	
	Raytheon	RF8602	
		RF9602	
9603	ITT	ITT74121	
	Motorola	MC8603	
		MC9603	
	National	DM54121	
		DM74121	
	Signetics	54121	
		74121	
	TI	SN54121	
		SN74121	
961	National	DM961	
9614	AMD	9614	
	ITT	ITT9614	
	TI	SN55114	
		SN75114	
9615	AMD	9615	
	ITT	ITT9615	
	TI	SN55115	
		SN75115	
9616	AMD	9616	
9617	AMD	9617	
96176	Motorola	MC83176	
962	National	DM962	
9620	AMD	9620	
9621	AMD	9621	
	Raytheon	RC9621	
		RM9621	
9622	Raytheon	RC9622	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Manufacturer Device	Replacement Source	Device	IC Master Page
Fairchild (cont'd)			
9622	Raytheon	RM9622	
963	National	DM963	
9637	Motorola	MC3486	
9638	Motorola	MC3487	
9640	AMD	AM26S10	
	Motorola	MC3440	
		MC3443	
	TI	AM26S10	
9641	AMD	AM26S11	
	TI	AM26S11	
9664	Signetics	7524	
	TI	SN75492	
9665	Exar	XR2201	
	Motorola	MC1411	
	SGS	L201	
	Signetics	NE5501	
		ULN2001	
		7525	
	Silicon G	SG2001	
	Sprague	ULN-2001	
	TI	ULN2001	
9666	Exar	XR2202	
	Motorola	MC1412	
	SGS	L202	
	Signetics	NE5502	
		ULN2002	
	Silicon G	SG2002	
	Sprague	ULN-2002	
	TI	ULN2002	
9667	Exar	XR2203	
	Motorola	MC1413	
	SGS	L203	
	Signetics	NE5503	
		ULN2003	
	Silicon G	SG2003	
	Sprague	ULN-2003	
	TI	ULN2003	
9668	Exar	XR2204	
	Motorola	MC1416	
	Signetics	NE5504	
		ULN2004	
	Silicon G	SG2004	
	Sprague	ULN-2004	
	TI	ULN2004	
9930	Hitachi	HD2204	
	Raytheon	RM930	
	TI	SN15830	
		SN15930	
9932	Hitachi	HD2201	
	Raytheon	RM932	
	TI	SN15832	
		SN15932	
9933	Hitachi	HD2202	
	Raytheon	RM933	
	TI	SN15833	
		SN15933	
9935	Hitachi	HD2208	
	Raytheon	RM935	
	TI	SN15835	
		SN15935	
9936	Hitachi	HD2206	
	Raytheon	RM936	
	TI	SN15836	
		SN15936	
9937	Raytheon	RM937	
	TI	SN15837	
		SN15937	
9941	Raytheon	RM941	
	TI	SN15841	
		SN15941	
9944	Hitachi	HD2209	
	Raytheon	RM944	
	TI	SN15844	
		SN15944	
9945	Hitachi	HD2205	
	Raytheon	RM945	
	TI	SN15845	
		SN15945	
9946	Hitachi	HD2203	
	Raytheon	RM946	
	TI	SN15846	
		SN15946	
9948	Raytheon	RM948	
9948	TI	SN15848	
		SN15948	
9949	TI	SN15849	
		SN15949	
9950	Raytheon	RM950	
	TI	SN15850	
		SN15950	
9951	Raytheon	RM951	
	TI	SN15851	
		SN15951	
9961	Raytheon	RM961	
	TI	SN15861	
		SN15961	
9962	Hitachi	HD2207	
	Raytheon	RM962	
	TI	SN15862	
		SN15962	
9963	Raytheon	RM963	
	TI	SN15863	
		SN15963	
Ferranti Electric			
ZN425	Datel	ADC-MC8B	
Fujitsu			
MB2114	**NEC Micro**	**μPD2114**	**1489**
MB7054	**NEC Micro**	**μPB426**	**1470**
MB7055	Signetics	N82S2708	
MB7057	**NEC Micro**	**μPB403**	**1462**
MB7059	**NEC Micro**	**μPB406**	**1470**
MB8101	**NEC Micro**	**μPD2101AL**	**1424**
MB8107	**NEC Micro**	**μPD411**	**1375**
MB8111	**NEC Micro**	**μPD2111AL**	**1433**
MB8114	TI	TMS4045	
MB8116	**NEC Micro**	**μPD416**	**1402**
MB8224	**NEC Micro**	**μPD414**	**1395**
MB8227	**NEC Micro**	**μPD414A**	**1395,1488**
MB8308	**NEC Micro**	**μPD2308**	**1478**
MB8515	AMD	2708	
	EA	EA2708	
	Intel	2708	
	Mostek	MK2708	
	Motorola	MCM2708	
	National	MM2708	
	TI	TMS2708	
MB93415	**NEC Micro**	**μPB2205**	**1418**
General Instrument			
AY1-0212	AMI	S50242	
AY1-2006	AMI	S10131	
♦AY5-1012	TI	TMS6011	
AY5-1013A	**AMI**	**S1883**	**354,1587**
	SMC	COM2502H	
	Western	TR1402	
		TR1602	
AY5-2376	SMC	KR2376	
AY5-3507	Plessey	μP3202	
AY5-3600	SMC	KR3600	
♦DL9-1402	SGS	M141	
	Signetics	2502	
♦DL9-1403	SGS	M136	
♦DL9-1404	SGS	M130	
		M141	
RA3-4402	EMM/Semi	4402	
♦RA9-1101	Intersil	IM7501	
		IM7511	
	Mostek	MK4007	
♦RA9-1103	Signetics	1103	
♦RO1-2048	AMI	S8773	
RO3-16384	AMI	S8996	
	EMM/Semi	RO3-16384	
RO3-4096	EMM/Semi	RO3-4096	
RO3-5120	EMM/Semi	RO3-5120	
RO3-8316	EMM/Semi	RO3-8316	
	Mostek	MK31000	
RO3-9316	Mostek	MK34000	
RO5-2240	Mostek	MK2302	
RO5-8192	AMI	S8865	
♦RO6-1024	AMI	S8773	
♦RO6-2048	AMI	S8773	
Harris Semiconductor			
HA-2055	Datel	AM-405-2	
HA-2065	Datel	AM-406-2	
HA-2425	**Datel**	**SHM-IC-1**	**393**
HA-2500	Intersil	HA2500	
HA-2502	Intersil	HA2502	
HA-2505	Datel	AM-450-2	
	Intersil	HA2505	
HA-2520	AD	AD509	
	Intersil	HA2520	
HA-2522	AD	AD509	
	Intersil	HA2522	
HA-2525	AD	AD509	
	Datel	AM-452-2	
	Intersil	HA2525	
HA-2600	Intersil	HA2600	
HA-2602	Intersil	HA2602	
HA-2605	Datel	AM-460	
HA-2620	Intersil	HA2620	
HA-2622	Intersil	HA2622	
HA-2625	AD	AD507	
	Datel	AM-462-2	
HA-2640	National	LM143	
HA-2645	Datel	AM-464-2	
	National	LM343	
HA-2650	Exar	XR1558	
HA-2665	Exar	XR1458	
HA-2720	Fairchild	μA776	
	Intersil	8021	
HA-2905	Datel	AN-490-2	
	TI	TL089	
HA-4741	Exar	XR4741	
	Raytheon	HA4741	
HA1488	Signetics	MC1488	
♦HD14518	RCA	CD4518	
	SSS	SCL4518	
♦HD14520	RCA	CD4520	
	SSS	SCL4520	
♦HD14529	RCA	CD4052	
HD1489	Signetics	MC1489	
HD1489A	Signetics	MC1489A	
♦HD4000	Motorola	MC14000	
	RCA	CD4000	
	SSS	SCL4000	
♦HD4001	Motorola	MC14001	
	National	CD4001	
	RCA	CD4001	
	SSS	SCL4001	
♦HD4002	Motorola	MC14002	
	National	CD4002	
	RCA	CD4002	
	SSS	SCL4002	
♦HD4006	RCA	CD4006	
	SSS	SCL4006	
♦HD4007	Motorola	MC14007	
	National	CD4007	
	RCA	CD4007	
	SSS	SCL4007	
♦HD4008	RCA	CD4008	
♦HD4011	National	CD4011	
	RCA	CD4011	
	SSS	SCL4011	
♦HD4012	Motorola	MC14012	
	National	CD4012	
	RCA	CD4012	
	SSS	SCL4012	
♦HD4013	Motorola	MC14013	
	National	CD4013	
	RCA	CD4013	
	SSS	SCL4013	
♦HD4014	National	CD4014	
	RCA	CD4014	
	SSS	SCL4014	
♦HD4015	National	CD4015	
	RCA	CD4015	
	SSS	SCL4015	
♦HD4017	National	CD4017	
	RCA	CD4017	
	SSS	SCL4017	
♦HD4018	National	CD4018	
	RCA	CD4018	
	SSS	SCL4018	
♦HD4019	National	CD4019	
	RCA	CD4019	
	SSS	SCL4019	
♦HD4020	National	CD4020	
	RCA	CD4020	
	SSS	SCL4020	
♦HD4021	National	CD4021	
	RCA	CD4021	
	SSS	SCL4021	
♦HD4022	National	CD4022	
	RCA	CD4022	
	SSS	SCL4022	
♦HD4023	Motorola	MC14023	
	National	CD4023	
	RCA	CD4023	
	SSS	SCL4023	
♦HD4024	National	CD4024	
	RCA	CD4024	
	SSS	SCL4024	
♦HD4025	Motorola	MC14025	
	National	CD4025	
	RCA	CD4025	
	SSS	SCL4025	
♦HD4027	National	CD4027	
	RCA	CD4027	
	SSS	SCL4027	
♦HD4028	National	CD4028	
	RCA	CD4028	
	SSS	SCL4028	
♦HD4029	National	CD4029	
	RCA	CD4029	
	SSS	SCL4029	
♦HD4030	National	CD4030	
	RCA	CD4030	
		CD4070	
	SSS	SCL4030	
♦HD4035	National	CD4035	
	RCA	CD4035	
	SSS	SCL4035	
♦HD4040	National	CD4040	
	RCA	CD4040	
	SSS	SCL4040	
♦HD4042	National	CD4042	
	SSS	SCL4042	
♦HD4049	National	CD4049	
	RCA	CD4049	
	SSS	SCL4049	
♦HD4050	National	CD4050	
	RCA	CD4050	
	SSS	SCL4050	
♦HD4066	National	CD4066	
	RCA	CD4066	
	SSS	SCL4066	
HD4702	Fairchild	F4702	
HD54C00	National	MM54C00	
HD54C02	National	MM54C02	
HD54C04	National	MM54C04	
HD54C08	National	MM54C08	
HD54C10	National	MM54C10	
HD54C107	National	MM54C107	
HD54C14	National	MM54C14	
HD54C151	National	MM54C151	
HD54C154	National	MM54C154	
HD54C157	National	MM54C157	
HD54C160	National	MM54C160	
	SSS	SCL4160	
HD54C161	National	MM54C161	
	SSS	SCL4161	
HD54C162	National	MM54C162	
	SSS	SCL4162	
HD54C163	National	MM54C163	
	SSS	SCL4163	
HD54C164	National	MM54C164	
HD54C165	National	MM54C165	
HD54C173	National	MM54C173	
HD54C174	National	MM54C174	
HD54C175	National	MM54C175	
HD54C192	National	MM54C192	
HD54C193	National	MM54C193	
HD54C195	National	MM54C195	
HD54C20	National	MM54C20	
HD54C200	**National**	**MM54C200**	**1355**
HD54C221	National	MM54C221	
HD54C30	National	MM54C30	
HD54C32	National	MM54C32	
HD54C42	National	MM54C42	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Harris Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
HD54C48	National	MM54C48	
HD54C73	National	MM54C73	
HD54C74	National	MM54C74	
HD54C76	National	MM54C76	
HD54C83	National	MM54C83	
HD54C85	National	MM54C85	
HD54C86	National	MM54C86	
HD54C89	**National**	**MM54C89**	**1352**
HD54C90	National	MM54C90	
HD54C901	National	MM54C901	
HD54C902	National	MM54C902	
HD54C903	National	MM54C903	
HD54C904	National	MM54C904	
HD54C906	National	MM54C906	
HD54C907	National	MM54C907	
HD54C914	National	MM54C914	
HD54C922	National	MM54C922	
HD54C923	National	MM54C923	
HD54C925	National	MM54C925	
HD54C926	National	MM54C926	
HD54C927	National	MM54C927	
HD54C928	National	MM54C928	
HD54C93	National	MM54C93	
HD54C95	National	MM54C95	
HD6101	Intersil	IM6101	
HD6101A	Intersil	IM6101A	
HD6101C	Intersil	IM6101C	
HD6402	Intersil	IM6402	
HD6402A	Intersil	IM6402A	
HD6402C	Intersil	IM6402C	
HD6403	Intersil	IM6403	
HD6403A	Intersil	IM6403A	
HD6403C	Intersil	IM6403C	
HD70C95	National	MM70C95	
HD70C97	National	MM70C97	
HD74C00	National	MM54C95	
		MM74C00	
	RCA	CD4011	
HD74C02	National	MM74C02	
	RCA	CD4001	
HD74C04	Fairchild	F4069	
	Mitel	SIL4069	
	Motorola	MC14069	
	National	CD4069	
		MM74C04	
	NEC America	μPD4069	
	RCA	CD4069	
	Solitron	CM4069	
	SSS	SCL4069	
	TI	TP4069	
	Toshiba	TC4069	
HD74C08	National	MM74C08	
HD74C10	National	MM74C10	
	RCA	CD4023	
HD74C107	National	MM74C107	
HD74C14	National	MM74C14	
	SSS	SCL4584	
HD74C151	National	MM74C151	
HD74C154	National	MM74C154	
HD74C157	National	MM74C157	
HD74C160	Fairchild	F40160	
	National	MM74C160	
	SSS	SCL4160	
HD74C161	Fairchild	F40161	
	National	MM74C161	
	SSS	SCL4161	
HD74C162	Fairchild	F40162	
	National	MM74C162	
	SSS	SCL4162	
HD74C163	Fairchild	F40163	
	National	MM74C163	
	SSS	SCL4163	
HD74C164	National	MM74C164	
HD74C165	National	MM74C165	
HD74C173	Fairchild	F4076	
	Mitel	SIL4076	
	Motorola	MC14076	
	National	CD4076	
		MM74C173	
	RCA	CD4076	
	Solitron	CM4076	
	SSS	SCL4076	
HD74C174	Fairchild	F40174	
HD74C174	National	MM74C174	
HD74C175	Fairchild	F40175	
	National	MM74C175	
HD74C192	Fairchild	F40192	
	National	MM74C192	
	RCA	CD40192	
HD74C193	Fairchild	F40193	
	National	MM74C193	
	RCA	CD40193	
HD74C195	Fairchild	F40195	
	National	MM74C195	
HD74C20	National	MM74C20	
	RCA	CD4012	
HD74C200	**National**	**MM74C200**	**1355**
HD74C221	National	MM74C221	
HD74C30	National	MM74C30	
HD74C32	National	MM74C32	
HD74C42	National	MM74C42	
	RCA	CD4028	
HD74C48	National	MM74C48	
HD74C73	National	MM74C73	
HD74C74	National	MM74C74	
	RCA	CD4013	
HD74C76	National	MM74C76	
	RCA	CD4027	
HD74C83	National	MM74C83	
HD74C85	Fairchild	F40085	
	National	MM74C85	
HD74C86	National	MM74C86	
HD74C89	**National**	**MM74C89**	**1352**
HD74C90	National	MM74C90	
HD74C901	National	MM74C901	
HD74C902	National	MM74C902	
HD74C903	National	MM74C903	
HD74C904	National	MM74C904	
HD74C906	National	MM74C906	
HD74C907	National	MM74C907	
HD74C914	National	MM74C914	
HD74C922	National	MM74C922	
HD74C923	National	MM74C923	
HD74C925	National	MM74C925	
HD74C926	National	MM74C926	
HD74C927	National	MM74C927	
HD74C928	National	MM74C928	
HD74C93	National	MM74C93	
HD74C95	National	MM74C95	
HD80C95	National	MM70C95	
HD80C97	Fairchild	F40097	
	National	MM70C97	
		MM80C97	
HI1818	RCA	CD4051	
HI1828	RCA	CD4052	
HI5040	Intersil	IH5040	
HI5041	Intersil	IH5041	
HI5042	Intersil	IH5042	
HI5044	Intersil	IH5044	
HI5045	Intersil	IH5045	
HI5046	Intersil	IH5046	
HI5047	Intersil	IH5047	
HI5048	Intersil	IH5048	
HI5049	Intersil	IH5049	
HI5050	Intersil	IH5050	
HI5051	Intersil	IH5051	
HI506	Datel	MV-1606	
	Intersil	IH5060	
	RCA	CD4067	
	Siliconix	DG506	
HI506A	Datel	MX-1606	
	Teledyne P	4552	
HI507	Datel	MVD-807	
	RCA	CD4097	
	Siliconix	DG507	
HI507A	Datel	MXD-807	
	Teledyne P	4551	
HI508	RCA	CD4051	
HI508A	Datel	MX-808	
HI509	RCA	CD4052	
HI509A	Datel	MXD-409	
HM5101	**AMI**	**S5101**	**1041**
HM6100	Intersil	IM6100	
HM6100A	Intersil	IM6100A	
HM6100C	Intersil	IM6100C	
HM6501	**AMI**	**S5101**	**1041**
	Intel	2101	
		5101	
	NEC Micro	**μPD5101**	**1438**
HM6501	RCA	CPD1822	
		MWS5040	
HM6504	AMD	9145	
	Mostek	MK4104	
HM6508	**AMI**	**S6508**	**1046**
	Intel	2125	
	Intersil	IM6508	
	National	**MM74C929**	**1363**
	NEC Micro	**μPD6508**	**1488**
HM6514	Intel	2114	
HM6518	AMI	S6518	
	Intersil	IM6518	
	National	**MM74C930**	**1363**
HM6551	Intersil	IM6551	
	National	**MM74C920**	**1361**
HM6561	Intersil	IM6561	
HM7602	AMD	AM27S09	
	MMI	**5330**	**1248**
		6330	**1252**
	National	DM7577	
		DM8577	
	Signetics	N82S23	
	TI	SN54S188	
		SN74S188	
HM7603	**MMI**	**5331**	**1248**
		6331	**1252**
	Signetics	N82S123	
	TI	SN54S288	
		SN74S288	
HM7610	Intel	3601-1	
	Intersil	IM5603	
	MMI	**5300**	**1248**
		6300	**1252**
	National	**DM54S387**	**1264**
		DM74S387	**1264**
	NEC Micro	**μPB403**	**1462**
	Signetics	N82S126	
	TI	SN54S387	
		SN74S387	
HM7611	Intel	3621-1	
	Intersil	IM5623	
	MMI	**5301**	**1248**
		6301	**1252**
	National	DM7574	
	Signetics	82S129	
	TI	SN54S287	
		SN74S287	
HM7620	Intel	3602	
	MMI	**5305**	**1248**
		6305	**1252**
	National	DM54S570	
		DM74S570	**1266**
	Signetics	82S130	
	TI	SN54S270	
		SN74S270	
HM7621	Intel	3622	
	MMI	**5306**	**1248**
		6306	**1252**
	National	**DM54S571**	**1266**
		DM74S571	**1266**
	Signetics	82S131	
	TI	SN54S370	
		SN74S370	
HM7640	Intel	3604	
	MMI	**5340**	**1563**
		6340	**1252**
	Motorola	MCM7640	
	National	**DM77S295**	**1270**
		DM87S295	**1270**
	NEC Micro	μPB405	
	RCA	CD40032	
	TI	SN54S475	
		SN74S475	
HM7641	Intel	3624	
	MMI	**5341**	**1563**
		6341	**1252**
	Motorola	MCM7641	
	National	**DM77S296**	**1270**
		DM87S296	**1270**
	NEC Micro	**μPB425**	**1466**
	TI	SN54S474	
		SN74S474	
HM7642	Intel	3605	
	MMI	**5352**	**1563**
		6352	**1252**
	National	**DM54S572**	**1268**
HM7642	**National**	**DM74S572**	**1268**
	NEC Micro	**μPB406**	**1470**
	Signetics	82S136	
HM7643	Intel	3625	
	MMI	**5353**	**1563**
		6353	**1252**
	National	**DM54S573**	**1268**
		DM74S573	**1268**
	NEC Micro	**μPB426**	**1470**
	Signetics	82S137	
HPROM0512	TI	SN54186	
		SN74186	
HPROM1024	Intel	3621	
	MMI	**5301**	**1248**
		6301	**1252**
	Signetics	N82S129	
	TI	SN54S287	
		SN74S287	
HPROM1024A	Fairchild	93416	
	Intel	M3601	
		3601	
	Intersil	IM5603	
	MMI	**5300**	**1248**
		6300	**1252**
	NEC Micro	**μPB403**	**1462**
	Signetics	N82S126	
	TI	SN54S387	
		SN74S387	
♦HPROM2048	**Fairchild**	**93446**	**1151**
	Intersil	IM5624	
	Signetics	N82S131	
HPROM2048A	AMD	AM27S08	
	Fairchild	**93436**	**1151**
	Signetics	N82S130	
HPROM8256	Intersil	IM5600	
	MMI	**5330**	**1248**
		6330	**1252**
	National	DM7577	
		DM8577	
	Signetics	N82S23	
	TI	SN54S188	
		SN74S188	
		SN74188	
HROM1024	TI	SN74187	

Hitachi America, Ltd.

Manufacturer Device	Replacement Source	Device	IC Master Page
HA1137	Sanyo	LA7230	
HA1197	Sanyo	LA1240	
HD10101	Fairchild	F10101	
	Motorola	MC10101	
	NEC America	μPB10101	
	Plessey	SP10101	
	Signetics	10101	
HD10102	Fairchild	F10102	
	Motorola	MC10102	
	NEC America	μPB10102	
	Plessey	SP10102	
	Signetics	10102	
HD10104	Fairchild	F10104	
	Motorola	MC10104	
	Plessey	SP10104	
	Signetics	10104	
HD10105	Fairchild	F10105	
	Motorola	MC10105	
	National	DM10105	
	NEC America	μPB10105	
	Plessey	SP10105	
	Signetics	10105	
HD10106	Fairchild	F10106	
	Motorola	MC10106	
	National	DM10106	
	NEC America	μPB10106	
	Plessey	SP10106	
	Signetics	10106	
HD10107	Fairchild	F10107	
	Motorola	MC10107	
	NEC America	μPB10107	
	Plessey	SP10107	
	Signetics	10107	
HD10109	Fairchild	F10109	
	Motorola	MC10109	
	National	DM10109	
	NEC America	μPB10109	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Hitachi America, Ltd. (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
HD10109	Plessey	SP10109	
	Signetics	10109	
HD10110	Fairchild	F10110	
	Motorola	MC10110	
	NEC America	μPB10110	
	Plessey	SP10110	
	Signetics	10110	
HD10111	Fairchild	F10111	
	Motorola	MC10111	
	National	DM10111	
	NEC America	μPB10111	
	Plessey	SP10111	
	Signetics	10111	
HD10116	Fairchild	F10116	
	Motorola	MC10116	
	National	DM10116	
	Plessey	SP10116	
	Signetics	10116	
HD10117	Fairchild	F10117	
	Motorola	MC10117	
	National	DM10117	
	NEC America	μPB10117	
	Plessey	SP10117	
	Signetics	10117	
HD10118	Fairchild	F10118	
	Motorola	MC10118	
	National	DM10118	
	NEC America	μPB10118	
	Plessey	SP10118	
	Signetics	10118	
HD10119	Fairchild	F10119	
	Motorola	MC10119	
	National	DM10119	
	Plessey	SP10119	
	Signetics	10119	
HD10121	Fairchild	F10121	
	Motorola	MC10121	
	National	DM10121	
	Plessey	SP10121	
	Signetics	10121	
HD10124	Fairchild	F10124	
	Motorola	MC10124	
	National	DM10124	
	NEC America	μPB10124	
	Plessey	SP10124	
	Signetics	10124	
HD10125	Fairchild	F10125	
	Motorola	MC10125	
	Plessey	SP10125	
	Signetics	10125	
HD10130	Fairchild	F10130	
	Motorola	MC10130	
	Plessey	SP10130	
	Signetics	10130	
HD10131	Fairchild	F10131	
	Motorola	MC10131	
	NEC America	μPB10131	
	Plessey	SP10131	
	Signetics	10131	
HD10132	Fairchild	F10132	
	Motorola	MC10132	
	Signetics	10132	
HD10133	Fairchild	F10133	
	Motorola	MC10133	
	NEC America	μPB10133	
	Plessey	SP10133	
	Signetics	10133	
HD10134	Fairchild	F10134	
	Motorola	MC10134	
	Plessey	SP10134	
	Signetics	10134	
HD10136	Fairchild	F10136	
	Motorola	MC10136	
	Plessey	SP10136	
	Signetics	10136	
HD10145	Fairchild	F10145	
	Motorola	MC10145	
	Plessey	SP10145	
	Signetics	10145	
HD10148	NEC America	μPB10148	
	Plessey	SP10148	
	Signetics	10148	
	TI	SN10148	
HD10160	Fairchild	F10160	
	Motorola	MC10160	
	Plessey	SP10160	
	Signetics	10160	
HD10161	Fairchild	F10161	
	Motorola	MC10161	
	NEC America	μPB10161	
	Plessey	SP10161	
	Signetics	10161	
HD10162	Fairchild	F10162	
	Motorola	MC10162	
	NEC America	μPB10162	
	Plessey	SP10162	
	Signetics	10162	
HD10164	Fairchild	F10164	
	Motorola	MC10164	
	NEC America	μPB10164	
	Plessey	SP10164	
	Signetics	10164	
	TI	SN10164	
HD10165	Fairchild	F10165	
	Motorola	MC10165	
	Plessey	SP10165	
	Signetics	10165	
HD10174	Fairchild	F10174	
	Motorola	MC10174	
	NEC America	μPB10174	
	Plessey	SP10174	
	Signetics	10174	
	TI	SN10174	
HD10175	Fairchild	F10175	
	Motorola	MC10175	
	Plessey	SP10175	
	Signetics	10175	
HD10179	Fairchild	F10179	
	Motorola	MC10179	
	Plessey	SP10179	
	Signetics	10179	
HD10180	Fairchild	F10180	
	Motorola	MC10180	
	NEC America	μPB10180	
	Plessey	SP10180	
	Signetics	10180	
HD10181	Fairchild	F10181	
	Motorola	MC10181	
	NEC America	μPB10181	
	Plessey	SP10181	
	Signetics	10181	
HD74S00	Fairchild	74S00	
	Hitachi	HD74S00	
	Mitsubishi	M5S000	
	National	DM74S00	
	Signetics	74S00	
	TI	SN74S00	
HD74S03	Fairchild	74S03	
	Mitsubishi	M5S003	
	National	DM74S03	
	Signetics	74S03	
	TI	SN74S03	
HD74S04	Fairchild	74S04	
	Mitsubishi	M5S004	
	National	DM74S04	
	Signetics	74S04	
	TI	SN74S04	
HD74S05	Fairchild	74S05	
	Mitsubishi	M5S005	
	National	DM74S05	
	Signetics	74S05	
	TI	SN74S05	
HD74S10	Fairchild	74S10	
	Mitsubishi	M5S010	
	National	DM74S10	
	Signetics	74S10	
	TI	SN74S10	
HD74S11	Fairchild	74S11	
	Mitsubishi	M5S011	
	National	DM74S11	
	Signetics	74S11	
	TI	SN74S11	
HD74S112	Fairchild	74S112	
	Mitsubishi	M5S112	
	Motorola	SN74S112	
	National	DM74S112	
	Signetics	74S112	
	TI	SN74S112	
HD74S113	Fairchild	74S113	
HD74S113	Mitsubishi	M5S113	
	Motorola	SN74S113	
	National	DM74S113	
	Signetics	74S113	
	TI	SN74S113	
HD74S114	Fairchild	74S114	
	Mitsubishi	M5S114	
	National	DM74S114	
	Signetics	74S114	
	TI	SN74S114	
HD74S133	Fairchild	74S133	
	Mitsubishi	M5S133	
	National	DM74S133	
	Signetics	74S133	
	TI	SN74S133	
HD74S134	Fairchild	74S134	
	National	DM74S134	
	Signetics	74S134	
	TI	SN74S134	
HD74S135	Fairchild	74S135	
	National	DM74S135	
	Signetics	74S135	
	TI	SN74S135	
HD74S140	Fairchild	74S140	
	National	DM74S140	
	Signetics	74S140	
	TI	SN74S140	
HD74S15	Fairchild	74S15	
	Mitsubishi	M5S015	
	National	DM74S15	
	Signetics	74S15	
	TI	SN74S15	
HD74S151	AMD	SN74S151	
	Fairchild	74S151	
	Mitsubishi	M5S151	
	National	DM74S151	
	Signetics	74S151	
	TI	SN74S151	
HD74S174	AMD	SN74S174	
	Fairchild	74S174	
	Mitsubishi	M5S174	
	National	DM74S174	
	Signetics	74S174	
	TI	SN74S174	
HD74S175	AMD	SN74S175	
	Fairchild	74S175	
	Mitsubishi	M5S175	
	National	DM74S175	
	Signetics	74S175	
	TI	SN74S175	
HD74S181	AMD	SN74S181	
	Fairchild	74S181	
	Mitsubishi	M5S181	
	Signetics	74S181	
	TI	SN74S181	
HD74S20	Fairchild	74S20	
	Mitsubishi	M5S020	
	National	DM74S20	
	Signetics	74S20	
	TI	SN74S20	
HD74S22	Fairchild	74S22	
	Mitsubishi	M5S22	
	National	DM74S22	
	Signetics	74S22	
	TI	SN74S22	
HD74S251	AMD	SN74S251	
	Fairchild	74S251	
	Mitsubishi	M5S251	
	National	DM74S251	
	Signetics	74S251	
	TI	SN74S251	
HD74S40	Fairchild	74S40	
	Mitsubishi	M5S040	
	National	DM74S40	
	Signetics	74S40	
	TI	SN74S40	
HD74S64	Fairchild	74S64	
	National	DM74S64	
	Signetics	74S64	
	TI	SN74S64	
HD74S65	Fairchild	74S65	
	National	DM74S65	
	Signetics	74S65	
	TI	SN74S65	
HD74S74	Fairchild	74S74	
	Mitsubishi	M5S074	
HD74S74	TI	SN74S74	
HD74S86	Fairchild	74S86	
	National	DM74S86	
	Signetics	74S86	
	TI	SN74S86	
HD7400	Fairchild	7400	
	ITT	ITT7400	
	Mitsubishi	M53200	
	Motorola	MC7400	
	National	DM7400	
	NEC America	μPB7400	
	Raytheon	7400	
	Signetics	7400	
	TI	SN7400	
	Toshiba	TC7400	
	TRW	7400	
HD7402	Fairchild	7402	
	ITT	ITT7402	
	Mitsubishi	M53202	
	Motorola	MC7402	
	National	DM7402	
	NEC America	μPB7402	
	Signetics	7402	
	TI	SN7402	
	TRW	7402	
HD7403	Fairchild	7403	
	ITT	ITT7403	
	Mitsubishi	M53203	
	Motorola	MC7403	
	National	DM7403	
	Raytheon	7403	
	Signetics	7403	
	TI	SN7403	
	TRW	7403	
HD7404	Fairchild	7404	
	ITT	ITT7404	
	Mitsubishi	M53204	
	Motorola	MC7404	
	National	DM7404	
	NEC America	μPB7404	
	Raytheon	7404	
	Signetics	7404	
	TI	SN7404	
	Toshiba	TC7404	
	TRW	7404	
HD7405	Fairchild	7405	
	ITT	ITT7405	
	Mitsubishi	M53205	
	Motorola	MC7405	
	National	DM7405	
	NEC America	μPB7405	
	Raytheon	7405	
	Signetics	7405	
	TI	SN7405	
	TRW	7405	
HD7406	Fairchild	7406	
	ITT	ITT7406	
	Mitsubishi	M53206	
	Motorola	MC7406	
	National	DM7406	
	Signetics	7406	
	TI	SN7406	
	TRW	7406	
HD7407	Fairchild	7407	
	ITT	ITT7407	
	Mitsubishi	M53207	
	Motorola	MC7407	
	National	DM7407	
	Signetics	7407	
	TI	SN7407	
	TRW	7407	
HD7409	Fairchild	7409	
	ITT	ITT7409	
	Mitsubishi	M53209	
	Motorola	MC7409	
	National	DM7409	
	Raytheon	7409	
	Signetics	7409	
	TI	SN7409	
	TRW	7409	
HD7410	Fairchild	7410	
	ITT	ITT7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
	National	DM7410	
	NEC America	μPB7410	

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The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
HD7410	Raytheon	7410	
	Signetics	7410	
	TI	SN7410	
		SN7427	
	Toshiba	TC7410	
	TRW	7410	
HD74107	Fairchild	74107	
	ITT	ITT74107	
	Mitsubishi	M53307	
	Motorola	MC74107	
	National	DM74107	
	NEC America	μPB74107	
	Signetics	74107	
	TI	SN74107	
HD7411	Fairchild	7411	
	ITT	ITT7411	
	National	DM7411	
	Raytheon	7411	
	Signetics	7411	
HD7412	Fairchild	7412	
	ITT	ITT7412	
	Raytheon	7412	
	Signetics	7412	
	TI	SN7412	
	TRW	7412	
HD74121	Fairchild	74121	
	ITT	ITT74121	
	Mitsubishi	M53321	
	Motorola	MC74121	
	National	DM74121	
	Signetics	74121	
	TI	SN74121	
	TRW	74121	
HD74125	Fairchild	74125	
	Mitsubishi	M53325	
	National	DM74125	
	Signetics	74125	
	TI	SN74125	
HD74126	Fairchild	74126	
	Mitsubishi	M53326	
	National	DM74126	
	Signetics	74126	
	TI	SN74126	
HD74132	Fairchild	74132	
	Mitsubishi	M53332	
	Motorola	MC74132	
	National	DM74132	
	Signetics	74132	
	TI	SN74132	
HD74136	Motorola	MC74136	
	Raytheon	74136	
	TI	SN74136	
	TRW	74136	
HD7414	Fairchild	7414	
	Mitsubishi	M53214	
	Motorola	MC7414	
	National	DM7414	
	Signetics	7414	
	TI	SN7414	
HD74147	Mitsubishi	M53347	
	National	DM74147	
	NEC America	μPB74147	
	Signetics	74147	
	TI	SN74147	
HD74148	Mitsubishi	M53348	
	National	DM74148	
	NEC America	μPB74148	
	Signetics	74148	
	TI	SN74148	
HD74150	Fairchild	74150	
	Mitsubishi	M53350	
	Motorola	MC74150	
	National	DM74150	
	NEC America	μPB74150	
	Raytheon	74150	
	Signetics	74150	
	TI	SN74150	
	TRW	74150	
HD74151	Fairchild	74151	
	ITT	ITT74151	
	Mitsubishi	M53351	
	Motorola	MC74151	
	National	DM74151	
HD74151	NEC America	μPB74151	
	Raytheon	74151	
	Signetics	74151	
	TI	SN74151	
	TRW	74151	
HD74156	Fairchild	74156	
	ITT	ITT74156	
	Mitsubishi	M53356	
	Motorola	MC74156	
	National	DM74156	
	NEC America	μPB74156	
	Raytheon	74156	
	Signetics	74156	
	TI	SN74156	
	TRW	74156	
HD74157	AMD	SN74157	
	Fairchild	74157	
	ITT	ITT74157	
	Mitsubishi	M53357	
	Motorola	MC74157	
	National	DM74157	
	NEC America	μPB74157	
	Raytheon	74157	
	Signetics	74157	
	TI	SN74157	
HD7416	Fairchild	7416	
	ITT	ITT7416	
	Mitsubishi	M53216	
	Motorola	MC7416	
	National	DM7416	
	Signetics	7416	
	TI	SN7416	
	TRW	7416	
HD74160	AMD	SN74160	
	Fairchild	74160	
	ITT	ITT74160	
	Mitsubishi	M53360	
	Motorola	MC74160	
	National	DM74160	
	Raytheon	74160	
	Signetics	74160	
	TI	SN74160	
	TRW	74160	
HD74161	AMD	SN74161	
	Fairchild	74161	
	ITT	ITT74161	
	Mitsubishi	M53361	
	Motorola	MC74161	
	National	DM74161	
	NEC America	μPB74161	
	Raytheon	74161	
	Signetics	74161	
	TI	SN74161	
	TRW	74161	
HD74162	AMD	SN74162	
	Fairchild	74162	
	ITT	ITT74162	
	Mitsubishi	M53362	
	Motorola	MC74162	
	National	DM74162	
	Raytheon	74162	
	Signetics	74162	
	TI	SN74162	
	TRW	74162	
HD74163	AMD	SN74163	
	Fairchild	74163	
	ITT	ITT74163	
	Mitsubishi	M53363	
	Motorola	MC74163	
	National	DM74163	
	Raytheon	74163	
	Signetics	74163	
	TI	SN74163	
	TRW	74163	
HD74164	AMD	74164	
	Fairchild	74164	
	ITT	ITT74164	
	Mitsubishi	M53364	
	National	DM74164	
	NEC America	μPB74164	
	Raytheon	74164	
	Signetics	74164	
	TI	SN74164	
HD74166	Fairchild	74166	
	Mitsubishi	M53366	
	National	DM74166	
HD74166	Raytheon	74166	
	Signetics	74166	
	TI	SN74166	
HD7417	Fairchild	7417	
	ITT	ITT7417	
	Mitsubishi	M53217	
	Motorola	MC7417	
	National	DM7417	
	Signetics	7417	
	TI	SN7417	
	TRW	7417	
HD74174	AMD	SN74174	
	Fairchild	74174	
	Mitsubishi	M53374	
	Motorola	MC74174	
	National	DM74174	
	Raytheon	74174	
	Signetics	74174	
	TI	SN74174	
HD74175	AMD	SN74175	
	Fairchild	74175	
	Mitsubishi	M53375	
	Motorola	MC74175	
	National	DM74175	
	NEC America	μPB74175	
	Raytheon	74175	
	Signetics	74175	
	TI	SN74175	
HD74180	Fairchild	74180	
	ITT	ITT74180	
	Mitsubishi	M53380	
	Motorola	MC74180	
	National	DM74180	
	NEC America	μPB74180	
	Raytheon	74180	
	Signetics	74180	
	TI	SN74180	
	TRW	74180	
HD74190	Fairchild	74190	
	ITT	ITT74190	
	Mitsubishi	M53390	
	Motorola	MC74190	
	National	DM74190	
	Raytheon	74190	
	Signetics	74190	
	TI	SN74190	
HD74191	Fairchild	74191	
	ITT	ITT74191	
	Mitsubishi	M53391	
	Motorola	MC74191	
	National	DM74191	
	Raytheon	74191	
	Signetics	74191	
	TI	SN74191	
HD74194	AMD	SN74194	
	Fairchild	74194	
	ITT	ITT74194	
	Motorola	MC74194	
	National	DM74194	
	Signetics	74194	
	TI	SN74194	
HD74198	Fairchild	74198	
	Mitsubishi	M53398	
	National	DM74198	
	NEC America	μPB74198	
	Raytheon	74198	
	Signetics	74198	
	TI	SN74198	
HD7420	Fairchild	7420	
	ITT	ITT7420	
	Mitsubishi	M53220	
	Motorola	MC7420	
	National	DM7420	
	NEC America	μPB7420	
	Raytheon	7420	
	Signetics	7420	
	TI	SN7420	
	Toshiba	TC7420	
	TRW	7420	
HD7422	Fairchild	7422	
	Raytheon	7422	
	TI	SN7422	
HD7426	Fairchild	7426	
	ITT	ITT7426	
	Motorola	MC7426	
	National	DM7426	
HD7426	Signetics	7426	
	TI	SN7426	
	TRW	7426	
HD7427	Fairchild	7427	
	Mitsubishi	M53227	
	Motorola	MC7427	
	National	DM7427	
	Signetics	7427	
HD7430	Fairchild	7430	
	ITT	ITT7430	
	Mitsubishi	M53230	
	Motorola	MC7430	
	National	DM7430	
	NEC America	μPB7430	
	Signetics	7430	
	TI	SN7430	
	TRW	7430	
HD7432	Fairchild	7432	
	ITT	ITT7432	
	National	DM7432	
	Signetics	7432	
	TI	SN7432	
HD7440	Fairchild	7440	
	ITT	ITT7440	
	Mitsubishi	M53240	
	Motorola	MC7440	
	National	DM7440	
	NEC America	μPB7440	
	Signetics	7440	
	TI	SN7440	
	TRW	7440	
HD7442	Fairchild	7442	
	ITT	ITT7442	
	Mitsubishi	M53242	
	Motorola	MC7442	
	National	DM7442	
	NEC America	μPB7442	
	Raytheon	7442	
	Signetics	7442	
	TI	SN7442	
HD7443	Fairchild	7443	
	ITT	ITT7443	
	Mitsubishi	M53243	
	Motorola	MC7443	
	Raytheon	7443	
	Signetics	7443	
	TI	SN7443	
HD7444	Fairchild	7444	
	ITT	ITT7444	
	Mitsubishi	M53244	
	Motorola	MC7444	
	Raytheon	7444	
	Signetics	7444	
	TI	SN7444	
HD7450	Fairchild	7450	
	ITT	ITT7450	
	Mitsubishi	M53250	
	Motorola	MC7450	
	National	DM7450	
	NEC America	μPB7450	
	Signetics	7450	
	TI	SN7450	
	TRW	7450	
HD7451	Fairchild	7451	
	ITT	ITT7451	
	Motorola	MC7451	
	National	DM7451	
	NEC America	μPB7451	
	Signetics	7451	
	TI	SN7451	
	TRW	7451	
HD7453	Fairchild	7453	
	ITT	ITT7453	
	Mitsubishi	M53253	
	Motorola	MC7453	
	National	DM7453	
	NEC America	μPB7453	
	Signetics	7453	
	TI	SN7453	
	TRW	7453	
HD7454	Fairchild	7454	
	ITT	ITT7454	
	Motorola	MC7454	
	National	DM7454	
	NEC America	μPB7454	
	Signetics	7454	

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Manufacturer Device	Replacement Source	Device	IC Master Page
HD7454	TI	SN7454	
	TRW	7454	
HD7460	Fairchild	7460	
	Mitsubishi	M53260	
	Motorola	MC7460	
	National	DM7460	
	NEC America	μPB7460	
	Signetics	7460	
	TI	SN7460	
	TRW	7460	
HD7472	Fairchild	7472	
	ITT	ITT7472	
	Mitsubishi	M53272	
	Motorola	MC7472	
	National	DM7472	
	Signetics	7472	
	TI	SN7472	
	TRW	7472	
HD7474	Fairchild	7474	
	ITT	ITT7474	
	Mitsubishi	M53274	
	Motorola	MC7474	
	National	DM7474	
	NEC America	μPB7474	
	Raytheon	7474	
	Signetics	7474	
	TI	SN7474	
	TRW	7474	
HD7475	Fairchild	7475	
	ITT	ITT7475	
	Mitsubishi	M53275	
	Motorola	MC7475	
	National	DM7475	
	Signetics	7475	
	TI	SN7475	
	TRW	7475	
HD7485	Fairchild	7485	
	Mitsubishi	M53285	
	Motorola	MC7485	
	National	DM7485	
	NEC America	μPB7485	
	Signetics	7485	
	TI	SN7485	
	TRW	7485	
HD7486	Fairchild	7486	
	ITT	ITT7486	
	Mitsubishi	M53286	
	Motorola	MC7486	
	National	DM7486	
	NEC America	μPB7486	
	Raytheon	7486	
	Signetics	7486	
	TI	SN7486	
	TRW	7486	
HD7490	Fairchild	7490	
	ITT	ITT7490	
	Mitsubishi	M53290	
	Motorola	MC7490	
	National	DM7490	
	Signetics	7490	
	TI	SN7490	
	TRW	7490	
HD7492	Fairchild	7492	
	ITT	ITT7492	
	Mitsubishi	M53292	
	Motorola	MC7492	
	National	DM7492	
	Signetics	7492	
	TI	SN7492	
	TRW	7492	
HD7493	Fairchild	7493	
	ITT	ITT7493	
	Mitsubishi	M53293	
	Motorola	MC7493	
	National	DM7493	
	Signetics	7493	
	TI	SN7493	
	TRW	7493	
HD7496	Fairchild	7496	
	ITT	ITT7496	
	Mitsubishi	M53296	
	Motorola	MC7496	
	National	DM7496	
HD7496	Signetics	7496	
	TI	SN7496	
	TRW	7496	
HM2114	TI	TMS4045	
M6800	**AMI**	**S6800**	**1538,1548**
	Fairchild	F6800	
	Motorola	MC6800	

Hughes Aircraft, Solid State Products

HCMP1802	RCA	CDP1802	
HCMP1824	RCA	CDP1824	
HCMP1831	RCA	CDP1831	
HCMP1832	RCA	CDP1832	
HCMP1833	RCA	CDP1833	
HCMP1834	RCA	CDP1834	
HCMP1852	RCA	CDP1852	
HCMP1853	RCA	CDP1853	
HCMP1854	RCA	CDP1854	
HCMP1856	RCA	CDP1856	
HCMP1857	RCA	CDP1857	
HCMP1858	RCA	CDP1858	
HCMP1859	RCA	CDP1859	

Hybrid Systems

ADC586-10	Teledyne S	8701	
ADC586-12	Teledyne S	8702	
ADC586-8	Teledyne S	8700	

Intel

1101	AMD	1101	
	Intersil	IM7501	
		IM7511	
	Mostek	MK4007	
	National	MM1101	
1103	AMI	S146	
	Fairchild	1103	
	Hitachi	HM3503	
	Nortec	1103	
	Rockwell	1103	
	Signetics	1103	
	Synertek	SY1103	
1103A	AMI	S1103A	
	Rockwell	1103A	
	Synertek	1103A	
♦1301	AMI	S8773	
1302	GI	R05-1302	
1402	AMD	1402	
	AMI	S2502A	
	National	MM1402	
	Nortec	1402	
	SGS	M141	
	Signetics	2502	
	Synertek	SY1402	
1403	AMD	1403	
	National	MM1403	
	Nortec	1403	
	SGS	M136	
	Signetics	2503	
	Synertek	SY1403	
1404	AMD	1404	
	National	MM1404	
	Nortec	1404	
	SGS	M130	
	Signetics	2504	
	Synertek	SY1404	
1405	AMD	1405	
	Signetics	2505	
1406	AMD	1406	
1407	AMD	1407	
1504	AMI	S1685	
1506	AMD	1506	
1507	AMD	1507	
♦1702	AMD	1702	
	Mostek	MK3702	
	National	**MM1702**	**1365**
	Signetics	1702	
1702A	AMD	1702	
	Mostek	MK3702	
	National	**MM1702**	**1365**
1702A	Signetics	1702	
2101	AMD	2101	
	EA	EA2101	
	Fujitsu	MB8101	
	Harris	**HM6501**	**1174**
	Hitachi	HM2101	
	National	MM2101	
	NEC Micro	μPD2101	
	Signetics	2101	
	Synertek	SY2101	
	TI	TMS2101	
		TMS4039	
2102	AMD	2102	
		9102	
	EA	EA2102	
	Fairchild	21L02	
		2102	
	Fujitsu	MB8102	
	Intersil	IM7552	
	Mostek	MK4102	
	National	**MM2102**	**1300**
	NEC Micro	μPD2102	
	SGS	M330	
	Signetics	21F02	
		2102	
	Synertek	SY2102	
		SY5102	
	TI	TMS2102	
		TMS4033	
		TMS4034	
		TMS4035	
2104	Fairchild	4096	
	Mostek	MK4027	
		MK4096	
	NEC Micro	**μPD414**	**1395**
2104A	**Fairchild**	**M4027**	**1118**
	Signetics	4027	
2107	**NEC Micro**	**μPD411**	**1375**
2107A	TI	TMS4030	
		TMS4060	
2107B	Fujitsu	MB8107	
	Intersil	7280	
	National	**MM5280**	**1336**
	NEC Micro	**μPD411**	**1375**
	TI	TMS4060	
2111	AMD	2111	
	EA	EA2111	
	Fujitsu	MB8111	
	National	MM2111	
	NEC Micro	μPD2111	
	Signetics	2111	
	Synertek	SY2111	
	TI	TMS2111	
		TMS4042	
2112	AMD	2112	
	EA	EA2112	
	Fujitsu	MB8112	
	National	MM2112	
	Signetics	2112	
	Synertek	SY2112	
	TI	TMS2112	
		TMS4043	
2114	**AMI**	**S4016**	**1035**
	EMM/Semi	**2114**	**1078**
	Fairchild	2114	
	Fujitsu	MB8114	
	Harris	**HM6514**	**1178**
	Motorola	MCM2114	
	NEC Micro	**μPD2114**	**1489**
	Synertek	SY2114	
	TI	TMS4045	
2115	**AMI**	**S4015**	**1032**
	Fujitsu	MB8115	
	NEC Micro	**μPD2114**	**1489**
2116	**Fairchild**	**F16K**	**1110**
	Intersil	7116	
	Mostek	MK4116	
	Motorola	MCM4116	
	NEC Micro	**μPD416**	**1402**
	Signetics	2690	
	TI	TMS4116	
2117	Mostek	MK4116	
	Zilog	Z6116	
2125	**AMI**	**S4025**	**1032**
	Fujitsu	MB8125	
	Harris	**HM6508**	**1180**
2125	NEC Micro	μPD2125	
2146	AMI	S146	
2147	AMI	S4019	
2308	EA	EA2308	
	Fairchild	3508	
	Fujitsu	MB8308	
	Mostek	MK30000	
	NEC Micro	**μPD2308**	**1478**
2316	EA	2316	
	EMM/Semi	RO3-8316	
	GI	RO3-8316	
	Mostek	MK31000	
		MK34000	
	Motorola	MCM68316	
	NEC Micro	**μPD2316**	**1481**
2401	Synertek	SY2401	
2405	AMI	S1685	
	Synertek	SY2405	
2616	**NEC Micro**	**μPD2316**	**1481**
2708	AMD	2708	
	EA	EA2708	
	Fairchild	**2708**	**1093**
	Fujitsu	MB8518	
	Mostek	MK2708	
	Motorola	MCM2708	
		MC27A08	
		MC2708	
	National	MM2708	
	TI	TMS2708	
3002	**Signetics**	**N3002**	**1868**
3101	AMD	AM27S02	
		3101	
	MMI	5560	
		6560	
	National	MM54S289	
		MM74S289	
	NEC Micro	μPB2089	
		μPB2289	
	Signetics	N82S25	
		3101	
	TI	~~SN54S289~~	
		SN74S289	
3102	Fairchild	93400	
3104	Fairchild	93402	
3106	Fairchild	93421	
	MMI	6531	
	National	MM74S200	
	NEC Micro	μPB2200	
	Raytheon	RC5340	
		RM5340	
	Signetics	82S16	
	TI	SN54S200A	
		SN54S201	
		SN74S200A	
		SN74S201	
3107	Fairchild	93411	
	MMI	5530	
		6530	
	National	MM74S206	
	NEC Micro	μPB2206	
	Raytheon	RC5330	
		RM5330	
	Signetics	S82S17	
		74S01	
		82S17	
	TI	SN54S300	
		SN54S301	
		SN74S300	
		SN74S301	
3110	TI	SN74S214	
		SN74S314	
3202	Fairchild	93401	
3207A	NEC Micro	μPD246	
	Signetics	3207	
3212	TI	SN54S412	
		SN74S412	
3232	Motorola	MC3232	
3245	Motorola	MC3245	
♦3301	AMD	SN74186	
	Intersil	IM5603	
	MMI	H6200	
		5200	**1252**
	Signetics	82S226	
	TI	SN54187	
		SN74187	
♦3304	**MMI**	**6340**	**1252**

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Intel (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
♦3304	Signetics	82S215	
		8205	
3601	**Fairchild**	**93417**	**1151**
	Harris	**HM7610**	**1192**
		HM7610A	**1200**
		HPROM1024A	
	Intersil	IM5603	
	MMI	**5300**	**1248**
		6300	**1252**
	NEC Micro	**μPB403**	**1462**
	Signetics	N82S126	
	TI	SN54S387	
		SN74S387	
3601-1	**National**	**DM54S387**	**1264**
		DM74S387	**1264**
3602	**Fairchild**	**93436**	**1151**
	Harris	**HM7620**	**1192**
		HM7620A	**1202**
	MMI	**5305**	**1248**
		6305	**1252**
	National	DM54S570	
		DM74S570	**1266**
	Signetics	82S130	
	TI	SN54S475	
		SN74S475	
3604	**Harris**	**HM7640**	**1192**
		HM7640A	**1204**
	MMI	**5340**	**1563**
		6340	**1252**
	National	**DM77S295**	**1270**
		DM87S295	**1270**
		SN54S475	
		SN74S475	
	NEC Micro	μPB405	
	Signetics	N82S140	
3605	**Harris**	**HM7642**	**1192**
	MMI	**5352**	**1563**
		6352	**1252**
	National	**DM54S572**	**1268**
		DM74S572	**1268**
	NEC Micro	**μPB406**	**1470**
	Signetics	82S136	
3608	**Harris**	**HM7680**	**1220**
	MMI	6380	
	NEC Micro	**μPB408**	**1491**
	Signetics	N82S280	
3621	**Harris**	**HM7611**	**1192**
		HM7611A	**1200**
	MMI	**5301**	**1248**
		6301	**1252**
	National	**DM54S287**	**1264**
		DM74S287	**1264**
	TI	SN54S287	
		SN74S287	
3622	**Fairchild**	**93446**	**1151**
	Harris	**HM7621**	**1192**
		HM7621A	**1202**
	MMI	**5306**	**1248**
		6306	**1252**
	National	**DM54S571**	**1266**
		DM74S571	**1266**
	Signetics	82S131	
3624	**Harris**	**HM7641**	**1192**
		HM7641A	**1204**
	MMI	**5341**	**1563**
		6341	**1252**
	National	**DM77S296**	**1270**
		DM87S296	**1270**
		SN54S474	
		SN74S474	
	NEC Micro	**μPB425**	**1466**
	Signetics	N82S141	
3625	**Harris**	**HM7643**	**1192**
	MMI	**5353**	**1563**
		6353	**1252**
	National	**DM54S573**	**1268**
		DM74S573	**1268**
	NEC Micro	**μPB426**	**1470**
	Signetics	82S137	
3628	**Harris**	**HM7681**	**1220**
	MMI	6381	
	NEC Micro	**μPB428**	**1491**
	Signetics	N82S181	
4001	**Harris**	**HM7621**	**1192**
		HM7621A	**1202**
	National	INS4001	
4002	National	INS4002	
4003	National	INS4003	
4004	**National**	**INS4004**	**1656**
4008	National	INS4008	
4009	National	INS4009	
4201	**National**	**DP4201**	**465**
4316	**NEC Micro**	**μPD2316A**	**1481**
4702	AMD	4702	
5101	**AMI**	**S5101**	**1041**
		S6831B	**1062,1560**
	Harris	**HM6501**	**1174**
	NEC Micro	**μPD5101**	**1438**
5201	SSS	SCL5424	
5801	SSS	SCL5437	
8035	**NEC Micro**	**μPD8035**	**1849**
8048	AMD	8048	
	NEC Micro	**μPD8048**	**1849**
	Signetics	8048	
8080A	AMD	9080A	
	National	**INS8080A**	**1656,1670**
	NEC Micro	**μPD8080AF**	**1736**
	Signetics	MP8080A	
	TI	TMS8080A	
8085	AMD	8085	
	NEC Micro	**μPD8085**	**1847**
8101	NEC Micro	μPD2101A	
8102	NEC Micro	μP2102A	
8111	NEC Micro	μP2111AL	
8155	**NEC Micro**	**μPD8155**	**1847**
8156	**NEC Micro**	**μPD8156**	**1847**
8212	AMD	8212	
	National	**DP8212**	**469**
	NEC Micro	**μPB8212**	**1804**
	TI	SN54S412	
		SN74S412	
8214	**NEC Micro**	**μPB8214**	**1758**
8216	AMD	8216	
	NEC Micro	**μPB8216**	**1810**
8224	AMD	8224	
	National	**DP8224**	**477**
	NEC Micro	**μPB8224**	**1764**
	TI	SN74LS424	
8226	AMD	8226	
	NEC Micro	**μPB8226**	**1810**
8228	AMD	8228	
	National	**DP8228**	**483**
	NEC Micro	**μPB8228**	**1769**
	TI	SN74S428	
		TIM8228	
8238	AMD	8238	
	National	**DP8238**	**483**
	NEC Micro	**μPB8238**	**1769**
		μPD8238	
	TI	SN74S438	
		TIM8238	
8251	AMD	9551	
	National	DP8251	
	NEC Micro	**μPD8251**	**1814**
8253	**NEC Micro**	**μPD8253**	**1845**
8255	AMD	9555	
	National	DP8255	
	NEC Micro	μPD8225	
		μPD8255	**1830**
8257	AMD	8257	
	NEC Micro	**μPD8257**	**1837**
8259	AMD	8259	
	NEC Micro	**μPD8259**	**1846**
8300	**National**	**DP8300**	**488**
8302	**National**	**DP8302**	**496**
8304	**National**	**DP8304**	**501**
8308	AMD	9208	
	EA	EA8308	
	Mostek	MK30000	
	NEC Micro	**μPD2308**	**1478**
	TI	TMS4700	
8316	**AMI**	**S6831**	**1062,1560**
		86831B	
	EA	EA8316	
	GI	RO3-8316	
	Mostek	MK31000	
		MK34000	
8316	**NEC Micro**	**μPD2316**	**1481**
	Synertek	SY2316	
8316A	AMD	8316A	
	AMI	**S6831A**	**1062,1560**
	EA	EA8316A	
	NEC Micro	μPB2316A	
	Synertek	SY8316A	
8316B	**AMI**	**S6831B**	**1062,1560**
	EA	EA8316B	
	NEC Micro	μPB2316B	
	Synertek	SY8316B	
8355	**NEC Micro**	**μPD8355**	**1848**
8702	AMD	8702	
8708	Mostek	MK2708	
8748	**NEC Micro**	**μPD8748**	**1849**
8755	**NEC Micro**	**μPD8755**	**1848**

Interdesign

Manufacturer Device	Replacement Source	Device	IC Master Page
Monochip A	Exar	XR-A100	
Monochip B	Exar	XR-B100	
Monochip D	Exar	XR-D100	

Intersil

Manufacturer Device	Replacement Source	Device	IC Master Page
AH0126	Siliconix	DG126	
AH0129	Siliconix	DG129	
AH0133	Siliconix	DG133	
AH0134	Siliconix	DG134	
AH0139	Siliconix	DG139	
AH0140	Siliconix	DG140	
AH0141	Siliconix	DG141	
AH0142	Siliconix	DG142	
AH0143	Siliconix	DG143	
AH0144	Siliconix	DG144	
AH0145	Siliconix	DG145	
AH0146	Siliconix	DG146	
AH0151	Siliconix	DG151	
AH0152	Siliconix	DG152	
AH0153	Siliconix	DG153	
AH0154	Siliconix	DG154	
AH0161	Siliconix	DG161	
AH0162	Siliconix	DG162	
AH0163	Siliconix	DG163	
AH0164	Siliconix	DG164	
DG111	Siliconix	DGM111	
DG116	Siliconix	DG116	
DG118	Siliconix	DG172	
DG123	Siliconix	DG123	
DG125	Siliconix	DG125	
DG126	Siliconix	DG126	
DG129	Siliconix	DG129	
DG133	Siliconix	DG133	
DG134	Siliconix	DG134	
DG139	Siliconix	DG139	
DG140	Siliconix	DG140	
DG141	Siliconix	DG141	
DG142	Siliconix	DG142	
DG143	Siliconix	DG143	
DG144	Siliconix	DG144	
DG145	Siliconix	DG145	
DG146	Siliconix	DG146	
DG151	Siliconix	DG151	
DG152	Siliconix	DG152	
DG153	Siliconix	DG153	
DG154	Siliconix	DG154	
DG161	Siliconix	DG161	
DG162	Siliconix	DG162	
DG163	Siliconix	DG163	
DG164	Siliconix	DG164	
DG182	Siliconix	DG182	
DG185	Siliconix	DG185	
DG188	Siliconix	DG188	
DG191	Siliconix	DG191	
DG426	Siliconix	DG126	
DG464	Siliconix	DG164	
D123	Siliconix	D123	
D125	Siliconix	D125	
G115	Siliconix	G115	
G116	Siliconix	G116	
G117	Siliconix	G117	
G118	Siliconix	G118	
G119	Siliconix	G119	
G123	Siliconix	G123	
G125	Siliconix	G125	
G126	Siliconix	G126	
G127	Siliconix	G127	
G128	Siliconix	G128	
G129	Siliconix	G129	
G130	Siliconix	G130	
G131	Siliconix	G131	
G132	Siliconix	G132	
HA2505	Datel	AM-450-2	
HA2525	Datel	AM-450-2	
IH5009	AMI	MX52	
	National	AH5009	
IH5010	AMI	MX52	
	National	AH5010	
IH5040	**Harris**	**HI5040**	**410**
IH5041	**Harris**	**HI5041**	**410**
IH5042	**Harris**	**HI5042**	**410**
	Siliconix	DG188	
IH5043	Siliconix	DG191	
IH5044	**Harris**	**HI5044**	**410**
IH5045	**Harris**	**HI5045**	**410**
	Siliconix	DG185	
IH5046	**Harris**	**HI5046**	**410**
IH5047	**Harris**	**HI5047**	**410**
IH5048	Siliconix	DG181	
IH5049	**Harris**	**HI5049**	**410**
	Siliconix	DG184	
IH5050	**Harris**	**HI5050**	**410**
	Siliconix	DG187	
IH5051	**Harris**	**HI5051**	**410**
	Siliconix	DG190	
IH5060	**Harris**	**HI506**	**418**
IH5070	AD	AD7507	
	Harris	**HI507**	**418**
	Siliconix	DG507	
IM55S08	TI	SN54S314	
		SN74S314	
IM55S18	TI	SN54S214	
		SN74S214	
		SN74S314	
IM5501	AMD	IM5501	
	MMI	5560	
		6560	
	NEC Micro	μPB2089	
	Signetics	82S25	
	TI	SN54S289	
		SN74S289	
IM5502	TI	SN54S81A	
		SN5481A	
IM5503	MMI	6531	
	Signetics	N82S17	
		74S301	
	TI	SN54S300	
		SN54S301	
		SN74S300	
		SN74S301	
IM5508	**Fairchild**	**93415**	**1137**
	Signetics	N82S10	
	TI	SN54214	
		SN54314	
		SN74S314	
		SN7481A	
IM5512	TI	SN5481A	
IM5523	Fairchild	93421	
	MMI	5531	
		6531	
	National	MM74S200	
	NEC Micro	μPB2200	
	Raytheon	RC5340	
		RC5540	
		RM5340	
	Signetics	N82S16	
		S82S16	
	TI	SN54S201	
		SN54200A	
		SN74S201	
		SN74200A	
IM5533	Fairchild	93411	
	MMI	5530	
		6530	
	National	MM74S206	
	NEC Micro	μPB2206	
	Raytheon	RC5330	
		RM5330	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Intersil (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
IM5533	Signetics	N82S17	
	TI	SN54S301	
		SN74S300	
		SN74S301	
IM5543	Fairchild	93421	
	TI	SN54S301	
		SN54S475	
		SN74S301	
		SN74S475	
IM5553	Fairchild	93411	
	TI	SN54S200	
		SN74S200	
IM56S06	Fujitsu	MB7059	
IM56S26	Fujitsu	MB7054	
IM5600	Fujitsu	MB7056	
	Harris	HPROM8256	
	MMI	**5330**	**1248**
		6330	**1252**
	National	DM7577	
		DM8577	
	Signetics	N82S23	
	TI	SN54S188	
		SN74S188	
IM5602	**MMI**	**6340**	**1252**
	TI	SN54S475	
		SN74S475	
IM5603	Fairchild	93416	
	Fujitsu	MB7057	
	Harris	HPROM1024A	
	Intel	M3601	
		3601	
	MMI	**5300**	**1248**
		6300	**1252**
	NEC Micro	**μPB403**	**1462**
	Signetics	82S126	
	TI	SN54S387	
		SN74S387	
IM5604	Fairchild	93436	1151
	Fujitsu	MB7058	
	Harris	**HM7620**	**1192**
		HM7620A	**1202**
	Intel	3602	
	MMI	**5305**	**1248**
		6305	**1252**
	National	DM54S570	
		DM74S570	**1266**
	Signetics	N82S130	
	TI	SN54S270	
		SN74S270	
IM5605	**Harris**	**HM7640**	**1192**
		HM7640A	**1204**
	Intel	3604	
	MMI	**5340**	**1563**
		6340	**1252**
	National	**DM77S295**	**1270**
		DM87S295	**1270**
	NEC Micro	μPB405	
	TI	SN54S475	
		SN74S475	
IM5606	**National**	**DM54S572**	**1268**
		DM74S572	**1268**
	NEC Micro	**μPB406**	**1470**
IM5610	Fujitsu	MB7051	
	Harris	**HM7603**	**1192**
	MMI	**5331**	**1248**
		6331	**1252**
	National	DM7578	
		DM8578	
	Signetics	N82S123	
	TI	SN54S288	
		SN74S288	
IM5623	Fairchild	93426	
	Fujitsu	MB7052	
	Harris	HPROM1024	
	Intel	3621	
	MMI	**5301**	**1248**
		6301	**1252**
	Signetics	N82S129	
	TI	SN54S287	
		SN74S287	
IM5624	**Fairchild**	**93446**	**1151**
	Fujitsu	MB7053	
	Harris	**HM7621**	**1192**
IM5624	**Harris**	**HM7621A**	**1202**
	Intel	3622	
	MMI	**5306**	**1248**
		6306	**1252**
	National	**DM54S571**	**1266**
		DM74S571	**1266**
	Signetics	N82S131	
	TI	SN54S370	
		SN74S370	
IM5625	**Harris**	**HM7641**	**1192**
		HM7641A	**1204**
	Intel	3624	
	MMI	**5341**	**1563**
		6341	**1252**
	National	**DM77S296**	**1270**
		DM87S296	**1270**
	NEC Micro	**μPB425**	**1466**
	TI	SN54S474	
		SN74S474	
IM5626	**National**	**DM54S573**	**1268**
		DM74S573	**1268**
IM6100	**Harris**	**HM6100**	**1631**
IM6100A	**Harris**	**HM6100A**	**1631**
IM6100C	**Harris**	**HM6100C**	**1631**
IM6101	**Harris**	**HD6101**	**1633**
IM6101A	Harris	HD6101A	
IM6101C	Harris	HD6101C	
IM6312	Harris	HM6312	
IM6402	**Harris**	**HD6402**	**1632**
IM6402A	Harris	HD6402A	
IM6402C	Harris	HD6402C	
IM6403A	Harris	HD6403A	
IM6508	**AMI**	**S6508**	**1046**
	Fairchild	F4736	
	Harris	**HM6508**	**1180**
	National	**MM74C929**	**1363**
	NEC Micro	**μPD6508**	**1488**
IM6508C	**Harris**	**HM6508C**	**1180**
IM6518	**Harris**	**HM6518**	**1181**
	National	**MM74C930**	**1363**
IM6522	National	MM74C200	1355
	RCA	CD4061	
IM6551	Fairchild	F4721	
	Harris	**HM6551**	**1175**
	National	**MM74C920**	**1361**
IM6561	**Harris**	**HM6561**	**1182**
IM6900	Harris	HM6900	
IM7001	RCA	MW7001	
IM7027	Mostek	MK4027	
IM7051	AMD	1101	
IM7114	Intel	2114	
	Motorola	MCM2114	
	National	MM2114	
	Signetics	2614	
	TI	TMS4045	
IM7116	Intel	2116	
	Mostek	MK4116	
	Motorola	MCM4116	
	NEC Micro	**μPD416**	**1402**
IM7141	Intel	2141	
	National	**MM5257**	**1319**
	Signetics	2613	
	TI	TMS4044	
IM7210	AMI	S2733	
IM7270	**National**	**MM5270**	**1325**
IM7271	**National**	**MM5271**	**1333**
IM7280	National	MM7280	
	TI	TMS4060	
IM7501	Mostek	MK4007	
IM7511	Mostek	MK4007	
IM7512	Mostek	MK4007	
	Signetics	1101	
IM7552	Mostek	MK4102	
	NEC Micro	**μPD2102AL**	**1429**
	SGS	M330	
	Signetics	2102	
	TI	TMS4033	
		TMS4034	
		TMS4035	
IM7702	Nortec	1402	
	Signetics	2502	
IM7703	Nortec	1403	
	Signetics	2503	
IM7704	Nortec	1404	
	Signetics	2504	
IM7708	Intel	2708	
IM7708	Signetics	2708	
	TI	TMS2708	
IM7712	AMD	AM2806	
	Nortec	2512	
	Signetics	2512	
IM7716	**Fairchild**	**F16K**	**1110**
IM7722	AMD	AM2808	
	Signetics	2525	
IM7780	Mostek	MK1007	
	Signetics	2532	
	TI	TMS3409	
LD110	**Siliconix**	**LD110**	**535**
LD111	**Siliconix**	**LD111**	**535**
LF155	AMD	LF155	
	Fairchild	μAF155	
	Motorola	LF155	
	National	**LF155**	**786**
	PMI	**PM155**	**871**
	Raytheon	LF155	
	Signetics	LF155	
	TI	LF155	
LF156	AMD	LF156	
	Fairchild	μAF156	
	Motorola	LF156	
	National	**LF156**	**786**
	PMI	**PM156**	**877**
	Raytheon	LF156	
	Signetics	LF156	
	TI	LF156	
LF157	AMD	LF157	
	Fairchild	μAF157	
	Motorola	LF157	
	National	**LF157**	**786**
	PMI	**PM157**	**882**
	Raytheon	LF157	
	Signetics	LF157	
	TI	LF157	
LF255	AMD	LF255	
	Fairchild	μAF255	
	Motorola	LF255	
	National	**LF255**	**786**
	PMI	**PM255**	**871**
	Raytheon	LF255	
	Signetics	LF255	
	TI	LF255	
LF256	AMD	LF256	
	Fairchild	μAF256	
	Motorola	LF256	
	National	**LF256**	**786**
	PMI	**PM256**	**877**
	Raytheon	LF256	
	Signetics	LF256	
	TI	LF256	
LF257	AMD	LF257	
	Fairchild	μAF257	
	Motorola	LF257	
	National	**LF257**	**786**
	PMI	**PM257**	**882**
	Raytheon	LF257	
	Signetics	LF257	
	TI	LF257	
LF355	AMD	LF355	
	Fairchild	μAF355	
	Motorola	LF355	
	National	**LF355**	**786**
	PMI	**PM355**	**871**
	Raytheon	LF355	
	Signetics	LF355	
	TI	LF355	
LF356	AMD	LF356	
	Fairchild	μAF356	
	Motorola	LF356	
	National	**LF356**	**786**
	PMI	**PM356**	**877**
	Raytheon	LF356	
	Signetics	LF356	
	TI	LF356	
LF357	AMD	LF357	
	Fairchild	μAF357	
	Motorola	LF357	
	National	**LF357**	**786**
	PMI	**PM357**	**882**
	Raytheon	LF357	
	Signetics	LF357	
	TI	LF357	
LM148	AMD	LM148	
LM148	Exar	XR4741	
	Raytheon	LM148	
LM248	AMD	LM248	
	Exar	XR4741	
	Raytheon	LM248	
LM348	AMD	LM348	
	Raytheon	LM348	
MM452	Siliconix	SI452	
MM455	Siliconix	SI455	
MM552	Siliconix	SI552	
MM555	Siliconix	SI555	
NE555	Exar	XR555	
	RCA	CA555	
NE556	Exar	XR555	
SE555	Exar	XR555M	
	RCA	CA555	
SE556	Exar	XR555M	
SSS1458	Exar	XR1458	
	RCA	CA1458	
	Silicon G	SG1458	
SSS1558	AD	AD101	
	Exar	XR1558	
	National	LM101	
	RCA	CA101	
		CA1558	
		CA748	
	Silicon G	SG1558	
101	Motorola	LM101	
	Silicon G	SG101	
105	Motorola	LM105	
	Silicon G	SG105	
107	Motorola	LM107	
	RCA	CA107	
	Silicon G	SG107	
108	AD	AD108	
	National	LM108	
	Raytheon	LM108	
	RCA	CA108	
	Silicon G	SG108	
111	Motorola	LM111	
	RCA	CA111	
	Silicon G	SG111	
201	AD	AD201	
	Motorola	LM201	
	National	LM201	
	RCA	CA201	
		CA748	
	Silicon G	SG201	
205	Motorola	LM205	
	Silicon G	SG205	
207	Motorola	LM207	
	RCA	CA207	
	Silicon G	SG207	
208	AD	AD208	
	Motorola	LM208	
	National	LM208	
	Raytheon	LM208	
	RCA	CA208	
	Silicon G	SG208	
211	Motorola	LM211	
	RCA	CA211	
	Silicon G	SG211	
2650	Signetics	2650	
301	AD	AD301	
	Motorola	LM301	
	National	LM301	
	Raytheon	LM301	
	RCA	CA301	
	Silicon G	SG301	
305	Motorola	LM305	
	Silicon G	SG305	
307	RCA	CA307	
	Silicon G	SG307	
308	AD	AD308	
	Motorola	LM308	
	National	LM308	
	Raytheon	LM308	
	RCA	CA308	
	Silicon G	SG308	
311	Motorola	LM311	
	RCA	CA311	
	Silicon G	SG311	
4250	National	LM4250	
	Silicon G	SG4250	
5101	**AMI**	**S5101**	**1041**
555	Motorola	MC1455	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Intersil (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
555	National	LM555	
	Raytheon	RC555	
		RM555	
	RCA	CA355	
	Silicon G	SG555	
7114	**NEC Micro**	**μPD2114**	**1489**
7116	TI	TMS4116	
	Zilog	Z6116	
723	Motorola	MC1723	
	National	LM723	
	Raytheon	RC723	
		RM723	
	RCA	CA723	
	Signetics	μA723	
	Silicon G	SG723	
741	AD	AD741	
	Fairchild	μA741	
	Motorola	MC1741	
	National	LM741	
	PMI	**SSS741**	**839**
	Raytheon	RC741	
		RM741	
	RCA	CA741	
	Silicon G	SG741	
747	Motorola	MC1747	
	RCA	CA747	
	Silicon G	SG747	
748	Fairchild	μA748	
	Motorola	MC1748	
	National	LM748	
	Raytheon	RC748	
		RM748	
	RCA	CA748	
	Silicon G	SG748	
8007	AD	AD8007	
8013	AD	AD530	
		AD533	
8021	**Harris**	**HA-2720**	**712**
8038	Exar	XR8038	
8101	RCA	CA748	
8201	RCA	CA748	
8240	Exar	XR2240	

ITT Semiconductors

Manufacturer Device	Replacement Source	Device	IC Master Page
♦ITT1330	Motorola	MC1330	
♦ITT1352	Motorola	MC1352	
ITT1488	Exar	XR1488	
	Signetics	MC1488	
	TI	SN75188	
ITT1489	Signetics	MC1489	
	TI	SN75189	
ITT1489A	Exar	XR1489A	
	Signetics	MC1489A	
	TI	SN75189A	
ITT2001	Sprague	ULN-2001	
ITT2002	Sprague	ULN-2002	
ITT2003	Sprague	ULN-2003	
♦ITT3064	Motorola	MC1364	
♦ITT3065	Motorola	MC1358	
ITT491	TI	SN75491	
ITT492	TI	SN75492	
♦ITT493	TI	SN75493	
♦ITT494	TI	SN75494	
ITT54H00	Fairchild	54H00	
	National	DM54H00	
	Raytheon	54H00	
	Signetics	54H00	
	TI	SN54H00	
ITT54H01	Fairchild	54H01	
	National	DM54H01	
	Raytheon	54H01	
	Signetics	54H01	
	TI	SN54H01	
ITT54H04	Fairchild	54H04	
	National	DM54H04	
	Raytheon	54H04	
	Signetics	54H04	
	TI	SN54H04	
ITT54H05	Fairchild	54H05	
	National	DM54H05	
	Raytheon	54H05	
ITT54H05	Signetics	54H05	
	TI	SN54H05	
ITT54H10	Fairchild	54H10	
	National	DM54H10	
	Raytheon	54H10	
	Signetics	54H10	
	TI	SN54H10	
ITT54H11	Fairchild	54H11	
	National	DM54H11	
	Raytheon	54H11	
	Signetics	54H11	
	TI	SN54H11	
ITT54H20	Fairchild	54H20	
	National	DM54H20	
	Raytheon	54H20	
	Signetics	54H20	
	TI	SN54H20	
ITT54H21	Fairchild	54H21	
	National	DM54H21	
	Signetics	54H21	
ITT54H30	Fairchild	54H30	
	National	DM54H30	
	Signetics	54H30	
	TI	SN54H30	
ITT54H40	Fairchild	54H40	
	National	DM54H40	
	Raytheon	54H40	
	Signetics	54H40	
	TI	SN54H40	
ITT54H50	Fairchild	54H50	
	National	DM54H50	
	Signetics	54H50	
	TI	SN54H50	
ITT54H51	Fairchild	54H51	
	National	DM54H51	
	Signetics	54H51	
	TI	SN54H51	
ITT54H53	Fairchild	54H53	
	National	DM54H53	
	Signetics	54H53	
	TI	SN54H53	
ITT54H54	Fairchild	54H54	
	National	DM54H54	
	Signetics	54H54	
	TI	SN54H54	
ITT54H60	Fairchild	54H60	
	National	DM54H60	
	Signetics	54H60	
	TI	SN54H60	
ITT54H72	Fairchild	54H72	
		54H73	
	National	DM54H72	
	Signetics	54H72	
	TI	SN54H72	
ITT54H73	Fairchild	54H73	
	National	DM54H73	
	Signetics	54H73	
	TI	SN54H73	
ITT54H74	Fairchild	54H74	
	National	DM54H74	
	Raytheon	54H74	
	Signetics	54H74	
	TI	SN54H74	
♦ITT54H76	Fairchild	54H76	
	National	DM54H76	
	Signetics	54H76	
	TI	SN54H76	
ITT5400	Fairchild	5400	
	Motorola	MC5400	
	National	DM5400	
	Raytheon	5400	
	Signetics	5400	
	TI	SN5400	
ITT5401	Fairchild	5401	
	Motorola	MC5401	
	National	DM5401	
	Raytheon	5401	
	Signetics	5401	
	TI	SN5401	
ITT5402	Fairchild	5402	
	Motorola	MC5402	
	National	DM5402	
	Signetics	5402	
	TI	SN5402	
ITT5403	Fairchild	5403	
	Motorola	MC5403	
ITT5403	National	DM5403	
	Raytheon	5403	
	Signetics	5403	
	TI	SN5403	
ITT5404	Fairchild	5404	
	Motorola	MC5404	
	National	DM5404	
	Raytheon	5404	
	Signetics	5404	
	TI	SN5404	
ITT5405	Fairchild	5405	
	Motorola	MC5405	
	National	DM5405	
	Raytheon	5405	
	Signetics	5405	
	TI	SN5405	
ITT5406	Fairchild	5406	
	Motorola	MC5406	
	National	DM5406	
	Signetics	5406	
	TI	SN5406	
ITT5407	Fairchild	5407	
	Motorola	MC5407	
	National	DM5407	
	Signetics	5407	
	TI	SN5407	
ITT5408	Fairchild	5408	
	Motorola	MC5408	
	National	DM5408	
	Raytheon	5408	
	Signetics	5408	
	TI	SN5408	
ITT5409	Fairchild	5409	
	Motorola	MC5409	
	National	DM5409	
	Raytheon	5409	
	Signetics	5409	
	TI	SN5409	
ITT5410	Fairchild	5410	
	Motorola	MC5410	
	National	DM5410	
	Raytheon	5410	
	Signetics	5410	
	TI	SN5410	
ITT54107	Fairchild	54107	
	Motorola	MC54107	
	National	DM54107	
	Signetics	54107	
	TI	SN54107	
ITT5411	Fairchild	5411	
	National	DM5411	
	Raytheon	5411	
	Signetics	5411	
	TI	SN5411	
ITT5412	Fairchild	5412	
	Raytheon	5412	
	Signetics	5412	
	TI	SN5412	
ITT54121	Fairchild	54121	
	Motorola	MC54121	
	National	DM54121	
	Signetics	54121	
	TI	SN54121	
ITT54122	Fairchild	54122	
	Motorola	MC54122	
	TI	SN54122	
ITT54123	AMD	SN54123	
	Fairchild	54123	
	Motorola	MC54123	
	National	DM54123	
	Raytheon	54123	
	Signetics	54123	
	TI	SN54123	
ITT5413	Fairchild	5413	
	Motorola	MC5413	
	National	DM5413	
	Signetics	5413	
	TI	SN5413	
♦ITT54141	Motorola	MC54141	
	National	DM54141	
	TI	SN54141	
ITT54145	Fairchild	54145	
	Motorola	MC54145	
	National	DM54145	
	Raytheon	54145	
	Signetics	54145	
ITT54145	TI	SN54145	
♦ITT54150	Fairchild	54150	
	Motorola	MC54150	
	National	DM54150	
	Raytheon	54150	
	Signetics	54150	
	TI	SN54150	
ITT54151	Fairchild	54151	
	Motorola	MC54151	
	National	DM54151	
	Raytheon	54151	
	Signetics	54151	
	TI	SN54151	
ITT54153	Fairchild	54153	
	Motorola	MC54153	
	National	DM54153	
	Raytheon	54153	
	Signetics	54153	
	TI	SN54153	
♦ITT54154	AMD	SN54154	
	Fairchild	54154	
	Motorola	MC54154	
	National	DM54154	
	Raytheon	54154	
	Signetics	54154	
	TI	SN54154	
ITT54155	Fairchild	54155	
	Motorola	MC54155	
	National	DM54155	
	Raytheon	54155	
	Signetics	54155	
	TI	SN54155	
ITT54156	Fairchild	54156	
	Motorola	MC54156	
	National	DM54156	
	Raytheon	54156	
	Signetics	54156	
	TI	SN54156	
ITT54157	AMD	SN54157	
	Fairchild	54157	
	Motorola	MC54157	
	National	DM54157	
	Raytheon	54157	
	Signetics	54157	
	TI	SN54157	
ITT5416	Fairchild	5416	
	Motorola	MC5416	
	National	DM5416	
	Signetics	5416	
	TI	SN5416	
ITT54160	AMD	SN54160	
	Fairchild	54160	
	Motorola	MC54160	
	National	DM54160	
	Raytheon	54160	
	Signetics	54160	
	TI	SN54160	
ITT54161	AMD	SN54161	
	Fairchild	54161	
	Motorola	MC54161	
	National	DM54161	
	Raytheon	54161	
	Signetics	54161	
	TI	SN54161	
ITT54162	AMD	SN54162	
	Fairchild	54162	
	Motorola	MC54162	
	National	DM54162	
	Raytheon	54162	
	Signetics	54162	
	TI	SN54162	
ITT54163	AMD	SN54163	
	Fairchild	54163	
	Motorola	MC54163	
	National	DM54163	
	Raytheon	54163	
	Signetics	54163	
	TI	SN54163	
ITT54164	AMD	SN54164	
	Fairchild	54164	
	National	DM54164	
	Raytheon	54164	
	Signetics	54164	
	TI	SN54164	
ITT5417	Fairchild	5417	
	Motorola	MC5417	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

ITT Semiconductors (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
ITT5417	National	DM5417	
	Signetics	5417	
	TI	SN5417	
ITT54180	Fairchild	54180	
	Motorola	MC54180	
	National	DM54180	
	Raytheon	54180	
	Signetics	54180	
	TI	SN54180	
ITT54182	AMD	SN54182	
	Fairchild	54182	
	Motorola	MC54182	
	National	DM54182	
	Raytheon	54182	
	Signetics	54182	
	TI	SN54182	
ITT54190	Fairchild	54190	
	Motorola	MC54190	
	National	DM54190	
	Raytheon	54190	
	Signetics	54190	
	TI	SN54190	
ITT54191	Fairchild	54191	
	Motorola	MC54191	
	National	DM54191	
	Raytheon	54191	
	Signetics	54191	
	TI	SN54191	
ITT54192	AMD	SN54192	
	Fairchild	54192	
	Motorola	MC54192	
	National	DM54192	
	Raytheon	54192	
	Signetics	54192	
	TI	SN54192	
ITT54193	AMD	SN54193	
	Fairchild	54193	
	Motorola	MC54193	
	National	DM54193	
	Raytheon	54193	
	Signetics	54193	
	TI	SN54193	
ITT54194	AMD	SN54194	
	Fairchild	54194	
	Motorola	MC54194	
	National	DM54194	
	Signetics	54194	
	TI	SN54194	
ITT54195	AMD	SN54195	
	Fairchild	54195	
	Motorola	MC54195	
	National	DM54195	
	Raytheon	54195	
	Signetics	54195	
	TI	SN54195	
ITT5420	Fairchild	5420	
	Motorola	MC5420	
	National	DM5420	
	Raytheon	5420	
	Signetics	5420	
	TI	SN5420	
ITT5421	Fairchild	5421	
	Raytheon	5421	
	Signetics	5421	
ITT5425	Fairchild	5425	
	Motorola	MC5425	
	National	DM5425	
	TI	SN5425	
ITT5426	Fairchild	5426	
	Motorola	MC5426	
	National	DM5426	
	Signetics	5426	
	TI	SN5426	
♦ITT5428	TI	SN5428	
ITT5430	Fairchild	5430	
	Motorola	MC5430	
	National	DM5430	
	Signetics	5430	
	TI	SN5430	
ITT5432	Fairchild	5432	
	National	DM5432	
	Signetics	5432	
	TI	SN5432	
♦ITT5433	TI	SN5433	
ITT5437	Fairchild	5437	
	Motorola	MC5437	
	National	DM5437	
	Raytheon	5437	
	Signetics	5437	
	TI	SN5437	
ITT5438	Fairchild	5438	
	Motorola	MC5438	
	National	DM5438	
	Raytheon	5438	
	Signetics	5438	
	TI	SN5438	
ITT5440	Fairchild	5440	
	Motorola	MC5440	
	National	DM5440	
	Signetics	5440	
	TI	SN5440	
♦ITT5441	Fairchild	5441	
	National	DM5441	
ITT5442	Fairchild	5442	
	Motorola	MC5442	
	National	DM5442	
	Raytheon	5442	
	Signetics	5442	
	TI	SN5442	
ITT5443	Fairchild	5443	
	Motorola	MC5443	
	Raytheon	5443	
	Signetics	5443	
	TI	SN5443	
ITT5444	Fairchild	5444	
	Motorola	MC5444	
	Raytheon	5444	
	Signetics	5444	
	TI	SN5444	
ITT5445	Fairchild	5445	
	Motorola	MC5445	
	National	DM5445	
	Raytheon	5445	
	Signetics	5445	
	TI	SN5445	
ITT5446	Fairchild	5446	
	Motorola	MC5446	
	National	DM5446	
	Signetics	5446	
	TI	SN5446	
ITT5447	Fairchild	5447	
	Motorola	MC5447	
	National	DM5447	
	Signetics	5447	
	TI	SN5447	
ITT5448	Fairchild	5448	
	Motorola	MC5448	
	National	DM5448	
	Signetics	5448	
	TI	SN5448	
ITT5450	Fairchild	5450	
	Motorola	MC5450	
	National	DM5450	
	Signetics	5450	
	TI	SN5450	
ITT5451	Fairchild	5451	
	Motorola	MC5451	
	National	DM5451	
	Signetics	5451	
	TI	SN5451	
ITT5453	Fairchild	5453	
	Motorola	MC5453	
	National	DM5453	
	Signetics	5453	
	TI	SN5453	
ITT5454	Fairchild	5454	
	Motorola	MC5454	
	National	DM5454	
	Signetics	5454	
	TI	SN5454	
♦ITT5460	Fairchild	5460	
	Motorola	MC5460	
	National	DM5460	
	Signetics	5460	
	TI	SN5460	
ITT5470	Fairchild	5470	
	Motorola	MC5470	
	National	DM5470	
	TI	SN5470	
ITT5472	Fairchild	5472	
	Motorola	MC5472	
	National	DM5472	
	Signetics	5472	
	TI	SN5472	
ITT5473	Fairchild	5473	
	Motorola	MC5473	
	National	DM5473	
	Signetics	5473	
	TI	SN5473	
ITT5474	Fairchild	5474	
	Motorola	MC5474	
	National	DM5474	
	Raytheon	5474	
	Signetics	5474	
	TI	SN5474	
ITT5475	Fairchild	5475	
	Motorola	MC5475	
	National	DM5475	
	Signetics	5475	
	TI	SN5475	
ITT5476	Fairchild	5476	
	Motorola	MC5476	
	National	DM5476	
	Signetics	5476	
	TI	SN5476	
ITT5480	Fairchild	5480	
	Motorola	MC5480	
	Signetics	5480	
	TI	SN5480	
ITT5482	Fairchild	5482	
	Motorola	MC5482	
	TI	SN5482	
ITT5486	Fairchild	5486	
	Motorola	MC5486	
	National	DM5486	
	Raytheon	5486	
	Signetics	5486	
	TI	SN5486	
ITT5490	Fairchild	5490	
	Motorola	MC5490	
	National	DM5490	
	Signetics	5490	
	TI	SN5490	
ITT5491	Fairchild	5491	
	Motorola	MC5491	
	National	DM5491	
	Signetics	5491	
	TI	SN5491	
ITT5492	Fairchild	5492	
	Motorola	MC5492	
	National	DM5492	
	Signetics	5492	
	TI	SN5492	
ITT5493	Fairchild	5493	
	Motorola	MC5493	
	National	DM5493	
	TI	SN5493	
♦ITT5494	Fairchild	5494	
	Motorola	MC5494	
	TI	SN5494	
ITT5495	Fairchild	5495	
	Motorola	MC5495	
	National	DM5495	
	Signetics	5495	
	TI	SN5495	
ITT5496	Fairchild	5496	
	Motorola	MC5496	
	National	DM5496	
	Signetics	5496	
	TI	SN5496	
ITT5510A	TI	SN55107A	
ITT55107B	TI	SN55107B	
ITT55108B	TI	SN55108B	
ITT55109	TI	SN55109	
ITT55110	TI	SN55110	
ITT55138	TI	SN55138	
ITT552	Sprague	ULN-2001	
ITT5520	TI	SN5520	
♦ITT5521	TI	SN5520	
ITT5522	TI	SN5522	
♦ITT5523	TI	SN5522	
ITT55234	TI	SN55234	
♦ITT55235	TI	SN55234	
ITT5524	TI	SN5524	
ITT5525	TI	SN5524	
ITT5528	TI	SN5528	
ITT55324	TI	SN55324	
ITT55325	TI	SN55324	
ITT554	Sprague	ULN-2002	
ITT55450	TI	SN55450	
ITT55451	TI	SN55451	
ITT55452	TI	SN55452	
ITT55453	TI	SN55453	
ITT55454	TI	SN55454	
ITT55460	TI	SN55460	
ITT55461	TI	SN55461	
ITT55462	TI	SN55462	
ITT55463	TI	SN55463	
ITT55464	TI	SN55464	
ITT556	Sprague	ULN-2003	
ITT652	Motorola	MC1411	
	Sprague	ULN-2001	
ITT654	Motorola	MC1412	
	Sprague	ULN-2002	
ITT656	Motorola	MC1413	
	Sprague	ULN-2003	
ITT74H01	Fairchild	74H01	
	National	DM74H01	
	NEC America	μPB74H01	
	Raytheon	74H01	
	Signetics	74H01	
	TI	SN74H01	
ITT74H04	Fairchild	74H04	
	National	DM74H04	
	NEC America	μPB74H04	
	Raytheon	74H04	
	Signetics	74H04	
	TI	SN74H04	
ITT74H05	Fairchild	74H05	
	National	DM74H05	
	Raytheon	74H05	
	TI	SN74H05	
ITT74H10	Fairchild	74H10	
	National	DM74H10	
	NEC America	μPB74H10	
	Raytheon	74H10	
	Signetics	74H10	
	TI	SN74H10	
ITT74H11	Fairchild	74H11	
	National	DM74H11	
	Raytheon	74H11	
	Signetics	74H11	
	TI	SN74H11	
ITT74H20	Fairchild	74H20	
	National	DM74H20	
	NEC America	μPB74H20	
	Raytheon	74H20	
	Signetics	74H20	
	TI	SN74H20	
ITT74H21	Fairchild	74H21	
	National	DM74H21	
	Signetics	74H21	
	TI	SN74H21	
ITT74H30	Fairchild	74H30	
	National	DM74H30	
	NEC America	μPB74H30	
	Signetics	74H30	
	TI	SN74H30	
ITT74H40	Fairchild	74H40	
	National	DM74H40	
	NEC America	μPB74H40	
	Raytheon	74H40	
	Signetics	74H40	
	TI	SN74H40	
ITT74H50	Fairchild	74H50	
	National	DM74H50	
	Signetics	74H50	
	TI	SN74H50	
ITT74H51	Fairchild	74H51	
	National	DM74H51	
	NEC America	μPB74H51	
	Signetics	74H51	
	TI	SN74H51	
ITT74H53	Fairchild	74H53	
	National	DM74H53	
	Signetics	74H53	
	TI	SN74H53	
ITT74H54	Fairchild	74H54	
	National	DM74H54	
	Signetics	74H54	
	TI	SN74H54	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

ITT Semiconductors (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
ITT74H60	Fairchild	74H60	
	National	DM74H60	
	Signetics	74H60	
	TI	SN74H60	
ITT74H72	Fairchild	74H72	
	National	DM74H72	
	Signetics	74H72	
	TI	SN74H72	
ITT74H73	Fairchild	74H73	
	National	DM74H73	
	Signetics	74H73	
	TI	SN74H73	
ITT74H74	Fairchild	74H74	
	National	DM74H74	
	Raytheon	74H74	
	Signetics	74H74	
	TI	SN74H74	
♦ITT74H76	Fairchild	74H76	
	National	DM74H76	
	Signetics	74H76	
	TI	SN74H76	
ITT74LS00	Fairchild	74LS00	
	Motorola	SN74LS00	
	National	DM74LS00	
	NEC America	μPB74LS00	
	Raytheon	74LS00	
	Signetics	74LS00	
	TI	SN74LS00	
ITT74LS01	Fairchild	74LS01	
	National	DM74LS01	
	Raytheon	74LS01	
	Signetics	74LS01	
	TI	SN74LS01	
ITT74LS02	Fairchild	74LS02	
	Motorola	SN74LS02	
	National	DM74LS02	
	NEC America	μPB74LS02	
	Raytheon	74LS02	
	Signetics	74LS02	
	TI	SN74LS02	
ITT74LS03	Fairchild	74LS03	
	Motorola	SN74LS03	
	National	DM74LS03	
	NEC America	μPB74LS03	
	Raytheon	74LS03	
	Signetics	74LS03	
	TI	SN74LS03	
ITT74LS04	Fairchild	74LS04	
	Motorola	SN74LS04	
	National	DM74LS04	
	NEC America	μPB74LS04	
	Raytheon	74LS04	
	Signetics	74LS04	
	TI	SN74LS04	
ITT74LS05	Fairchild	74LS05	
	Motorola	SN74LS05	
	National	DM74LS05	
	NEC America	μPB74LS05	
	Raytheon	74LS05	
	Signetics	74LS05	
	TI	SN74LS05	
ITT74LS08	Fairchild	74LS08	
	Motorola	SN74LS08	
	National	DM74LS08	
	NEC America	μPB74LS08	
	Raytheon	74LS08	
	Signetics	74LS08	
	TI	SN74LS08	
ITT74LS09	Fairchild	74LS09	
	Motorola	SN74LS09	
	National	DM74LS09	
	Raytheon	74LS09	
	Signetics	74LS09	
	TI	SN74LS09	
ITT74LS10	Fairchild	74LS10	
	Motorola	SN74LS10	
	National	DM74LS10	
	NEC America	μPB74LS10	
	Raytheon	74LS10	
	Signetics	74LS10	
	TI	SN74LS10	
ITT74LS107	Fairchild	74LS107	
	Raytheon	74LS107	
ITT74LS107	Signetics	74LS107	
ITT74LS109A	Fairchild	74LS109	
	Motorola	SN74LS109	
	National	DM74LS109	
	NEC America	μPB74LS109	
	Raytheon	74LS109	
	Signetics	74LS109	
	TI	SN74LS109	
ITT74LS11	Fairchild	74LS11	
	Motorola	SN74LS11	
	National	DM74LS11	
	NEC America	μPB74LS11	
	Raytheon	74LS11	
	Signetics	74LS11	
	TI	SN74LS11	
ITT74LS112	Fairchild	74LS112	
	National	DM74LS112	
	NEC America	μPB74LS112	
	Raytheon	74LS112	
	Signetics	74LS112	
	TI	SN74LS112	
ITT74LS113	Fairchild	74LS113	
	National	DM74LS113	
	NEC America	μPB74LS113	
	Raytheon	74LS113	
	Signetics	74LS113	
	TI	SN74LS113	
ITT74LS114	Fairchild	74LS114	
	Motorola	SN74LS114	
	National	DM74LS114	
	Raytheon	74LS114	
	Signetics	74LS114	
	TI	SN74LS114	
ITT74LS123	AMD	SN74LS123	
	National	DM74LS123	
	Raytheon	**74LS123**	**275**
	TI	SN74LS123	
ITT74LS125	Fairchild	74LS125	
	National	DM74LS125	
	Raytheon	74LS125	
	Signetics	74LS125	
	TI	SN74LS125A	
ITT74LS126	Fairchild	74LS126	
	Motorola	SN74LS126	
	National	DM74LS126	
	Raytheon	74LS126	
	Signetics	74LS126	
	TI	SN74LS126A	
ITT74LS13	Fairchild	74LS13	
	Motorola	SN74LS13	
	National	DM74LS13	
	Raytheon	**74LS13**	**264**
	Signetics	74LS13	
	TI	SN74LS13	
ITT74LS132	Fairchild	74LS132	
	Motorola	SN74LS132	
	National	DM74LS132	
	Raytheon	**74LS132**	**264**
	Signetics	74LS132	
	TI	SN74LS132	
ITT74LS133	TI	SN74LS133	
ITT74LS136	Fairchild	74LS136	
	Motorola	SN74LS136	
	National	DM74LS136	
	Raytheon	74LS136	
	Signetics	74LS136	
	TI	SN74LS136	
ITT74LS138	AMD	SN74LS138	
	Fairchild	74LS138	
	Motorola	SN74LS138	
	National	DM74LS138	
	NEC America	μPB74LS138	
	Raytheon	74LS138	
	Signetics	74LS138	
	TI	SN74LS138	
ITT74LS139	AMD	SN74LS139	
	Fairchild	74LS139	
	Motorola	SN74LS139	
	National	DM74LS139	
	NEC America	μPB74LS139	
	Raytheon	74LS139	
	Signetics	74LS139	
	TI	SN74LS139	
ITT74LS14	Fairchild	74LS14	
	Motorola	SN74LS14	
	National	DM74LS14	
ITT74LS14	**Raytheon**	**74LS14**	**264**
	Signetics	74LS14	
	TI	SN74LS14	
ITT74LS15	Fairchild	74LS15	
	Motorola	SN74LS15	
	National	DM74LS15	
	Raytheon	74LS15	
	Signetics	74LS15	
	TI	SN74LS15	
ITT74LS151	AMD	SN74LS151	
	Fairchild	74LS151	
	Motorola	SN74LS151	
	National	DM74LS151	
	NEC America	μPB74LS151	
	Raytheon	74LS151	
	Signetics	74LS151	
	TI	SN74LS151	
ITT74LS153	AMD	SN74LS153	
	Fairchild	74LS153	
	Motorola	SN74LS153	
	National	DM74LS153	
	NEC America	μPB74LS153	
	Raytheon	74LS153	
	Signetics	74LS153	
	TI	SN74LS153	
ITT74LS155	Fairchild	74LS155	
	Motorola	SN74LS155	
	National	DM74LS155	
	NEC America	μPB74LS155	
	Raytheon	74LS155	
	Signetics	74LS155	
	TI	SN74LS155	
ITT74LS156	Fairchild	74LS156	
	Motorola	SN74LS156	
	National	DM74LS156	
	Raytheon	74LS156	
	Signetics	74LS156	
	TI	SN74LS156	
ITT74LS157	AMD	SN74LS157	
	Fairchild	74LS157	
	Motorola	SN74LS157	
	National	DM74LS157	
	NEC America	μPB74LS157	
	Raytheon	74LS157	
	Signetics	74LS157	
	TI	SN74LS157	
ITT74LS158	AMD	SN74LS158	
	Fairchild	74LS158	
	Motorola	SN74LS158	
	National	DM74LS158	
	Raytheon	74LS158	
	Signetics	74LS158	
	TI	SN74LS158	
ITT74LS160	AMD	SN74LS160	
	Fairchild	74LS160	
	Motorola	SN74LS160	
	National	DM74LS160	
	Raytheon	74LS160	
	Signetics	74LS160	
	TI	SN74LS160	
ITT74LS161	AMD	SN74LS161	
	Fairchild	74LS161	
	Motorola	SN74LS161	
	National	DM74LS161	
	NEC America	μPB74LS161	
	Raytheon	74LS161	
	Signetics	74LS161	
	TI	SN74LS161	
ITT74LS162	AMD	SN74LS162	
	Fairchild	74LS162	
	Motorola	SN74LS162	
	National	DM74LS162	
	Raytheon	74LS162	
	Signetics	74LS162	
	TI	SN74LS162	
ITT74LS163	AMD	SN74LS163	
	Fairchild	74LS163	
	Motorola	SN74LS163	
	National	DM74LS163	
	Raytheon	74LS163	
	Signetics	74LS163	
	TI	SN74LS163	
ITT74LS164	AMD	SN74LS164	
	Fairchild	74LS164	
	Motorola	SN74LS164	
	National	DM74LS164	
ITT74LS164	NEC America	μPB74LS164	
	Raytheon	**74LS164**	**272**
	Signetics	74LS164	
	TI	SN74LS164	
ITT74LS170	AMD	SN74LS170	
	Fairchild	74LS170	
	Motorola	SN74LS170	
	National	DM74LS170	
	Raytheon	74LS170	
	Signetics	74LS170	
	TI	SN74LS170	
ITT74LS174	AMD	SN74LS174	
	Fairchild	74LS174	
	Motorola	SN74LS174	
	National	DM74LS174	
	Raytheon	74LS174	
	Signetics	74LS174	
	TI	SN74LS174	
ITT74LS175	AMD	SN74LS175	
	Fairchild	74LS175	
	Motorola	SN74LS175	
	National	DM74LS175	
	NEC America	μPB74LS175	
	Raytheon	74LS175	
	Signetics	74LS175	
	TI	SN74LS175	
ITT74LS190	AMD	SN74LS190	
	Fairchild	74LS190	
	Motorola	SN74LS190	
	National	DM74LS190	
	Raytheon	74LS190	
	Signetics	74LS190	
	TI	SN74LS190	
ITT74LS191	AMD	SN74LS191	
	Fairchild	74LS191	
	Motorola	SN74LS191	
	National	DM74LS191	
	Raytheon	74LS191	
	Signetics	74LS191	
	TI	SN74LS191	
ITT74LS192	AMD	SN74LS192	
	Fairchild	74LS192	
	Motorola	SN74LS192	
	National	DM74LS192	
	NEC America	μPB74LS192	
	Raytheon	74LS192	
	Signetics	74LS192	
	TI	SN74LS192	
ITT74LS193	AMD	SN74LS193	
	Fairchild	74LS193	
	Motorola	SN74LS193	
	National	DM74LS193	
	NEC America	μPB74LS193	
	Raytheon	74LS193	
	Signetics	74LS193	
	TI	SN74LS193	
ITT74LS194A	AMD	SN74LS194A	
	Fairchild	74LS194	
	Motorola	SN74LS194	
	NEC America	μPB74LS194	
	Raytheon	74LS194A	
	Signetics	74LS194A	
	TI	SN74LS194A	
ITT74LS195A	AMD	SN74LS195A	
	Fairchild	74LS195	
	Motorola	SN74LS195	
	NEC America	μPB74LS195	
	Raytheon	74LS195A	
	Signetics	74LS195A	
	TI	SN74LS195A	
ITT74LS196	Fairchild	74LS196	
	Motorola	SN74LS196	
	National	DM74LS196	
	Raytheon	74LS196	
	Signetics	74LS196	
	TI	SN74LS196	
ITT74LS197	Fairchild	74LS197	
	Motorola	SN74LS197	
	National	DM74LS197	
	Raytheon	74LS197	
	Signetics	74LS197	
	TI	SN74LS197	
ITT74LS20	Fairchild	74LS20	
	Motorola	SN74LS20	
	National	DM74LS20	
	NEC America	μPB74LS20	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

ITT Semiconductors (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
ITT74LS20	Raytheon	74LS20	
	Signetics	74LS20	
	TI	SN74LS20	
ITT74LS21	Fairchild	74LS21	
	Motorola	SN74LS21	
	National	DM74LS21	
	NEC America	μPB74LS21	
	Raytheon	74LS21	
	Signetics	74LS21	
	TI	SN74LS21	
ITT74LS22	Fairchild	74LS22	
	Motorola	SN74LS22	
	National	DM74LS22	
	Raytheon	74LS22	
	Signetics	74LS22	
	TI	SN74LS22	
ITT74LS221	Fairchild	74LS221	
	Motorola	SN74LS221	
	National	DM74LS221	
	Raytheon	**74LS221**	**275**
	Signetics	74LS221	
	TI	SN74LS221	
ITT74LS240	AMD	SN74LS240	
	Fairchild	74LS240	
	MMI	74LS240	
	Motorola	SN74LS240	
	Raytheon	**74LS240**	**279**
	Signetics	74LS240	
	TI	SN74LS240	
ITT74LS241	AMD	SN74LS241	
	Fairchild	74LS241	
	MMI	74LS241	
	Motorola	SN74LS241	
	Raytheon	**74LS241**	**279**
	Signetics	74LS241	
	TI	SN74LS241	
ITT74LS242	AMD	SN74LS242	
	Fairchild	74LS242	
	Motorola	SN74LS242	
	Raytheon	**74LS242**	**282**
	Signetics	74LS242	
	TI	SN74LS242	
ITT74LS243	AMD	SN74LS243	
	Fairchild	74LS243	
	Motorola	SN74LS243	
	Raytheon	**74LS243**	**282**
	Signetics	74LS243	
	TI	SN74LS243	
ITT74LS244	AMD	SN74LS244	
	Fairchild	74LS244	
	MMI	74LS244	
	Motorola	SN74LS244	
	Raytheon	**74LS244**	**279**
	Signetics	74LS244	
	TI	SN74LS244	
ITT74LS251	AMD	SN74LS251	
	Fairchild	74LS251	
	Motorola	SN74LS251	
	National	DM74LS251	
	NEC America	μPB74LS251	
	Raytheon	74LS251	
	Signetics	74LS251	
	TI	SN74LS251	
ITT74LS253	AMD	SN74LS253	
	Fairchild	74LS253	
	Motorola	SN74LS253	
	National	DM74LS253	
	NEC America	μPB74LS253	
	Raytheon	74LS253	
	Signetics	74LS253	
	TI	SN74LS253	
ITT74LS257	AMD	SN74LS257	
	Fairchild	74LS257	
	Motorola	SN74LS257	
	National	DM74LS257	
	NEC America	μPB74LS257	
	Raytheon	74LS257	
	Signetics	74LS257	
	TI	SN74LS257	
ITT74LS258	AMD	SN74LS258	
	Fairchild	74LS258	
	Motorola	SN74LS258	
	National	DM74LS258	
ITT74LS258	NEC America	μPB74LS258	
	Raytheon	74LS258	
	Signetics	74LS258	
	TI	SN74LS258	
ITT74LS259	Fairchild	74LS259	
	Motorola	SN74LS259	
	TI	SN74LS259	
ITT74LS261	**Raytheon**	**74LS261**	**284**
	Signetics	74LS261	
	TI	SN74LS261	
ITT74LS266	Fairchild	74LS266	
	Motorola	SN74LS266	
	Raytheon	74LS266	
	Signetics	74LS266	
	TI	SN74LS266	
ITT74LS27	Fairchild	74LS27	
	Motorola	SN74LS27	
	National	DM74LS27	
	NEC America	μPB74LS27	
	Raytheon	74LS27	
	Signetics	74LS27	
	TI	SN74LS27	
ITT74LS273	AMD	SN74LS273	
	Fairchild	74LS273	
	Signetics	74LS273	
	TI	SN74LS273	
ITT74LS279	Fairchild	74LS279	
	Motorola	SN74LS279	
	National	DM74LS279	
	NEC America	μPB74LS279	
	Raytheon	74LS279	
	Signetics	74LS279	
	TI	SN74LS279	
ITT74LS28	Fairchild	74LS28	
	Raytheon	74LS28	
	Signetics	74LS28	
	TI	SN74LS28	
ITT74LS283	Fairchild	74LS283	
	Motorola	SN74LS283	
	National	DM74LS283	
	Raytheon	74LS283	
	Signetics	74LS283	
	TI	SN74LS283	
ITT74LS290	Fairchild	74LS290	
	Motorola	SN74LS290	
	National	DM74LS290	
	Signetics	74LS290	
	TI	SN74LS290	
ITT74LS293	Fairchild	74LS293	
	Motorola	SN74LS293	
	National	DM74LS293	
	Signetics	74LS293	
	TI	SN74LS293	
ITT74LS299	AMD	SN74LS299	
	Fairchild	74LS299	
	Raytheon	74LS299	
	TI	SN74LS299	
ITT74LS30	Fairchild	74LS30	
	Motorola	SN74LS30	
	National	DM74LS30	
	NEC America	μPB74LS30	
	Raytheon	74LS30	
	Signetics	74LS30	
	TI	SN74LS30	
ITT74LS32	Fairchild	74LS32	
	Motorola	SN74LS32	
	National	DM74LS32	
	NEC America	μPB74LS32	
	Raytheon	74LS32	
	Signetics	74LS32	
	TI	SN74LS32	
ITT74LS323	AMD	SN74LS323	
	Raytheon	74LS323	
	TI	SN74LS323	
ITT74LS365	Fairchild	74LS365	
	Motorola	SN74LS365	
	National	DM74LS365	
	NEC America	μPB74LS365	
	Raytheon	**74LS365**	**286**
	Signetics	74LS365	
	TI	SN74LS365	
ITT74LS366	Fairchild	74LS366	
	Motorola	SN74LS366	
	National	DM74LS366	
	NEC America	μPB74LS366	
	Raytheon	**74LS366**	**286**
ITT74LS366	Signetics	74LS366	
	TI	SN74LS366	
ITT74LS367	Fairchild	74LS367	
	Motorola	SN74LS367	
	National	DM74LS367	
	NEC America	μPB74LS367	
	Raytheon	**74LS367**	**286**
	Signetics	74LS367	
	TI	SN74LS367	
ITT74LS368	Fairchild	74LS368	
	Motorola	SN74LS368	
	National	DM74LS368	
	NEC America	μPB74LS368	
	Raytheon	**74LS368**	**286**
	Signetics	74LS368	
	TI	SN74LS368	
ITT74LS37	Fairchild	74LS37	
	Motorola	SN74LS37	
	National	DM74LS37	
	NEC America	μPB74LS37	
	Raytheon	74LS37	
	Signetics	74LS37	
	TI	SN74LS37	
ITT74LS373	AMD	SN74LS373	
	Fairchild	74LS373	
	MMI	74LS373	
	Raytheon	**74LS373**	**288**
	Signetics	74LS373	
	TI	SN74LS373	
ITT74LS374	AMD	SN74LS374	
	Fairchild	74LS374	
	MMI	74LS374	
	Raytheon	**74LS374**	**288**
	TI	SN74LS374	
ITT74LS375	Motorola	SN74LS375	
	NEC America	μPB74LS375	
	Raytheon	74LS375	
	Signetics	74LS375	
	TI	SN74LS375	
ITT74LS377	AMD	SN74LS377	
	Fairchild	74LS377	
	Raytheon	**74LS377**	**288**
	Signetics	74LS377	
	TI	SN74LS377	
ITT74LS378	AMD	SN74LS378	
	Fairchild	74LS378	
	Signetics	74LS378	
	TI	SN74LS378	
ITT74LS38	Fairchild	74LS38	
	Motorola	SN74LS38	
	National	DM74LS38	
	NEC America	μPB74LS38	
	Raytheon	74LS38	
	Signetics	74LS38	
	TI	SN74LS38	
ITT74LS381	AMD	SN74LS381	
	TI	SN74LS381	
ITT74LS386	Fairchild	74LS386	
	Motorola	SN74LS386	
	National	DM74LS386	
	Raytheon	74LS386	
	Signetics	74LS386	
	TI	SN74LS386	
ITT74LS40	Fairchild	74LS40	
	Motorola	SN74LS40	
	National	DM74LS40	
	NEC America	μPB74LS40	
	Raytheon	74LS40	
	Signetics	74LS40	
	TI	SN74LS40	
ITT74LS42	Fairchild	74LS42	
	Motorola	SN74LS42	
	National	DM74LS42	
	NEC America	μPB74LS42	
	Raytheon	**74LS42**	**266**
	Signetics	74LS42	
	TI	SN74LS42	
ITT74LS51	Fairchild	74LS51	
	Motorola	SN74LS51	
	National	DM74LS51	
	NEC America	μPB74LS51	
	Raytheon	74LS51	
	Signetics	74LS51	
	TI	SN74LS51	
ITT74LS54	Fairchild	74LS54	
	Motorola	SN74LS54	
ITT74LS54	National	DM74LS54	
	NEC America	μPB74LS54	
	Raytheon	74LS54	
	Signetics	74LS54	
	TI	SN74LS54	
ITT74LS73	Fairchild	74LS73	
	Motorola	SN74LS73	
	National	DM74LS73	
	Raytheon	74LS73	
	Signetics	74LS73	
	TI	SN74LS73	
ITT74LS74	Fairchild	74LS74	
	Motorola	SN74LS74	
	National	DM74LS74	
	NEC America	μPB74LS74	
	Raytheon	74LS74	
	Signetics	74LS74	
	TI	SN74LS74	
ITT74LS75	Fairchild	74LS75	
	National	DM74LS75	
	Raytheon	74LS75	
	Signetics	74LS75	
	TI	SN74LS75	
ITT74LS76	National	DM74LS76	
	Raytheon	74LS76	
	Signetics	74LS76	
	TI	SN74LS76	
ITT74LS78	National	DM74LS78	
	Raytheon	74LS78	
	Signetics	74LS78	
	TI	SN74LS78	
ITT74LS83A	Fairchild	74LS83	
	Motorola	SN74LS83	
	National	DM74LS83A	
	Raytheon	74LS83A	
	Signetics	74LS83	
	TI	SN74LS83A	
ITT74LS85	Fairchild	74LS85	
	Motorola	SN74LS85	
	National	DM74LS85	
	Raytheon	74LS85	
	Signetics	74LS85	
	TI	SN74LS85	
ITT74LS86	Fairchild	74LS86	
	Motorola	SN74LS86	
	NEC America	μPB74LS86	
	Raytheon	74LS86	
	Signetics	74LS86	
	TI	SN74LS86	
ITT74LS90	Fairchild	74LS90	
	Motorola	SN74LS90	
	Raytheon	**74LS90**	**268**
	Signetics	74LS90	
	TI	SN74LS90	
ITT74LS93	Fairchild	74LS93	
	Motorola	SN74LS93	
	Raytheon	**74LS93**	**268**
	Signetics	74LS93	
	TI	SN74LS93	
ITT74LS95B	Fairchild	74LS95	
	Motorola	SN74LS95	
	Raytheon	74LS95B	
	Signetics	74LS95B	
	TI	SN74LS95B	
ITT74LS96	TI	SN74LS96	
ITT7400	Fairchild	7400	
	Hitachi	HD7400	
	Mitsubishi	M53200	
	Motorola	MC7400	
	National	DM7400	
	NEC America	μPB7400	
	Raytheon	7400	
	Signetics	7400	
	TI	SN7400	
	Toshiba	TC7400	
	TRW	7400	
ITT7401	Fairchild	7401	
	Mitsubishi	M53201	
	Motorola	MC7401	
	National	DM7401	
	Raytheon	7401	
	Signetics	7401	
	TI	SN7401	
	TRW	7401	
ITT7402	Fairchild	7402	
	Hitachi	HD7402	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

ITT Semiconductors (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
ITT7402	Mitsubishi	M53202	
	Motorola	MC7402	
	National	DM7402	
	NEC America	μPB7402	
	Signetics	7402	
	TI	SN7402	
●	TRW	7402	
ITT7403	Fairchild	7403	
	Hitachi	HD7403	
	Mitsubishi	M53203	
	Motorola	MC7403	
	National	DM7403	
	Raytheon	7403	
	Signetics	7403	
	TI	SN7403	
	TRW	7403	
ITT7404	Fairchild	7404	
	Hitachi	HD7404	
	Mitsubishi	M53204	
●	Motorola	MC7404	
	National	DM7404	
	NEC America	μPB7404	
	Raytheon	7404	
	Signetics	7404	
	TI	SN7404	
	Toshiba	TC7404	
	TRW	7404	
ITT7405	Fairchild	7405	
	Hitachi	HD7405	
	Mitsubishi	M53205	
	Motorola	MC7405	
	National	DM7405	
	NEC America	μPB7405	
	Raytheon	7405	
	Signetics	7405	
	TI	SN7405	
	TRW	7405	
ITT7406	Fairchild	7406	
	Hitachi	HD7406	
	Mitsubishi	M53206	
	Motorola	MC7406	
	National	DM7406	
	Signetics	7406	
	TI	SN7406	
	TRW	7406	
ITT7407	Fairchild	7407	
	Hitachi	HD7407	
	Mitsubishi	M53207	
	Motorola	MC7407	
	National	DM7407	
	Signetics	7407	
	TI	SN7407	
	TRW	7407	
ITT7408	Fairchild	7408	
	Mitsubishi	M53208	
	Motorola	MC7408	
	National	DM7408	
	Raytheon	7408	
	Signetics	7408	
	TI	SN7408	
	Toshiba	TC7408	
	TRW	7408	
ITT7409	Fairchild	7409	
	Hitachi	HD7409	
	Mitsubishi	M53209	
	Motorola	MC7409	
	National	DM7409	
	Raytheon	7409	
	Signetics	7409	
	TI	SN7409	
	TRW	7409	
ITT7410	Fairchild	7410	
	Hitachi	HD7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
	National	DM7410	
	NEC America	μPB7410	
	Raytheon	7410	
	Signetics	7410	
	TI	SN7410	
		SN7427	
	Toshiba	TC7410	
	TRW	7410	
ITT74107	Fairchild	74107	
	Hitachi	HD74107	
	Mitsubishi	M53307	
	Motorola	MC74107	
	National	DM74107	
	NEC America	μPB74107	
	Signetics	74107	
	TI	SN74107	
ITT7411	Fairchild	7411	
	Hitachi	HD7411	
	National	DM7411	
	Raytheon	7411	
	Signetics	7411	
ITT7412	Fairchild	7412	
	Hitachi	HD7412	
	Raytheon	7412	
	Signetics	7412	
	TI	SN7412	
	TRW	7412	
ITT74121	Fairchild	74121	
	Hitachi	HD74121	
	Mitsubishi	M53321	
	Motorola	MC74121	
	National	DM74121	
	Signetics	74121	
	TI	SN74121	
	TRW	74121	
ITT74122	Fairchild	74122	
	Mitsubishi	M53322	
	Motorola	MC74122	
	Signetics	74122	
	TI	SN74122	
ITT74123	AMD	SN74123	
	Fairchild	74123	
	Mitsubishi	M53323	
	Motorola	MC74123	
	National	DM74123	
	NEC America	μPB74123	
	Raytheon	74123	
	Signetics	74123	
	TI	SN74123	
	TRW	74123	
ITT7413	Fairchild	7413	
	Mitsubishi	M53213	
	Motorola	MC7413	
	National	DM7413	
	NEC America	μPB7413	
	Signetics	7413	
	TI	SN7413	
	TRW	7413	
♦ITT74141	Fairchild	74141	
	Motorola	MC74141	
	National	DM74141	
	NEC America	μPB74141	
	TI	SN74141	
ITT74145	Fairchild	74145	
	Mitsubishi	M53345	
	Motorola	MC74145	
	National	DM74145	
	Raytheon	74145	
	Signetics	74145	
	TI	SN74145	
	TRW	74145	
♦ITT74150	Fairchild	74150	
	Hitachi	HD74150	
	Mitsubishi	M53350	
	Motorola	MC74150	
	National	DM74150	
	NEC America	μPB74150	
	Raytheon	74150	
	Signetics	74150	
	TI	SN74150	
	TRW	74150	
ITT74151	Fairchild	74151	
	Hitachi	HD74151	
	Mitsubishi	M53351	
	Motorola	MC74151	
	National	DM74151	
	NEC America	μPB74151	
	Raytheon	74151	
	Signetics	74151	
	TI	SN74151	
	TRW	74151	
ITT74153	Fairchild	74153	
	Mitsubishi	M53353	
	Motorola	MC74153	
ITT74153	National	DM74153	
	NEC America	μPB74153	
	Raytheon	74153	
	Signetics	74153	
	TI	SN74153	
	TRW	74153	
♦ITT74154	AMD	SN74154	
	Fairchild	74154	
	Mitsubishi	M53354	
	Motorola	MC74154	
	National	DM74154	
	NEC America	μPB74154	
	Raytheon	74154	
	Signetics	74154	
	TI	SN74154	
	TRW	74154	
ITT74155	Fairchild	74155	
	Mitsubishi	M53355	
	Motorola	MC74155	
	National	DM74155	
	NEC America	μPB74155	
	Raytheon	74155	
	Signetics	74155	
	TI	SN74155	
	TRW	74155	
ITT74156	Fairchild	74156	
	Hitachi	HD74156	
	Mitsubishi	M53356	
	Motorola	MC74156	
	National	DM74156	
	NEC America	μPB74156	
	Raytheon	74156	
	Signetics	74156	
	TI	SN74156	
	TRW	74156	
ITT74157	AMD	SN74157	
	Fairchild	74157	
	Hitachi	HD74157	
	Mitsubishi	M53357	
	Motorola	MC74157	
	National	DM74157	
	NEC America	μPB74157	
	Raytheon	74157	
	Signetics	74157	
	TI	SN74157	
ITT7416	Fairchild	7416	
	Hitachi	HD7416	
	Mitsubishi	M53216	
	Motorola	MC7416	
	National	DM7416	
	Signetics	7416	
	TI	SN7416	
	TRW	7416	
ITT74160	AMD	SN74160	
	Fairchild	74160	
	Hitachi	HD74160	
	Mitsubishi	M53360	
	Motorola	MC74160	
	National	DM74160	
	Raytheon	74160	
	Signetics	74160	
	TI	SN74160	
	TRW	74160	
ITT74161	AMD	SN74161	
	Fairchild	74161	
	Hitachi	HD74161	
	Mitsubishi	M53361	
	Motorola	MC74161	
	National	DM74161	
	NEC America	μPB74161	
	Raytheon	74161	
	Signetics	74161	
	TI	SN74161	
	TRW	74161	
ITT74162	AMD	SN74162	
	Fairchild	74162	
	Hitachi	HD74162	
	Mitsubishi	M53362	
	Motorola	MC74162	
	National	DM74162	
	Raytheon	74162	
	Signetics	74162	
	TI	SN74162	
	TRW	74162	
ITT74163	AMD	SN74163	
	Fairchild	74163	
ITT74163	Hitachi	HD74163	
	Mitsubishi	M53363	
	Motorola	MC74163	
	National	DM74163	
	Raytheon	74163	
	Signetics	74163	
	TI	SN74163	
	TRW	74163	
ITT74164	AMD	74164	
	Fairchild	74164	
	Hitachi	HD74164	
	Mitsubishi	M53364	
	National	DM74164	
	NEC America	μPB74164	
	Raytheon	74164	
	Signetics	74164	
	TI	SN74164	
ITT7417	Fairchild	7417	
	Hitachi	HD7417	
	Mitsubishi	M53217	
	Motorola	MC7417	
	National	DM7417	
	Signetics	7417	
	TI	SN7417	
	TRW	7417	
ITT74180	Fairchild	74180	
	Hitachi	HD74180	
	Mitsubishi	M53380	
	Motorola	MC74180	
	National	DM74180	
	NEC America	μPB74180	
	Raytheon	74180	
	Signetics	74180	
	TI	SN74180	
	TRW	74180	
ITT74182	AMD	SN74182	
	Fairchild	74182	
	Mitsubishi	M53382	
	Motorola	MC74182	
	National	DM74182	
	NEC America	μPB74182	
	Raytheon	74182	
	Signetics	74182	
	TI	SN74182	
ITT74190	Fairchild	74190	
	Hitachi	HD74190	
	Mitsubishi	M53390	
	Motorola	MC74190	
	National	DM74190	
	Raytheon	74190	
	Signetics	74190	
	TI	SN74190	
ITT74191	Fairchild	74191	
	Hitachi	HD74191	
	Mitsubishi	M53391	
	Motorola	MC74191	
	National	DM74191	
	Raytheon	74191	
	Signetics	74191	
	TI	SN74191	
ITT74192	AMD	SN74192	
	Fairchild	74192	
	Mitsubishi	M53392	
	Motorola	MC74192	
	National	DM74192	
	NEC America	μPB74192	
	Raytheon	74192	
	Signetics	74192	
	TI	SN74192	
ITT74193	AMD	SN74193	
	Fairchild	74193	
	Mitsubishi	M53393	
	Motorola	MC74193	
	National	DM74193	
	NEC America	μPB74193	
	Raytheon	74193	
	Signetics	74193	
	TI	SN74193	
ITT74194	AMD	SN74194	
	Fairchild	74194	
	Hitachi	HD74194	
	Motorola	MC74194	
	National	DM74194	
	Signetics	74194	
	TI	SN74194	
ITT74195	AMD	SN74195	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

ITT Semiconductors (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
ITT74195	Fairchild	74195	
	Motorola	MC74195	
	National	DM74195	
	NEC America	μPB74195	
	Raytheon	74195	
	Signetics	74195	
	TI	SN74195	
ITT7420	Fairchild	7420	
	Hitachi	HD7420	
	Mitsubishi	M53220	
	Motorola	MC7420	
	National	DM7420	
	NEC America	μPB7420	
	Raytheon	7420	
	Signetics	7420	
	TI	SN7420	
	Toshiba	TC7420	
	TRW	7420	
ITT7421	Fairchild	7421	
	Raytheon	7421	
	Signetics	7421	
ITT7425	Fairchild	7425	
	Mitsubishi	M53225	
	Motorola	MC7425	
	National	DM7425	
	TI	SN7425	
ITT7426	Fairchild	7426	
	Hitachi	HD7426	
	Motorola	MC7426	
	National	DM7426	
	Signetics	7426	
	TI	SN7426	
	TRW	7426	
♦ITT7428	Signetics	7428	
	TI	SN7428	
ITT7430	Fairchild	7430	
	Hitachi	HD7430	
	Mitsubishi	M53230	
	Motorola	MC7430	
	National	DM7430	
	NEC America	μPB7430	
	Signetics	7430	
	TI	SN7430	
	TRW	7430	
ITT7432	Fairchild	7432	
	Hitachi	HD7432	
	National	DM7432	
	Signetics	7432	
	TI	SN7432	
♦ITT7433	Signetics	7433	
	TI	SN7433	
ITT7437	Fairchild	7437	
	Mitsubishi	M53237	
	Motorola	MC7437	
	National	DM7437	
	NEC America	μPB7437	
	Raytheon	7437	
	Signetics	7437	
	TI	SN7437	
	TRW	7437	
ITT7438	Fairchild	7438	
	Mitsubishi	M53238	
	Motorola	MC7438	
	National	DM7438	
	NEC America	μPB7438	
	Raytheon	7438	
	Signetics	7438	
	TI	SN7438	
	TRW	7438	
ITT7440	Fairchild	7440	
	Hitachi	HD7440	
	Mitsubishi	M53240	
	Motorola	MC7440	
	National	DM7440	
	NEC America	μPB7440	
	Signetics	7440	
	TI	SN7440	
	TRW	7440	
♦ITT7441	Fairchild	7441	
	Mitsubishi	M53241	
	National	DM7441	
ITT7442	Fairchild	7442	
	Hitachi	HD7442	
ITT7442	Mitsubishi	M53242	
	Motorola	MC7442	
	National	DM7442	
	NEC America	μPB7442	
	Raytheon	7442	
	Signetics	7442	
	TI	SN7442	
ITT7443	Fairchild	7443	
	Hitachi	HD7443	
	Mitsubishi	M53243	
	Motorola	MC7443	
	Raytheon	7443	
	Signetics	7443	
	TI	SN7443	
ITT7444	Fairchild	7444	
	Hitachi	HD7444	
	Mitsubishi	M53244	
	Motorola	MC7444	
	Raytheon	7444	
	Signetics	7444	
	TI	SN7444	
ITT7445	Fairchild	7445	
	Mitsubishi	M53245	
	Motorola	MC7445	
	National	DM7445	
	NEC America	μPB7445	
	Raytheon	7445	
	Signetics	7445	
	TI	SN7445	
	TRW	7445	
ITT7446	Fairchild	7446	
	Motorola	MC7446	
	National	DM7446	
	Signetics	7446	
	TI	SN7446	
ITT7447	Fairchild	7447	
	Mitsubishi	M53247	
	Motorola	MC7447	
	National	DM7447	
	NEC America	μPB7447	
	Signetics	7447	
	TI	SN7447	
ITT7448	Fairchild	7448	
	Mitsubishi	M53248	
	Motorola	MC7448	
	National	DM7448	
	Signetics	7448	
	TI	SN7448	
ITT7450	Fairchild	7450	
	Hitachi	HD7450	
	Mitsubishi	M53250	
	Motorola	MC7450	
	National	DM7450	
	NEC America	μPB7450	
	Signetics	7450	
	TI	SN7450	
	TRW	7450	
ITT7451	Fairchild	7451	
	Hitachi	HD7451	
	Motorola	MC7451	
	National	DM7451	
	NEC America	μPB7451	
	Signetics	7451	
	TI	SN7451	
	TRW	7451	
ITT7453	Fairchild	7453	
	Hitachi	HD7453	
	Mitsubishi	M53253	
	Motorola	MC7453	
	National	DM7453	
	NEC America	μPB7453	
	Signetics	7453	
	TI	SN7453	
	TRW	7453	
ITT7454	Fairchild	7454	
	Hitachi	HD7454	
	Motorola	MC7454	
	National	DM7454	
	NEC America	μPB7454	
	Signetics	7454	
	TI	SN7454	
	TRW	7454	
♦ITT7460	Fairchild	7460	
	Hitachi	HD7460	
	Mitsubishi	M53260	
	Motorola	MC7460	
♦ITT7460	National	DM7460	
	NEC America	μPB7460	
	Signetics	7460	
	TI	SN7460	
	TRW	7460	
ITT7470	Fairchild	7470	
	Mitsubishi	M53270	
	Motorola	MC7470	
	National	DM7470	
	Signetics	7470	
	TI	SN7470	
ITT7472	Fairchild	7472	
	Hitachi	HD7472	
	Mitsubishi	M53272	
	Motorola	MC7472	
	National	DM7472	
	Signetics	7472	
	TI	SN7472	
	TRW	7472	
ITT7473	Fairchild	7473	
	Mitsubishi	M53273	
	Motorola	MC7473	
	National	DM7473	
	NEC America	μPB7473	
	Signetics	7473	
	TI	SN7473	
ITT7474	Fairchild	7474	
	Hitachi	HD7474	
	Mitsubishi	M53274	
	Motorola	MC7474	
	National	DM7474	
	NEC America	μPB7474	
	Raytheon	7474	
	Signetics	7474	
	TI	SN7474	
	TRW	7474	
ITT7475	Fairchild	7475	
	Hitachi	HD7475	
	Mitsubishi	M53275	
	Motorola	MC7475	
	National	DM7475	
	Signetics	7475	
	TI	SN7475	
	TRW	7475	
ITT7476	Fairchild	7476	
	Mitsubishi	M53276	
	Motorola	MC7476	
	National	DM7476	
	NEC America	μPB7476	
	Signetics	7476	
	TI	SN7476	
	TRW	7476	
ITT7480	Fairchild	7480	
	Mitsubishi	M53280	
	Motorola	MC7480	
	NEC America	μPB7480	
	Signetics	7480	
	TI	SN7480	
ITT7482	Fairchild	7482	
	Motorola	MC7482	
	TI	SN7482	
ITT7483	Fairchild	7483	
	Mitsubishi	M53283	
	Motorola	MC7483	
	National	DM7483	
	Raytheon	7483	
	Signetics	7483	
	TI	SN7483	
ITT7486	Fairchild	7486	
	Hitachi	HD7486	
	Mitsubishi	M53286	
	Motorola	MC7486	
	National	DM7486	
	NEC America	μPB7486	
	Raytheon	7486	
	Signetics	7486	
	TI	SN7486	
	TRW	7486	
ITT7490	Fairchild	7490	
	Hitachi	HD7490	
	Mitsubishi	M53290	
	Motorola	MC7490	
	National	DM7490	
	Signetics	7490	
	TI	SN7490	
	TRW	7490	
ITT7491	Fairchild	7491	
	Mitsubishi	M53291	
	Motorola	MC7491	
	National	DM7491	
	NEC America	μPB7491	
	Signetics	7491	
	TI	SN7491	
ITT7492	Fairchild	7492	
	Hitachi	HD7492	
	Mitsubishi	M53292	
	Motorola	MC7492	
	National	DM7492	
	Signetics	7492	
	TI	SN7492	
	TRW	7492	
ITT7493	Fairchild	7493	
	Hitachi	HD7493	
	Mitsubishi	M53293	
	Motorola	MC7493	
	National	DM7493	
	Signetics	7493	
	TI	SN7493	
	TRW	7493	
♦ITT7494	Fairchild	7494	
	Motorola	MC7494	
	TI	SN7494	
ITT7495	Fairchild	7495	
	Mitsubishi	M53295	
	Motorola	MC7495	
	National	DM7495	
	Signetics	7495	
	TI	SN7495	
ITT7496	Fairchild	7496	
	Hitachi	HD7496	
	Mitsubishi	M53296	
	Motorola	MC7496	
	National	DM7496	
	Signetics	7496	
	TI	SN7496	
	TRW	7496	
ITT75107A	TI	SN75107A	
ITT75107B	TI	SN75107B	
ITT75108A	TI	SN75108A	
ITT75108B	TI	SN75108B	
ITT75109	TI	SN75109	
ITT75110	TI	SN75110	
ITT75138	TI	SN75138	
ITT7520	TI	SN7520	
ITT75207	TI	SN75207	
ITT75208	TI	SN75208	
♦ITT7521	TI	SN7520	
ITT7522	TI	SN7522	
♦ITT7523	TI	SN7522	
ITT75234	TI	SN75234	
♦ITT75235	TI	SN75234	
ITT7524	TI	SN7524	
♦ITT7525	TI	SN7524	
ITT7528	TI	SN7528	
♦ITT7529	TI	SN7528	
ITT75322	TI	SN75322	
ITT75324	TI	SN75324	
ITT75325	TI	SN75324	
ITT75450	TI	SN75450	
ITT75451	TI	SN75451	
ITT75452	TI	SN75452	
ITT75453	TI	SN75453	
ITT75454	TI	SN75454	
ITT75460	TI	SN75460	
ITT75461	TI	SN75461	
ITT75462	TI	SN75462	
ITT75463	TI	SN75463	
ITT75464	TI	SN75464	
ITT9000	Fairchild	9000	
	TI	SN29000	
ITT9001	Fairchild	9001	
	TI	SN29001	
ITT9002	Fairchild	9002	
	TI	SN29002	
ITT9003	Fairchild	9003	
	TI	SN29003	
ITT9004	Fairchild	9004	
ITT9005	Fairchild	9005	
	TI	SN29005	
♦ITT9006	Fairchild	9006	
♦ITT9007	Fairchild	9007	
	TI	SN29007	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

ITT Semiconductors (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
ITT9008	Fairchild	9008	
	TI	SN29008	
ITT9009	Fairchild	9009	
	TI	SN29009	
ITT9016	Fairchild	9016	
	TI	SN29016	
ITT9022	Fairchild	9022	
ITT9024	Fairchild	9024	
	TI	SN29024	
♦ITT9033	Fairchild	9033	
ITT9093	Motorola	MC853	
		MC953	
	Raytheon	RM993	
	TI	SN158093	
		SN159093	
ITT9094	Motorola	MC856	
		MC956	
	Raytheon	RM994	
	TI	SN158094	
		SN159094	
ITT9097	Motorola	MC855	
		MC955	
	Raytheon	RM997	
ITT9099	Motorola	MC852	
		MC952	
	Raytheon	RM999	
	TI	SN158099	
		SN159099	
ITT930	Motorola	MC830	
		MC930	
	Raytheon	RM930	
	TI	SN15830	
		SN15930	
ITT9300	AMD	9300	
	Fairchild	9300	
	TI	SN29300	
		SN39300	
ITT9301	AMD	9301	
	Fairchild	9301	
	TI	SN29301	
		SN39301	
ITT9304	AMD	9304	
	Fairchild	9304	
ITT9309	AMD	9309	
	Fairchild	9309	
	TI	SN29309	
		SN39309	
ITT931	Motorola	MC831	
		MC931	
	TI	SN15831	
		SN15931	
ITT9312	AMD	9312	
	Fairchild	9312	
	TI	SN29312	
		SN39312	
ITT9316	AMD	9316	
	Fairchild	9316	
	Raytheon	RM9316	
	TI	SN29316	
		SN39316	
ITT932	Motorola	MC832	
		MC932	
	Raytheon	RM932	
	TI	SN15832	
		SN15932	
ITT933	Motorola	MC833	
		MC933	
	Raytheon	RM933	
	TI	SN15833	
		SN15933	
ITT935	Motorola	MC840	
		MC940	
	Raytheon	RM935	
	TI	SN15835	
		SN15935	
ITT936	Motorola	MC936	
	Raytheon	RM936	
	TI	SN15836	
		SN15936	
ITT937	Motorola	MC837	
		MC937	
	Raytheon	RM937	
	TI	SN15837	
ITT937	TI	SN15937	
ITT944	Motorola	MC844	
		MC944	
	Raytheon	RM944	
	TI	SN15844	
		SN15944	
ITT945	Motorola	MC845	
		MC945	
	Raytheon	RM945	
	TI	SN15845	
		SN15945	
ITT946	Motorola	MC846	
		MC946	
	Raytheon	RM946	
	TI	SN15846	
		SN15946	
ITT948	Motorola	MC848	
		MC948	
	Raytheon	RM948	
	TI	SN15848	
		SN15948	
ITT949	Motorola	MC849	
		MC949	
	Raytheon	RM949	
	TI	SN15849	
		SN15949	
♦ITT950	Motorola	MC850	
		MC950	
	Raytheon	RM950	
	TI	SN15850	
		SN15950	
♦ITT951	Motorola	MC851	
		MC951	
	Raytheon	RM951	
	TI	SN15851	
		SN15951	
ITT9601	AMD	9601	
	Fairchild	9601	
	TI	SN29601	
ITT961	Motorola	MC861	
		MC961	
	Raytheon	RM961	
	TI	SN15861	
		SN15961	
ITT9614	TI	SN75114	
ITT9615	TI	SN75115	
ITT962	Motorola	MC862	
		MC962	
	Raytheon	RM962	
	TI	SN15862	
		SN15962	
ITT963	Motorola	MC1141	
		MC863	
		MC963	
	Raytheon	RM963	
	TI	SN5481A	
		SN7481A	
SAA1024	SGS	M1024	
SAA1025	SGS	M1025	
TAA7756	NPC	SFC606	
TBA800	SGS	TBA800	
TCA350	AMI	S10110	
ZTK33	NPC	TAA550	

Micro Components

MCC555	Exar	XR555	

Micro Networks

DAC80	Beckman	877-80	
	Burr-Brown	DAC80	
	Datel	DAC-HZ12B	
DAC85	Beckman	877-85	
MN5065	Motorola	MC1358	

Micro Power Systems

MPS7501	AD	AD7501	
MPS7502	AD	AD7502	
MPS7503	AD	AD7503	
MPS7506	AD	AD7506	
MPS7507	AD	AD7507	
MPS7510	AD	AD7510	
MPS7511	AD	AD7511	
MPS7512	AD	AD7512	
MPS7513	AD	AD7513	
MPS7516	AD	AD7516	
	Fairchild	F4016	
	Mitel	SIL4016	
	Motorola	MC14016	
	National	CD4016	
	RCA	CD4016	
	Solitron	CM4016	
	SSS	SCL4016	
	TI	TP4016	
MPS7519	AD	AD7519	
MPS7520	AD	AD7520	
MPS7521	AD	AD7521	
MPS7522	AD	AD7522	
MPS7550	AD	AD7550	
MPS7570	AD	AD7570	

Mitel Semiconductor

SIL4000	Motorola	MC14000	
	National	CD4000	
	RCA	CD4000	
	Solitron	CM4000	
	SSS	SCL4000	
	TI	TP4000	
SIL4001	Fairchild	F4001	
	Motorola	MC14001	
	National	CD4001	
	NEC America	μPD4001	
	RCA	CD4001	
	SGS	HBF4001	
	Solitron	CM4001	
	SSS	SCL4001	
	TI	TP4001	
	Toshiba	TC4001	
SIL4002	Fairchild	F4002	
	Motorola	MC14002	
	National	CD4002	
	NEC America	μPD4002	
	RCA	CD4002	
	SGS	HBF4002	
	Solitron	CM4002	
	SSS	SCL4002	
	TI	TP4002	
	Toshiba	TC4002	
SIL4007	Fairchild	F4007	
	Motorola	MC14007	
	National	CD4007	
	RCA	CD4007	
	SGS	HBF4007	
	Solitron	CM4007	
	SSS	SCL4007	
	TI	TP4007	
	Toshiba	TC4007	
SIL4009	National	CD4009	
	RCA	CD4009	
	SGS	HBF4009	
	Solitron	CM4009	
	SSS	SCL4009	
	TI	TP4009	
	Toshiba	TC4009	
SIL4010	National	CD4010	
	RCA	CD4010	
	SGS	HBF4010	
	Solitron	CM4010	
	SSS	SCL4010	
	TI	TP4010	
	Toshiba	TC4010	
SIL4011	Fairchild	F4011	
	Motorola	MC14011	
	National	CD4011	
	NEC America	μPD4011	
	RCA	CD4011	
	SGS	HBF4011	
	Solitron	CM4011	
	SSS	SCL4011	
	TI	TP4011	
	Toshiba	TC4011	
SIL4012	Fairchild	F4012	
	Motorola	MC14012	
	National	CD4012	
	NEC America	μPD4012	
SIL4012	RCA	CD4012	
	SGS	HBF4012	
	Solitron	CM4012	
	SSS	SCL4012	
	TI	TP4012	
	Toshiba	TC4012	
SIL4013	Fairchild	F4013	
	Motorola	MC14013	
	National	CD4013	
	NEC America	μPD4013	
	RCA	CD4013	
	SGS	HBF4013	
	Solitron	CM4013	
	SSS	SCL4013	
	TI	TP4013	
	Toshiba	TC4013	
SIL4014	Fairchild	F4014	
	Motorola	MC14014	
	National	CD4014	
	NEC America	μPD4014	
	RCA	CD4014	
	SGS	HBF4014	
	Solitron	CM4014	
	SSS	SCL4014	
	TI	TP4014	
	Toshiba	TC4014	
SIL4015	Fairchild	F4015	
	Motorola	MC14015	
	National	CD4015	
	NEC America	μPD4015	
	RCA	CD4015	
	SGS	HBF4015	
	Solitron	CM4015	
	SSS	SCL4015	
	TI	TP4015	
	Toshiba	TC4015	
SIL4016	AD	AD7516	
	Fairchild	F4016	
	Micro Power	MPS7516	
	Motorola	MC14016	
	National	CD4016	
	RCA	CD4016	
	Solitron	CM4016	
	SSS	SCL4016	
	TI	TP4016	
SIL4017	Fairchild	F4017	
	Motorola	MC14017	
	National	CD4017	
	NEC America	μPD4017	
	RCA	CD4017	
	SGS	HBF4017	
	Solitron	CM4017	
	SSS	SCL4017	
	TI	TP4017	
	Toshiba	TC4017	
SIL4018	Fairchild	F4018	
	National	CD4018	
	RCA	CD4018	
	SGS	HBF4018	
	Solitron	CM4018	
	SSS	SCL4018	
	TI	TP4018	
	Toshiba	TC4018	
SIL4019	Fairchild	F4019	
	National	CD4019	
	RCA	CD4019	
	SGS	HBF4019	
	Solitron	CM4019	
	SSS	SCL4019	
	TI	TP4019	
	Toshiba	TC4019	
SIL4020	Fairchild	F4020	
	Motorola	MC14020	
	National	CD4020	
	NEC America	μPD4020	
	RCA	CD4020	
	SGS	HBF4020	
	Solitron	CM4020	
	SSS	SCL4020	
	TI	TP4020	
	Toshiba	TC4020	
SIL4021	Fairchild	F4021	
	Motorola	MC14021	
	National	CD4021	
	NEC America	μPD4021	
	RCA	CD4021	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Mitel Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
SIL4021	Solitron	CM4021	
	SSS	SCL4021	
	TI	TP4021	
	Toshiba	TC4021	
SIL4022	Fairchild	F4022	
	Motorola	MC14022	
	National	CD4022	
	RCA	CD4022	
	SGS	HBF4022	
	Solitron	CM4022	
	SSS	SCL4022	
	TI	TP4022	
	Toshiba	TC4022	
SIL4023	Fairchild	F4023	
	Motorola	MC14023	
	National	CD4023	
	NEC America	μPD4023	
	RCA	CD4023	
	SGS	HBF4023	
	Solitron	CM4023	
	SSS	SCL4023	
	TI	TP4023	
	Toshiba	TC4023	
SIL4024	Fairchild	F4024	
	Motorola	MC14024	
	National	CD4024	
	RCA	CD4024	
	SGS	HBF4024	
	Solitron	CM4024	
	SSS	SCL4024	
	TI	TP4024	
	Toshiba	TC4024	
SIL4025	Fairchild	F4025	
	Motorola	MC14025	
	National	CD4025	
	NEC America	μPD4025	
	RCA	CD4025	
	SGS	HBF4025	
	Solitron	CM4025	
	SSS	SCL4025	
	TI	TP4025	
	Toshiba	TC4025	
SIL4027	Fairchild	F4027	
	Motorola	MC14027	
	National	CD4027	
	NEC America	μPD4027	
	RCA	CD4027	
	SGS	HBF4027	
	Solitron	CM4027	
	SSS	SCL4027	
	TI	TP4027	
	Toshiba	TC4027	
SIL4028	Fairchild	F4028	
	Motorola	MC14028	
	National	CD4028	
	NEC America	μPD4028	
	RCA	CD4028	
	SGS	HBF4028	
	Solitron	CM4028	
	SSS	SCL4028	
	TI	TP4028	
	Toshiba	TC4028	
SIL4029	Fairchild	F4029	
	National	CD4029	
	NEC America	μPD4029	
	RCA	CD4029	
	SGS	HBF4029	
	Solitron	CM4029	
	SSS	SCL4029	
	TI	TP4029	
	Toshiba	TC4029	
SIL4030	Fairchild	F4030	
	National	CD4030	
	NEC America	μPD4030	
	RCA	CD4030	
	SGS	HBF4030	
	Solitron	CM4030	
	SSS	SCL4030	
	TI	TP4030	
	Toshiba	TC4030	
SIL4035	Fairchild	F4035	
	Motorola	MC14035	
	National	CD4035	
SIL4035	NEC America	μPD4035	
	RCA	CD4035	
	SGS	HBF4035	
	Solitron	CM4035	
	SSS	SCL4035	
	TI	TP4035	
	Toshiba	TC4035	
SIL4040	Fairchild	F4040	
	National	CD4040	
	NEC America	μPD4040	
	RCA	CD4040	
	Solitron	CM4040	
	SSS	SCL4040	
	TI	TP4040	
	Toshiba	TC4040	
SIL4042	Fairchild	F4042	
	Motorola	MC14042	
	National	CD4042	
	NEC America	μPD4042	
	RCA	CD4042	
	SGS	HBF4042	
	Solitron	CM4042	
	SSS	SCL4042	
	TI	TP4042	
	Toshiba	TC4042	
SIL4043	Fairchild	F4043	
	Motorola	MC14043	
	National	CD4043	
	NEC America	μPD4043	
	RCA	CD4043	
	Solitron	CM4043	
	SSS	SCL4043	
	TI	TP4043	
	Toshiba	TC4043	
SIL4044	Fairchild	F4044	
	Motorola	MC14044	
	National	CD4044	
	NEC America	μPD4044	
	RCA	CD4044	
	Solitron	CM4044	
	SSS	SCL4044	
	TI	TP4044	
	Toshiba	TC4044	
SIL4046	Fairchild	F4046	
	Motorola	MC14046	
	National	CD4046	
	RCA	CD4046	
	Solitron	CM4046	
	SSS	SCL4046	
SIL4049	Fairchild	F4049	
	Motorola	MC14049	
	National	CD4049	
	NEC America	μPD4049	
	RCA	CD4049	
	SGS	HBF4049	
	Solitron	CM4049	
	SSS	SCL4049	
	TI	TP4049	
	Toshiba	TC4049	
SIL4050	Fairchild	F4050	
	Motorola	MC14050	
	National	CD4050	
	NEC America	μPD4050	
	RCA	CD4050	
	SGS	HBF4050	
	Solitron	CM4050	
	SSS	SCL4050	
	TI	TP4050	
	Toshiba	TC4050	
SIL4051	Fairchild	F4051	
	Motorola	MC14051	
	National	CD4051	
	RCA	CD4051	
	Solitron	CM4051	
	SSS	SCL4051	
	TI	TP4051	
	Toshiba	TC4051	
SIL4052	Fairchild	F4052	
	Motorola	MC14052	
	National	CD4052	
	RCA	CD4052	
	Solitron	CM4052	
	SSS	SCL4052	
	TI	TP4052	
	Toshiba	TC4052	
SIL4053	Fairchild	F4053	
SIL4053	Motorola	MC14053	
	National	CD4053	
	RCA	CD4053	
	Solitron	CM4053	
	SSS	SCL4053	
	Toshiba	TC4053	
SIL4055	RCA	CD4055	
SIL4056	RCA	CD4056	
SIL4060	National	CD4060	
	RCA	CD4060	
	SSS	SCL4060	
SIL4066	Fairchild	F4066	
	Motorola	MC14066	
	National	CD4066	
	NEC America	μPD4066	
	RCA	CD4066	
	SGS	HBF4066	
	Signetics	N4066	
	Solitron	CM4066	
	SSS	SCL4066	
	Toshiba	TC4066	
SIL4068	Fairchild	F4068	
	Motorola	MC14068	
	RCA	CD4068	
	Solitron	CM4068	
	SSS	SCL4068	
	TI	TP4068	
	Toshiba	TC4068	
SIL4069	Fairchild	F4069	
	Harris	HD74C04	
	Motorola	MC14069	
	National	CD4069	
		MM74C04	
	NEC America	μPD4069	
	RCA	CD4069	
	Solitron	CM4069	
	SSS	SCL4069	
	TI	TP4069	
	Toshiba	TC4069	
SIL4070	Fairchild	F4070	
	National	CD4070	
		MM74C86	
	RCA	CD4070	
	Solitron	CM4070	
	SSS	SCL4070	
SIL4071	Fairchild	F4071	
	Motorola	MC14071	
	National	CD4071	
	NEC America	μPD4071	
	RCA	CD4071	
	Solitron	CM4071	
	SSS	SCL4071	
	TI	TP4071	
	Toshiba	TC4071	
SIL4072	Fairchild	F4072	
	Motorola	MC14072	
	RCA	CD4072	
	SSS	SCL4072	
	TI	TP4072	
	Toshiba	TC4072	
SIL4073	Fairchild	F4073	
	Motorola	MC14073	
	National	CD4073	
	RCA	CD4073	
	Solitron	CM4073	
	SSS	SCL4073	
	TI	TP4073	
	Toshiba	TC4073	
SIL4075	Fairchild	F4075	
	Motorola	MC14075	
	National	CD4075	
	RCA	CD4075	
	SSS	SCL4075	
	TI	TP4075	
	Toshiba	TC4075	
SIL4076	Fairchild	F4076	
	Harris	HD74C173	
	Motorola	MC14076	
	National	CD4076	
		MM74C173	
	RCA	CD4076	
	Solitron	CM4076	
	SSS	SCL4076	
SIL4077	Fairchild	F4077	
	Motorola	MC14077	
	RCA	CD4077	
SIL4077	Solitron	CM4077	
	SSS	SCL4077	
SIL4078	Fairchild	F4078	
	Motorola	MC14078	
	RCA	CD4078	
	Solitron	CM4078	
	SSS	SCL4078	
	Toshiba	TC4078	
SIL4081	Fairchild	F4081	
	Motorola	MC14081	
	National	CD4081	
	NEC America	μPD4081	
	RCA	CD4081	
	Solitron	CM4081	
	SSS	SCL4081	
	TI	TP4081	
	Toshiba	TC4081	
SIL4082	Fairchild	F4082	
	Motorola	MC14082	
	RCA	CD4082	
	SSS	SCL4082	
	TI	TP4082	
	Toshiba	TC4082	
SIL4098	RCA	CD4098	
SIL4502	Motorola	MC14502	
	RCA	CD4502	
	SSS	SCL4502	
SIL4508	Motorola	MC14508	
	RCA	CD4508	
	SSS	SCL4508	
	Toshiba	TC4508	
SIL4510	Fairchild	F4510	
	Motorola	MC14510	
	National	CD4510	
	RCA	CD40192	
		CD4510	
	SSS	SCL4510	
	Toshiba	TC4510	
SIL4511	Fairchild	F4511	
	Motorola	MC14511	
	National	CD4511	
	RCA	CD4511	
	Solitron	CM4511	
	SSS	SCL4511	
	TI	TP4511	
SIL4512	Fairchild	F4512	
	Motorola	MC14512	
	National	CD4512	
	NEC America	μPD4512	
	SSS	SCL4512	
	TI	TP4512	
	Toshiba	TC4512	
SIL4514	Fairchild	F4514	
	Motorola	MC14514	
	National	CD4514	
	RCA	CD4514	
	Solitron	CM4514	
	SSS	SCL4514	
	Toshiba	TC4514	
SIL4515	Fairchild	F4515	
	Motorola	MC14515	
	National	CD4515	
	RCA	CD4515	
	Solitron	CM4515	
	SSS	SCL4515	
	Toshiba	TC4515	
SIL4516	Fairchild	F4516	
	Motorola	MC14516	
	National	CD4516	
	RCA	CD40193	
		CD4516	
	SSS	SCL4516	
	Toshiba	TC4516	
SIL4518	Fairchild	F4518	
	Motorola	MC14518	
	National	CD4518	
	RCA	CD4518	
	Solitron	CM4518	
	SSS	SCL4518	
	TI	TP4518	
	Toshiba	TC4518	
SIL4520	Fairchild	F4520	
	Motorola	MC14520	
	National	CD4520	
	NEC America	μPD4520	
	RCA	CD4520	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Mitel Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
SIL4520	Solitron	CM4520	
	SSS	SCL4520	
	TI	TP4520	
	Toshiba	TC4520	

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Manufacturer Device	Replacement Source	Device	IC Master Page
M5S000	Fairchild	74S00	
	Hitachi	HD74S00	
	National	DM74S00	
	Signetics	74S00	
	TI	SN74S00	
M5S003	Fairchild	74S03	
	Hitachi	HD74S03	
	National	DM74S03	
	Signetics	74S03	
	TI	SN74S03	
M5S004	Fairchild	74S04	
	Hitachi	HD74S04	
	National	DM74S04	
	Signetics	74S04	
	TI	SN74S04	
M5S005	Fairchild	74S05	
	Hitachi	HD74S05	
	National	DM74S05	
	Signetics	74S05	
	TI	SN74S05	
M5S010	Fairchild	74S10	
	Hitachi	HD74S10	
	National	DM74S10	
	Signetics	74S10	
	TI	SN74S10	
M5S011	Fairchild	74S11	
	Hitachi	HD74S11	
	National	DM74S11	
	Signetics	74S11	
	TI	SN74S11	
M5S015	Fairchild	74S15	
	Hitachi	HD74S15	
	National	DM74S15	
	Signetics	74S15	
	TI	SN74S15	
M5S020	Fairchild	74S20	
	Hitachi	HD74S20	
	National	DM74S20	
	Signetics	74S20	
	TI	SN74S20	
M5S030	Fairchild	74S30	
	National	DM74S30	
	TI	SN74S30	
M5S040	Fairchild	74S40	
	Hitachi	HD74S40	
	National	DM74S40	
	Signetics	74S40	
	TI	SN74S40	
M5S051	Fairchild	74S51	
	National	DM74S51	
	Signetics	74S51	
	TI	SN74S51	
M5S074	Fairchild	74S74	
	Hitachi	HD74S74	
	TI	SN74S74	
M5S085	Signetics	74S85	
	TI	SN74S85	
M5S112	Fairchild	74S112	
	Hitachi	HD74S112	
	Motorola	SN74S112	
	National	DM74S112	
	Signetics	74S112	
	TI	SN74S112	
M5S113	Fairchild	74S113	
	Hitachi	HD74S113	
	Motorola	SN74S113	
	National	DM74S113	
	Signetics	74S113	
	TI	SN74S113	
M5S114	Fairchild	74S114	
	Hitachi	HD74S114	
	National	DM74S114	
	Signetics	74S114	
	TI	SN74S114	
M5S133	Fairchild	74S133	
M5S133	Hitachi	HD74S133	
	National	DM74S133	
	Signetics	74S133	
	TI	SN74S133	
M5S138	AMD	SN74S138	
	Fairchild	74S138	
	National	DM74S138	
	Signetics	74S138	
	TI	SN74S138	
M5S151	AMD	SN74S151	
	Fairchild	74S151	
	Hitachi	HD74S151	
	National	DM74S151	
	Signetics	74S151	
	TI	SN74S151	
M5S153	AMD	SN74S153	
	Fairchild	74S153	
	National	DM74S153	
	Signetics	74S153	
	TI	SN74S153	
M5S157	AMD	SN74S157	
	Fairchild	74S157	
	National	DM74S157	
	Signetics	74S157	
	TI	SN74S157	
M5S158	AMD	SN74S158	
	Fairchild	74S158	
	National	DM74S158	
	Signetics	74S158	
	TI	SN74S158	
M5S174	AMD	SN74S174	
	Fairchild	74S174	
	Hitachi	HD74S174	
	National	DM74S174	
	Signetics	74S174	
	TI	SN74S174	
M5S175	AMD	SN74S175	
	Fairchild	74S175	
	Hitachi	HD74S175	
	National	DM74S175	
	Signetics	74S175	
	TI	SN74S175	
M5S181	AMD	SN74S181	
	Fairchild	74S181	
	Hitachi	HD74S181	
	Signetics	74S181	
	TI	SN74S181	
M5S182	Fairchild	74S182	
	National	DM74S182	
	Signetics	74S182	
	TI	SN74S182	
M5S22	Fairchild	74S22	
	Hitachi	HD74S22	
	National	DM74S22	
	Signetics	74S22	
	TI	SN74S22	
M5S251	AMD	SN74S251	
	Fairchild	74S251	
	Hitachi	HD74S251	
	National	DM74S251	
	Signetics	74S251	
	TI	SN74S251	
M5S257	AMD	SN74S257	
	Fairchild	74S257	
	National	DM74S257	
	Signetics	74S257	
	TI	SN74S257	
M5S258	AMD	SN74S258	
	Fairchild	74S258	
	Signetics	74S258	
	TI	SN74S258	
M53200	Fairchild	7400	
	Hitachi	HD7400	
	ITT	ITT7400	
	Motorola	MC7400	
	National	DM7400	
	NEC America	μPB7400	
	Raytheon	7400	
	Signetics	7400	
	TI	SN7400	
	Toshiba	TC7400	
	TRW	7400	
M53201	Fairchild	7401	
	ITT	ITT7401	
	Motorola	MC7401	
	National	DM7401	
M53201	Raytheon	7401	
	Signetics	7401	
	TI	SN7401	
	TRW	7401	
M53202	Fairchild	7402	
	Hitachi	HD7402	
	ITT	ITT7402	
	Motorola	MC7402	
	National	DM7402	
	NEC America	μPB7402	
	Signetics	7402	
	TI	SN7402	
	TRW	7402	
M53203	Fairchild	7403	
	Hitachi	HD7403	
	ITT	ITT7403	
	Motorola	MC7403	
	National	DM7403	
	Raytheon	7403	
	Signetics	7403	
	TI	SN7403	
	TRW	7403	
M53204	Fairchild	7404	
	Hitachi	HD7404	
	ITT	ITT7404	
	Motorola	MC7404	
	National	DM7404	
	NEC America	μPB7404	
	Raytheon	7404	
	Signetics	7404	
	TI	SN7404	
	Toshiba	TC7404	
	TRW	7404	
M53205	Fairchild	7405	
	Hitachi	HD7405	
	ITT	ITT7405	
	Motorola	MC7405	
	National	DM7405	
	NEC America	μPB7405	
	Raytheon	7405	
	Signetics	7405	
	TI	SN7405	
	TRW	7405	
M53206	Fairchild	7406	
	Hitachi	HD7406	
	ITT	ITT7406	
	Motorola	MC7406	
	National	DM7406	
	Signetics	7406	
	TI	SN7406	
	TRW	7406	
M53207	Fairchild	7407	
	Hitachi	HD7407	
	ITT	ITT7407	
	Motorola	MC7407	
	National	DM7407	
	Signetics	7407	
	TI	SN7407	
	TRW	7407	
M53208	Fairchild	7408	
	ITT	ITT7408	
	Motorola	MC7408	
	National	DM7408	
	Raytheon	7408	
	Signetics	7408	
	TI	SN7408	
	Toshiba	TC7408	
	TRW	7408	
M53209	Fairchild	7409	
	Hitachi	HD7409	
	ITT	ITT7409	
	Motorola	MC7409	
	National	DM7409	
	Raytheon	7409	
	Signetics	7409	
	TI	SN7409	
	TRW	7409	
M53210	Fairchild	7410	
	Hitachi	HD7410	
	ITT	ITT7410	
	Motorola	MC7410	
	National	DM7410	
	NEC America	μPB7410	
	Raytheon	7410	
	Signetics	7410	
	TI	SN7410	
M53210	TI	SN7427	
	Toshiba	TC7410	
	TRW	7410	
M53213	Fairchild	7413	
	ITT	ITT7413	
	Motorola	MC7413	
	National	DM7413	
	NEC America	μPB7413	
	Signetics	7413	
	TI	SN7413	
	TRW	7413	
M53214	Fairchild	7414	
	Hitachi	HD7414	
	Motorola	MC7414	
	National	DM7414	
	Signetics	7414	
	TI	SN7414	
M53216	Fairchild	7416	
	Hitachi	HD7416	
	ITT	ITT7416	
	Motorola	MC7416	
	National	DM7416	
	Signetics	7416	
	TI	SN7416	
	TRW	7416	
M53217	Fairchild	7417	
	Hitachi	HD7417	
	ITT	ITT7417	
	Motorola	MC7417	
	National	DM7417	
	Signetics	7417	
	TI	SN7417	
	TRW	7417	
M53220	Fairchild	7420	
	Hitachi	HD7420	
	ITT	ITT7420	
	Motorola	MC7420	
	National	DM7420	
	NEC America	μPB7420	
	Raytheon	7420	
	Signetics	7420	
	TI	SN7420	
	Toshiba	TC7420	
	TRW	7420	
M53225	Fairchild	7425	
	ITT	ITT7425	
	Motorola	MC7425	
	National	DM7425	
	TI	SN7425	
M53227	Fairchild	7427	
	Hitachi	HD7427	
	Motorola	MC7427	
	National	DM7427	
	Signetics	7427	
M53230	Fairchild	7430	
	Hitachi	HD7430	
	ITT	ITT7430	
	Motorola	MC7430	
	National	DM7430	
	NEC America	μPB7430	
	Signetics	7430	
	TI	SN7430	
	TRW	7430	
M53237	Fairchild	7437	
	ITT	ITT7437	
	Motorola	MC7437	
	National	DM7437	
	NEC America	μPB7437	
	Raytheon	7437	
	Signetics	7437	
	TI	SN7437	
	TRW	7437	
M53238	Fairchild	7438	
	ITT	ITT7438	
	Motorola	MC7438	
	National	DM7438	
	NEC America	μPB7438	
	Raytheon	7438	
	Signetics	7438	
	TI	SN7438	
	TRW	7438	
M53240	Fairchild	7440	
	Hitachi	HD7440	
	ITT	ITT7440	
	Motorola	MC7440	
	National	DM7440	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
M53240	NEC America	μPB7440	
	Signetics	7440	
	TI	SN7440	
	TRW	7440	
M53241	Fairchild	7441	
	National	DM7441	
M53242	Fairchild	7442	
	Hitachi	HD7442	
	ITT	ITT7442	
	Motorola	MC7442	
	National	DM7442	
	NEC America	μPB7442	
	Raytheon	7442	
	Signetics	7442	
	TI	SN7442	
M53243	Fairchild	7443	
	Hitachi	HD7443	
	ITT	ITT7443	
	Motorola	MC7443	
	Raytheon	7443	
	Signetics	7443	
	TI	SN7443	
M53244	Fairchild	7444	
	Hitachi	HD7444	
	ITT	ITT7444	
	Motorola	MC7444	
	Raytheon	7444	
	Signetics	7444	
	TI	SN7444	
M53245	Fairchild	7445	
	ITT	ITT7445	
	Motorola	MC7445	
	National	DM7445	
	NEC America	μPB7445	
	Raytheon	7445	
	Signetics	7445	
	TI	SN7445	
	TRW	7445	
M53247	Fairchild	7447	
	ITT	ITT7447	
	Motorola	MC7447	
	National	DM7447	
	NEC America	μPB7447	
	Signetics	7447	
	TI	SN7447	
M53248	Fairchild	7448	
	ITT	ITT7448	
	Motorola	MC7448	
	National	DM7448	
	Signetics	7448	
	TI	SN7448	
M53250	Fairchild	7450	
	Hitachi	HD7450	
	ITT	ITT7450	
	Motorola	MC7450	
	National	DM7450	
	NEC America	μPB7450	
	Signetics	7450	
	TI	SN7450	
	TRW	7450	
M53253	Fairchild	7453	
	Hitachi	HD7453	
	ITT	ITT7453	
	Motorola	MC7453	
	National	DM7453	
	NEC America	μPB7453	
	Signetics	7453	
	TI	SN7453	
	TRW	7453	
M53260	Fairchild	7460	
	Hitachi	HD7460	
	Motorola	MC7460	
	National	DM7460	
	NEC America	μPB7460	
	Signetics	7460	
	TI	SN7460	
	TRW	7460	
M53270	Fairchild	7470	
	ITT	ITT7470	
	Motorola	MC7470	
	National	DM7470	
	Signetics	7470	
M53270	TI	SN7470	
M53272	Fairchild	7472	
	Hitachi	HD7472	
	ITT	ITT7472	
	Motorola	MC7472	
	National	DM7472	
	Signetics	7472	
	TI	SN7472	
	TRW	7472	
M53273	Fairchild	7473	
	ITT	ITT7473	
	Motorola	MC7473	
	National	DM7473	
	NEC America	μPB7473	
	Signetics	7473	
	TI	SN7473	
M53274	Fairchild	7474	
	Hitachi	HD7474	
	ITT	ITT7474	
	Motorola	MC7474	
	National	DM7474	
	NEC America	μPB7474	
	Raytheon	7474	
	Signetics	7474	
	TI	SN7474	
	TRW	7474	
M53275	Fairchild	7475	
	Hitachi	HD7475	
	ITT	ITT7475	
	Motorola	MC7475	
	National	DM7475	
	Signetics	7475	
	TI	SN7475	
	TRW	7475	
M53276	Fairchild	7476	
	ITT	ITT7476	
	Motorola	MC7476	
	National	DM7476	
	NEC America	μPB7476	
	Signetics	7476	
	TI	SN7476	
	TRW	7476	
M53280	Fairchild	7480	
	ITT	ITT7480	
	Motorola	MC7480	
	NEC America	μPB7480	
	Signetics	7480	
	TI	SN7480	
M53283	Fairchild	7483	
	ITT	ITT7483	
	Motorola	MC7483	
	National	DM7483	
	Raytheon	7483	
	Signetics	7483	
	TI	SN7483	
M53285	Fairchild	7485	
	Hitachi	HD7485	
	Motorola	MC7485	
	National	DM7485	
	NEC America	μPB7485	
	Signetics	7485	
	TI	SN7485	
	TRW	7485	
M53286	Fairchild	7486	
	Hitachi	HD7486	
	ITT	ITT7486	
	Motorola	MC7486	
	National	DM7486	
	NEC America	μPB7486	
	Raytheon	7486	
	Signetics	7486	
	TI	SN7486	
	TRW	7486	
M53289	AMD	SN7489	
	Fairchild	7489	
	National	**DM7489**	**1287**
	TI	SN7489	
	TRW	7489	
M53290	Fairchild	7490	
	Hitachi	HD7490	
	ITT	ITT7490	
	Motorola	MC7490	
	National	DM7490	
	Signetics	7490	
	TI	SN7490	
	TRW	7490	
M53291	Fairchild	7491	
	ITT	ITT7491	
	Motorola	MC7491	
	National	DM7491	
	NEC America	μPB7491	
	Signetics	7491	
	TI	SN7491	
M53292	Fairchild	7492	
	Hitachi	HD7492	
	ITT	ITT7492	
	Motorola	MC7492	
	National	DM7492	
	Signetics	7492	
	TI	SN7492	
	TRW	7492	
M53293	Fairchild	7493	
	Hitachi	HD7493	
	ITT	ITT7493	
	Motorola	MC7493	
	National	DM7493	
	Signetics	7493	
	TI	SN7493	
	TRW	7493	
M53295	Fairchild	7495	
	ITT	ITT7495	
	Motorola	MC7495	
	National	DM7495	
	Signetics	7495	
	TI	SN7495	
M53296	Fairchild	7496	
	Hitachi	HD7496	
	ITT	ITT7496	
	Motorola	MC7496	
	National	DM7496	
	Signetics	7496	
	TI	SN7496	
	TRW	7496	
M53307	Fairchild	74107	
	Hitachi	HD74107	
	ITT	ITT74107	
	Motorola	MC74107	
	National	DM74107	
	NEC America	μPB74107	
	Signetics	74107	
	TI	SN74107	
M53321	Fairchild	74121	
	Hitachi	HD74121	
	ITT	ITT74121	
	Motorola	MC74121	
	National	DM74121	
	Signetics	74121	
	TI	SN74121	
	TRW	74121	
M53322	Fairchild	74122	
	ITT	ITT74122	
	Motorola	MC74122	
	Signetics	74122	
	TI	SN74122	
M53323	AMD	SN74123	
	Fairchild	74123	
	ITT	ITT74123	
	Motorola	MC74123	
	National	DM74123	
	NEC America	μPB74123	
	Raytheon	74123	
	Signetics	74123	
	TI	SN74123	
	TRW	74123	
M53325	Fairchild	74125	
	Hitachi	HD74125	
	National	DM74125	
	Signetics	74125	
	TI	SN74125	
M53326	Fairchild	74126	
	Hitachi	HD74126	
	National	DM74126	
	Signetics	74126	
	TI	SN74126	
M53332	Fairchild	74132	
	Hitachi	HD74132	
	Motorola	MC74132	
	National	DM74132	
	Signetics	74132	
	TI	SN74132	
M53345	Fairchild	74145	
	ITT	ITT74145	
M53345	Motorola	MC74145	
	National	DM74145	
	Raytheon	74145	
	Signetics	74145	
	TI	SN74145	
	TRW	74145	
M53347	Hitachi	HD74147	
	National	DM74147	
	NEC America	μPB74147	
	Signetics	74147	
	TI	SN74147	
M53348	Hitachi	HD74148	
	National	DM74148	
	NEC America	μPB74148	
	Signetics	74148	
	TI	SN74148	
M53350	Fairchild	74150	
	Hitachi	HD74150	
	Motorola	MC74150	
	National	DM74150	
	NEC America	μPB74150	
	Raytheon	74150	
	Signetics	74150	
	TI	SN74150	
	TRW	74150	
M53351	Fairchild	74151	
	Hitachi	HD74151	
	ITT	ITT74151	
	Motorola	MC74151	
	National	DM74151	
	NEC America	μPB74151	
	Raytheon	74151	
	Signetics	74151	
	TI	SN74151	
	TRW	74151	
M53353	Fairchild	74153	
	ITT	ITT74153	
	Motorola	MC74153	
	National	DM74153	
	NEC America	μPB74153	
	Raytheon	74153	
	Signetics	74153	
	TI	SN74153	
	TRW	74153	
M53354	AMD	SN74154	
	Fairchild	74154	
	Motorola	MC74154	
	National	DM74154	
	NEC America	μPB74154	
	Raytheon	74154	
	Signetics	74154	
	TI	SN74154	
	TRW	74154	
M53355	Fairchild	74155	
	ITT	ITT74155	
	Motorola	MC74155	
	National	DM74155	
	NEC America	μPB74155	
	Raytheon	74155	
	Signetics	74155	
	TI	SN74155	
	TRW	74155	
M53356	Fairchild	74156	
	Hitachi	HD74156	
	ITT	ITT74156	
	Motorola	MC74156	
	National	DM74156	
	NEC America	μPB74156	
	Raytheon	74156	
	Signetics	74156	
	TI	SN74156	
	TRW	74156	
M53357	AMD	SN74157	
	Fairchild	74157	
	Hitachi	HD74157	
	ITT	ITT74157	
	Motorola	MC74157	
	National	DM74157	
	NEC America	μPB74157	
	Raytheon	74157	
	Signetics	74157	
	TI	SN74157	
M53358	Raytheon	74158	
	Signetics	74158	
M53360	AMD	SN74160	
	Fairchild	74160	

◆ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
M53360	Hitachi	HD74160	
	ITT	ITT74160	
	Motorola	MC74160	
	National	DM74160	
	Raytheon	74160	
	Signetics	74160	
	TI	SN74160	
	TRW	74160	
M53361	AMD	SN74161	
	Fairchild	74161	
	Hitachi	HD74161	
	ITT	ITT74161	
	Motorola	MC74161	
	National	DM74161	
	NEC America	μPB74161	
	Raytheon	74161	
	Signetics	74161	
	TI	SN74161	
	TRW	74161	
M53362	AMD	SN74162	
	Fairchild	74162	
	Hitachi	HD74162	
	ITT	ITT74162	
	Motorola	MC74162	
	National	DM74162	
	Raytheon	74162	
	Signetics	74162	
	TI	SN74162	
	TRW	74162	
M53363	AMD	SN74163	
	Fairchild	74163	
	Hitachi	HD74163	
	ITT	ITT74163	
	Motorola	MC74163	
	National	DM74163	
	Raytheon	74163	
	Signetics	74163	
	TI	SN74163	
	TRW	74163	
M53364	AMD	74164	
	Fairchild	74164	
	Hitachi	HD74164	
	ITT	ITT74164	
	National	DM74164	
	NEC America	μPB74164	
	Raytheon	74164	
	Signetics	74164	
	TI	SN74164	
M53365	Fairchild	74165	
	Motorola	MC74165	
	National	DM74165	
	Raytheon	74165	
	Signetics	74165	
	TI	SN74165	
M53366	Fairchild	74166	
	Hitachi	HD74166	
	National	DM74166	
	Raytheon	74166	
	Signetics	74166	
	TI	SN74166	
M53370	Fairchild	74170	
	National	DM74170	
	NEC America	μPB74170	
	Raytheon	74170	
	Signetics	74170	
	TI	SN74170	
M53374	AMD	SN74174	
	Fairchild	74174	
	Hitachi	HD74174	
	Motorola	MC74174	
	National	DM74174	
	Raytheon	74174	
	Signetics	74174	
	TI	SN74174	
M53375	AMD	SN74175	
	Fairchild	74175	
	Hitachi	HD74175	
	Motorola	MC74175	
	National	DM74175	
	NEC America	μPB74175	
	Raytheon	74175	
	Signetics	74175	
M53375	TI	SN74175	
M53376	Fairchild	74176	
	Motorola	MC74176	
	National	DM74176	
	Signetics	74176	
	TI	SN74176	
M53377	Fairchild	74177	
	Motorola	MC74177	
	National	DM74177	
	Signetics	74177	
	TI	SN74177	
M53380	Fairchild	74180	
	Hitachi	HD74180	
	ITT	ITT74180	
	Motorola	MC74180	
	National	DM74180	
	NEC America	μPB74180	
	Raytheon	74180	
	Signetics	74180	
	TI	SN74180	
	TRW	74180	
M53381	AMD	SN74181	
	Fairchild	74181	
	Motorola	MC74181	
	National	DM74181	
	NEC America	μPB74181	
	Raytheon	74181	
	Signetics	74181	
	TI	SN74181	
M53382	AMD	SN74182	
	Fairchild	74182	
	ITT	ITT74182	
	Motorola	MC74182	
	National	DM74182	
	NEC America	μPB74182	
	Raytheon	74182	
	Signetics	74182	
	TI	SN74182	
M53385	National	DM74185	
	TI	SN74185	
M53390	Fairchild	74190	
	Hitachi	HD74190	
	ITT	ITT74190	
	Motorola	MC74190	
	National	DM74190	
	Raytheon	74190	
	Signetics	74190	
	TI	SN74190	
M53391	Fairchild	74191	
	Hitachi	HD74191	
	ITT	ITT74191	
	Motorola	MC74191	
	National	DM74191	
	Raytheon	74191	
	Signetics	74191	
	TI	SN74191	
M53392	AMD	SN74192	
	Fairchild	74192	
	ITT	ITT74192	
	Motorola	MC74192	
	National	DM74192	
	NEC America	μPB74192	
	Raytheon	74192	
	Signetics	74192	
	TI	SN74192	
M53393	AMD	SN74193	
	Fairchild	74193	
	ITT	ITT74193	
	Motorola	MC74193	
	National	DM74193	
	NEC America	μPB74193	
	Raytheon	74193	
	Signetics	74193	
	TI	SN74193	
M53398	Fairchild	74198	
	Hitachi	HD74198	
	National	DM74198	
	NEC America	μPB74198	
	Raytheon	74198	
	Signetics	74198	
	TI	SN74198	
M53399	Fairchild	74199	
	National	DM74199	
	Raytheon	74199	
	Signetics	74199	
	TI	SN74199	
M53478	TI	SN74278	
M53483	Fairchild	74283	
	NEC America	μPB74283	
	Raytheon	74283	
	TI	SN74283	
M53490	Fairchild	74290	
	Motorola	MC74290	
	TI	SN74290	
	TRW	74290	
M53493	Fairchild	74293	
	Motorola	MC74293	
	TI	SN74293	
	TRW	74293	

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Manufacturer Device	Replacement Source	Device	IC Master Page
♦A5280	AMD	AM27S80	
♦A5281	AMD	AM27S81	
♦A6280	AMD	AM27S80	
♦A6281	AMD	AM27S81	
♦H5201	TI	SN54S287	
♦H6201	TI	SN74S287	
♦L5560	AMD	31L01	
	National	DM54LS289	
		DM54L89	
		DM54L89A	
♦L5561	National	DM76L99	
♦L6560	AMD	31L01	
	National	DM74L89	
♦L6561	**National**	**DM74S189**	**1292**
		DM86L89	
5200	Fairchild	93416	
	Intersil	IM5603	
	Signetics	82S226	
	TI	SN54187	
5200-1	Fairchild	93457	
	Intel	3301A	
	National	**DM54S189**	**1292**
	Signetics	82S226	
	TI	SN54187	
5201	Intersil	IM5623	
	Signetics	82S299	
	TI	SN54S387	
5201-1	Fairchild	93467	
	National	DM75S97	
	Signetics	82S299	
5205	Intersil	IM5604	
	TI	SN54S270	
5205-1	Fairchild	93431	
	National	**DM54S270**	**1279**
	Signetics	82S230	
	TI	SN54S270	
5206	TI	SN54S370	
5206-1	Fairchild	93441	
	National	**DM54S370**	**1279**
	Signetics	82S231	
	TI	SN54S370	
5230	Intersil	IM5600	
	National	DM5488	
	TI	SN5488A	
5230-1	National	DM5488	
5231	Intersil	IM5610	
	TI	SN54S188	
5231-1	National	DM7598	
5240-1	Fairchild	93432	
	National	**DM77S95**	**1281**
5241-1	Fairchild	93442	
	National	**DM77S96**	**1281**
5275-1	Signetics	82S291	
		87S290	
5280-1	Fairchild	93454	
	National	DM87S29	
	Signetics	82S280	
5280-2	Fairchild	93454	
5281-1	Fairchild	93464	
	National	DM87S29	
	Signetics	82S281	
5281-2	Fairchild	93464	
5300	**Fairchild**	**93417**	**1151**
	Harris	HPROM1024A	
	Intel	M3601	
	Intersil	IM5603	
	National	**DM54S387**	**1264**
	NEC Micro	μPD403	
	Signetics	82S126	
5300	TI	SN54S387	
5300-1	AMD	AM29S10	
		AM29760	
	Fairchild	**93417**	**1151**
	Harris	**HM7610-2**	**1192**
	Intel	M3601	
	Intersil	IM5603	
	National	**DM54S387**	**1264**
	Signetics	82S126	
	TI	SN54S387	
5301	Harris	HPROM1024	
	Intersil	IM5623	
	National	DM54S281	
	Signetics	82S129	
	TI	SN54S287	
5301-1	AMD	AM29S11	
		AM29761	
	Fairchild	**93427**	**1151**
	Harris	**HM7611-2**	**1192**
	Intel	3621	
	Intersil	IM5623	
	National	**DM54S287**	**1264**
	Signetics	82S129	
	TI	SN54S287	
5305	**Fairchild**	**93436**	**1151**
	Harris	**HM7620**	**1192**
		HM7620A	**1202**
	Intersil	IM5604	
	National	**DM54S571**	**1266**
	Signetics	82S130	
	TI	SN54S270	
5305-1	AMD	AM27S12	
		AM29770	
	Fairchild	**93436**	**1151**
	Harris	**HM7620-2**	**1192**
	Intel	3602	
	Intersil	IM5604	
	National	DM54S570	
	Signetics	82S130	
5306	**Fairchild**	**93446**	**1151**
	Harris	**HM7621**	**1192**
		HM7621A	**1202**
	Intersil	IM5624	
	National	**DM54S571**	**1266**
	Signetics	S82S131	
	TI	SN54S370	
5306-1	AMD	AM27S13	
		AM29771	
	Fairchild	**93446**	**1151**
	Harris	**HM7621-2**	**1192**
	Intel	3622	
	Intersil	IM5624	
	National	**DM54S571**	**1266**
	Signetics	82S131	
5308	TI	SN54S470	
5308-1	National	DM54S470	
	TI	SN54S470	
5309	TI	SN54S471	
5309-1	National	DM54S471	
	TI	SN54S471	
5330	AMD	AM27S08	
	Harris	HPROM8256	
	Intersil	IM5533	
	National	DM7577	
	Signetics	82S23	
	TI	SN54S188	
5330-1	AMD	AM27S08	
		AM29750	
	Harris	**HM7602-2**	**1192**
	Intersil	IM5600	
	National	**DM54S188**	**1262**
	Signetics	82S23	
	TI	SN54S188	
5331	**Harris**	**HM7603**	**1192**
	National	DM7578	
	Signetics	82S123	
	TI	SN54S288	
5331-1	AMD	AM27S09	
		AM29750	
	Harris	**HM7603-2**	**1192**
	Intersil	IM5610	
	National	**DM54S288**	**1262**
	Signetics	82S123	
	TI	SN54S288	
5340	**Harris**	**HM7640**	**1192**
		HM7640A	**1204**

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
5340	Intel	M3604	
	National	**DM77S296**	**1270**
	TI	SN54S475	
5340-1	**Fairchild**	**93438**	**1151**
	Harris	**HM7640-2**	**1192**
	Intersil	IM5605	
	National	**DM77S295**	**1270**
	Signetics	82S140	
	TI	SN54S475	
5341	**Harris**	**HM7641**	**1192**
		HM7641A	**1204**
	Intel	M3624	
	National	**DM77S296**	**1270**
	TI	SN54S474	
		SN74S471	
5341-1	Intel	3624	
5348	TI	SN54S473	
5348-1	**National**	**DM54S473**	**1272**
	TI	SN54S473	
5349	TI	SN54S472	
5349-1	**National**	**DM54S472**	**1272**
	TI	SN54S472	
5352	**National**	**DM54S572**	**1268**
5352-1	**Fairchild**	**93452**	**1151**
	Harris	**HM7642-2**	**1192**
	Intel	3605	
	National	**DM54S572**	**1268**
	Signetics	82S136	
	TI	SN54S476	
5353	**Harris**	**HM7642**	**1192**
	National	**DM54S573**	**1268**
5353-1	**Fairchild**	**93453**	**1151**
	Harris	**HM7643-2**	**1192**
	Intel	3625	
	National	**DM54S573**	**1268**
	Signetics	**82S137**	
	TI	SN54S477	
5380-1	**Harris**	**HM7680**	**1220**
	Intel	3608	
	National	75S228	
	Signetics	82S180	
5381-1	**Harris**	**HM7681**	**1220**
	Intel	3628	
	National	76S229	
	Signetics	82S181	
5385-1	Signetics	82S2708	
54LS240	AMD	SN54LS240	
	Fairchild	54LS240	
	TI	SN54LS240	
54LS241	AMD	SN54LS241	
	Fairchild	54LS241	
	TI	SN54LS241	
54LS244	TI	SN54LS244	
54LS363	TI	SN54LS363	
54LS373	TI	SN54LS373	
54LS374	AMD	SN54LS374	
	TI	SN54LS374	
54S240	AMD	SN54S240	
	Raytheon	54S240	
	TI	SN54S240	
54S241	AMD	SN54S241	
	Raytheon	54S241	
	TI	SN54S241	
54S244	AMD	SN54S244	
	Raytheon	54S244	
	TI	SN54S244	
54S373	TI	SN54S373	
54S374	TI	SN54S374	
5530	Fairchild	93411	
	Intel	3107	
	Intersil	IM5533	
	National	**DM54S206**	**1297**
	Raytheon	RM5330	
	Signetics	82S17	
	TI	SN54S206	
		SN54S301	
5531	Fairchild	93421	
	Intersil	IM5523	
	National	DM54S200	
	Raytheon	RM5340	
	Signetics	82S16	
	TI	SN54S201	
5560	AMD	AM27S02	
	Fairchild	93435	
	Intel	3101	
	Intersil	IM5501	
	National	DM54S289	
		DM5489	**1287**
	TI	SN54S289	
5561	AMD	AM27S03	
	National	**DM54S189**	**1292**
	TI	SN54S189	
6200	Intersil	IM5603	
	Signetics	82S226	
	TI	SN74187	
6200-1	Fairchild	93457	
	National	DM74S187	
	Signetics	82S226	
	TI	SN74187	
6201	Intersil	IM5623	
	National	DM85S97	
	Signetics	82S229	
	TI	SN74S387	
6201-1	Fairchild	93467	
	National	DM85S97	
	Signetics	82S229	
6205	Intersil	IM5604	
	Signetics	82S230	
	TI	SN74S270	
6205-1	Fairchild	93431	
	Intel	3302A	
	National	**DM74S270**	**1279**
	Signetics	82S230	
	TI	SN74S270	
6206	Signetics	82S231	
	TI	SN74S370	
6206-1	Fairchild	93441	
	Intel	3322A	
	National	**DM74S370**	**1279**
	Signetics	82S231	
	TI	SN74370	
6230	Intersil	IM5600	
	Motorola	MCM4002	
	National	DM7488	
	Signetics	8223	
	TI	SN7488A	
6230-1	National	DM7488	
	TI	SN7488A	
6231	National	DM8598	
6231-1	National	DM8598	
6240-1	Fairchild	93432	
	Intel	3304A	
	National	**DM87S95**	**1281**
6241-1	Fairchild	93442	
	Intel	3324A	
	National	**DM87S96**	**1281**
6246	Signetics	N8204	
6247	Signetics	N8205	
6275-1	Signetics	82S290	
6276-1	Signetics	82S291	
6280-1	Fairchild	93454	
	National	**DM85S29**	**1283**
	Signetics	82S280	
6280-2	Fairchild	93454	
6281-1	Fairchild	93464	
	National	**DM85S28**	**1283**
	Signetics	82S281	
6281-2	Fairchild	93464	
6300	**Fairchild**	**93417**	**1151**
	Harris	HPROM1024A	
	Intel	3601	
	Intersil	IM5603	
	Mitsubishi	M54700	
	National	DM745487	
	NEC Micro	μPD403	
	Signetics	82S126	
	TI	SN74S387	
6300-1	AMD	AM27S104	
		AM29760	
	Fairchild	**93417**	**1151**
	Harris	**HM7610**	**1192**
	Intel	3601	
	Intersil	IM5603	
	National	**DM74S387**	**1264**
	NEC Micro	**μPB403**	**1462**
	Signetics	82S126	
	TI	SN74S387	
6301	Fairchild	93426	
6301	Harris	HPROM1024	
	Intel	3621	
	Intersil	IM5623	
	Mitsubishi	M54730	
	National	**DM74S387**	**1264**
	Signetics	82S129	
	TI	SN74S287	
6301-1	AMD	AM27S11	
		AM29761	
	Fairchild	**93427**	**1151**
	Harris	**HM7611**	**1192**
	Intel	3621	
	Intersil	IM5623	
	National	**DM74S287**	**1264**
	Signetics	82S129	
	TI	SN74S287	
6305	**Fairchild**	**93436**	**1151**
	Harris	**HM7620**	**1192**
		HM7620A	**1202**
	Intel	3602	
	Intersil	IM5604	
	National	**DM74S571**	**1266**
	Signetics	82S130	
	TI	SN74S270	
6305-1	AMD	AM27S12	
		AM29770	
	Fairchild	**93436**	**1151**
	Harris	HM76220	
	Intel	3602	
	Intersil	IM5604	
	National	**DM74S570**	**1266**
	Signetics	82S130	
6306	**Fairchild**	**93446**	**1151**
	Harris	**HM7621**	**1192**
		HM7621A	**1202**
	Intel	3622	
	National	**DM74S571**	**1266**
	Signetics	82S131	
	TI	SN74S370	
6306-1	AMD	AM27S13	
		AM29770	
	Fairchild	**93446**	**1151**
	Harris	**HM7621**	**1192**
	Intel	3622	
	Intersil	IM5624	
	National	**DM74S571**	**1266**
	Signetics	82S131	
6308	TI	SN74S470	
6308-1	National	DM74S470	
	TI	SN74S470	
6309	TI	SN74S471	
6309-1	National	DM74S471	
	TI	SN74S471	
6330	AMD	AM27S08	
	Harris	HPROM8256	
	Intersil	IM5600	
	National	DM8577	
	Signetics	82S23	
	TI	SN74188A	
6330-1	AMD	AM27S08	
		AM29750	
	Harris	**HM7602**	**1192**
	Intersil	IM5600	
	National	**DM74S188**	**1262**
	Signetics	82S23	
	TI	SN74S188	
6331	AMD	AM27S09	
	Harris	**HM7603**	**1192**
	Intersil	IM5610	
	National	DM8578	
	Signetics	82S123	
	TI	SN74S288	
6331-1	AMD	AM27S09	
		AM29751	
	Harris	**HM7603**	**1192**
	Intersil	IM5610	
	National	**DM74S288**	**1262**
	Signetics	82S123	
	TI	SN74S288	
6335	**Fairchild**	**93436**	**1151**
	Intel	3602	
6340	**Harris**	**HM7640**	**1192**
		HM7640A	**1204**
	Intel	3604	
	Intersil	IM5605	
	National	**DM87S296**	**1270**
6340	TI	SN74S475	
6340-1	**Fairchild**	**93438**	**1151**
	Harris	**HM7640**	**1192**
	Intel	3604	
	Intersil	IM5605	
	National	**DM87S295**	**1270**
	NEC Micro	μPB405	
	Signetics	82S140	
	TI	SN74S475	
6341	**Harris**	**HM7641**	**1192**
		HM7641A	**1204**
	Intel	3624	
	Intersil	IM5625	
	National	**DM87S295**	**1270**
		DM87S296	**1270**
	TI	SN74S474	
6341-1	**Fairchild**	**93448**	**1151**
	Harris	**HM7641**	**1192**
	Intel	3624	
	Intersil	IM5625	
	National	**DM87S296**	**1270**
	NEC Micro	**μPB425**	**1466**
	Signetics	82S141	
	TI	SN74S474	
6348	TI	SN74S473	
6348-1	**National**	**DM74S473**	**1272**
	NEC Micro	μPB405	
	TI	SN74S473	
6349	TI	SN74S472	
6349-1	National	DM74S472	
	NEC Micro	**μPB425**	**1466**
	TI	SN74S472	
6352	Intel	3605	
	National	**DM74S572**	**1268**
6352-1	**Fairchild**	**93452**	**1151**
	Harris	**HM7642**	**1192**
	Intel	3605	
	National	**DM74S572**	**1268**
	NEC Micro	**μPB406**	**1470**
	Signetics	82S136	
	TI	SN74S476	
6353	**Harris**	**HM7642**	**1192**
	Intel	3605	
6353-1	**Fairchild**	**93453**	**1151**
	Harris	**HM7643**	**1192**
	Intel	3625	
	National	**DM74S573**	**1268**
	NEC Micro	**μPB426**	**1470**
	Signetics	82S137	
	TI	SN74S477	
6380	**Harris**	**HM7680**	**1220**
	Intel	3608	
6380-1	**Harris**	**HM7680**	**1220**
	Intel	3608	
	National	DM85S228	
	NEC Micro	**μPB408**	**1491**
	Signetics	82S180	
6381	**Harris**	**HM7681**	**1220**
	Intel	3628	
6381-1	**Harris**	**HM7681**	**1220**
	Intel	3628	
	National	DM85S299	
	NEC Micro	**μPB428**	**1491**
	Signetics	82S181	
6385-1	Signetics	82S2708	
6530	AMD	AM2701	
	Fairchild	93411	
	Intersil	IM5533	
	National	**DM74S206**	**1297**
	NEC Micro	μPB2206	
	Raytheon	RC5330	
	Signetics	82S17	
	TI	SN74S206	
		SN74S301	
6531	AMD	AM27S02	
	Fairchild	93421	
	Intersil	IM5523	
	National	DM74S200	
	NEC Micro	μPB2200	
	Signetics	82S16	
	TI	SN74S200	
		SN74S201	
6560	AMD	AM27S02	
		AM2700	
		MM6560	
	Fairchild	93435	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
6560	Fairchild	93435M	
	Intel	3101	
	Intersil	IM5501	
	National	DM74S289	
	Signetics	3101A	
		82S25	
	TI	SN74S289	
6561	AMD	AM27S03	
		MM6561	
	National	**DM74S189**	**1292**
	TI	SN74S189	
74LS240	AMD	SN74LS240	
	Fairchild	74LS240	
	ITT	ITT74LS240	
	Motorola	SN74LS240	
	Raytheon	**74LS240**	**279**
	Signetics	74LS240	
	TI	SN74LS240	
74LS241	AMD	SN74LS241	
	Fairchild	74LS241	
	ITT	ITT74LS241	
	Motorola	SN74LS241	
	Raytheon	**74LS241**	**279**
	Signetics	74LS241	
	TI	SN74LS241	
74LS244	AMD	SN74LS244	
	Fairchild	74LS244	
	ITT	ITT74LS244	
	Motorola	SN74LS244	
	Raytheon	**74LS244**	**279**
	Signetics	74LS244	
	TI	SN74LS244	
74LS373	AMD	SN74LS373	
	Fairchild	74LS373	
	ITT	ITT74LS373	
	Raytheon	**74LS373**	**288**
	Signetics	74LS373	
	TI	SN74LS373	
74LS374	AMD	SN74LS374	
	Fairchild	74LS374	
	ITT	ITT74LS374	
	National	DM74LS374	
	Raytheon	**74LS374**	**288**
	TI	SN74LS374	
74S240	AMD	SN74S240	
	Raytheon	74S240	
	TI	SN74S240	
74S241	AMD	SN74S241	
	Raytheon	74S241	
	TI	SN74S241	
74S244	AMD	SN74S244	
	Raytheon	74S244	
	TI	SN74S244	
74S373	TI	SN74S02	
		SN74S373	
74S374	TI	SN74S374	

MOS Technology

Manufacturer Device	Replacement Source	Device	IC Master Page
MCS6502	Rockwell	R6502	
	Synertek	SY6502	
MCS6503	Rockwell	R6503	
	Synertek	SY6503	
MCS6504	Rockwell	R6504	
	Synertek	SY6504	
MCS6505	Rockwell	R6505	
	Synertek	SY6505	
MCS6512	Rockwell	R6512	
	Synertek	SY6512	
MCS6513	Synertek	SY6513	
MCS6514	Rockwell	R6514	
	Synertek	SY6514	
MCS6515	Rockwell	R6515	
	Synertek	SY6515	
MCS6520	Rockwell	R6520	
	Synertek	SY6520	
MCS6522	Synertek	SY6522	
MCS6530	Rockwell	R6530	
	Synertek	SY6530	
MCS6532	Rockwell	R6532	
	Synertek	SY6532	

Mostek

Manufacturer Device	Replacement Source	Device	IC Master Page
F8	Fairchild	F8	
MK1002	AMD	1002	
MK1007	Intersil	IM7780	
	Signetics	2532	
	TI	TMS3409	
MK2302	Fairchild	3757	
	GI	RO5-2240S	
♦MK2400	AMI	S8773	
MK2500	AMI	S5232	
	Fairchild	3514	
		3515	
MK2600	AMI	S3514	
	Fairchild	3514	
		3515	
MK2708	AMD	2708	
	EA	EA2708	
	Fujitsu	MB8518	
	Intel	2708	
	Motorola	MCM2708	
	National	MM2708	
	TI	TMS2708	
MK30000	**NEC Micro**	**μPD2308**	**1478**
MK31000	**NEC Micro**	**μPD2316A**	**1481**
MK32000	**NEC Micro**	**μPD2332**	**1485**
	Signetics	2633	
	TI	TMS4800	
MK34000	**NEC Micro**	**μPD2316E**	**1492**
MK36000	Signetics	2665	
MK3702	Intel	1702A	
MK3850	**Fairchild**	**3850**	**1606**
MK3851	**Fairchild**	**3851**	**1606**
MK3852	**Fairchild**	**3852**	**1607**
MK3853	**Fairchild**	**3853**	**1607**
MK3854	**Fairchild**	**3854**	**1607**
MK3861	**Fairchild**	**3861**	**1609**
MK3870	Fairchild	3870	
MK3871	**Fairchild**	**3871**	**1609**
MK3880	**NEC Micro**	**μPDZ-80**	**1850**
	Zilog	Z80-CPU	
MK3881	Zilog	Z80-PIO	
MK3882	Zilog	Z80-CTC	
MK3883	Zilog	Z80-DMA	
MK3884	Zilog	Z80-SIO	
MK4006	Motorola	MCM4006	
	TI	SN74S387	
MK4007	Intersil	IM7501	
		IM7511	
MK4027	Fairchild	FM4027	
	Fujitsu	MB8227	
	ITT	ITT4027	
	Motorola	MCM4027	
	NEC Micro	**μPD414**	**1395**
	Signetics	4027	
	TI	TMS4027	
MK4096	EA	EA4096	
	EMM/Semi	RO3-4096	
	Fairchild	4096	
	Fujitsu	MB8224	
	NEC Micro	**μPD414**	**1395**
	Rockwell	1604	
MK4101	**Harris**	**HM6504**	**1176**
MK4102	Fairchild	2102	
	Intersil	IM7552	
	NEC Micro	μPD2102A	
	Signetics	2102	
	TI	TMS4033	
		TMS4035	
MK4104	**NEC Micro**	**μPD4104**	**1490**
MK4116	**Fairchild**	**F16K**	**1110**
	Fujitsu	MB8116	
	Intel	2116	
	Intersil	7116	
	ITT	ITT4116	
	Motorola	MCM4116	
	NEC Micro	**μPD416**	**1402**
	Signetics	2690	
	TI	TMS4116	
	Zilog	Z6116	
MK50240	AMI	S50240	
	GI	AY3-0215	
MK50241	AMI	S50241	
	GI	AY3-0216	
MK50242	AMI	S50242	
MK50242	GI	AY1-0212	
		AY3-0214	
MK5085	**AMI**	**S2559**	**372**
MK5086	**AMI**	**S2559**	**372**

Motorola Semiconductor

Manufacturer Device	Replacement Source	Device	IC Master Page
LF155	AMD	LF155	
	Fairchild	μAF155	
	Intersil	LF155	
	National	**LF155**	**786**
	PMI	**PM155**	**871**
	Raytheon	LF155	
	Signetics	LF155	
	TI	LF155	
LF156	AMD	LF156	
	Fairchild	μAF156	
	Intersil	LF156	
	National	**LF156**	**786**
	PMI	**PM156**	**877**
	Raytheon	LF156	
	Signetics	LF156	
	TI	LF156	
LF157	AMD	LF157	
	Fairchild	μAF157	
	Intersil	LF157	
	National	**LF157**	**786**
	PMI	**PM157**	**882**
	Raytheon	LF157	
	Signetics	LF157	
	TI	LF157	
LF255	AMD	LF255	
	Fairchild	μAF255	
	Intersil	LF255	
	National	**LF255**	**786**
	PMI	**PM255**	**871**
	Raytheon	LF255	
	Signetics	LF255	
	TI	LF255	
LF256	AMD	LF256	
	Fairchild	μAF256	
	Intersil	LF256	
	National	**LF256**	**786**
	PMI	**PM256**	**877**
	Raytheon	LF256	
	Signetics	LF256	
	TI	LF256	
LF257	AMD	LF257	
	Fairchild	μAF257	
	Intersil	LF257	
	National	**LF257**	**786**
	PMI	**PM257**	**882**
	Raytheon	LF257	
	Signetics	LF257	
	TI	LF257	
LF355	AMD	LF355	
	Fairchild	μAF355	
	Intersil	LF355	
	National	**LF355**	**786**
	PMI	**PM355**	**871**
	Raytheon	LF355	
	Signetics	LF355	
	TI	LF355	
LF356	AMD	LF356	
	Fairchild	μAF356	
	Intersil	LF356	
	National	**LF356**	**786**
	PMI	**PM356**	**877**
	Raytheon	LF356	
	Signetics	LF356	
	TI	LF356	
LF357	AMD	LF357	
	Fairchild	μAF357	
	Intersil	LF357	
	National	**LF357**	**786**
	PMI	**PM357**	**882**
	Raytheon	LF357	
	Signetics	LF357	
	TI	LF357	
LM101	AMD	LM101	
	Fairchild	μA101	
	Intersil	LM101	
	National	LM101	
	RCA	CA101	
	Signetics	LM101	
LM101	Silicon G	SG101	
	TI	LM101	
LM104	Fairchild	μA104	
	National	LM104	
	Raytheon	LM104	
	Silicon G	SG104	
	TI	LM104	
LM105	AMD	LM105	
	Fairchild	μA105	
	Intersil	LM105	
	National	LM105	
	Raytheon	LM105	
	Silicon G	SG105	
	TI	LM105	
LM107	AMD	LM107	
	Fairchild	μA107	
	Intersil	LM107	
	National	LM107	
	Raytheon	LM107	
	RCA	CA107	
	Signetics	LM107	
	Silicon G	SG107	
	TI	LM107	
LM108	RCA	CA108	
	Silicon G	SG108	
		SG208	
LM109	Fairchild	μA109	
	National	LM109	
	Raytheon	LM109	
	Signetics	LM109	
	Silicon G	SG109	
	TI	LM109	
LM110	AMD	LM110	
	Fairchild	μA110	
	Intersil	LM110	
	National	LM110	
	Silicon G	SG110	
LM111	AMD	LM111	
	National	LM111	
	Raytheon	LM111	
	RCA	CA111	
	Signetics	LM111	
	Silicon G	SG111	
	TI	LM111	
LM124	RCA	CA124	
LM139	RCA	CA139	
LM158	National	LM158	
LM201	AMD	LM201	
	Fairchild	μA201	
	Intersil	LM201	
	National	LM201	
	RCA	CA201	
	Signetics	LM201	
	Silicon G	SG201	
	TI	LM201	
LM204	Fairchild	μA204	
	National	LM204	
	Raytheon	LM204	
	Silicon G	SG204	
	TI	LM204	
LM205	AMD	LM205	
	Intersil	LM205	
	National	LM205	
	Raytheon	LM205	
	Silicon G	SG205	
	TI	LM205	
LM207	AMD	LM207	
	Fairchild	μA207	
	Intersil	LM207	
	National	LM207	
	Raytheon	LM207	
	RCA	CA207	
	Signetics	LM207	
	Silicon G	SG207	
	TI	LM207	
LM208	RCA	CA208	
LM209	AMD	LM209	
	Fairchild	μA209	
	National	LM209	
	Raytheon	LM209	
	Signetics	LM209	
	Silicon G	SG209	
	TI	LM209	
LM210	AMD	LM210	
	Fairchild	μA210	
	Intersil	LM210	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Motorola Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
LM210	National	LM210	
	Silicon G	SG210	
LM211	AMD	LM211	
	Intersil	LM211	
	National	LM211	
	Raytheon	LM211	
	RCA	CA211	
	Signetics	LM211	
	Silicon G	SG211	
	TI	LM211	
LM224	RCA	CA224	
LM239	RCA	CA239	
LM258	National	LM258	
LM289	Silicon G	SG208	
LM301	AMD	LM301	
	Fairchild	μA301	
	Intersil	LM301	
	National	LM301	
	Raytheon	LM301	
	RCA	CA301	
	Signetics	LM301	
	Silicon G	SG301	
	TI	LM301	
LM304	Fairchild	μA304	
	National	LM304	
	Raytheon	LM304	
	Silicon G	SG304	
	TI	LM304	
LM305	AMD	LM305	
	Fairchild	μA305	
	Intersil	LM305	
	National	LM305	
	Raytheon	LM305	
	Silicon G	SG305	
	TI	LM305	
LM307	AMD	LM307	
	Fairchild	μA307	
	Intersil	LM307	
	National	LM307	
	Raytheon	LM307	
	RCA	CA307	
	Signetics	LM307	
	Silicon G	SG307	
	TI	LM307	
LM308	RCA	CA308	
	Silicon G	SG308	
LM309	AMD	LM309	
	Fairchild	μA309	
	National	LM309	
	Raytheon	LM309	
	Signetics	LM309	
	Silicon G	SG309	
	TI	LM309	
LM310	AMD	LM310	
	Fairchild	μA310	
	Intersil	LM310	
	National	LM310	
	Silicon G	SG310	
LM311	AMD	LM311	
	Fairchild	μA311	
	Intersil	LM311	
	National	LM311	
	Raytheon	LM311	
	RCA	CA311	
	Signetics	LM311	
	Silicon G	SG311	
	TI	LM311	
LM317	**National**	**LM317**	**828**
LM323	National	LM323	
LM324	RCA	CA324	
LM358	National	LM358	
MCC14483	AMI	2733	
♦MCM10140	Plessey	SP10140	
	Signetics	10140	
	TI	SN10140	
♦MCM10142	NEC America	μPB10142	
	Plessey	SP10142	
	TI	SN10142	
MCM10144	Fairchild	F10410	
	Plessey	SP10144	
	Raytheon	RC10144	
	Signetics	10144	
MCM10144	TI	SN10144	
MCM10145	Hitachi	MD10145	
	Plessey	SP10145	
	Signetics	10145	
	TI	SN10145	
MCM10147	Fairchild	F10405	
	Fujitsu	MB7047	
	TI	SN10147	
MCM10148	Plessey	SP10148	
♦MCM10148	Signetics	10148	
	TI	SN10147	
		SN10148	
MCM10149	Signetics	10149	
MCM10152	Fujitsu	MB7042	
MCM1110	National	MM5231	
	Signetics	2430	
♦MCM1112	National	MM4230	
		MM5230	
♦MCM1131	AMI	S8614	
♦MCM1132	AMI	S8614	
♦MCM1173	AMI	S2103	
MCM14537	RCA	CD4061	
♦MCM2102	Mostek	MK4102	
MCM2111	NEC Micro	μPD2111A	
MCM2114	Intel	2114	
	TI	TMS4045	
MCM2141	TI	TMS4044	
MCM2708	AMD	2708	
	EA	EA2708	
	Fujitsu	MB8518	
	Intel	2708	
	Mostek	MK2708	
	National	MM2708	
	TI	TMS2708	
MCM4002	Intersil	IM5600	
	MMI	**6230**	**1252**
	National	DM5488	
		DM7488	
	TI	SN7488	
MCM4004	Fairchild	93407	
	Intersil	IM5603	
	MMI	**6200**	**1252**
	TI	SN7481A	
MCM4005	Fairchild	93407	
	TI	SN7481A	
MCM4006	TI	SN74S387	
MCM4027	**Fairchild**	**M4027**	**1118**
	Mostek	MK4027	
	NEC Micro	**μPD414**	**1395**
	TI	TMS4027	
MCM4064	Fairchild	93403	
♦MCM4065	Signetics	8225	
MCM4116	**Fairchild**	**F16K**	**1110**
	Intel	2116	
	Intersil	7116	
	Mostek	MK4116	
	NEC Micro	**μPD416**	**1402**
	Signetics	2690	
	TI	TMS4116	
	Zilog	Z6116	
MCM5303	Harris	HPROM0512	
MCM6560	Nitron	NCM6560	
MCM6561	Nitron	NCM6561	
MCM6570	Nitron	NCM6570	
MCM6571	Nitron	NCM6571	
MCM6572	Nitron	NCM6572	
MCM6580	Nitron	NCM6580	
MCM6581	Nitron	NCM6581	
MCM6583	Nitron	NCM6583	
MCM6590	Nitron	NCM6590	
MCM6591	Nitron	NCM6591	
MCM6604	Mostek	MK4096	
MCM6605	Intersil	IM7505	
MCM6810	**AMI**	**S6810**	**1061**
MCM68111	NEC Micro	μPD2111A	
MCM68316	Mostek	MK34000	
MCM68317	**NEC Micro**	**μPD2316E**	**1492**
MCM6832	Nitron	NCM6832	
♦MCM7001	RCA	MW7001	
MC10100	Fairchild	F10100	
	NEC America	μPB10100	
	Plessey	SP10100	
	Signetics	10100	
MC10101	Fairchild	F10101	
	Hitachi	HD10101	
	NEC America	μPB10101	
MC10101	Plessey	SP10101	
	Signetics	10101	
MC10102	Fairchild	F10102	
	Hitachi	HD10102	
	NEC America	μPB10102	
	Plessey	SP10102	
	Signetics	10102	
MC10103	Fairchild	F10103	
	NEC America	μPB10103	
	Plessey	SP10103	
	Signetics	10103	
MC10104	Fairchild	F10104	
	Hitachi	HD10104	
	Plessey	SP10104	
	Signetics	10104	
MC10105	Fairchild	F10105	
	Hitachi	HD10105	
	National	DM10105	
	NEC America	μPB10105	
	Plessey	SP10105	
	Signetics	10105	
MC10106	Fairchild	F10106	
	Hitachi	HD10106	
	National	DM10106	
	NEC America	μPB10106	
	Plessey	SP10106	
	Signetics	10106	
MC10107	Fairchild	F10107	
	Hitachi	HD10107	
	NEC America	μPB10107	
	Plessey	SP10107	
	Signetics	10107	
MC10109	Fairchild	F10109	
	Hitachi	HD10109	
	National	DM10109	
	NEC America	μPB10109	
	Plessey	SP10109	
	Signetics	10109	
MC10110	Fairchild	F10110	
	Hitachi	HD10110	
	NEC America	μPB10110	
	Plessey	SP10110	
	Signetics	10110	
MC10111	Fairchild	F10111	
	Hitachi	HD10111	
	National	DM10111	
	NEC America	μPB10111	
	Plessey	SP10111	
	Signetics	10111	
MC10113	Fairchild	F10113	
	Plessey	SP10113	
	Signetics	10113	
MC10114	Fairchild	F10114	
	Plessey	SP10114	
	Signetics	10114	
MC10115	Fairchild	F10115	
	National	DM10115	
	NEC America	μPB10115	
	Plessey	SP10115	
	Signetics	10115	
MC10116	Fairchild	F10116	
	Hitachi	HD10116	
	National	DM10116	
	Plessey	SP10116	
	Signetics	10116	
MC10117	Fairchild	F10117	
	Hitachi	HD10117	
	National	DM10117	
	NEC America	μPB10117	
	Plessey	SP10117	
	Signetics	10117	
MC10118	Fairchild	F10118	
	Hitachi	HD10118	
	National	DM10118	
	NEC America	μPB10118	
	Plessey	SP10118	
	Signetics	10118	
MC10119	Fairchild	F10119	
	Hitachi	HD10119	
	National	DM10119	
	Plessey	SP10119	
	Signetics	10119	
MC10121	Fairchild	F10121	
	Hitachi	HD10121	
	National	DM10121	
	Plessey	SP10121	
MC10121	Signetics	10121	
MC10123	Fairchild	F10123	
	Plessey	SP10123	
	Signetics	10123	
MC10124	Fairchild	F10124	
	Hitachi	HD10124	
	National	DM10124	
	NEC America	μPB10124	
	Plessey	SP10124	
	Signetics	10124	
MC10125	Fairchild	F10125	
	Hitachi	HD10125	
	Plessey	SP10125	
	Signetics	10125	
MC10128	Plessey	SP10128	
	Signetics	10128	
MC10129	Plessey	SP10129	
	Signetics	10129	
MC10130	Fairchild	F10130	
	Hitachi	HD10130	
	Plessey	SP10130	
	Signetics	10130	
MC10131	Fairchild	F10131	
	Hitachi	HD10131	
	NEC America	μPB10131	
	Plessey	SP10131	
	Signetics	10131	
MC10132	Fairchild	F10132	
	Hitachi	HD10132	
	Signetics	10132	
MC10133	Fairchild	F10133	
	Hitachi	HD10133	
	NEC America	μPB10133	
	Plessey	SP10133	
	Signetics	10133	
MC10134	Fairchild	F10134	
	Hitachi	HD10134	
	Plessey	SP10134	
	Signetics	10134	
MC10135	Fairchild	F10135	
	Plessey	SP10135	
	Signetics	10135	
MC10136	Fairchild	F10136	
	Hitachi	HD10136	
	Plessey	SP10136	
	Signetics	10136	
MC10137	Fairchild	F10137	
	Plessey	SP10137	
	Signetics	10137	
MC10138	Plessey	SP10138	
	Signetics	10138	
MC10139	Intersil	IM5600	
	Signetics	10139	
MC10141	Fairchild	F10141	
	Plessey	SP10141	
	Signetics	10141	
MC10144	NEC America	μPB10144	
	Plessey	SP10144	
	Raytheon	RC10144	
	Signetics	10144	
	TI	SN10144	
MC10145	Fairchild	F10145	
	Hitachi	HD10145	
	Plessey	SP10145	
	Signetics	10145	
MC10149	Signetics	10149	
MC10153	Fairchild	F10153	
MC10158	Fairchild	F10158	
	NEC America	μPB10158	
	Signetics	10158	
MC10159	Fairchild	F10159	
	Signetics	10159	
MC10160	Fairchild	F10160	
	Hitachi	HD10160	
	Plessey	SP10160	
	Signetics	10160	
MC10161	Fairchild	F10161	
	Hitachi	HD10161	
	NEC America	μPB10161	
	Plessey	SP10161	
	Signetics	10161	
MC10162	Fairchild	F10162	
	Hitachi	HD10162	
	NEC America	μPB10162	
	Plessey	SP10162	
	Signetics	10162	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Motorola Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Replacement Device	IC Master Page
MC10164	Fairchild	F10164	
	Hitachi	HD10164	
	NEC America	μPB10164	
	Plessey	SP10164	
	Signetics	10164	
	TI	SN10164	
MC10165	Fairchild	F10165	
	Hitachi	HD10165	
	Plessey	SP10165	
	Signetics	10165	
MC10166	Fairchild	F10166	
MC10168	Fairchild	F10168	
MC10170	Fairchild	F10170	
	Signetics	10170	
MC10171	Fairchild	F10171	
	Plessey	SP10171	
	Signetics	10171	
MC10172	Fairchild	F10172	
	Plessey	SP10172	
	Signetics	10172	
MC10173	Fairchild	F10173	
	Plessey	SP10173	
	Signetics	10173	
MC10174	Fairchild	F10174	
	Hitachi	HD10174	
	NEC America	μPB10174	
	Plessey	SP10174	
	Signetics	10174	
	TI	SN10174	
MC10175	Fairchild	F10175	
	Hitachi	HD10175	
	Plessey	SP10175	
	Signetics	10175	
MC10176	Fairchild	F10176	
	Plessey	SP10176	
	Signetics	10176	
MC10177	Fairchild	F10177	
MC10178	Fairchild	F10178	
	Plessey	SP10178	
	Signetics	10178	
MC10179	Fairchild	F10179	
	Hitachi	HD10179	
	Plessey	SP10179	
	Signetics	10179	
MC10180	Fairchild	F10180	
	Hitachi	HD10180	
	NEC America	μPB10180	
	Plessey	SP10180	
	Signetics	10180	
MC10181	Fairchild	F10181	
	Hitachi	HD10181	
	NEC America	μPB10181	
	Plessey	SP10181	
	Signetics	10181	
MC10186	Fairchild	F10186	
	Signetics	10186	
MC10190	Plessey	SP10190	
	Signetics	10190	
MC10191	Signetics	10191	
MC10192	Fairchild	F10192	
	Signetics	10192	
MC10195	Signetics	10195	
MC10210	Plessey	SP10210	
MC10212	Fairchild	F10212	
	Plessey	SP10212	
MC10216	Plessey	SP10216	
	Signetics	10216	
MC10231	Plessey	SP10231	
	Signetics	10231	
MC10501	Plessey	SP10501	
MC10502	Plessey	SP10502	
MC10504	Plessey	SP10504	
MC10505	Plessey	SP10505	
MC10506	Plessey	SP10506	
MC10507	Plessey	SP10507	
MC10509	Plessey	SP10509	
MC10514	Plessey	SP10514	
MC10515	Plessey	SP10515	
MC10516	Plessey	SP10516	
MC10517	Plessey	SP10517	
MC10518	Plessey	SP10518	
MC10519	Plessey	SP10519	
MC10521	Plessey	SP10521	
MC10524	Plessey	SP10524	
MC10525	Plessey	SP10525	
MC10531	Plessey	SP10531	
♦MC1150	AMI	MX53D	
♦MC1160	TI	TMS3003	
♦MC1161	TI	TMS4062	
♦MC1180	AMI	S2470	
♦MC1181	AMI	S2567	
	Nitron	NC1181	
♦MC1182	AMI	S2566	
	Nitron	NC1182	
♦MC1183	AMI	S2555	
	Nitron	NC1183	
♦MC1184	AMI	S2556	
	Nitron	NC1184	
MC1303	Raytheon	RC4739	
♦MC1304	Fairchild	μA732	
	National	LM1304	
♦MC1305	National	LM1305	
♦MC1307	Fairchild	μA767	
	National	LM1307	
MC1310	Exar	XR1310	
	Plessey	MC1310	
	RCA	CA1310	
	Sprague	ULN-2211	
♦MC1311	Exar	XR1800	
	Fairchild	μA758	
	RCA	CA758	
	Sprague	ULN-2244	
MC1312	Fairchild	μA1312	
MC1324	Sprague	ULN-2224	
MC1327	Sprague	ULN-2217	
♦MC1328	RCA	CA3072	
	Sprague	ULN-2114	
		ULN-2228	
MC1330	Mitsubishi	M5169	
♦MC1339	Signetics	PA239	
MC1350	NPC	ESM1350	
MC1351	National	LM1351	
MC1352	Mitsubishi	M5183	
	RCA	CA1352	
	Sanyo	LA1352	
MC1353	Mitsubishi	M5784	
	Sanyo	LA1353	
MC1356	Sprague	ULN-2136	
MC1357	Fairchild	μA2136	
	RCA	CA2111	
	Signetics	ULN2111	
	Sprague	ULN-2111	
		ULN-2113	
MC1358	Fairchild	μA3065	
	RCA	CA3065	
	Sprague	ULN-2165	
MC1364	Fairchild	μA3064	
	RCA	CA3064	
	Sprague	ULN-2264	
♦MC1370	Fairchild	μA780	
	RCA	CA3070	
	Sprague	ULN-2124	
♦MC1371	Fairchild	μA781	
	RCA	CA3071	
	Sprague	ULN-2127	
MC1375	RCA	CA3075	
MC1389	RCA	CA3089	
MC1391	Fairchild	μA1391	
	RCA	CA1391	
	Sprague	ULN-2291	
MC1394	Fairchild	μA1394	
	RCA	CA1394	
	Sprague	ULN-2294	
MC1398	Mitsubishi	M5190	
	RCA	CA1398	
	Sprague	ULN-2298	
MC1399	Signetics	MC1399	
	Sprague	ULN-2299	
MC14000	Mitel	SIL4000	
	National	CD4000	
	RCA	CD4000	
	Solitron	CM4000	
	SSS	SCL4000	
	TI	TP4000	
MC14001	Fairchild	F4001	
	Mitel	SIL4001	
	National	CD4001	
	NEC America	μPD4001	
MC14001	RCA	CD4001	
	SGS	HBF4001	
	Solitron	CM4001	
	SSS	SCL4001	
	TI	TP4001	
	Toshiba	TC4001	
MC14002	Fairchild	F4002	
	Mitel	SIL4002	
	National	CD4002	
	NEC America	μPD4002	
	RCA	CD4002	
	SGS	HBF4002	
	Solitron	CM4002	
	SSS	SCL4002	
	TI	TP4002	
	Toshiba	TC4002	
MC14006	Fairchild	F4006	
	National	CD4006	
	NEC America	μPD4006	
	RCA	CD4006	
	Solitron	CM4006	
	SSS	SCL4006	
MC14007	Fairchild	F4007	
	Mitel	SIL4007	
	National	CD4007	
	RCA	CD4007	
	SGS	HBF4007	
	Solitron	CM4007	
	SSS	SCL4007	
	TI	TP4007	
	Toshiba	TC4007	
MC14008	Fairchild	F4008	
	National	CD4008	
	RCA	CD4008	
	SGS	HBF4008	
	Solitron	CM4008	
	SSS	SCL4008	
	TI	TP4008	
	Toshiba	TC4008	
MC14009	National	CD4009	
	RCA	CD4009	
	SSS	SCL4009	
MC14010	National	CD4010	
	RCA	CD4010	
	SSS	SCL4010	
MC14011	Fairchild	F4011	
	Mitel	SIL4011	
	National	CD4011	
	NEC America	μPD4011	
	RCA	CD4011	
	SGS	HBF4011	
	Solitron	CM4011	
	SSS	SCL4011	
	TI	TP4011	
	Toshiba	TC4011	
MC14012	Fairchild	F4012	
	Mitel	SIL4012	
	National	CD4012	
	NEC America	μPD4012	
	RCA	CD4012	
	SGS	HBF4012	
	Solitron	CM4012	
	SSS	SCL4012	
	TI	TP4012	
	Toshiba	TC4012	
MC14013	Fairchild	F4013	
	Mitel	SIL4013	
	National	CD4013	
	NEC America	μPD4013	
	RCA	CD4013	
	SGS	HBF4013	
	Solitron	CM4013	
	SSS	SCL4013	
	TI	TP4013	
	Toshiba	TC4013	
MC14014	Fairchild	F4014	
	Mitel	SIL4014	
	National	CD4014	
	NEC America	μPD4014	
	RCA	CD4014	
	SGS	HBF4014	
	Solitron	CM4014	
	SSS	SCL4014	
	TI	TP4014	
	Toshiba	TC4014	
MC14015	Fairchild	F4015	
MC14015	Mitel	SIL4015	
	National	CD4015	
	NEC America	μPD4015	
	RCA	CD4015	
	SGS	HBF4015	
	Solitron	CM4015	
	SSS	SCL4015	
	TI	TP4015	
	Toshiba	TC4015	
MC14016	AD	AD7516	
	Fairchild	F4016	
	Micro Power	MPS7516	
	Mitel	SIL4016	
	National	CD4016	
	RCA	CD4016	
	Solitron	CM4016	
	SSS	SCL4016	
	TI	TP4016	
MC14017	Fairchild	F4017	
	Mitel	SIL4017	
	National	CD4017	
	NEC America	μPD4017	
	RCA	CD4017	
	SGS	HBF4017	
	Solitron	CM4017	
	SSS	SCL4017	
	TI	TP4017	
	Toshiba	TC4017	
MC14018	TI	TP4018	
MC14020	Fairchild	F4020	
	Mitel	SIL4020	
	National	CD4020	
	NEC America	μPD4020	
	RCA	CD4020	
	SGS	HBF4020	
	Solitron	CM4020	
	SSS	SCL4020	
	TI	TP4020	
	Toshiba	TC4020	
MC14021	Fairchild	F4021	
	Mitel	SIL4021	
	National	CD4021	
	NEC America	μPD4021	
	RCA	CD4021	
	Solitron	CM4021	
	SSS	SCL4021	
	TI	TP4021	
	Toshiba	TC4021	
MC14022	Fairchild	F4022	
	Mitel	SIL4022	
	National	CD4022	
	RCA	CD4022	
	SGS	HBF4022	
	Solitron	CM4022	
	SSS	SCL4022	
	TI	TP4022	
	Toshiba	TC4022	
MC14023	Fairchild	F4023	
	Mitel	SIL4023	
	National	CD4023	
	NEC America	μPD4023	
	RCA	CD4023	
	SGS	HBF4023	
	Solitron	CM4023	
	SSS	SCL4023	
	TI	TP4023	
	Toshiba	TC4023	
MC14024	Fairchild	F4024	
	Mitel	SIL4024	
	National	CD4024	
	NEC America	μPD4024	
	RCA	CD4024	
	SGS	HBF4024	
	Solitron	CM4024	
	SSS	SCL4024	
	TI	TP4024	
	Toshiba	TC4024	
MC14025	Fairchild	F4025	
	Mitel	SIL4025	
	National	CD4025	
	NEC America	μPD4025	
	RCA	CD4025	
	SGS	HBF4025	
	Solitron	CM4025	
	SSS	SCL4025	
	TI	TP4025	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Motorola Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
MC14025	Toshiba	TC4025	
MC14027	Fairchild	F4027	
	Mitel	SIL4027	
	National	CD4027	
	NEC America	μPD4027	
	RCA	CD4027	
	SGS	HBF4027	
	Solitron	CM4027	
	SSS	SCL4027	
	TI	TP4027	
	Toshiba	TC4027	
MC14028	Fairchild	F4028	
	Mitel	SIL4028	
	National	CD4028	
	NEC America	μPD4028	
	RCA	CD4028	
	SGS	HBF4028	
	Solitron	CM4028	
	SSS	SCL4028	
	TI	TP4028	
	Toshiba	TC4028	
MC14032	RCA	CD4032	
	Solitron	CM4032	
	Toshiba	TC4032	
MC14034	Fairchild	F4034	
	National	CD4034	
	NEC America	μPD4034	
	RCA	CD4034	
	Solitron	CM4034	
	SSS	SCL4034	
	Toshiba	TC4034	
MC14035	Fairchild	F4035	
	Mitel	SIL4035	
	National	CD4035	
	NEC America	μPD4035	
	RCA	CD4035	
	SGS	HBF4035	
	Solitron	CM4035	
	SSS	SCL4035	
	TI	TP4035	
	Toshiba	TC4035	
MC14038	RCA	CD4038	
	Toshiba	TC4038	
MC14040	Fairchild	F4040	
	National	CD4040	
	RCA	CD4040	
	SSS	SCL4040	
	TI	TP4040	
	Toshiba	TC4040	
MC14042	Fairchild	F4042	
	Mitel	SIL4042	
	National	CD4042	
	NEC America	μPD4042	
	RCA	CD4042	
	SGS	HBF4042	
	Solitron	CM4042	
	SSS	SCL4042	
	TI	TP4042	
	Toshiba	TC4042	
MC14043	Fairchild	F4043	
	Mitel	SIL4043	
	National	CD4043	
	NEC America	μPD4043	
	RCA	CD4043	
	Solitron	CM4043	
	SSS	SCL4043	
	TI	TP4043	
	Toshiba	TC4043	
MC14044	Fairchild	F4044	
	Mitel	SIL4044	
	National	CD4044	
	NEC America	μPD4044	
	RCA	CD4044	
	Solitron	CM4044	
	SSS	SCL4044	
	TI	TP4044	
	Toshiba	TC4044	
MC14046	Fairchild	F4046	
	Mitel	SIL4046	
	National	CD4046	
	RCA	CD4046	
	Solitron	CM4046	
MC14046	SSS	SCL4046	
MC14049	Fairchild	F4049	
	Mitel	SIL4049	
	National	CD4049	
	NEC America	μPD4049	
	RCA	CD4009	
		CD4049	
	SGS	HBF4049	
	Solitron	CM4049	
	SSS	SCL4049	
	TI	TP4049	
	Toshiba	TC4049	
MC14050	Fairchild	F4050	
	Mitel	SIL4050	
	National	CD4050	
	NEC America	μPD4050	
	RCA	CD4010	
		CD4050	
	SGS	HBF4050	
	Solitron	CM4050	
	SSS	SCL4050	
	TI	TP4050	
	Toshiba	TC4050	
MC14051	Fairchild	F4051	
	Mitel	SIL4051	
	National	CD4051	
	NEC America	μPD4051	
	RCA	CD4051	
	Solitron	CM4051	
	SSS	SCL4051	
	TI	TP4051	
	Toshiba	TC4051	
MC14052	Fairchild	F4052	
	Mitel	SIL4052	
	National	CD4052	
	NEC America	μPD4052	
	RCA	CD4052	
	Solitron	CM4052	
	SSS	SCL4052	
	TI	TP4052	
	Toshiba	TC4052	
MC14053	Fairchild	F4053	
	Mitel	SIL4053	
	National	CD4053	
	NEC America	μPD4053	
	RCA	CD4053	
	Solitron	CM4053	
	SSS	SCL4053	
	TI	TP4053	
	Toshiba	TC4053	
MC14066	Fairchild	F4066	
	Mitel	SIL4066	
	National	CD4066	
	NEC America	μPD4066	
	RCA	CD4063	
		CD4066	
	SGS	HBF4066	
	Signetics	N4066	
	Solitron	CM4066	
	SSS	SCL4066	
	Toshiba	TC4066	
MC14068	Fairchild	F4068	
	Mitel	SIL4068	
	NEC America	μPD4068	
	RCA	CD4068	
	Solitron	CM4068	
	SSS	SCL4068	
	TI	TP4068	
	Toshiba	TC4068	
MC14069	Fairchild	F4069	
	Harris	HD74C04	
	Mitel	SIL4069	
	National	CD4069	
		MM74C04	
	NEC America	μPD4069	
	RCA	CD4069	
	Solitron	CM4069	
	SSS	SCL4069	
	TI	TP4069	
	Toshiba	TC4069	
MC14070	RCA	CD4070	
	SSS	SCL4070	
MC14071	Fairchild	F4071	
	Mitel	SIL4071	
	National	CD4071	
	NEC America	μPD4071	
MC14071	RCA	CD4071	
	Solitron	CM4071	
	SSS	SCL4071	
	TI	TP4071	
	Toshiba	TC4071	
MC14072	Fairchild	F4072	
	Mitel	SIL4072	
	NEC America	μPD4072	
	RCA	CD4072	
	SSS	SCL4072	
	TI	TP4072	
	Toshiba	TC4072	
MC14073	Fairchild	F4073	
	Mitel	SIL4073	
	National	CD4073	
	NEC America	μPD4073	
	RCA	CD4073	
	Solitron	CM4073	
	SSS	SCL4073	
	TI	TP4073	
	Toshiba	TC4073	
MC14075	Fairchild	F4075	
	Mitel	SIL4075	
	National	CD4075	
	NEC America	μPD4075	
	RCA	CD4075	
	SSS	SCL4075	
	TI	TP4075	
	Toshiba	TC4075	
MC14076	Fairchild	F4076	
	Harris	HD74C173	
	Mitel	SIL4076	
	National	CD4076	
		MM74C173	
	RCA	CD4076	
	Solitron	CM4076	
	SSS	SCL4076	
MC14077	Fairchild	F4077	
	Mitel	SIL4077	
	RCA	CD4077	
	Solitron	CM4077	
	SSS	SCL4077	
MC14078	Fairchild	F4078	
	Mitel	SIL4078	
	NEC America	μPD4078	
	RCA	CD4078	
	Solitron	CM4078	
	SSS	SCL4078	
	TI	TP4078	
	Toshiba	TC4078	
MC1408	AD	AD559	
	AMD	SSS1408	
	Datel	DAC-IC8BC	
	Fairchild	μA0802C	
	PMI	SSS1408	
	Signetics	MC1408	
MC14081	Fairchild	F4081	
	Mitel	SIL4081	
	National	CD4081	
	NEC America	μPD4081	
	RCA	CD4081	
	Solitron	CM4081	
	SSS	SCL4081	
	TI	TP4081	
	Toshiba	TC4081	
MC14082	Fairchild	F4082	
	Mitel	SIL4082	
	NEC America	μPD4082	
	RCA	CD4082	
	SSS	SCL4082	
	TI	TP4082	
	Toshiba	TC4082	
MC14093	Fairchild	F4093	
	National	CD4093	
	NEC America	μPD4093	
	RCA	CD4093	
MC1411	Signetics	NE5501	
		ULN2001	
	Sprague	ULN-2001	
	TI	ULN2001	
MC1412	Signetics	NE5502	
		ULN2002	
	Sprague	ULN-2002	
	TI	ULN2002	
MC1413	Signetics	NE5503	
		ULN2003	
MC1413	Sprague	ULN-2003	
	TI	ULN2003	
MC1414	National	LM1414	
	Raytheon	RC1414	
	TI	TL514	
MC1416	Signetics	NE5504	
		ULN2004	
	TI	ULN2004	
MC14160	Fairchild	F40160	
	SSS	SCL4160	
	TI	TP4360	
MC14161	Fairchild	F40161	
	SSS	SCL4161	
	TI	TP4361	
MC14162	Fairchild	F40162	
	SSS	SCL4162	
	TI	TP4362	
MC14163	Fairchild	F40163	
	SSS	SCL4163	
	TI	TP4363	
MC14174	Fairchild	F40174	
MC14175	NEC America	μPD4175	
MC14194	Fairchild	F40194	
	NEC America	μPD4194	
MC14308	RCA	CD4038	
	Solitron	CM4038	
	Toshiba	TC4038	
MC1436	**Harris**	**HA-2645**	**700**
	National	LM1436	
	Silicon G	SG1436	
MC1437	Raytheon	RC1437	
♦MC1441	RCA	CA1541	
MC14501	NEC America	μPD4501	
	RCA	CD4068	
MC14502	Mitel	SIL4502	
	RCA	CD4502	
	SSS	SCL4502	
MC14503	National	CD4503	
	NEC America	μPD4503	
MC14506	RCA	CD4085	
MC14507	National	CD4070	
		CD4507	
		MM74C86	
	RCA	CD4030	
		CD4070	
		CD4070A	
	SSS	SCL4030	
	TI	TP4507	
MC14508	Mitel	SIL4508	
	NEC America	μPD4508	
	RCA	CD4508	
	Solitron	CM4508	
	SSS	SCL4508	
	Toshiba	TC4508	
MC14510	Fairchild	F4510	
	Mitel	SIL4510	
	National	CD4510	
	NEC America	μPD4510	
	RCA	CD40192	
		CD4510	
	SSS	SCL4510	
	Toshiba	TC4510	
MC14511	Fairchild	F4511	
	Mitel	SIL4511	
	National	CD4511	
	NEC America	μPD4511	
	RCA	CD4511	
	Solitron	CM4511	
	SSS	SCL4511	
	TI	TP4511	
MC14512	Fairchild	F4512	
	Mitel	SIL4512	
	National	CD4512	
	NEC America	μPD4512	
	SSS	SCL4512	
	TI	TP4512	
	Toshiba	TC4512	
MC14514	Fairchild	F4514	
	Mitel	SIL4514	
	National	CD4514	
	NEC America	μPD4514	
	RCA	CD4514	
	Solitron	CM4514	
	SSS	SCL4514	
	Toshiba	TC4514	
MC14515	Fairchild	F4515	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Motorola Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
MC14515	Mitel	SIL4515	
	National	CD4515	
	NEC America	µPD4515	
	RCA	CD4515	
	Solitron	CM4515	
	SSS	SCL4515	
	Toshiba	TC4515	
MC14516	Fairchild	F4516	
	Mitel	SIL4516	
	National	CD4516	
	NEC America	µPD4516	
	RCA	CD40193	
		CD4516	
	SSS	SCL4516	
	Toshiba	TC4516	
MC14517	NEC America	µPD4517	
	SSS	SCL4517	
MC14518	Fairchild	F4518	
	Mitel	SIL4518	
	National	CD4518	
	NEC America	µPD4518	
	RCA	CD4518	
	Solitron	CM4518	
	SSS	SCL4518	
	TI	TP4518	
	Toshiba	TC4518	
MC14519	Fairchild	F4519	
	National	CD4519	
	NEC America	µPD4519	
	RCA	CD4019	
	TI	TP4519	
MC14520	Fairchild	F4520	
	Mitel	SIL4520	
	National	CD4520	
	NEC America	µPD4520	
	RCA	CD4520	
	Solitron	CM4520	
	SSS	SCL4520	
	TI	TP4520	
	Toshiba	TC4520	
MC14522	Fairchild	F4522	
	National	CD4522	
	NEC America	µPD4522	
	RCA	CD4018	
	SSS	SCL4522	
	TI	TP4522	
MC14526	Fairchild	F4526	
	NEC America	µPD4526	
	SSS	SCL4526	
	TI	TP4526	
MC14527	National	CD4527	
	RCA	CD4527	
	SSS	SCL4527	
MC14528	Fairchild	F4528	
	National	CD4528	
	NEC America	µPD4528	
	RCA	CD4528	
	SSS	SCL4528	
	Toshiba	TC4528	
MC14529	National	CD4529	
	RCA	CD4067	
MC14530	NEC America	µPD4530	
MC14531	Fairchild	F4531	
	RCA	CD40101	
	SSS	SCL4531	
	TI	TP4531	
MC14532	Fairchild	F4532	
	NEC America	µPD4532	
	RCA	CD4532	
	Toshiba	TC4532	
MC14539	Fairchild	F4539	
	NEC America	µPD4539	
	Toshiba	TC4539	
MC14543	National	CD4543	
	RCA	CD4056	
	SSS	SCL4543	
MC1455	AMD	NE555	
	Exar	XR555	
	Fairchild	µA555	
	Raytheon	RC555	
	RCA	CA555	
	Signetics	NE555	
MC1455	TI	NE555	
MC14553	Fairchild	F4553	
MC14555	Fairchild	F4555	
	NEC America	µPD4555	
	RCA	CD4555	
	SSS	SCL4555	
MC14556	Fairchild	F4556	
	NEC America	µPD4556	
	RCA	CD4556	
	SSS	SCL4556	
MC14557	Fairchild	F4557	
	RCA	CD4031	
MC14558	RCA	CD4055	
MC1456	**Harris**	**HA-2605**	**688**
	Raytheon	RC1556	
	Signetics	MC1456	
	Silicon G	SG1456	
MC14560	NEC America	µPD4560	
MC14561	NEC America	µPD4561	
MC14562	RCA	CD4062	
MC14569	RCA	CD4059	
MC1456	AMD	AM1458	
	Exar	XR1458	
	Fairchild	µA1458	
	Harris	**HA-2655**	**704**
	National	LM1458	
	PMI	**OP-17**	**882**
		SSS1458	**844**
	Raytheon	RC1458	
		RC4558	
	RCA	CA1458	
	Signetics	MC1458	
	Silicon G	SG1458	
	TI	MC1458	
MC14580	RCA	CD40108	
MC14581	RCA	CD40181	
		CD4057	
	SSS	SCL4581	
	TI	TP4581	
MC14582	Fairchild	F4582	
	RCA	CD40182	
	SSS	SCL4582	
	TI	TP4582	
MC14583	Fairchild	F4583	
	RCA	CD40100	
	Toshiba	TC4583	
MC14584	National	CD40106	
		CD4584	
		MM74C14	
	NEC America	µPD4584	
	RCA	CD40106	
		CD4016	
	SSS	SCL4584	
MC14585	National	MM74C85	
	RCA	CD4063	
	SSS	HD14585	
		SCL4585	
	Toshiba	TC4585	
MC1468	Exar	XR1468	
	Silicon G	SG1468	
MC1488	AMD	MC1488	
	Exar	XR1488	
	ITT	ITT1488	
	National	DS1488	
	Raytheon	RC1488	
		RM1488	
	Signetics	MC1488	
	Silicon G	SG1488	
	TI	MC1488	
		SN75188	
MC1489	AMD	MC1489	
	Exar	XR1489	
	ITT	ITT1489	
	National	DS1489	
	Raytheon	RC1489	
	Signetics	MC1489	
	Silicon G	SG1489	
	TI	MC1489	
		SN75189	
MC1489A	Exar	XR1489A	
MC1495	Intech/FMI	A8495	
	Plessey	SL1495	
	Silicon G	SG1495	
MC1496	Fairchild	µA796	
	Plessey	SL1496	
	Signetics	MC1496	
MC1496	Silicon G	SG1496	
MC1508	AD	AD559	
	AMD	SSS1508	
	Datel	DAC-IC8BM	
	Fairchild	MA0802M	
	PMI	SSS1508	
MC1510	TI	SN75189	
MC1514	National	LM1514	
	Raytheon	RM1514	
	TI	TL514	
MC1536	**Harris**	**HA-2640**	**700**
	National	LM1536	
	Silicon G	SG1536	
MC1537	Raytheon	RM1537	
MC1541	RCA	CA1541	
MC1555	AMD	SE555	
	Exar	XR555M	
	Raytheon	RM555	
	RCA	CA555	
	Signetics	SE555	
	Silicon G	NE555	
	TI	NE555	
MC1556	**Harris**	**HA-2600**	**688**
	Raytheon	RM1556	
		RM1556A	
	Signetics	MC1556	
	Silicon G	SG1556	
MC1558	AMD	1558	
	Exar	XR1558	
	Fairchild	µA1558	
	Harris	**HA-2650**	**704**
	National	LM1558	
	PMI	**PM1558**	**844**
		SSS1558	**844**
	Raytheon	RM1558	
		RM4558	
	RCA	CA1558	
	Signetics	MC1558	
	Silicon G	SG1558	
	TI	MC1558	
MC1568	Exar	XR1568	
	Silicon G	SG1568	
MC1595	Intech/FMI	A8495	
		A8595	
	Plessey	MC1595	
	Silicon G	SG1595	
MC1596	Fairchild	µA796	
	National	LM1596	
	Plessey	MC1596	
	Signetics	MC1596	
	Silicon G	SG1596	
MC1648	Plessey	SP1648	
MC1650	Plessey	SP1650	
MC1651	Plessey	SP1651	
MC1658	Fairchild	11C58	
	Plessey	SP1658	
MC1660	Plessey	SP1660	
MC1661	Plessey	SL1661	
MC1662	Plessey	SP1662	
MC1663	Plessey	SL1663	
MC1664	Plessey	SP1664	
MC1665	Plessey	SL1665	
MC1666	Plessey	SP1666	
MC1667	Plessey	SL1667	
MC1668	Plessey	SP1668	
MC1669	Plessey	SL1669	
MC1670	Plessey	SP1670	
MC1671	Plessey	SL1671	
MC1672	Plessey	SP1672	
MC1673	Plessey	SL1673	
MC1674	Plessey	SP1674	
MC1675	Plessey	SL1675	
MC1690	Fairchild	11C06C	
	Plessey	SP1690	
MC1692	Plessey	SP1692	
MC1709	Fairchild	µA709	
	National	LM1709	
		LM709	
	Raytheon	RC709	
		RM709	
	Signetics	µA709	
	TI	µA709	
MC1710	Fairchild	µA710	
	National	LM710	
	Raytheon	RC710	
		RM710	
MC1710	Signetics	µA710	
	Silicon G	SG1710	
		SG710	
	TI	µA710	
MC1711	Fairchild	µA711	
	National	LM711	
	Raytheon	RC711	
		RM711	
	Signetics	µA711	
	Silicon G	SG1711	
		SG711	
	TI	µA711	
MC1712	Fairchild	µA702	
	Raytheon	RC702	
		RM702	
	TI	µA702	
MC1723	AMD	723	
	Fairchild	µA723	
	Intersil	723	
	National	LM723	
	Raytheon	RC723	
		RM723	
	RCA	CA723	
	Signetics	µA723	
	Silicon G	SG1723	
		SG723	
	TI	µA723	
MC1733	AMD	733	
	National	LM733	
	Raytheon	RC733	
		RM733	
	Signetics	µA733	
	Silicon G	SG733	
	TI	µA733	
MC1741	AMD	741	
	Fairchild	µA741	
	Intersil	741	
	National	LM741	
	PMI	**OP-02**	**839**
		PM741	**839**
		SSS741	**839**
	Raytheon	RC741	
		RM741	
	RCA	CA741	
	Signetics	µA741	
	Silicon G	SG1741	
		SG741	
	TI	µA741	
MC1741S	Silicon G	SG1741S	
MC1747	AMD	747	
	Fairchild	µA747	
	PMI	**PM747**	**844**
	Raytheon	RC747	
		RM747	
	RCA	CA747	
	Signetics	µA747	
	Silicon G	SG747	
	Teledyne S	747	
	TI	µA747	
MC1748	AMD	748	
	Fairchild	µA748	
	Intersil	748	
	National	LM748	
	Raytheon	RC748	
		RM748	
	RCA	CA748	
	Signetics	µA748	
	Silicon G	SG1748	
		SG748	
	TI	µA748	
MC1776	Fairchild	µA776	
MC1800	National	DM1800	
	TI	SN151800	
MC1801	National	DM1801	
	TI	SN151801	
MC1802	TI	SN151802	
MC1803	TI	SN151803	
MC1804	TI	SN151804	
MC1805	TI	SN151805	
MC1806	TI	SN151806	
MC1807	TI	SN151807	
MC1808	TI	SN151808	
MC1809	TI	SN151809	
MC1810	TI	SN151810	
MC1811	TI	SN151811	
MC1812	TI	SN151812	

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Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Motorola Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
MC1900	TI	SN151900	
MC1901	TI	SN151901	
MC1902	TI	SN151902	
MC1903	TI	SN151903	
MC1904	TI	SN151904	
MC1905	TI	SN151905	
MC1906	TI	SN151906	
MC1907	TI	SN151907	
MC1908	TI	SN151908	
MC1909	TI	SN151909	
MC1910	TI	SN151910	
MC1911	TI	SN151911	
MC1912	TI	SN151912	
MC2257	Nitron	NC2257	
MC2259	Nitron	NC2259	
MC2260	Nitron	NC2260	
MC26S10	AMD	AM26S10	
MC2901	AMD	AM2901A	
	Fairchild	F2901A	
		9409	
	National	**IDM2901A**	
			1656,1680
	NEC Micro	**μPB2901**	**1850**
	Raytheon	AM2901A	
	Signetics	**N2901**	**1851**
MC2902	AMD	AM2902	
	National	IDM2902	
	NEC Micro	**μPB2902**	**1850**
	Raytheon	AM2902	
MC2905	AMD	AM2905	
	Raytheon	AM2905	
MC2906	AMD	AM2906	
	Raytheon	AM2906	
MC2907	AMD	AM2907	
	Raytheon	AM2907	
MC2909	AMD	AM2909	
	National	IDM2909	
	NEC Micro	**μPB2909**	**1850**
	Raytheon	AM2909	
MC2911	AMD	AM2911	
	National	IDM2911	
	NEC Micro	**μPB2911**	**1850**
	Raytheon	AM2911	
MC2915	AMD	AM2915	
	NEC Micro	**μPB2915**	**1850**
MC2916	AMD	AM2916	
	NEC Micro	**μPB2916**	**1850**
MC2917	AMD	AM2917	
	NEC Micro	**μPB2917**	**1850**
MC2918	AMD	AM2918	
	NEC Micro	**μPB2918**	**1850**
	Raytheon	AM2918	
MC3000	Fairchild	74H00	
		9H00	
	ITT	ITT54H00	
	TI	SN74H00	
MC3001	Fairchild	74H08	
		9H08	
	ITT	ITT7408	
	TI	SN7408	
MC3003	ITT	ITT7432	
	TI	SN7432	
MC3004	Fairchild	74H01	
		9H01	
	ITT	ITT74H01	
	TI	SN74H01	
MC3005	Fairchild	74H10	
		9H10	
	ITT	ITT74H10	
	TI	SN74H10	
MC3006	Fairchild	74H11	
		9H11	
	ITT	ITT74H11	
	TI	SN74H11	
MC3008	Fairchild	74H04	
		9H04	
	ITT	ITT74H04	
	TI	SN74H04	
MC3009	Fairchild	74H05	
		9H05	
	ITT	ITT74H05	
	TI	SN74H05	
MC3010	Fairchild	74H20	
		9H20	
	ITT	ITT74H20	
	TI	SN74H20	
MC3011	Fairchild	74H21	
		9H21	
		9H60	
	ITT	ITT74H21	
	TI	SN74H21	
MC3012	Fairchild	74H22	
		9H22	
	TI	SN74H22	
MC3015	TI	SN74H30	
MC3016	Fairchild	74H30	
		9H30	
	ITT	ITT74H30	
	TI	SN74430	
MC3018	Fairchild	74H62	
		9H62	
	TI	SN74H62	
MC3019	Fairchild	74H61	
		9H61	
	TI	SN74H61	
MC3020	Fairchild	74H50	
		9H50	
	ITT	ITT74H50	
	TI	SN74H50	
MC3021	TI	SN74S86	
MC3023	Fairchild	74H51	
		9H51	
	ITT	ITT74H51	
	TI	SN74H51	
MC3024	Fairchild	74H40	
		9H40	
	ITT	ITT74H40	
	TI	SN74H40	
MC3025	ITT	ITT74H40	
	TI	SN74H40	
MC3030	Fairchild	74H60	
		9H60	
	ITT	ITT74H60	
	TI	SN74H60	
MC3031	Fairchild	74H52	
		9H52	
	TI	SN74H52	
MC3032	Fairchild	74H53	
		9H53	
	ITT	ITT74H53	
	TI	SN74H53	
MC3033	Fairchild	74H54	
		9H54	
	ITT	ITT74H54	
	TI	SN74H54	
MC3034	Fairchild	74H55	
		9H55	
	TI	SN74H55	
MC3054	Fairchild	74H71	
		9H71	
	TI	SN74H71	
MC3055	Fairchild	74H72	
		9H72	
	TI	SN74H72	
MC3060	ITT	ITT74H74	
	TI	SN74H74	
MC3061	Fairchild	9S114	
	TI	SN74S114	
MC3062	Fairchild	9S113	
	TI	SN74S113	
MC3063	Fairchild	74H73	
		9H73	
	ITT	ITT74H73	
	TI	SN74H73	
MC3100	TI	SN54H00	
MC3101	TI	SN5408	
MC3103	TI	SN5432	
MC3104	TI	SN54H01	
MC3105	TI	SN54H10	
MC3106	TI	SN54H11	
MC3108	TI	SN54H04	
MC3109	TI	SN54H05	
MC3110	TI	SN54H20	
MC3111	TI	SN54H21	
MC3112	TI	SN54H22	
MC3116	TI	SN54H30	
MC3118	TI	SN54H62	
MC3119	TI	SN54H61	
MC3120	TI	SN54H50	
MC3121	TI	SN54H86	
MC3123	TI	SN54H51	
MC3124	TI	SN54H40	
MC3125	TI	SN54H40	
MC3130	TI	SN54H60	
MC3131	TI	SN54H52	
MC3132	TI	SN54H53	
MC3133	TI	SN54H54	
MC3134	TI	SN54H55	
MC3154	TI	SN54H71	
MC3155	TI	SN54H72	
MC3160	TI	SN54H74	
MC3161	TI	SN54S114	
MC3162	TI	SN54S113	
MC3163	TI	SN54H73	
MC3301	Fairchild	μA3301	
	Raytheon	LM2900	
		RC3301	
MC3302	Fairchild	μA3302	
	Raytheon	RC3302	
	RCA	CA339	
	Silicon G	SG3302	
	TI	LM3302	
MC3346	RCA	CA3046	
		CA3086	
MC3401	Fairchild	μA3401	
	Raytheon	LM3900	
		RC3401	
	RCA	CA3401	
MC3403	Exar	XR3403	
	Fairchild	μA3403C	
	Raytheon	RC3403	
		RC4137	
MC3410C	Datel	DAC-IC10B	
MC3416	Raytheon	RC4444	
MC3423	TI	MC3423	
MC3437	National	DS8837	
MC3438	National	DS8838	
MC3441	**National**	**DS3651**	**517**
MC3443	National	DS3653	
MC3446	TI	MC3446	
MC3450	National	DS3650	
MC3452	National	DS3652	
MC3456	AMD	NE556	
	Exar	XR556	
	Signetics	NE556	
MC3460	National	DS3674	
MC3503	Exar	XR3503	
	Fairchild	μA3503	
	Raytheon	RM3503	
		RM4137	
MC3523	TI	MC3523	
MC3556	AMD	SE556	
	Exar	XR556M	
MC4004	TI	SN7481A	
MC4005	Fairchild	93407	
	TI	SN7481	
MC4015	Raytheon	RL4015	
MC4024	Fairchild	11C24C	
MC4044	Fairchild	11C44C	
MC4064	MMI	6560	
	Signetics	N82S16	
MC4304	TI	SN5481A	
MC4305	TI	SN5481A	
MC4558	Exar	XR4558	
	Raytheon	RC4558	
MC4741	Exar	XR4741	
	Harris	**HA-4741**	**735**
	National	LM148	
MC5003	TI	SN74186	
MC5005	**MMI**	**6300**	**1252**
	TI	SN74S387	
MC5303	TI	SN54186	
MC5400	Fairchild	5400	
	ITT	ITT5400	
	National	DM5400	
	Raytheon	5400	
	Signetics	5400	
	TI	SN5400	
MC5401	Fairchild	5401	
	ITT	ITT5401	
	National	DM5401	
	Raytheon	5401	
	Signetics	5401	
	TI	SN5401	
MC5402	Fairchild	5402	
	ITT	ITT5402	
	National	DM5402	
	Signetics	5402	
	TI	SN5402	
MC5403	Fairchild	5403	
	ITT	ITT5403	
	National	DM5403	
	Raytheon	5403	
	Signetics	5403	
	TI	SN5403	
MC5404	Fairchild	5404	
	ITT	ITT5404	
	National	DM5404	
	Raytheon	5404	
	Signetics	5404	
	TI	SN5404	
MC5405	Fairchild	5405	
	ITT	ITT5405	
	National	DM5405	
	Raytheon	5405	
	Signetics	5405	
	TI	SN5405	
MC5406	Fairchild	5406	
	ITT	ITT5406	
	National	DM5406	
	Signetics	5406	
	TI	SN5406	
MC5407	Fairchild	5407	
	ITT	ITT5407	
	National	DM5407	
	Signetics	5407	
	TI	SN5407	
MC5408	Fairchild	5408	
	ITT	ITT5408	
	National	DM5408	
	Raytheon	5408	
	Signetics	5408	
	TI	SN5408	
MC5409	Fairchild	5409	
	ITT	ITT5409	
	National	DM5409	
	Raytheon	5409	
	Signetics	5409	
	TI	SN5409	
MC5410	Fairchild	5410	
	ITT	ITT5410	
	National	DM5410	
	Raytheon	5410	
	Signetics	5410	
	TI	SN5410	
MC54100	Signetics	54100	
	TI	SN54100	
MC54107	Fairchild	54107	
	ITT	ITT54107	
	National	DM54107	
	Signetics	54107	
	TI	SN54107	
MC5411	Raytheon	5411	
MC5412	Raytheon	5412	
MC54120	TI	SN54120	
MC54121	Fairchild	54121	
	ITT	ITT54121	
	National	DM54121	
	Signetics	54121	
	TI	SN54121	
MC54122	Fairchild	54122	
	ITT	ITT54122	
	TI	SN54122	
MC54123	AMD	SN54123	
	Fairchild	54123	
	ITT	ITT54123	
	National	DM54123	
	Raytheon	54123	
	Signetics	54123	
	TI	SN54123	
MC5413	Fairchild	5413	
	ITT	ITT5413	
	National	DM5413	
	Signetics	5413	
	TI	SN5413	
MC54132	Fairchild	54132	
	National	DM54132	
	Signetics	54132	
	TI	SN54132	
MC54136	Raytheon	54136	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Replacement Device	IC Master Page
MC5414	Fairchild	5414	
	National	DM5414	
	Signetics	5414	
	TI	SN5414	
MC54141	ITT	ITT54141	
	National	DM54141	
	TI	SN54141	
MC54145	Fairchild	54145	
	National	DM54145	
	Raytheon	54145	
	Signetics	54145	
	TI	SN54145	
MC5415	Raytheon	5415	
MC54150	Fairchild	54150	
	National	DM54150	
	Raytheon	54150	
	Signetics	54150	
	TI	SN54150	
MC54151	Fairchild	54151	
	ITT	ITT54151	
	National	DM54151	
	Raytheon	54151	
	Signetics	54151	
	TI	SN54151	
MC54152	Fairchild	54152	
	Raytheon	54152	
	Signetics	54152	
	TI	SN54152	
MC54153	Fairchild	54153	
	ITT	ITT54153	
	National	DM54153	
	Raytheon	54153	
	Signetics	54153	
	TI	SN54153	
MC54154	AMD	SN54154	
	Fairchild	54154	
	National	DM54154	
	Raytheon	54154	
	Signetics	54154	
	TI	SN54154	
MC54155	Fairchild	54155	
	ITT	ITT54155	
	National	DM54155	
	Raytheon	54155	
	Signetics	54155	
	TI	SN54155	
MC54156	Fairchild	54156	
	ITT	ITT54156	
	National	DM54156	
	Raytheon	54156	
	Signetics	54156	
	TI	SN54156	
MC54157	AMD	SN54157	
	Fairchild	54157	
	ITT	ITT54157	
	National	DM54157	
	Raytheon	54157	
	Signetics	54157	
	TI	SN54157	
MC54158	Raytheon	54158	
MC54159	Raytheon	54159	
MC5416	Fairchild	5416	
	ITT	ITT5416	
	National	DM5416	
	Signetics	5416	
	TI	SN5416	
MC54160	AMD	SN54160	
	Fairchild	54160	
	ITT	ITT54160	
	National	DM54160	
	Raytheon	54160	
	Signetics	54160	
	TI	SN54160	
MC54161	AMD	SN54161	
	Fairchild	54161	
	ITT	ITT54161	
	National	DM54161	
	Raytheon	54161	
	Signetics	54161	
	TI	SN54161	
MC54162	AMD	SN54162	
	Fairchild	54162	
MC54162	ITT	ITT54162	
	National	DM54162	
	Raytheon	54162	
	Signetics	54162	
	TI	SN54162	
MC54163	AMD	SN54163	
	Fairchild	54163	
	ITT	ITT54163	
	National	DM54163	
	Raytheon	54163	
	Signetics	54163	
	TI	SN54163	
♦MC54164	Raytheon	54164	
MC54165	Fairchild	54165	
	National	DM54165	
	Raytheon	54165	
	Signetics	54165	
	TI	SN54165	
MC54166	Raytheon	54166	
MC54167	TI	SN54167	
MC5417	Fairchild	5417	
	ITT	ITT5417	
	National	DM5417	
	Signetics	5417	
	TI	SN5417	
MC54170	Raytheon	54170	
MC54174	AMD	SN74174	
	Fairchild	54174	
	National	DM54174	
	Raytheon	54174	
	Signetics	54174	
	TI	SN54174	
MC54175	AMD	SN54175	
	Fairchild	54175	
	National	DM54175	
	Raytheon	54175	
	Signetics	54175	
	TI	SN54175	
MC54176	Fairchild	54176	
	National	DM54176	
	Signetics	54176	
	TI	SN54176	
MC54177	Fairchild	54177	
	National	DM54177	
	Signetics	54177	
	TI	SN54177	
MC54180	Fairchild	54180	
	ITT	ITT54180	
	National	DM54180	
	Raytheon	54180	
	Signetics	54180	
	TI	SN54180	
MC54181	AMD	SN54181	
	Fairchild	54181	
	National	DM54181	
	Raytheon	54181	
	Signetics	54181	
	TI	SN54181	
MC54182	AMD	SN54182	
	Fairchild	54182	
	ITT	ITT54182	
	National	DM54182	
	Raytheon	54182	
	Signetics	54182	
	TI	SN54182	
MC54190	Fairchild	54190	
	ITT	ITT54190	
	National	DM54190	
	Raytheon	54190	
	Signetics	54190	
	TI	SN54190	
MC54191	Fairchild	54191	
	ITT	ITT54191	
	National	DM54191	
	Raytheon	54191	
	Signetics	54191	
	TI	SN54191	
MC54192	AMD	SN54192	
	Fairchild	54192	
	ITT	ITT54192	
	National	DM54192	
	Raytheon	54192	
	Signetics	54192	
	TI	SN54192	
MC54193	AMD	SN54193	
	Fairchild	54193	
MC54193	ITT	ITT54193	
	National	DM54193	
	Raytheon	54193	
	Signetics	54193	
	TI	SN54193	
MC54194	AMD	SN54194	
	Fairchild	54194	
	ITT	ITT54194	
	National	DM54194	
	Raytheon	54194	
	Signetics	54194	
	TI	SN54194	
MC54195	AMD	SN54195	
	Fairchild	54195	
	ITT	ITT54195	
	National	DM54195	
	Raytheon	54195	
	Signetics	54195	
	TI	SN54195	
MC54196	Fairchild	54196	
	National	DM54196	
	Signetics	54196	
	TI	SN54196	
MC54197	Fairchild	54197	
	National	DM54197	
	Signetics	54197	
	TI	SN54197	
MC54198	Raytheon	54198	
MC54199	Raytheon	54199	
MC5420	Fairchild	5420	
	ITT	ITT5420	
	National	DM5420	
	Raytheon	5420	
	Signetics	5420	
	TI	SN5420	
MC5421	Raytheon	5421	
MC5422	Raytheon	5422	
MC5423	Fairchild	5423	
	National	DM5423	
	TI	SN5423	
MC5425	Fairchild	5425	
	ITT	ITT5425	
	National	DM5425	
	TI	SN5425	
MC5426	Fairchild	5426	
	ITT	ITT5426	
	National	DM5426	
	Signetics	5426	
	TI	SN5426	
MC5427	Fairchild	5427	
	National	DM5427	
	TI	SN5427	
MC54283	Raytheon	54283	
MC54290	TI	SN54290	
MC54293	TI	SN54293	
MC54298	Fairchild	54298	
	Signetics	54298	
	TI	SN54298	
MC5430	Fairchild	5430	
	ITT	ITT5430	
	National	DM5430	
	Signetics	5430	
	TI	SN5430	
MC5437	Fairchild	5437	
	ITT	ITT5437	
	National	DM5437	
	Raytheon	5437	
	Signetics	5437	
	TI	SN5437	
MC5438	Fairchild	5438	
	ITT	ITT5438	
	National	DM5438	
	Raytheon	5438	
	Signetics	5438	
	TI	SN5438	
MC5440	Fairchild	5440	
	ITT	ITT5440	
	National	DM5440	
	Signetics	5440	
	TI	SN5440	
MC5442	Fairchild	5442	
	ITT	ITT5442	
	National	DM5442	
	Raytheon	5442	
	Signetics	5442	
	TI	SN5442	
MC5443	Fairchild	5443	
	ITT	ITT5443	
	Raytheon	5443	
	Signetics	5443	
	TI	SN5443	
MC5444	Fairchild	5444	
	ITT	ITT5444	
	Raytheon	5444	
	Signetics	5444	
	TI	SN5444	
MC5445	Fairchild	5445	
	ITT	ITT5445	
	National	DM5445	
	Raytheon	5445	
	Signetics	5445	
	TI	SN5445	
MC5446	Fairchild	5446	
	ITT	ITT5446	
	National	DM5446	
	Signetics	5446	
	TI	SN5446	
MC5447	Fairchild	5447	
	ITT	ITT5447	
	National	DM5447	
	Signetics	5447	
	TI	SN5447	
MC5448	Fairchild	5448	
	ITT	ITT5448	
	National	DM5448	
	Signetics	5448	
	TI	SN5448	
MC5449	Fairchild	5449	
	TI	SN5449	
MC5450	Fairchild	5450	
	ITT	ITT5450	
	National	DM5450	
	Signetics	5450	
	TI	SN5450	
MC5451	Fairchild	5451	
	ITT	ITT5451	
	National	DM5451	
	Signetics	5451	
	TI	SN5451	
MC5453	Fairchild	5453	
	ITT	ITT5453	
	National	DM5453	
	Signetics	5453	
	TI	SN5453	
MC5454	Fairchild	5454	
	ITT	ITT5454	
	National	DM5454	
	Signetics	5454	
	TI	SN5454	
MC5460	Fairchild	5460	
	National	DM5460	
	Signetics	5460	
	TI	SN5460	
MC5470	Fairchild	5470	
	ITT	ITT5470	
	National	DM5470	
	TI	SN5470	
MC5472	Fairchild	5472	
	ITT	ITT5472	
	National	DM5472	
	Signetics	5472	
	TI	SN5472	
MC5473	Fairchild	5473	
	ITT	ITT5473	
	National	DM5473	
	Signetics	5473	
	TI	SN5473	
MC5474	Fairchild	5474	
	ITT	ITT5474	
	National	DM5474	
	Raytheon	5474	
	Signetics	5474	
	TI	SN5474	
MC5475	Fairchild	5475	
	ITT	ITT5475	
	National	DM5475	
	Signetics	5475	
	TI	SN5475	
MC5476	Fairchild	5476	
	ITT	ITT5476	
	National	DM5476	
	Signetics	5476	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Motorola Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
MC5476	TI	SN5476	
MC5477	Fairchild	5477	
	Signetics	5477	
	TI	SN5477	
MC5480	Fairchild	5480	
	ITT	ITT5480	
	Signetics	5480	
	TI	SN5480	
MC5482	Fairchild	5482	
	ITT	ITT5482	
	TI	SN5482	
MC5483	Raytheon	5483	
MC5485	Fairchild	5485	
	National	DM5485	
	Signetics	5485	
	TI	SN5485	
MC5486	Fairchild	5486	
	ITT	ITT5486	
	National	DM5486	
	Raytheon	5486	
	Signetics	5486	
	TI	SN5486	
MC5490	Fairchild	5490	
	ITT	ITT5490	
	National	DM5490	
	Signetics	5490	
	TI	SN5490	
MC5491	Fairchild	5491	
	ITT	ITT5491	
	National	DM5491	
	Signetics	5491	
	TI	SN5491	
MC5492	Fairchild	5492	
	ITT	ITT5492	
	National	DM5492	
	Signetics	5492	
	TI	SN5492	
MC5493	Fairchild	5493	
	ITT	ITT5493	
	National	DM5493	
	TI	SN5493	
MC5494	Fairchild	5494	
	TI	SN5494	
MC5495	Fairchild	5495	
	ITT	ITT5495	
	National	DM5495	
	Signetics	5495	
	TI	SN5495	
MC5496	Fairchild	5496	
	ITT	ITT5496	
	National	DM5496	
	Signetics	5496	
	TI	SN5496	
MC5497	Fairchild	5497	
	TI	SN5497	
MC55107	AMD	SN55107	
	Fairchild	55107	
	National	**DS55107**	**504**
	Raytheon	RM55107	
	TI	SN55107	
MC55108	AMD	SN55108	
	Fairchild	55108	
	National	**DS55108**	**504**
	Raytheon	RM55108	
	TI	SN55108	
♦MC55109	AMD	SN55109	
	Fairchild	55109	
	Raytheon	RM55109	
	TI	SN55109	
♦MC55110	AMD	SN55110	
	Fairchild	55110	
	Raytheon	RM55110	
	TI	SN55110	
♦MC5522	National	DS5522	
	TI	SN5522	
♦MC5523	National	DS5523	
	TI	SN5522	
MC5524	AMD	SN5524	
	National	DS5524	
	TI	SN5524	
MC5525	AMD	SN5525	
	National	DS5525	
MC5525	TI	SN5524	
MC5528	Fairchild	5528	
	TI	SN5528	
MC5529	Fairchild	5529	
MC55325	AMD	SN55325	
	Fairchild	55325	
	TI	SN55325	
MC5534	Fairchild	5534	
MC5535	Fairchild	5535	
MC6002	TI	TMS4062	
MC68A00	**AMI**	**S68A00**	**1548**
MC68A10	**AMI**	**S68A10**	**1552**
MC68A21	**AMI**	**S68A21**	**1556**
MC68A50	**AMI**	**S68A50**	**1567**
MC68B00	**AMI**	**S68B00**	**1548**
MC68B10	**AMI**	**S68B10**	**1552**
MC68B21	**AMI**	**S68B21**	**1556**
MC68B50	**AMI**	**S68B50**	**1567**
MC6800	**AMI**	**S6800**	**1538,1548**
	Fairchild	F6800	
		F6800A	
	Hitachi	M6800	
MC6802	Fairchild	F6802	
MC6820	**AMI**	**S6820**	**1556**
	Fairchild	F6820A	
MC6850	**AMI**	**S6850**	**1567**
	Fairchild	F6850	
MC6860	Fairchild	F6860	
MC7241	Raytheon	RC8241	
	Signetics	N8241	
MC7242	Fairchild	9386	
	Raytheon	RC8242	
	Signetics	N8242	
MC7250	Raytheon	RC8250	
	Signetics	N8250	
MC7251	Raytheon	RC8251	
	Signetics	N8251	
MC7261	Raytheon	RC8261	
	Signetics	N8261	
MC73525	AMD	SN75325	
MC74H00	Raytheon	74H00	
MC74H01	Raytheon	74H01	
MC74H04	Raytheon	74H04	
MC74H05	Raytheon	74H05	
MC74H10	Raytheon	74H10	
MC74H11	Raytheon	74H11	
MC74H20	Raytheon	74H20	
MC74H22	Raytheon	74H22	
MC74H40	Raytheon	74H40	
MC74H74	Raytheon	74H74	
MC74H87	Fairchild	74H87	
	TI	SN74H87	
MC7400	Fairchild	7400	
	Hitachi	HD2503	
		HD7400	
	ITT	ITT7400	
	Mitsubishi	M53200	
	National	DM7400	
	NEC America	μPB7400	
	Raytheon	7400	
	Signetics	7400	
	TI	SN7400	
	Toshiba	TC7400	
	TRW	7400	
MC7401	Fairchild	7401	
	Hitachi	HD2509	
	ITT	ITT7401	
	Mitsubishi	M53201	
	National	DM7401	
	Raytheon	7401	
	Signetics	7401	
	TI	SN7401	
	TRW	7401	
MC7402	Fairchild	7402	
	Hitachi	HD2511	
		HD7402	
	ITT	ITT7402	
	Mitsubishi	M53202	
	National	DM7402	
	NEC America	μPB7402	
	Signetics	7402	
	TI	SN7402	
	TRW	7402	
MC7403	Fairchild	7403	
	Hitachi	HD7403	
	ITT	ITT7403	
MC7403	Mitsubishi	M53203	
	National	DM7403	
	Raytheon	7403	
	Signetics	7403	
	TI	SN7403	
	TRW	7403	
MC7404	Fairchild	7404	
	Hitachi	HD2522	
		HD7404	
	ITT	ITT7404	
	Mitsubishi	M53204	
	National	DM7404	
	NEC America	μPB7404	
	Raytheon	7404	
	Signetics	7404	
	TI	SN7404	
	Toshiba	TC7404	
	TRW	7404	
MC7405	Fairchild	7405	
	Hitachi	HD2523	
		HD7405	
	ITT	ITT7405	
	Mitsubishi	M53205	
	National	DM7405	
	NEC America	μPB7405	
	Raytheon	7405	
	Signetics	7405	
	TI	SN7405	
	TRW	7405	
MC7406	Fairchild	7406	
	Hitachi	HD7406	
	ITT	ITT7406	
	Mitsubishi	M53206	
	National	DM7406	
	Signetics	7406	
	TI	SN7406	
	TRW	7406	
MC7407	Fairchild	7407	
	Hitachi	HD7407	
	ITT	ITT7407	
	Mitsubishi	M53207	
	National	DM7407	
	Signetics	7407	
	TI	SN7407	
	TRW	7407	
MC7408	Fairchild	7408	
	ITT	ITT7408	
	Mitsubishi	M53208	
	National	DM7408	
	Raytheon	7408	
	Signetics	7408	
	TI	SN7408	
	Toshiba	TC7408	
	TRW	7408	
MC7409	Fairchild	7409	
	Hitachi	HD7409	
	ITT	ITT7409	
	Mitsubishi	M53209	
	National	DM7409	
	Raytheon	7409	
	Signetics	7409	
	TI	SN7409	
	TRW	7409	
MC7410	Fairchild	7410	
	Hitachi	HD2507	
		HD7410	
	ITT	ITT7410	
	Mitsubishi	M53210	
	National	DM7410	
	NEC America	μPB7410	
	Raytheon	7410	
	Signetics	7410	
	TI	SN7410	
		SN7427	
	Toshiba	TC7410	
	TRW	7410	
MC74100	Signetics	74100	
	TI	SN74100	
MC74107	Fairchild	74107	
	Hitachi	HD2530	
		HD74107	
	ITT	ITT74107	
	Mitsubishi	M53307	
	National	DM74107	
	NEC America	μPB74107	
	Signetics	74107	
MC74107	TI	SN74107	
MC7411	Raytheon	7411	
MC7412	Raytheon	7412	
MC74120	TI	SN74120	
MC74121	Fairchild	74121	
	Hitachi	HD2543	
		HD74121	
	ITT	ITT74121	
	Mitsubishi	M53321	
	National	DM74121	
	Signetics	74121	
	TI	SN74121	
	TRW	74121	
MC74122	Fairchild	74122	
	ITT	ITT74122	
	Mitsubishi	M53322	
	Signetics	74122	
	TI	SN74122	
MC74123	AMD	SN74123	
	Fairchild	74123	
	ITT	ITT74123	
	Mitsubishi	M53323	
	National	DM74123	
	NEC America	μPB74123	
	Raytheon	74123	
	Signetics	74123	
	TI	SN74123	
	TRW	74123	
MC7413	Fairchild	7413	
	ITT	ITT7413	
	Mitsubishi	M53213	
	National	DM7413	
	NEC America	μPB7413	
	Signetics	7413	
	TI	SN7413	
	TRW	7413	
MC74132	Fairchild	74132	
	Hitachi	HD74132	
	Mitsubishi	M53332	
	National	DM74132	
	Signetics	74132	
	TI	SN74132	
MC74136	Hitachi	HD74136	
	Raytheon	74136	
	TI	SN74136	
	TRW	74136	
MC7414	Fairchild	7414	
	Hitachi	HD7414	
	Mitsubishi	M53214	
	National	DM7414	
	Signetics	7414	
	TI	SN7414	
MC74141	Fairchild	74141	
	National	DM74141	
	NEC America	μPB74141	
	TI	SN74141	
MC74145	Fairchild	74145	
	ITT	ITT74145	
	Mitsubishi	M53345	
	National	DM74145	
	Raytheon	74145	
	Signetics	74145	
	TI	SN74145	
	TRW	74145	
MC7415	Raytheon	7415	
MC74150	Fairchild	74150	
	Hitachi	HD2548	
		HD74150	
	Mitsubishi	M53350	
	National	DM74150	
	NEC America	μPB74150	
	Raytheon	74150	
	Signetics	74150	
	TI	SN74150	
	TRW	74150	
MC74151	Fairchild	74151	
	Hitachi	HD2549	
		HD74151	
	ITT	ITT74151	
	Mitsubishi	M53351	
	National	DM74151	
	NEC America	μPB74151	
	Raytheon	74151	
	Signetics	74151	
	TI	SN74151	
		SN74151A	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Manufacturer Device	Replacement Source	Device	IC Master Page
Motorola Semiconductor (cont'd)			
MC74151	TRW	74151	
MC74152	Fairchild	74152	
	Raytheon	74152	
	TRW	74152	
MC74153	Fairchild	74153	
	ITT	ITT74153	
	Mitsubishi	M53353	
	National	DM74153	
	NEC America	μPB74153	
	Raytheon	74153	
	Signetics	74153	
	TI	SN74153	
	TRW	74153	
MC74154	AMD	SN74154	
	Fairchild	74154	
	Mitsubishi	M53354	
	National	DM74154	
	NEC America	μPB74154	
	Raytheon	74154	
	Signetics	74154	
	TI	SN74154	
	TRW	74154	
MC74155	Fairchild	74155	
	ITT	ITT74155	
	Mitsubishi	M53355	
	National	DM74155	
	NEC America	μPB74155	
	Raytheon	74155	
	Signetics	74155	
	TI	SN74155	
	TRW	74155	
MC74156	Fairchild	74156	
	Hitachi	HD74156	
	ITT	ITT74156	
	Mitsubishi	M53356	
	National	DM74156	
	NEC America	μPB74156	
	Raytheon	74156	
	Signetics	74156	
	TI	SN74156	
	TRW	74156	
MC74157	AMD	SN74157	
	Fairchild	74157	
	Hitachi	HD74157	
	ITT	ITT74157	
	Mitsubishi	M53357	
	National	DM74157	
	NEC America	μPB74157	
	Raytheon	74157	
	Signetics	74157	
	TI	SN74157	
MC74158	Raytheon	74158	
MC74159	Raytheon	74159	
MC7416	Fairchild	7416	
	Hitachi	HD7416	
	ITT	ITT7416	
	Mitsubishi	M53216	
	National	DM7416	
	Signetics	7416	
	TI	SN7416	
	TRW	7416	
MC74160	AMD	SN74160	
	Fairchild	74160	
	Hitachi	HD74160	
	ITT	ITT74160	
	Mitsubishi	M53360	
	National	DM74160	
	Raytheon	74160	
	Signetics	74160	
	TI	SN74160	
	TRW	74160	
MC74161	AMD	SN74161	
	Fairchild	74161	
	Hitachi	HD74161	
	ITT	ITT74161	
	Mitsubishi	M53361	
	National	DM74161	
	NEC America	μPB74161	
	Raytheon	74161	
	Signetics	74161	
	TI	SN74161	
	TRW	74161	
MC74162	AMD	SN74162	
	Fairchild	74162	
	Hitachi	HD74162	
	ITT	ITT74162	
	Mitsubishi	M53362	
	National	DM74162	
	Raytheon	74162	
	Signetics	74162	
	TI	SN74162	
	TRW	74162	
MC74163	AMD	SN74163	
	Fairchild	74163	
	Hitachi	HD74163	
	ITT	ITT74163	
	Mitsubishi	M53363	
	National	DM74163	
	Raytheon	74163	
	Signetics	74163	
	TI	SN74163	
	TRW	74163	
♦MC74164	Raytheon	74164	
MC74165	Fairchild	74165	
	Mitsubishi	M53365	
	National	DM74165	
	Raytheon	74165	
	Signetics	74165	
	TI	SN74165	
MC74166	Raytheon	74166	
MC74167	TI	SN74167	
MC7417	Fairchild	7417	
	Hitachi	HD7417	
	ITT	ITT7417	
	Mitsubishi	M53217	
	National	DM7417	
	Signetics	7417	
	TI	SN7417	
	TRW	7417	
MC74170	Raytheon	74170	
MC74174	AMD	SN74174	
	Fairchild	74174	
	Hitachi	HD74174	
	Mitsubishi	M53374	
	National	DM74174	
	Raytheon	74174	
	Signetics	74174	
	TI	SN74174	
MC74175	AMD	SN74175	
	Fairchild	74175	
	Hitachi	HD74175	
	Mitsubishi	M53375	
	National	DM74175	
	NEC America	μPB74175	
	Raytheon	74175	
	Signetics	74175	
	TI	SN74175	
MC74176	Fairchild	74176	
	Mitsubishi	M53376	
	National	DM74176	
	Signetics	74176	
	TI	SN74176	
MC74177	Fairchild	74177	
	Mitsubishi	M53377	
	National	DM74177	
	Signetics	74177	
	TI	SN74177	
MC74180	Fairchild	74180	
	Hitachi	HD74180	
	ITT	ITT74180	
	Mitsubishi	M53380	
	National	DM74180	
	NEC America	μPB74180	
	Raytheon	74180	
	Signetics	74180	
	TI	SN74180	
	TRW	74180	
MC74181	AMD	SN74181	
	Fairchild	74181	
	Mitsubishi	M53381	
	National	DM74181	
	NEC America	μPB74181	
	Raytheon	74181	
	Signetics	74181	
	TI	SN74181	
MC74182	AMD	SN74182	
	Fairchild	74182	
	ITT	ITT74182	
MC74182	Mitsubishi	M53382	
	National	DM74182	
	NEC America	μPB74182	
	Raytheon	74182	
	Signetics	74182	
	TI	SN74182	
MC74190	Fairchild	74190	
	Hitachi	HD74190	
	ITT	ITT74190	
	Mitsubishi	M53390	
	National	DM74190	
	Raytheon	74190	
	Signetics	74190	
	TI	SN74190	
MC74191	Fairchild	74191	
	Hitachi	HD74191	
	ITT	ITT74191	
	Mitsubishi	M53391	
	National	DM74191	
	Raytheon	74191	
	Signetics	74191	
	TI	SN74191	
MC74192	AMD	SN74192	
	Fairchild	74192	
	ITT	ITT74192	
	Mitsubishi	M53392	
	National	DM74192	
	NEC America	μPB74192	
	Raytheon	74192	
	Signetics	74192	
	TI	SN74192	
MC74193	AMD	SN74193	
	Fairchild	74193	
	ITT	ITT74193	
	Mitsubishi	M53393	
	National	DM74193	
	NEC America	μPB74193	
	Raytheon	74193	
	Signetics	74193	
	TI	SN74193	
MC74194	AMD	SN74194	
	Fairchild	74194	
	Hitachi	HD74194	
	ITT	ITT74194	
	National	DM74194	
	Raytheon	74194	
	Signetics	74194	
	TI	SN74194	
MC74195	AMD	SN74195	
	Fairchild	74195	
	ITT	ITT74195	
	National	DM74195	
	NEC America	μPB74195	
	Raytheon	74195	
	Signetics	74195	
	TI	SN74195	
MC74196	Fairchild	74196	
	National	DM74196	
	Signetics	74196	
	TI	SN74196	
MC74197	Fairchild	74197	
	National	DM74197	
	Signetics	74197	
	TI	SN74197	
MC74198	Raytheon	74198	
MC74199	Raytheon	74199	
MC7420	Fairchild	7420	
	Hitachi	HD2504	
		HD7420	
	ITT	ITT7420	
	Mitsubishi	M53220	
	National	DM7420	
	NEC America	μPB7420	
	Raytheon	7420	
	Signetics	7420	
	TI	SN7420	
	Toshiba	TC7420	
	TRW	7420	
MC7421	Raytheon	7421	
MC7422	Raytheon	7422	
MC7423	Fairchild	7423	
	National	DM7423	
	TI	SN7423	
MC7425	Fairchild	7425	
	ITT	ITT7425	
	Mitsubishi	M53225	
MC7425	National	DM7425	
	TI	SN7425	
MC7426	Fairchild	7426	
	Hitachi	HD7426	
	ITT	ITT7426	
	National	DM7426	
	Signetics	7426	
	TI	SN7426	
	TRW	7426	
MC7427	Fairchild	7427	
	Hitachi	HD7427	
	Mitsubishi	M53227	
	National	DM7427	
	Signetics	7427	
MC74283	Raytheon	74283	
MC74290	Fairchild	74290	
	Mitsubishi	M53490	
	TI	SN74290	
	TRW	74290	
MC74293	Fairchild	74293	
	Mitsubishi	M53493	
	TI	SN74293	
	TRW	74293	
MC74298	Fairchild	74298	
	Signetics	74298	
	TI	SN74298	
MC7430	Fairchild	7430	
	Hitachi	HD2508	
		HD7430	
	ITT	ITT7430	
	Mitsubishi	M53230	
	National	DM7430	
	NEC America	μPB7430	
	Signetics	7430	
	TI	SN7430	
	TRW	7430	
MC7437	Fairchild	7437	
	ITT	ITT7437	
	Mitsubishi	M53237	
	National	DM7437	
	NEC America	μPB7437	
	Raytheon	7437	
	Signetics	7437	
	TI	SN7437	
	TRW	7437	
MC7438	Fairchild	7438	
	ITT	ITT7438	
	Mitsubishi	M53238	
	National	DM7438	
	NEC America	μPB7438	
	Raytheon	7438	
	Signetics	7438	
	TI	SN7438	
	TRW	7438	
MC7440	Fairchild	7440	
	Hitachi	HD2501	
		HD7440	
	ITT	ITT7440	
	Mitsubishi	M53240	
	National	DM7440	
	NEC America	μPB7440	
	Signetics	7440	
	TI	SN7440	
	TRW	7440	
♦MC7441	Hitachi	HD2518	
	TI	SN74141	
MC7442	Fairchild	7442	
	Hitachi	HD7442	
	ITT	ITT7442	
	Mitsubishi	M53242	
	National	DM7442	
	NEC America	μPB7442	
	Raytheon	7442	
	Signetics	7442	
	TI	SN7442	
MC7443	Fairchild	7443	
	Hitachi	HD7443	
	ITT	ITT7443	
	Mitsubishi	M53243	
	Raytheon	7443	
	Signetics	7443	
	TI	SN7443	
MC7444	Fairchild	7444	
	Hitachi	HD7444	
	ITT	ITT7444	
	Mitsubishi	M53244	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Motorola Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
MC7444	Raytheon	7444	
	Signetics	7444	
	TI	SN7444	
MC7445	Fairchild	7445	
	ITT	ITT7445	
	Mitsubishi	M53245	
	National	DM7445	
	NEC America	μPB7445	
	Raytheon	7445	
	Signetics	7445	
	TI	SN7445	
	TRW	7445	
MC7446	Fairchild	7446	
	ITT	ITT7446	
	National	DM7446	
	Signetics	7446	
	TI	SN7446	
MC7447	Fairchild	7447	
	ITT	ITT7447	
	Mitsubishi	M53247	
	National	DM7447	
	NEC America	μPB7447	
	Signetics	7447	
	TI	SN7447	
MC7448	Fairchild	7448	
	ITT	ITT7448	
	Mitsubishi	M53248	
	National	DM7448	
	Signetics	7448	
	TI	SN7448	
MC7449	Fairchild	7449	
	TI	SN7449	
MC7450	Fairchild	7450	
	Hitachi	HD2506	
		HD7450	
	ITT	ITT7450	
	Mitsubishi	M53250	
	National	DM7450	
	NEC America	μPB7450	
	Signetics	7450	
	TI	SN7450	
	TRW	7450	
MC7451	Fairchild	7451	
	Hitachi	HD2505	
		HD7451	
	ITT	ITT7451	
	National	DM7451	
	NEC America	μPB7451	
	Signetics	7451	
	TI	SN7451	
	TRW	7451	
MC7453	Fairchild	7453	
	Hitachi	HD2512	
		HD7453	
	ITT	ITT7453	
	Mitsubishi	M53253	
	National	DM7453	
	NEC America	μPB7453	
	Signetics	7453	
	TI	SN7453	
	TRW	7453	
MC7454	Fairchild	7454	
	Hitachi	HD2514	
		HD7454	
	ITT	ITT7454	
	National	DM7454	
	NEC America	μPB7454	
	Signetics	7454	
	TI	SN7454	
	TRW	7454	
MC7460	Fairchild	7460	
	Hitachi	HD2502	
		HD7460	
	Mitsubishi	M53260	
	National	DM7460	
	NEC America	μPB7460	
	Signetics	7460	
	TI	SN7460	
	TRW	7460	
MC7470	Fairchild	7470	
	ITT	ITT7470	
	Mitsubishi	M53270	
MC7470	National	DM7470	
	Signetics	7470	
	TI	SN7470	
MC7472	Fairchild	7472	
	Hitachi	HD2529	
		HD7472	
	ITT	ITT7472	
	Mitsubishi	M53272	
	National	DM7472	
	Signetics	7472	
	TI	SN7472	
	TRW	7472	
MC7473	Fairchild	7473	
	Hitachi	HD2515	
	ITT	ITT7473	
	Mitsubishi	M53273	
	National	DM7473	
	NEC America	μPB7473	
	Signetics	7473	
	TI	SN7473	
MC7474	Fairchild	7474	
	Hitachi	HD2510	
		HD7474	
	ITT	ITT7474	
	Mitsubishi	M53274	
	National	DM7474	
	NEC America	μPB7474	
	Raytheon	MC7474	
		7474	
	Signetics	7474	
	TI	SN7474	
	TRW	7474	
MC7475	Fairchild	7475	
	Hitachi	HD2517	
		HD7475	
	ITT	ITT7475	
	Mitsubishi	M53275	
	National	DM7475	
	Signetics	7475	
	TI	SN7475	
	TRW	7475	
MC7476	Fairchild	7476	
	Hitachi	HD2516	
	ITT	ITT7476	
	Mitsubishi	M53276	
	National	DM7476	
	NEC America	μPB7476	
	Signetics	7476	
	TI	SN7476	
	TRW	7476	
MC7477	Fairchild	7477	
	Signetics	7477	
	TI	SN7477	
MC7480	Fairchild	7480	
	ITT	ITT7480	
	Mitsubishi	M53280	
	NEC America	μPB7480	
	Signetics	7480	
	TI	SN7480	
MC7482	Fairchild	7482	
	ITT	ITT7482	
	TI	SN7482	
MC7483	Fairchild	7483	
	ITT	ITT7483	
	Mitsubishi	M53283	
	National	DM7483	
	Raytheon	7483	
	Signetics	7483	
	TI	SN7483	
MC7485	Fairchild	7485	
	Hitachi	HD7485	
	Mitsubishi	M53285	
	National	DM7485	
	NEC America	μPB7485	
	Signetics	7485	
	TI	SN7485	
	TRW	7485	
MC7486	Fairchild	7486	
	Hitachi	HD7486	
	ITT	ITT7486	
	Mitsubishi	M53286	
	National	DM7486	
	NEC America	μPB7486	
	Raytheon	7486	
	Signetics	7486	
	TI	SN7486	
MC7486	TRW	7486	
MC7490	Fairchild	7490	
	Hitachi	HD2541	
		HD7490	
	ITT	ITT7490	
	Mitsubishi	M53290	
	National	DM7490	
	Signetics	7490	
	TI	SN7490	
		SN7490A	
	TRW	7490	
MC7491	Fairchild	7491	
	Hitachi	HD2524	
	ITT	ITT7491	
	Mitsubishi	M53291	
	National	DM7491	
	NEC America	μPB7491	
	Signetics	7491	
	TI	SN7491	
		SN7491A	
MC7492	Fairchild	7492	
	Hitachi	HD7492	
	ITT	ITT7492	
	Mitsubishi	M53292	
	National	DM7492	
	Signetics	7492	
	TI	SN7492	
		SN7492A	
	TRW	7492	
MC7493	Fairchild	7493	
	Hitachi	HD2520	
		HD7493	
	ITT	ITT7493	
	Mitsubishi	M53293	
	National	DM7493	
	Signetics	7493	
	TI	SN7493	
		SN7493A	
	TRW	7493	
MC7494	Fairchild	7494	
	TI	SN7494	
MC7495	Fairchild	7495	
	Hitachi	HD2534	
	ITT	ITT7495	
	Mitsubishi	M53295	
	National	DM7495	
	Signetics	7495	
	TI	SN7495	
		SN7495A	
MC7496	Fairchild	7496	
	Hitachi	HD2546	
		HD7496	
	ITT	ITT7496	
	Mitsubishi	M53296	
	National	DM7496	
	Signetics	7496	
	TI	SN7496	
	TRW	7496	
MC7497	Fairchild	7497	
	TI	SN7497	
♦MC75107	AMD	SN75107	
	Fairchild	75107	
	National	**DS75107**	**504**
	Raytheon	RC75107	
	TI	SN75107A	
♦MC75108	AMD	SN75108	
	Fairchild	75108	
	National	**DS75108**	**504**
	Raytheon	RC75108	
	TI	SN75108A	
MC75109	AMD	SN75109	
	Fairchild	75109	
	ITT	ITT75109	
	Raytheon	RC75109	
	TI	SN75109	
MC75110	AMD	SN75110	
	Fairchild	75110	
	ITT	ITT75110	
	Raytheon	RC75110	
	TI	SN75110	
MC75140	TI	SN75140	
MC7520	ITT	ITT7520	
	National	DS7520	
	Signetics	7520	
●	Silicon G	SG7520	
	TI	SN7520	
MC7521	National	DS7521	
	Signetics	7521	
	Silicon G	SG7521	
♦MC7522	ITT	ITT7522	
	National	DS7522	
	Signetics	7522	
	Silicon G	SG7522	
	TI	SN7522	
♦MC7523	National	DS7523	
	Signetics	7523	
	Silicon G	SG7523	
	TI	SN7522	
MC75235	ITT	ITT75235	
MC7524	AMD	SN7524	
	Fairchild	7524	
	National	DS7524	
	Signetics	7524	
	Silicon G	SG7524	
	TI	SN7524	
MC7525	AMD	SN7525	
	Fairchild	7525	
	National	DS7525	
	Signetics	7525	
	Silicon G	SG7525	
	TI	SN7524	
MC7528	Fairchild	7528	
	ITT	ITT7528	
	National	DS7528	
	Silicon G	SG7528	
	TI	SN7528	
MC7529	Fairchild	7529	
	Silicon G	SG7529	
	TI	SN7528	
MC75325	Fairchild	75325	
	National	**DS75325**	**520**
	Raytheon	RC75325	
	Silicon G	SG75325	
	TI	SN75325	
MC7534	Fairchild	7534	
	ITT	ITT7534	
	National	DS7534	
	Silicon G	SG7534	
MC7535	Fairchild	7535	
	National	DS7535	
	Silicon G	SG7535	
MC75358	TI	SN75368	
MC75365	TI	SN75365	
MC75368	TI	SN75368	
MC7538	National	DS7538	
	Silicon G	SG7538	
MC7539	National	DS7539	
	Silicon G	SG7539	
MC75450	Fairchild	75450	
	ITT	ITT75450	
	National	DS75450	
	Raytheon	RC75450	
	Silicon G	SG75450	
	TI	●SN75450	
MC75451	Fairchild	75451	
	ITT	ITT75451	
	National	DS75451	
	Raytheon	RC75451	
	Silicon G	SG75451	
	TI	SN75451	
MC75452	Fairchild	75452	
	National	DS75452	
	Raytheon	RC75452	
	Silicon G	SG75452	
	TI	SN75452	
MC75453	Fairchild	75453	
	ITT	ITT75453	
	National	DS75453	
	Raytheon	RC75453	
	Silicon G	SG75453	
	TI	SN75453	
MC75454	Fairchild	75454	
	ITT	ITT75454	
	Silicon G	SG75454	
	TI	SN75454	
MC75460	TI	SN75460	
MC75461	TI	SN75461	
MC75462	TI	SN75462	
MC75463	TI	SN75463	
MC75464	TI	SN75464	
MC75491	Fairchild	75491	
	National	DS75491	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
MC75491	TI	SN75491	
MC75492	Fairchild	75492	
	National	DS75492	
	TI	SN75492	
MC7705	Signetics	μA78M05	
MC7706	Signetics	μA78M06	
MC78L02	Signetics	μA78L02	
MC78L02.6	TI	μA78L02	
MC78L05	Signetics	μA78L05	
	TI	μA78L05	
MC78L06.2	TI	μA78L06	
MC78L08	Signetics	μA78L08	
	TI	μA78L08	
MC78L12	Signetics	μA78L12	
	TI	μA78L12	
MC78L15	Signetics	μA78L15	
	TI	μA78L15	
MC78L24	Signetics	μA78L24	
MC78M05	Signetics	μA78M05	
	TI	μA78M05	
MC78M06	Signetics	μA78M06	
	TI	μA78M06	
MC78M08	TI	μA78M08	
MC78M12	TI	μA78M12	
MC78M15	TI	μA78M15	
MC78M20	TI	μA78M20	
MC78M24	TI	μA78M24	
MC7805	Fairchild	μA7805	
	National	**LM340-5**	**806**
	Raytheon	RC7805	
	Signetics	μA7805	
	Silicon G	SG7805	
	TI	μA7805	
MC7806	Fairchild	μA7806	
	National	**LM340-6**	**806**
	Raytheon	RC7806	
	Signetics	μA7806	
	Silicon G	SG7806	
	TI	μA7806	
MC7808	Fairchild	μA7808	
	National	**LM340-8**	**806**
	Raytheon	RC7808	
	Signetics	μA7808	
	Silicon G	SG7808	
	TI	μA7808	
MC7812	Fairchild	μA7812	
	National	**LM340-12**	**806**
	Raytheon	RC7812	
	Signetics	μA7812	
	Silicon G	SG7812	
	TI	μA7812	
MC7815	Fairchild	μA7815	
	National	**LM340-15**	**806**
	Raytheon	RC7815	
	Signetics	μA7815	
	Silicon G	SG7815	
	TI	μA7815	
MC7818	Fairchild	μA7818	
	National	**LM340-18**	**806**
	Raytheon	RC7818	
	Signetics	μA7818	
	Silicon G	SG7818	
	TI	μA7818	
MC7824	Fairchild	μA7824	
	National	**LM340-24**	**806**
	Raytheon	RC7824	
	Signetics	μA7824	
	Silicon G	SG7824	
	TI	μA7824	
MC7905	Fairchild	μA7905	
	National	LM7905	
	Signetics	μA7905	
	Silicon G	SG320	
	TI	μA7905	
MC7905.2	Signetics	μA7905.2	
MC7906	Fairchild	μA7906	
	National	LM7906	
	Signetics	μA7906	
	TI	μA7906	
MC7908	Fairchild	μA7908	
	National	LM7908	
	Signetics	μA7908	
MC7908	TI	μA7908	
MC7912	Fairchild	μA7912	
	National	LM7912	
	Signetics	μA7912	
	Silicon G	SG320	
	TI	μA7912	
MC7915	Fairchild	μA7915	
	National	LM7915	
	Signetics	μA7915	
	Silicon G	SG320	
	TI	μA7915	
MC7918	Fairchild	μA7918	
	Nitron	LM7918	
	Signetics	μA7918	
	TI	μA7918	
MC7924	Fairchild	μA7924	
	National	LM7924	
	Signetics	μA7924	
	TI	μA7924	
MC7952	Silicon G	SG320	
MC8T13	Fairchild	8T13	
	TI	SN75121	
MC8T14	Fairchild	8T14	
	TI	SN75122	
MC8T23	Fairchild	8T23	
	TI	SN75123	
MC8T24	Fairchild	8T24	
	TI	SN75124	
MC8T26	AMD	N8T26	
	Signetics	N8T26	
MC8T28	Signetics	N8T28	
MC8241	Raytheon	RM8241	
	Signetics	S8241	
MC8242	Fairchild	9386	
	Raytheon	RM8242	
	Signetics	S8242	
MC8250	Raytheon	RM8250	
	Signetics	S8250	
MC8251	Raytheon	RM8251	
	Signetics	S8251	
MC8260	Raytheon	RM8260	
MC8261	Raytheon	RM8261	
	Signetics	S8261	
MC830	Hitachi	HD2204	
	National	DM930	
	TI	SN15930	
MC8300	AMD	9300	
	Fairchild	9300	
	Raytheon	RC9300	
	TI	SN74195	
MC8301	AMD	9301	
	Fairchild	9301	
	Signetics	N8252	
	TI	SN29301	
MC8304	AMD	9304	
	Fairchild	9304	
	Raytheon	RC9304	
MC8308	AMD	9308	
	Fairchild	9308	
	Raytheon	RC9308	
	TI	SN29308	
MC8309	AMD	9309	
	Fairchild	9309	
	TI	SN29309	
MC831	TI	SN15831	
MC8310	AMD	9310	
	Fairchild	9310	
	Raytheon	RC9310	
	TI	SN74160	
MC8311	AMD	9311	
	Fairchild	9311	
	Raytheon	RC9311	
	TI	SN74154	
MC8312	AMD	9312	
	Fairchild	9312	
	Raytheon	RC9312	
	Signetics	N8230	
	TI	SN29312	
MC8314	AMD	9314	
MC8316	AMD	9316	
	Fairchild	9316	
	Raytheon	RC9316	
	TI	SN74161	
MC8318	AMD	9318	
	TI	SN29318	
MC832	Hitachi	HD2201	
MC832	National	DM932	
	TI	SN15832	
MC8328	AMD	9328	
	Fairchild	9328	
	Signetics	N8277	
MC833	Hitachi	HD2202	
	National	DM933	
	TI	SN15833	
MC834	TI	SN15834	
MC835	TI	SN15838	
MC836	Hitachi	HD2206	
	National	DM936	
	TI	SN15836	
MC837	National	DM937	
	TI	SN15837	
MC840	National	DM935	
	TI	SN15835	
MC841	TI	SN15835	
MC844	Hitachi	HD2209	
	National	DM944	
MC845	Hitachi	HD2205	
	National	DM945	
	TI	SN15845	
MC846	Hitachi	HD2203	
	National	DM946	
	TI	SN15846	
MC848	National	DM948	
	TI	SN15848	
MC849	National	DM949	
	TI	SN15849	
MC850	TI	SN15850	
MC851	TI	SN15851	
MC852	National	DM9099	
	TI	SN158099	
MC853	National	DM9093	
	TI	SN158093	
MC855	National	DM9097	
	TI	SN158097	
MC856	National	DM9094	
	TI	SN158094	
MC857	Hitachi	HD2213	
	National	DM957	
	TI	SN15857	
MC858	Hitachi	HD2214	
	National	DM958	
	TI	SN15858	
MC8601	AMD	9601	
	Fairchild	9601	
	Raytheon	RF8601	
	Signetics	8T22	
	TI	SN29601	
MC8602	AMD	9602	
	Raytheon	RF8602	
MC861	National	DM961	
	TI	SN15861	
MC862	Hitachi	HD2207	
	National	DM962	
	TI	SN15862	
MC863	National	DM963	
	TI	SN15863	
MC930	Raytheon	RM930	
	TI	SN15930	
MC9300	AMD	9300	
	Raytheon	RM9300	
	TI	SN54195	
MC9301	AMD	9301	
	TI	SN39301	
MC9304	AMD	9304	
	Raytheon	RM9304	
MC9308	AMD	9308	
	Raytheon	RM9308	
	TI	SN39308	
MC931	TI	SN15931	
MC9310	AMD	9310	
	Raytheon	RM9310	
	TI	SN54160	
MC9311	AMD	9311	
	Raytheon	RM9311	
	TI	SN54154	
MC9312	AMD	9312	
	Raytheon	RM9312	
	Signetics	S8230	
	TI	SN39312	
MC9314	AMD	9314	
MC9316	AMD	9316	
	Raytheon	RM9316	
MC9316	TI	SN54161	
MC9318	AMD	9318	
	TI	SN39318	
MC932	Raytheon	RM932	
	TI	SN15939	
MC9328	AMD	9328	
	Signetics	N8277	
MC933	TI	SN15933	
MC934	TI	SN15934	
MC935	Raytheon	RM935	
	TI	SN15935	
MC936	Raytheon	RM936	
	TI	SN15936	
MC937	Raytheon	RM937	
	TI	SN15937	
MC940	Raytheon	RM940	
	TI	SN15935	
MC943	Fairchild	SH2001	
MC944	Raytheon	RM944	
	TI	SN15944	
MC945	Raytheon	RM945	
	TI	SN15945	
MC946	Raytheon	RM946	
	TI	SN15946	
MC948	Raytheon	RM948	
	TI	SN15948	
MC949	Raytheon	RM949	
	TI	SN15949	
MC950	Raytheon	RM950	
	TI	SN15950	
MC951	Raytheon	RM951	
	TI	SN15951	
MC952	Raytheon	RM952	
	TI	SN159099	
MC953	TI	SN159093	
MC955	TI	SN159097	
MC956	TI	SN159094	
MC957	Raytheon	RM957	
	TI	SN15957	
MC958	Raytheon	RM958	
	TI	SN15958	
MC9601	AMD	9601	
	Raytheon	RF9601	
	Signetics	S8T22	
	TI	SN29601	
MC9602	AMD	9602	
	Raytheon	RF9602	
MC961	Raytheon	RM961	
	TI	SN15961	
MC962	Raytheon	RM962	
	TI	SN15962	
MC963	Raytheon	RM963	
	TI	SN15963	
♦MFC4000	Motorola	MC3360	
♦MFC4010	Motorola	MC3310	
♦MFC6040	Motorola	MC3340	
♦MFC8030	Motorola	MC3330	
♦MFC8070	Motorola	MC3370	
MLM	Motorola	Now LM	
MMH0026	AMD	MMH0026	
	National	**DS0026**	**503**
	TI	SN75369	
MQ3724	RCA	CA3724	
MQ3725	RCA	CA3725	
NE592	AMD	NE592	
SE592	AMD	SE592	
SN54H54	ITT	ITT54H54	
	Signetics	10170	
SN54LS00	Fairchild	54LS00	
	National	DM54LS00	
	Raytheon	54LS00	
	Signetics	54LS00	
	TI	SN54LS00	
SN54LS02	Fairchild	54LS02	
	National	DM54LS02	
	Raytheon	54LS02	
	Signetics	54LS02	
	TI	SN54LS02	
SN54LS03	Fairchild	54LS03	
	National	DM54LS03	
	Raytheon	54LS03	
	Signetics	54LS03	
	TI	SN54LS03	
SN54LS04	Fairchild	54LS04	
	National	DM54LS04	
	Raytheon	54LS04	

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN54LS04	Signetics	54LS04	
	TI	SN54LS04	
SN54LS05	Fairchild	54LS05	
	National	DM54LS05	
	Raytheon	54LS05	
	Signetics	54LS05	
	TI	SN54LS05	
SN54LS08	Fairchild	54LS08	
	National	DM54LS08	
	Raytheon	54LS08	
	Signetics	54LS08	
	TI	SN54LS08	
SN54LS09	Fairchild	54LS09	
	National	DM54LS09	
	Raytheon	54LS09	
	Signetics	54LS09	
	TI	SN54LS09	
SN54LS10	Fairchild	54LS10	
	National	DM54LS10	
	Raytheon	54LS10	
	Signetics	54LS10	
	TI	SN54LS10	
SN54LS107	Fairchild	54LS107	
	National	DM54LS107	
	Raytheon	54LS107	
	Signetics	54LS107	
	TI	SN54LS107	
SN54LS109	Fairchild	54LS109	
	National	DM54LS109	
	Raytheon	**54LS109**	
	Signetics	54LS109	
	TI	SN54LS109	
SN54LS11	Fairchild	54LS11	
	National	DM54LS11	
	Raytheon	54LS11	
	Signetics	54LS11	
	TI	SN54LS11	
SN54LS114	Fairchild	54LS114	
	National	DM54LS114	
	Raytheon	54LS114	
	Signetics	54LS114	
	TI	SN54LS114A	
SN54LS126	Fairchild	54LS126	
	National	DM54LS126	
	Raytheon	54LS126	
	Signetics	54LS126	
	TI	SN54LS126A	
SN54LS13	National	DM54LS13	
	Raytheon	**54LS13**	**264**
	Signetics	54LS13	
	TI	SN54LS13	
SN54LS132	Fairchild	54LS132	
	National	DM54LS132	
	Raytheon	**54LS132**	**264**
	Signetics	54LS132	
	TI	SN54LS132	
SN54LS136	Fairchild	54LS136	
	Raytheon	54LS136	
	Signetics	54LS136	
	TI	SN54LS136	
SN54LS138	Fairchild	54LS138	
	National	DM54LS138	
	Raytheon	54LS138	
	Signetics	54LS138	
	TI	SN54LS138	
SN54LS139	AMD	SN54LS139	
	Fairchild	54LS139	
	National	DM54LS139	
	Raytheon	54LS139	
	Signetics	74LS139	
	TI	SN54LS139	
SN54LS14	Fairchild	54LS14	
	National	DM54LS14	
	Raytheon	**54LS14**	**264**
	Signetics	54LS14	
	TI	SN54LS14	
SN54LS15	Fairchild	54LS15	
	National	DM54LS15	
	Raytheon	54LS15	
	Signetics	54LS15	
	TI	SN54LS15	
SN54LS151	AMD	SN54LS151	
SN54LS151	Fairchild	54LS151	
	National	DM54LS151	
	Raytheon	54LS151	
	Signetics	54LS151	
	TI	SN54LS151	
SN54LS152	Fairchild	54LS152	
	Raytheon	54LS152	
	TI	SN54LS152	
SN54LS153	AMD	SN54LS153	
	Fairchild	54LS153	
	National	DM54LS153	
	Raytheon	54LS153	
	Signetics	54LS153	
	TI	SN54LS153	
SN54LS155	Fairchild	54LS155	
	National	DM54LS155	
	Raytheon	74LS155	
	TI	SN54LS155	
SN54LS156	Fairchild	54LS156	
	National	DM54LS156	
	Raytheon	54LS156	
	TI	SN54LS156	
SN54LS157	AMD	SN54LS157	
	Fairchild	54LS157	
	National	DM54LS157	
	Raytheon	54LS157	
	Signetics	54LS157	
	TI	SN54LS157	
SN54LS158	Fairchild	54LS158	
	National	DM54LS158	
	Raytheon	54LS158	
	Signetics	54LS158	
	TI	SN54LS158	
SN54LS160	AMD	SN54LS160	
	Fairchild	54LS160	
	National	DM54LS160	
	Raytheon	54LS160	
	TI	SN54LS160	
SN54LS161	AMD	SN54LS161	
	Fairchild	54LS161	
	National	DM54LS161	
	Raytheon	54LS161	
	Signetics	54LS161	
	TI	SN54LS161	
SN54LS162	AMD	SN54LS162	
	Fairchild	54LS162	
	National	DM54LS162	
	Raytheon	54LS162	
	TI	SN54LS162	
SN54LS163	AMD	SN54LS163	
	Fairchild	54LS163	
	National	DM54LS163	
	Raytheon	54LS163	
	Signetics	54LS163	
	TI	SN54LS163	
SN54LS164	AMD	SN54LS164	
	Fairchild	54LS164	
	National	DM54LS164	
	Raytheon	**54LS164**	**272**
	Signetics	54LS164	
	TI	SN54LS164	
SN54LS170	AMD	SN54LS170	
	Fairchild	54LS170	
	National	DM54LS170	
	Raytheon	54LS170	
	Signetics	54LS170	
	TI	SN54LS170	
SN54LS175	AMD	SN54LS175	
	Fairchild	54LS175	
	National	DM54LS175	
	Raytheon	54LS175	
	Signetics	54LS175	
	TI	SN54LS175	
SN54LS181	AMD	SN54LS181	
	Fairchild	54LS181	
	Raytheon	54LS181	
	Signetics	54LS181	
	TI	SN54LS181	
SN54LS190	AMD	SN54LS190	
	Fairchild	54LS190	
	National	DM54LS190	
	Raytheon	54LS190	
	Signetics	54LS190	
	TI	SN54LS190	
SN54LS191	AMD	SN54LS191	
	Fairchild	54LS191	
SN54LS191	National	DM54LS191	
	Raytheon	54LS191	
	Signetics	54LS191	
	TI	SN54LS191	
SN54LS192	AMD	SN54LS192	
	Fairchild	54LS192	
	National	DM54LS192	
	Raytheon	54LS192	
	Signetics	54LS192	
	TI	SN54LS192	
SN54LS193	AMD	SN54LS193	
	Fairchild	54LS193	
	National	DM54LS193	
	Raytheon	54LS193	
	Signetics	54LS193	
	TI	SN54LS193	
SN54LS194	AMD	SN54LS194A	
	Fairchild	54LS194	
	Raytheon	54LS194A	
	TI	SN54LS194A	
SN54LS195	AMD	SN54LS195A	
	Fairchild	54LS195	
	Raytheon	54LS195A	
	Signetics	54LS195A	
	TI	SN54LS195A	
SN54LS196	Fairchild	54LS196	
	National	DM54LS196	
	Raytheon	54LS196	
	TI	SN54LS196	
SN54LS197	Fairchild	54LS197	
	National	DM54LS197	
	Raytheon	54LS197	
	TI	SN54LS197	
SN54LS20	Fairchild	54LS20	
	National	DM54LS20	
	Raytheon	54LS20	
	Signetics	54LS20	
	TI	SN54LS20	
SN54LS21	Fairchild	54LS21	
	National	DM54LS21	
	Raytheon	54LS21	
	Signetics	54LS21	
	TI	SN54LS21	
SN54LS22	Fairchild	54LS22	
	National	DM54LS22	
	Raytheon	54LS22	
	Signetics	54LS22	
	TI	SN54LS22	
SN54LS251	AMD	SN54LS251	
	Fairchild	54LS251	
	Raytheon	54LS251	
	Signetics	54LS251	
	TI	SN54LS251	
SN54LS253	AMD	SN54LS253	
	Fairchild	54LS253	
	National	DM54LS253	
	Raytheon	54LS253	
	Signetics	54LS253	
	TI	SN54LS253	
SN54LS257	Fairchild	54LS257	
	National	DM54LS257	
	Raytheon	54LS257	
	Signetics	54LS257	
	TI	SN54LS257	
SN54LS258	AMD	SN54LS258	
	Fairchild	54LS258	
	Raytheon	54LS258	
	TI	SN54LS258	
SN54LS259	Fairchild	54LS259	
	TI	SN54LS259	
SN54LS266	Fairchild	54LS266	
	Raytheon	54LS266	
	Signetics	54LS266	
	TI	SN54LS266	
SN54LS27	Fairchild	54LS27	
	National	DM54LS27	
	Raytheon	54LS27	
	Signetics	54LS27	
	TI	SN54LS27	
SN54LS279	Fairchild	54LS279	
	National	DM54LS279	
	Raytheon	74LS279	
	Signetics	54LS279	
	TI	SN54LS279	
SN54LS283	Fairchild	54LS283	
	National	DM54LS283	
SN54LS283	Raytheon	54LS283	
	TI	SN54LS283	
SN54LS295	Fairchild	54LS295	
	Raytheon	54LS295A	
	TI	SN54LS295B	
SN54LS298	Fairchild	54LS298	
	Raytheon	54LS298	
	TI	SN54LS298	
SN54LS30	Fairchild	54LS30	
	National	DM54LS30	
	Raytheon	54LS30	
	Signetics	54LS30	
	TI	SN54LS30	
SN54LS32	Fairchild	54LS32	
	National	DM54LS32	
	Raytheon	54LS32	
	Signetics	54LS32	
	TI	SN54LS32	
SN54LS365	Fairchild	54LS365	
	Raytheon	**54LS365**	**286**
	Signetics	54LS365	
	TI	SN54LS365	
SN54LS366	Fairchild	54LS366	
	Raytheon	**54LS366**	**286**
	Signetics	54LS366	
	TI	SN54LS366	
SN54LS367	Fairchild	54LS367	
	Raytheon	**54LS367**	**286**
	Signetics	54LS367	
	TI	SN54LS367	
SN54LS368	Fairchild	54LS368	
	Raytheon	**54LS368**	**286**
	Signetics	54LS368	
	TI	SN54LS368	
SN54LS37	Fairchild	54LS37	
	National	DM54LS37	
	Raytheon	54LS37	
	Signetics	54LS37	
	TI	SN54LS37	
SN54LS38	Fairchild	54LS38	
	National	DM54LS38	
	Raytheon	54LS38	
	Signetics	54LS38	
	TI	SN54LS38	
SN54LS40	Fairchild	54LS40	
	National	DM54LS40	
	Raytheon	54LS40	
	Signetics	54LS40	
	TI	SN54LS40	
SN54LS42	Fairchild	54LS42	
	National	DM54LS42	
	Raytheon	**54LS42**	**266**
	Signetics	54LS42	
	TI	SN54LS42	
SN54LS51	Fairchild	54LS51	
	National	DM54LS51	
	Raytheon	54LS51	
	Signetics	54LS51	
	TI	SN54LS51	
SN54LS54	Fairchild	54LS54	
	National	DM54LS54	
	Raytheon	54LS54	
	Signetics	54LS54	
	TI	SN54LS54	
SN54LS55	Fairchild	54LS55	
	National	DM54LS55	
	Raytheon	54LS55	
	Signetics	54LS55	
	TI	SN54LS55	
SN54LS670	AMD	SN54LS670	
	Fairchild	54LS670	
	National	DM54LS670	
	Raytheon	54LS670	
	Signetics	54LS670	
	TI	SN54LS670	
SN54LS73	Fairchild	54LS73	
	National	DM54LS73	
	Raytheon	54LS73	
	Signetics	54LS73	
	TI	SN54LS73	
SN54LS74	Fairchild	54LS74	
	National	DM54LS74	
	Raytheon	54LS74	
	Signetics	54LS74	
	TI	SN54LS74	
SN54LS83	Fairchild	54LS83	

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The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN54LS83	National	DM54LS83	
	Raytheon	54LS83A	
	TI	SN54LS83A	
SN54LS86	Fairchild	54LS86	
	Raytheon	54LS86	
	Signetics	54LS86	
	TI	SN54LS86	
SN54LS90	Fairchild	54LS90	
	Raytheon	**54LS90**	**268**
	Signetics	54LS90	
	TI	SN54LS90	
SN54LS92	**Raytheon**	**54LS92**	**268**
	Signetics	54LS92	
	TI	SN54LS92	
SN54LS93	Fairchild	54LS93	
	Raytheon	**54LS93**	**268**
	Signetics	54LS93	
	TI	SN54LS93	
SN54LS95B	Fairchild	54LS95B	
	Raytheon	54LS95B	
	TI	SN54LS95B	
SN54S112	Fairchild	54S112	
	TI	SN54S112	
SN54S113	Fairchild	54S113	
	TI	SN54S113	
SN74LS00	Fairchild	74LS00	
	ITT	ITT74LS00	
	National	DM74LS00	
	NEC America	μPB74LS00	
	Raytheon	74LS00	
	Signetics	74LS00	
	TI	SN74LS00	
SN74LS02	Fairchild	74LS02	
	ITT	ITT74LS02	
	National	DM74LS02	
	NEC America	μPB74LS02	
	Raytheon	74LS02	
	Signetics	74LS02	
	TI	SN74LS02	
SN74LS03	Fairchild	74LS03	
	ITT	ITT74LS03	
	National	DM74LS03	
	NEC America	μPB74LS03	
	Raytheon	74LS03	
	Signetics	74LS03	
	TI	SN74LS03	
SN74LS04	Fairchild	74LS04	
	ITT	ITT74LS04	
	National	DM74LS04	
	NEC America	μPB74LS04	
	Raytheon	74LS04	
	Signetics	74LS04	
	TI	SN74LS04	
SN74LS05	Fairchild	74LS05	
	ITT	ITT74LS05	
	National	DM74LS05	
	NEC America	μPB74LS05	
	Raytheon	74LS05	
	Signetics	74LS05	
	TI	SN74LS05	
SN74LS08	Fairchild	74LS08	
	ITT	ITT74LS08	
	National	DM74LS08	
	NEC America	μPB74LS08	
	Raytheon	74LS08	
	Signetics	74LS08	
	TI	SN74LS08	
SN74LS09	Fairchild	74LS09	
	ITT	ITT74LS09	
	National	DM74LS09	
	Raytheon	74LS09	
	Signetics	74LS09	
	TI	SN74LS09	
SN74LS10	Fairchild	74LS10	
	ITT	ITT74LS10	
	National	DM74LS10	
	NEC America	μPB74LS10	
	Raytheon	74LS10	
	Signetics	74LS10	
	TI	SN74LS10	
SN74LS109	Fairchild	74LS109	
	ITT	ITT74LS109A	
SN74LS109	National	DM74LS109	
	NEC America	μPB74LS109	
	Raytheon	74LS109	
	Signetics	74LS109	
	TI	SN74LS109	
SN74LS11	Fairchild	74LS11	
	ITT	ITT74LS11	
	National	DM74LS11	
	NEC America	μPB74LS11	
	Raytheon	74LS11	
	Signetics	74LS11	
	TI	SN74LS11	
SN74LS114	Fairchild	74LS114	
	ITT	ITT74LS114	
	National	DM74LS114	
	Raytheon	74LS114	
	Signetics	74LS114	
	TI	SN74LS114	
SN74LS126	Fairchild	74LS126	
	ITT	ITT74LS126	
	National	DM74LS126	
	Raytheon	74LS126	
	Signetics	74LS126	
	TI	SN74LS126A	
SN74LS13	Fairchild	74LS13	
	ITT	ITT74LS13	
	National	DM74LS13	
	Raytheon	**74LS13**	**264**
	Signetics	74LS13	
	TI	SN74LS13	
SN74LS132	Fairchild	74LS132	
	ITT	ITT74LS132	
	National	DM74LS132	
	Raytheon	**74LS132**	**264**
	Signetics	74LS132	
	TI	SN74LS132	
SN74LS136	Fairchild	74LS136	
	ITT	ITT74LS136	
	National	DM74LS136	
	Raytheon	74LS136	
	Signetics	74LS136	
	TI	SN74LS136	
SN74LS138	AMD	SN74LS138	
	Fairchild	74LS138	
	ITT	ITT74LS138	
	National	DM74LS138	
	NEC America	μPB74LS138	
	Raytheon	74LS138	
	Signetics	74LS138	
	TI	SN74LS138	
SN74LS139	AMD	SN74LS139	
	Fairchild	74LS139	
	ITT	ITT74LS139	
	National	DM74LS139	
	NEC America	μPB74LS139	
	Raytheon	74LS139	
	Signetics	74LS139	
	TI	SN74LS139	
SN74LS14	Fairchild	74LS14	
	ITT	ITT74LS14	
	National	DM74LS14	
	Raytheon	**74LS14**	**264**
	Signetics	74LS14	
	TI	SN74LS14	
SN74LS15	Fairchild	74LS15	
	ITT	ITT74LS15	
	National	DM74LS15	
	Raytheon	74LS15	
	Signetics	74LS15	
	TI	SN74LS15	
SN74LS151	AMD	SN74LS151	
	Fairchild	74LS151	
	ITT	ITT74LS151	
	National	DM74LS151	
	NEC America	μPB74LS151	
	Raytheon	74LS151	
	Signetics	74LS151	
	TI	SN74LS151	
SN74LS152	Fairchild	74LS152	
	Raytheon	74LS152	
SN74LS153	AMD	SN74LS153	
	Fairchild	74LS153	
	ITT	ITT74LS153	
	National	DM74LS153	
	NEC America	μPB74LS153	
	Raytheon	74LS153	
SN74LS153	Signetics	74LS153	
	TI	SN74LS153	
SN74LS155	Fairchild	74LS155	
	ITT	ITT74LS155	
	National	DM74LS155	
	NEC America	μPB74LS155	
	Raytheon	74LS155	
	Signetics	74LS155	
	TI	SN74LS155	
SN74LS156	Fairchild	74LS156	
	ITT	ITT74LS156	
	National	DM74LS156	
	Raytheon	74LS156	
	Signetics	74LS156	
	TI	SN74LS156	
SN74LS157	AMD	SN74LS157	
	Fairchild	74LS157	
	ITT	ITT74LS157	
	National	DM74LS157	
	NEC America	μPB74LS157	
	Raytheon	74LS157	
	Signetics	74LS157	
	TI	SN74LS157	
SN74LS158	AMD	SN74LS158	
	Fairchild	74LS158	
	ITT	ITT74LS158	
	National	DM74LS158	
	Raytheon	74LS158	
	Signetics	74LS158	
	TI	SN74LS158	
SN74LS160	AMD	SN74LS160	
	Fairchild	74LS160	
	ITT	ITT74LS160	
	National	DM74LS160	
	Raytheon	74LS160	
	Signetics	74LS160	
	TI	SN74LS160	
SN74LS161	AMD	SN74LS161	
	Fairchild	74LS161	
	ITT	ITT74LS161	
	National	DM74LS161	
	NEC America	μPB74LS161	
	Raytheon	74LS161	
	Signetics	74LS161	
	TI	SN74LS161	
SN74LS162	AMD	SN74LS162	
	Fairchild	74LS162	
	ITT	ITT74LS162	
	National	DM74LS162	
	Raytheon	74LS162	
	Signetics	74LS162	
	TI	SN74LS162	
SN74LS163	AMD	SN74LS163	
	Fairchild	74LS163	
	ITT	ITT74LS163	
	National	DM74LS163	
	Raytheon	74LS163	
	Signetics	74LS163	
	TI	SN74LS163	
SN74LS164	AMD	SN74LS164	
	Fairchild	74LS164	
	ITT	ITT74LS164	
	National	DM74LS164	
	NEC America	μPB74LS164	
	Raytheon	**74LS164**	**272**
	Signetics	74LS164	
	TI	SN74LS164	
SN74LS170	AMD	SN74LS170	
	Fairchild	74LS170	
	ITT	ITT74LS170	
	National	DM74LS170	
	Raytheon	74LS170	
	Signetics	74LS170	
	TI	SN74LS170	
SN74LS174	AMD	SN74LS174	
	Fairchild	74LS174	
	ITT	ITT74LS174	
	National	DM74LS174	
	Raytheon	74LS174	
	Signetics	74LS174	
	TI	SN74LS174	
SN74LS175	AMD	SN74LS175	
	Fairchild	74LS175	
	ITT	ITT74LS175	
	National	DM74LS175	
	NEC America	μPB74LS175	
SN74LS175	Raytheon	74LS175	
	Signetics	74LS175	
	TI	SN74LS175	
SN74LS181	AMD	SN74LS181	
	Fairchild	74LS181	
	Raytheon	74LS181	
	Signetics	74LS181	
	TI	SN74LS181	
SN74LS190	AMD	SN74LS190	
	Fairchild	74LS190	
	ITT	ITT74LS190	
	National	DM74LS190	
	Raytheon	74LS190	
	Signetics	74LS190	
	TI	SN74LS190	
SN74LS191	AMD	SN74LS191	
	Fairchild	74LS191	
	ITT	ITT74LS191	
	National	DM74LS191	
	Raytheon	74LS191	
	Signetics	74LS191	
	TI	SN74LS191	
SN74LS192	AMD	SN74LS192	
	Fairchild	74LS192	
	ITT	ITT74LS192	
	National	DM74LS192	
	NEC America	μPB74LS192	
	Raytheon	74LS192	
	Signetics	74LS192	
	TI	SN74LS192	
SN74LS193	AMD	SN74LS193	
	Fairchild	74LS193	
	ITT	ITT74LS193	
	National	DM74LS193	
	NEC America	μPB74LS193	
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	TI	SN74LS193	
SN74LS194	AMD	SN74LS194A	
	Fairchild	74LS194	
	ITT	ITT74LS194A	
	NEC America	μPB74LS194	
	Raytheon	74LS194A	
	Signetics	74LS194A	
	TI	SN74LS194A	
SN74LS195	AMD	SN74LS195A	
	Fairchild	74LS195	
	ITT	ITT74LS195A	
	NEC America	μPB74LS195	
	Raytheon	74LS195A	
	Signetics	74LS195A	
	TI	SN74LS195A	
SN74LS196	Fairchild	74LS196	
	ITT	ITT74LS196	
	National	DM74LS196	
	Raytheon	74LS196	
	Signetics	74LS196	
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SN74LS197	Fairchild	74LS197	
	ITT	ITT74LS197	
	National	DM74LS197	
	Raytheon	74LS197	
	Signetics	74LS197	
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SN74LS20	Fairchild	74LS20	
	ITT	ITT74LS20	
	National	DM74LS20	
	NEC America	μPB74LS20	
	Raytheon	74LS20	
	Signetics	74LS20	
	TI	SN74LS20	
SN74LS21	Fairchild	74LS21	
	ITT	ITT74LS21	
	National	DM74LS21	
	NEC America	μPB74LS21	
	Raytheon	74LS21	
	Signetics	74LS21	
	TI	SN74LS21	
SN74LS22	Fairchild	74LS22	
	ITT	ITT74LS22	
	National	DM74LS22	
	Raytheon	74LS22	
	Signetics	74LS22	
	TI	SN74LS22	
SN74LS221	Fairchild	74LS221	
	ITT	ITT74LS221	

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Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN74LS221	National	DM74LS221	
	Raytheon	**74LS221**	**275**
	Signetics	74LS221	
	TI	SN74LS221	
SN74LS240	AMD	SN74LS240	
	Fairchild	74LS240	
	ITT	ITT74LS240	
	MMI	74LS240	
	Raytheon	**74LS240**	**279**
	Signetics	74LS240	
	TI	SN74LS240	
SN74LS241	AMD	SN74LS241	
	Fairchiid	74LS241	
	ITT	ITT74LS241	
	MMI	74LS241	
	Raytheon	**74LS241**	**279**
	Signetics	74LS241	
	TI	SN74LS241	
SN74LS242	AMD	SN74LS242	
	Fairchild	74LS242	
	ITT	ITT74LS242	
	Raytheon	**74LS242**	**282**
	Signetics	74LS242	
	TI	SN74LS242	
SN74LS243	AMD	SN74LS243	
	Fairchild	74LS243	
	ITT	ITT74LS243	
	Raytheon	**74LS243**	**282**
	Signetics	74LS243	
	TI	SN74LS243	
SN74LS244	AMD	SN74LS244	
	Fairchild	74LS244	
	ITT	ITT74LS244	
	MMI	74LS244	
	Raytheon	**74LS244**	**279**
	Signetics	74LS244	
	TI	SN74LS244	
SN74LS251	AMD	SN74LS251	
	Fairchild	74LS251	
	ITT	ITT74LS251	
	National	DM74LS251	
	NEC America	μPB74LS251	
	Raytheon	74LS251	
	Signetics	74LS251	
	TI	SN74LS251	
SN74LS253	AMD	SN74LS253	
	Fairchild	74LS253	
	ITT	ITT74LS253	
	National	DM74LS253	
	NEC America	μPB74LS253	
	Raytheon	74LS253	
	Signetics	74LS253	
	TI	SN74LS253	
SN74LS257	AMD	SN74LS257	
	Fairchild	74LS257	
	ITT	ITT74LS257	
	National	DM74LS257	
	NEC America	μPB74LS257	
	Raytheon	74LS257	
	Signetics	74LS257	
	TI	SN74LS257	
SN74LS258	AMD	SN74LS258	
	Fairchild	74LS258	
	ITT	ITT74LS258	
	National	DM74LS258	
	NEC America	μPB74LS258	
	Raytheon	74LS258	
	Signetics	74LS258	
	TI	SN74LS258	
SN74LS259	Fairchild	74LS259	
	ITT	ITT74LS259	
	TI	SN74LS259	
SN74LS266	Fairchild	74LS266	
	ITT	ITT74LS266	
	Raytheon	74LS266	
	Signetics	74LS266	
	TI	SN74LS266	
SN74LS27	Fairchild	74LS27	
	ITT	ITT74LS27	
	National	DM74LS27	
	NEC America	μPB74LS27	
	Raytheon	74LS27	
SN74LS27	Signetics	74LS27	
	TI	SN74LS27	
SN74LS279	Fairchild	74LS279	
	ITT	ITT74LS279	
	National	DM74LS279	
	NEC America	μPB74LS279	
	Raytheon	74LS279	
	Signetics	74LS279	
	TI	SN74LS279	
SN74LS283	Fairchild	74LS283	
	ITT	ITT74LS283	
	National	DM74LS283	
	Raytheon	74LS283	
	Signetics	74LS283	
	TI	SN74LS283	
SN74LS290	Fairchild	74LS290	
	ITT	ITT74LS290	
	National	DM74LS290	
	Signetics	74LS290	
	TI	SN74LS290	
SN74LS293	Fairchild	74LS293	
	ITT	ITT74LS293	
	National	DM74LS293	
	Signetics	74LS293	
	TI	SN74LS293	
SN74LS295	Fairchild	74LS295	
	NEC America	μPB74LS295	
	Raytheon	74LS295A	
	Signetics	74LS295	
	TI	SN74LS295B	
SN74LS298	Fairchild	74LS298	
	Raytheon	74LS298	
	Signetics	74LS298	
	TI	SN74LS298	
SN74LS30	Fairchild	74LS30	
	ITT	ITT74LS30	
	National	DM74LS30	
	NEC America	μPB74LS30	
	Raytheon	74LS30	
	Signetics	74LS30	
	TI	SN74LS30	
SN74LS32	Fairchild	74LS32	
	ITT	ITT74LS32	
	National	DM74LS32	
	NEC America	μPB74LS32	
	Raytheon	74LS32	
	Signetics	74LS32	
	TI	SN74LS32	
SN74LS365	Fairchild	74LS365	
	ITT	ITT74LS365	
	National	DM74LS365	
	NEC America	μPB74LS365	
	Raytheon	**74LS365**	**286**
	Signetics	74LS365	
	TI	SN74LS365	
SN74LS366	Fairchild	74LS366	
	ITT	ITT74LS366	
	National	DM74LS366	
	NEC America	μPB74LS366	
	Raytheon	**74LS366**	**286**
	Signetics	74LS366	
	TI	SN74LS366	
SN74LS367	Fairchild	74LS367	
	ITT	ITT74LS367	
	National	DM74LS367	
	NEC America	μPB74LS367	
	Raytheon	**74LS367**	**286**
	Signetics	74LS367	
	TI	SN74LS367	
SN74LS368	Fairchild	74LS368	
	ITT	ITT74LS368	
	National	DM74LS368	
	NEC America	μPB74LS368	
	Raytheon	**74LS368**	**286**
	Signetics	74LS368	
	TI	SN74LS368	
SN74LS37	Fairchild	74LS37	
	ITT	ITT74LS37	
	National	DM74LS37	
	NEC America	μPB74LS37	
	Raytheon	74LS37	
	Signetics	74LS37	
	TI	SN74LS37	
SN74LS375	ITT	ITT74LS375	
	NEC America	μPB74LS375	
	Raytheon	74LS375	
SN74LS375	Signetics	74LS375	
	TI	SN74LS375	
SN74LS38	Fairchild	74LS38	
	ITT	ITT74LS38	
	National	DM74LS38	
	NEC America	μPB74LS38	
	Raytheon	74LS38	
	Signetics	74LS38	
	TI	SN74LS38	
SN74LS386	Fairchild	74LS386	
	ITT	ITT74LS386	
	National	DM74LS386	
	Raytheon	74LS386	
	Signetics	74LS386	
	TI	SN74LS386	
SN74LS40	Fairchild	74LS40	
	ITT	ITT74LS40	
	National	DM74LS40	
	NEC America	μPB74LS40	
	Raytheon	74LS40	
	Signetics	74LS40	
	TI	SN74LS40	
SN74LS42	Fairchild	74LS42	
	ITT	ITT74LS42	
	National	DM74LS42	
	NEC America	μPB74LS42	
	Raytheon	**74LS42**	**266**
	Signetics	74LS42	
	TI	SN74LS42	
SN74LS51	Fairchild	74LS51	
	ITT	ITT74LS51	
	National	DM74LS51	
	NEC America	μPB74LS51	
	Raytheon	74LS51	
	Signetics	74LS51	
	TI	SN74LS51	
SN74LS54	Fairchild	74LS54	
	ITT	ITT74LS54	
	National	DM74LS54	
	NEC America	μPB74LS54	
	Raytheon	74LS54	
	Signetics	74LS54	
	TI	SN74LS54	
SN74LS55	Fairchild	74LS55	
	National	DM74LS55	
	NEC America	μPB74LS55	
	Raytheon	74LS55	
	Signetics	74LS55	
	TI	SN74LS55	
SN74LS670	AMD	SN74LS670	
	Fairchild	74LS670	
	National	DM74LS670	
	Raytheon	74LS670	
	Signetics	74LS670	
	TI	SN74LS670	
SN74LS73	Fairchild	74LS73	
	ITT	ITT74LS73	
	National	DM74LS73	
	Raytheon	74LS73	
	Signetics	74LS73	
	TI	SN74LS73	
SN74LS74	Fairchild	74LS74	
	ITT	ITT74LS74	
	National	DM74LS74	
	NEC America	μPB74LS74	
	Raytheon	74LS74	
	Signetics	74LS74	
	TI	SN74LS74	
SN74LS83	Fairchild	74LS83	
	ITT	ITT74LS83A	
	National	DM74LS83	
		DM74LS83A	
	Raytheon	74LS83A	
	Signetics	74LS83	
	TI	SN74LS83A	
SN74LS85	Fairchild	74LS85	
	ITT	ITT74LS85	
	National	DM74LS85	
	Raytheon	74LS85	
	Signetics	74LS85	
	TI	SN74LS85	
SN74LS86	Fairchild	74LS86	
	ITT	ITT74LS86	
	NEC America	μPB74LS86	
	Raytheon	74LS86	
	Signetics	74LS86	
SN74LS86	TI	SN74LS86	
SN74LS90	Fairchild	74LS90	
	ITT	ITT74LS90	
	Raytheon	**74LS90**	**268**
	Signetics	74LS90	
	TI	SN74LS90	
SN74LS92	Fairchild	74LS92	
	Raytheon	**74LS92**	**268**
	Signetics	74LS92	
	TI	SN74LS92	
SN74LS93	Fairchild	74LS93	
	ITT	ITT74LS93	
	Raytheon	**74LS93**	**268**
	Signetics	74LS93	
	TI	SN74LS93	
SN74LS95	Fairchild	74LS95	
	ITT	ITT74LS95B	
	Raytheon	74LS95B	
	Signetics	74LS95B	
	TI	SN74LS95B	
SN74S112	Fairchild	74S112	
	Hitachi	HD74S112	
	Mitsubishi	M5S112	
	National	DM74S112	
	Signetics	74S112	
	TI	SN74S112	
SN74S113	Fairchild	74S113	
	Hitachi	HD74S113	
	Mitsubishi	M5S113	
	National	DM74S113	
	Signetics	74S113	
	TI	SN74S113	
ULN2001	Exar	XR2201	
ULN2002	Exar	XR2202	
ULN2003	Exar	XR2203	
ULN2004	Exar	XR2204	

National Semiconductor

Manufacturer Device	Replacement Source	Device
AH0126	Siliconix	DG126
AH0129	Siliconix	DG129
AH0133	Siliconix	DG133
AH0134	Siliconix	DG134
AH0139	Siliconix	DG139
AH0140	Siliconix	DG140
AH0141	Siliconix	DG141
AH0142	Siliconix	DG142
AH0143	Siliconix	DG143
AH0144	Siliconix	DG144
AH0145	Siliconix	DG145
AH0146	Siliconix	DG146
AH0151	Siliconix	DG151
AH0152	Siliconix	DG152
AH0153	Siliconix	DG153
AH0154	Siliconix	DG154
AH0161	Siliconix	DG161
AH0162	Siliconix	DG162
AH0163	Siliconix	DG163
AH0164	Siliconix	DG164
CD4000	Mitel	SIL4000
	Motorola	MC14000
	RCA	CD4000
	Solitron	CM4000
	SSS	SCL4000
	TI	TP4000
CD4001	Fairchild	F4001
	Mitel	SIL4001
		SIL4901
	Motorola	MC14001
	NEC America	μPD4001
	RCA	CD4001
	SGS	HBF4001
	Solitron	CM4001
	SSS	SCL4001
	TI	TP4001
	Toshiba	TC4001
CD4002	Fairchild	F4002
	Mitel	SIL4002
	Motorola	MC14002
	NEC America	μPD4002
	RCA	CD4002
	SGS	HBF4002
	Solitron	CM4002
	SSS	SCL4002
	TI	TP4002

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

National Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
CD4002	Toshiba	TC4002	
CD4006	Fairchild	F4006	
	Motorola	MC14006	
	NEC America	µPD4006	
	RCA	CD4006	
	Solitron	CM4006	
	SSS	SCL4006	
CD4007	Fairchild	F4007	
	Mitel	SIL4007	
	Motorola	MC14007	
	RCA	CD4007	
	SGS	HBF4007	
	Solitron	CM4007	
	SSS	SCL4007	
	TI	TP4007	
	Toshiba	TC4007	
CD4008	Fairchild	F4008	
	Motorola	MC14008	
	RCA	CD4008	
	SGS	HBF4008	
	Solitron	CM4008	
	SSS	SCL4008	
	TI	TP4008	
	Toshiba	TC4008	
CD4009	Mitel	SIL4009	
	RCA	CD4009	
	SGS	HBF4009	
	Solitron	CM4009	
	SSS	SCL4009	
	TI	TP4009	
	Toshiba	TC4009	
CD4010	Mitel	SIL4010	
	RCA	CD4010	
	SGS	HBF4010	
	Solitron	CM4010	
	SSS	SCL4010	
	TI	TP4010	
	Toshiba	TC4010	
CD40106	Motorola	MC14584	
	National	MM74C14	
	RCA	CD40106	
CD4011	Fairchild	F4011	
	Mitel	SIL4011	
		SIL4911	
	Motorola	MC14011	
	NEC America	µPD4011	
	RCA	CD4011	
	SGS	HBF4011	
	Solitron	CM4011	
	SSS	SCL4011	
	TI	TP4011	
	Toshiba	TC4011	
CD4012	Fairchild	F4012	
	Mitel	SIL4012	
		SIL4912	
	Motorola	MC14012	
	NEC America	µPD4012	
	RCA	CD4012	
	SGS	HBF4012	
	Solitron	CM4012	
	SSS	SCL4012	
	TI	TP4012	
	Toshiba	TC4012	
CD4013	Fairchild	F4013	
	Mitel	SIL4013	
	Motorola	MC14013	
	NEC America	µPD4013	
	RCA	CD4013	
	SGS	HBF4013	
	Solitron	CM4013	
	SSS	SCL4013	
	TI	TP4013	
	Toshiba	TC4013	
CD4014	Fairchild	F4014	
	Mitel	SIL4014	
	Motorola	MC14014	
	NEC America	µPD4014	
	RCA	CD4014	
	SGS	HBF4014	
	Solitron	CM4014	
	SSS	SCL4014	
	TI	TP4014	
CD4014	Toshiba	TC4014	
CD4015	Fairchild	F4015	
	Mitel	SIL4015	
	Motorola	MC14015	
	NEC America	µPD4015	
	RCA	CD4015	
	SGS	HBF4015	
	Solitron	CM4015	
	SSS	SCL4015	
	TI	TP4015	
	Toshiba	TC4015	
CD4016	AD	AD7516	
	Fairchild	F4016	
	Micro Power	MPS7516	
	Mitel	SIL4016	
	Motorola	MC14016	
	RCA	CD4016	
	Solitron	CM4016	
	SSS	SCL4016	
	TI	TP4016	
CD40160	Fairchild	F40160	
	RCA	CD40160	
CD40161	Fairchild	F40161	
	RCA	CD40161	
CD40162	Fairchild	F40162	
	RCA	CD40162	
CD40163	Fairchild	F40163	
	RCA	CD40163	
CD4017	Fairchild	F4017	
	Mitel	SIL4017	
	Motorola	MC14017	
	NEC America	µPD4017	
	RCA	CD4017	
	SGS	HBF4017	
	Solitron	CM4017	
	SSS	SCL4017	
	TI	TP4017	
	Toshiba	TC4017	
CD40174	Fairchild	F40174	
	RCA	CD40174	
CD4018	Fairchild	F4018	
	Mitel	SIL4018	
	RCA	CD4018	
	SGS	HBF4018	
	Solitron	CM4018	
	SSS	SCL4018	
	TI	TP4018	
	Toshiba	TC4018	
CD4019	Fairchild	F4019	
	Mitel	SIL4019	
	NEC America	µPD4019	
	RCA	CD4019	
	SGS	HBF4019	
	Solitron	CM4019	
	SSS	SCL4019	
	TI	TP4019	
	Toshiba	TC4019	
CD40192	Fairchild	F40192	
	National	MM74C192	
	RCA	CD40192	
CD40193	Fairchild	F40193	
	National	MM74C193	
	RCA	CD40193	
CD4020	Fairchild	F4020	
	Mitel	SIL4020	
	Motorola	MC14020	
	NEC America	µPD4020	
	RCA	CD4020	
	SGS	HBF4020	
	Solitron	CM4020	
	SSS	SCL4020	
	TI	TP4020	
	Toshiba	TC4020	
CD4021	Fairchild	F4021	
	Mitel	SIL4021	
	Motorola	MC14021	
	NEC America	µPD4021	
	RCA	CD4021	
	Solitron	CM4021	
	SSS	SCL4021	
	TI	TP4021	
	Toshiba	TC4021	
CD4022	Fairchild	F4022	
	Mitel	SIL4022	
	Motorola	MC14022	
	RCA	CD4022	
CD4022	SGS	HBF4022	
	Solitron	CM4022	
	SSS	SCL4022	
	TI	TP4022	
	Toshiba	TC4022	
CD4023	Fairchild	F4023	
	Mitel	SIL4023	
		SIL4923	
	Motorola	MC14023	
	NEC America	µPD4023	
	RCA	CD4023	
	SGS	HBF4023	
	Solitron	CM4023	
	SSS	SCL4023	
	TI	TP4023	
	Toshiba	TC4023	
CD4024	Fairchild	F4024	
	Mitel	SIL4024	
	Motorola	MC14024	
	NEC America	µPD4024	
	RCA	CD4024	
	SGS	HBF4024	
	Solitron	CM4024	
	SSS	SCL4024	
	TI	TP4024	
	Toshiba	TC4024	
CD4025	Fairchild	F4025	
	Mitel	SIL4025	
		SIL4925	
	Motorola	MC14025	
	NEC America	µPD4025	
	RCA	CD4025	
	SGS	HBF4025	
	Solitron	CM4025	
	SSS	SCL4025	
	TI	TP4025	
	Toshiba	TC4025	
CD4027	Fairchild	F4027	
	Mitel	SIL4027	
	Motorola	MC14027	
	NEC America	µPD4027	
	RCA	CD4027	
	SGS	HBF4027	
	Solitron	CM4027	
	SSS	SCL4027	
	TI	TP4027	
	Toshiba	TC4027	
CD4028	Fairchild	F4028	
	Mitel	SIL4028	
	Motorola	MC14028	
	NEC America	µPD4028	
	RCA	CD4028	
	SGS	HBF4028	
	Solitron	CM4028	
	SSS	SCL4028	
	TI	TP4028	
	Toshiba	TC4028	
CD4029	Fairchild	F4029	
	Mitel	SIL4029	
	NEC America	µPD4029	
	RCA	CD4029	
	SGS	HBF4029	
	Solitron	CM4029	
	SSS	SCL4029	
	TI	TP4029	
	Toshiba	TC4029	
CD4030	Fairchild	F4030	
	Mitel	SIL4030	
	NEC America	µPD4030	
	RCA	CD4030	
	SGS	HBF4030	
	Solitron	CM4030	
	SSS	SCL4030	
	TI	TP4030	
	Toshiba	TC4030	
CD4031	Fairchild	F4031	
	RCA	CD4031	
CD4034	Fairchild	F4034	
	Motorola	MC14034	
	NEC America	µPD4034	
	RCA	CD4034	
	Solitron	CM4034	
	SSS	SCL4034	
	Toshiba	TC4034	
CD4035	Fairchild	F4035	
	Mitel	SIL4035	
CD4035	Motorola	MC14035	
	NEC America	µPD4035	
	RCA	CD4035	
	SGS	HBF4035	
	Solitron	CM4035	
	SSS	SCL4035	
	TI	TP4035	
	Toshiba	TC4035	
CD4040	Fairchild	F4040	
	Mitel	SIL4040	
	NEC America	µPD4040	
	RCA	CD4040	
	Solitron	CM4040	
	SSS	SCL4040	
	TI	TP4040	
	Toshiba	TC4040	
CD4041	Fairchild	F4041	
	RCA	CD4041	
	Solitron	CM4041	
	SSS	CL4041	
		SCL4041	
CD4042	Fairchild	F4042	
	Mitel	SIL4042	
	Motorola	MC14042	
	NEC America	µPD4042	
	RCA	CD4042	
	SGS	HBF4042	
	Solitron	CM4042	
	SSS	SCL4042	
	TI	TP4042	
	Toshiba	TC4042	
CD4043	Fairchild	F4043	
	Mitel	SIL4043	
	Motorola	MC14043	
	NEC America	µPD4043	
	RCA	CD4043	
	Solitron	CM4043	
	SSS	SCL4043	
	TI	TP4043	
	Toshiba	TC4043	
CD4044	Fairchild	F4044	
	Mitel	SIL4044	
	Motorola	MC14044	
	NEC America	µPD4044	
	RCA	CD4044	
	Solitron	CM4044	
	SSS	SCL4044	
	TI	TP4044	
	Toshiba	TC4044	
CD4046	Fairchild	F4046	
	Mitel	SIL4046	
	Motorola	MC14046	
	RCA	CD4046	
	Solitron	CM4046	
	SSS	SCL4046	
CD4048	RCA	CD4048	
CD4049	Fairchild	F4049	
	Mitel	SIL4049	
	Motorola	MC14049	
	NEC America	µPD4049	
	RCA	CD4049	
	SGS	HBF4049	
	Solitron	CM4049	
	SSS	SCL4049	
	TI	TP4049	
	Toshiba	TC4049	
CD4050	Fairchild	F4050	
	Mitel	SIL4050	
	Motorola	MC14050	
	NEC America	µPD4050	
	RCA	CD4050	
	SGS	HBF4050	
	Solitron	CM4050	
	SSS	SCL4050	
	TI	TP4050	
	Toshiba	TC4050	
CD4051	Fairchild	F4051	
	Mitel	SIL4051	
	Motorola	MC14051	
	NEC America	µPD4051	
	RCA	CD4051	
	Solitron	CM4051	
	SSS	SCL4051	
	TI	TP4051	
	Toshiba	TC4051	
CD4052	Fairchild	F4052	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

National Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
CD4052	Mitel	SIL4052	
	Motorola	MC14052	
	NEC America	µPD4052	
	RCA	CD4052	
	Solitron	CM4052	
	SSS	SCL4052	
	TI	TP4052	
	Toshiba	TC4052	
CD4053	Fairchild	F4053	
	Mitel	SIL4053	
	Motorola	MC14053	
	NEC America	µPD4053	
	RCA	CD4053	
	Solitron	CM4053	
	SSS	SCL4053	
	Toshiba	TC4053	
CD4060	Mitel	SIL4060	
	RCA	CD4060	
	SSS	SCL4060	
CD4066	Fairchild	F4066	
	Mitel	SIL4066	
	Motorola	MC14066	
	NEC America	µPD4066	
	RCA	CD4066	
	SGS	HBF4066	
	Signetics	N4066	
	Solitron	CM4066	
	SSS	SCL4066	
	Toshiba	TC4066	
CD4069	Fairchild	F4069	
	Harris	HD74C04	
	Mitel	SIL4069	
	Motorola	MC14069	
	National	MM74C04	
	NEC America	µPD4069	
	RCA	CD4069	
	Solitron	CM4069	
	SSS	SCL4069	
	TI	TP4069	
	Toshiba	TC4069	
CD4070	Fairchild	F4070	
	Mitel	SIL4070	
	Motorola	MC14507	
	National	CD4507	
		MM74C86	
	RCA	CD4030	
		CD4070	
	Solitron	CM4070	
	SSS	SCL4030	
		SCL4070	
	TI	TP4507	
CD4071	Fairchild	F4071	
	Mitel	SIL4071	
	Motorola	MC14071	
	NEC America	µPD4071	
	RCA	CD4071	
	Solitron	CM4071	
	SSS	SCL4071	
	TI	TP4071	
	Toshiba	TC4071	
CD4073	Fairchild	F4073	
	Mitel	SIL4073	
	Motorola	MC14073	
	NEC America	µPD4073	
	RCA	CD4073	
	Solitron	CM4073	
	SSS	SCL4073	
	TI	TP4073	
	Toshiba	TC4073	
CD4075	Fairchild	F4075	
	Mitel	SIL4075	
	Motorola	MC14075	
	NEC America	µPD4075	
	RCA	CD4075	
	SSS	SCL4075	
	TI	TP4075	
	Toshiba	TC4075	
CD4076	Fairchild	F4076	
	Harris	HD74C173	
	Mitel	SIL4076	
	Motorola	MC14076	
	RCA	CD4076	
CD4076	Solitron	CM4076	
	SSS	SCL4076	
CD4081	Fairchild	F4081	
	Mitel	SIL4081	
	Motorola	MC14081	
	NEC America	µPD4081	
	RCA	CD4081	
	Solitron	CM4081	
	SSS	SCL4081	
	TI	TP4081	
	Toshiba	TC4081	
CD4089	RCA	CD4089	
CD4093	Fairchild	F4093	
	Motorola	MC14093	
	NEC America	µPD4093	
	RCA	CD4093	
CD4099	Fairchild	F4099	
	NEC America	µPD4099	
	RCA	CD4099	
CD4503	Motorola	MC14503	
	NEC America	µPD4503	
CD4507	Motorola	MC14507	
	National	CD4070	
		MM74C86	
	RCA	CD4030	
		CD4070	
	SSS	SCL4030	
	TI	TP4507	
CD4510	Fairchild	F4510	
	Mitel	SIL4510	
	Motorola	MC14510	
	NEC America	µPD4510	
	RCA	CD40192	
		CD4510	
	SSS	SCL4510	
	Toshiba	TC4510	
CD4511	Fairchild	F4511	
	Mitel	SIL4511	
	Motorola	MC14511	
	NEC America	µPD4511	
	RCA	CD4511	
	Solitron	CM4511	
	SSS	SCL4511	
	TI	TP4511	
CD4512	Fairchild	F4512	
	Mitel	SIL4512	
	Motorola	MC14512	
	NEC America	µPD4512	
	SSS	SCL4512	
	TI	TP4512	
	Toshiba	TC4512	
CD4514	Fairchild	F4514	
	Mitel	SIL4514	
	Motorola	MC14514	
	RCA	CD4514	
	SSS	SCL4514	
	Toshiba	TC4514	
CD4515	Fairchild	F4515	
	Mitel	SIL4515	
	Motorola	MC14515	
	RCA	CD4515	
	SSS	SCL4515	
	Toshiba	TC4515	
CD4516	Fairchild	F4516	
	Mitel	SIL4516	
	Motorola	MC14516	
	NEC America	µPD4516	
	RCA	CD40193	
		CD4516	
	SSS	SCL4516	
	Toshiba	TC4516	
CD4518	Fairchild	F4518	
	Mitel	SIL4518	
	Motorola	MC14518	
	NEC America	µPD4518	
	RCA	CD4518	
	Solitron	CM4518	
	SSS	SCL4518	
	TI	TP4518	
	Toshiba	TC4518	
CD4519	Fairchild	F4519	
	Motorola	MC14519	
	NEC America	µPD4519	
	RCA	CD4019	
	TI	TP4519	
CD4520	Fairchild	F4520	
CD4520	Mitel	SIL4520	
	Motorola	MC14520	
	NEC America	µPD4520	
	RCA	CD4520	
	Solitron	CM4520	
	SSS	SCL4520	
	TI	TP4520	
	Toshiba	TC4520	
CD4522	Fairchild	F4522	
	Motorola	MC14522	
	SSS	SCL4522	
	TI	TP4522	
CD4527	Motorola	MC14527	
	RCA	CD4527	
	SSS	SCL4527	
CD4528	Fairchild	F4528	
	Motorola	MC14528	
	NEC America	µPD4528	
	RCA	CD4528	
	SSS	SCL4528	
CD4529	Motorola	MC14529	
CD4543	Motorola	MC14543	
	SSS	SCL4543	
CD4584	Motorola	MC14584	
	National	MM74C14	
	NEC America	µPD4584	
	RCA	CD4016	
	SSS	SCL4584	
DAC0800	Datel	DAC-08B	
	PMI	**DAC-08**	**919**
DAC0801	Datel	DAC-08B	
	PMI	**DAC-08**	**919**
♦DH3724	RCA	CA3724	
DH3725	RCA	CA3725	
DM10101	Motorola	MC10101	
DM10102	Motorola	MC10102	
DM10105	Fairchild	F10105	
	Hitachi	HD10105	
	Motorola	MC10105	
	NEC America	µPB10105	
	Plessey	SP10105	
	Signetics	10105	
DM10106	Fairchild	F10106	
	Hitachi	HD10106	
	Motorola	MC10106	
	NEC America	µPB10106	
	Plessey	SP10106	
	Signetics	10106	
♦DM10107	Motorola	MC10107	
DM10109	Fairchild	F10109	
	Hitachi	HD10109	
	Motorola	MC10109	
	NEC America	µPB10109	
	Plessey	SP10109	
	Signetics	10109	
♦DM10110	Motorola	MC10110	
DM10111	Fairchild	F10111	
	Hitachi	HD10111	
	Motorola	MC10111	
	NEC America	µPB10111	
	Plessey	SP10111	
	Signetics	10111	
DM10112	Plessey	SP10112	
	Signetics	10112	
DM10115	Fairchild	F10115	
	Motorola	MC10115	
	NEC America	µPB10115	
	Plessey	SP10115	
	Signetics	10115	
♦DM10116	Fairchild	F10116	
	Hitachi	HD10116	
	Motorola	MC10116	
	Plessey	SP10116	
	Signetics	10116	
DM10117	Fairchild	F10117	
	Hitachi	HD10117	
	Motorola	MC10117	
	NEC America	µPB10117	
	Plessey	SP10117	
	Signetics	10117	
DM10118	Fairchild	F10118	
	Hitachi	HD10118	
	Motorola	MC10118	
	NEC America	µPB10118	
	Plessey	SP10118	
	Signetics	10118	
DM10119	Fairchild	F10119	
	Hitachi	HD10119	
	Motorola	MC10119	
	Plessey	SP10119	
	Signetics	10119	
DM10121	Fairchild	F10121	
	Hitachi	HD10121	
	Motorola	MC10121	
	Plessey	SP10121	
	Signetics	10121	
DM10124	Fairchild	F10124	
	Hitachi	HD10124	
	Motorola	MC10124	
	NEC America	µPB10124	
	Plessey	SP10124	
	Signetics	10124	
♦DM10130	Motorola	MC10130	
♦DM1800	Motorola	MC1800	
♦DM1801	Motorola	MC1801	
DM54H00	Fairchild	54H00	
		9H00	
	ITT	ITT54H00	
	Raytheon	54H00	
	Signetics	54H00	
	TI	SN54H00	
DM54H01	Fairchild	54H01	
	ITT	ITT54H01	
	Raytheon	54H01	
	Signetics	54H01	
	TI	SN54H01	
DM54H04	Fairchild	54H04	
	ITT	ITT54H04	
	Raytheon	54H04	
	Signetics	54H04	
	TI	SN54H04	
DM54H05	Fairchild	54H05	
	ITT	ITT54H05	
	Raytheon	54H05	
	Signetics	54H05	
	TI	SN54H05	
DM54H08	Fairchild	54H08	
	Signetics	54H08	
DM54H10	Fairchild	54H10	
	ITT	ITT54H10	
	Raytheon	54H10	
	Signetics	54H10	
	TI	SN54H10	
DM54H103	Fairchild	54H103	
	Signetics	54H103	
	TI	SN54H103	
DM54H106	Fairchild	54H106	
	Signetics	54H106	
	TI	SN54H106	
DM54H108	Fairchild	54H108	
	Signetics	54H108	
	TI	SN54H108	
DM54H11	Fairchild	54H11	
	ITT	ITT54H11	
	Raytheon	54H11	
	Signetics	54H11	
	TI	SN54H11	
DM54H20	Fairchild	54H20	
	ITT	ITT54H20	
	Raytheon	54H20	
	Signetics	54H20	
	TI	SN54H20	
DM54H21	Fairchild	54H21	
	ITT	ITT54H21	
	Signetics	54H21	
DM54H22	Fairchild	54H22	
	Raytheon	54H22	
	Signetics	54H22	
	TI	SN54H22	
DM54H30	Fairchild	54H30	
	ITT	ITT54H30	
	Signetics	54H30	
	TI	SN54H30	
DM54H40	Fairchild	54H40	
	ITT	ITT54H40	
	Raytheon	54H40	
	Signetics	54H40	
	TI	SN54H40	
DM54H50	Fairchild	54H50	
	ITT	ITT54H50	
	Signetics	54H50	
	TI	SN54H50	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
DM54H51	Fairchild	54H51	
	ITT	ITT54H51	
	Signetics	54H51	
	TI	SN54H51	
DM54H52	Fairchild	54H52	
	Signetics	54H52	
	TI	SN54H52	
DM54H53	Fairchild	54H53	
	ITT	ITT54H53	
	Signetics	54H53	
	TI	SN54H53	
DM54H54	Fairchild	54H54	
	ITT	ITT54H54	
	Signetics	54H54	
	TI	SN54H54	
DM54H55	Fairchild	54H55	
	Signetics	54H55	
	TI	SN54H55	
DM54H60	Fairchild	54H60	
	ITT	ITT54H60	
	Signetics	54H60	
	TI	SN54H60	
DM54H61	Fairchild	54H61	
	Signetics	54H61	
	TI	SN54H61	
DM54H62	Fairchild	54H62	
	Signetics	54H62	
	TI	SN54H62	
DM54H71	Fairchild	54H71	
	Signetics	54H71	
	TI	SN54H71	
DM54H72	Fairchild	54H72	
		54H73	
	Signetics	54H72	
	TI	SN54H72	
DM54H73	Fairchild	54H73	
	ITT	ITT54H73	
	Signetics	54H73	
	TI	SN54H73	
DM54H74	Fairchild	54H74	
	ITT	ITT54H74	
	Raytheon	54H74	
	Signetics	54H74	
	TI	SN54H74	
DM54H76	Fairchild	54H76	
	Signetics	54H76	
	TI	SN54H76	
DM54H78	Fairchild	54H78	
	TI	SN54H78	
DM54LS00	Fairchild	54LS00	
	Motorola	SN54LS00	
	Raytheon	54LS00	
	Signetics	54LS00	
	TI	SN54LS00	
DM54LS01	Fairchild	54LS01	
	Raytheon	54LS01	
	Signetics	54LS01	
	TI	SN54LS01	
DM54LS02	Fairchild	54LS02	
	Motorola	SN54LS02	
	Raytheon	54LS02	
	Signetics	54LS02	
	TI	SN54LS02	
DM54LS03	Fairchild	54LS03	
	Motorola	SN54LS03	
	Raytheon	54LS03	
	Signetics	54LS03	
	TI	SN54LS03	
DM54LS04	Fairchild	54LS04	
	Motorola	SN54LS04	
	Raytheon	54LS04	
	Signetics	54LS04	
	TI	SN54LS04	
DM54LS05	Fairchild	54LS05	
	Motorola	SN54LS05	
	Raytheon	54LS05	
	Signetics	54LS05	
	TI	SN54LS05	
DM54LS08	Fairchild	54LS08	
	Motorola	SN54LS08	
	Raytheon	54LS08	
	Signetics	54LS08	
DM54LS08	TI	SN54LS08	
DM54LS09	Fairchild	54LS09	
	Motorola	SN54LS09	
	Raytheon	54LS09	
	Signetics	54LS09	
	TI	SN54LS09	
DM54LS10	Fairchild	54LS10	
	Motorola	SN54LS10	
	Raytheon	54LS10	
	Signetics	54LS10	
	TI	SN54LS10	
DM54LS107	Fairchild	54LS107	
	Motorola	SN54LS107	
	Raytheon	54LS107	
	Signetics	54LS107	
	TI	SN54LS107	
DM54LS109	Fairchild	54LS109	
	Motorola	SN54LS109	
	Raytheon	54LS109	
	Signetics	54LS109	
	TI	SN54LS109	
DM54LS11	Fairchild	54LS11	
	Motorola	SN54LS11	
	Raytheon	54LS11	
	Signetics	54LS11	
	TI	SN54LS11	
DM54LS112	Fairchild	54LS112	
	Raytheon	54LS112	
	Signetics	54LS112	
	TI	SN54LS112	
DM54LS113	Fairchild	54LS113	
	Raytheon	54LS113	
	Signetics	54LS113	
	TI	SN54LS113	
DM54LS114	Fairchild	54LS114	
	Motorola	SN54LS114	
	Raytheon	54LS114	
	Signetics	54LS114	
	TI	SN54LS114	
DM54LS12	Fairchild	54LS12	
	Raytheon	54LS12	
	Signetics	54LS12	
	TI	SN54LS12	
DM54LS122	**Raytheon**	**54LS122**	**275**
	TI	SN54LS122	
DM54LS123	AMD	SN54LS123	
	Raytheon	**54LS123**	**275**
	TI	SN54LS123	
DM54LS125	Fairchild	54LS125	
	Raytheon	54LS125	
	Signetics	54LS125	
	TI	SN54LS125A	
DM54LS126	Fairchild	54LS126	
	Motorola	SN54LS126	
	Raytheon	54LS126	
	Signetics	54LS126	
	TI	SN54LS126A	
DM54LS13	Motorola	SN54LS13	
	Raytheon	**54LS13**	**264**
	Signetics	54LS13	
	TI	SN54LS13	
DM54LS132	Fairchild	54LS132	
	Motorola	SN54LS132	
	Raytheon	**54LS132**	**264**
		74LS132	**264**
	Signetics	54LS132	
	TI	SN54LS132	
DM54LS136	Motorola	SN54SL136	
DM54LS138	Fairchild	54LS138	
	Motorola	SN54LS138	
	Raytheon	54LS138	
	Signetics	54LS138	
	TI	SN54LS138	
DM54LS139	AMD	SN54LS139	
	Fairchild	54LS139	
	Motorola	SN54LS139	
	Raytheon	54LS139	
	Signetics	74LS139	
	TI	SN54LS139	
DM54LS14	Fairchild	54LS14	
	Motorola	SN54LS14	
	Raytheon	**54LS14**	**264**
	Signetics	54LS14	
	TI	SN54LS14	
DM54LS15	Fairchild	54LS15	
	Motorola	SN54LS15	
DM54LS15	Raytheon	54LS15	
	Signetics	54LS15	
	TI	SN54LS15	
DM54LS151	AMD	SN54LS151	
	Fairchild	54LS151	
	Motorola	SN54LS151	
	Raytheon	54LS151	
	Signetics	54LS151	
	TI	SN54LS151	
DM54LS153	AMD	SN54LS153	
	Fairchild	54LS153	
	Motorola	SN54LS153	
	Raytheon	54LS153	
	Signetics	54LS153	
	TI	SN54LS153	
DM54LS154	Signetics	54LS154	
DM54LS155	Fairchild	54LS155	
	Motorola	SN54LS155	
	Raytheon	74LS155	
	TI	SN54LS155	
DM54LS156	Fairchild	54LS156	
	Motorola	SN54LS156	
	Raytheon	54LS156	
	TI	SN54LS156	
DM54LS157	AMD	SN54LS157	
	Fairchild	54LS157	
	Motorola	SN54LS157	
	Raytheon	54LS157	
	Signetics	54LS157	
	TI	SN54LS157	
DM54LS158	Fairchild	54LS158	
	Motorola	SN54LS158	
	Raytheon	54LS158	
	Signetics	54LS158	
	TI	SN54LS158	
DM54LS160	AMD	SN54LS160	
	Fairchild	54LS160	
	Motorola	SN54LS160	
	Raytheon	54LS160	
	TI	SN54LS160	
DM54LS161	AMD	SN54LS161	
	Fairchild	54LS161	
	Motorola	SN54LS161	
	Raytheon	54LS161	
	Signetics	54LS161	
	TI	SN54LS161	
DM54LS162	AMD	SN54LS162	
	Fairchild	54LS162	
	Motorola	SN54LS162	
	Raytheon	54LS162	
	TI	SN54LS162	
DM54LS163	AMD	SN54LS163	
	Fairchild	54LS163	
	Motorola	SN54LS163	
	Raytheon	54LS163	
	Signetics	54LS163	
	TI	SN54LS163	
DM54LS164	AMD	SN54LS164	
	Fairchild	54LS164	
	Motorola	SN54LS164	
	Raytheon	**54LS164**	**272**
	Signetics	54LS164	
	TI	SN54LS164	
DM54LS168	AMD	SN54LS168	
	Fairchild	54LS168	
	TI	SN54LS168	
DM54LS169	AMD	SN54LS169	
	Fairchild	54LS169	
	TI	SN54LS169	
DM54LS170	AMD	SN54LS170	
	Fairchild	54LS170	
	Motorola	SN54LS170	
	Raytheon	54LS170	
	Signetics	54LS170	
	TI	SN54LS170	
DM54LS173	Fairchild	54LS173	
	Signetics	54LS173	
	TI	SN54LS173	
DM54LS174	AMD	SN54LS174	
	Fairchild	54LS174	
	Raytheon	54LS174	
	Signetics	54LS174	
	TI	SN54LS174	
DM54LS175	AMD	SN54LS175	
	Fairchild	54LS175	
	Motorola	SN54LS175	
DM54LS175	Raytheon	54LS175	
	Signetics	54LS175	
	TI	SN54LS175	
DM54LS190	AMD	SN54LS190	
	Fairchild	54LS190	
	Motorola	SN54LS190	
	Raytheon	54LS190	
	Signetics	54LS190	
	TI	SN54LS190	
DM54LS191	AMD	SN54LS191	
	Fairchild	54LS191	
	Motorola	SN54LS191	
	Raytheon	54LS191	
	Signetics	54LS191	
	TI	SN54LS191	
DM54LS192	AMD	SN54LS192	
	Fairchild	54LS192	
	Motorola	SN54LS192	
	Raytheon	54LS192	
	Signetics	54LS192	
	TI	SN54LS192	
DM54LS193	AMD	SN54LS193	
	Fairchild	54LS193	
	Motorola	SN54LS193	
	Raytheon	54LS193	
	Signetics	54LS193	
	TI	SN54LS193	
DM54LS196	Fairchild	54LS196	
	Motorola	SN54LS196	
	Raytheon	54LS196	
	TI	SN54LS196	
DM54LS197	Fairchild	54LS197	
	Motorola	SN54LS197	
	Raytheon	54LS197	
	TI	SN54LS197	
DM54LS20	Fairchild	54LS20	
	Motorola	SN54LS20	
	Raytheon	54LS20	
	Signetics	54LS20	
	TI	SN54LS20	
DM54LS21	Fairchild	54LS21	
	Motorola	SN54LS21	
	Raytheon	54LS21	
	Signetics	54LS21	
	TI	SN54LS21	
DM54LS22	Fairchild	54LS22	
	Motorola	SN54LS22	
	Raytheon	54LS22	
	Signetics	54LS22	
	TI	SN54LS22	
DM54LS221	**Raytheon**	**54LS221**	**275**
	Signetics	54LS221	
	TI	SN54LS221	
DM54LS247	TI	SN54LS247	
DM54LS248	TI	SN54LS248	
DM54LS249	TI	SN54LS249	
DM54LS253	AMD	SN54LS253	
	Fairchild	54LS253	
	Motorola	SN54LS253	
	Raytheon	54LS253	
	Signetics	54LS253	
	TI	SN54LS253	
DM54LS257	Fairchild	54LS257	
	Motorola	SN54LS257	
	Raytheon	54LS257	
	Signetics	54LS257	
	TI	SN54LS257	
DM54LS26	Fairchild	54LS26	
	Raytheon	54LS26	
	Signetics	54LS26	
	TI	SN54LS26	
DM54LS27	Fairchild	54LS27	
	Motorola	SN54LS27	
	Raytheon	54LS27	
	Signetics	54LS27	
	TI	SN54LS27	
DM54LS279	Fairchild	54LS279	
	Motorola	SN54LS279	
	Raytheon	74LS279	
	Signetics	54LS279	
	TI	SN54LS279	
DM54LS283	Fairchild	54LS283	
	Motorola	SN54LS283	
	Raytheon	54LS283	
	TI	SN54LS283	
DM54LS30	Fairchild	54LS30	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
DM54LS30	Motorola	SN54LS30	
	Raytheon	54LS30	
	Signetics	54LS30	
	TI	SN54LS30	
DM54LS32	Fairchild	54LS32	
	Motorola	SN54LS32	
	Raytheon	54LS32	
	Signetics	54LS32	
	TI	SN54LS32	
DM54LS352	Fairchild	54LS352	
	TI	SN54LS352	
DM54LS353	Fairchild	54LS353	
	TI	SN54LS353	
DM54LS37	Fairchild	54LS37	
	Motorola	SN54LS37	
	Raytheon	54LS37	
	Signetics	54LS37	
	TI	SN54LS37	
DM54LS38	Fairchild	54LS38	
	Motorola	SN54LS38	
	Raytheon	54LS38	
	Signetics	54LS38	
	TI	SN54LS38	
DM54LS395	Fairchild	54LS095	
	Raytheon	**54LS395**	**291**
	Signetics	54LS395	
	TI	SN54LS395	
DM54LS40	Fairchild	54LS40	
	Motorola	SN54LS40	
	Raytheon	54LS40	
	Signetics	54LS40	
	TI	SN54LS40	
DM54LS42	Fairchild	54LS42	
	Motorola	SN54LS42	
	Raytheon	**54LS42**	**266**
	Signetics	54LS42	
	TI	SN54LS42	
DM54LS51	Fairchild	54LS51	
	Motorola	SN54LS51	
	Raytheon	54LS51	
	Signetics	54LS51	
	TI	SN54LS51	
DM54LS54	Fairchild	54LS54	
	Motorola	SN54LS54	
	Raytheon	54LS54	
	Signetics	54LS54	
	TI	SN54LS54	
DM54LS55	Fairchild	54LS55	
	Motorola	SN54LS55	
	Raytheon	54LS55	
	Signetics	54LS55	
	TI	SN54LS55	
DM54LS670	AMD	SN54LS670	
	Fairchild	54LS670	
	Motorola	SN54LS670	
	Raytheon	54LS670	
	Signetics	54LS670	
	TI	SN54LS670	
DM54LS73	Fairchild	54LS73	
	Motorola	SN54LS73	
	Raytheon	54LS73	
	Signetics	54LS73	
	TI	SN54LS73	
DM54LS74	Fairchild	54LS74	
	Motorola	SN54LS74	
	Raytheon	54LS74	
	Signetics	54LS74	
	TI	SN54LS74	
DM54LS75	Fairchild	54LS75	
	Raytheon	54LS75	
	Signetics	54LS75	
	TI	SN54LS75	
DM54LS76	Raytheon	54LS76	
	Signetics	54LS76	
	TI	SN54LS76	
DM54LS78	Raytheon	54LS78	
	Signetics	54LS78	
	TI	SN54LS78	
DM54LS83A	Fairchild	54LS83	
	Motorola	SN54LS83	
	Raytheon	54LS83A	
	TI	SN54LS83A	
DM54LS85	Fairchild	54LS85	
	Raytheon	54LS85	
	Signetics	54LS85	
	TI	SN54LS85	
DM54LS93	Fairchild	54LS93	
	Motorola	SN54LS93	
	Raytheon	**54LS93**	**268**
	Signetics	54LS93	
	TI	SN54LS93	
DM54L187	Intersil	IM5603	
DM54L89	MMI	L5560	
	TI	SN54S287	
DM54S22	Fairchild	54S22	
	Signetics	54S22	
	TI	SN54S22	
DM54S387	Intel	M3601	
	MMI	**5300**	**1248**
	TI	SN54S387	
DM5400	Fairchild	5400	
		9N00	
	ITT	ITT5400	
	Motorola	MC5400	
	Raytheon	5400	
	Signetics	5400	
	TI	SN5400	
DM5401	Fairchild	5401	
	ITT	ITT5401	
	Motorola	MC5401	
	Raytheon	5401	
	Signetics	5401	
	TI	SN5401	
DM5402	Fairchild	5402	
	ITT	ITT5402	
	Motorola	MC5402	
	Signetics	5402	
	TI	SN5402	
DM5403	Fairchild	5403	
	ITT	ITT5403	
	Motorola	MC5403	
	Raytheon	5403	
	Signetics	5403	
	TI	SN5403	
DM5404	Fairchild	5404	
	ITT	ITT5404	
	Motorola	MC5404	
	Raytheon	5404	
	Signetics	5404	
	TI	SN5404	
DM5405	Fairchild	5405	
	ITT	ITT5405	
	Motorola	MC5405	
	Raytheon	5405	
	Signetics	5405	
	TI	SN5405	
DM5406	Fairchild	5406	
	ITT	ITT5406	
	Motorola	MC5406	
	Signetics	5406	
	TI	SN5406	
DM5407	Fairchild	5407	
	ITT	ITT5407	
	Motorola	MC5407	
	Signetics	5407	
	TI	SN5407	
DM5408	Fairchild	5408	
	ITT	ITT5408	
	Motorola	MC5408	
	Raytheon	5408	
	Signetics	5408	
	TI	SN5408	
DM5409	Fairchild	5409	
	ITT	ITT5409	
	Motorola	MC5409	
	Raytheon	5409	
	Signetics	5409	
	TI	SN5409	
DM5410	Fairchild	5410	
	ITT	ITT5410	
	Motorola	MC5410	
	Raytheon	5410	
	Signetics	5410	
	TI	SN5410	
DM54107	Fairchild	54107	
	ITT	ITT54107	
	Motorola	MC54107	
	Signetics	54107	
DM54107	TI	SN54107	
DM54109	Signetics	54109	
	TI	SN54109	
DM5411	Fairchild	5411	
	ITT	ITT5411	
	Raytheon	5411	
	Signetics	5411	
	TI	SN5411	
♦DM5412	Raytheon	5412	
DM54121	Fairchild	54121	
	ITT	ITT54121	
	Motorola	MC54121	
	Signetics	54121	
	TI	SN54121	
DM54123	AMD	SN54123	
	Fairchild	54123	
	ITT	ITT54123	
	Motorola	MC54123	
	Raytheon	54123	
	Signetics	54123	
	TI	SN54123	
DM54125	Fairchild	54125	
	Signetics	54125	
	TI	SN54125	
DM54126	Fairchild	54126	
	Signetics	54126	
	TI	SN54126	
DM5413	Fairchild	5413	
	ITT	ITT5413	
	Motorola	MC5413	
	Signetics	5413	
	TI	SN5413	
DM54132	Fairchild	54132	
	Motorola	MC54132	
	Signetics	54132	
	TI	SN54132	
♦DM54136	Raytheon	54136	
DM5414	Fairchild	5414	
	Motorola	MC5414	
	Signetics	5414	
	TI	SN5414	
DM54141	Motorola	MC54141	
	TI	SN54141	
DM54145	Fairchild	54145	
	ITT	ITT54145	
	Motorola	MC54145	
	Raytheon	54145	
	Signetics	54145	
	TI	SN54145	
DM54147	Signetics	54147	
	TI	SN54147	
DM54148	Signetics	54148	
	TI	SN54148	
♦DM5415	Raytheon	5415	
DM54150	Fairchild	54150	
	Motorola	MC54150	
	Raytheon	54150	
	Signetics	54150	
	TI	SN54150	
DM54151	Fairchild	54151	
	ITT	ITT54151	
	Motorola	MC54151	
	Raytheon	54151	
	Signetics	54151	
	TI	SN54151	
♦DM54152	Raytheon	54152	
DM54153	AMD	SN54153	
	Fairchild	54153	
	ITT	ITT54153	
	Motorola	MC54153	
	Raytheon	54153	
	Signetics	54153	
	TI	SN54153	
DM54154	AMD	SN54154	
	Fairchild	54154	
	Motorola	MC54154	
	Raytheon	54154	
	Signetics	54154	
	TI	SN54154	
DM54155	Fairchild	54155	
	ITT	ITT54155	
	Motorola	MC54155	
	Raytheon	54155	
	Signetics	54155	
	TI	SN54155	
DM54156	Fairchild	54156	
DM54156	ITT	ITT54156	
	Motorola	MC54156	
	Raytheon	54156	
	Signetics	54156	
	TI	SN54156	
DM54157	AMD	SN54157	
	Fairchild	54157	
	ITT	ITT54157	
	Motorola	MC54157	
	Raytheon	54157	
	Signetics	54157	
	TI	SN54157	
♦DM54158	Raytheon	54158	
♦DM54159	Raytheon	54159	
DM5416	Fairchild	5416	
	ITT	ITT5416	
	Motorola	MC5416	
	Signetics	5416	
	TI	SN5416	
DM54160	AMD	SN54160	
	Fairchild	54160	
	ITT	ITT54160	
	Motorola	MC54160	
	Raytheon	54160	
	Signetics	54160	
	TI	SN54160	
DM54161	AMD	SN54161	
	Fairchild	54161	
	ITT	ITT54161	
	Motorola	MC54161	
	Raytheon	54161	
	Signetics	54161	
	TI	SN54161	
DM54162	AMD	SN54162	
	Fairchild	54162	
	ITT	ITT54162	
	Motorola	MC54162	
	Raytheon	54162	
	Signetics	54162	
	TI	SN54162	
DM54163	AMD	SN54163	
	Fairchild	54163	
	ITT	ITT54163	
	Motorola	MC54163	
	Raytheon	54163	
	Signetics	54163	
	TI	SN54163	
DM54164	AMD	SN54164	
	Fairchild	54164	
	ITT	ITT54164	
	Raytheon	54164	
	Signetics	54164	
	TI	SN54164	
DM54165	Fairchild	54165	
	Motorola	MC54165	
	Raytheon	54165	
	Signetics	54165	
	TI	SN54165	
DM54166	Fairchild	54166	
	Raytheon	54166	
	Signetics	54166	
	TI	SN54166	
DM5417	Fairchild	5417	
	ITT	ITT5417	
	Motorola	MC5417	
	Signetics	5417	
	TI	SN5417	
♦DM54170	Fairchild	54170	
	Raytheon	54170	
	Signetics	54170	
	TI	SN54170	
DM54173	Fairchild	54173	
	TI	SN54173	
DM54174	AMD	SN74174	
	Fairchild	54174	
	Motorola	MC54174	
	Raytheon	54174	
	Signetics	54174	
	TI	SN54174	
DM54175	AMD	SN54175	
	Fairchild	54175	
	Motorola	MC54175	
	Raytheon	54175	
	Signetics	54175	
	TI	SN54175	
DM54176	Fairchild	54176	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
DM54176	Motorola	MC54176	
	Signetics	54176	
	TI	SN54176	
DM54177	Fairchild	54177	
	Motorola	MC54177	
	Signetics	54177	
	TI	SN54177	
DM54180	Fairchild	54180	
	ITT	ITT54180	
	Motorola	MC54180	
	Raytheon	54180	
	Signetics	54180	
	TI	SN54180	
DM54181	AMD	SN54181	
	Fairchild	54181	
	Motorola	MC54181	
	Raytheon	54181	
	Signetics	54181	
	TI	SN54181	
DM54182	AMD	SN54182	
	Fairchild	54182	
	ITT	ITT54182	
	Motorola	MC54182	
	Raytheon	54182	
	Signetics	54182	
	TI	SN54182	
DM54184	TI	SN54184	
DM54185	TI	SN54185	
♦DM54187	Intersil	IM5603	
	MMI	**5200**	**1252**
	National	DM54S187	
	TI	SN54187	
DM54190	Fairchild	54190	
	ITT	ITT54190	
	Motorola	MC54190	
	Raytheon	54190	
	Signetics	54190	
	TI	SN54190	
DM54191	Fairchild	54191	
	ITT	ITT54191	
	Motorola	MC54191	
	Raytheon	54191	
	Signetics	54191	
	TI	SN54191	
DM54192	AMD	SN54192	
	Fairchild	54192	
	ITT	ITT54192	
	Motorola	MC54192	
	Raytheon	54192	
	Signetics	54192	
	TI	SN54192	
DM54193	AMD	SN54193	
	Fairchild	54193	
	ITT	ITT54193	
	Motorola	MC54193	
	Raytheon	54193	
	Signetics	54193	
	TI	SN54193	
DM54194	AMD	SN54194	
	Fairchild	54194	
	ITT	ITT54194	
	Motorola	MC54194	
	Raytheon	54194	
	Signetics	54194	
	TI	SN54194	
DM54195	AMD	SN54195	
	Fairchild	54195	
	ITT	ITT54195	
	Motorola	MC54195	
	Raytheon	54195	
	Signetics	54195	
	TI	SN54195	
DM54196	Fairchild	54196	
	Motorola	MC54196	
	Signetics	54196	
	TI	SN54196	
DM54197	Fairchild	54197	
	Motorola	MC54197	
	Signetics	54197	
	TI	SN54197	
DM54198	Fairchild	54198	
	Raytheon	54198	
DM54198	Signetics	54198	
	TI	SN54198	
DM54199	Fairchild	54199	
	Raytheon	54199	
	Signetics	54199	
	TI	SN54199	
DM5420	Fairchild	5420	
	ITT	ITT5420	
	Motorola	MC5420	
	Raytheon	5420	
	Signetics	5420	
	TI	SN5420	
♦DM54200	MMI	5531	
	Raytheon	RM5340	
	TI	SN54S201	
♦DM5421	Raytheon	5421	
♦DM5422	Raytheon	5422	
DM5423	Fairchild	5423	
	Motorola	MC5423	
	TI	SN5423	
DM5425	Fairchild	5425	
	ITT	ITT5425	
	Motorola	MC5425	
	TI	SN5425	
DM54251	TI	SN54251	
DM5426	Fairchild	5426	
	ITT	ITT5426	
	Motorola	MC5426	
	Signetics	5426	
	TI	SN5426	
DM5427	Fairchild	5427	
	Motorola	MC5427	
	TI	SN5427	
♦DM54283	Raytheon	54283	
DM5430	Fairchild	5430	
	ITT	ITT5430	
	Motorola	MC5430	
	Signetics	5430	
	TI	SN5430	
DM5432	Fairchild	5432	
	ITT	ITT5432	
	Signetics	5432	
	TI	SN5432	
DM5437	Fairchild	5437	
	ITT	ITT5437	
	Motorola	MC5437	
	Raytheon	5437	
	Signetics	5437	
	TI	SN5437	
DM5438	Fairchild	5438	
	ITT	ITT5438	
	Motorola	MC5438	
	Raytheon	5438	
	Signetics	5438	
	TI	SN5438	
DM5440	Fairchild	5440	
	ITT	ITT5440	
	Motorola	MC5440	
	Signetics	5440	
	TI	SN5440	
DM5441	Fairchild	5441	
DM5442	Fairchild	5442	
	ITT	ITT5442	
	Motorola	MC5442	
	Raytheon	5442	
	Signetics	5442	
	TI	SN5442	
♦DM5443	Raytheon	5443	
♦DM5444	Raytheon	5444	
DM5445	Fairchild	5445	
	ITT	ITT5445	
	Motorola	MC5445	
	Raytheon	5445	
	Signetics	5445	
	TI	SN5445	
DM5446	Fairchild	5446	
	ITT	ITT5446	
	Motorola	MC5446	
	Signetics	5446	
	TI	SN5446	
DM5447	Fairchild	5447	
	ITT	ITT5447	
	Motorola	MC5447	
	Signetics	5447	
	TI	SN5447	
DM5448	Fairchild	5448	
DM5448	ITT	ITT5448	
	Motorola	MC5448	
	Signetics	5448	
	TI	SN5448	
DM5450	Fairchild	5450	
	ITT	ITT5450	
	Motorola	MC5450	
	Signetics	5450	
	TI	SN5450	
DM5451	Fairchild	5451	
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	Signetics	5451	
	TI	SN5451	
DM5453	Fairchild	5453	
	ITT	ITT5453	
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	Signetics	5453	
	TI	SN5453	
DM5454	Fairchild	5454	
	ITT	ITT5454	
	Motorola	MC5454	
	Signetics	5454	
	TI	SN5454	
DM5460	Fairchild	5460	
	ITT	ITT5460	
	Motorola	MC5460	
	Signetics	5460	
	TI	SN5460	
DM5470	Fairchild	5470	
	ITT	ITT5470	
	Motorola	MC5470	
	TI	SN5470	
DM5472	Fairchild	5472	
	ITT	ITT5472	
	Motorola	MC5472	
	Signetics	5472	
	TI	SN5472	
DM5473	Fairchild	5473	
	ITT	ITT5473	
	Motorola	MC5473	
	Signetics	5473	
	TI	SN5473	
DM5474	Fairchild	5474	
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	Motorola	MC5474	
	Raytheon	5474	
	Signetics	5474	
	TI	SN5474	
DM5475	Fairchild	5475	
	ITT	ITT5475	
	Motorola	MC5475	
	Signetics	5475	
	TI	SN5475	
DM5476	Fairchild	5476	
	ITT	ITT5476	
	Motorola	MC5476	
	Signetics	5476	
	TI	SN5476	
DM5483	Raytheon	5483	
DM5485	Fairchild	5485	
	Motorola	MC5485	
	Signetics	5485	
	TI	SN5485	
DM5486	Fairchild	5486	
	ITT	ITT5486	
	Motorola	MC5486	
	Raytheon	5486	
	Signetics	5486	
	TI	SN5486	
DM5488	Intersil	IM5600	
	MMI	**5230**	**1252**
	TI	SN5488	
		SN5488A	
DM5489	AMD	SN5489	
		31013	
		5889	
	Fairchild	5489	
	MMI	5560	
	Raytheon	5489	
	TI	SN5489	
DM5490	Fairchild	5490	
	ITT	ITT5490	
	Motorola	MC5490	
	Signetics	5490	
	TI	SN5490	
DM5490	TI	SN5490A	
DM5491	Fairchild	5491	
	ITT	ITT5491	
	Motorola	MC5491	
	Signetics	5491	
	TI	SN5491	
		SN5491A	
DM5492	Fairchild	5492	
	ITT	ITT5492	
	Motorola	MC5492	
	Signetics	5492	
	TI	SN5492	
		SN5492A	
DM5493	Fairchild	5493	
	ITT	ITT5493	
	Motorola	MC5493	
	Signetics	5493	
	TI	SN5493	
		SN5493A	
DM5495	Fairchild	5495	
	ITT	ITT5495	
	Motorola	MC5495	
	Signetics	5495	
	TI	SN5495	
DM5496	Fairchild	5496	
	ITT	ITT5496	
	Motorola	MC5496	
	Signetics	5496	
	TI	SN5496	
DM7093	TI	SN54125	
DM7094	TI	SN54126	
DM7095	TI	SN54365	
DM7096	TI	SN54366	
DM7097	TI	SN54367	
DM7098	TI	SN54368	
DM71L22	TI	SN54L157	
DM71S60	Fairchild	93S43	
DM7121	TI	SN54251	
DM7123	TI	SN54S257	
DM7213	TI	SN54154	
DM7214	TI	SN54LS253	
DM7280	TI	SN54176	
DM7281	TI	SN54177	
DM7283	TI	SN54836	
DM7290	TI	SN54196	
DM7291	TI	SN54197	
DM74H00	Fairchild	74H00	
		9H00	
	NEC America	μPB74H00	
	Raytheon	74H00	
	Signetics	74H00	
	TI	SN74H00	
DM74H01	Fairchild	74H01	
	ITT	ITT74H01	
	NEC America	μPB74H01	
	Raytheon	74H01	
	Signetics	74H01	
	TI	SN74H01	
DM74H04	Fairchild	74H04	
	ITT	ITT74H04	
	NEC America	μPB74H04	
	Raytheon	74H04	
	Signetics	74H04	
	TI	SN74H04	
DM74H05	Fairchild	74H05	
	ITT	ITT74H05	
	Raytheon	74H05	
	Signetics	74H05	
	TI	SN74H05	
DM74H08	Fairchild	74H08	
	Signetics	74H08	
DM74H10	Fairchild	74H10	
	ITT	ITT74H10	
	NEC America	μPB74H10	
	Raytheon	74H10	
	Signetics	74H10	
	TI	SN74H10	
DM74H103	Fairchild	74H103	
	Signetics	74H103	
	TI	SN74H103	
DM74H106	Fairchild	74H106	
	Signetics	74H106	
	TI	SN74H106	
DM74H108	Fairchild	74H108	
	Signetics	74H108	
	TI	SN74H108	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
DM74H11	Fairchild	74H11	
	ITT	ITT74H11	
	Raytheon	74H11	
	Signetics	74H11	
	TI	SN74H11	
DM74H20	Fairchild	74H20	
	ITT	ITT74H20	
	NEC America	μPB74H20	
	Raytheon	74H20	
	Signetics	74H20	
	TI	SN74H20	
DM74H21	Fairchild	74H21	
	ITT	ITT74H21	
	Signetics	74H21	
	TI	SN74H21	
DM74H22	Fairchild	74H22	
	Raytheon	74H22	
	Signetics	74H22	
	TI	SN74H22	
DM74H30	Fairchild	74H30	
	ITT	ITT74H30	
	NEC America	μPB74H30	
	Signetics	74H30	
	TI	SN74H30	
DM74H40	Fairchild	74H40	
	ITT	ITT74H40	
	NEC America	μPB74H40	
	Raytheon	74H40	
	Signetics	74H40	
	TI	SN74H40	
DM74H50	Fairchild	74H50	
	ITT	ITT74H50	
	Signetics	74H50	
	TI	SN74H50	
DM74H51	Fairchild	74H51	
	ITT	ITT74H51	
	NEC America	μPB74H51	
	~~Signetics~~	~~74H51~~	
	TI	SN74H51	
DM74H52	Fairchild	74H52	
	Signetics	74H52	
	TI	SN74H52	
DM74H53	Fairchild	74H53	
	ITT	ITT74H53	
	Signetics	74H53	
	TI	SN74H53	
DM74H54	Fairchild	74H54	
	ITT	ITT74H54	
	Signetics	74H54	
	TI	SN74H54	
DM74H55	Fairchild	74H55	
	Signetics	74H55	
	TI	SN74H55	
DM74H60	Fairchild	74H60	
	ITT	ITT74H60	
	Signetics	74H60	
	TI	SN74H60	
DM74H62	Fairchild	74H62	
	Signetics	74H62	
	TI	SN74H62	
DM74H71	Fairchild	74H71	
	Signetics	74H71	
	TI	SN74H71	
DM74H72	Fairchild	74H72	
	ITT	ITT74H72	
	Signetics	74H72	
	TI	SN74H72	
DM74H73	Fairchild	74H73	
	ITT	ITT74H73	
	Signetics	74H73	
	TI	SN74H73	
DM74H74	Fairchild	74H74	
	ITT	ITT74H74	
	Raytheon	74H74	
	Signetics	74H74	
	TI	SN74H74	
DM74H76	Fairchild	74H76	
	Signetics	74H76	
	TI	SN74H76	
DM74H78	Fairchild	74H78	
	TI	SN74H78	
DM74LS00	Fairchild	74LS00	
DM74LS00	ITT	ITT74LS00	
	Motorola	SN74LS00	
	NEC America	μPB74LS00	
	Raytheon	74LS00	
	Signetics	74LS00	
	TI	SN74LS00	
DM74LS01	Fairchild	74LS01	
	ITT	ITT74LS01	
	Raytheon	74LS01	
	Signetics	74LS01	
	TI	SN74LS01	
DM74LS02	Fairchild	74LS02	
	ITT	ITT74LS02	
	Motorola	SN74LS02	
	NEC America	μPB74LS02	
	Raytheon	74LS02	
	Signetics	74LS02	
	TI	SN74LS02	
DM74LS03	Fairchild	74LS03	
	ITT	ITT74LS03	
	Motorola	SN74LS03	
	NEC America	μPB74LS03	
	Raytheon	74LS03	
	Signetics	74LS03	
	TI	SN74LS03	
DM74LS04	Fairchild	74LS04	
	ITT	ITT74LS04	
	Motorola	SN74LS04	
	NEC America	μPB74LS04	
	Raytheon	74LS04	
	Signetics	74LS04	
	TI	SN74LS04	
DM74LS05	Fairchild	74LS05	
	ITT	ITT74LS05	
	Motorola	SN74LS05	
	NEC America	μPB74LS05	
	Raytheon	74LS05	
	Signetics	74LS05	
	TI	SN74LS05	
DM74LS08	Fairchild	74LS08	
	ITT	ITT74LS08	
	~~Motorola~~	~~SN74LS08~~	
	NEC America	μPB74LS08	
	Raytheon	74LS08	
	Signetics	74LS08	
	TI	SN74LS08	
DM74LS09	Fairchild	74LS09	
	ITT	ITT74LS09	
	Motorola	SN74LS09	
	Raytheon	74LS09	
	Signetics	74LS09	
	TI	SN74LS09	
DM74LS10	Fairchild	74LS10	
	ITT	ITT74LS10	
	Motorola	SN74LS10	
	NEC America	μPB74LS10	
	Raytheon	74LS10	
	Signetics	74LS10	
	TI	SN74LS10	
DM74LS107	Fairchild	74LS107	
	Raytheon	74LS107	
	Signetics	74LS107	
	TI	SN74LS107	
DM74LS109	Fairchild	74LS109	
	ITT	ITT74LS109A	
	Motorola	SN74LS109	
	NEC Americа	μPB74LS109	
	Raytheon	74LS109	
	Signetics	74LS109	
	TI	SN74LS109	
DM74LS11	Fairchild	74LS11	
	ITT	ITT74LS11	
	Motorola	SN74LS11	
	NEC America	μPB74LS11	
	Raytheon	74LS11	
	Signetics	74LS11	
	TI	SN74LS11	
DM74LS112	Fairchild	74LS112	
	ITT	ITT74LS112	
	NEC America	μPB74LS112	
	Raytheon	74LS112	
	Signetics	74LS112	
	TI	SN74LS112	
DM74LS113	Fairchild	74LS113	
	ITT	ITT74LS113	
	NEC America	μPB74LS113	
DM74LS113	Raytheon	74LS113	
	Signetics	74LS113	
	TI	SN74LS113	
DM74LS114	Fairchild	74LS114	
	ITT	ITT74LS114	
	Motorola	SN74LS114	
	Raytheon	74LS114	
	Signetics	74LS114	
	TI	SN74LS114	
DM74LS12	Fairchild	74LS12	
	Raytheon	74LS12	
	Signetics	74LS12	
	TI	SN74LS12	
DM74LS122	**Raytheon**	**74LS122**	**275**
	TI	SN74LS122	
DM74LS123	AMD	SN74LS123	
	ITT	ITT74LS123	
	Raytheon	**74LS123**	**275**
	TI	SN74LS123	
DM74LS125	Fairchild	74LS125	
	ITT	ITT74LS125	
	Raytheon	74LS125	
	Signetics	74LS125	
	TI	SN74LS125A	
DM74LS126	Fairchild	74LS126	
	ITT	ITT74LS126	
	Motorola	SN74LS126	
	Raytheon	74LS126	
	Signetics	74LS126	
	TI	SN74LS126A	
DM74LS13	Fairchild	74LS13	
	ITT	ITT74LS13	
	Motorola	SN74LS13	
	Raytheon	**74LS13**	**264**
	Signetics	74LS13	
	TI	SN74LS13	
DM74LS132	Fairchild	74LS132	
	ITT	ITT74LS132	
	Motorola	SN74LS132	
	Raytheon	**74LS132**	**264**
	Signetics	74LS132	
	TI	**SN74LS132**	
DM74LS136	Fairchild	74LS136	
	ITT	ITT74LS136	
	Motorola	SN74LS136	
	Raytheon	74LS136	
	Signetics	74LS136	
	TI	SN74LS136	
DM74LS138	AMD	SN74LS138	
	Fairchild	74LS138	
	ITT	ITT74LS138	
	Motorola	SN74LS138	
	NEC America	μPB74LS138	
	Raytheon	74LS138	
	Signetics	74LS138	
	TI	SN74LS138	
DM74LS139	AMD	SN74LS139	
	Fairchild	74LS139	
	ITT	ITT74LS139	
	Motorola	SN74LS139	
	NEC America	μPB74LS139	
	Raytheon	74LS139	
	Signetics	74LS139	
	TI	SN74LS139	
DM74LS14	Fairchild	74LS14	
	ITT	ITT74LS14	
	Motorola	SN74LS14	
	Raytheon	**74LS14**	**264**
	Signetics	74LS14	
	TI	SN74LS14	
DM74LS15	Fairchild	74LS15	
	ITT	ITT74LS15	
	Motorola	SN74LS15	
	Raytheon	74LS15	
	Signetics	74LS15	
	TI	SN74LS15	
DM74LS151	AMD	SN74LS151	
	Fairchild	74LS151	
	ITT	ITT74LS151	
	Motorola	SN74LS151	
	NEC America	μPB74LS151	
	Raytheon	74LS151	
	Signetics	74LS151	
	TI	SN74LS151	
DM74LS153	AMD	SN74LS153	
	Fairchild	74LS153	
DM74LS153	ITT	ITT74LS153	
	Motorola	SN74LS153	
	NEC America	μPB74LS153	
	Raytheon	74LS153	
	Signetics	74LS153	
	TI	SN74LS153	
DM74LS154	Signetics	74LS154	
DM74LS155	Fairchild	74LS155	
	ITT	ITT74LS155	
	Motorola	SN74LS155	
	NEC America	μPB74LS155	
	Raytheon	74LS155	
	Signetics	74LS155	
	TI	SN74LS155	
DM74LS156	Fairchild	74LS156	
	ITT	ITT74LS156	
	Motorola	SN74LS156	
	Raytheon	74LS156	
	Signetics	74LS156	
	TI	SN74LS156	
DM74LS157	AMD	SN74LS157	
	Fairchild	74LS157	
	ITT	ITT74LS157	
	Motorola	SN74LS157	
	NEC America	μPB74LS157	
	Raytheon	74LS157	
	Signetics	74LS157	
	TI	SN74LS157	
DM74LS158	AMD	SN74LS158	
	Fairchild	74LS158	
	ITT	ITT74LS158	
	Motorola	SN74LS158	
	Raytheon	74LS158	
	Signetics	74LS158	
	TI	SN74LS158	
DM74LS160	AMD	SN74LS160	
	Fairchild	74LS160	
	ITT	ITT74LS160	
	Motorola	SN74LS160	
	Raytheon	74LS160	
	Signetics	74LS160	
	~~TI~~	~~SN74LS160~~	
DM74LS161	AMD	SN74LS161	
	Fairchild	74LS161	
	ITT	ITT74LS161	
	Motorola	SN74LS161	
	NEC America	μPB74LS161	
	Raytheon	74LS161	
	Signetics	74LS161	
	TI	SN74LS161	
DM74LS162	AMD	SN74LS162	
	Fairchild	74LS162	
	ITT	ITT74LS162	
	Motorola	SN74LS162	
	Raytheon	74LS162	
	Signetics	74LS162	
	TI	SN74LS162	
DM74LS163	AMD	SN74LS163	
	Fairchild	74LS163	
	ITT	ITT74LS163	
	Motorola	SN74LS163	
	Raytheon	74LS163	
	Signetics	74LS163	
	TI	SN74LS163	
DM74LS164	AMD	SN74LS164	
	Fairchild	74LS164	
	ITT	ITT74LS164	
	Motorola	SN74LS164	
	NEC America	μPB74LS164	
	Raytheon	**74LS164**	**272**
	Signetics	74LS164	
	TI	SN74LS164	
DM74LS168	AMD	SN74LS168	
	Fairchild	74LS168	
	TI	SN74LS168	
DM74LS169	AMD	SN74LS169	
	Fairchild	74LS169	
	TI	SN74LS169	
DM74LS170	AMD	SN74LS170	
	Fairchild	74LS170	
	ITT	ITT74LS170	
	Motorola	SN74LS170	
	Raytheon	74LS170	
	Signetics	74LS170	
	TI	SN74LS170	
DM74LS173	Fairchild	74LS173	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
DM74LS173	Signetics	74LS173	
	TI	SN74LS173	
DM74LS174	AMD	SN74LS174	
	Fairchild	74LS174	
	ITT	ITT74LS174	
	Motorola	SN74LS174	
	Raytheon	74LS174	
	Signetics	74LS174	
	TI	SN74LS174	
DM74LS175	AMD	SN74LS175	
	Fairchild	74LS175	
	ITT	ITT74LS175	
	Motorola	SN74LS175	
	NEC America	μPB74LS175	
	Raytheon	74LS175	
	Signetics	74LS175	
	TI	SN74LS175	
DM74LS190	AMD	SN74LS190	
	Fairchild	74LS190	
	ITT	ITT74LS190	
	Motorola	SN74LS190	
	Raytheon	74LS190	
	Signetics	74LS190	
	TI	SN74LS190	
DM74LS191	AMD	SN74LS191	
	Fairchild	74LS191	
	ITT	ITT74LS191	
	Motorola	SN74LS191	
	Raytheon	74LS191	
	Signetics	74LS191	
	TI	SN74LS191	
DM74LS192	AMD	SN74LS192	
	Fairchild	74LS192	
	ITT	ITT74LS192	
	Motorola	SN74LS192	
	NEC America	μPB74LS192	
	Raytheon	74LS192	
	Signetics	74LS192	
	TI	SN74LS192	
DM74LS193	AMD	SN74LS193	
	Fairchild	74LS193	
	ITT	ITT74LS193	
	Motorola	SN74LS193	
	NEC America	μPB74LS193	
	Raytheon	74LS193	
	Signetics	74LS193	
	TI	SN74LS193	
DM74LS196	Fairchild	74LS196	
	ITT	ITT74LS196	
	Motorola	SN74LS196	
	Raytheon	74LS196	
	Signetics	74LS196	
	TI	SN74LS196	
DM74LS197	Fairchild	74LS197	
	ITT	ITT74LS197	
	Motorola	SN74LS197	
	Raytheon	74LS197	
	Signetics	74LS197	
	TI	SN74LS197	
DM74LS20	Fairchild	74LS20	
	ITT	ITT74LS20	
	Motorola	SN74LS20	
	NEC America	μPB74LS20	
	Raytheon	74LS20	
	Signetics	74LS20	
	TI	SN74LS20	
DM74LS21	Fairchild	74LS21	
	ITT	ITT74LS21	
	Motorola	SN74LS21	
	NEC America	μPB74LS21	
	Raytheon	74LS21	
	Signetics	74LS21	
	TI	SN74LS21	
DM74LS22	Fairchild	74LS22	
	ITT	ITT74LS22	
	Motorola	SN74LS22	
	Raytheon	74LS22	
	Signetics	74LS22	
	TI	SN74LS22	
DM74LS221	Fairchild	74LS221	
	ITT	ITT74LS221	
	Motorola	SN74LS221	
DM74LS221	**Raytheon**	**74LS221**	**275**
	Signetics	74LS221	
	TI	SN74LS221	
DM74LS247	Fairchild	74LS247	
	TI	SN74LS247	
DM74LS248	Fairchild	74LS248	
	TI	SN74LS248	
DM74LS249	Fairchild	74LS249	
	TI	SN74LS249	
DM74LS251	AMD	SN74LS251	
	Fairchild	74LS251	
	ITT	ITT74LS251	
	Motorola	SN74LS251	
	NEC America	μPB74LS251	
	Raytheon	74LS251	
	Signetics	74LS251	
	TI	SN74LS251	
DM74LS253	AMD	SN74LS253	
	Fairchild	74LS253	
	ITT	ITT74LS253	
	Motorola	SN74LS253	
	NEC America	μPB74LS253	
	Raytheon	74LS253	
	Signetics	74LS253	
	TI	SN74LS253	
DM74LS257	AMD	SN74LS257	
	Fairchild	74LS257	
	ITT	ITT74LS257	
	Motorola	SN74LS257	
	NEC America	μPB74LS257	
	Raytheon	74LS257	
	Signetics	74LS257	
	TI	SN74LS257	
DM74LS258	AMD	SN74LS258	
	Fairchild	74LS258	
	ITT	ITT74LS258	
	Motorola	SN74LS258	
	NEC America	μPB74LS258	
	Raytheon	**74LS258**	
	Signetics	74LS258	
	TI	SN74LS258	
DM74LS26	Fairchild	74LS26	
	Raytheon	74LS26	
	Signetics	74LS26	
	TI	SN74LS26	
DM74LS27	Fairchild	74LS27	
	ITT	ITT74LS27	
	Motorola	SN74LS27	
	NEC America	μPB74LS27	
	Raytheon	74LS27	
	Signetics	74LS27	
	TI	SN74LS27	
DM74LS279	Fairchild	74LS279	
	ITT	ITT74LS279	
	Motorola	SN74LS279	
	NEC America	μPB74LS279	
	Raytheon	74LS279	
	Signetics	74LS279	
	TI	SN74LS279	
DM74LS283	Fairchild	74LS283	
	ITT	ITT74LS283	
	Motorola	SN74LS283	
	Raytheon	74LS283	
	Signetics	74LS283	
	TI	SN74LS283	
DM74LS290	Fairchild	74LS290	
	ITT	ITT74LS290	
	Motorola	SN74LS290	
	Signetics	74LS290	
	TI	SN74LS290	
DM74LS293	Fairchild	74LS293	
	ITT	ITT74LS293	
	Motorola	SN74LS293	
	Signetics	74LS293	
	TI	SN74LS293	
DM74LS30	Fairchild	74LS30	
	ITT	ITT74LS30	
	Motorola	SN74LS30	
	NEC America	μPB74LS30	
	Raytheon	74LS30	
	Signetics	74LS30	
	TI	SN74LS30	
DM74LS32	Fairchild	74LS32	
	ITT	ITT74LS32	
	Motorola	SN74LS32	
	NEC America	μPB74LS32	
DM74LS32	Raytheon	74LS32	
	Signetics	74LS32	
	TI	SN74LS32	
DM74LS352	Fairchild	74LS352	
	TI	SN74LS352	
DM74LS353	Fairchild	74LS353	
	TI	SN74LS353	
DM74LS365	Fairchild	74LS365	
	ITT	ITT74LS365	
	Motorola	SN74LS365	
	NEC America	μPB74LS365	
	Raytheon	**74LS365**	**286**
	Signetics	74LS365	
	TI	SN74LS365	
DM74LS366	Fairchild	74LS366	
	ITT	ITT74LS366	
	Motorola	SN74LS366	
	NEC America	μPB74LS366	
	Raytheon	**74LS366**	**286**
	Signetics	74LS366	
	TI	SN74LS366	
DM74LS367	Fairchild	74LS367	
	ITT	ITT74LS367	
	Motorola	SN74LS367	
	NEC America	μPB74LS367	
	Raytheon	**74LS367**	**286**
	Signetics	74LS367	
	TI	SN74LS367	
DM74LS368	Fairchild	74LS368	
	ITT	ITT74LS368	
	Motorola	SN74LS368	
	NEC America	μPB74LS368	
	Raytheon	**74LS368**	**286**
	Signetics	74LS368	
	TI	SN74LS368	
DM74LS37	Fairchild	74LS37	
	ITT	ITT74LS37	
	Motorola	SN74LS37	
	NEC America	μPB74LS37	
	Raytheon	74LS37	
	Signetics	74LS37	
	TI	SN74LS37	
DM74LS38	Fairchild	74LS38	
	ITT	ITT74LS38	
	Motorola	SN74LS38	
	NEC America	μPB74LS38	
	Raytheon	74LS38	
	Signetics	74LS38	
	TI	SN74LS38	
DM74LS386	Fairchild	74LS386	
	ITT	ITT74LS386	
	Motorola	SN74LS386	
	Raytheon	74LS386	
	Signetics	74LS386	
	TI	SN74LS386	
DM74LS395	Fairchild	74LS395	
	Raytheon	**74LS395**	**291**
	Signetics	74LS395	
	TI	SN74LS395	
DM74LS40	Fairchild	74LS40	
	ITT	ITT74LS40	
	Motorola	SN74LS40	
	NEC America	μPB74LS40	
	Raytheon	74LS40	
	Signetics	74LS40	
	TI	SN74LS40	
DM74LS42	Fairchild	74LS42	
	ITT	ITT74LS42	
	Motorola	SN74LS42	
	NEC America	μPB74LS42	
	Raytheon	**74LS42**	**266**
	Signetics	74LS42	
	TI	SN74LS42	
DM74LS51	Fairchild	74LS51	
	ITT	ITT74LS51	
	Motorola	SN74LS51	
	NEC America	μPB74LS51	
	Raytheon	74LS51	
	Signetics	74LS51	
	TI	SN74LS51	
DM74LS54	Fairchild	74LS54	
	ITT	ITT74LS54	
	Motorola	SN74LS54	
	NEC America	μPB74LS54	
	Raytheon	74LS54	
	Signetics	74LS54	
DM74LS54	TI	SN74LS54	
DM74LS55	Fairchild	74LS55	
	Motorola	SN74LS55	
	NEC America	μPB74LS55	
	Raytheon	74LS55	
	Signetics	74LS55	
	TI	SN74LS55	
DM74LS670	AMD	SN74LS670	
	Fairchild	74LS670	
	Motorola	SN74LS670	
	Raytheon	74LS670	
	Signetics	74LS670	
	TI	SN74LS670	
DM74LS73	Fairchild	74LS73	
	ITT	ITT74LS73	
	Motorola	SN74LS73	
	Raytheon	74LS73	
	Signetics	74LS73	
	TI	SN74LS73	
DM74LS74	Fairchild	74LS74	
	ITT	ITT74LS74	
	Motorola	SN74LS74	
	NEC America	μPB74LS74	
	Raytheon	74LS74	
	Signetics	74LS74	
	TI	SN74LS74	
DM74LS75	Fairchild	74LS75	
	ITT	ITT74LS75	
	Raytheon	74LS75	
	Signetics	74LS75	
	TI	SN74LS75	
DM74LS76	ITT	ITT74LS76	
	Raytheon	74LS76	
	Signetics	74LS76	
	TI	SN74LS76	
DM74LS77	Fairchild	74LS77	
	Raytheon	54LS77	
DM74LS78	ITT	ITT74LS78	
	Raytheon	**74LS78**	
	Signetics	74LS78	
	TI	SN74LS78	
DM74LS83A	Fairchild	74LS83	
	ITT	ITT74LS83A	
	Motorola	SN74LS83	
	Raytheon	74LS83A	
	Signetics	74LS83	
	TI	SN74LS83A	
DM74LS85	Fairchild	74LS85	
	ITT	ITT74LS85	
	Motorola	SN74LS85	
	Raytheon	74LS85	
	Signetics	74LS85	
	TI	SN74LS85	
DM74LS93	Fairchild	74LS93	
	ITT	ITT74LS93	
	Motorola	SN74LS93	
	Raytheon	**74LS93**	**268**
	Signetics	74LS93	
	TI	SN74LS93	
DM74L187	Intersil	IM5603	
DM74L63	TI	SN54L193	
DM74L89	MMI	L6560	
DM74S00	Fairchild	74S00	
	Hitachi	HD74S00	
	Mitsubishi	M5S000	
	Signetics	74S00	
	TI	SN74S00	
DM74S02	Fairchild	74S02	
	Signetics	74S02	
	TI	SN74S32	
DM74S03	Fairchild	74S03	
	Hitachi	HD74S03	
	Mitsubishi	M5S003	
	Signetics	74S03	
	TI	SN74S03	
DM74S04	Fairchild	74S04	
	Hitachi	HD74S04	
	Mitsubishi	M5S004	
	Signetics	74S04	
	TI	SN74S04	
DM74S05	Fairchild	74S05	
	Hitachi	HD74S05	
	Mitsubishi	M5S005	
	Signetics	74S05	
	TI	SN74S05	
DM74S10	Fairchild	74S10	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
DM74S10	Hitachi	HD74S10	
	Mitsubishi	M5S010	
	Signetics	74S10	
	TI	SN74S10	
DM74S11	Fairchild	74S11	
	Hitachi	HD74S11	
	Mitsubishi	M5S011	
	Signetics	74S11	
	TI	SN74S11	
DM74S112	Fairchild	74S112	
	Hitachi	HD74S112	
	Mitsubishi	M5S112	
	Motorola	SN74S112	
	Signetics	74S112	
	TI	SN74S112	
DM74S113	Fairchild	74S113	
	Hitachi	HD74S113	
	Mitsubishi	M5S113	
	Motorola	SN74S113	
	Signetics	74S113	
	TI	SN74S113	
DM74S114	Fairchild	74S114	
	Hitachi	HD74S114	
	Mitsubishi	M5S114	
	Signetics	74S114	
	TI	SN74S114	
DM74S133	Fairchild	74S133	
	Hitachi	HD74S133	
	Mitsubishi	M5S133	
	Signetics	74S133	
	TI	SN74S133	
DM74S134	Fairchild	74S134	
	Hitachi	HD74S134	
	Signetics	74S134	
	TI	SN74S134	
DM74S135	Fairchild	74S135	
	Hitachi	HD74S135	
	Signetics	74S135	
	TI	SN74S135	
DM74S138	AMD	SN74S138	
	Fairchild	74S138	
	Mitsubishi	M5S138	
	Signetics	74S138	
	TI	SN74S138	
DM74S139	AMD	SN74S139	
	Fairchild	74S139	
	Signetics	74S139	
	TI	SN74S139	
DM74S140	Fairchild	74S140	
	Hitachi	HD74S140	
	Signetics	74S140	
	TI	SN74S140	
DM74S15	Fairchild	74S15	
	Hitachi	HD74S15	
	Mitsubishi	M5S015	
	Signetics	74S15	
	TI	SN74S15	
DM74S151	AMD	SN74S151	
	Fairchild	74S151	
	Hitachi	HD74S151	
	Mitsubishi	M5S151	
	Signetics	74S151	
	TI	SN74S151	
DM74S153	AMD	SN74S153	
	Fairchild	74S153	
	Mitsubishi	M5S153	
	Signetics	74S153	
	TI	SN74S153	
DM74S157	AMD	SN74S157	
	Fairchild	74S157	
	Mitsubishi	M5S157	
	Signetics	74S157	
	TI	SN74S157	
DM74S158	AMD	SN74S158	
	Fairchild	74S158	
	Mitsubishi	M5S158	
	Signetics	74S158	
	TI	SN74S158	
DM74S174	AMD	SN74S174	
	Fairchild	74S174	
	Hitachi	HD74S174	
	Mitsubishi	M5S174	
DM74S174	Signetics	74S174	
	TI	SN74S174	
DM74S175	AMD	SN74S175	
	Fairchild	74S175	
	Hitachi	HD74S175	
	Mitsubishi	M5S175	
	Signetics	74S175	
	TI	SN74S175	
DM74S182	Fairchild	74S182	
	Mitsubishi	M5S182	
	Signetics	74S182	
	TI	SN74S182	
DM74S195	AMD	SN74S195	
	Fairchild	74S195	
	Signetics	74S195	
	TI	SN74S195	
DM74S20	Fairchild	74S20	
	Hitachi	HD74S20	
	Mitsubishi	M5S020	
	Signetics	74S20	
	TI	SN74S20	
DM74S200	Signetics	74S200	
DM74S22	Fairchild	74S22	
	Hitachi	HD74S22	
	Mitsubishi	M5S22	
	Signetics	74S22	
	TI	SN74S22	
DM74S251	AMD	SN74S251	
	Fairchild	74S251	
	Hitachi	HD74S251	
	Mitsubishi	M5S251	
	Signetics	74S251	
	TI	SN74S251	
DM74S253	AMD	SN74S253	
	Fairchild	74S253	
	Signetics	74S253	
DM74S257	AMD	SN74S257	
	Fairchild	74S257	
	Mitsubishi	M5S257	
	Signetics	74S257	
	TI	SN74S257	
DM74S280	Signetics	74S280	
	TI	SN74S280	
DM74S281	TI	SN74S281	
DM74S30	Fairchild	74S30	
	Mitsubishi	M5S030	
	TI	SN74S30	
DM74S387	Intel	3601-1	
	MMI	**6300**	**1252**
	NEC Micro	**μPB403**	**1462**
	Signetics	N82S126	
	TI	SN74S387	
DM74S40	Fairchild	74S40	
	Hitachi	HD74S40	
	Mitsubishi	M5S040	
	Signetics	74S40	
	TI	SN74S40	
DM74S51	Fairchild	74S51	
	Mitsubishi	M5S051	
	Signetics	74S51	
	TI	SN74S51	
DM74S572	Intel	3605	
	NEC Micro	**μPB406**	**1470**
DM74S573	Intel	3625	
	NEC Micro	**μPB426**	**1470**
DM74S64	Fairchild	74S64	
	Hitachi	HD74S64	
	Signetics	74S64	
	TI	SN74S64	
DM74S65	Fairchild	74S65	
	Hitachi	HD74S65	
	Signetics	74S65	
	TI	SN74S65	
DM74S86	Fairchild	74S86	
	Hitachi	HD74S86	
	Signetics	74S86	
	TI	SN74S86	
DM7400	Fairchild	7400	
		9N00	
	Hitachi	HD2503	
		HD7400	
	ITT	ITT7400	
	Mitsubishi	M53200	
	Motorola	MC7400	
	NEC America	μPB7400	
	Raytheon	7400	
DM7400	Signetics	7400	
	TI	SN7400	
	Toshiba	TC7400	
	TRW	7400	
DM7401	Fairchild	7401	
	Hitachi	HD2509	
	ITT	ITT7401	
	Mitsubishi	M53201	
	Motorola	MC7401	
	Raytheon	7401	
	Signetics	7401	
	TI	SN7401	
	TRW	7401	
DM7402	Fairchild	7402	
	Hitachi	HD2511	
		HD7402	
	ITT	ITT7402	
	Mitsubishi	M53202	
	Motorola	MC7402	
	NEC America	μPB7402	
	Signetics	7402	
	TI	SN7402	
	TRW	7402	
DM7403	Fairchild	7403	
	Hitachi	HD2528	
		HD7403	
	ITT	ITT7403	
	Mitsubishi	M53203	
	Motorola	MC7403	
	Raytheon	7403	
	Signetics	7403	
	TI	SN7403	
	TRW	7403	
DM7404	Fairchild	7404	
	Hitachi	HD2522	
		HD7404	
	ITT	ITT7404	
	Mitsubishi	M53204	
	Motorola	MC7404	
	NEC America	μPB7404	
	Raytheon	7404	
	Signetics	7404	
	TI	SN7404	
	Toshiba	TC7404	
	TRW	7404	
DM7405	Fairchild	7405	
	Hitachi	HD2523	
		HD7405	
	ITT	ITT7405	
	Mitsubishi	M53205	
	Motorola	MC7405	
	NEC America	μPB7405	
	Raytheon	7405	
	Signetics	7405	
	TI	SN7405	
	TRW	7405	
DM7406	Fairchild	7406	
	Hitachi	HD7406	
	ITT	ITT7406	
	Mitsubishi	M53206	
	Motorola	MC7406	
	Signetics	7406	
	TI	SN7406	
	TRW	7406	
DM7407	Fairchild	7407	
	Hitachi	HD7407	
	ITT	ITT7407	
	Mitsubishi	M53207	
	Motorola	MC7407	
	Signetics	7407	
	TI	SN7407	
	TRW	7407	
DM7408	Fairchild	7408	
	Hitachi	HD2550	
	ITT	ITT7408	
	Mitsubishi	M53208	
	Motorola	MC7408	
	Raytheon	7408	
	Signetics	7408	
	TI	SN7408	
	Toshiba	TC7408	
	TRW	7408	
DM7409	Fairchild	7409	
	Hitachi	HD2551	
		HD7409	
	ITT	ITT7409	
DM7409	Mitsubishi	M53209	
	Motorola	MC7409	
	Raytheon	7409	
	Signetics	7409	
	TI	SN7409	
	TRW	7409	
DM7410	Fairchild	7410	
	Hitachi	HD2507	
		HD7410	
	ITT	ITT7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
	NEC America	μPB7410	
	Raytheon	7410	
	Signetics	7410	
	TI	SN7410	
		SN7427	
	Toshiba	TC7410	
	TRW	7410	
DM74107	Fairchild	74107	
	Hitachi	HD2530	
		HD74107	
	ITT	ITT74107	
	Mitsubishi	M53307	
	Motorola	MC74107	
	NEC America	μPB74107	
	Signetics	74107	
	TI	SN74107	
DM74109	Fairchild	74109	
	Signetics	74109	
	TI	SN74109	
DM7411	Fairchild	7411	
	Hitachi	HD7411	
	ITT	ITT7411	
	Raytheon	7411	
	Signetics	7411	
♦DM7412	Raytheon	7412	
DM74121	Fairchild	74121	
	Hitachi	HD74121	
	ITT	ITT74121	
	Mitsubishi	M53321	
	Motorola	MC74121	
	Signetics	74121	
	TI	SN74121	
	TRW	74121	
DM74123	AMD	SN74123	
	Fairchild	74123	
	ITT	ITT74123	
	Mitsubishi	M53323	
	Motorola	MC74123	
	NEC America	μPB74123	
	Raytheon	74123	
	Signetics	74123	
	TI	SN74123	
	TRW	74123	
DM74125	Fairchild	74125	
	Hitachi	HD74125	
	Mitsubishi	M53325	
	Signetics	74125	
	TI	SN74125	
		SN74425	
DM74126	Fairchild	74126	
	Hitachi	HD74126	
	Mitsubishi	M53326	
	Signetics	74126	
	TI	SN74126	
		SN74426	
DM7413	Fairchild	7413	
	ITT	ITT7413	
	Mitsubishi	M53213	
	Motorola	MC7413	
	NEC America	μPB7413	
	Signetics	7413	
	TI	SN7413	
	TRW	7413	
DM74132	Fairchild	74132	
	Hitachi	HD74132	
	Mitsubishi	M53332	
	Motorola	MC74132	
	Signetics	74132	
	TI	SN74132	
♦DM74136	Raytheon	74136	
DM7414	Fairchild	7414	
	Hitachi	HD7414	
	Mitsubishi	M53214	
	Motorola	MC7414	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Replacement Device	IC Master Page
DM7414	Signetics	7414	
	TI	SN7414	
DM74141	Fairchild	74141	
	Motorola	MC74141	
	NEC America	μPB74141	
	Signetics	74141	
	TI	SN74141	
DM74145	Fairchild	74145	
	ITT	ITT74145	
	Mitsubishi	M53345	
	Motorola	MC74145	
	Raytheon	74145	
	Signetics	74145	
	TI	SN74145	
	TRW	74145	
DM74147	Hitachi	HD74147	
	Mitsubishi	M53347	
	NEC America	μPB74147	
	Signetics	74147	
	TI	SN74147	
DM74148	Hitachi	HD74148	
	Mitsubishi	M53348	
	NEC America	μPB74148	
	Signetics	74148	
	TI	SN74148	
♦DM7415	Raytheon	7415	
DM74150	Fairchild	74150	
	Hitachi	HD74150	
	Mitsubishi	M53350	
	Motorola	MC74150	
	NEC America	μPB74150	
	Raytheon	74150	
	Signetics	74150	
	TI	SN74150	
	TRW	74150	
DM74151	Fairchild	74151	
	Hitachi	HD74151	
	ITT	ITT74151	
	Mitsubishi	M53351	
	Motorola	MC74151	
	NEC America	μPB74151	
	Raytheon	74151	
	Signetics	74151	
	TI	SN74151	
		SN74151A	
	TRW	74151	
♦DM74152	Raytheon	74152	
DM74153	AMD	SN74153	
	Fairchild	74153	
	Hitachi	HD2564	
	ITT	ITT74153	
	Mitsubishi	M53353	
	Motorola	MC74153	
	NEC America	μPB74153	
	Raytheon	74153	
	Signetics	74153	
	TI	SN74153	
	TRW	74153	
DM74154	AMD	SN74154	
	Fairchild	74154	
	Hitachi	HD2580	
	Mitsubishi	M53354	
	Motorola	MC74154	
	NEC America	μPB74154	
	Raytheon	74154	
	Signetics	74154	
	TI	SN74154	
	TRW	74154	
DM74155	Fairchild	74155	
	ITT	ITT74155	
	Mitsubishi	M53355	
	Motorola	MC74155	
	NEC America	μPB74155	
	Raytheon	74155	
	Signetics	74155	
	TI	SN74155	
	TRW	74155	
DM74156	Fairchild	74156	
	Hitachi	HD74156	
	ITT	ITT74156	
	Mitsubishi	M53356	
	Motorola	MC74156	
DM74156	NEC America	μPB74156	
	Raytheon	74156	
	Signetics	74156	
	TI	SN74156	
	TRW	74156	
DM74157	AMD	SN74157	
	Fairchild	74157	
	Hitachi	HD74157	
	ITT	ITT74157	
	Mitsubishi	M53357	
	Motorola	MC74157	
	NEC America	μPB74157	
	Raytheon	74157	
	Signetics	74157	
	TI	SN74157	
♦DM74158	Raytheon	74158	
♦DM74159	Raytheon	74159	
DM7416	Fairchild	7416	
	Hitachi	HD7416	
	ITT	ITT7416	
	Mitsubishi	M53216	
	Motorola	MC7416	
	Signetics	7416	
	TI	SN7416	
	TRW	7416	
DM74160	AMD	SN74160	
	Fairchild	74160	
	Hitachi	HD74160	
	ITT	ITT74160	
	Mitsubishi	M53360	
	Motorola	MC74160	
	Raytheon	74160	
	Signetics	74160	
	TI	SN74160	
	TRW	74160	
DM74161	AMD	SN74161	
	Fairchild	74161	
	Hitachi	HD74161	
	ITT	ITT74161	
	Mitsubishi	M53361	
	Motorola	MC74161	
	NEC America	μPB74161	
	Raytheon	74161	
	Signetics	74161	
	TI	SN74161	
	TRW	74161	
DM74162	AMD	SN74162	
	Fairchild	74162	
	Hitachi	HD74162	
	ITT	ITT74162	
	Mitsubishi	M53362	
	Motorola	MC74162	
	Raytheon	74162	
	Signetics	74162	
	TI	SN74162	
	TRW	74162	
DM74163	AMD	SN74163	
	Fairchild	74163	
	Hitachi	HD74163	
	ITT	ITT74163	
	Mitsubishi	M53363	
	Motorola	MC74163	
	Raytheon	74163	
	Signetics	74163	
	TI	SN74163	
	TRW	74163	
DM74164	AMD	SN74164	
		74164	
	Fairchild	74164	
	Hitachi	HD74164	
	ITT	ITT74164	
	Mitsubishi	M53364	
	NEC America	μPB74164	
	Raytheon	74164	
	Signetics	74164	
	TI	SN74164	
DM74165	Fairchild	74165	
	Mitsubishi	M53365	
	Motorola	MC74165	
	Raytheon	74165	
	Signetics	74165	
	TI	SN74165	
DM74166	Fairchild	74166	
	Hitachi	HD74166	
	Mitsubishi	M53366	
	Raytheon	74166	
DM74166	Signetics	74166	
	TI	SN74166	
DM7417	Fairchild	7417	
	Hitachi	HD7417	
	ITT	ITT7417	
	Mitsubishi	M53217	
	Motorola	MC7417	
	Signetics	7417	
	TI	SN7417	
	TRW	7417	
DM74170	Fairchild	74170	
	Hitachi	HD2540	
	Mitsubishi	M53370	
	NEC America	μPB74170	
	Raytheon	74170	
	Signetics	74170	
	TI	SN74170	
DM74172	Signetics	74S172	
		74172	
	TI	SN74172	
DM74173	Fairchild	74173	
	TI	SN74173	
DM74174	AMD	SN74174	
	Fairchild	74174	
	Hitachi	HD74174	
	Mitsubishi	M53374	
	Motorola	MC74174	
	Raytheon	74174	
	Signetics	74174	
	TI	SN74174	
DM74175	AMD	SN74175	
	Fairchild	74175	
	Hitachi	HD74175	
	Mitsubishi	M53375	
	Motorola	MC74175	
	NEC America	μPB74175	
	Raytheon	74175	
	Signetics	74175	
	TI	SN74175	
DM74176	Fairchild	74176	
	Mitsubishi	M53376	
	Motorola	MC74176	
	Signetics	74176	
	TI	SN74176	
DM74177	Fairchild	74177	
	Mitsubishi	M53377	
	Motorola	MC74177	
	Signetics	74177	
	TI	SN74177	
DM74180	Fairchild	74180	
	Hitachi	HD74180	
	ITT	ITT74180	
	Mitsubishi	M53380	
	Motorola	MC74180	
	NEC America	μPB74180	
	Raytheon	74180	
	Signetics	74180	
	TI	SN74180	
	TRW	74180	
DM74181	AMD	SN74181	
	Fairchild	74181	
	Mitsubishi	M53381	
	Motorola	MC74181	
	NEC America	μPB74181	
	Raytheon	74181	
	Signetics	74181	
	TI	SN74181	
DM74182	AMD	SN74182	
	Fairchild	74182	
	ITT	ITT74182	
	Mitsubishi	M53382	
	Motorola	MC74182	
	NEC America	μPB74182	
	Raytheon	74182	
	Signetics	74182	
	TI	SN74182	
DM74184	TI	SN74184	
DM74185	Mitsubishi	M53385	
	TI	SN74185	
♦DM74187	Intersil	IM5603	
	MMI	**6200**	**1252**
	National	DM74S187	
	Signetics	N82S226	
	TI	SN74187	
DM74190	Fairchild	74190	
	Hitachi	HD74190	
DM74190	ITT	ITT74190	
	Mitsubishi	M53390	
	Motorola	MC74190	
	Raytheon	74190	
	Signetics	74190	
	TI	SN74190	
DM74191	Fairchild	74191	
	Hitachi	HD74191	
	ITT	ITT74191	
	Mitsubishi	M53391	
	Motorola	MC74191	
	Raytheon	74191	
	Signetics	74191	
	TI	SN74191	
DM74192	AMD	SN74192	
	Fairchild	74192	
	ITT	ITT74192	
	Mitsubishi	M53392	
	Motorola	MC74192	
	NEC America	μPB74192	
	Raytheon	74192	
	Signetics	74192	
	TI	SN74192	
DM74193	AMD	SN74193	
	Fairchild	74193	
	ITT	ITT74193	
	Mitsubishi	M53393	
	Motorola	MC74193	
	NEC America	μPB74193	
	Raytheon	74193	
	Signetics	74193	
	TI	SN74193	
DM74194	AMD	SN74194	
	Fairchild	74194	
	Hitachi	HD74194	
	ITT	ITT74194	
	Motorola	MC74194	
	Raytheon	74194	
	Signetics	74194	
	TI	SN74194	
DM74195	AMD	SN74195	
	Fairchild	74195	
	ITT	ITT74195	
	Motorola	MC74195	
	NEC America	μPB74195	
	Raytheon	74195	
	Signetics	74195	
	TI	SN74195	
DM74196	Fairchild	74196	
	Motorola	MC74196	
	Signetics	74196	
	TI	SN74196	
DM74197	Fairchild	74197	
	Motorola	MC74197	
	Signetics	74197	
	TI	SN74197	
DM74198	Fairchild	74198	
	Hitachi	HD74198	
	Mitsubishi	M53398	
	NEC America	μPB74198	
	Raytheon	74198	
	Signetics	74198	
	TI	SN74198	
DM74199	Fairchild	74199	
	Mitsubishi	M53399	
	Raytheon	74199	
	Signetics	74199	
	TI	SN74199	
DM7420	Fairchild	7420	
	Hitachi	HD2504	
		HD7420	
	ITT	ITT7420	
	Mitsubishi	M53220	
	Motorola	MC7420	
	NEC America	μPB7420	
	Raytheon	7420	
	Signetics	7420	
	TI	SN7420	
	Toshiba	TC7420	
	TRW	7420	
♦DM74200	Fairchild	93421	
	MMI	6531	
	Raytheon	RC5340	
	TI	SN74S201	
♦DM7421	Raytheon	7421	
♦DM7422	Raytheon	7422	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
DM7423	Fairchild	7423	
	Motorola	MC7423	
	TI	SN7423	
DM7425	Fairchild	7425	
	ITT	ITT7425	
	Mitsubishi	M53225	
	Motorola	MC7425	
	TI	SN7425	
DM74251	TI	SN74251	
DM7426	Fairchild	7426	
	Hitachi	HD7426	
	ITT	ITT7426	
	Motorola	MC7426	
	Signetics	7426	
	TI	SN7426	
	TRW	7426	
DM7427	Fairchild	7427	
	Hitachi	HD7427	
	Mitsubishi	M53227	
	Motorola	MC7427	
	Signetics	7427	
♦DM74283	Raytheon	74283	
DM74287	Intel	3621-1	
DM7430	Fairchild	7430	
	Hitachi	HD2508	
		HD7430	
	ITT	ITT7430	
	Mitsubishi	M53230	
	Motorola	MC7430	
	NEC America	μPB7430	
	Signetics	7430	
	TI	SN7430	
	TRW	7430	
DM7432	Fairchild	7432	
	Hitachi	HD7432	
	ITT	ITT7432	
	Signetics	7432	
	TI	SN7432	
DM7437	Fairchild	7437	
	ITT	ITT7437	
	Mitsubishi	M53237	
	Motorola	MC7437	
	NEC America	μPB7437	
	Raytheon	7437	
	Signetics	7437	
	TI	SN7437	
	TRW	7437	
DM7438	Fairchild	7438	
	ITT	ITT7438	
	Mitsubishi	M53238	
	Motorola	MC7438	
	NEC America	μPB7438	
	Raytheon	7438	
	Signetics	7438	
	TI	SN7438	
	TRW	7438	
DM7440	Fairchild	7440	
	Hitachi	HD2501	
		HD7440	
	ITT	ITT7440	
	Mitsubishi	M53240	
	Motorola	MC7440	
	NEC America	μPB7440	
	Signetics	7440	
	TI	SN7440	
	TRW	7440	
DM7441	Fairchild	7441	
	Hitachi	HD2518	
	Mitsubishi	M53241	
	Signetics	7441	
	TI	SN74141	
DM7442	Fairchild	7442	
	Hitachi	HD2536	
		HD7442	
	ITT	ITT7442	
	Mitsubishi	M53242	
	Motorola	MC7442	
	NEC America	μPB7442	
	Raytheon	7442	
	Signetics	7442	
	TI	SN7442	
		SN7442A	
♦DM7443	Raytheon	7443	
♦DM7444	Raytheon	7444	
DM7445	Fairchild	7445	
	ITT	ITT7445	
	Mitsubishi	M53245	
	Motorola	MC7445	
	NEC America	μPB7445	
	Raytheon	7445	
	Signetics	7445	
	TI	SN7445	
	TRW	7445	
DM7446	Fairchild	7446	
	Hitachi	HD2553	
	ITT	ITT7446	
	Motorola	MC7446	
	Signetics	7446	
	TI	SN7446	
		SN7446A	
DM7447	Fairchild	7447	
	Hitachi	HD2532	
	ITT	ITT7447	
	Mitsubishi	M53247	
	Motorola	MC7447	
	NEC America	μPB7447	
	Signetics	7447	
	TI	SN7447	
		SN7447A	
DM7448	Fairchild	7448	
	ITT	ITT7448	
	Mitsubishi	M53248	
	Motorola	MC7448	
	Signetics	7448	
	TI	SN7448	
DM7450	Fairchild	7450	
	Hitachi	HD2506	
		HD7450	
	ITT	ITT7450	
	Mitsubishi	M53250	
	Motorola	MC7450	
	NEC America	μPB7450	
	Signetics	7450	
	TI	SN7450	
	TRW	7450	
DM7451	Fairchild	7451	
	Hitachi	HD2505	
		HD7451	
	ITT	ITT7451	
	Motorola	MC7451	
	NEC America	μPB7451	
	Signetics	7451	
	TI	SN7451	
	TRW	7451	
DM7453	Fairchild	7453	
	Hitachi	HD2512	
		HD7453	
	ITT	ITT7453	
	Mitsubishi	M53253	
	Motorola	MC7453	
	NEC America	μPB7453	
	Signetics	7453	
	TI	SN7453	
	TRW	7453	
DM7454	Fairchild	7454	
	Hitachi	HD2514	
		HD7454	
	ITT	ITT7454	
	Motorola	MC7454	
	NEC America	μPB7454	
	Signetics	7454	
	TI	SN7454	
	TRW	7454	
DM7460	Fairchild	7460	
	Hitachi	HD7460	
	Mitsubishi	M53260	
	Motorola	MC7460	
	NEC America	μPB7460	
	Signetics	7460	
	TI	SN7460	
	TRW	7460	
DM7470	Fairchild	7470	
	ITT	ITT7470	
	Mitsubishi	M53270	
	Motorola	MC7470	
	Signetics	7470	
	TI	SN7470	
DM7472	Fairchild	7472	
DM7472	Hitachi	HD2529	
		HD7472	
	ITT	ITT7472	
	Mitsubishi	M53272	
	Motorola	MC7472	
	Signetics	7472	
	TI	SN7472	
	TRW	7472	
DM7473	Fairchild	7473	
	Hitachi	HD2515	
	ITT	ITT7473	
	Mitsubishi	M53273	
	Motorola	MC7473	
	NEC America	μPB7473	
	Signetics	7473	
	TI	SN7473	
DM7474	Fairchild	7474	
	Hitachi	HD2510	
		HD7474	
	ITT	ITT7474	
	Mitsubishi	M53274	
	Motorola	MC7474	
	NEC America	μPB7474	
	Raytheon	7474	
	Signetics	7474	
	TI	SN7474	
	TRW	7474	
DM7475	Fairchild	7475	
	Hitachi	HD2517	
		HD7475	
	ITT	ITT7475	
	Mitsubishi	M53275	
	Motorola	MC7475	
	Signetics	7475	
	TI	SN7475	
	TRW	7475	
DM7476	Fairchild	7476	
	Hitachi	HD2516	
	ITT	ITT7476	
	Mitsubishi	M53276	
	Motorola	MC7476	
	NEC America	μPB7476	
	Signetics	7476	
	TI	SN7476	
	TRW	7476	
DM7483	Fairchild	7483	
	Hitachi	HD2535	
	ITT	ITT7483	
	Mitsubishi	M53283	
	Motorola	MC7483	
	Raytheon	7483	
	Signetics	7483	
	TI	SN7483	
		SN7483A	
DM7485	Fairchild	7485	
	Hitachi	HD7485	
	Mitsubishi	M53285	
	Motorola	MC7485	
	NEC America	μPB7485	
	Signetics	7485	
	TI	SN7485	
	TRW	7485	
DM7486	Fairchild	7486	
	Hitachi	HD2526	
		HD7486	
	ITT	ITT7486	
	Mitsubishi	M53286	
	Motorola	MC7486	
	NEC America	μPB7486	
	Raytheon	7486	
	Signetics	7486	
	TI	SN7486	
	TRW	7486	
DM7488	Intersil	IM5600	
	MMI	6230	1252
	TI	SN7488	
		SN7488A	
DM7489	AMD	C3101	
		SN7489	
	Fairchild	7489	
	Mitsubishi	M53289	
	MMI	6560	
	NEC Micro	μPB2089	
	Raytheon	7489	
	TI	SN7489	
	TRW	7489	
DM7490	Fairchild	7490	
	Hitachi	HD2519	
		HD7490	
	ITT	ITT7490	
	Mitsubishi	M53290	
	Motorola	MC7490	
	Signetics	7490	
	TI	SN7490	
		SN7490A	
	TRW	7490	
DM7491	Fairchild	7491	
	ITT	ITT7491	
	Mitsubishi	M53291	
	Motorola	MC7491	
	NEC America	μPB7491	
	Signetics	7491	
	TI	SN7491	
		SN7491A	
DM7492	Fairchild	7492	
	Hitachi	HD2521	
		HD7492	
	ITT	ITT7492	
	Mitsubishi	M53292	
	Motorola	MC7492	
	Signetics	7492	
	TI	SN7492	
		SN7492A	
	TRW	7492	
DM7493	Fairchild	7493	
	Hitachi	HD2520	
		HD7493	
	ITT	ITT7493	
	Mitsubishi	M53293	
	Motorola	MC7493	
	Signetics	7493	
	TI	SN7493	
		SN7493A	
	TRW	7493	
DM7495	Fairchild	7495	
	Hitachi	HD2534	
	ITT	ITT7495	
	Mitsubishi	M53295	
	Motorola	MC7495	
	Signetics	7495	
	TI	SN7495	
		SN7495A	
DM7496	Fairchild	7496	
	Hitachi	HD2546	
		HD7496	
	ITT	ITT7496	
	Mitsubishi	M53296	
	Motorola	MC7496	
	Signetics	7496	
	TI	SN7496	
	TRW	7496	
DM75L60	TI	SN54L192	
DM75L63	TI	SN54L193	
DM7535	NEC Micro	μPB403	1462
DM75491	Motorola	MC75491	
	National	DS75491	
DM75492	Motorola	MC75492	
	National	DS75492	
DM7551	TI	SN54173	
DM7560	TI	SN54192	
DM7563	TI	SN54193	
DM7570	TI	SN54164	
♦DM7573	Harris	HPROM1024A	
	Intel	M3601	
	Intersil	IM5603	
	MMI	5300	1248
	National	DM54S387	1264
	TI	SN54S387	
♦DM7574	AMD	AM27S09	
	Harris	HM7602	1192
		HPROM1024	
	Intersil	IM5623	
	MMI	5301	1248
	National	DM54S287	1264
	NEC Micro	μPB403	1462
	TI	SN54S287	
DM7577	Harris	HM7602	1192
	TI	SN54S188	
DM7578	Harris	HM7603	1192
	TI	SN54S288	
♦DM7582	TI	SN54S301	
DM7588	TI	SN54S188	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

National Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
DM7590	TI	SN54165	
DM7596	TI	SN54S473	
♦DM7597	Intersil	IM5623	
	MMI	**5201**	**1252**
	National	DM75S97	
	TI	SN54S287	
		SN54S370	
♦DM7598	Intersil	IM5610	
	MMI	**5231**	**1252**
	National	DM75598	
DM7599	AMD	AM27S03	
		DM7599	
	MMI	5561	
	TI	SN54S189	
DM76L70	TI	SN54L164	
DM76L97	Intersil	IM5623	
♦DM76L99	MMI	L5561	
	National	**DM54S189**	**1292**
♦DM7640	National	DS7640	
DM77S295	NEC Micro	μPB405	
DM77S296	**NEC Micro**	**μPB425**	**1466**
♦DM7795	**National**	**DM77S95**	**1281**
♦DM7796	**MMI**	**5241**	**1252**
	National	**DM77S96**	**1281**
♦DM78XX	National	DS78XX	
DM7800	TI	SN55180	
DM7810	TI	SN5426	
DM7812	TI	SN5416	
♦DM7893	National	DS55493	
♦DM7894	National	DS55494	
DM8093	TI	SN74125	
DM8094	TI	SN74126	
DM8095	TI	SN74365	
DM8096	TI	SN74366	
DM8097	TI	SN74367	
DM8098	TI	SN74368	
♦DM81L22	TI	SN74L157	
♦DM81S60	Fairchild	93S47	
DM8121	TI	SN74251	
DM8123	TI	SN74S257	
DM8200	Signetics	N8269	
♦DM8213	Fairchild	9311	
	Motorola	MC8311	
	Raytheon	RC9311	
	Signetics	74154	
	TI	SN74154	
DM8214	TI	SN74LS253	
DM8220	Hitachi	HD2525	
DM8280	Fairchild	93176	
	Raytheon	RC8280	
	Signetics	N8280	
	TI	SN74176	
DM8281	Fairchild	93177	
	Raytheon	RC8281	
	Signetics	N8281	
	TI	SN74177	
♦DM8283	Fairchild	9383	
	Motorola	MC7483	
	Signetics	7483	
	TI	SN7483A	
DM8288	Signetics	N8288	
DM8290	Fairchild	93196	
	Raytheon	RC8290	
	TI	SN74196	
DM8291	Fairchild	93197	
	Raytheon	RC8291	
	TI	SN74197	
♦DM8296	TI	SN74196	
DM8300	AMD	9300	
	Fairchild	9300	
	Raytheon	RC9300	
	TI	SN29300	
DM8301	AMD	9301	
	TI	SN29301	
DM8309	AMD	9309	
	Fairchild	9309	
	TI	SN29309	
DM8310	AMD	9310	
	Fairchild	9310	
	Raytheon	RC9310	
	TI	SN29310	
DM8311	AMD	9311	
DM8311	Fairchild	9311	
	Raytheon	RC9311	
	TI	SN29311	
DM8312	AMD	9312	
	Fairchild	9312	
	Raytheon	RC9312	
	TI	SN29312	
DM8316	AMD	9316	
	Fairchild	9316	
	Raytheon	RC9316	
	TI	SN29316	
DM8322	AMD	9322	
	Fairchild	9322	
	Raytheon	RC9322	
		74154	
		74157	
	TI	SN29322	
DM85L60	TI	SN74L192	
DM85L63	TI	SN74L193	
DM85S228	**Harris**	**HM7681**	**1220**
DM85S229	**Harris**	**HM7680**	**1220**
♦DM85S99	AMD	SN74S189	
	TI	SN74S189	
♦DM8500	Signetics	7476	
	TI	SN7476	
♦DM8501	Signetics	7473	
	TI	SN7473	
♦DM8510	Signetics	7474	
	TI	SN7474	
♦DM8530	Fairchild	9390	
	Motorola	MC7490	
	Signetics	7490	
	TI	SN7490A	
♦DM8532	Fairchild	9392	
	Motorola	MC7492	
	Signetics	7492	
	TI	SN7492A	
♦DM8533	Fairchild	9393	
	Motorola	MC7493	
	Signetics	7493	
	TI	SN7493A	
♦DM8550	Fairchild	9375	
	Motorola	MC7475	
	Signetics	7475	
	TI	SN7475	
DM8551	TI	SN74173	
DM8560	Fairchild	9360	
	Hitachi	HD2541	
	ITT	ITT74192	
	Motorola	MC74192	
	Raytheon	74192	
	Signetics	74192	
	TI	SN74192	
DM8563	Fairchild	9366	
	Hitachi	HD2542	
	ITT	ITT74193	
	Motorola	MC74193	
	Raytheon	74193	
	Signetics	74193	
	TI	SN74193	
DM8570	Fairchild	93164	
	Motorola	MC74164	
	Raytheon	74164	
	TI	SN74164	
♦DM8573	Fairchild	93416	
	Harris	HPROM1024A	
	Intel	3601	
	Intersil	IM5603	
	MMI	**6300**	**1252**
	National	**DM74S387**	**1264**
	Signetics	N82S126	
	TI	SN74S387	
♦DM8574	Fairchild	93426	
	Harris	HPROM1024	
	Intel	3621	
	Intersil	IM5603	
		IM5623	
	MMI	**6301**	**1252**
	National	**DM74S287**	**1264**
	TI	SN74S287	
DM8577	AMD	AM27S08	
	Harris	**HM7602**	**1192**
	TI	SN74S188	
DM8578	**Harris**	**HM7603**	**1192**
	MMI	**6331**	**1252**
	Signetics	N82S123	
DM8578	TI	SN74S288	
DM8579	TI	SN74164	
♦DM8580	Fairchild	9395	
	Motorola	MC7495	
	Signetics	7495	
	TI	SN7495A	
♦DM8582	Fairchild	93411	
	MMI	6530	
	TI	SN74S301	
♦DM8588	Intersil	IM5600	
	TI	SN74S188	
DM8590	Fairchild	93165	
	Raytheon	74165	
	TI	SN74165	
♦DM8597	Intersil	IM5623	
	MMI	**6201**	**1252**
	National	DM85S97	
	TI	SN74S287	
		SN74S370	
DM8598	Intersil	IM5610	
	MMI	**6231**	**1252**
	TI	SN74S288	
DM8599	AMD	AM27S03	
		DM8599	
	MMI	6561	
	TI	SN74S189	
DM86L70	TI	SN74L164	
DM86L97	Intersil	IM5623	
♦DM86L99	Fairchild	IM5501	
	MMI	L6561	
	National	**DM74LS189**	**1289**
♦DM8600	Motorola	MC8300	
DM8601	AMD	9601	
	Fairchild	9601	
	Raytheon	RF8601	
	Signetics	N8T22	
	TI	SN29601	
DM8602	AMD	9602	
	Fairchild	9602	
	Raytheon	RF8602	
♦DM8640	National	DS8640	
	TI	SN74141	
DM8796	**MMI**	**6241**	**1252**
♦DM88XX	National	DS88XX	
DM8810	TI	SN7426	
DM8842	TI	SN7442A	
DM8846	TI	SN7446A	
DM8847	TI	SN7447A	
DM8848	TI	SN7448	
♦DM8860	National	DS75491	
♦DM8862	National	DS75492	
DM8893	National	DS75493	
DM8894	National	DS75494	
DM9093	Motorola	MC853	
	Raytheon	RM993	
	TI	SN158093	
DM9094	Motorola	MC856	
	Raytheon	RM9094	
	TI	SN158094	
DM9097	Motorola	MC855	
	TI	SN158097	
DM9099	Motorola	MC852	
	Raytheon	RM999	
	TI	SN158099	
DM930	Motorola	MC830	
	Raytheon	RM930	
	TI	SN15830	
DM9300	AMD	9300	
	Raytheon	RM9300	
	TI	SN29300	
DM9301	AMD	9301	
	TI	SN29301	
DM9312	AMD	9312	
	TI	SN29312	
DM932	Motorola	MC832	
	Raytheon	RM932	
	TI	SN15838	
DM9322	AMD	9322	
	Raytheon	RM9322	
		54157	
	TI	SN29322	
DM933	Motorola	MC833	
	Raytheon	RM933	
	TI	SN15833	
DM93415	**NEC Micro**	**μPB2205**	**1418**
DM935	Motorola	MC840	
DM935	Raytheon	RM935	
	TI	SN15835	
DM936	Motorola	MC836	
	Raytheon	RM936	
	TI	SN15836	
DM937	Motorola	MC837	
	Raytheon	RM937	
	TI	SN15837	
DM944	Motorola	MC844	
	Raytheon	RM944	
	TI	SN15844	
DM945	Motorola	MC845	
	Raytheon	RM945	
	TI	SN15845	
DM946	Motorola	MC846	
	Raytheon	RM946	
	TI	SN15846	
DM948	Motorola	MC848	
	Raytheon	RM948	
	TI	SN15848	
DM949	Motorola	MC849	
	Raytheon	RM949	
	TI	SN15849	
DM951	Motorola	MC851	
	Raytheon	RM951	
	TI	SN15851	
DM9567	Motorola	MC857	
DM957	Raytheon	RM957	
	TI	SN15857	
DM958	Motorola	MC858	
	Raytheon	RM958	
	TI	SN15858	
DM9601	AMD	9601	
	Raytheon	RF9601	
	TI	SN29601	
DM9602	AMD	9602	
	Raytheon	RF9602	
DM961	Motorola	MC861	
	Raytheon	RM961	
	TI	SN15861	
DM962	Motorola	MC862	
	Raytheon	RM962	
	TI	SN15862	
DM963	Motorola	MC863	
	Raytheon	RM963	
	TI	SN15863	
DP8212	**NEC Micro**	**μPB8212**	**1804**
DP8216	**NEC Micro**	**μPB8216**	**1810**
DP8224	**NEC Micro**	**μPB8224**	**1764**
DP8226	**NEC Micro**	**μPB8226**	**1810**
DP8228	**NEC Micro**	**μPB8228**	**1769**
DP8238	**NEC Micro**	**μPB8238**	**1769**
DS0026	AMD	MH0026	
	Motorola	MMH0026	
	TI	SN75369	
DS1488	AMD	MC1488	
	Exar	XR1488	
	ITT	ITT1488	
	Motorola	MC1488	
	Raytheon	RC1488	
	Signetics	MC1488	
	Silicon G	SG1488	
	TI	SN75188	
DS1489	AMD	MC1489	
	Exar	XR1489	
	ITT	ITT1489	
	Motorola	MC1489	
	Raytheon	RC1489	
	Signetics	MC1489	
	Silicon G	SG1489	
	TI	SN75189	
DS1489A	Exar	XR1489A	
	Signetics	MC1489A	
DS1603	AMD	DS1603	
DS3603	AMD	DS3603	
DS3604	AMD	DS3604	
DS3611	Signetics	DS3611	
DS3612	Signetics	DS3612	
DS3613	Signetics	DS3613	
DS3614	Signetics	DS3614	
DS36147	Motorola	DS36147	
DS36177	Motorola	DS36177	
DS3645	Motorola	DS3645	
DS3647	Motorola	DS3647	
DS3650	Motorola	MC3450	
DS3651	Motorola	MC3430	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

National Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
DS3652	Motorola	MC3452	
DS3653	Motorola	MC3432	
DS3674	Motorola	MC3460	
DS3675	Motorola	DS3675	
DS3677	Motorola	DS3677	
DS3687	Motorola	MC3487	
DS55107	AMD	SN55107	
	Fairchild	55107	
	Motorola	MC55107	
	Raytheon	RM55107	
	TI	SN55107B	
DS55108	AMD	SN55108	
	Fairchild	55108	
	Motorola	MC55108	
	Raytheon	RM55108	
	TI	SN55108B	
DS55109	AMD	SN55109	
	Fairchild	55109	
	Raytheon	RM55109	
	TI	SN55109A	
DS55110	AMD	SN55110	
	Fairchild	55110	
	TI	SN55110A	
DS55121	Fairchild	55121	
	TI	SN55121	
DS55122	Fairchild	55122	
	TI	SN55122	
DS5520	AMD	SN5520	
	TI	SN5520	
DS5521	AMD	SN5521	
	TI	SN5520	
DS5522	TI	SN5522	
DS5523	TI	SN5522	
DS5524	AMD	SN5524	
	Fairchild	5524	
	Motorola	MC5524	
	TI	SN5524	
DS5525	AMD	SN5525	
	Fairchild	5525	
	Motorola	SN5525	
	TI	SN5524	
DS5528	Fairchild	5528	
	Motorola	MC5528	
	TI	SN5528	
DS5529	Fairchild	5529	
	Motorola	MC5529	
	TI	SN5528	
DS55325	AMD	SN55325	
	Motorola	MC55325	
	Raytheon	RM55325	
	TI	SN55325	
DS5534	Fairchild	5534	
	Motorola	MC5534	
DS5535	Fairchild	5535	
	Motorola	MC5535	
DS5538	Motorola	MC5538	
DS5539	Motorola	MC5539	
DS55450	TI	SN55450	
DS55451	TI	SN55451	
DS55452	TI	SN55452	
DS55453	TI	SN55453	
DS55454	TI	SN55454	
DS55460	TI	SN55460	
DS55461	TI	SN55461	
DS55462	TI	SN55462	
DS55463	TI	SN55463	
DS55464	TI	SN55464	
DS75107	AMD	SN75107	
	Fairchild	75107	
	ITT	ITT75107	
	Motorola	MC75107	
	Raytheon	RC75107	
	TI	SN75107B	
DS75108	AMD	SN74108	
	Fairchild	75108	
	ITT	ITT75108	
	Motorola	MC75108	
	Raytheon	RC75108	
	TI	SN75108B	
DS75109	AMD	SN75109	
	Fairchild	75109	
	ITT	ITT75109	
DS75109	Motorola	MC75109	
	Raytheon	RC75109	
	TI	SN75109A	
DS75110	AMD	SN75110	
	Fairchild	75110	
	ITT	ITT75110	
	Motorola	MC75110	
	Raytheon	RC75110	
	TI	SN75110A	
DS75121	Fairchild	75121	
	Motorola	MC8T13	
	TI	SN75121	
DS75122	Fairchild	75122	
	Motorola	MC8T14	
	TI	SN75122	
DS75123	Fairchild	75123	
	Motorola	MC8T23	
	TI	SN75123	
DS75124	Fairchild	75124	
	Motorola	MC8T24	
	TI	SN75124	
DS75150	TI	SN75150	
DS75154	Fairchild	75154	
	TI	SN75154	
DS7520	AMD	SN7520	
	ITT	ITT7520	
	Motorola	MC7520	
	Signetics	7520	
	Silicon G	SG7520	
	TI	SN7520	
DS75207	AMD	SN75207	
	Fairchild	75207	
	TI	SN75207B	
DS75208	AMD	SN75208	
	Fairchild	75208	
	TI	SN75208B	
DS7521	AMD	SN7521	
	Signetics	7521	
	Silicon G	SG7521	
	TI	SN7520	
DS7522	ITT	ITT7522	
	Motorola	MC7522	
	Signetics	7522	
	Silicon G	SG7522	
	TI	SN7522	
DS7523	Motorola	MC7523	
	Signetics	7523	
	Silicon G	SG7523	
	TI	SN7522	
DS7524	AMD	SN7524	
	Fairchild	7524	
	ITT	ITT7524	
	Motorola	MC7524	
	Signetics	7524	
	Silicon G	SG7524	
	TI	SN7524	
DS7525	AMD	SN7525	
	Fairchild	7525	
	ITT	ITT7524	
	Motorola	MC7525	
	NPC	SFC2525	
	Signetics	7525	
	Silicon G	SG7525	
	TI	SN7524	
DS7528	Fairchild	7528	
	ITT	ITT7528	
	Motorola	MC7528	
	NPC	SFC2528	
	Silicon G	SG7528	
	TI	SN7528	
DS7529	Fairchild	7529	
	Motorola	MC7529	
	Silicon G	SG7529	
	TI	SN7528	
DS75322	TI	SN75322	
DS75324	Raytheon	RC75324	
	TI	SN75324	
DS75325	AMD	SN75325	
	Fairchild	75325	
	ITT	ITT75325	
	Motorola	MC75325	
	Raytheon	RC75325	
	Silicon G	SG75325	
	TI	SN75325	
DS7534	Fairchild	7534	
	Motorola	MC7534	
DS7534	Silicon G	SG7534	
DS7535	Fairchild	7535	
	Motorola	MC7535	
DS75361	TI	SN75361A	
DS75364	TI	SN75364	
DS75365	Motorola	MC75365	
	TI	SN75365	
DS7538	Motorola	MC7538	
	Silicon G	SG7538	
DS7539	Motorola	MC7539	
	Silicon G	SG7539	
DS75450	Fairchild	75450	
	Motorola	MC75450	
	Raytheon	RC75450	
	Signetics	75450	
	Silicon G	SG75450	
	TI	SN75450	
DS75451	Fairchild	75451	
	Motorola	MC75451	
	Raytheon	RC75451	
	Signetics	75451	
	Silicon G	SG75451	
	TI	SN75451	
DS75452	Fairchild	75452	
	Motorola	MC75452	
	Raytheon	RC75452	
	Signetics	75452	
	Silicon G	SG75452	
	TI	SN75452	
DS75453	Fairchild	75453	
	Motorola	MC75453	
	Raytheon	RC75453	
	Signetics	75453	
	TI	SN75453	
DS75454	Fairchild	75454	
	Motorola	MC75454	
	Raytheon	RC75454	
	Signetics	75454	
	Silicon G	SG75454	
	TI	SN75454	
DS75460	TI	SN75460	
DS75461	Motorola	MC75401	
	TI	SN75461	
DS75462	Motorola	MC75402	
	TI	SN75462	
DS75463	Motorola	MC75403	
	TI	SN75463	
DS75464	Motorola	MC75404	
	TI	SN75464	
DS75491	Fairchild	75491	
	Motorola	MC75491	
	TI	SN75491	
DS75492	Fairchild	75492	
	Motorola	MC75492	
	TI	SN75492	
DS75493	TI	SN75493	
DS75494	TI	SN75494	
DS7800	TI	SN55180	
DS7820	AMD	DM7820	
	Signetics	DS7820	
	TI	SN55182	
DS7830	AMD	DM7830	
	Signetics	DS7830	
	TI	SN55183	
DS7831	AMD	DM7831	
	TI	DS7831	
DS7832	AMD	DM7832	
	TI	DS7832	
DS7838	AMD	DS7838	
DS8640	Signetics	SP380	
DS8641	Motorola	DS8641	
DS8800	TI	SN75180	
DS8820	AMD	DM8820	
	Signetics	DS8820	
	TI	DS8820	
		SN75182	
DS8830	AMD	DM8830	
	Signetics	DS8830	
	TI	SN75183	
DS8831	AMD	DM8831	
	TI	DS8831	
DS8832	AMD	DM8832	
	TI	DS8832	
DS8837	Motorola	MC3437	
DS8838	AMD	DS8838	
	Motorola	MC3438	
DS8880	Signetics	DS8880	
	TI	SN75480	
DS8889	Motorola	MC3491	
IDM2901A	AMD	AM2901A	
	Fairchild	F2901A	
		9409	
	NEC Micro	**μPB2901**	**1850**
	Raytheon	AM2901A	
	Signetics	**N2901**	**1851**
IDM2902	AMD	2902	
	Motorola	MC2902	
	NEC Micro	**μPB2902**	**1850**
	Raytheon	AM2902	
IDM2909A	AMD	2909	
	Motorola	MC2909	
	NEC Micro	**μPB2909**	**1850**
	Raytheon	AM2909	
IDM2911A	AMD	AM2911	
	Motorola	MC2911	
	NEC Micro	**μPB2911**	**1850**
	Raytheon	AM2911	
INS1671	Western	UC1671	
INS1771	Western	FD1771	
INS2650	Signetics	2650	
INS2651	Signetics	2651	
INS2656	Signetics	2656	
INS4001	Intel	4001	
INS4002	Intel	4002	
INS4003	Intel	4003	
INS4004	Intel	4004	
INS4008	Intel	4008	
INS4009	Intel	4009	
INS8080A	AMD	9080A	
	Intel	8080A	
	NEC Micro	**μPD8080AF**	**1736**
	Signetics	MP8080A	
	TI	TMS8080A	
INS8251	**NEC Micro**	**μPD8251**	**1814**
INS8255	**NEC Micro**	**μPD8255**	**1830**
ISP-8A/600	Signetics	ISP-8A/600	
LF111	AMD	LF111	
	Fairchild	μAF111	
LF11508	**PMI**	**MUX-08**	**958**
		MUX-88	**962**
LF12508	**PMI**	**MUX-08**	**958**
		MUX-88	**962**
LF13508	**PMI**	**MUX-08**	**958**
		MUX-88	**962**
LF152	Datel	AM-435-1M	
LF155	AMD	LF155	
	Fairchild	μAF155	
	Intersil	LF155	
	Motorola	LF155	
	PMI	**OP-15**	**871**
		PM155	**871**
	Raytheon	LF155	
	TI	LF155	
LF156	AMD	LF156	
	Fairchild	μAF156	
	Intersil	LF156	
	Motorola	LF156	
	PMI	**OP-16**	**877**
		PM156	**877**
	Raytheon	LF156	
	TI	LF156	
LF157	AMD	LF157	
	Fairchild	μAF157	
	Intersil	LF157	
	Motorola	LF157	
	PMI	**OP-17**	**882**
		PM157	**882**
	Raytheon	LF157	
	TI	LF157	
LF198	AMD	LF198	
LF211	AMD	LF211	
	Fairchild	μAF211	
LF255	AMD	LF255	
	Fairchild	μAF255	
	Intersil	LF255	
	Motorola	LF255	
	PMI	**OP-15**	**871**
		PM255	**871**
	Raytheon	LF255	
	TI	LF255	
LF256	AMD	LF256	
	Fairchild	μAF256	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

National Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
LF256	Intersil	LF256	
	Motorola	LF256	
	PMI	**OP-16**	**877**
		PM256	**877**
	Raytheon	LF256	
	TI	LF256	
LF257	AMD	LF257	
	Fairchild	μAF257	
	Intersil	LF257	
	Motorola	LF257	
	PMI	**OP-17**	**882**
		PM257	**882**
	Raytheon	LF257	
	TI	LF257	
LF298	AMD	LF298	
LF311	AMD	LF311	
LF352	Datel	AM-435-1C	
LF355	AMD	LF355	
	Fairchild	μAF355	
	Intersil	LF355	
	Motorola	LF355	
	PMI	**OP-15**	**871**
		PM355	**871**
	Raytheon	LF355	
	TI	LF355	
LF356	AMD	LF356	
	Fairchild	μAF356	
	Intersil	LF356	
	Motorola	LF356	
	PMI	**OP-16**	**877**
		PM356	**877**
	Raytheon	LF356	
	TI	LF356	
LF357	**AMD**	LF357	
	Fairchild	μAF357	
	Intersil	LF357	
	Motorola	LF357	
	PMI	**OP-17**	**882**
		PM357	**882**
	Raytheon	LF357	
	TI	LF357	
LF398	AMD	LF398	
	Datel	**SHM-LM-2**	**393**
LH0021	Beckman	833-21	
LH0042	AD	AD0042	
	Intersil	LH0042	
LH0062	AD	AD528	
LH2101	**AMD**	LH2101	
	Intersil	LH2101	
LH2108	Intersil	LH2108	
LH2110	Intersil	LH2110	
LH2111	AMD	LH2111	
	Intersil	LH2111	
LH2201	AMD	LH2201	
LH2211	**AMD**	LH2211	
LH2301	AMD	LH2301	
	Intersil	LH2301	
LH2308	Intersil	LH2308	
LH2310	Intersil	LH2310	
LH2311	AMD	LH2311	
	Intersil	LH2311	
LH740	Fairchild	μA740	
	Intersil	LH740	
	Signetics	μA740	
LM0052	AD	AD506	
LM100	Intersil	LM100	
	NPC	SFC2100	
	Silicon G	SG100	
LM101	AD	AD101	
	AMD	LM101	
	Fairchild	μA101	
	Intersil	LM101	
	Motorola	LM101	
	NPC	SFC2101	
	RCA	CA101	
		CA748	
	Signetics	LM101	
	Silicon G	SG101	
	TI	LM101	
LM102	AMD	LM102	
	Fairchild	μA102	
	Intersil	LM102	
LM102	Motorola	LM110	
	Silicon G	SG102	
LM104	Fairchild	μA104	
	Motorola	LM104	
	NPC	SFC2104	
	Raytheon	LM104	
	Silicon G	SG104	
	TI	LM104	
LM105	AMD	LM105	
	Fairchild	μA105	
	Intersil	LM105	
	Motorola	LM105	
	NPC	SFC2105	
	Raytheon	LM105	
	Silicon G	SG105	
	TI	LM105	
LM106	AMD	LM106	
	Raytheon	LM106	
	TI	LM106	
LM107	AD	AD741S	
	AMD	LM107	
	Fairchild	μA107	
	Intersil	LM107	
	Motorola	LM107	
	NPC	SFC2107	
	Raytheon	LM107	
	RCA	CA107	
	Signetics	LM107	
	Silicon G	SG107	
	TI	LM107	
LM108	AD	AD108	
	AMD	LM108	
	Fairchild	μA108	
	Intersil	LM108	
	Motorola	LM108	
	PMI	**PM108**	**858**
	Raytheon	LM108	
	RCA	CA108	
	Signetics	LM108	
	Silicon G	SG108	
LM109	Fairchild	μA109	
	Intersil	LM109	
	Motorola	LM109	
	NPC	SFC2109	
	Raytheon	LM109	
	Signetics	LM109	
	Silicon G	SG109	
	TI	LM109	
LM110	AMD	LM110	
	Fairchild	μA110	
	Intersil	LM110	
	Motorola	LM110	
	Silicon G	SG110	
LM111	AMD	LM111	
	Fairchild	μA111	
	Intersil	LM111	
	Motorola	LM111	
	NPC	SFC2111	
	Raytheon	LM111	
	RCA	CA111	
	Signetics	LM111	
	Silicon G	SG111	
	TI	LM111	
LM112	AMD	LM112	
	Raytheon	LM112	
	Silicon G	SG1118	
LM114	**PMI**	**MAT-01**	**887**
LM117	Motorola	LM117	
	TI	LM117	
LM118	AD	AD518	
	AMD	LM118	
	Raytheon	LM118	
	TI	LM118	
LM119	AMD	LM119	
LM120	Silicon G	SG120	
LM123	Motorola	LM123	
	Silicon G	SG123	
LM124	AMD	LM124	
	Fairchild	μA124	
	Intersil	LM124	
	Motorola	LM124	
	Raytheon	LM124	
	RCA	CA124	
	Signetics	LM124	
	Silicon G	SG124	
	TI	LM124	
LM1303	Motorola	MC1303	
	Raytheon	RC4739	
LM1304	Fairchild	μA732	
LM1307	Fairchild	μA767	
	Motorola	MC1307	
		MC1317	
LM1310	Exar	XR1310	
	Motorola	MC1310	
	RCA	CA1310	
	Sprague	ULN-2210	
LM1351	Motorola	MC1351	
LM139	AMD	LM139	
	Fairchild	μA139	
	Motorola	LM139	
	Raytheon	LM139	
	RCA	CA139	
	Signetics	LM139	
	Silicon G	SG139	
	TI	LM139	
LM1391	Motorola	MC1391	
	RCA	CA1391	
LM1394	Motorola	MC1394	
	RCA	CA1394	
LM140	Exar	XR146	
LM140-05	Silicon G	SG140-05	
LM140-06	Silicon G	SG140-06	
LM140-08	Silicon G	SG140-08	
LM140-12	Silicon G	SG140-12	
LM140-15	Silicon G	SG140-15	
LM140-18	Silicon G	SG140-18	
LM140-24	Silicon G	SG140-24	
LM1408	Datel	DAC-IC8BC	
LM1414	Motorola	MC1414	
	Raytheon	RC1414	
	TI	TL514	
LM143	**Harris**	**HA-2640**	**700**
LM1458	AMD	1458	
	Exar	XR1458	
	Fairchild	μA1458	
	Harris	**HA-2655**	**704**
	Motorola	MC1458	
	PMI	**OP-14**	**844**
		SSS1458	**844**
	Raytheon	RC1458	
		RC4558	
	RCA	CA1458	
	Signetics	MC1458	
	Silicon G	SG1458	
	TI	MC1458	
LM148	AMD	LM148	
	Exar	XR4741	
	Harris	**HA-4741**	**735**
	Intersil	LM148	
	Motorola	LM148	
		MC4741	
	Raytheon	LM148	
LM1488	Exar	XR1488	
	Motorola	MC1488	
	National	DS1488	
LM1489	Motorola	MC1489	
	National	DS1489	
LM149	AMD	LM149	
	Intersil	LM149	
LM1496	Fairchild	μA796	
	Motorola	MC1496	
	Signetics	MC1496	
	Silicon G	SG1496	
LM1508	Datel	DAC-IC8BM	
LM1514	Motorola	MC1514	
	Raytheon	RM1514	
	TI	TL514	
LM1558	AMD	1558	
	Exar	XR1588	
	Fairchild	μA1558	
	Harris	**HA-2650**	**704**
	Motorola	MC1558	
	PMI	**PM1558**	**844**
		SSS1558	**844**
	Raytheon	RM1558	
	RCA	CA1558	
	Signetics	MC1558	
	Silicon G	SG1558	
	TI	MC1558	
LM158	Motorola	LM158	
	Raytheon	LM158	
		RM4139	
LM158	Signetics	SE532	
	TI	LM158	
LM1596	Motorola	MC1596	
	Signetics	MC1596	
	Silicon G	SG1596	
LM160	Fairchild	μA760	
LM1611	National	DS1611	
LM1612	National	DS1612	
LM1613	National	DS1613	
LM1614	National	DS1614	
LM163	**National**	**DS1603**	**504**
LM163A	National	DS1604	
LM1800	Exar	XR1800	
	Fairchild	μA758	
	RCA	CA758	
	Sprague	ULN-2244	
LM1820	Fairchild	μA720	
	Sprague	ULN-2137	
LM1829	Fairchild	μA787	
LM1841	Fairchild	μA2136	
	Motorola	MC1356	
	Sprague	ULN-2136	
LM193	Signetics	LM193	
	TI	LM193	
LM200	Intersil	LM200	
	NPC	SFC2200	
	Silicon G	SG200	
LM201	AD	AD201	
	AMD	LM201	
	Fairchild	μA201	
	Intersil	LM201	
	Motorola	LM201	
	NPC	SFC2201	
	RCA	CA201	
		CA748	
	Signetics	LM201	
	Silicon G	SG201	
	TI	LM201	
LM202	AMD	LM202	
	Fairchild	μA202	
	Intersil	LM202	
	Motorola	LM210	
	Silicon G	SG202	
LM204	Fairchild	μA204	
	Motorola	LM204	
	NPC	SFC2204	
	Raytheon	LM204	
	Silicon G	SG204	
	TI	LM204	
LM205	AMD	LM205	
	Fairchild	μA205	
	Intersil	LM205	
	Motorola	LM205	
	NPC	SFC2205	
	Raytheon	LM205	
	Silicon G	SG205	
	TI	LM205	
LM206	AMD	LM206	
	TI	LM206	
LM207	AD	AD741J	
	AMD	LM207	
	Fairchild	μA207	
	Intersil	LM207	
	Motorola	LM207	
	NPC	SFC2207	
	Raytheon	LM207	
	RCA	CA207	
	Signetics	LM207	
	Silicon G	SG207	
	TI	LM207	
LM208	AD	AD208	
	AMD	LM208	
	Fairchild	μA208	
	Intersil	LM208	
	Motorola	LM208	
	PMI	PM208	
	Raytheon	LM208	
	RCA	CA208	
	Signetics	LM208	
	Silicon G	SG208	
LM209	Fairchild	μA209	
	Intersil	LM209	
	Motorola	LM209	
	NPC	SFC2209	
	Raytheon	LM209	
	Signetics	LM209	

◆ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

National Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
LM209	Silicon G	SG209	
	TI	LM209	
LM210	AMD	LM210	
	Fairchild	μA210	
	Intersil	LM210	
	Motorola	LM210	
	Silicon G	SG210	
LM211	AMD	LM211	
	Fairchild	μA211	
	Intersil	LM211	
	Motorola	LM211	
	NPC	SFC2211	
	Raytheon	LM211	
	RCA	CA211	
	Signetics	LM211	
	Silicon G	SG211	
	TI	LM211	
LM2111	Motorola	MC1357	
	RCA	CA2111	
	Signetics	ULN2111	
	Sprague	ULN-2111	
LM2113	Sprague	ULN-2113	
LM212	AMD	LM212	
	Raytheon	LM212	
LM216	AMD	LM216	
LM217	Motorola	LM217	
	TI	LM217	
LM218	AD	AD518	
	AMD	LM218	
	Raytheon	LM218	
	TI	LM218	
LM219	AMD	LM219	
LM223	Motorola	LM223	
LM224	AMD	LM224	
	Intersil	LM224	
	Motorola	LM224	
	Raytheon	LM224	
	RCA	CA224	
	Signetics	LM224	
	Silicon G	SG224	
	TI	LM224	
LM239	AMD	LM239	
	Motorola	LM239	
		MC3302	
	Raytheon	LM239	
	RCA	CA239	
	Signetics	LM239	
	Silicon G	SG239	
	TI	LM239	
LM246	Exar	XR246	
LM248	AMD	LM248	
	Exar	XR4741	
	Intersil	LM248	
	Motorola	LM248	
		MC4741	
	Raytheon	LM248	
LM249	AMD	LM249	
	Intersil	LM249	
LM258	Motorola	LM258	
	Raytheon	LM258	
	Signetics	LM258	
	TI	LM258	
LM2900	Fairchild	μA2900	
	Motorola	LM2900	
	Raytheon	LM2900	
LM2901	Fairchild	μA2901	
	Motorola	LM2901	
	Raytheon	LM2901	
	TI	LM2901	
LM2902	Fairchild	μA2902	
	Motorola	LM2902	
	Raytheon	LM2902	
	TI	LM2902	
LM2903	TI	LM2903	
LM2904	Motorola	LM2904	
	TI	LM2904	
LM293	Signetics	LM293	
	TI	LM293	
LM300	Intersil	LM300	
	NPC	SFC2300	
	Silicon G	SG300	
LM301	AD	AD301	
LM301	AMD	LM301	
	Fairchild	μA301	
	Intersil	LM301	
	Motorola	LM301	
	NPC	SFC2301	
	Raytheon	LM301	
	RCA	CA301	
	Signetics	LM301	
	Silicon G	SG301	
	TI	LM301	
LM3011	RCA	CA3011	
LM3018	Fairchild	μA3018	
	RCA	CA3018	
LM3019	Fairchild	μA3019	
	RCA	CA3019	
LM302	AMD	LM302	
	Fairchild	μA302	
	Intersil	LM302	
	Motorola	LM310	
		MC7912	
	Silicon G	SG302	
LM3026	Fairchild	μA3026	
	RCA	CA3026	
LM3028	RCA	CA3028	
LM3039	RCA	CA3039	
LM304	Fairchild	μA304	
	Motorola	LM304	
	NPC	SFC2304	
	Raytheon	LM304	
	Silicon G	SG304	
	TI	LM304	
LM3045	Fairchild	μA3045	
	RCA	CA3045	
	Silicon G	SG3045	
LM3046	Fairchild	μA3046	
	Motorola	MC3346	
	RCA	CA3046	
	Silicon G	SG3046	
LM305	AMD	LM305	
	Fairchild	μA305	
	Intersil	LM305	
	Motorola	LM305	
	NPC	SFC2305	
	Raytheon	LM305	
	Silicon G	SG305	
	TI	LM305	
LM3053	Fairchild	μA753	
	RCA	CA3053	
LM3054	Fairchild	μA3054	
	Motorola	CA3054	
	RCA	CA3054	
LM306	AMD	LM306	
	Raytheon	LM306	
	TI	LM306	
LM3064	Fairchild	μA3064	
	Motorola	MC1364	
	RCA	CA3064	
	Sprague	ULN-2264	
LM3065	Fairchild	μA3065	
	Motorola	MC1358	
	RCA	CA3065	
	Sprague	ULN-2165	
♦LM3066	Fairchild	μA3066	
	RCA	CA3066	
LM3067	Fairchild	μA3067	
	RCA	CA3067	
LM307	AD	AD741J	
	AMD	LM307	
	Fairchild	μA307	
	Intersil	LM307	
	Motorola	LM307	
	NPC	SFC2307	
	Raytheon	LM307	
	RCA	CA307	
	Signetics	LM307	
	Silicon G	SG307	
	TI	LM307	
LM3070	Fairchild	μA780	
	RCA	CA3070	
	Sprague	ULN-2124	
LM3071	RCA	CA3071	
	Sprague	ULN-2127	
LM3072	RCA	CA3072	
LM3075	Fairchild	μA3075	
	Motorola	MC1375	
	RCA	CA3075	
LM308	AD	AD308	
	AMD	LM308	
	Fairchild	μA308	
	Intersil	LM308	
	Motorola	LM308	
	PMI	PM308	
	Raytheon	LM308	
	RCA	CA308	
	Signetics	LM308	
	Silicon G	SG308	
LM3086	Fairchild	μA3086	
	Motorola	MC3386	
	RCA	CA3086	
LM3089	RCA	CA3089	
LM309	Fairchild	μA309	
	Intersil	LM309	
	Motorola	LM309	
	NPC	SFC2309	
	Raytheon	LM309	
	Signetics	LM309	
	Silicon G	SG309	
	TI	LM309	
LM310	AMD	LM310	
	Fairchild	μA310	
	Intersil	LM310	
	Motorola	LM310	
	Silicon G	SG310	
LM311	AMD	LM311	
	Fairchild	μA311	
	Intersil	LM311	
	Motorola	LM311	
	NPC	SFC2311	
	Raytheon	LM311	
	RCA	CA311	
	Signetics	LM311	
	Silicon G	SG311	
	TI	LM311	
LM312	AMD	LM312	
	Raytheon	LM312	
LM3126	RCA	CA3126	
LM316	AMD	LM316	
LM317	Motorola	LM317	
	TI	LM317	
LM318	AD	AD518	
	AMD	LM318	
	Raytheon	LM318	
	TI	LM318	
LM319	AMD	LM319	
LM320	Motorola	MC7905	
	Silicon G	SG320	
LM320-05	Motorola	MC7905	
	Silicon G	SG320-05	
	TI	μA7905	
LM320-06	TI	μA7906	
LM320-08	TI	μA7908	
LM320-12	Motorola	MC7912	
	Silicon G	SG320-12	
	TI	μA7912	
LM320-15	TI	μA7915	
LM320-24	TI	μA7924	
LM320M-05	TI	μA79M05	
LM320M-06	TI	μA79M06	
LM320M-08	TI	μA79M08	
LM320M-12	TI	μA79M12	
LM320M-15	TI	μA79M15	
LM320M-24	Signetics	μA79M24	
	TI	μA79M24	
LM320M05	Signetics	μA79M05	
LM320M06	Signetics	μA79M06	
LM320M08	Signetics	μA79M08	
LM320M12	Signetics	μA79M12	
LM320M15	Signetics	μA79M15	
LM320M18	Signetics	μA79M18	
LM320T06	Signetics	μA7906	
LM320T08	Signetics	μA7908	
LM320T12	Signetics	μA7912	
LM320T15	Signetics	μA7915	
LM320T18	Signetics	μA7918	
LM320T24	Signetics	μA7924	
LM323	Fairchild	SH0323	
	Motorola	LM323	
	Silicon G	SG323	
LM324	AMD	LM324	
	Fairchild	μA324	
	Motorola	LM324	
	Raytheon	LM324	
LM324	RCA	CA324	
	Signetics	LM324	
	Silicon G	SG324	
	TI	LM324	
LM3301	Motorola	MC3301	
LM3302	Motorola	MC3302	
	Silicon G	SG3302	
	TI	LM3302	
LM339	AMD	LM339	
	Fairchild	μA339	
	Motorola	LM339	
		MC3302	
	Raytheon	LM339	
	RCA	CA339	
	Signetics	LM339	
	Silicon G	SG339	
	TI	LM339	
LM340-10	TI	LM340-10	
LM340-12	Fairchild	μA7812	
	Motorola	MC7812	
	Raytheon	RC7812	
	Signetics	LM340-12	
	Silicon G	SG340-12	
	TI	μA7812	
		LM340-12	
LM340-15	Fairchild	μA7815	
	Motorola	MC7815	
	Signetics	μA7815	
		LM340-15	
	Silicon G	SG340-15	
	TI	μA7815	
		LM340-15	
LM340-18	Fairchild	μA7818	
	Motorola	MC7818	
	Raytheon	RC7818	
	Signetics	μA7818	
		LM340-18	
	Silicon G	SG340-18	
	TI	μA7818	
		LM340-18	
LM340-24	Fairchild	μA7824	
	Motorola	MC7824	
	Raytheon	RC7824	
	Signetics	μA7824	
		LM340-24	
	Silicon G	SG340-24	
	TI	μA7824	
		LM340-24	
LM340-5	Fairchild	μA7805	
	Motorola	MC7805	
	Raytheon	RC7805	
	Signetics	μA7805	
		LM340-5	
	Silicon G	SG340-05	
	TI	μA7805	
		LM340-5	
LM340-6	Fairchild	μA7806	
	Motorola	MC7806	
	Raytheon	RC7806	
	Signetics	μA7806	
		LM340-6	
	Silicon G	SG340-06	
	TI	LM340-6	
LM340-8	Fairchild	μA7808	
	Motorola	MC7808	
	Raytheon	RC7808	
	Signetics	μA7808	
		LM340-8	
	Silicon G	SG340-08	
	TI	μA7808	
		LM340-8	
LM3401	Motorola	MC3401	
LM341-12	Motorola	MC78M12	
LM341-15	Motorola	MC78M15	
LM341-24	Motorola	MC78M24	
LM341-5	Motorola	MC78M05	
LM341-6	Motorola	MC78M06	
	Signetics	μA78M06	
LM341-8	Motorola	MC78M08	
LM342-05	Motorola	MC78M05	
LM342-06	Motorola	MC78M06	
LM342-08	Motorola	MC78M08	
LM342-12	Motorola	MC78M12	
LM342-15	Motorola	MC78M15	
LM342-18	Motorola	MC78M18	
LM342-24	Motorola	MC78M24	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

National Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
LM343	**Harris**	**HA-2645**	**700**
	Motorola	MC1439	
LM346	Exar	XR346	
LM348	AMD	LM348	
	Exar	XR4741	
	Harris	**HA-4741**	**735**
	Motorola	LM348	
		MC4741	
	Raytheon	LM348	
LM349	AMD	LM349	
LM350	National	DS350	
LM351	National	DS75453	
LM354	NPC	SFC2524	
		SFC2525	
♦LM358	Motorola	LM358	
	Raytheon	LM358	
		RC4139	
	Signetics	LM358	
	TI	LM358	
♦LM360	Fairchild	μA760	
LM3611	Sprague	ULN-3611	
♦LM3612	National	DS3612	
	Sprague	ULN-3612	
♦LM3613	National	DS3613	
	Sprague	ULN-3613	
♦LM3614	National	DS3614	
	Sprague	ULN-3614	
♦LM3625	**National**	**DS3625**	**514**
♦LM363	**National**	**DS3603**	**504**
♦LM363A	**National**	**DS3604**	**504**
♦LM367	Silicon G	SG305	
♦LM376	Fairchild	μA376	
	Motorola	LM305	
	NPC	SFC2376	
	TI	LM376	
LM377	Sprague	ULN 2278	
LM380	Sprague	ULN-2280	
LM3900	Fairchild	μA3900	
	Motorola	MC3401	
	Raytheon	RC3302	
♦LM3901	Motorola	MC3302	
	Raytheon	MC3302	
LM3909	**Siliconix**	**LM3909**	**984**
LM393	Signetics	LM393	
	TI	LM393	
LM4250	Fairchild	μA776	
	Harris	**HA-2720**	**712**
	Intersil	LM4250	
	Silicon G	SG4250	
	Solitron	UC4250	
LM55107A	Motorola	MC55107	
	National	**DS55107**	**504**
LM55108A	Motorola	MC55108	
	National	**DS55108**	**504**
LM5520	National	DS5520	
LM5521	National	DS5521	
LM5522	National	DS5522	
LM5523	National	DS5523	
LM5524	Motorola	MC5524	
	National	DS5524	
LM5525	Motorola	MC5525	
	National	DS5525	
LM5528	Motorola	MC5528	
	National	DS5528	
LM5529	Motorola	MC5529	
	National	DS5529	
LM55325	Motorola	MC55325	
	National	**DS55325**	**520**
LM5534	Motorola	MC5534	
	National	DS5534	
LM5535	Motorola	MC5535	
	National	DS5535	
♦LM5538	National	DS5538	
LM5539	Motorola	MC5539	
	National	DS5539	
LM55450	National	DS55450	
LM55451	National	DS55451	
LM55452	National	DS55452	
LM55454	National	DS55454	
LM555	AMD	LM555	
	Exar	XR555	
	Fairchild	μA555	
LM555	Intersil	LM555	
	Motorola	MC1455	
		MC1555	
	Raytheon	RC555	
		RM555	
	RCA	CA555	
	Signetics	NE555	
	Silicon G	SG555	
	TI	NE555	
		SE555	
LM556	AMD	LM556	
	Exar	XR556	
	Fairchild	μA556	
	Motorola	MC3456	
		MC3556	
	Silicon G	SG556	
	TI	NE556	
		SE556	
LM565	Motorola	LM565	
	Signetics	NE565	
LM566	Signetics	NE566	
LM567	Exar	XR567	
	Signetics	NE567	
LM703	Fairchild	μA703	
LM709	Fairchild	μA709	
	Motorola	MC1709	
	NPC	SFC2709	
	Raytheon	RC709	
		RM709	
	Signetics	μA709	
	TI	μA709	
LM710	Fairchild	μA710	
	Motorola	MC1710	
	NPC	SFC2710	
	Raytheon	RC710	
		RM710	
	RCA	CA710	
	Signetics	μA710	
	Silicon G	SG710	
	TI	μA710	
LM711	Fairchild	μA711	
	Motorola	MC1711	
	NPC	SFC2711	
	Raytheon	RC711	
		RM711	
	RCA	CA711	
	Signetics	μA711	
	Silicon G	SG711	
	TI	μA711	
LM723	AMD	723	
	Fairchild	μA723	
	Intersil	723	
	Motorola	MC1723	
	NPC	SFC2723	
	Raytheon	RC723	
		RM723	
	RCA	CA723	
	SGS	L123	
	Signetics	μA723	
	Silicon G	SG723	
	TI	μA723	
LM725	AMD	725	
	Fairchild	μA725	
	Intersil	SSS725	
	PMI	**PM725**	**849**
		SSS725	**849**
	Raytheon	RC725	
		RM725	
LM733	AMD	733	
	Fairchild	μA733	
	Motorola	MC1733	
	Raytheon	RC733	
		RM733	
	Signetics	μA733	
	Silicon G	SG733	
	TI	μA733	
LM741	AD	AD741	
	AMD	741	
	Fairchild	μA741	
	Intersil	SSS741	
		741	
	Motorola	MC1741	
	NPC	SFC2741	
	PMI	**OP-02**	**839**
		PM741	**839**
		SSS741	**839**
LM741	Raytheon	RC741	
		RM741	
	RCA	CA741	
	Signetics	μA741	
	Silicon G	SG741	
	TI	μA741	
LM746	Motorola	MC1328	
	Sprague	ULN-2114	
		ULN-2228	
LM747	AMD	747	
	Fairchild	μA747	
	Intersil	SSS747	
	Motorola	MC1747	
	PMI	**OP-04**	**844**
		PM747	**844**
		SSS747	**844**
	Raytheon	RC747	
		RM747	
	RCA	CA747	
	Signetics	μA747	
	Silicon G	SG747	
	TI	μA747	
LM748	AMD	748	
	Fairchild	μA748	
	Intersil	748	
	Motorola	MC1748	
	NPC	SFC2748	
	Raytheon	RC748	
		RM748	
	RCA	CA748	
	Signetics	μA748	
	Silicon G	SG748	
	TI	μA748	
LM75107A	Motorola	MC75107	
	National	**DS75107**	**504**
LM75108A	Motorola	MC75108	
	National	**DS75108**	**504**
LM75110	Motorola	MC75110	
LM75121	Motorola	MC8T13	
LM75122	Motorola	MC8T14	
LM75123	Motorola	MC8T23	
LM75124	Motorola	MC8T24	
LM7520	National	DS7520	
LM7521	National	DS7521	
LM7522	National	DS7522	
LM7523	National	DS7523	
LM7524	Motorola	MC7524	
	National	DS7524	
LM7525	Motorola	MC7525	
	National	DS7525	
LM7528	Motorola	MC7528	
	National	DS7528	
LM7529	Motorola	MC7529	
	National	DS7529	
LM75324	**National**	**DS75324**	**522**
LM75325	Motorola	MC75325	
	National	**DS75325**	**520**
LM7534	Motorola	MC7534	
	National	DS7534	
LM7535	Motorola	MC7535	
	National	DS7535	
LM7538	Motorola	MC7538	
	National	DS7538	
LM7539	Motorola	MC7539	
	National	DS7539	
LM75450	Motorola	MC75450	
	National	DS75450	
LM75451	Motorola	MC75451	
	National	DS75451	
LM75452	Motorola	MC75452	
	National	DS75452	
LM75453	Motorola	MC75453	
LM75454	Motorola	MC75454	
	National	DS75454	
LM78L05	Motorola	MC78L05	
	Signetics	μA78L05	
	Silicon G	SG7805	
	TI	μA78L05	
LM78L06	Signetics	μA78L06	
	TI	μA78L06	
LM78L08	Motorola	MC78L08	
	Signetics	μA78L08	
	Silicon G	SG7808	
	TI	μA78L08	
LM78L12	Motorola	MC78L12	
	Signetics	μA78L12	
LM78L12	Silicon G	SG7812	
	TI	μA78L12	
LM78L15	Motorola	MC78L15	
	Signetics	μA78L15	
	Silicon G	SG7815	
	TI	μA78L15	
LM78L18	Motorola	MC78L18	
	Silicon G	SG7818	
LM78L24	Motorola	MC78L24	
	Signetics	μA78L24	
	Silicon G	SG7824	
LM7805	Motorola	MC7805	
	Signetics	μA7805	
	Silicon G	SG7805	
	TI	μA7805	
LM7806	Motorola	MC7806	
	Signetics	μA7806	
	Silicon G	SG7806	
LM7808	Motorola	MC7808	
	Signetics	μA7808	
	TI	μA7808	
LM7812	Motorola	MC7812	
	Signetics	μA7812	
	Silicon G	SG7812	
	TI	μA7812	
LM7815	Motorola	MC7815	
	Signetics	μA7815	
	Silicon G	SG7815	
	TI	μA7815	
LM7818	Motorola	MC7818	
	Signetics	μA7818	
	Silicon G	SG7818	
	TI	μA7818	
		μA7918	
LM7824	Motorola	MC7824	
	Signetics	μA7824	
	Silicon G	SG7824	
	TI	μA7824	
LM7905	Motorola	MC7905	
	Signetics	μA7905	
	TI	μA7905	
LM7905.2	Motorola	MC7905.2	
	Signetics	μA7905.2	
LM7906	Motorola	MC7906	
	Signetics	μA7906	
	TI	μA7906	
LM7908	Motorola	MC7908	
	Signetics	μA7908	
	TI	μA7908	
LM7912	Motorola	MC7912	
	Signetics	μA7912	
	TI	μA7912	
LM7915	Motorola	MC7915	
	Signetics	μA7915	
	TI	μA7915	
LM7918	Signetics	μA7918	
LM7924	Motorola	MC7924	
	Signetics	μA7924	
	TI	μA7924	
MH0025	**National**	**DS0025**	**502**
MH0026	**National**	**DS0026**	**503**
MH0056	**National**	**DS0056**	**503**
MH7803	**National**	**DS7803**	**518**
MH8803	**National**	**DS8803**	**518**
MH8808	National	DS8808	
MM1101	AMD	1101	
	Intersil	IM7501	
		IM7511	
		IM7512	
	Mostek	MK4007	
MM1103	Signetics	1103	
MM1402	AMD	1402	
	SGS	M141	
	Signetics	1402	
		2502	
	Synertek	SY1402	
MM1403	AMD	1403	
	AMI	S2503	
	SGS	M136	
	Signetics	2503	
	Synertek	SY1403	
MM1404	AMD	1404	
	AMI	S2504	
	SGS	M130	
	Signetics	2504	
	Synertek	SY1404	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

National Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
MM1702A	Mostek	MK3702	
MM2101	NEC Micro	μPD2111A	
	Signetics	2101	
MM2102	Fairchild	21021	
		21022	
	Mostek	MK4102	
	Signetics	2102	
	TI	TMS4035	
MM2102A	NEC Micro	μPD2102A	
MM2111	Signetics	2111	
MM2112	Signetics	2112	
MM2316A	**NEC Micro**	**μPD2316A**	**1481**
MM233	Fairchild	3414	
		3415	
MM2521	AMD	AM2521	
	Signetics	2521	
MM2522	Signetics	2522	
MM2533	AMD	AM2533	
	Signetics	2533	
MM2708	AMD	2708	
	EA	EA2708	
	Fujitsu	MB8518	
	Intel	2708	
	Mostek	MK2708	
	Motorola	MCM2708	
	TI	TMS2708	
MM4232	Mostek	MK2500	
MM4240	AMI	S8614	
MM4280	**NEC Micro**	**μPD411**	**1375**
MM452	Siliconix	SI452	
MM455	Siliconix	SI455	
♦MM46XX	National	CD40XX	
♦MM5013	AMI	S2512A	
	Signetics	2512	
		2525	
MM5016	AMI	S1865	
♦**MM5020**	**Intersil**	**IM7780**	
MM5025	Synertek	SY2825	
MM5026	Synertek	SY2826	
MM5027	Synertek	SY2827	
MM5054	AMI	S2181	
MM5055	AMD	5055	
MM5057	AMD	5057	
MM5058	Signetics	2533	
MM506	Signetics	2506	
MM5060	AMI	S2181	
MM5062	Signetics	2532	
MM5066	AMD	5056	
MM507	Signetics	2517	
MM5204	**AMI**	**S5204**	**1057**
MM5231	AMI	S5232	
MM5232	AMI	S5232	
	Mostek	MK2500	
		MK2503	
		MK2600	
MM5233	AMI	S3514	
MM5257	Mostek	MK4104	
	Motorola	MCM2141	
	TI	TMS4044	
MM5262	Nortec	6003	
MM5264	Nortec	6003	
MM5280	Intersil	7280	
	Signetics	2680	
MM5280A	**NEC Micro**	**μPD411**	**1375**
MM5281	**NEC Micro**	**μPD411**	**1375**
MM5290	Signetics	2690	
MM5303	GI	AY3-1014A	
		AY3-1015	
		AY5-1013A	
MM5387	AMI	S1998	
MM54C00	Harris	HD54C00	
MM54C02	Harris	HD54C02	
MM54C04	Harris	HD54C04	
MM54C08	Harris	HD54C08	
MM54C10	Harris	HD54C10	
MM54C107	Harris	HD54C107	
MM54C14	Harris	HD54C14	
	Motorola	MC14584	
MM54C151	Harris	HD54C151	
MM54C154	Harris	HD54C154	
MM54C157	Harris	HD54C157	
MM54C160	Harris	HD54C160	
MM54C160	Motorola	MC14160	
MM54C161	Harris	HD54C161	
	Motorola	MC14161	
MM54C162	Harris	HD54C162	
	Motorola	MC14162	
MM54C163	Harris	HD54C163	
	Motorola	MC14163	
MM54C164	Harris	HD54C164	
	Motorola	MC14164	
MM54C165	Harris	HD54C165	
	Motorola	MC14165	
MM54C173	Harris	HD54C173	
	Motorola	MC14076	
MM54C174	Harris	HD54C174	
	Motorola	MC14174	
MM54C175	Harris	HD54C175	
	Motorola	MC14175	
MM54C192	Harris	HD54C192	
MM54C193	Harris	HD54C193	
MM54C195	Harris	HD54C195	
MM54C20	Harris	HD54C20	
MM54C221	Harris	HD54C221	
MM54C30	Harris	HD54C30	
MM54C32	Harris	HD54C32	
MM54C42	Harris	HD54C42	
MM54C48	Harris	HD54C48	
MM54C73	Harris	HD54C73	
MM54C74	Harris	HD54C74	
MM54C76	Harris	HD54C76	
MM54C83	Harris	HD54C83	
MM54C85	Harris	HD54C85	
MM54C86	Harris	HD54C86	
MM54C90	Harris	HD54C90	
MM54C901	Harris	HD54C901	
MM54C902	Harris	HD54C902	
MM54C903	Harris	HD54C903	
MM54C904	Harris	HD54C904	
MM54C906	Harris	HD54C906	
MM54C907	Harris	HD54C907	
MM54C914	Harris	HD54C914	
MM54C922	Harris	HD54C922	
MM54C923	Harris	HD54C923	
MM54C925	Harris	HD54C925	
MM54C926	Harris	HD54C926	
MM54C927	Harris	HD54C927	
MM54C928	Harris	HD54C928	
MM54C93	Harris	HD54C93	
MM54C95	Harris	HD54C95	
MM551	AMI	MX52D	
MM55104	Motorola	MC145104	
MM55106	Motorola	MC145106	
MM55114	Motorola	MC145104	
MM55116	Motorola	MC145106	
MM552	Siliconix	SI552	
MM555	Siliconix	SI555	
MM5555	Nitron	NCM1183	
MM5556	Nitron	NC1184	
MM5823	GI	AY1-2006	
MM5824	GI	AY1-1006	
MM5837	AMI	S2688	
MM70C95	Harris	HD70C95	
MM70C97	Harris	HD70C97	
MM74C00	Harris	HD74C00	
	RCA	CD4011	
MM74C02	Harris	HD74C02	
	RCA	CD4001	
MM74C04	Fairchild	F4069	
	Harris	HD74C04	
	Mitel	SIL4069	
	Motorola	MC14069	
	National	CD4069	
	NEC America	μPD4069	
	RCA	CD4069	
	Solitron	CM4069	
	SSS	SCL4069	
	TI	TP4069	
	Toshiba	TC4069	
MM74C08	Harris	HD74C08	
	RCA	CD4081	
MM74C10	Harris	HD74C10	
	RCA	CD4023	
MM74C107	Harris	HD74C107	
MM74C14	Harris	HD74C14	
	Motorola	MC14584	
	National	CD40106	
		CD4584	
MM74C14	RCA	CD40106	
		CD4016	
	SSS	SCL4584	
MM74C151	Harris	HD74C151	
MM74C154	Harris	HD74C154	
MM74C157	Harris	HD74C157	
MM74C160	Fairchild	F40160	
	Harris	HD74C160	
	Motorola	MC14160	
MM74C161	Fairchild	F40161	
	Harris	HD74C161	
	Motorola	MC14161	
	SSS	SCL4160	
MM74C162	Fairchild	F40162	
	Harris	HD74C162	
	Motorola	MC14162	
	SSS	SCL4162	
MM74C163	Fairchild	F40163	
	Harris	HD74C163	
	Motorola	MC14163	
	SSS	SCL4163	
MM74C164	Harris	HD74C164	
	Motorola	MC14015	
MM74C165	Harris	HD74C165	
	Motorola	MC14021	
MM74C173	Fairchild	F4076	
	Harris	HD74C173	
	Mitel	SIL4076	
	Motorola	MC14076	
	National	CD4076	
	RCA	CD4076	
	Solitron	CM4076	
	SSS	SCL4076	
	TI	TP4076	
MM74C174	Fairchild	F40174	
	Harris	HD74C174	
	Motorola	MC14174	
MM74C175	Fairchild	F40175	
	Harris	HD74C175	
	Motorola	MC14175	
MM74C192	Fairchild	F40192	
	Harris	HD74C192	
	National	CD40192	
	RCA	CD40192	
MM74C193	Fairchild	F40193	
	Harris	HD74C193	
	National	CD40193	
	RCA	CD40193	
MM74C195	Fairchild	F40195	
	Harris	HD74C195	
MM74C20	Harris	HD74C20	
	RCA	CD4012	
MM74C200	RCA	CD4061	
MM74C221	Harris	HD74C221	
	RCA	CD4098	
MM74C30	Harris	HD74C30	
	RCA	CD4068	
MM74C32	Harris	HD74C32	
	RCA	CD4071	
MM74C42	Harris	HD74C42	
	RCA	CD4028	
MM74C48	Harris	HD74C48	
MM74C73	Harris	HD74C73	
MM74C74	Harris	HD74C74	
	RCA	CD4013	
MM74C76	Harris	HD74C76	
	RCA	CD4027	
MM74C83	Harris	HD74C83	
	RCA	CD4008	
MM74C85	Fairchild	F40085	
	Harris	HD74C85	
	Motorola	MC14585	
	RCA	CD4063	
	SSS	SCL4585	
	Toshiba	TC4585	
MM74C86	Fairchild	F4070	
	Harris	HD74C86	
	Mitel	SIL4070	
	Motorola	MC14507	
	National	CD4070	
		CD4507	
	RCA	CD4030	
		CD4070	
	Solitron	CM4070	
	SSS	SCL4030	
		SCL4070	
MM74C86	TI	TP4507	
MM74C89	Fairchild	4725	
	Harris	HD74C89	
MM74C90	Harris	HD74C90	
MM74C901	Harris	HD74C901	
MM74C902	Harris	HD74C902	
MM74C903	Harris	HD74C903	
MM74C904	Harris	HD74C904	
MM74C906	Harris	HD74C906	
MM74C907	Harris	HD74C907	
MM74C914	Harris	HD74C914	
MM74C920	**AMI**	**S5101**	**1041**
	Harris	**HM6551**	**1175**
	NEC Micro	**μPD5101**	**1438**
MM74C922	Harris	HD74C922	
MM74C923	Harris	HD74C923	
MM74C925	Harris	HD74C925	
MM74C926	Harris	HD74C926	
MM74C927	Harris	HD74C927	
MM74C928	Harris	HD74C928	
MM74C929	**Harris**	**HM6508**	**1180**
MM74C93	Harris	HD74C93	
MM74C930	**Harris**	**HM6518**	**1181**
MM74C95	Harris	HD74C95	
MM74S157	Harris	HD74C157	
MM74S289	NEC Micro	μPB2089	
MM80C95	Harris	HD80C95	
MM80C97	Fairchild	F40097	
	Harris	HD80C97	
	Motorola	MC14503	
MM80C98	Fairchild	F40098	
♦NH00011	Fairchild	SH2001	
		SH2002	
♦NH00016	Fairchild	SH2200	
♦NH00017	Fairchild	SH2200	
♦NH00018	Fairchild	SH2200	
♦SM3611	National	DS3611	

NEC America

μPB10100	Fairchild	F10100
	Motorola	MC10100
	Plessey	SP10100
	Signetics	10100
μPB10101	Fairchild	F10101
	Hitachi	HD10101
	Motorola	MC10101
	Plessey	SP10101
	Signetics	10101
μPB10102	Fairchild	F10102
	Hitachi	HD10102
	Motorola	MC10102
	Plessey	SP10102
	Signetics	10102
μPB10103	Fairchild	F10103
	Motorola	MC10103
	Plessey	SP10103
	Signetics	10103
μPB10105	Fairchild	F10105
	Hitachi	HD10105
	Motorola	MC10105
	National	DM10105
	Plessey	SP10105
	Signetics	10105
μPB10106	Fairchild	F10106
	Hitachi	HD10106
	Motorola	MC10106
	National	DM10106
	Plessey	SP10106
	Signetics	10106
μPB10107	Fairchild	F10107
	Hitachi	HD10107
	Motorola	MC10107
	Plessey	SP10107
	Signetics	10107
μPB10109	Fairchild	F10109
	Hitachi	HD10109
	Motorola	MC10109
	National	DM10109
	Plessey	SP10109
	Signetics	10109
μPB10110	Fairchild	F10110
	Hitachi	HD10110
	Motorola	MC10110
	Plessey	SP10110

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

NEC America (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
μPB10110	Signetics	10110	
μPB10111	Fairchild	F10111	
	Hitachi	HD10111	
	Motorola	MC10111	
	National	DM10111	
	Plessey	SP10111	
	Signetics	10111	
μPB10115	Fairchild	F10115	
	Motorola	MC10115	
	National	DM10115	
	Plessey	SP10115	
	Signetics	10115	
μPB10117	Fairchild	F10117	
	Hitachi	HD10117	
	Motorola	MC10117	
	National	DM10117	
	Plessey	SP10117	
	Signetics	10117	
μPB10118	Fairchild	F10118	
	Hitachi	HD10118	
	Motorola	MC10118	
	National	DM10118	
	Plessey	SP10118	
	Signetics	10118	
μPB10124	Fairchild	F10124	
	Hitachi	HD10124	
	Motorola	MC10124	
	National	DM10124	
	Plessey	SP10124	
	Signetics	10124	
μPB10131	Fairchild	F10131	
	Hitachi	HD10131	
	Motorola	MC10131	
	Plessey	SP10131	
	Signetics	10131	
μPB10133	Fairchild	F10133	
	Hitachi	HD10133	
	Motorola	MC10133	
	Plessey	SP10133	
	Signetics	10133	
μPB10142	Plessey	SP10142	
	TI	SN10102	
μPB10144	Motorola	MC10144	
	Plessey	SP10144	
	Raytheon	RC10144	
	Signetics	10144	
	TI	SN10144	
μPB10148	Hitachi	HD10148	
	Plessey	SP10148	
	Signetics	10148	
	TI	SN10148	
μPB10158	Fairchild	F10158	
	Motorola	MC10158	
	Signetics	10158	
μPB10161	Fairchild	F10161	
	Hitachi	HD10161	
	Motorola	MC10161	
	Plessey	SP10161	
	Signetics	10161	
μPB10162	Fairchild	F10162	
	Hitachi	HD10162	
	Motorola	MC10162	
	Plessey	SP10162	
	Signetics	10162	
μPB10164	Fairchild	F10164	
	Hitachi	HD10164	
	Motorola	MC10164	
	Plessey	SP10164	
	Signetics	10164	
	TI	SN10164	
μPB10174	Fairchild	F10174	
	Hitachi	HD10174	
	Motorola	MC10174	
	Plessey	SP10174	
	Signetics	10174	
	TI	SN10174	
μPB10180	Fairchild	F10180	
	Hitachi	HD10180	
	Motorola	MC10180	
	Plessey	SP10180	
	Signetics	10180	
μPB10181	Fairchild	F10181	
	Hitachi	HD10181	
μPB10181	Motorola	MC10181	
	Plessey	SP10181	
	Signetics	10181	
μPB74H00	Fairchild	74H00	
	National	DM74H00	
	Raytheon	74H00	
	Signetics	74H00	
	TI	SN74H00	
μPB74H01	Fairchild	74H01	
	ITT	ITT74H01	
	National	DM74H01	
	Raytheon	74H01	
	Signetics	74H01	
	TI	SN74H01	
μPB74H04	Fairchild	74H04	
	ITT	ITT74H04	
	National	DM74H04	
	Raytheon	74H04	
	Signetics	74H04	
	TI	SN74H04	
μPB74H10	Fairchild	74H10	
	ITT	ITT74H10	
	National	DM74H10	
	Raytheon	74H10	
	Signetics	74H10	
	TI	SN74H10	
μPB74H20	Fairchild	74H20	
	ITT	ITT74H20	
	National	DM74H20	
	Raytheon	74H20	
	Signetics	74H20	
	TI	SN74H20	
μPB74H30	Fairchild	74H30	
	ITT	ITT74H30	
	National	DM74H30	
	Signetics	74H30	
	TI	SN74H30	
μPB74H40	Fairchild	74H40	
	ITT	ITT74H40	
	National	DM74H40	
	Raytheon	74H40	
	Signetics	74H40	
	TI	SN74H40	
μPB74H51	Fairchild	74H51	
	ITT	ITT74H51	
	National	DM74H51	
	Signetics	74H51	
	TI	SN74H51	
μPB74LS00	Fairchild	74LS00	
	ITT	ITT74LS00	
	Motorola	SN74LS00	
	National	DM74LS00	
	Raytheon	74LS00	
	Signetics	74LS00	
	TI	SN74LS00	
μPB74LS02	Fairchild	74LS02	
	ITT	ITT74LS02	
	Motorola	SN74LS02	
	National	DM74LS02	
	Raytheon	74LS02	
	Signetics	74LS02	
	TI	SN74LS02	
μPB74LS03	Fairchild	74LS03	
	ITT	ITT74LS03	
	Motorola	SN74LS03	
	National	DM74LS03	
	Raytheon	74LS03	
	Signetics	74LS03	
	TI	SN74LS03	
μPB74LS04	Fairchild	74LS04	
	ITT	ITT74LS04	
	Motorola	SN74LS04	
	National	DM74LS04	
	Raytheon	74LS04	
	Signetics	74LS04	
	TI	SN74LS04	
μPB74LS05	Fairchild	74LS05	
	ITT	ITT74LS05	
	Motorola	SN74LS05	
	National	DM74LS05	
	Raytheon	74LS05	
	Signetics	74LS05	
	TI	SN74LS05	
μPB74LS08	Fairchild	74LS08	
	ITT	ITT74LS08	
	Motorola	SN74LS08	
μPB74LS08	National	DM74LS08	
	Raytheon	74LS08	
	Signetics	74LS08	
	TI	SN74LS08	
μPB74LS10	Fairchild	74LS10	
	ITT	ITT74LS10	
	Motorola	SN74LS10	
	National	DM74LS10	
	Raytheon	74LS10	
	Signetics	74LS10	
	TI	SN74LS10	
μPB74LS109	Fairchild	74LS109	
	ITT	ITT74LS109A	
	Motorola	SN74LS109	
	National	DM74LS109	
	Raytheon	74LS109	
	Signetics	74LS109	
	TI	SN74LS109	
μPB74LS11	Fairchild	74LS11	
	ITT	ITT74LS11	
	Motorola	SN74LS11	
	National	DM74LS11	
	Raytheon	74LS11	
	Signetics	74LS11	
	TI	SN74LS11	
μPB74LS112	Fairchild	74LS112	
	ITT	ITT74LS112	
	National	DM74LS112	
	Raytheon	74LS112	
	Signetics	74LS112	
	TI	SN74LS112	
μPB74LS113	Fairchild	74LS113	
	ITT	ITT74LS113	
	National	DM74LS113	
	Raytheon	74LS113	
	Signetics	74LS113	
	TI	SN74LS113	
μPB74LS138	AMD	SN74LS138	
	Fairchild	74LS138	
	ITT	ITT74LS138	
	Motorola	SN74LS138	
	National	DM74LS138	
	Raytheon	74LS138	
	Signetics	74LS138	
	TI	SN74LS138	
μPB74LS139	AMD	SN74LS139	
	Fairchild	74LS139	
	ITT	ITT74LS139	
	Motorola	SN74LS139	
	National	DM74LS139	
	Raytheon	74LS139	
	Signetics	74LS139	
	TI	SN74LS139	
μPB74LS151	AMD	SN74LS151	
	Fairchild	74LS151	
	ITT	ITT74LS151	
	Motorola	SN74LS151	
	National	DM74LS151	
	Raytheon	74LS151	
	Signetics	74LS151	
	TI	SN74LS151	
μPB74LS153	AMD	SN74LS153	
	Fairchild	74LS153	
	ITT	ITT74LS153	
	Motorola	SN74LS153	
	National	DM74LS153	
	Raytheon	74LS153	
	Signetics	74LS153	
	TI	SN74LS153	
μPB74LS155	Fairchild	74LS155	
	ITT	ITT74LS155	
	Motorola	SN74LS155	
	National	DM74LS155	
	Raytheon	74LS155	
	Signetics	74LS155	
	TI	SN74LS155	
μPB74LS157	AMD	SN74LS157	
	Fairchild	74LS157	
	ITT	ITT74LS157	
	Motorola	SN74LS157	
	National	DM74LS157	
	Raytheon	74LS157	
	Signetics	74LS157	
	TI	SN74LS157	
μPB74LS161	AMD	SN74LS161	
	Fairchild	74LS161	
μPB74LS161	ITT	ITT74LS161	
	Motorola	SN74LS161	
	National	DM74LS161	
	Raytheon	74LS161	
	Signetics	74LS161	
	TI	SN74LS161	
μPB74LS164	AMD	SN74LS164	
	Fairchild	74LS164	
	ITT	ITT74LS164	
	Motorola	SN74LS164	
	National	DM74LS164	
	Raytheon	**74LS164**	**272**
	Signetics	74LS164	
	TI	SN74LS164	
μPB74LS175	AMD	SN74LS175	
	Fairchild	74LS175	
	ITT	ITT74LS175	
	Motorola	SN74LS175	
	National	DM74LS175	
	Raytheon	74LS175	
	Signetics	74LS175	
	TI	SN74LS175	
μPB74LS192	AMD	SN74LS192	
	Fairchild	74LS192	
	ITT	ITT74LS192	
	Motorola	SN74LS192	
	National	DM74LS192	
	Raytheon	74LS192	
	Signetics	74LS192	
	TI	SN74LS192	
μPB74LS193	AMD	SN74LS193	
	Fairchild	74LS193	
	ITT	ITT74LS193	
	Motorola	SN74LS193	
	National	DM74LS193	
	Raytheon	74LS193	
	Signetics	74LS193	
	TI	SN74LS193	
μPB74LS194	AMD	SN74LS194A	
	Fairchild	74LS194	
	ITT	ITT74LS194A	
	Motorola	SN74LS194	
	Raytheon	74LS194A	
	Signetics	74LS194A	
	TI	SN74LS194A	
μPB74LS195	AMD	SN74LS195A	
	Fairchild	74LS195	
	ITT	ITT74LS195A	
	Motorola	SN74LS195	
	Raytheon	74LS195A	
	Signetics	74LS195A	
	TI	SN74LS195A	
μPB74LS20	Fairchild	74LS20	
	ITT	ITT74LS20	
	Motorola	SN74LS20	
	National	DM74LS20	
	Raytheon	74LS20	
	Signetics	74LS20	
	TI	SN74LS20	
μPB74LS21	Fairchild	74LS21	
	ITT	ITT74LS21	
	Motorola	SN74LS21	
	National	DM74LS21	
	Raytheon	74LS21	
	Signetics	74LS21	
	TI	SN74LS21	
μPB74LS251	AMD	SN74LS251	
	Fairchild	74LS251	
	ITT	ITT74LS251	
	Motorola	SN74LS251	
	National	DM74LS251	
	Raytheon	74LS251	
	Signetics	74LS251	
	TI	SN74LS251	
μPB74LS253	AMD	SN74LS253	
	Fairchild	74LS253	
	ITT	ITT74LS253	
	Motorola	SN74LS253	
	National	DM74LS253	
	Raytheon	74LS253	
	Signetics	74LS253	
	TI	SN74LS253	
μPB74LS257	AMD	SN74LS257	
	Fairchild	74LS257	
	ITT	ITT74LS257	
	Motorola	SN74LS257	

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Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
μPB74LS257	National	DM74LS257	
	Raytheon	74LS257	
	Signetics	74LS257	
	TI	SN74LS257	
μPB74LS258	AMD	SN74LS258	
	Fairchild	74LS258	
	ITT	ITT74LS258	
	Motorola	SN74LS258	
	National	DM74LS258	
	Raytheon	74LS258	
	Signetics	74LS258	
	TI	SN74LS258	
μPB74LS27	Fairchild	74LS27	
	ITT	ITT74LS27	
	Motorola	SN74LS27	
	National	DM74LS27	
	Raytheon	74LS27	
	Signetics	74LS27	
	TI	SN74LS27	
μPB74LS279	Fairchild	74LS279	
	ITT	ITT74LS279	
	Motorola	SN74LS279	
	National	DM74LS279	
	Raytheon	74LS279	
	Signetics	74LS279	
	TI	SN74LS279	
μPB74LS295	Fairchild	74LS295	
	Motorola	SN74LS295	
	Raytheon	74LS295A	
	Signetics	74LS295	
	TI	SN74LS295B	
μPB74LS30	Fairchild	74LS30	
	ITT	ITT74LS30	
	Motorola	SN74LS30	
	National	DM74LS30	
	Raytheon	74LS30	
	Signetics	74LS30	
	TI	SN74LS30	
μPB74LS32	Fairchild	74LS32	
	ITT	ITT74LS32	
	Motorola	SN74LS32	
	National	DM74LS32	
	Raytheon	74LS32	
	Signetics	74LS32	
	TI	SN74LS32	
μPB74LS365	Fairchild	74LS365	
	ITT	ITT74LS365	
	Motorola	SN74LS365	
	National	DM74LS365	
	Raytheon	**74LS365**	**286**
	Signetics	74LS365	
	TI	SN74LS365	
μPB74LS366	Fairchild	74LS366	
	ITT	ITT74LS366	
	Motorola	SN74LS366	
	National	DM74LS366	
	Raytheon	**74LS366**	**286**
	Signetics	74LS366	
	TI	SN74LS366	
μPB74LS367	Fairchild	74LS367	
	ITT	ITT74LS367	
	Motorola	SN74LS367	
	National	DM74LS367	
	Raytheon	**74LS367**	**286**
	Signetics	74LS367	
	TI	SN74LS367	
μPB74LS368	Fairchild	74LS368	
	ITT	ITT74LS368	
	Motorola	SN74LS368	
	National	DM74LS368	
	Raytheon	**74LS368**	**286**
	Signetics	74LS368	
	TI	SN74LS368	
μPB74LS37	Fairchild	74LS37	
	ITT	ITT74LS37	
	Motorola	SN74LS37	
	National	DM74LS37	
	Raytheon	74LS37	
	Signetics	74LS37	
	TI	SN74LS37	
μPB74LS375	ITT	ITT74LS375	
	Motorola	SN74LS375	
	Raytheon	74LS375	
μPB74LS375	Signetics	74LS375	
	TI	SN74LS375	
μPB74LS38	Fairchild	74LS38	
	ITT	ITT74LS38	
	Motorola	SN74LS38	
	National	DM74LS38	
	Raytheon	74LS38	
	Signetics	74LS38	
	TI	SN74LS38	
μPB74LS40	Fairchild	74LS40	
	ITT	ITT74LS40	
	Motorola	SN74LS40	
	National	DM74LS40	
	Raytheon	74LS40	
	Signetics	74LS40	
	TI	SN74LS40	
μPB74LS42	Fairchild	74LS42	
	ITT	ITT74LS42	
	Motorola	SN74LS42	
	National	DM74LS42	
	Raytheon	**74LS42**	**266**
	Signetics	74LS42	
	TI	SN74LS42	
μPB74LS51	Fairchild	74LS51	
	ITT	ITT74LS51	
	Motorola	SN74LS51	
	National	DM74LS51	
	Raytheon	74LS51	
	Signetics	74LS51	
	TI	SN74LS51	
μPB74LS54	Fairchild	74LS54	
	ITT	ITT74LS54	
	Motorola	SN74LS54	
	National	DM74LS54	
	Raytheon	74LS54	
	Signetics	74LS54	
	TI	SN74LS54	
μPB74LS55	Fairchild	74LS55	
	Motorola	SN74LS55	
	National	DM74LS55	
	Raytheon	74LS55	
	Signetics	74LS55	
	TI	SN74LS55	
μPB74LS74	Fairchild	74LS74	
	ITT	ITT74LS74	
	Motorola	SN74LS74	
	National	DM74LS74	
	Raytheon	74LS74	
	Signetics	74LS74	
	TI	SN74LS74	
μPB74LS86	Fairchild	74LS86	
	ITT	ITT74LS86	
	Motorola	SN74LS86	
	Raytheon	74LS86	
	Signetics	74LS86	
	TI	SN74LS86	
μPB7400	Fairchild	7400	
	Hitachi	HD7400	
	ITT	ITT7400	
	Mitsubishi	M53200	
	Motorola	MC7400	
	National	DM7400	
	Raytheon	7400	
	Signetics	7400	
	TI	SN7400	
	Toshiba	TC7400	
	TRW	7400	
μPB7402	Fairchild	7402	
	Hitachi	HD7402	
	ITT	ITT7402	
	Mitsubishi	M53202	
	Motorola	MC7402	
	National	DM7402	
	Signetics	7402	
	TI	SN7402	
	TRW	7402	
μPB7404	Fairchild	7404	
	Hitachi	HD7404	
	ITT	ITT7404	
	Mitsubishi	M53204	
	Motorola	MC7404	
	National	DM7404	
	Raytheon	7404	
	Signetics	7404	
	TI	SN7404	
	Toshiba	TC7404	
μPB7404	TRW	7404	
μPB7405	Fairchild	7405	
	Hitachi	HD7405	
	ITT	ITT7405	
	Mitsubishi	M53205	
	Motorola	MC7405	
	National	DM7405	
	Raytheon	7405	
	Signetics	7405	
	TI	SN7405	
	TRW	7405	
μPB7410	Fairchild	7410	
	Hitachi	HD7410	
	ITT	ITT7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
	National	DM7410	
	Raytheon	7410	
	Signetics	7410	
	TI	SN7410	
		SN7427	
	Toshiba	TC7410	
	TRW	7410	
μPB74105	Fairchild	74105	
μPB74107	Fairchild	74107	
	Hitachi	HD74107	
	ITT	ITT74107	
	Mitsubishi	M53307	
	Motorola	MC74107	
	National	DM74107	
	Signetics	74107	
	TI	SN74107	
μPB74123	AMD	SN74123	
	Fairchild	74123	
	ITT	ITT74123	
	Mitsubishi	M53323	
	Motorola	MC74123	
	National	DM74123	
	Raytheon	74123	
	Signetics	74123	
	TI	SN74123	
	TRW	74123	
μPB7413	Fairchild	7413	
	ITT	ITT7413	
	Mitsubishi	M53213	
	Motorola	MC7413	
	National	DM7413	
	Signetics	7413	
	TI	SN7413	
	TRW	7413	
μPB74141	Fairchild	74141	
	ITT	ITT74141	
	Motorola	MC74141	
	National	DM74141	
	TI	SN74141	
μPB74147	Hitachi	HD74147	
	Mitsubishi	M53347	
	National	DM74147	
	Signetics	74147	
	TI	SN74147	
μPB74148	Hitachi	HD74148	
	Mitsubishi	M53348	
	National	DM74148	
	Signetics	74148	
	TI	SN74148	
μPB74150	Fairchild	74150	
	Hitachi	HD74150	
	ITT	ITT74150	
	Mitsubishi	M53350	
	Motorola	MC74150	
	National	DM74150	
	Raytheon	74150	
	Signetics	74150	
	TI	SN74150	
	Toshiba	TC74	
	TRW	74150	
μPB74151	Fairchild	74151	
	Hitachi	HD74151	
	ITT	ITT74151	
	Mitsubishi	M53351	
	Motorola	MC74151	
	National	DM74151	
	Raytheon	74151	
	Signetics	74151	
	TI	SN74151	
	TRW	74151	
μPB74153	Fairchild	74153	
	ITT	ITT74153	
	Mitsubishi	M53353	
	Motorola	MC74153	
	National	DM74153	
	Raytheon	74153	
	Signetics	74153	
	TI	SN74153	
	TRW	74153	
μPB74154	AMD	SN74154	
	Fairchild	74154	
	ITT	ITT74154	
	Mitsubishi	M53354	
	Motorola	MC74154	
	National	DM74154	
	Raytheon	74154	
	Signetics	74154	
	TI	SN74154	
	TRW	74154	
μPB74155	Fairchild	74155	
	ITT	ITT74155	
	Mitsubishi	M53355	
	Motorola	MC74155	
	National	DM74155	
	Raytheon	74155	
	Signetics	74155	
	TI	SN74155	
	TRW	74155	
μPB74156	Fairchild	74156	
	Hitachi	HD74156	
	ITT	ITT74156	
	Mitsubishi	M53356	
	Motorola	MC74156	
	National	DM74156	
	Raytheon	74156	
	Signetics	74156	
	TI	SN74156	
	TRW	74156	
μPB74157	AMD	SN74157	
	Fairchild	74157	
	Hitachi	HD74157	
	ITT	ITT74157	
	Mitsubishi	M53357	
	Motorola	MC74157	
	National	DM74157	
	Raytheon	74157	
	Signetics	74157	
	TI	SN74157	
μPB74161	AMD	SN74161	
	Fairchild	74161	
	Hitachi	HD74161	
	ITT	ITT74161	
	Mitsubishi	M53361	
	Motorola	MC74161	
	National	DM74161	
	Raytheon	74161	
	Signetics	74161	
	TI	SN74161	
	TRW	74161	
μPB74164	AMD	74164	
	Fairchild	74164	
	Hitachi	HD74164	
	ITT	ITT74164	
	Mitsubishi	M53364	
	National	DM74164	
	Raytheon	74164	
	Signetics	74164	
	TI	SN74164	
μPB74170	Fairchild	74170	
	Mitsubishi	M53370	
	National	DM74170	
	Raytheon	74170	
	Signetics	74170	
	TI	SN74170	
μPB74175	AMD	SN74175	
	Fairchild	74175	
	Hitachi	HD74175	
	Mitsubishi	M53375	
	Motorola	MC74175	
	National	DM74175	
	Raytheon	74175	
	Signetics	74175	
	TI	SN74175	
μPB74180	Fairchild	74180	
	Hitachi	HD74180	
	ITT	ITT74180	

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The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
μPB74180	Mitsubishi	M53380	
	Motorola	MC74180	
	National	DM74180	
	Raytheon	74180	
	Signetics	74180	
	TI	SN74180	
	TRW	74180	
μPB74181	AMD	SN74181	
	Fairchild	74181	
	Mitsubishi	M53381	
	Motorola	MC74181	
	National	DM74181	
	Raytheon	74181	
	Signetics	74181	
	TI	SN74181	
μPB74182	AMD	SN74182	
	Fairchild	74182	
	ITT	ITT74182	
	Mitsubishi	M53382	
	Motorola	MC74182	
	National	DM74182	
	Raytheon	74182	
	Signetics	74182	
	TI	SN74182	
μPB74192	AMD	SN74192	
	Fairchild	74192	
	ITT	ITT74192	
	Mitsubishi	M53392	
	Motorola	MC74192	
	National	DM74192	
	Raytheon	74192	
	Signetics	74192	
	TI	SN74192	
μPB74193	AMD	SN74193	
	Fairchild	74193	
	ITT	ITT74193	
	Mitsubishi	M53393	
	Motorola	MC74193	
	National	DM74193	
	Raytheon	74193	
	Signetics	74193	
	TI	SN74193	
μPB74195	AMD	SN74195	
	Fairchild	74195	
	ITT	ITT74195	
	Motorola	MC74195	
	National	DM74195	
	Raytheon	74195	
	Signetics	74195	
	TI	SN74195	
μPB74198	Fairchild	74198	
	Hitachi	HD74198	
	Mitsubishi	M53398	
	National	DM74198	
	Raytheon	74198	
	Signetics	74198	
	TI	SN74198	
μPB7420	Fairchild	7420	
	Hitachi	HD7420	
	ITT	ITT7420	
	Mitsubishi	M53220	
	Motorola	MC7420	
	National	DM7420	
	Raytheon	7420	
	Signetics	7420	
	TI	SN7420	
	Toshiba	TC7420	
	TRW	7420	
μPB74283	Fairchild	74283	
	Mitsubishi	M53483	
	Raytheon	74283	
	TI	SN74283	
μPB7430	Fairchild	7430	
	Hitachi	HD7430	
	ITT	ITT7430	
	Mitsubishi	M53230	
	Motorola	MC7430	
	National	DM7430	
	Signetics	7430	
	TI	SN7430	
	TRW	7430	
μPB7437	Fairchild	7437	
	ITT	ITT7437	
μPB7437	Mitsubishi	M53237	
	Motorola	MC7437	
	National	DM7437	
	Raytheon	7437	
	Signetics	7437	
	TI	SN7437	
	TRW	7437	
μPB7438	Fairchild	7438	
	ITT	ITT7438	
	Mitsubishi	M53238	
	Motorola	MC7438	
	National	DM7438	
	Raytheon	7438	
	Signetics	7438	
	TI	SN7438	
	TRW	7438	
μPB7440	Fairchild	7440	
	Hitachi	HD7440	
	ITT	ITT7440	
	Mitsubishi	M53240	
	Motorola	MC7440	
	National	DM7440	
	Signetics	7440	
	TI	SN7440	
	TRW	7440	
μPB7442	Fairchild	7442	
	Hitachi	HD7442	
	ITT	ITT7442	
	Mitsubishi	M53242	
	Motorola	MC7442	
	National	DM7442	
	Raytheon	7442	
	Signetics	7442	
	TI	SN7442	
μPB7445	Fairchild	7445	
	ITT	ITT7445	
	Mitsubishi	M53245	
	Motorola	MC7445	
	National	DM7445	
	Raytheon	7445	
	Signetics	7445	
	TI	SN7445	
	TRW	7445	
μPB7447	Fairchild	7447	
	ITT	ITT7447	
	Mitsubishi	M53247	
	Motorola	MC7447	
	National	DM7447	
	Signetics	7447	
	TI	SN7447	
μPB7450	Fairchild	7450	
	Hitachi	HD7450	
	ITT	ITT7450	
	Mitsubishi	M53250	
	Motorola	MC7450	
	National	DM7450	
	Signetics	7450	
	TI	SN7450	
	TRW	7450	
μPB7451	Fairchild	7451	
	Hitachi	HD7451	
	ITT	ITT7451	
	Motorola	MC7451	
	National	DM7451	
	Signetics	7451	
	TI	SN7451	
	TRW	7451	
μPB7453	Fairchild	7453	
	Hitachi	HD7453	
	ITT	ITT7453	
	Mitsubishi	M53253	
	Motorola	MC7453	
	National	DM7453	
	Signetics	7453	
	TI	SN7453	
	TRW	7453	
μPB7454	Fairchild	7454	
	Hitachi	HD7454	
	ITT	ITT7454	
	Motorola	MC7454	
	National	DM7454	
	Signetics	7454	
	TI	SN7454	
	TRW	7454	
μPB7460	Fairchild	7460	
	Hitachi	HD7460	
μPB7460	Mitsubishi	M53260	
	Motorola	MC7460	
	National	DM7460	
	Signetics	7460	
	TI	SN7460	
	TRW	7460	
μPB7473	Fairchild	7473	
	ITT	ITT7473	
	Mitsubishi	M53273	
	Motorola	MC7473	
	National	DM7473	
	Signetics	7473	
	TI	SN7473	
μPB7474	Fairchild	7474	
	Hitachi	HD7474	
	ITT	ITT7474	
	Mitsubishi	M53274	
	Motorola	MC7474	
	National	DM7474	
	Raytheon	7474	
	Signetics	7474	
	TI	SN7474	
	TRW	7474	
μPB7476	Fairchild	7476	
	ITT	ITT7476	
	Mitsubishi	M53276	
	Motorola	MC7476	
	National	DM7476	
	Signetics	7476	
	TI	SN7476	
	TRW	7476	
μPB7480	Fairchild	7480	
	ITT	ITT7480	
	Mitsubishi	M53280	
	Motorola	MC7480	
	Signetics	7480	
	TI	SN7480	
μPB7485	Fairchild	7485	
	Hitachi	HD7485	
	Mitsubishi	M53285	
	Motorola	MC7485	
	National	DM7485	
	Signetics	7485	
	TI	SN7485	
	TRW	7485	
μPB7486	Fairchild	7486	
	Hitachi	HD7486	
	ITT	ITT7486	
	Mitsubishi	M53286	
	Motorola	MC7486	
	National	DM7486	
	Raytheon	7486	
	Signetics	7486	
	TI	SN7486	
	TRW	7486	
μPB7491	Fairchild	7491	
	ITT	ITT7491	
	Mitsubishi	M53291	
	Motorola	MC7491	
	National	DM7491	
	Signetics	7491	
	TI	SN7491	
μPD4001	Fairchild	F4001	
	Mitel	SIL4001	
	Motorola	MC14001	
	National	CD4001	
	RCA	CD4001	
	SGS	HBF4001	
	Solitron	CM4001	
	SSS	SCL4001	
	TI	TP4001	
	Toshiba	TC4001	
μPD4002	Fairchild	F4002	
	Mitel	SIL4002	
	Motorola	MC14002	
	National	CD4002	
	RCA	CD4002	
	SGS	HBF4002	
	Solitron	CM4002	
	SSS	SCL4002	
	TI	TP4002	
	Toshiba	TC4002	
μPD4011	Fairchild	F4011	
	Mitel	SIL4011	
	Motorola	MC14011	
	National	CD4011	
μPD4011	RCA	CD4011	
	SGS	HBF4011	
	Solitron	CM4011	
	SSS	SCL4011	
	TI	TP4011	
	Toshiba	TC4011	
μPD4012	Fairchild	F4012	
	Mitel	SIL4012	
	Motorola	MC14012	
	National	CD4012	
	RCA	CD4012	
	SGS	HBF4012	
	Solitron	CM4012	
	SSS	SCL4012	
	TI	TP4012	
	Toshiba	TC4012	
μPD4013	Fairchild	F4013	
	Mitel	SIL4013	
	Motorola	MC14013	
	National	CD4013	
	RCA	CD4013	
	SGS	HBF4013	
	Solitron	CM4013	
	SSS	SCL4013	
	TI	TP4013	
	Toshiba	TC4013	
μPD4014	Fairchild	F4014	
	Mitel	SIL4014	
	Motorola	MC14014	
	National	CD4014	
	RCA	CD4014	
	SGS	HBF4014	
	Solitron	CM4014	
	SSS	SCL4014	
	TI	TP4014	
	Toshiba	TC4014	
μPD4015	Fairchild	F4015	
	Mitel	SIL4015	
	Motorola	MC14015	
	National	CD4015	
	RCA	CD4015	
	SGS	HBF4015	
	Solitron	CM4015	
	SSS	SCL4015	
	TI	TP4015	
	Toshiba	TC4015	
μPD4017	Fairchild	F4017	
	Mitel	SIL4017	
	Motorola	MC14017	
	National	CD4017	
	RCA	CD4017	
	SGS	HBF4017	
	Solitron	CM4017	
	SSS	SCL4017	
	TI	TP4017	
	Toshiba	TC4017	
μPD4020	Fairchild	F4020	
	Mitel	SIL4020	
	Motorola	MC14020	
	National	CD4020	
	RCA	CD4020	
	SGS	HBF4020	
	Solitron	CM4020	
	SSS	SCL4020	
	TI	TP4020	
	Toshiba	TC4020	
μPD4021	Fairchild	F4021	
	Mitel	SIL4021	
	Motorola	MC14021	
	National	CD4021	
	RCA	CD4021	
	Solitron	CM4021	
	SSS	SCL4021	
	TI	TP4021	
	Toshiba	TC4021	
μPD4023	Fairchild	F4023	
	Mitel	SIL4023	
	Motorola	MC14023	
	National	CD4023	
	RCA	CD4023	
	SGS	HBF4023	
	Solitron	CM4023	
	SSS	SCL4023	
	TI	TP4023	
	Toshiba	TC4023	
μPD4025	Fairchild	F4025	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

NEC America (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
μPD4025	Mitel	SIL4025	
	Motorola	MC14025	
	National	CD4025	
	RCA	CD4025	
	SGS	HBF4025	
	Solitron	CM4025	
	SSS	SCL4025	
	TI	TP4025	
	Toshiba	TC4025	
μPD4027	Fairchild	F4027	
	Mitel	SIL4027	
	Motorola	MC14027	
	National	CD4027	
	RCA	CD4027	
	SGS	HBF4027	
	Solitron	CM4027	
	SSS	SCL4027	
	TI	TP4027	
	Toshiba	TC4027	
μPD4028	Fairchild	F4028	
	Mitel	SIL4028	
	Motorola	MC14028	
	National	CD4028	
	RCA	CD4028	
	SGS	HBF4028	
	Solitron	CM4028	
	SSS	SCL4028	
	TI	TP4028	
	Toshiba	TC4028	
μPD4029	Fairchild	F4029	
	Mitel	SIL4029	
	National	CD4029	
	RCA	CD4029	
	SGS	HBF4029	
	Solitron	CM4029	
	SSS	SCL4029	
	TI	TP4029	
	Toshiba	TC4029	
μPD4030	Fairchild	F4030	
	Mitel	SIL4030	
	National	CD4030	
	RCA	CD4030	
	SGS	HBF4030	
	Solitron	CM4030	
	SSS	SCL4030	
	TI	TP4030	
	Toshiba	TC4030	
μPD4035	Fairchild	F4035	
	Mitel	SIL4035	
	Motorola	MC14035	
	National	CD4035	
	RCA	CD4035	
	SGS	HBF4035	
	Solitron	CM4035	
	SSS	SCL4035	
	TI	TP4035	
	Toshiba	TC4035	
μPD4040	Fairchild	F4040	
	Mitel	SIL4040	
	National	CD4040	
	RCA	CD4040	
	Solitron	CM4040	
	SSS	SCL4040	
	TI	TP4040	
	Toshiba	TC4040	
μPD4042	Fairchild	F4042	
	Mitel	SIL4042	
	Motorola	MC14042	
	National	CD4042	
	RCA	CD4042	
	SGS	HBF4042	
	Solitron	CM4042	
	SSS	SCL4042	
	TI	TP4042	
	Toshiba	TC4042	
μPD4043	Fairchild	F4043	
	Mitel	SIL4043	
	Motorola	MC14043	
	National	CD4043	
	RCA	CD4043	
	Solitron	CM4043	
	SSS	SCL4043	
	TI	TP4043	
μPD4043	Toshiba	TC4043	
μPD4044	Fairchild	F4044	
	Mitel	SIL4044	
	Motorola	MC14044	
	National	CD4044	
	RCA	CD4044	
	Solitron	CM4044	
	SSS	SCL4044	
	TI	TP4044	
	Toshiba	TC4044	
μPD4049	Fairchild	F4049	
	Mitel	SIL4049	
	Motorola	MC14049	
	National	CD4049	
	RCA	CD4049	
	SGS	HBF4049	
	Solitron	CM4049	
	SSS	SCL4049	
	TI	TP4049	
	Toshiba	TC4049	
μPD4050	Fairchild	F4050	
	Mitel	SIL4050	
	Motorola	MC14050	
	National	CD4050	
	RCA	CD4050	
	SGS	HBF4050	
	Solitron	CM4050	
	SSS	SCL4050	
	TI	TP4050	
	Toshiba	TC4050	
μPD4063	RCA	CD4063	
μPD4066	Fairchild	F4066	
	Mitel	SIL4066	
	Motorola	MC14066	
	National	CD4066	
	RCA	CD4066	
	SGS	HBF4066	
	Signetics	N4066	
	Solitron	CM4066	
	SSS	SCL4066	
	Toshiba	TC4066	
μPD4069	Fairchild	F4069	
	Harris	HD74C04	
	Mitel	SIL4069	
	Motorola	MC14069	
	National	CD4069	
		MM74C04	
	RCA	CD4069	
	Solitron	CM4069	
	SSS	SCL4069	
	TI	TP4069	
	Toshiba	TC4069	
μPD4071	Fairchild	F4071	
	Mitel	SIL4071	
	Motorola	MC14071	
	National	CD4071	
	RCA	CD4071	
	Solitron	CM4071	
	SSS	SCL4071	
	TI	TP4071	
	Toshiba	TC4071	
μPD4081	Fairchild	F4081	
	Mitel	SIL4081	
	Motorola	MC14081	
	National	CD4081	
	RCA	CD4081	
	Solitron	CM4081	
	SSS	SCL4081	
	TI	TP4081	
	Toshiba	TC4081	
μPD4512	Fairchild	F4512	
	Mitel	SIL4512	
	Motorola	MC14512	
	National	CD4512	
	SSS	SCL4512	
	TI	TP4512	
	Toshiba	TC4512	
μPD4519	Fairchild	F4519	
	Motorola	MC14519	
	National	CD4519	
	RCA	CD4019	
	TI	TP4519	
μPD4520	Fairchild	F4520	
	Mitel	SIL4520	
	Motorola	MC14520	
	National	CD4520	
μPD4520	RCA	CD4520	
	Solitron	CM4520	
	SSS	SCL4520	
	TI	TP4520	
	Toshiba	TC4520	
μPD4528	Fairchild	F4528	
	Motorola	MC14528	
	National	CD4528	
	RCA	CD4528	
	SSS	SCL4528	
	Toshiba	TC4528	
μPD4539	Fairchild	F4539	
	Motorola	MC14539	
	Toshiba	TC4539	
μPD4556	Fairchild	F4556	
	Motorola	MC14556	
	RCA	CD4556	
	SSS	SCL4556	

NEC Microcomputers

Manufacturer Device	Replacement Source	Device	IC Master Page
μPB2089	AMD	AM27S02	
		SN7489	
		3101	
	Fairchild	7489	
	Intersil	IM5501	
	National	**DM7489**	**1287**
		MM74S289	
	Signetics	N3101A	
		74S89	
	TI	SN74S289	
		SN7489	
μPB2200	AMD	AM27LS00	
	Intel	3106	
	Intersil	IM5523	
	MMI	6531	
	Signetics	N82S17	
		74S200	
	TI	SN74S301	
μPB2202	Signetics	74S201	
	TI	SN74S201	
μPB2205	AMD	93415M	
	Fairchild	**93415**	**1137**
	Fujitsu	MB93415	
	National	DM93415	
	Signetics	N93415A	
	TI	SN74S314	
μPB2206	AMD	AM27LS01	
	Fairchild	93411	
	Intel	3107	
	Intersil	IM5533	
	MMI	6530	
	Signetics	N82S16	
μPB2289	AMD	SN74S289	
μPB2901	AMD	AM2901A	
	Fairchild	F2901A	
		9409	
	Motorola	MC2901	
	National	**IDM2901A**	
			1656,1680
	Raytheon	AM2901A	
	Signetics	**N2901**	**1851**
μPB2902	Motorola	MC2902	
	National	IDM2902	
	Raytheon	AM2902	
μPB2909	AMD	AM2909	
	Motorola	MC2909	
	National	IDM2909	
	Raytheon	AM2909	
μPB2911	AMD	AM2911	
	Motorola	MC2911	
	National	IDM2911	
	Raytheon	AM2911	
μPB403	AMD	AM27LS10	
	Fairchild	**93417**	**1151**
	Fujitsu	MB7057	
	Harris	**HM7610**	**1192**
		HPROM-1024A	
	Intel	3601	
	Intersil	IM5603	
	MMI	**6300-1**	**1248**
	National	**DM74S387**	**1264**
		DM7535	
	Signetics	N82S126	
		N82S26	
μPB403	TI	SN74S387	
μPB405	**Fairchild**	**93438**	**1151**
	Harris	**HM7640**	**1192**
	Intel	3604	
	Intersil	IM5605	
	MMI	**6340-1**	**1248**
		6348-1	**1248**
	National	**DM77S295**	**1270**
	Signetics	N82S140	
	TI	SN74S475	
μPB406	**Fairchild**	**93452**	**1151**
	Fujitsu	MB7059	
	Harris	**HM7642**	**1192**
	Intel	3605	
	MMI	**6352-1**	**1248**
	National	**DM74S572**	**1268**
	Signetics	N82S136	
μPB408	AMD	AM27S80	
	Intel	3608	
	MMI	**6380-1**	**1248**
μPB410	**EMM/Semi**	**4200**	**1072**
μPB425	**Fairchild**	**93448**	**1151**
	Harris	**HM7641**	**1192**
	Intel	3624	
	Intersil	IM5625	
	MMI	**6341-1**	**1248**
		6349-1	**1248**
	National	**DM77S296**	**1270**
	Signetics	N82S115	
		N82S141	
	TI	SN74S44	
μPB426	**Fairchild**	**93453**	**1151**
	Fujitsu	MB7054	
	Harris	**HM7643**	**1192**
	Intel	3625	
	MMI	**6353-1**	**1248**
	National	**DM74S573**	**1268**
	Signetics	N82S137	
μPB428	AMD	AM27S81	
	Intel	3628	
	MMI	**6381-1**	**1248**
μPB8212	AMD	8212	
	Intel	8212	
	National	**DP8212**	**469**
	TI	SN74S412	
μPB8214	AMD	8214	
	Intel	8214	
μPB8216	AMD	8216	
	Intel	8216	
	National	DP8216	
μPB8224	AMD	8224	
	Intel	8224	
	National	**DP8224**	**477**
	TI	SN74LS424	
μPB8226	AMD	8226	
	Intel	8226	
	National	DP8226	
μPB8228	AMD	8228	
	Intel	8228	
	National	**DP8228**	**483**
	TI	SN74S428	
μPB8238	AMD	8238	
	Intel	8238	
	National	**DP8238**	**483**
	TI	SN74S438	
μPD2089	Intel	3101	
μPD2101	AMD	2101	
	Intel	2101	
μPD2101A	Intel	8101	
	National	MM2101	
	TI	TMS2101	
		TMS4039	
μPD2101AL	AMD	9101	
	Fairchild	3538	
	Fujitsu	MB8101	
	Signetics	2101	
		2601	
μPD2102	AMD	2102	
	Intel	2102	
μPD2102A	Intel	8102	
	Mostek	MK4102	
	National	**MM2102A**	**1300**
	TI	TMS2102	
		TMS4033	
		TMS4034	
μPD2102AL	AMD	9102	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

NEC Microcomputers (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
µPD2102AL	Fairchild	2102	
	Intersil	IM7552	
	Signetics	2102	
µPD2111	AMD	2111	
	Intel	2111	
µPD2111A	Motorola	MCM2111	
		MCM68111	
	National	MM2111	
	TI	TMS4042	
µPD2111AL	AMD	9111	
	Fujitsu	MB8111	
	Intel	8111	
	Signetics	2111	
		2611	
µPD2114	Fujitsu	MB2114	
	Intel	2114	
	Intersil	7114	
	TI	TMS4045	
µPD2308	AMD	9208	
	Fairchild	3508	
	Fujitsu	MB8308	
	Intel	2308	
		8308	
	Mostek	MK30000	
µPD2316	Intel	2316	
		2616	
		8316	
	Mostek	MK34000	
	Signetics	2316	
µPD2316A	Intel	4316	
	Mostek	MK31000	
	National	**MM2316A**	
			1307,1372
µPD2316E	AMD	9216	
	Mostek	MK34000	
	Motorola	MCM68317	
µPD2332	Mostek	MK32000	
	TI	TMS4732	
µPD410	**EMM/Semi**	**4200**	**1072**
		4202	
µPD4104	Mostek	MK4104	
µPD411	AMD	9060	
		9107	
	Fujitsu	MB8107	
	Intel	2107	
	National	**MM4280**	**1314**
		MM5280A	**1339**
		MM5281	
	TI	TMS4060	
µPD414	**Fairchild**	**M4027**	**1118**
		4096	
	Fujitsu	MB8224	
	Intel	2104	
	Mostek	MK4027	
		MK4096	
	Motorola	MCM4027	
		MCM4096	
	TI	TMS4027	
µPD414A	Fujitsu	MB8227	
µPD416	**Fairchild**	**F16K**	**1110**
	Fujitsu	MB8116	
	Intel	2116	
	Intersil	7116	
	Mostek	MK4116	
	Motorola	MCM4116	
	TI	TMS4116	
	Zilog	Z6116	
µPD418	AMD	9050	
	TI	TMS4050	
		TMS4051	
µPD5101	**AMI**	**S5101**	**1041**
	Harris	**HM6501**	**1174**
	Intel	5101	
	National	**MM74C920**	**1361**
µPD6508	**Harris**	**HM6508**	**1180**
	Intersil	IM6508	
µPD8035	**Intel**	**8035**	**1648**
µPD8048	AMD	8048	
	Intel	**8048**	**1648**
	Signetics	8048	
µPD8080AF	AMD	9080A	
	Intel	8080A	
µPD8080AF	**National**	**INS8080A**	
			1656,1670
	Signetics	MP8080A	
	TI	TMS8080A	
µPD8085	AMD	8085	
	Intel	**8085**	**1644**
µPD8155	AMD	8155	
	Intel	8155	
µPD8251	AMD	8251	
	Intel	8251	
	National	INS8251	
µPD8253	Intel	8253	
µPD8255	AMD	8255	
	Intel	8255	
	National	INS8255	
µPD8257	AMD	8257	
	Intel	8257	
µPD8259	Intel	8259	
µPD8355	AMD	8355	
	Intel	**8355**	**1646**
µPD8748	**Intel**	**8748**	**1648**
µPD8755	**Intel**	**8755**	**1646**

Nitron

♦NCM1110	National	MM5231	
	Signetics	2430	
♦NCM1111	Signetics	2461	
♦NCM1112	National	MM5230	
NC1181	AMI	S2567	
NC1182	AMI	S2566	
NC1183	AMI	S2555	
	National	MM5555	
NC1184	AMI	S2556	
	National	MM5556	
♦NC4104A	**EMM/Semi**	**4104A**	**1070**
♦NC4200	**EMM/Semi**	**4200**	**1072**
♦NC4402A	EMM/Semi	4402A	
♦NC4402B	EMM/Semi	4402B	
♦NC4801A	**EMM/Semi**	**4801A**	**1074**
♦NC4804A	**EMM/Semi**	**4804A**	**1074**
NC6560	Motorola	MCM6560	
NC6561	Motorola	MCM6561	
NC6570	Motorola	MCM6570	
NC6571	Motorola	MCM6571	
NC6572	Motorola	MCM6572	
NC6580	Motorola	MCM6580	
NC6581	Motorola	MCM6581	
NC6583	Motorola	MCM6583	
NC6590	Motorola	MCM6590	
NC6832	Motorola	MCM6832	

Nortec Electronics

2222	AMI	S2222	
6002	TI	TMS4062	
		TMS4732	
		TMS6002	
6003	TI	TMS4063	
7001	RCA	MW7001	

Panasonic

AN332	Mitsubishi	M5188	

Plessey Semiconductors

SL3045	RCA	CA3045	
SL3046	RCA	CA3046	
SL3083	Signetics	CA3083	
SL3086	RCA	CA3086	
SL3183	Signetics	CA3183	
SL78M05	Signetics	µA78M05	
SL78M06	Signetics	µA78M06	
SL78M08	Signetics	µA78M08	
SL78M12	Signetics	µA78M12	
SL78M15	Signetics	µA78M15	
SL78M20	Signetics	µA78M20	
SL78M24	Signetics	µA78M24	
SL7805	Signetics	µA7805	
SL7806	Signetics	µA7806	
SL7812	Signetics	µA7812	
SL7815	Signetics	µA7815	
SL7818	Signetics	µA7818	
SL7824	Signetics	µA7824	
SP1001	Motorola	MC1001	
SP1004	Motorola	MC1004	
SP1006	Motorola	MC1006	
SP1007	Motorola	MC1007	
SP1010	Motorola	MC1010	
SP10100	Fairchild	F10100	
	Motorola	MC10100	
		MC10500	
	NEC America	µPB10100	
	Signetics	10100	
SP10101	Fairchild	F10101	
	Hitachi	HD10101	
	Motorola	MC10101	
		MC10501	
	NEC America	µPB10101	
	Signetics	10101	
SP10102	Fairchild	F10102	
	Hitachi	HD10102	
	Motorola	MC10102	
	NEC America	µPB10102	
	Signetics	10102	
SP10103	Fairchild	F10103	
	Motorola	MC10103	
		MC10503	
	NEC America	µPB10103	
	Signetics	10103	
SP10104	Fairchild	F10104	
	Hitachi	HD10104	
	Motorola	MC10104	
		MC10504	
	Signetics	10104	
SP10105	Fairchild	F10105	
	Hitachi	HD10105	
	Motorola	MC10105	
		MC10505	
	National	DM10105	
	NEC America	µPB10105	
	Signetics	10105	
SP10106	Fairchild	F10106	
	Hitachi	HD10106	
	Motorola	MC10106	
		MC10506	
	National	DM10106	
	NEC America	µPB10106	
	Signetics	10106	
SP10107	Fairchild	F10107	
	Hitachi	HD10107	
	Motorola	MC10107	
		MC10507	
	NEC America	µPB10107	
	Signetics	10107	
SP10109	Fairchild	F10109	
	Hitachi	HD10109	
	Motorola	MC10109	
		MC10509	
	National	DM10109	
	NEC America	µPB10109	
	Signetics	10109	
SP1011	Motorola	MC1011	
SP10110	Fairchild	F10110	
	Hitachi	HD10110	
	Motorola	MC10110	
	NEC America	µPB10110	
	Signetics	10110	
SP10111	Fairchild	F10111	
	Hitachi	HD10111	
	Motorola	MC10111	
	National	DM10111	
	NEC America	µPB10111	
	Signetics	10111	
SP10112	National	DM10112	
	Signetics	10112	
SP10113	Fairchild	F10113	
	Motorola	MC10113	
		MC10513	
	Signetics	10113	
SP10114	Fairchild	F10114	
	Motorola	MC10114	
		MC10514	
	Signetics	10114	
SP10115	Fairchild	F10115	
	Motorola	MC10115	
		MC10515	
SP10115	National	DM10115	
	NEC America	µPB10115	
	Signetics	10115	
SP10116	Fairchild	F10116	
	Hitachi	HD10116	
	Motorola	MC10116	
		MC10516	
	National	DM10116	
	Signetics	10116	
SP10117	Fairchild	F10117	
	Hitachi	HD10117	
	Motorola	MC10117	
		MC10517	
	National	DM10117	
	NEC America	µPB10117	
	Signetics	10117	
SP10118	Fairchild	F10118	
	Hitachi	HD10118	
	Motorola	MC10118	
		MC10518	
	National	DM10118	
	NEC America	µPB10118	
	Signetics	10118	
SP10119	Fairchild	F10119	
	Hitachi	HD10119	
	Motorola	MC10119	
		MC10519	
	National	DM10119	
	Signetics	10119	
SP1012	Motorola	MC1012	
SP10121	Fairchild	F10121	
	Hitachi	HD10121	
	Motorola	MC10121	
		MC10521	
	National	DM10121	
	Signetics	10121	
SP10123	Fairchild	F10123	
	Motorola	MC10123	
	Signetics	10123	
SP10124	Fairchild	F10124	
	Hitachi	HD10124	
	Motorola	MC10124	
		MC10524	
	National	DM10124	
	NEC America	µPB10124	
	Signetics	10124	
SP10125	Fairchild	F10125	
	Hitachi	HD10125	
	Motorola	MC10125	
		MC10525	
	Signetics	10125	
SP10128	Motorola	MC10128	
SP10129	Motorola	MC10129	
	Signetics	10129	
SP1013	Motorola	MC1013	
SP10130	Fairchild	F10130	
	Hitachi	HD10130	
	Motorola	MC10130	
		MC10530	
	Signetics	10130	
SP10131	Fairchild	F10131	
	Hitachi	HD10131	
	Motorola	MC10131	
		MC10531	
	NEC America	µPB10131	
	Signetics	10131	
SP10133	Fairchild	F10133	
	Hitachi	HD10133	
	Motorola	MC10133	
	NEC America	µPB10133	
	Signetics	10133	
SP10134	Fairchild	F10134	
	Hitachi	HD10134	
	Motorola	MC10134	
	Signetics	10134	
SP10135	Fairchild	F10135	
	Motorola	MC10135	
		MC10535	
	Signetics	10135	
SP10136	Fairchild	F10136	
	Hitachi	HD10136	
	Motorola	MC10136	
		MC10536	
	Signetics	10136	
SP10137	Fairchild	F10137	
	Motorola	MC10137	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Plessey Semiconductors (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
SP10137	Motorola	MC10537	
	Signetics	10137	
SP10138	Motorola	MC10138	
		MC10538	
SP1014	Motorola	MC1014	
SP10140	Signetics	10140	
	TI	SN10140	
SP10141	Fairchild	F10141	
	Motorola	MC10141	
		MC10541	
	Signetics	10141	
SP10142	NEC America	μPB10142	
	TI	SN10102	
SP10144	Motorola	MCM10544	
		MC10144	
	NEC America	μPB10144	
	Raytheon	RC10144	
	Signetics	10144	
	TI	SN10144	
SP10145	Fairchild	F10145	
	Hitachi	HD10145	
	Motorola	MCM10545	
		MC10145	
	Signetics	10145	
SP10148	Hitachi	HD10148	
	NEC America	μPB10148	
	Signetics	10148	
	TI	SN10148	
SP1015	Motorola	MC1015	
SP1016	Motorola	MC1016	
SP10160	Fairchild	F10160	
	Hitachi	HD10160	
	Motorola	MC10160	
		MC10560	
	Signetics	10160	
SP10161	Fairchild	F10161	
	Hitachi	HD10161	
	Motorola	MC10161	
		MC10561	
	NEC America	μPB10161	
	Signetics	10161	
SP10162	Fairchild	F10162	
	Hitachi	HD10162	
	Motorola	MC10162	
		MC10562	
	NEC America	μPB10162	
	Signetics	10162	
SP10164	Fairchild	F10164	
	Hitachi	HD10164	
	Motorola	MC10164	
		MC10564	
	NEC America	μPB10164	
	Signetics	10164	
	TI	SN10164	
SP10165	Fairchild	F10165	
	Hitachi	HD10165	
	Motorola	MC10165	
		MC10565	
	Signetics	10165	
SP10171	Fairchild	F10171	
	Motorola	MC10171	
		MC10571	
	Signetics	10171	
SP10172	Fairchild	F10172	
	Motorola	MC10172	
		MC10572	
	Signetics	10172	
SP10173	Fairchild	F10173	
	Motorola	MC10173	
	Signetics	10173	
SP10174	Fairchild	F10174	
	Hitachi	HD10174	
	Motorola	MC10174	
		MC10574	
	NEC America	μPB10174	
	Signetics	10174	
	TI	SN10174	
SP10175	Fairchild	F10175	
	Hitachi	HD10175	
	Motorola	MC10175	
		MC10575	
	Signetics	10175	
SP10176	Fairchild	F10176	
	Motorola	MC10176	
		MC10576	
	Signetics	10176	
SP10178	Motorola	MC10178	
		MC10578	
SP10179	Fairchild	F10179	
	Hitachi	HD10179	
	Motorola	MC10179	
		MC10579	
	Signetics	10179	
SP10180	Fairchild	F10180	
	Hitachi	HD10180	
	Motorola	MC10180	
		MC10580	
	NEC America	μPB10180	
	Signetics	10180	
SP10181	Fairchild	F10181	
	Hitachi	HD10181	
	Motorola	MC10181	
		MC10581	
	NEC America	μPB10181	
	Signetics	10181	
SP10190	Motorola	MC10190	
SP1020	Motorola	MC1020	
SP10211	Motorola	MC10211	
		MC10611	
SP10212	Fairchild	F10212	
	Motorola	MC10212	
		MC10612	
SP10216	Motorola	MC10216	
		MC10616	
SP1023	Motorola	MC1023	
SP10231	Motorola	MC10231	
		MC10631	
SP1026	Motorola	MC1026	
SP1027	Motorola	MC1027	
SP1030	Motorola	MC1030	
SP1031	Motorola	MC1031	
SP1032	Motorola	MC1032	
SP1033	Motorola	MC1033	
SP1034	Motorola	MC1034	
SP1035	Motorola	MC1035	
SP1039	Motorola	MC1039	
SP1040	Motorola	MC1040	
SP1047	Motorola	MC1047	
SP1048	Motorola	MC1048	
SP1201	Motorola	MC1201	
SP1202	Motorola	MC1202	
SP1203	Motorola	MC1203	
SP1204	Motorola	MC1204	
SP1205	Motorola	MC1205	
SP1206	Motorola	MC1206	
SP1207	Motorola	MC1207	
SP1208	Motorola	MC1208	
SP1209	Motorola	MC1209	
SP1210	Motorola	MC1210	
SP1211	Motorola	MC1211	
SP1212	Motorola	MC1212	
SP1213	Motorola	MC1213	
SP1214	Motorola	MC1214	
SP1215	Motorola	MC1215	
SP1216	Motorola	MC1216	
SP1220	Motorola	MC1220	
SP1226	Motorola	MC1226	
SP1230	Motorola	MC1226	
SP1231	Motorola	MC1231	
SP1233	Motorola	MC1233	
SP1235	Motorola	MC1235	
SP1239	Motorola	MC1239	
SP1240	Motorola	MC1240	
SP1247	Motorola	MC1247	
SP1248	Motorola	MC1248	
SP1660	Motorola	MC1660	
SP1662	Motorola	MC1662	
SP1664	Motorola	MC1664	
SP1666	Motorola	MC1666	
SP1668	Motorola	MC1668	
SP1670	Motorola	MC1670	
SP1690	Motorola	MC1690	
SP1692	Motorola	MC1692	
SP8616	Fairchild	11C05C	
SP8640	Fairchild	95H90	

Precision Monolithics, Inc.

Manufacturer Device	Replacement Source	Device	IC Master Page
DAC-08	AMD	DAC-08	
	Datel	DAC-08B	
	Fairchild	μA0801	
	Signetics	NE5007	
		NE5008	
		NE5009	
		SE5008	
		SE5009	
OP-07	**Fairchild**	**μA714**	**627**
PM1458	Exar	XR1458	
PM155	AMD	LF155	
	Fairchild	μAF155	
	Intersil	LF155	
	Motorola	LF155	
	National	**LF155**	**786**
	Raytheon	LF155	
	Signetics	LF155	
	TI	LF155	
PM1558	Exar	XR1558	
PM156	AMD	LF156	
	Fairchild	μAF156	
	Intersil	LF156	
	Motorola	LF156	
	National	**LF156**	**786**
	Raytheon	LF156	
	Signetics	LF156	
	TI	LF156	
PM157	AMD	LF157	
	Fairchild	μAF157	
	Intersil	LF157	
	Motorola	LF157	
	National	**LF157**	**786**
	Raytheon	LF157	
	Signetics	LF157	
	TI	LF157	
PM255	AMD	LF255	
	Fairchild	μAF255	
	Intersil	LF255	
	Motorola	LF255	
	National	**LF255**	**786**
	Raytheon	LF255	
	Signetics	LF255	
	TI	LF255	
PM256	AMD	LF256	
	Fairchild	μAF256	
	Intersil	LF256	
	Motorola	LF256	
	National	**LF256**	**786**
	Raytheon	LF256	
	Signetics	LF256	
	TI	LF256	
PM257	AMD	LF257	
	Fairchild	μAF257	
	Intersil	LF257	
	Motorola	LF257	
	National	**LF257**	**786**
	Raytheon	LF257	
	Signetics	LF257	
	TI	LF257	
PM355	AMD	LF355	
	Fairchild	μAF355	
	Intersil	LF355	
	Motorola	LF355	
	National	**LF355**	**786**
	Raytheon	LF355	
	Signetics	LF355	
	TI	LF355	
PM356	AMD	LF356	
	Fairchild	μAF356	
	Intersil	LF356	
	Motorola	LF356	
	National	**LF356**	**786**
	Raytheon	LF356	
	Signetics	LF356	
	TI	LF356	
PM357	AMD	LF357	
	Fairchild	μAF357	
	Intersil	LF357	
	Motorola	LF357	
	National	**LF357**	**786**
	Raytheon	LF357	
	Signetics	LF357	
	TI	LF357	
PM4136	Exar	XR4136	
♦SSS108	RCA	CA108	
SSS1408	AMD	AM1408	
		SSS1408	
	Datel	DAC-IC8B	
	Motorola	MC1408	
SSS1408A	AMD	SSS1408A	
SSS1458	Exar	XR1458	
	Motorola	MC1458	
SSS1508	AMD	SSS1508	
	Datel	DAC-IC8BM	
	Motorola	MC1508	
SSS1558	Exar	XR1558	
	Motorola	MC1558	
♦SSS208	Motorola	LM208	
	RCA	CA208	
♦SSS308	Motorola	LM308	
	RCA	CA308	
SSS741	Motorola	MC1741	
SSS747	AMD	SSS747	
	Motorola	MC1747	

Raytheon Semiconductor

Manufacturer Device	Replacement Source	Device	IC Master Page
AM2901A	AMD	AM2901A	
	Fairchild	F2901A	
		9409	
	Motorola	MC2901	
	National	**IDM2901A**	
			1656,1680
	NEC Micro	**μPB2901**	**1850**
	Signetics	**N2901**	**1851**
AM2902	AMD	AM2902	
	Motorola	MC2902	
	National	IDM2902	
	NEC Micro	**μPB2902**	**1850**
AM2905	AMD	AM2905	
	Motorola	MC2905	
	NEC Micro	**μPB2905**	**1850**
AM2906	AMD	AM2906	
	Motorola	MC2906	
	NEC Micro	**μPB2906**	**1850**
AM2907	AMD	AM2907	
	Motorola	MC2907	
	NEC Micro	**μPB2907**	**1850**
AM2909	AMD	AM2909	
	Motorola	MC2909	
	National	IDM2909A	
	NEC Micro	**μPB2909**	**1850**
AM2911	AMD	AM2911	
	Motorola	MC2911	
	National	IDM2911A	
	NEC Micro	**μPB2911**	**1850**
AM2918	AMD	AM2918	
	NEC Micro	**μPB2918**	**1850**
HA4741	**Harris**	**HA-4741**	**735**
LF155	AMD	LF155	
	Fairchild	μAF155	
	Intersil	LF155	
	Motorola	LF155	
	National	**LF155**	**786**
	PMI	**PM155**	**871**
	Signetics	LF155	
	TI	LF155	
LF156	AMD	LF156	
	Fairchild	μAF156	
	Intersil	LF156	
	Motorola	LF156	
	National	**LF156**	**786**
	PMI	**PM156**	**877**
	Signetics	LF156	
	TI	LF156	
LF157	AMD	LF157	
	Fairchild	μAF157	
	Intersil	LF157	
	Motorola	LF157	
	National	**LF157**	**786**
	PMI	**PM157**	**882**
	Signetics	LF157	
	TI	LF157	
LF255	AMD	LF255	
	Fairchild	μAF255	
	Intersil	LF255	
	Motorola	LF255	
	National	**LF255**	**786**

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Raytheon Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
LF255	**PMI**	**PM255**	**871**
	Signetics	LF255	
	TI	LF255	
LF256	AMD	LF256	
	Fairchild	μAF256	
	Intersil	LF256	
	Motorola	LF256	
	National	**LF256**	**786**
	PMI	**PM256**	**877**
	Signetics	LF256	
	TI	LF256	
LF257	AMD	LF257	
	Fairchild	μAF257	
	Intersil	LF257	
	Motorola	LF257	
	National	**LF257**	**786**
	PMI	**PM257**	**882**
	Signetics	LF257	
	TI	LF257	
LF355	AMD	LF355	
	Fairchild	μAF355	
	Intersil	LF355	
	Motorola	LF355	
	National	**LF355**	**786**
	PMI	**PM355**	**871**
	Signetics	LF355	
	TI	LF355	
LF356	AMD	LF356	
	Fairchild	μAF356	
	Intersil	LF356	
	Motorola	LF356	
	National	**LF356**	**786**
	PMI	**PM356**	**877**
	Signetics	LF356	
	TI	LF356	
LF357	AMD	LF357	
	Fairchild	μAF357	
	Intersil	LF357	
	Motorola	LF357	
	National	**LF357**	**786**
	PMI	**PM357**	**882**
	Signetics	LF357	
	TI	LF357	
LM101	AMD	LM101	
	Intersil	LM101	
	Motorola	LM101	
	National	LM101	
	RCA	CA101	
	Signetics	LM101	
	Silicon G	SG101	
	TI	LM101	
LM104	Motorola	LM104	
	Silicon G	SG104	
	TI	LM104	
LM105	AMD	LM105	
	Intersil	LM105	
	Motorola	LM105	
	National	LM105	
	Silicon G	SG105	
	TI	LM105	
LM106	AMD	LM106	
	TI	LM106	
LM107	AMD	LM107	
	Intersil	LM107	
	Motorola	LM107	
	National	LM107	
	RCA	CA107	
	Signetics	LM107	
	Silicon G	SG107	
	TI	LM107	
LM108	AMD	LM108	
	Intersil	LM108	
	Motorola	LM108	
	National	LM108	
	PMI	**OP-08**	**858**
		PM108	**858**
	RCA	CA108	
	Signetics	LM108	
	Silicon G	SG108	
LM109	Motorola	LM109	
	National	LM109	
	Signetics	LM109	
LM109	Silicon G	SG109	
	TI	LM109	
LM111	AMD	LM111	
	Intersil	LM111	
	Motorola	LM111	
	National	LM111	
	RCA	CA111	
	Signetics	LM111	
	Silicon G	SG111	
	TI	LM111	
LM112	AMD	LM112	
LM118	AMD	LM118	
	TI	LM118	
LM124	Motorola	LM124	
	National	LM104	
	Silicon G	SG124	
	TI	LM124	
LM139	Motorola	LM139	
	Silicon G	SG139	
	TI	LM139	
LM148	AMD	LM148	
	Exar	XR4741	
LM201	AMD	LM201	
	Intersil	LM201	
	Motorola	LM201	
	National	LM201	
	RCA	CA201	
	Silicon G	SG201	
	TI	LM201	
LM204	Motorola	LM204	
	National	LM204	
	Silicon G	SG204	
	TI	LM204	
LM205	AMD	LM205	
	Intersil	LM205	
	Motorola	LM205	
	National	LM205	
	Silicon G	SG205	
	TI	LM205	
LM207	AMD	LM207	
	Intersil	LM207	
	Motorola	LM207	
	National	LM207	
	RCA	CA207	
	Silicon G	SG207	
	TI	LM207	
LM208	AMD	LM208	
	Intersil	LM208	
	Motorola	LM208	
	PMI	**OP-08**	**858**
		PM208	
	RCA	CA208	
	Silicon G	SG208	
LM209	National	LM209	
	Signetics	LM209	
LM211	AMD	LM211	
	Intersil	LM211	
	Motorola	LM211	
	National	LM211	
	RCA	CA211	
	Signetics	LM211	
	Silicon G	SG211	
	TI	LM211	
LM216	AMD	LM216	
LM224	Motorola	LM224	
	Silicon G	SG224	
	TI	LM224	
LM239	Motorola	LM239	
	Silicon G	SG239	
	TI	LM239	
LM248	AMD	LM248	
	Exar	XR4741	
LM2900	National	LM2900	
LM2902	Motorola	LM2902	
	National	LM2902	
	TI	LM2902	
LM301	AMD	LM301	
	Intersil	LM301	
	Motorola	LM301	
	National	LM301	
	RCA	CA301	
	Signetics	LM301	
	Silicon G	SG301	
	TI	LM301	
LM304	Motorola	LM304	
	National	LM304	
LM304	Silicon G	SG304	
	TI	LM304	
LM305	AMD	LM305	
	Intersil	LM305	
	Motorola	LM305	
	National	LM305	
	Silicon G	SG305	
	TI	LM305	
LM306	AMD	LM306	
	TI	LM306	
LM307	AMD	LM307	
	Intersil	LM307	
	Motorola	LM307	
	National	LM307	
	RCA	CA307	
	Signetics	LM307	
	Silicon G	SG307	
	TI	LM307	
LM308	AMD	LM308	
	Intersil	LM308	
	Motorola	LM308	
	PMI	**OP-08**	**858**
		PM308	
	RCA	CA308	
	Signetics	LM308	
	Silicon G	SG308	
LM309	Motorola	LM309	
	National	LM309	
	Signetics	LM309	
	Silicon G	SG309	
	TI	LM309	
LM311	AMD	LM311	
	Intersil	LM311	
	Motorola	LM311	
	National	LM311	
	RCA	CA311	
	Signetics	LM311	
	Silicon G	SG311	
	TI	LM311	
LM312	AMD	LM312	
LM316	AMD	LM316	
LM318	AMD	LM318	
	TI	LM318	
LM324	Motorola	LM324	
	Silicon G	SG324	
	TI	LM324	
LM339	Motorola	LM339	
	RCA	CA339	
	Silicon G	SG339	
LM348	AMD	LM348	
	Exar	XR4741	
RC10144	Fairchild	F10410	
	Motorola	MC10144	
	NEC America	μPB10144	
	Plessey	SP10144	
	Signetics	10144	
	TI	SN10144	
RC1414	Motorola	MC1414	
RC1437	Motorola	MC1437	
RC1458	Exar	XR1458	
	Harris	**HA-2655**	**704**
	Motorola	MC1458	
	PMI	**OP-14**	**844**
		SSS1458	**844**
	RCA	CA1458	
	Signetics	MC1458	
	Silicon G	SG1458	
	TI	MC1458	
RC1488	Exar	XR1488	
	Motorola	MC1488	
	Signetics	MC1488	
	Silicon G	SG1488	
	TI	SN75188	
RC1489	Exar	XR1489	
	Motorola	MC1489	
	Signetics	MC1489	
	Silicon G	SG1489	
	TI	SN75189	
RC1489A	Signetics	MC1489A	
RC1556	Motorola	MC1456	
	Signetics	MC1456	
	Silicon G	SG1456	
RC1558	Motorola	RC1558	
RC2207	Exar	XR2207	
RC2211	Exar	XR2211	
RC2567	Exar	XR2567	
RC2567	Exar	XR2567C	
RC3302	Motorola	MC3302	
	TI	LM3302	
RC3403	Exar	XR3403	
		XR3403C	
	Fairchild	μA3403	
	Motorola	MC3403	
RC4136	Exar	XR4136	
		XR4212	
	Fairchild	μA4136	
	PMI	**OP-09**	**864**
		PM4136	**864**
	TI	RC4136	
RC414	TI	TL514	
RC4151	TI	XR4151	
RC4152	TI	XR4152	
RC4156	TI	XR4156	
RC4194	Exar	XR4194	
RC4444	Motorola	MC3416	
RC4531	Signetics	NE531	
RC4558	Exar	XR4558	
	Fairchild	μA4558	
	Motorola	MC4558	
	TI	RC4558	
RC4739	Exar	XR4739	
RC5332	Fairchild	93411	
RC5342	Fairchild	93411	
RC5500	TI	SN74S314	
RC555	Exar	XR555	
	Fairchild	μA555	
	Intersil	NE555	
	Motorola	MC1455	
	RCA	CA555	
	Signetics	NE555	
	Silicon G	SG555	
	TI	NE555	
RC556	Exar	XR556	
	Fairchild	μA556	
	Motorola	MC3456	
	Signetics	NE556	
	Silicon G	SG556	
	TI	NE556	
RC592	Motorola	NE592	
	Signetics	NE592	
RC702	Motorola	MC1712	
	TI	μA702	
RC709	Motorola	MC1709	
	Signetics	μA709	
	TI	μA709	
RC710	Motorola	MC1710	
	Signetics	μA710	
	Silicon G	SG710	
	TI	TL710	
RC711	Motorola	MC1711	
	Signetics	μA711	
	Silicon G	SG711	
	TI	μA711	
RC723	AMD	723	
	Intersil	723	
	Motorola	MC1723	
	National	LM723	
	RCA	CA723	
	Signetics	μA723	
	Silicon G	SG723	
	TI	μA723	
RC725	AMD	725	
	PMI	**PM725**	**849**
		SSS725	**849**
RC733	AMD	733	
	Fairchild	μA733	
	Motorola	MC1733	
	Signetics	μA733	
	Silicon G	SG733	
	TI	μA733	
RC741	AMD	741	
	Intersil	741	
	Motorola	MC1741	
	PMI	**OP-02**	**839**
		SSS741	**839**
	RCA	CA741	
	Signetics	μA741	
	Silicon G	SG741	
	TI	μA741	
RC747	AMD	747	
	Motorola	MC1747	
	PMI	**OP-04**	**844**

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Raytheon Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
RC747	**PMI**	**SSS747**	844
	RCA	CA747	
	Signetics	µA747	
	Silicon G	SG747	
	TI	µA747	
RC748	AMD	748	
	Intersil	748	
	Motorola	MC1748	
	RCA	CA748	
	Signetics	µA748	
	Silicon G	SG748	
	TI	µA748	
RC75107	Fairchild	75107	
	Motorola	MC75107	
	TI	SN75107	
RC75108	Fairchild	75108	
	Motorola	MC75108	
	TI	SN75108	
RC75109	Fairchild	75109	
	TI	SN75109	
RC75110	Fairchild	75110	
	Motorola	MC75110	
	TI	SN75110	
♦RC7520	Signetics	7520	
	Silicon G	SG7520	
	TI	SN7520	
♦RC7521	Signetics	7521	
	Silicon G	SG7521	
♦RC7522	Motorola	MC7522	
	Signetics	7522	
	Silicon G	SG7522	
	TI	SN7522	
♦RC7523	Motorola	MC7523	
	Signetics	7523	
	Silicon G	SG7523	
RC75235	TI	SN75235	
♦RC7524	Fairchild	7524	
	Motorola	MC7524	
	Signetics	7524	
	Silicon G	SG7524	
	TI	SN7524	
♦RC7525	Fairchild	7525	
	Motorola	MC7525	
	Signetics	7525	
	Silicon G	SG7525	
RC7528	Fairchild	7528	
	Silicon G	SG7528	
	TI	SN7528	
RC7529	Fairchild	7529	
	Silicon G	SG7529	
RC75325	Fairchild	75325	
	Motorola	MC75325	
	Silicon G	SG75325	
RC8T09	Signetics	8T09	
RC8T10	Signetics	8T10	
♦RC8T13	Fairchild	8t13	
	Signetics	8T13	
♦RC8T14	Fairchild	8T14	
	Motorola	MC8T14	
	Signetics	8T14	
♦RC8T23	Fairchild	8T23	
	Motorola	MC8T23	
♦RC8T24	Fairchild	8T24	
	Motorola	MC8T24	
	Signetics	8T24	
RC8200	Signetics	N8200	
RC8201	Signetics	N8201	
RC8202	Signetics	N8202	
RC8203	Signetics	N8203	
RC8225	Signetics	N8225	
	TI	SN74S189	
		SN74S289	
RC8230	Signetics	N8230	
RC8231	Signetics	N8231	
RC8233	Signetics	N8233	
RC8234	Signetics	N8234	
RC8241	Signetics	N8241	
RC8242	Signetics	N8242	
RC8243	Signetics	N8243	
RC8250	Signetics	N8250	
RC8251	Signetics	N8251	
RC8252	Signetics	N8252	
RC8260	Signetics	N8260	
RC8261	Signetics	N8261	
RC8263	Signetics	N8263	
RC8264	Signetics	N8264	
RC8266	Signetics	N8266	
RC8267	Signetics	N8267	
RC8270	Signetics	N8270	
	TI	SN74178	
RC8271	Signetics	N8271	
	TI	SN74179	
RC8273	Signetics	N8273	
RC8274	Signetics	N8274	
RC8280	Signetics	N8280	
	TI	SN74176	
RC8281	Signetics	N8281	
RC8290	Signetics	N8290	
		8290	
	TI	SN74196	
RC8291	Signetics	N8291	
	TI	SN74197	
♦RC8513	Motorola	MC8T13	
RC930	Motorola	MC830	
	TI	SN15830	
RC932	Motorola	MC832	
	TI	SN15832	
RC933	Motorola	MC933	
	TI	SN15833	
RC934	Motorola	MC934	
	TI	SN15834	
RC935	Motorola	MC835	
	TI	SN15835	
RC936	Motorola	MC836	
RC937	Motorola	MC837	
	TI	SN15837	
RC940	Motorola	MC840	
RC941	Motorola	MC841	
RC944	Motorola	MC844	
	TI	SN15844	
RC945	Motorola	MC845	
	TI	SN15845	
RC946	**Motorola**	**MC846**	
	TI	SN15846	
RC948	Motorola	MC848	
	TI	SN15848	
RC949	Motorola	MC849	
	TI	SN15849	
RC950	Motorola	MC850	
	TI	SN15850	
RC951	Motorola	MC851	
	TI	SN15851	
RC957	Motorola	MC857	
	TI	SN15857	
RC958	Motorola	MC858	
	TI	SN15858	
RC961	Motorola	MC861	
	TI	SN15861	
RC962	Motorola	MC862	
	TI	SN15862	
RC9621	Fairchild	9621	
RC9622	Fairchild	9622	
RC963	Motorola	MC863	
	TI	SN15863	
RC993	Motorola	MC853	
	TI	SN158093	
RC994	Motorola	MC856	
	TI	SN158094	
RC997	Motorola	MC855	
	TI	SN158097	
RC999	Motorola	MC852	
	TI	SN158092	
RM1514	Motorola	MC1514	
	TI	TL514	
RM1537	Motorola	MC1537	
RM1556	Motorola	MC1556	
	Signetics	MC1556	
	Silicon G	SG1556	
RM1558	Exar	XR1558	
	Harris	**HA-2650**	**704**
	Motorola	MC1558	
	PMI	**PM1558**	**844**
		SSS1558	**844**
	RCA	CA1558	
	Signetics	MC1558	
	Silicon G	SG1558	
	TI	MC1558	
RM2207	Exar	XR2207	
RM2211	Exar	XR2211	
RM2567	Exar	XR2567	
		XR2567M	
RM3403	Exar	XR3403M	
RM3503	Exar	XR3503	
	Fairchild	µA3503	
	Motorola	MC3503	
RM4136	Exar	XR4136	
		XR4136M	
	Fairchild	µA4136	
	PMI	**OP-09**	**864**
	TI	RM4136	
RM4151	TI	XR4151	
RM4152	TI	XR4152	
RM4156	TI	XR4156	
RM4194	Exar	XR4194	
RM4531	Signetics	SE531	
RM4558	Motorola	MC4558	
	RCA	CA1558	
	Silicon G	SG1558	
	TI	RM4558	
RM55107	Fairchild	55107	
	Motorola	MC55107	
	TI	SN55107	
RM55108	Fairchild	55108	
	TI	SN55108	
RM55109	Fairchild	55109	
	TI	SN55109	
RM55110	Fairchild	55110	
	TI	SN55110	
RM5524	Fairchild	5524	
	TI	SN5524	
RM5525	Fairchild	5525	
RM55325	Fairchild	55325	
	Motorola	MC55325	
	TI	SN55325	
RM555	AMD	SE555	
	Exar	XR555M	
	Fairchild	µA555	
	Intersil	SE555	
	Motorola	**MC1555**	
	Signetics	SE555	
	Silicon G	SG555	
	TI	SE555	
RM556	Exar	XR556M	
	Fairchild	µA556	
	Motorola	MC3556	
	Silicon G	SG556	
	TI	SE556	
RM592	Motorola	SE592	
	Signetics	SE592	
RM702	Motorola	MC1712	
	TI	µA702	
RM709	Motorola	MC1709	
	Signetics	µA709	
	TI	µA709	
RM710	Motorola	MC1710	
	Signetics	µA710	
	Silicon G	SG710	
	TI	µA710	
RM711	Motorola	MC1711	
	Signetics	µA711	
	Silicon G	SG711	
	Teledyne S	711	
	TI	µA711	
RM723	AMD	723	
	Intersil	723	
	Motorola	MC1723	
	National	LM723	
	RCA	CA723	
	Signetics	µA723	
	Silicon G	SG723	
	TI	µA723	
RM725	AMD	725	
	PMI	**PM725**	**849**
		SSS725	**849**
RM733	AMD	733	
	Fairchild	µA733	
	Motorola	MC1733	
	Signetics	µA733	
	Silicon G	SG733	
	TI	µA733	
RM741	AMD	741	
	Intersil	741	
	Motorola	MC1741	
	PMI	**PM741**	**839**
RM741	**PMI**	**SSS741**	**839**
	RCA	CA741	
	Signetics	µA741	
	Silicon G	SG741	
	TI	µA741	
RM747	AMD	747	
	Motorola	MC1747	
	PMI	**PM747**	**844**
		SSS747	**844**
	RCA	CA747	
	Signetics	µA747	
	Silicon G	SG747	
	TI	µA747	
RM748	AMD	748	
	Intersil	748	
	Motorola	MC1748	
	RCA	CA748	
	Signetics	µA748	
	Silicon G	SG748	
	TI	µA748	
♦RM8T13	Fairchild	8T13	
♦RM8T14	Fairchild	8T14	
RM930	Motorola	MC930	
	TI	SN15930	
RM932	Motorola	MC932	
	TI	SN15932	
RM933	Motorola	MC933	
	TI	SN15933	
RM934	Motorola	MC934	
	TI	SN15934	
RM935	Motorola	MC935	
	TI	SN15935	
RM936	Motorola	MC936	
	TI	SN15936	
RM937	Motorola	MC937	
	TI	SN15937	
RM940	Motorola	MC940	
RM941	Motorola	MC941	
RM944	Motorola	MC944	
	TI	SN15944	
RM945	Motorola	MC945	
	TI	SN15945	
RM946	Motorola	MC946	
	TI	SN15946	
RM947	TI	SN15947	
RM948	Motorola	MC948	
	TI	SN15948	
RM949	Motorola	MC949	
	TI	SN15949	
RM950	Motorola	MC950	
	TI	SN15950	
RM951	Motorola	MC951	
	TI	SN15951	
RM957	Motorola	MC957	
	TI	SN15957	
RM958	Motorola	MC958	
	TI	SN15958	
RM961	Motorola	MC961	
	TI	SN15961	
RM962	Motorola	MC962	
	TI	SN15962	
RM9621	Fairchild	9621	
RM9622	Fairchild	9622	
RM963	Motorola	MC963	
	TI	SN15963	
RM993	Motorola	MC953	
	TI	SN159093	
RM994	Motorola	MC956	
	TI	SN159094	
RM997	Motorola	MC955	
	TI	SN159097	
RM999	Motorola	MC952	
	TI	SN159099	
RV4151	TI	XR4151	
RV4152	TI	XR4152	
RV4156	TI	XR4156	
SP3724	RCA	CA3724	
SP3725	RCA	CA3725	
25LS138	AMD	AM25LS138	
25LS139	AMD	AM25LS138	
25LS14	AMD	AM25LS14	
25LS15	AMD	AM25LS15	
25LS151	AMD	AM25LS125	
25LS153	AMD	AM25LS153	
25LS157	AMD	AM25LS157	
25LS158	AMD	AM25LS158	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
25LS160	AMD	AM25LS160	
25LS161	AMD	AM25LS161	
25LS162	AMD	AM25LS162	
25LS163	AMD	AM25LS163	
25LS164	AMD	AM25LS164	
25LS170	AMD	AM25LS170	
25LS174	AMD	AM25LS174	
25LS175	AMD	AM25LS175	
25LS181	AMD	AM25LS181	
25LS190	AMD	AM25LS190	
25LS191	AMD	AM25LS191	
25LS192	AMD	AM25LS192	
25LS193	AMD	AM25LS193	
25LS194A	AMD	AM25LS194A	
25LS195	AMD	AM25LS195	
25LS22	AMD	AM25LS22	
25LS23	AMD	AM25LS23	
25LS240	AMD	25LS240	
25LS241	AMD	AM25LS241	
25LS251	AMD	AM25LS251	
25LS253	AMD	AM25LS253	
25LS258	AMD	AM25LS258	
25LS299	AMD	AM25LS299	
25LS373	AMD	25LS373	
25LS670	AMD	AM25LS670	
26S10	AMD	AM26S10	
26S11	AMD	AM26S11	
54H00	Fairchild	54H00	
	ITT	ITT54H00	
	National	DM54H00	
	Signetics	54H00	
	TI	SN54H00	
54H01	Fairchild	54H01	
	ITT	ITT54H01	
	National	DM54H01	
	Signetics	54H01	
	TI	SN54H01	
54H04	Fairchild	54H04	
	ITT	ITT54H04	
	National	DM54H04	
	Signetics	54H04	
	TI	SN54H04	
54H05	Fairchild	54H05	
	ITT	ITT54H05	
	National	DM54H05	
	Signetics	54H05	
	TI	SN54H05	
54H10	Fairchild	54H10	
	ITT	ITT54H10	
	National	DM54H10	
	Signetics	54H10	
	TI	SN54H10	
54H11	Fairchild	54H11	
	ITT	ITT54H11	
	National	DM54H11	
	Signetics	54H11	
	TI	SN54H11	
54H15	Fairchild	54H15	
	TI	SN54H15	
54H20	Fairchild	54H20	
	ITT	ITT54H20	
	National	DM54H20	
	Signetics	54H20	
	TI	SN54H20	
54H22	Fairchild	54H22	
	National	DM54H22	
	Signetics	54H22	
	TI	SN54H22	
54H40	Fairchild	54H40	
	ITT	ITT54H40	
	National	DM54H40	
	Signetics	54H40	
	TI	SN54H40	
54H74	Fairchild	54H74	
	ITT	ITT54H74	
	National	DM54H74	
	Signetics	54H74	
	TI	SN54H74	
54LS00	Fairchild	54LS00	
	Motorola	SN54LS00	
	National	DM54LS00	
	Signetics	54LS00	
54LS00	TI	SN54LS00	
54LS01	Fairchild	54LS01	
	National	DM54LS01	
	Signetics	54LS01	
	TI	SN54LS01	
54LS02	Fairchild	54LS02	
	Motorola	SN54LS02	
	National	DM54LS02	
	Signetics	54LS02	
	TI	SN54LS02	
54LS03	Fairchild	54LS03	
	Motorola	SN54LS03	
	National	DM54LS03	
	Signetics	54LS03	
	TI	SN54LS03	
54LS04	Fairchild	54LS04	
	Motorola	SN54LS04	
	National	DM54LS04	
	Signetics	54LS04	
	TI	SN54LS04	
54LS05	Fairchild	54LS05	
	Motorola	SN54LS05	
	National	DM54LS05	
	Signetics	54LS05	
	TI	SN54LS05	
54LS08	Fairchild	54LS08	
	Motorola	SN54LS08	
	National	DM54LS08	
	Signetics	54LS08	
	TI	SN54LS08	
54LS09	Fairchild	54LS09	
	Motorola	SN54LS09	
	National	DM54LS09	
	Signetics	54LS09	
	TI	SN54LS09	
54LS10	Fairchild	54LS10	
	Motorola	SN54LS10	
	National	DM54LS10	
	Signetics	54LS10	
	TI	SN54LS10	
54LS107	Fairchild	54LS107	
	Motorola	SN54LS107	
	National	DM54LS107	
	Signetics	54LS107	
	TI	SN54LS107	
54LS109	Fairchild	54LS109	
	Motorola	SN54LS109	
	National	DM54LS109	
	Signetics	54LS109	
	TI	SN54LS109	
54LS11	Fairchild	54LS11	
	Motorola	SN54LS11	
	National	DM54LS11	
	Signetics	54LS11	
	TI	SN54LS11	
54LS112	Fairchild	54LS112	
	National	DM54LS112	
	Signetics	54LS112	
	TI	SN54LS112	
54LS113	Fairchild	54LS113	
	National	DM54LS113	
	Signetics	54LS113	
	TI	SN54LS113	
54LS114	Fairchild	54LS114	
	Motorola	SN54LS114	
	National	DM54LS114	
	Signetics	54LS114	
	TI	SN54LS114	
54LS12	Fairchild	54LS12	
	National	DM54LS12	
	Signetics	54LS12	
	TI	SN54LS12	
54LS122	National	DM54LS122	
	TI	SN54LS122	
54LS123	AMD	SN54LS123	
	National	DM54LS123	
	TI	SN54LS123	
54LS125	Fairchild	54LS125	
	National	DM54LS125	
	Signetics	54LS125	
	TI	SN54LS125A	
54LS126	Fairchild	54LS126	
	Motorola	SN54LS126	
	National	DM54LS126	
	Signetics	54LS126	
	TI	SN54LS126A	
54LS13	Motorola	SN54LS13	
	National	DM54LS13	
	Signetics	54LS13	
	TI	SN54LS13	
54LS132	Fairchild	54LS132	
	Motorola	SN54LS132	
	National	DM54LS132	
	Signetics	54LS132	
54LS136	Fairchild	54LS136	
	Motorola	SN54LS136	
	Signetics	54LS136	
	TI	SN54LS136	
54LS138	Fairchild	54LS138	
	Motorola	SN54LS138	
	National	DM54LS138	
	Signetics	54LS138	
	TI	SN54LS138	
54LS139	AMD	SN54LS139	
	Fairchild	54LS139	
	Motorola	SN54LS139	
	National	DM54LS139	
	Signetics	54LS139	
		74LS139	
	TI	SN54LS139	
54LS14	Fairchild	54LS14	
	Motorola	SN54LS14	
	National	DM54LS14	
	Signetics	54LS14	
	TI	SN54LS14	
54LS15	Fairchild	54LS15	
	Motorola	SN54LS15	
	National	DM54LS15	
	Signetics	54LS15	
	TI	SN54LS15	
54LS151	AMD	SN54LS151	
	Fairchild	54LS151	
	Motorola	SN54LS151	
	National	DM54LS151	
	Signetics	54LS151	
		54LS153	
	TI	SN54LS151	
54LS152	Fairchild	54LS152	
	Motorola	SN54LS152	
	TI	SN54LS152	
54LS153	AMD	SN54LS153	
	Fairchild	54LS153	
	Motorola	SN54LS153	
	National	DM54LS153	
	Signetics	54LS153	
	TI	SN54LS153	
54LS156	Fairchild	54LS156	
	Motorola	SN54LS156	
	National	DM54LS156	
	TI	SN54LS156	
54LS157	AMD	SN54LS157	
	Fairchild	54LS157	
	Motorola	SN54LS157	
	National	DM54LS157	
	Signetics	54LS157	
	TI	SN54LS157	
54LS158	Fairchild	54LS158	
	Motorola	SN54LS158	
	National	DM54LS158	
	Signetics	54LS158	
	TI	SN54LS158	
54LS160	AMD	SN54LS160	
	Fairchild	54LS160	
	Motorola	SN54LS160	
	National	DM54LS160	
	Signetics	54LS160	
	TI	SN54LS160	
54LS161	AMD	SN54LS161	
	Fairchild	54LS161	
	Motorola	SN54LS161	
	National	DM54LS161	
	Signetics	54LS161	
	TI	SN54LS161	
54LS162	AMD	SN54LS162	
	Fairchild	54LS162	
	Motorola	SN54LS162	
	National	DM54LS162	
	Signetics	54LS162	
	TI	SN54LS162	
54LS163	AMD	SN54LS163	
	Fairchild	54LS163	
	Motorola	SN54LS163	
54LS163	National	DM54LS163	
	Signetics	54LS163	
	TI	SN54LS163	
54LS164	AMD	SN54LS164	
	Fairchild	54LS164	
	Motorola	SN54LS164	
	National	DM54LS164	
	Signetics	54LS164	
	TI	SN54LS164	
54LS170	AMD	SN54LS170	
	Fairchild	54LS170	
	Motorola	SN54LS170	
	National	DM54LS170	
	Signetics	54LS170	
	TI	SN54LS170	
54LS174	AMD	SN54LS174	
	Fairchild	54LS174	
	National	DM54LS174	
	Signetics	54LS174	
	TI	SN54LS174	
54LS175	AMD	SN54LS175	
	Fairchild	54LS175	
	Motorola	SN54LS175	
	National	DM54LS175	
	Signetics	54LS175	
	TI	SN54LS175	
54LS181	AMD	SN54LS181	
	Fairchild	54LS181	
	Motorola	SN54LS181	
	Signetics	54LS181	
	TI	SN54LS181	
54LS190	AMD	SN54LS190	
	Fairchild	54LS190	
	Motorola	SN54LS190	
	National	DM54LS190	
	Signetics	54LS190	
	TI	SN54LS190	
54LS191	AMD	SN54LS191	
	Fairchild	54LS191	
	Motorola	SN54LS191	
	National	DM54LS191	
	Signetics	54LS191	
	TI	SN54LS191	
54LS192	AMD	SN54LS192	
	Fairchild	54LS192	
	Motorola	SN54LS192	
	National	DM54LS192	
	Signetics	54LS192	
	TI	SN54LS192	
54LS193	AMD	SN54LS193	
	Fairchild	54LS193	
	Motorola	SN54LS193	
	National	DM54LS193	
	Signetics	54LS193	
	TI	SN54LS193	
54LS194A	AMD	SN54LS194A	
	Fairchild	54LS194	
	Motorola	SN54LS194	
	Signetics	54LS194A	
	TI	SN54LS194A	
54LS195A	AMD	SN54LS195A	
	Fairchild	54LS195	
	Motorola	SN54LS195	
	Signetics	54LS195A	
	TI	SN54LS195A	
54LS196	Fairchild	54LS196	
	Motorola	SN54LS196	
	National	DM54LS196	
	Signetics	54LS196	
	TI	SN54LS196	
54LS197	Fairchild	54LS197	
	Motorola	SN54LS197	
	National	DM54LS197	
	Signetics	54LS197	
	TI	SN54LS197	
54LS20	Fairchild	54LS20	
	Motorola	SN54LS20	
	National	DM54LS20	
	Signetics	54LS20	
	TI	SN54LS20	
54LS21	Fairchild	54LS21	
	Motorola	SN54LS21	
	National	DM54LS21	
	Signetics	54LS21	
	TI	SN54LS21	
54LS22	Fairchild	54LS22	

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Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Raytheon Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
54LS22	Motorola	SN54LS22	
	National	DM54LS22	
	Signetics	54LS22	
	TI	SN54LS22	
54LS221	National	DM54LS221	
	Signetics	54LS221	
	TI	SN54LS221	
54LS242	AMD	SN54LS242	
	TI	SN54LS242	
54LS243	AMD	SN54LS243	
	TI	SN54LS243	
54LS251	AMD	SN54LS251	
	Fairchild	54LS251	
	Motorola	SN54LS251	
	Signetics	54LS251	
	TI	SN54LS251	
54LS253	AMD	SN54LS253	
	Fairchild	54LS253	
	Motorola	SN54LS253	
	National	DM54LS253	
	Signetics	54LS253	
	TI	SN54LS253	
54LS257	Fairchild	54LS257	
	Motorola	SN54LS257	
	National	DM54LS257	
	Signetics	54LS257	
	TI	SN54LS257	
54LS258	AMD	SN54LS258	
	Fairchild	54LS258	
	Motorola	SN54LS258	
	Signetics	54LS258	
	TI	SN54LS258	
54LS26	Fairchild	54LS26	
	National	DM54LS26	
	Signetics	54LS26	
	TI	SN54LS26	
54LS261	Signetics	54LS261	
	TI	SN54LS261	
54LS266	Fairchild	54LS266	
	Motorola	SN54LS266	
	Signetics	54LS266	
	TI	SN54LS266	
54LS27	Fairchild	54LS27	
	Motorola	SN54LS27	
	National	DM54LS27	
	Signetics	54LS27	
	TI	SN54LS27	
54LS28	Signetics	54LS28	
	TI	SN54LS28	
54LS283	Fairchild	54LS283	
	Motorola	SN54LS283	
	National	DM54LS283	
	Signetics	54LS283	
	TI	SN54LS283	
54LS295A	Fairchild	54LS295	
	Motorola	SN54LS295	
	Signetics	54LS295A	
	TI	SN54LS295B	
54LS298	Fairchild	54LS298	
	Motorola	SN54LS298	
	TI	SN54LS298	
54LS299	AMD	SN54LS299	
	Fairchild	54LS299	
	TI	SN54LS299	
54LS30	Fairchild	54LS30	
	Motorola	SN54LS30	
	National	DM54LS30	
	Signetics	54LS30	
	TI	SN54LS30	
54LS32	Fairchild	54LS32	
	Motorola	SN54LS32	
	National	DM54LS32	
	Signetics	54LS32	
	TI	SN54LS32	
54LS33	Fairchild	54LS33	
	Signetics	54LS33	
	TI	SN54LS33	
54LS365	Fairchild	54LS365	
	Motorola	SN54LS365	
	Signetics	54LS365	
	TI	SN54LS365	
54LS366	Fairchild	54LS366	
54LS366	Motorola	SN54LS366	
	Signetics	54LS366	
	TI	SN54LS366	
54LS367	Fairchild	54LS367	
	Motorola	SN54LS367	
	Signetics	54LS367	
	TI	SN54LS367	
54LS368	Fairchild	54LS368	
	Motorola	SN54LS368	
	Signetics	54LS368	
	TI	SN54LS368	
54LS37	Fairchild	54LS37	
	Motorola	SN54LS37	
	National	DM54LS37	
	Signetics	54LS37	
	TI	SN54LS37	
54LS375	Signetics	54LS375	
	TI	SN54LS375	
54LS38	Fairchild	54LS38	
	Motorola	SN54LS38	
	National	DM54LS38	
	Signetics	54LS38	
	TI	SN54LS38	
54LS386	Signetics	54LS386	
	TI	54LS386	
54LS395	Fairchild	54LSO95	
	National	DM54LS395	
	Signetics	54LS395	
	TI	SN54LS395	
54LS40	Fairchild	54LS40	
	Motorola	SN54LS40	
	National	DM54LS40	
	Signetics	54LS40	
	TI	SN54LS40	
54LS42	Fairchild	54LS42	
	Motorola	SN54LS42	
	National	DM54LS42	
	Signetics	54LS42	
	TI	SN54LS42	
54LS51	Fairchild	54LS51	
	Motorola	SN54LS51	
	National	DM54LS51	
	Signetics	54LS51	
	TI	SN54LS51	
54LS54	Fairchild	54LS54	
	Motorola	SN54LS54	
	National	DM54LS54	
	Signetics	54LS54	
	TI	SN54LS54	
54LS55	Fairchild	54LS55	
	Motorola	SN54LS55	
	National	DM54LS55	
	Signetics	54LS55	
	TI	SN54LS55	
54LS670	AMD	SN54LS670	
	Fairchild	54LS670	
	Motorola	SN54LS670	
	National	DM54LS670	
	Signetics	54LS670	
	TI	SN54LS670	
54LS73	Fairchild	54LS73	
	Motorola	SN54LS73	
	National	DM54LS73	
	Signetics	54LS73	
	TI	SN54LS73	
54LS74	Fairchild	54LS74	
	Motorola	SN54LS74	
	National	DM54LS74	
	Signetics	54LS74	
	TI	SN54LS74	
54LS75	Fairchild	54LS75	
	National	DM54LS75	
	Signetics	54LS75	
	TI	SN54LS75	
54LS76	National	DM54LS76	
	Signetics	54LS76	
	TI	SN54LS76	
54LS77	Fairchild	54LS77	
		74LS77	
	National	DM74LS77	
	TI	SN54LS77	
54LS78	National	DM54LS78	
	Signetics	54LS78	
	TI	SN54LS78	
54LS83A	Fairchild	54LS83	
	Motorola	SN54LS83	
54LS83A	National	DM54LS83	
	Signetics	54LS83A	
	TI	SN54LS83A	
54LS85	Fairchild	54LS85	
	National	DM54LS85	
	Signetics	54LS85	
	TI	SN54LS85	
54LS86	Fairchild	54LS86	
	Motorola	SN54LS86	
	Signetics	54LS86	
	TI	SN54LS86	
54LS90	Fairchild	54LS90	
	Motorola	SN54LS90	
	Signetics	54LS90	
	TI	SN54LS90	
54LS91	TI	SN54LS91	
54LS92	Motorola	SN54LS92	
	Signetics	54LS92	
	TI	SN54LS92	
54LS93	Fairchild	54LS93	
	Motorola	SN54LS93	
	Signetics	54LS93	
	TI	SN54LS93	
54LS95B	Fairchild	54LS95B	
	Motorola	SN54LS95B	
	Signetics	54LS95B	
	TI	SN54LS95B	
54S240	AMD	SN54S240	
	MMI	**54S240**	**462**
	TI	SN54S240	
54S241	AMD	SN54S241	
	MMI	**54S241**	**462**
	TI	SN54S241	
54S244	AMD	SN54S244	
	MMI	**54S244**	**462**
5400	Fairchild	5400	
	ITT	ITT5400	
	Motorola	MC5400	
	National	DM5400	
	Signetics	5400	
	TI	SN5400	
5401	Fairchild	5401	
	ITT	ITT5401	
	Motorola	MC5401	
	National	DM5401	
	Signetics	5401	
	TI	SN5401	
5403	Fairchild	5403	
	ITT	ITT5403	
	Motorola	MC5403	
	National	DM5403	
	Signetics	5403	
	TI	SN5403	
5404	Fairchild	5404	
	ITT	ITT5404	
	Motorola	MC5404	
	National	DM5404	
	Signetics	5404	
	TI	SN5404	
5405	Fairchild	5405	
	ITT	ITT5405	
	Motorola	MC5405	
	National	DM5405	
	Signetics	5405	
	TI	SN5405	
5408	Fairchild	5408	
	ITT	ITT5408	
	Motorola	MC5408	
	National	DM5408	
	Signetics	5408	
	TI	SN5408	
5409	Fairchild	5409	
	ITT	ITT5409	
	Motorola	MC5409	
	National	DM5409	
	Signetics	5409	
	TI	SN5409	
5410	Fairchild	5410	
	ITT	ITT5410	
	Motorola	MC5410	
	National	DM5410	
	Signetics	5410	
	TI	SN5410	
5411	Fairchild	5411	
	ITT	ITT5411	
	National	DM5411	
5411	Signetics	5411	
	TI	SN5411	
5412	Fairchild	5412	
	ITT	ITT5412	
	Signetics	5412	
	TI	SN5412	
54123	AMD	SN54123	
	Fairchild	54123	
	ITT	ITT54123	
	Motorola	MC54123	
	National	DM54123	
	Signetics	54123	
	TI	SN54123	
54145	Fairchild	54145	
	ITT	ITT54145	
	Motorola	MC54145	
	National	DM54145	
	Signetics	54145	
	TI	SN54145	
54150	Fairchild	54150	
	Motorola	MC54150	
	National	DM54150	
	Signetics	54150	
	TI	SN54150	
54151	Fairchild	54151	
	ITT	ITT54151	
	Motorola	MC54151	
	National	DM54151	
	Signetics	54151	
	TI	SN54151	
54152	Fairchild	54152	
	Motorola	MC54152	
	Signetics	54152	
	TI	SN54152	
54153	Fairchild	54153	
	ITT	ITT54153	
	Motorola	MC54153	
	National	DM54153	
	Signetics	54153	
	TI	SN54153	
54154	AMD	SN54154	
	Fairchild	54154	
	Motorola	MC54154	
	National	DM54154	
	Signetics	54154	
	TI	SN54154	
54155	Fairchild	54155	
	ITT	ITT54155	
	Motorola	MC54155	
	National	DM54155	
	Signetics	54155	
	TI	SN54155	
54156	Fairchild	54156	
	ITT	ITT54156	
	Motorola	MC54156	
	National	DM54156	
	Signetics	54156	
	TI	SN54156	
54157	AMD	SN54157	
	Fairchild	54157	
	ITT	ITT54157	
	Motorola	MC54157	
	National	DM54157	
	Signetics	54157	
	TI	SN54157	
54158	Signetics	54158	
54159	TI	SN54159	
54160	AMD	SN54160	
	Fairchild	54160	
	ITT	ITT54160	
	Motorola	MC54160	
	National	DM54160	
	Signetics	54160	
	TI	SN54160	
54161	AMD	SN54161	
	Fairchild	54161	
	ITT	ITT54161	
	Motorola	MC54161	
	National	DM54161	
	Signetics	54161	
	TI	SN54161	
54162	AMD	SN54162	
	Fairchild	54162	
	ITT	ITT54162	
	Motorola	MC54162	
	National	DM54162	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
54162	Signetics	54162	
	TI	SN54162	
54163	AMD	SN54163	
	Fairchild	54163	
	ITT	ITT54163	
	Motorola	MC54163	
	National	DM54163	
	Signetics	54163	
	TI	SN54163	
54164	AMD	SN54164	
	Fairchild	54164	
	ITT	ITT54164	
	National	DM54164	
	Signetics	54164	
	TI	SN54164	
54165	Fairchild	54165	
	Motorola	MC54165	
	National	DM54165	
	Signetics	54165	
	TI	SN54165	
54166	Fairchild	54166	
	National	DM54166	
	Signetics	54166	
	TI	SN54166	
54170	Fairchild	54170	
	National	DM54170	
	Signetics	54170	
	TI	SN54170	
54174	AMD	SN74174	
	Fairchild	54174	
	Motorola	MC54174	
	National	DM54174	
	Signetics	54174	
	TI	SN54174	
54175	AMD	SN54175	
	Fairchild	54175	
	Motorola	MC54175	
	National	DM54175	
	Signetics	54175	
	TI	SN54175	
54180	Fairchild	54180	
	ITT	ITT54180	
	Motorola	MC54180	
	National	DM54180	
	Signetics	54180	
	TI	SN54180	
54181	AMD	SN54181	
	Fairchild	54181	
	Motorola	MC54181	
	National	DM54181	
	Signetics	54181	
	TI	SN54181	
54182	AMD	SN54182	
	Fairchild	54182	
	ITT	ITT54182	
	Motorola	MC54182	
	National	DM54182	
	Signetics	54182	
	TI	SN54182	
54190	Fairchild	54190	
	ITT	ITT54190	
	Motorola	MC54190	
	National	DM54190	
	Signetics	54190	
	TI	SN54190	
54191	Fairchild	54191	
	ITT	ITT54191	
	Motorola	MC54191	
	National	DM54191	
	Signetics	54191	
	TI	SN54191	
54192	AMD	SN54192	
	Fairchild	54192	
	ITT	ITT54192	
	Motorola	MC54192	
	National	DM54192	
	Signetics	54192	
	TI	SN54192	
54193	AMD	SN54193	
	Fairchild	54193	
	ITT	ITT54193	
	Motorola	MC54193	
54193	National	DM54193	
	Signetics	54193	
	TI	SN54193	
54195	AMD	SN54195	
	Fairchild	54195	
	ITT	ITT54195	
	Motorola	MC54195	
	National	DM54195	
	Signetics	54195	
	TI	SN54195	
54198	Fairchild	54198	
	National	DM54198	
	Signetics	54198	
	TI	SN54198	
54199	Fairchild	54199	
	National	DM54199	
	Signetics	54199	
	TI	SN54199	
5420	Fairchild	5420	
	ITT	ITT5420	
	Motorola	MC5420	
	National	DM5420	
	Signetics	5420	
	TI	SN5420	
5421	Fairchild	5421	
	ITT	ITT5421	
	Signetics	5421	
5422	Fairchild	5422	
	TI	SN5422	
54283	Fairchild	54283	
	TI	SN54283	
5437	Fairchild	5437	
	ITT	ITT5437	
	Motorola	MC5437	
	National	DM5437	
	Signetics	5437	
	TI	SN5437	
5438	Fairchild	5438	
	ITT	ITT5438	
	Motorola	MC5438	
	National	DM5438	
	Signetics	5438	
	TI	SN5438	
5442	Fairchild	5442	
	ITT	ITT5442	
	Motorola	MC5442	
	National	DM5442	
	Signetics	5442	
	TI	SN5442	
5443	Fairchild	5443	
	ITT	ITT5443	
	Motorola	MC5443	
	Signetics	5443	
	TI	SN5443	
5444	Fairchild	5444	
	ITT	ITT5444	
	Motorola	MC5444	
	Signetics	5444	
	TI	SN5444	
5445	Fairchild	5445	
	ITT	ITT5445	
	Motorola	MC5445	
	National	DM5445	
	Signetics	5445	
	TI	SN5445	
5474	Fairchild	5474	
	ITT	ITT5474	
	Motorola	MC5474	
	National	DM5474	
	Signetics	5474	
	TI	SN5474	
5486	Fairchild	5486	
	ITT	ITT5486	
	Motorola	MC5486	
	National	DM5486	
	Signetics	5486	
	TI	SN5486	
74H00	Fairchild	74H00	
	National	DM74H00	
	NEC America	μPB74H00	
	Signetics	74H00	
	TI	SN74H00	
74H01	Fairchild	74H01	
	ITT	ITT74H01	
	National	DM74H01	
	NEC America	μPB74H01	
74H01	Signetics	74H01	
	TI	SN74H01	
74H04	Fairchild	74H04	
	ITT	ITT74H04	
	National	DM74H04	
	NEC America	μPB74H04	
	Signetics	74H04	
	TI	SN74H04	
74H05	Fairchild	74H05	
	ITT	ITT74H05	
	National	DM74H05	
	TI	SN74H05	
74H10	Fairchild	74H10	
	ITT	ITT74H10	
	National	DM74H10	
	NEC America	μPB74H10	
	Signetics	74H10	
	TI	SN74H10	
74H11	Fairchild	74H11	
	ITT	ITT74H11	
	National	DM74H11	
	Signetics	74H11	
	TI	SN74H11	
74H15	Fairchild	74H15	
	TI	SN74H15	
74H20	Fairchild	74H20	
	ITT	ITT74H20	
	National	DM74H20	
	NEC America	μPB74H20	
	Signetics	74H20	
	TI	SN74H20	
74H22	Fairchild	74H22	
	National	DM74H22	
	Signetics	74H22	
	TI	SN74H22	
74H40	Fairchild	74H40	
	ITT	ITT74H40	
	National	DM74H40	
	NEC America	μPB74H40	
	Signetics	74H40	
	TI	SN74H40	
74H74	Fairchild	74H74	
	ITT	ITT74H74	
	National	DM74H74	
	Signetics	74H74	
	TI	SN74H74	
74LS00	Fairchild	74LS00	
	ITT	ITT74LS00	
	Motorola	SN74LS00	
	National	DM74LS00	
	NEC America	μPB74LS00	
	Signetics	74LS00	
	TI	SN74LS00	
74LS01	Fairchild	74LS01	
	ITT	ITT74LS01	
	National	DM74LS01	
	Signetics	74LS01	
	TI	SN74LS01	
74LS02	Fairchild	74LS02	
	ITT	ITT74LS02	
	Motorola	SN74LS02	
	National	DM74LS02	
	NEC America	μPB74LS02	
	Signetics	74LS02	
	TI	SN74LS02	
74LS03	Fairchild	74LS03	
	ITT	ITT74LS03	
	Motorola	SN74LS03	
	National	DM74LS03	
	NEC America	μPB74LS03	
	Signetics	74LS03	
	TI	SN74LS03	
74LS04	Fairchild	74LS04	
	ITT	ITT74LS04	
	Motorola	SN74LS04	
	National	DM74LS04	
	NEC America	μPB74LS04	
	Signetics	74LS04	
	TI	SN74LS04	
74LS05	Fairchild	74LS05	
	ITT	ITT74LS05	
	Motorola	SN74LS05	
	National	DM74LS05	
	NEC America	μPB74LS05	
	Signetics	74LS05	
	TI	SN74LS05	
74LS08	Fairchild	74LS08	
	ITT	ITT74LS08	
	Motorola	SN74LS08	
	National	DM74LS08	
	NEC America	μPB74LS08	
	Signetics	74LS08	
	TI	SN74LS08	
74LS09	Fairchild	74LS09	
	ITT	ITT74LS09	
	Motorola	SN74LS09	
	National	DM74LS09	
	Signetics	74LS09	
	TI	SN74LS09	
74LS10	Fairchild	74LS10	
	ITT	ITT74LS10	
	Motorola	SN74LS10	
	National	DM74LS10	
	NEC America	μPB74LS10	
	Signetics	74LS10	
	TI	SN74LS10	
74LS107	Fairchild	74LS107	
	ITT	ITT74LS107	
	National	DM74LS107	
	Signetics	74LS107	
	TI	SN74LS107	
74LS109	Fairchild	74LS109	
	ITT	ITT74LS109A	
	Motorola	SN74LS109	
	National	DM74LS109	
	NEC America	μPB74LS109	
	Signetics	74LS109	
	TI	SN74LS109	
74LS11	Fairchild	74LS11	
	ITT	ITT74LS11	
	Motorola	SN74LS11	
	National	DM74LS11	
	NEC America	μPB74LS11	
	Signetics	74LS11	
	TI	SN74LS11	
74LS112	Fairchild	74LS112	
	ITT	ITT74LS112	
	National	DM74LS112	
	NEC America	μPB74LS112	
	Signetics	74LS112	
	TI	SN74LS112	
74LS113	Fairchild	74LS113	
	ITT	ITT74LS113	
	National	DM74LS113	
	NEC America	μPB74LS113	
	Signetics	74LS113	
	TI	SN74LS113	
74LS114	Fairchild	74LS114	
	ITT	ITT74LS114	
	Motorola	SN74LS114	
	National	DM74LS114	
	Signetics	74LS114	
	TI	SN74LS114	
74LS12	Fairchild	74LS12	
	National	DM74LS12	
	Signetics	74LS12	
	TI	SN74LS12	
74LS122	National	DM74LS122	
	TI	SN74LS122	
74LS123	AMD	SN74LS123	
	ITT	ITT74LS123	
	National	DM74LS123	
	TI	SN74LS123	
74LS125	Fairchild	74LS125	
	ITT	ITT74LS125	
	National	DM74LS125	
	Signetics	74LS125	
	TI	SN74LS125A	
74LS126	Fairchild	74LS126	
	ITT	ITT74LS126	
	Motorola	SN74LS126	
	National	DM74LS126	
	Signetics	74LS126	
	TI	SN74LS126A	
74LS13	Fairchild	74LS13	
	ITT	ITT74LS13	
	Motorola	SN74LS13	
	National	DM74LS13	
	Signetics	74LS13	
	TI	SN74LS13	
74LS132	Fairchild	74LS132	
	ITT	ITT74LS132	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Raytheon Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Replacement Device	IC Master Page
74LS132	Motorola	SN74LS132	
	National	DM54LS132	
		DM74LS132	
	Signetics	74LS132	
	TI	SN74LS132	
74LS136	Fairchild	74LS136	
	ITT	ITT74LS136	
	Motorola	SN74LS136	
	National	DM74LS136	
	Signetics	74LS136	
	TI	SN74LS136	
74LS138	AMD	SN74LS138	
	Fairchild	74LS138	
	ITT	ITT74LS138	
	Motorola	SN74LS138	
	National	DM74LS138	
	NEC America	μPB74LS138	
	Signetics	74LS138	
	TI	SN74LS138	
74LS139	AMD	SN74LS139	
	Fairchild	74LS139	
	ITT	ITT74LS139	
	Motorola	SN74LS139	
	National	DM74LS139	
	NEC America	μPB74LS139	
	Signetics	74LS139	
	TI	SN74LS139	
74LS14	Fairchild	74LS14	
	ITT	ITT74LS14	
	Motorola	SN74LS14	
	National	DM74LS14	
	Signetics	74LS14	
	TI	SN74LS14	
74LS15	Fairchild	74LS15	
	ITT	ITT74LS15	
	Motorola	SN74LS15	
	National	DM74LS15	
	Signetics	74LS15	
	TI	SN74LS15	
74LS151	AMD	SN74LS151	
	Fairchild	74LS151	
	ITT	ITT74LS151	
	Motorola	SN74LS151	
	National	DM74LS151	
	NEC America	μPB74LS151	
	Signetics	74LS151	
	TI	SN74LS151	
74LS152	Fairchild	74LS152	
	Motorola	SN74LS152	
74LS153	AMD	SN74LS153	
	Fairchild	74LS153	
	ITT	ITT74LS153	
	Motorola	SN74LS153	
	National	DM74LS153	
	NEC America	μPB74LS153	
	Signetics	74LS153	
	TI	SN74LS153	
74LS155	Fairchild	54LS155	
		74LS155	
	ITT	ITT74LS155	
	Motorola	SN54LS155	
		SN74LS155	
	National	DM54LS155	
		DM74LS155	
	NEC America	μPB74LS155	
	Signetics	74LS155	
	TI	SN54LS155	
		SN74LS155	
74LS156	Fairchild	74LS156	
	ITT	ITT74LS156	
	Motorola	SN74LS156	
	National	DM74LS156	
	Signetics	74LS156	
	TI	SN74LS156	
74LS157	AMD	SN74LS157	
	Fairchild	74LS157	
	ITT	ITT74LS157	
	Motorola	SN74LS157	
	National	DM74LS157	
	NEC America	μPB74LS157	
	Signetics	74LS157	
	TI	SN74LS157	
74LS158	AMD	SN74LS158	
	Fairchild	74LS158	
	ITT	ITT74LS158	
	Motorola	SN74LS158	
	National	DM74LS158	
	Signetics	74LS158	
	TI	SN74LS158	
74LS160	AMD	SN74LS160	
	Fairchild	74LS160	
	ITT	ITT74LS160	
	Motorola	SN74LS160	
	National	DM74LS160	
	Signetics	74LS160	
	TI	SN74LS160	
74LS161	AMD	SN74LS161	
	Fairchild	74LS161	
	ITT	ITT74LS161	
	Motorola	SN74LS161	
	National	DM74LS161	
	NEC America	μPB74LS161	
	Signetics	74LS161	
	TI	SN74LS161	
74LS162	AMD	SN74LS162	
	Fairchild	74LS162	
	ITT	ITT74LS162	
	Motorola	SN74LS162	
	National	DM74LS162	
	Signetics	74LS162	
	TI	SN74LS162	
74LS163	AMD	SN74LS163	
	Fairchild	74LS163	
	ITT	ITT74LS163	
	Motorola	SN74LS163	
	National	DM74LS163	
	Signetics	74LS163	
	TI	SN74LS163	
74LS164	AMD	SN74LS164	
	Fairchild	74LS164	
	ITT	ITT74LS164	
	Motorola	SN74LS164	
	National	DM74LS164	
	NEC America	μPB74LS164	
	Signetics	74LS164	
	TI	SN74LS164	
74LS170	AMD	SN74LS170	
	Fairchild	74LS170	
	ITT	ITT74LS170	
	Motorola	SN74LS170	
	National	DM74LS170	
	Signetics	74LS170	
	TI	SN74LS170	
74LS174	AMD	SN74LS174	
	Fairchild	74LS174	
	ITT	ITT74LS174	
	Motorola	SN74LS174	
	National	DM74LS174	
	Signetics	74LS174	
	TI	SN74LS174	
74LS175	AMD	SN74LS175	
	Fairchild	74LS175	
	ITT	ITT74LS175	
	Motorola	SN74LS175	
	National	DM74LS175	
	NEC America	μPB74LS175	
	Signetics	74LS175	
	TI	SN74LS175	
74LS181	AMD	SN74LS181	
	Fairchild	74LS181	
	Motorola	SN74LS181	
	Signetics	74LS181	
	TI	SN74LS181	
74LS190	AMD	SN74LS190	
	Fairchild	74LS190	
	ITT	ITT74LS190	
	Motorola	SN74LS190	
	National	DM74LS190	
	Signetics	74LS190	
	TI	SN74LS190	
74LS191	AMD	SN74LS191	
	Fairchild	74LS191	
	ITT	ITT74LS191	
	Motorola	SN74LS191	
	National	DM74LS191	
	Signetics	74LS191	
	TI	SN74LS191	
74LS192	AMD	SN74LS192	
	Fairchild	74LS192	
	ITT	ITT74LS192	
	Motorola	SN74LS192	
	National	DM74LS192	
	NEC America	μPB74LS192	
	Signetics	74LS192	
	TI	SN74LS192	
74LS193	AMD	SN74LS193	
	Fairchild	74LS193	
	ITT	ITT74LS193	
	Motorola	SN74LS193	
	National	DM74LS193	
	NEC America	μPB74LS193	
	Signetics	74LS193	
	TI	SN74LS193	
74LS194A	AMD	SN74LS194A	
	Fairchild	74LS194	
	ITT	ITT74LS194A	
	Motorola	SN74LS194	
	NEC America	μPB74LS194	
	Signetics	74LS194A	
	TI	SN74LS194A	
74LS195A	AMD	SN74LS195A	
	Fairchild	74LS195	
	ITT	ITT74LS195A	
	Motorola	SN74LS195	
	NEC America	μPB74LS195	
	Signetics	74LS195A	
	TI	SN74LS195A	
74LS196	Fairchild	74LS196	
	ITT	ITT74LS196	
	Motorola	SN74LS196	
	National	DM74LS196	
	Signetics	74LS196	
	TI	SN74LS196	
74LS197	Fairchild	74LS197	
	ITT	ITT74LS197	
	Motorola	SN74LS197	
	National	DM74LS197	
	Signetics	74LS197	
	TI	SN74LS197	
74LS20	Fairchild	74LS20	
	ITT	ITT74LS20	
	Motorola	SN74LS20	
	National	DM74LS20	
	NEC America	μPB74LS20	
	Signetics	74LS20	
	TI	SN74LS20	
74LS21	Fairchild	74LS21	
	ITT	ITT74LS21	
	Motorola	SN74LS21	
	National	DM74LS21	
	NEC America	μPB74LS21	
	Signetics	74LS21	
	TI	SN74LS21	
74LS22	Fairchild	74LS22	
	ITT	ITT74LS22	
	Motorola	SN74LS22	
	National	DM74LS22	
	Signetics	74LS22	
	TI	SN74LS22	
74LS221	Fairchild	74LS221	
	ITT	ITT74LS221	
	Motorola	SN74LS221	
	National	DM74LS221	
	Signetics	74LS221	
	TI	SN74LS221	
74LS240	AMD	SN74LS240	
	Fairchild	74LS240	
	ITT	ITT74LS240	
	MMI	74LS240	
	Motorola	SN74LS240	
	Signetics	74LS240	
	TI	SN74LS240	
74LS241	AMD	SN74LS241	
	Fairchild	74LS241	
	ITT	ITT74LS241	
	MMI	74LS241	
	Motorola	SN74LS241	
	Signetics	74LS241	
	TI	SN74LS241	
74LS242	AMD	SN74LS242	
	Fairchild	74LS242	
	ITT	ITT74LS242	
	Motorola	SN74LS242	
	Signetics	74LS242	
74LS242	TI	SN74LS242	
74LS243	AMD	SN74LS243	
	Fairchild	74LS243	
	ITT	ITT74LS243	
	Motorola	SN74LS243	
	Signetics	74LS243	
	TI	SN74LS243	
74LS244	AMD	SN74LS244	
	Fairchild	74LS244	
	ITT	ITT74LS244	
	MMI	74LS244	
	Motorola	SN74LS244	
	Signetics	74LS244	
	TI	SN74LS244	
74LS251	AMD	SN74LS251	
	Fairchild	74LS251	
	ITT	ITT74LS251	
	Motorola	SN74LS251	
	National	DM74LS251	
	NEC America	μPB74LS251	
	Signetics	74LS251	
	TI	SN74LS251	
74LS253	AMD	SN74LS253	
	Fairchild	74LS253	
	ITT	ITT74LS253	
	Motorola	SN74LS253	
	National	DM74LS253	
	NEC America	μPB74LS253	
	Signetics	74LS253	
	TI	SN74LS253	
74LS257	AMD	SN74LS257	
	Fairchild	74LS257	
	ITT	ITT74LS257	
	Motorola	SN74LS257	
	National	DM74LS257	
	NEC America	μPB74LS257	
	Signetics	74LS257	
	TI	SN74LS257	
74LS258	AMD	SN74LS258	
	Fairchild	74LS258	
	ITT	ITT74LS258	
	Motorola	SN74LS258	
	National	DM74LS258	
	NEC America	μPB74LS258	
	Signetics	74LS258	
	TI	SN74LS258	
74LS26	Fairchild	74LS26	
	National	DM74LS26	
	Signetics	74LS26	
	TI	SN74LS26	
74LS261	ITT	ITT74LS261	
	Signetics	74LS261	
	TI	SN74LS261	
74LS266	Fairchild	74LS266	
	ITT	ITT74LS266	
	Motorola	SN74LS266	
	Signetics	74LS266	
	TI	SN74LS266	
74LS27	Fairchild	74LS27	
	ITT	ITT74LS27	
	Motorola	SN74LS27	
	National	DM74LS27	
	NEC America	μPB74LS27	
	Signetics	74LS27	
	TI	SN74LS27	
74LS279	Fairchild	54LS279	
		74LS279	
	ITT	ITT74LS279	
	Motorola	SN54LS279	
		SN74LS279	
	National	DM54LS279	
		DM74LS279	
	NEC America	μPB74LS279	
	Signetics	54LS279	
		74LS279	
	TI	SN54LS279	
		SN74LS279	
74LS28	Fairchild	74LS28	
	ITT	ITT74LS28	
	Signetics	74LS28	
	TI	SN74LS28	
74LS283	Fairchild	74LS283	
	ITT	ITT74LS283	
	Motorola	SN74LS283	
	National	DM74LS283	
	Signetics	74LS283	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Raytheon Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
74LS283	TI	SN74LS283	
74LS295A	Fairchild	74LS295	
	Motorola	SN74LS295	
	NEC America	μPB74LS295	
	Signetics	74LS295	
	TI	SN74LS295B	
74LS298	Fairchild	74LS298	
	Motorola	SN74LS298	
	Signetics	74LS298	
	TI	SN74LS298	
74LS299	AMD	SN74LS299	
	Fairchild	74LS299	
	ITT	ITT74LS299	
	TI	SN74LS299	
74LS30	Fairchild	74LS30	
	ITT	ITT74LS30	
	Motorola	SN74LS30	
	National	DM74LS30	
	NEC America	μPB74LS30	
	Signetics	74LS30	
	TI	SN74LS30	
74LS32	Fairchild	74LS32	
	ITT	ITT74LS32	
	Motorola	SN74LS32	
	National	DM74LS32	
	NEC America	μPB74LS32	
	Signetics	74LS32	
	TI	SN74LS32	
74LS323	AMD	SN74LS323	
	ITT	ITT74LS323	
	TI	SN74LS323	
74LS33	Signetics	74LS33	
	TI	SN74LS33	
74LS365	Fairchild	74LS365	
	ITT	ITT74LS365	
	Motorola	SN74LS365	
	National	DM74LS365	
	NEC America	μPB74LS365	
	Signetics	74LS365	
	TI	SN74LS365	
74LS366	Fairchild	74LS366	
	ITT	ITT74LS366	
	Motorola	SN74LS366	
	National	DM74LS366	
	NEC America	μPB74LS366	
	Signetics	74LS366	
	TI	SN74LS366	
74LS367	Fairchild	74LS367	
	ITT	ITT74LS367	
	Motorola	SN74LS367	
	National	DM74LS367	
	NEC America	μPB74LS367	
	Signetics	74LS367	
	TI	SN74LS367	
74LS368	Fairchild	74LS368	
	ITT	ITT74LS368	
	Motorola	SN74LS368	
	National	DM74LS368	
	NEC America	μPB74LS368	
	Signetics	74LS368	
	TI	SN74LS368	
74LS37	Fairchild	74LS37	
	ITT	ITT74LS37	
	Motorola	SN74LS37	
	National	DM74LS37	
	NEC America	μPB74LS37	
	Signetics	74LS37	
	TI	SN74LS37	
74LS373	AMD	SN74LS373	
	Fairchild	74LS373	
	ITT	ITT74LS373	
	MMI	74LS373	
	Signetics	74LS373	
	TI	SN74LS373	
74LS374	AMD	SN74LS374	
	Fairchild	74LS374	
	ITT	ITT74LS374	
	MMI	74LS374	
	TI	SN74LS374	
74LS375	ITT	ITT74LS375	
	Motorola	SN74LS375	
	NEC America	μPB74LS375	
74LS375	Signetics	74LS375	
	TI	SN74LS375	
74LS377	AMD	SN74LS377	
	Fairchild	74LS377	
	ITT	ITT74LS377	
	Signetics	74LS377	
	TI	SN74LS377	
74LS38	Fairchild	74LS38	
	ITT	ITT74LS38	
	Motorola	SN74LS38	
	National	DM74LS38	
	NEC America	μPB74LS38	
	Signetics	74LS38	
	TI	SN74LS38	
74LS386	Fairchild	74LS386	
	ITT	ITT74LS386	
	Motorola	SN74LS386	
	National	DM74LS386	
	Signetics	74LS386	
	TI	SN74LS386	
74LS395	Fairchild	74LS395	
	National	DM74LS395	
	Signetics	74LS395	
	TI	SN74LS395	
74LS40	Fairchild	74LS40	
	ITT	ITT74LS40	
	Motorola	SN74LS40	
	National	DM74LS40	
	NEC America	μPB74LS40	
	Signetics	74LS40	
	TI	SN74LS40	
74LS42	Fairchild	74LS42	
	ITT	ITT74LS42	
	Motorola	SN74LS42	
	National	DM74LS42	
	NEC America	μPB74LS42	
	Signetics	74LS42	
	TI	SN74LS42	
74LS51	Fairchild	74LS51	
	ITT	ITT74LS51	
	Motorola	SN74LS51	
	National	DM74LS51	
	NEC America	μPB74LS51	
	Signetics	74LS51	
	TI	SN74LS51	
74LS54	Fairchild	74LS54	
	ITT	ITT74LS54	
	Motorola	SN74LS54	
	National	DM74LS54	
	NEC America	μPB74LS54	
	Signetics	74LS54	
	TI	SN74LS54	
74LS55	Fairchild	74LS55	
	Motorola	SN74LS55	
	National	DM74LS55	
	NEC America	μPB74LS55	
	Signetics	74LS55	
	TI	SN74LS55	
74LS670	AMD	SN74LS670	
	Fairchild	74LS670	
	Motorola	SN74LS670	
	National	DM74LS670	
	Signetics	74LS670	
	TI	SN74LS670	
74LS73	Fairchild	74LS73	
	ITT	ITT74LS73	
	Motorola	SN74LS73	
	National	DM74LS73	
	Signetics	74LS73	
	TI	SN74LS73	
74LS74	Fairchild	74LS74	
	ITT	ITT74LS74	
	Motorola	SN74LS74	
	National	DM74LS74	
	NEC America	μPB74LS74	
	Signetics	74LS74	
	TI	SN74LS74	
74LS75	Fairchild	74LS75	
	ITT	ITT74LS75	
	National	DM74LS75	
	Signetics	74LS75	
	TI	SN74LS75	
74LS76	ITT	ITT74LS76	
	National	DM74LS76	
	Signetics	74LS76	
	TI	SN74LS76	
74LS78	ITT	ITT74LS78	
	National	DM74LS78	
	Signetics	74LS76	
	TI	SN74LS78	
74LS83A	Fairchild	74LS83	
	ITT	ITT74LS83A	
	Motorola	SN74LS83	
	National	DM74LS83	
		DM74LS83A	
	Signetics	74LS83	
	TI	SN74LS83A	
74LS85	Fairchild	74LS85	
	ITT	ITT74LS85	
	Motorola	SN74LS85	
	National	DM74LS85	
	Signetics	74LS85	
	TI	SN74LS85	
74LS86	Fairchild	74LS86	
	ITT	ITT74LS86	
	Motorola	SN74LS86	
	NEC America	μPB74LS86	
	Signetics	74LS86	
	TI	SN74LS86	
74LS90	Fairchild	74LS90	
	ITT	ITT74LS90	
	Motorola	SN74LS90	
	National	DM74LS90	
	Signetics	74LS90	
	TI	SN74LS90	
74LS91	TI	SN74LS91	
74LS92	Fairchild	74LS92	
	Motorola	SN74LS92	
	National	DM74LS92	
	Signetics	74LS92	
	TI	SN74LS92	
74LS93	Fairchild	74LS93	
	ITT	ITT74LS93	
	Motorola	SN74LS93	
	National	DM74LS93	
	Signetics	74LS93	
	TI	SN74LS93	
74LS95B	Fairchild	74LS95	
	ITT	ITT74LS95B	
	Motorola	SN74LS95	
	National	DM74LS95B	
	Signetics	74LS95B	
	TI	SN74LS95B	
74S240	AMD	SN74S240	
	MMI	**74S240**	**462**
	TI	SN74S240	
74S241	AMD	SN74S241	
	MMI	**74S241**	**462**
	TI	SN74S241	
74S244	AMD	SN74S244	
	MMI	**74S244**	**462**
7400	Fairchild	7400	
	Hitachi	HD7400	
	ITT	ITT7400	
	Mitsubishi	M53200	
	Motorola	MC7400	
	National	DM7400	
	NEC America	μPB7400	
	Signetics	7400	
	TI	SN7400	
	Toshiba	TC7400	
	TRW	7400	
7401	Fairchild	7401	
	ITT	ITT7401	
	Mitsubishi	M53201	
	Motorola	MC7401	
	National	DM7401	
	Signetics	7401	
	TI	SN7401	
	TRW	7401	
7403	Fairchild	7403	
	Hitachi	HD7403	
	ITT	ITT7403	
	Mitsubishi	M53203	
	Motorola	MC7403	
	National	DM7403	
	Signetics	7403	
	TI	SN7403	
	TRW	7403	
7404	Fairchild	7404	
	Hitachi	HD7404	
	ITT	ITT7404	
7404	Mitsubishi	M53204	
	Motorola	MC7404	
	National	DM7404	
	NEC America	μPB7404	
	Signetics	7404	
	TI	SN7404	
	Toshiba	TC7404	
	TRW	7404	
7405	Fairchild	7405	
	Hitachi	HD7405	
	ITT	ITT7405	
	Mitsubishi	M53205	
	Motorola	MC7405	
	National	DM7405	
	NEC America	μPB7405	
	Signetics	7405	
	TI	SN7405	
	TRW	7405	
7408	Fairchild	7408	
	ITT	ITT7408	
	Mitsubishi	M53208	
	Motorola	MC7408	
	National	DM7408	
	Signetics	7408	
	TI	SN7408	
	Toshiba	TC7408	
	TRW	7408	
7409	Fairchild	7409	
	Hitachi	HD7409	
	ITT	ITT7409	
	Mitsubishi	M53209	
	Motorola	MC7409	
	National	DM7409	
	Signetics	7409	
	TI	SN7409	
	TRW	7409	
7410	Fairchild	7410	
	Hitachi	HD7410	
	ITT	ITT7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
	National	DM7410	
	NEC America	μPB7410	
	Signetics	7410	
	TI	SN7410	
		SN7427	
	Toshiba	TC7410	
	TRW	7410	
7411	Fairchild	7411	
	Hitachi	HD7411	
	ITT	ITT7411	
	National	DM7411	
	Signetics	7411	
7412	Fairchild	7412	
	Hitachi	HD7412	
	ITT	ITT7412	
	Signetics	7412	
	TI	SN7412	
	TRW	7412	
74123	AMD	SN74123	
	Fairchild	74123	
	ITT	ITT74123	
	Mitsubishi	M53323	
	Motorola	MC74123	
	National	DM74123	
	NEC America	μPB74123	
	Signetics	74123	
	TI	SN74123	
	TRW	74123	
74136	Hitachi	HD74136	
	Motorola	MC74136	
	TI	SN74136	
	TRW	74136	
74145	Fairchild	74145	
	ITT	ITT74145	
	Mitsubishi	M53345	
	Motorola	MC74145	
	National	DM74145	
	Signetics	74145	
	TI	SN74145	
	TRW	74145	
74150	Fairchild	74150	
	Hitachi	HD74150	
	Mitsubishi	M53350	
	Motorola	MC74150	
	National	DM74150	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Raytheon Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
74150	NEC America	μPB74150	
	Signetics	74150	
	TI	SN74150	
	TRW	74150	
74151	Fairchild	74151	
	Hitachi	HD74151	
	ITT	ITT74151	
	Mitsubishi	M53351	
	Motorola	MC74151	
	National	DM74151	
	NEC America	μPB74151	
	Signetics	74151	
	TI	SN74151	
	TRW	74151	
74152	Fairchild	74152	
	Motorola	MC74152	
	TRW	74152	
74153	Fairchild	74153	
	ITT	ITT74153	
	Mitsubishi	M53353	
	Motorola	MC74153	
	National	DM74153	
	NEC America	μPB74153	
	Signetics	74153	
	TI	SN74153	
	TRW	74153	
74154	AMD	SN74154	
	Fairchild	74154	
	Mitsubishi	M53354	
	Motorola	MC74154	
	National	DM74154	
	NEC America	μPB74154	
	Signetics	74154	
	TI	SN74154	
	TRW	74154	
74155	Fairchild	74155	
	ITT	ITT74155	
	Mitsubishi	M53355	
	Motorola	MC74155	
	National	DM74155	
	NEC America	μPB74155	
	Signetics	74155	
	TI	SN74155	
	TRW	74155	
74156	Fairchild	74156	
	Hitachi	HD74156	
	ITT	ITT74156	
	Mitsubishi	M53356	
	Motorola	MC74156	
	National	DM74156	
	NEC America	μPB74156	
	Signetics	74156	
	TI	SN74156	
	TRW	74156	
74157	AMD	SN74157	
	Fairchild	74157	
	Hitachi	HD74157	
	ITT	ITT74157	
	Mitsubishi	M53357	
	Motorola	MC74157	
	National	DM74157	
	NEC America	μPB74157	
	Signetics	74157	
	TI	SN74157	
74158	Mitsubishi	M53358	
	Signetics	74158	
74159	TI	SN74159	
74160	AMD	SN74160	
	Fairchild	74160	
	Hitachi	HD74160	
	ITT	ITT74160	
	Mitsubishi	M53360	
	Motorola	MC74160	
	National	DM74160	
	Signetics	74160	
	TI	SN74160	
	TRW	74160	
74161	AMD	SN74161	
	Fairchild	74161	
	Hitachi	HD74161	
	ITT	ITT74161	
	Mitsubishi	M53361	
74161	Motorola	MC74161	
	National	DM74161	
	NEC America	μPB74161	
	Signetics	74161	
	TI	SN74161	
	TRW	74161	
74162	AMD	SN74162	
	Fairchild	74162	
	Hitachi	HD74162	
	ITT	ITT74162	
	Mitsubishi	M53362	
	Motorola	MC74162	
	National	DM74162	
	Signetics	74162	
	TI	SN74162	
	TRW	74162	
74163	AMD	SN74163	
	Fairchild	74163	
	Hitachi	HD74163	
	ITT	ITT74163	
	Mitsubishi	M53363	
	Motorola	MC74163	
	National	DM74163	
	Signetics	74163	
	TI	SN74163	
	TRW	74163	
74164	AMD	74164	
	Fairchild	74164	
	Hitachi	HD74164	
	ITT	ITT74164	
	Mitsubishi	M53364	
	National	DM74164	
	NEC America	μPB74164	
	Signetics	74164	
	TI	SN74164	
74165	Fairchild	74165	
	Mitsubishi	M53365	
	Motorola	MC74165	
	National	DM74165	
	Signetics	74165	
	TI	SN74165	
74166	Fairchild	74166	
	Hitachi	HD74166	
	Mitsubishi	M53366	
	National	DM74166	
	Signetics	74166	
	TI	SN74166	
74170	Fairchild	74170	
	Mitsubishi	M53370	
	National	DM74170	
	NEC America	μPB74170	
	Signetics	74170	
	TI	SN74170	
74174	AMD	SN74174	
	Fairchild	74174	
	Hitachi	HD74174	
	Mitsubishi	M53374	
	Motorola	MC74174	
	National	DM74174	
	Signetics	74174	
	TI	SN74174	
74175	AMD	SN74175	
	Fairchild	74175	
	Hitachi	HD74175	
	Mitsubishi	M53375	
	Motorola	MC74175	
	National	DM74175	
	NEC America	μPB74175	
	Signetics	74175	
	TI	SN74175	
74180	Fairchild	74180	
	Hitachi	HD74180	
	ITT	ITT74180	
	Mitsubishi	M53380	
	Motorola	MC74180	
	National	DM74180	
	NEC America	μPB74180	
	Signetics	74180	
	TI	SN74180	
	TRW	74180	
74181	AMD	SN74181	
	Fairchild	74181	
	Mitsubishi	M53381	
	Motorola	MC74181	
	National	DM74181	
	NEC America	μPB74181	
74181	Signetics	74181	
	TI	SN74181	
74182	AMD	SN74182	
	Fairchild	74182	
	ITT	ITT74182	
	Mitsubishi	M53382	
	Motorola	MC74182	
	National	DM74182	
	NEC America	μPB74182	
	Signetics	74182	
	TI	SN74182	
74190	Fairchild	74190	
	Hitachi	HD74190	
	ITT	ITT74190	
	Mitsubishi	M53390	
	Motorola	MC74190	
	National	DM74190	
	Signetics	74190	
	TI	SN74190	
74191	Fairchild	74191	
	Hitachi	HD74191	
	ITT	ITT74191	
	Mitsubishi	M53391	
	Motorola	MC74191	
	National	DM74191	
	Signetics	74191	
	TI	SN74191	
74192	AMD	SN74192	
	Fairchild	74192	
	ITT	ITT74192	
	Mitsubishi	M53392	
	Motorola	MC74192	
	National	DM74192	
	NEC America	μPB74192	
	Signetics	74192	
	TI	SN74192	
74193	AMD	SN74193	
	Fairchild	74193	
	ITT	ITT74193	
	Mitsubishi	M53393	
	Motorola	MC74193	
	National	DM74193	
	NEC America	μPB74193	
	Signetics	74193	
	TI	SN74193	
74195	AMD	SN74195	
	Fairchild	74195	
	ITT	ITT74195	
	Motorola	MC74195	
	National	DM74195	
	NEC America	μPB74195	
	Signetics	74195	
	TI	SN74195	
74198	Fairchild	74198	
	Hitachi	HD74198	
	Mitsubishi	M53398	
	National	DM74198	
	NEC America	μPB74198	
	Signetics	74198	
	TI	SN74198	
74199	Fairchild	74199	
	Mitsubishi	M53399	
	National	DM74199	
	Signetics	74199	
	TI	SN74199	
7420	Fairchild	7420	
	Hitachi	HD7420	
	ITT	ITT7420	
	Mitsubishi	M53220	
	Motorola	MC7420	
	National	DM7420	
	NEC America	μPB7420	
	Signetics	7420	
	TI	SN7420	
	Toshiba	TC7420	
	TRW	7420	
7421	Fairchild	7421	
	ITT	ITT7421	
	Signetics	7421	
7422	Fairchild	7422	
	Hitachi	HD7422	
	TI	SN7422	
74283	Fairchild	74283	
	Mitsubishi	M53483	
	NEC America	μPB74283	
	TI	SN74283	
7437	Fairchild	7437	
	ITT	ITT7437	
	Mitsubishi	M53237	
	Motorola	MC7437	
	National	DM7437	
	NEC America	μPB7437	
	Signetics	7437	
	TI	SN7437	
	TRW	7437	
7438	Fairchild	7438	
	ITT	ITT7438	
	Mitsubishi	M53238	
	Motorola	MC7438	
	National	DM7438	
	NEC America	μPB7438	
	Signetics	7438	
	TI	SN7438	
	TRW	7438	
7442	Fairchild	7442	
	Hitachi	HD7442	
	ITT	ITT7442	
	Mitsubishi	M53242	
	Motorola	MC7442	
	National	DM7442	
	NEC America	μPB7442	
	Signetics	7442	
	TI	SN7442	
7443	Fairchild	7443	
	Hitachi	HD7443	
	ITT	ITT7443	
	Mitsubishi	M53243	
	Motorola	MC7443	
	Signetics	7443	
	TI	SN7443	
7444	Fairchild	7444	
	Hitachi	HD7444	
	ITT	ITT7444	
	Mitsubishi	M53244	
	Motorola	MC7444	
	Signetics	7444	
	TI	SN7444	
7445	Fairchild	7445	
	ITT	ITT7445	
	Mitsubishi	M53245	
	Motorola	MC7445	
	National	DM7445	
	NEC America	μPB7445	
	Signetics	7445	
	TI	SN7445	
	TRW	7445	
7474	Fairchild	7474	
	Hitachi	HD7474	
	ITT	ITT7474	
	Mitsubishi	M53274	
	Motorola	MC7474	
	National	DM7474	
	NEC America	μPB7474	
	Signetics	7474	
	TI	SN7474	
	TRW	7474	
7483	Fairchild	7483	
	ITT	ITT7483	
	Mitsubishi	M53283	
	Motorola	MC7483	
	National	DM7483	
	Signetics	7483	
	TI	SN7483	
7486	Fairchild	7486	
	Hitachi	HD7486	
	ITT	ITT7486	
	Mitsubishi	M53286	
	Motorola	MC7486	
	National	DM7486	
	NEC America	μPB7486	
	Signetics	7486	
	TI	SN7486	
	TRW	7486	
9LS00	Fairchild	9LS00	
9LS02	Fairchild	9LS02	
9LS03	Fairchild	9LS03	
9LS04	Fairchild	9LS04	
9LS05	Fairchild	9LS05	
9LS08	Fairchild	9LS08	
9LS09	Fairchild	9LS09	
9LS10	Fairchild	9LS10	
9LS109	Fairchild	9LS109	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Raytheon Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
9LS11	Fairchild	9LS11	
9LS112	Fairchild	9LS112	
9LS113	Fairchild	9LS113	
9LS114	Fairchild	9LS114	
9LS132	Fairchild	9LS132	
9LS136	Fairchild	9LS136	
9LS138	Fairchild	9LS138	
9LS139	Fairchild	9LS139	
9LS14	Fairchild	9LS14	
9LS15	Fairchild	9LS15	
9LS151	Fairchild	9LS151	
9LS152	Fairchild	9LS159	
9LS153	Fairchild	9LS153	
9LS155	Fairchild	9LS155	
9LS156	Fairchild	9LS156	
9LS157	Fairchild	9LS157	
9LS158	Fairchild	9LS158	
9LS159	Fairchild	9LS159	
9LS160	Fairchild	9LS160	
9LS161	Fairchild	9LS161	
9LS162	Fairchild	9LS162	
9LS163	Fairchild	9LS163	
9LS164	Fairchild	9LS164	
9LS170	Fairchild	9LS170	
9LS173	Fairchild	9LS173	
9LS174	Fairchild	9LS174	
9LS175	Fairchild	9LS175	
9LS181	Fairchild	9LS181	
9LS190	Fairchild	9LS190	
9LS191	Fairchild	9LS191	
9LS192	Fairchild	9LS192	
9LS193	Fairchild	9LS193	
9LS194	Fairchild	9LS194	
9LS195	Fairchild	9LS195	
9LS196	Fairchild	9LS196	
9LS197	Fairchild	9LS197	
9LS20	Fairchild	9LS20	
9LS21	Fairchild	9LS21	
9LS22	Fairchild	9LS22	
9LS251	Fairchild	9LS251	
9LS253	Fairchild	9LS253	
9LS257	Fairchild	9LS257	
9LS258	Fairchild	9LS258	
9LS259	Fairchild	9LS259	
9LS266	Fairchild	9LS266	
9LS27	Fairchild	9LS27	
9LS279	Fairchild	9LS279	
9LS283	Fairchild	9LS283	
9LS295	Fairchild	9LS295	
9LS298	AMD	9LS298	
	Fairchild	9LS298	
9LS30	Fairchild	9LS30	
9LS32	Fairchild	9LS32	
9LS37	Fairchild	9LS37	
9LS38	Fairchild	9LS38	
9LS40	Fairchild	9LS40	
9LS42	Fairchild	9LS42	
9LS51	Fairchild	9LS51	
9LS54	Fairchild	9LS54	
9LS55	Fairchild	9LS55	
9LS670	Fairchild	9LS670	
9LS73	Fairchild	9LS73	
9LS74	Fairchild	9LS74	
9LS83	Fairchild	9LS83	
9LS86	Fairchild	9LS86	
9LS93	Fairchild	9LS93	
9LS95B	Fairchild	9LS95	

RCA Solid State Division

Manufacturer Device	Replacement Source	Device	IC Master Page
CA101	AD	AD101	
	AMD	LM101	
	Fairchild	μA101	
	Intersil	LM101	
	Motorola	LM101	
	National	LM101	
	NPC	SFC2121	
	Signetics	LM101	
	Silicon G	SG101	
	TI	LM101	
CA107	AMD	LM107	
	Intersil	LM107	
	Motorola	LM107	
	National	LM107	
	Raytheon	LM107	
	Signetics	LM107	
	Silicon G	SG107	
	TI	LM107	
CA108	AMD	LM108	
	Fairchild	μA108	
	Motorola	LM108	
	National	LM108	
	PMI	**PM108**	**858**
	Raytheon	LM108	
	Signetics	LM108	
	Silicon G	SG108	
CA111	AMD	LM111	
	Intersil	LM111	
	Motorola	LM111	
	National	LM111	
	NPC	SFC2111	
	Raytheon	LM111	
	Signetics	LM111	
	Silicon G	SG111	
	TI	LM111	
CA1310	Motorola	MC1310	
	Sprague	ULN-2210	
CA1352	Motorola	MC1352	
	Sanyo	LA1352	
CA139	Motorola	LM139	
CA1391	Motorola	MC1391	
	Sprague	ULN-2291	
CA1394	Motorola	MC1394	
	Sprague	ULN-2294	
CA1398	Motorola	MC1398	
	Sprague	ULN-2298	
CA1458	Exar	XR1458	
	Fairchild	μA1458	
	Harris	**HA-2655**	**704**
	Motorola	MC1458	
	National	LM1458	
	PMI	**OP-14**	**844**
		SSS1458	**844**
	Raytheon	RC1458	
	Signetics	MC1458	
	Silicon G	SG1458	
	TI	MC1458	
CA1541	Motorola	MC1441	
CA1558	Exar	XR1558	
	Fairchild	μA1558	
	Harris	**HA-2650**	**704**
	Motorola	MC1558	
	National	LM1558	
	PMI	**PM1558**	**844**
		SSS1558	**844**
	Raytheon	RM1558	
	Signetics	MC1558	
	Silicon G	SG1558	
	TI	**MC1558**	
CA201	AD	AD201	
	AMD	LM201	
	Fairchild	μA201	
	Intersil	LM201	
	Motorola	LM201	
	National	LM201	
	Signetics	LM201	
	Silicon G	SG201	
	TI	LM201	
CA207	AMD	LM207	
	Fairchild	μA207	
	Intersil	LM207	
	Motorola	LM207	
	National	LM207	
	Raytheon	LM207	
	Signetics	LM207	
	Silicon G	SG207	
	TI	LM207	
CA208	AD	AD208	
	AMD	LM208	
	Fairchild	μA208	
	Intersil	LM208	
	Motorola	LM208	
	National	LM208	
	NPC	SFC2208	
	PMI	PM208	
	Raytheon	LM208	
	Signetics	LM208	
CA208	Silicon G	SG208	
CA211	AMD	LM211	
	Intersil	LM211	
	Motorola	LM211	
	National	LM211	
	NPC	SFC2211	
	Raytheon	LM211	
	Signetics	LM211	
	Silicon G	SG211	
	TI	LM211	
CA2111	Motorola	MC1357	
	Sprague	ULN-2111	
CA239	Motorola	LM239	
	Silicon G	SG239	
	TI	LM239	
CA301	AD	AD301	
	Fairchild	μA301	
	Intersil	LM301	
	Motorola	LM301	
	National	LM301	
	NPC	SFC2301	
	Raytheon	LM301	
	Signetics	LM301	
	Silicon G	SG301	
	TI	LM301	
CA3011	Motorola	MC1590	
CA3012	Motorola	MC1590	
CA3013	Motorola	MC1355	
CA3014	Motorola	MC1357	
CA3018	Fairchild	μA3018	
	NPC	SFC2018	
	Silicon G	SG3818	
CA3019	Fairchild	μA3019	
CA3026	Fairchild	μA3026	
	Silicon G	SG3822	
♦CA3032	Motorola	MC1712	
CA3036	Fairchild	μA3036	
	NPC	SFC2036	
CA3038	Motorola	MC1709	
CA3039	Fairchild	μA3039	
CA3044	Fairchild	μA3064	
	Mitsubishi	M5134	
CA3045	Fairchild	μA3045	
	National	LM3045	
	Plessey	SL3045	
	Silicon G	SG3045	
		SG3821	
	Sprague	ULS-2045	
CA3046	Fairchild	μA3046	
	Motorola	MC3346	
	National	LM3046	
	NPC	SFC2046	
	Plessey	SL3046	
	Silicon G	SG3046	
		SG3821	
		SG3822	
	Sprague	ULN-2046	
CA3054	Fairchild	μA3054	
	Motorola	CA3054	
	National	LM3054	
	NPC	SFC2054	
	Silicon G	SG3822	
	Sprague	ULN-2054	
CA3055	Silicon G	SG300	
CA3056	Motorola	MC1741	
CA3058	Plessey	SL447	
	Silicon G	SG3058	
CA3059	Motorola	CA3059	
	Plessey	SL448	
	Silicon G	SG3059	
CA3064	Fairchild	μA3064	
	Mitsubishi	M5135	
	Motorola	MC1364	
	Sprague	ULN-2264	
CA3065	Fairchild	μA3065	
	Motorola	MC1358	
		M5140	
	Sanyo	LA1365	
	Sprague	ULN-2165	
CA3066	Fairchild	μA3066	
CA3067	Fairchild	μA3067	
CA307	AMD	LM307	
	Fairchild	μA307	
	Intersil	LM307	
	Motorola	LM307	
	National	LM307	
CA307	Raytheon	LM307	
	Signetics	LM307	
	Silicon G	SG307	
	TI	LM307	
CA3070	Fairchild	μA780	
	Sprague	ULN-2124	
CA3071	Fairchild	μA781	
	Sprague	ULN-2127	
CA3072	Fairchild	μA746	
	Sprague	ULN-2114	
CA3075	Fairchild	μA3075	
	Motorola	MC1375	
CA3076	Fairchild	μA3076	
CA3079	Plessey	SL449	
	Silicon G	SG3079	
CA308	AD	AD308	
	AMD	LM308	
	Fairchild	μA308	
	Intersil	LM308	
	Motorola	LM308	
	National	LM308	
	NPC	SFC308	
	PMI	PM308	
	Raytheon	LM308	
	Signetics	LM308	
	Silicon G	SG308	
CA3081	Plessey	SL3081	
	Silicon G	SG3081	
	Sprague	ULN-2081	
CA3082	Plessey	SL3082	
	Silicon G	SG3082	
	Sprague	ULN-2082	
CA3083	Plessey	SL3083	
	Signetics	CA3083	
	Silicon G	SG3083	
CA3086	Fairchild	μA3086	
	Motorola	MC3386	
	National	LM3086	
	Plessey	SL3086	
	Silicon G	SG3086	
CA3089	Fairchild	μA3089	
	SGS	TDA1200	
	Signetics	CA3089	
	Sprague	ULN-2289	
CA311	AMD	LM311	
	Fairchild	μA311	
	Intersil	LM311	
	Motorola	LM311	
	National	LM311	
	NPC	SFC3111	
	Raytheon	LM311	
	Signetics	LM311	
	Silicon G	SG311	
	TI	LM311	
CA3120	Sprague	ULN-2125	
CA3121	Sprague	ULN-2269	
CA3123	Sprague	ULN-2137	
CA3126	Fairchild	μA787	
CA3140	Intersil	CA3140	
CA3146	Plessey	CA3146	
	Silicon G	SG3146	
CA3183	Plessey	CA3183	
	Signetics	CA3183	
	Silicon G	SG3183	
CA324	Motorola	LM324	
	National	LM324	
	Signetics	LM324	
	Silicon G	SG324	
	TI	LM324	
CA3302	Motorola	MC3302	
	Silicon G	SG3302	
CA339	Motorola	LM339	
	National	LM339	
	Raytheon	LM339	
	Signetics	LM339	
	Silicon G	SG339	
	TI	LM339	
CA3401	Motorola	MC3401	
♦CA3458	RCA	CA1458	
♦CA3558	RCA	CA1558	
♦CA3741	RCA	CA741	
♦CA3747	RCA	CA747	
♦CA3748	RCA	CA748	
CA555	AMD	NE555	
		SE555	
	Exar	XR555	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
CA555	Intersil	NE555	
	Motorola	MC1455	
		MC1555	
	National	LM555	
	Raytheon	RC555	
		RM555	
	Signetics	NE555	
	Silicon G	SG555	
	TI	NE555	
		SE555	
CA723	AMD	723	
	Fairchild	μA723	
	Intersil	723	
	Motorola	MC1723	
	National	LM723	
	NPC	SFC2723	
	Raytheon	RC723	
	Signetics	μA723	
	Silicon G	SG723	
	TI	μA723	
CA741	AD	AD741	
	AMD	SSS741	
		741	
	Fairchild	μA741	
	Intersil	SSS741	
		741	
	Motorola	MC1741	
	National	LM741	
	NPC	SFC2741	
	PMI	**OP-02**	**839**
		PM741	**839**
		SSS741	**839**
	Raytheon	RC741	
		RM741	
	Signetics	μA741	
	Silicon G	SG741	
	TI	μA741	
CA747	AMD	SSS747	
		747	
	Fairchild	μA747	
	Intersil	SSS747	
	Motorola	MC1747	
	National	LM747	
	PMI	**OP-04**	**844**
		PM747	**844**
		SSS747	**844**
	Raytheon	RC747	
		RM747	
	Signetics	μA747	
	Silicon G	SG747	
	TI	μA747	
CA748	AMD	748	
	Fairchild	μA748	
	Intersil	748	
	Motorola	MC1748	
	National	LM748	
	Raytheon	RC748	
		RM748	
	Signetics	μA748	
	Silicon G	SG748	
	TI	μA748	
CA758	Sprague	ULN-2244	
CA810	Motorola	MC1384	
	SGS	TBA810	
CDP1802	Hughes	HMPC1802	
CDP1822	**Harris**	**HM6501**	**1174**
CDP1824	Hughes	HCMP1824	
CDP1831	Hughes	HCMP1831	
CDP1832	Hughes	HCMP1832	
CDP1833	Hughes	HCMP1833	
CDP1834	Hughes	HCMP1834	
CDP1852	Hughes	HCMP1852	
CDP1853	Hughes	HCMP1853	
CDP1854	Hughes	HCMP1854	
CDP1856	Hughes	HCMP1856	
CDP1857	Hughes	HCMP1857	
CDP1858	Hughes	HCMP1858	
CDP1859	Hughes	HCMP1859	
CD4000	Mitel	SIL4000	
	Motorola	MC14000	
	National	CD4000	
	Solitron	CM4000	
CD4000	SSS	SCL4000	
	TI	TP4000	
CD4001	Fairchild	F4001	
	Mitel	SIL4001	
		SIL4901	
	Motorola	MC14001	
	National	CD4001	
	NEC America	μPD4001	
	SGS	HBF4001	
	Solitron	CM4001	
	SSS	SCL4001	
	TI	TP4001	
	Toshiba	TC4001	
CD4002	Fairchild	F4002	
	Mitel	SIL4002	
	Motorola	MC14002	
	National	CD4002	
	NEC America	μPD4002	
	SGS	HBF4002	
	Solitron	CM4002	
	SSS	SCL4002	
	TI	TP4002	
	Toshiba	TC4002	
CD4006	Fairchild	F4006	
	Motorola	MC14006	
	National	CD4006	
	NEC America	μPD4006	
	Solitron	CM4006	
	SSS	SCL4006	
CD4007	Fairchild	F4007	
	Mitel	SIL4007	
	Motorola	MC14007	
	National	CD4007	
	SGS	HBF4007	
	Solitron	CM4007	
	SSS	SCL4007	
	TI	TP4007	
	Toshiba	TC4007	
CD4008	Fairchild	F4008	
	Motorola	MC14008	
	National	CD4008	
	SGS	HBF4008	
	Solitron	CM4008	
	SSS	SCL4008	
	TI	TP4008	
	Toshiba	TC4008	
CD4009	Mitel	SIL4009	
	National	CD4009	
	SGS	HBF4009	
	Solitron	CM4009	
	SSS	SCL4009	
	TI	TP4009	
	Toshiba	TC4009	
CD4010	Mitel	SIL4010	
	National	CD4010	
	SGS	HBF4010	
	Solitron	CM4010	
	SSS	SCL4010	
	TI	TP4010	
	Toshiba	TC4010	
CD40100	Fairchild	F4583	
	Motorola	MC14583	
	Toshiba	TC4583	
CD40101	Fairchild	F4531	
	Motorola	MC14531	
	SSS	SCL4531	
	TI	TP4531	
CD40106	Motorola	MC14584	
	National	CD40106	
		MM74C14	
CD40108	Motorola	MC14580	
CD4011	Fairchild	F4011	
	Mitel	SIL4011	
		SIL4911	
	Motorola	MC14011	
	National	CD4011	
	NEC America	μPD4011	
	SGS	HBF4011	
	Solitron	CM4011	
	SSS	SCL4011	
	TI	TP4011	
	Toshiba	TC4011	
CD4012	Fairchild	F4012	
	Mitel	SIL4012	
		SIL4912	
	Motorola	MC14012	
CD4012	National	CD4012	
	NEC America	μPD4012	
	SGS	HBF4012	
	Solitron	CM4012	
	SSS	SCL4012	
	TI	TP4012	
	Toshiba	TC4012	
CD4013	Fairchild	F4013	
	Mitel	SIL4013	
	Motorola	MC14013	
	National	CD4013	
	NEC America	μPD4013	
	SGS	HBF4013	
	Solitron	CM4013	
	SSS	SCL4013	
	TI	TP4013	
	Toshiba	TC4013	
CD4014	Fairchild	F4014	
	Mitel	SIL4014	
	Motorola	MC14014	
	National	CD4014	
	NEC America	μPD4014	
	SGS	HBF4014	
	Solitron	CM4014	
	SSS	SCL4014	
	TI	TP4014	
	Toshiba	TC4014	
CD4015	Fairchild	F4015	
	Mitel	SIL4015	
	Motorola	MC14015	
	National	CD4015	
	NEC America	μPD4015	
	SGS	HBF4015	
	Solitron	CM4015	
	SSS	SCL4015	
	TI	TP4015	
	Toshiba	TC4015	
CD4016	AD	AD7516	
	Fairchild	F4016	
	Micro Power	MPS7516	
	Mitel	SIL4016	
	Motorola	MC14016	
		MC14584	
	National	CD4016	
		CD4584	
		MM74C14	
	Solitron	CM4016	
	SSS	SCL4016	
		SCL4584	
	TI	TP4016	
CD40160	Fairchild	F40160	
	National	CD40160	
CD40161	Fairchild	F40161	
	National	CD40161	
CD40162	Fairchild	F40162	
	National	CD40162	
CD40163	Fairchild	F40163	
	National	CD40163	
CD4017	Fairchild	F4017	
	Mitel	SIL4017	
	Motorola	MC14017	
	National	CD4017	
	NEC America	μPD4017	
	SGS	HBF4017	
	Solitron	CM4017	
	SSS	SCL4017	
	TI	TP4017	
	Toshiba	TC4017	
CD40174	Fairchild	F40174	
	National	CD40174	
CD4018	Fairchild	F4018	
		F4522	
	Mitel	SIL4018	
	Motorola	MC14018	
		MC14522	
	National	CD4018	
	SGS	HBF4018	
	Solitron	CM4018	
	SSS	SCL4018	
		SCL4522	
	TI	TP4018	
		TP4522	
	Toshiba	TC4018	
CD40181	Motorola	MC14581	
	SSS	SCL4581	
	TI	TP4581	
CD40182	Fairchild	F4582	
	Motorola	MC14582	
	SSS	SCL4582	
	TI	TP4582	
CD4019	Fairchild	F4019	
		F4519	
	Mitel	SIL4019	
	Motorola	MC14519	
	National	CD4019	
		CD4519	
	NEC America	μPD4019	
		μPD4519	
	SGS	HBF4019	
	Solitron	CM4019	
	SSS	SCL4019	
	TI	TP4019	
		TP4519	
	Toshiba	TC4019	
CD40192	Fairchild	F40192	
		F4510	
	Mitel	SIL4510	
	Motorola	MC14510	
	National	CD40192	
		CD4510	
		MM74C192	
	RCA	CD4510	
	SSS	SCL4510	
	Toshiba	TC4510	
CD40193	Fairchild	F40193	
		F4516	
	Mitel	SIL4516	
	Motorola	MC14516	
	National	CD40193	
		CD4516	
		MM74C193	
	RCA	CD4516	
	SSS	SCL4516	
	Toshiba	TC4516	
CD40194	Fairchild	F40194	
	Motorola	MC14194	
CD40196	Fairchild	F40196	
CD4020	Fairchild	F4020	
	Mitel	SIL4020	
	Motorola	MC14020	
	National	CD4020	
	NEC America	μPD4020	
	SGS	HBF4020	
	Solitron	CM4020	
	SSS	SCL4020	
	TI	TP4020	
	Toshiba	TC4020	
CD4021	Fairchild	F4021	
	Mitel	SIL4021	
	Motorola	MC14021	
	National	CD4021	
	NEC America	μPD4021	
	Solitron	CM4021	
	SSS	SCL4021	
	TI	TP4021	
	Toshiba	TC4021	
CD4022	Fairchild	F4022	
	Mitel	SIL4022	
	Motorola	MC14022	
	National	CD4022	
	SGS	HBF4022	
	Solitron	CM4022	
	SSS	SCL4022	
	TI	TP4022	
	Toshiba	TC4022	
CD4023	Fairchild	F4023	
	Mitel	SIL4023	
		SIL4923	
	Motorola	MC14023	
	National	CD4023	
	NEC America	μPD4023	
	SGS	HBF4023	
	Solitron	CM4023	
	SSS	SCL4023	
	TI	TP4023	
	Toshiba	TC4023	
CD4024	Fairchild	F4024	
	Mitel	SIL4024	
	Motorola	MC14024	
	National	CD4024	
	NEC America	μPD4024	
	SGS	HBF4024	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

RCA Solid State Division (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
CD4024	Solitron	CM4024	
	SSS	SCL4024	
	TI	TP4024	
	Toshiba	TC4024	
CD4025	Fairchild	F4025	
	Mitel	SIL4025	
		SIL4925	
	Motorola	MC14025	
	National	CD4025	
	NEC America	μPD4025	
	SGS	HBF4025	
	Solitron	CM4025	
	SSS	SCL4025	
	TI	TP4025	
	Toshiba	TC4025	
CD4026	Solitron	CM4026	
	SSS	SCL4026	
CD4027	Fairchild	F4027	
	Mitel	SIL4027	
	Motorola	MC14027	
	National	CD4027	
	NEC America	μPD4027	
	SGS	HBF4027	
	Solitron	CM4027	
	SSS	SCL4027	
	TI	TP4027	
	Toshiba	TC4027	
CD4028	Fairchild	F4028	
	Mitel	SIL4028	
	Motorola	MC14028	
	National	CD4028	
	NEC America	μPD4028	
	SGS	HBF4028	
	Solitron	CM4028	
	SSS	SCL4028	
	TI	TP4028	
	Toshiba	TC4028	
CD4029	Fairchild	F4029	
	Mitel	SIL4029	
	Motorola	MC14510	
	National	CD4029	
	NEC America	μPD4029	
	SGS	HBF4029	
	Solitron	CM4029	
	SSS	SCL4029	
	TI	TP4029	
	Toshiba	TC4029	
CD4030	Fairchild	F4030	
	Mitel	SIL4030	
	Motorola	MC14070	
		MC14507	
	National	CD4030	
		CD4070	
		CD4507	
		MM74C86	
	NEC America	μPD4030	
	RCA	CD4070	
	SGS	HBF4030	
	Solitron	CM4030	
	SSS	SCL4030	
	TI	TP4030	
		TP4507	
	Toshiba	TC4030	
CD4031	Fairchild	F4031	
		F4557	
	Motorola	MC14557	
	National	CD4031	
CD4032	Motorola	MC14032	
	Solitron	CM4032	
	Toshiba	TC4032	
CD4033	SGS	HBF4033	
	Solitron	CM4033	
	SSS	SCL4033	
CD4034	Fairchild	F4034	
	Motorola	MC14034	
	National	CD4034	
	Solitron	CM4034	
	SSS	SCL4034	
	Toshiba	TC4034	
CD4035	Fairchild	F4035	
	Mitel	SIL4035	
	Motorola	MC14035	
CD4035	National	CD4035	
	NEC America	μPD4035	
	SGS	HBF4035	
	Solitron	CM4035	
	SSS	SCL4035	
	TI	TP4035	
	Toshiba	TC4035	
CD4038	Motorola	MC14038	
		MC14308	
	Solitron	CM4038	
	Toshiba	TC4038	
CD4039	Solitron	CM4039	
CD4040	Fairchild	F4040	
	Mitel	SIL4040	
	Motorola	MC14040	
	National	CD4040	
	NEC America	μPD4040	
	Solitron	CM4040	
	SSS	SCL4040	
	TI	TP4040	
	Toshiba	TC4040	
CD4041	Fairchild	F4041	
	National	CD4041	
	Solitron	CM4041	
	SSS	CL4041	
		SCL4041	
CD4042	Fairchild	F4042	
	Mitel	SIL4042	
	Motorola	MC14042	
	National	CD4042	
	NEC America	μPD4042	
	SGS	HBF4042	
	Solitron	CM4042	
	SSS	SCL4042	
	TI	TP4042	
	Toshiba	TC4042	
CD4043	Fairchild	F4043	
	Mitel	SIL4043	
	Motorola	MC14043	
	National	CD4043	
	NEC America	μPD4043	
	Solitron	CM4043	
	SSS	SCL4043	
	TI	TP4043	
	Toshiba	TC4043	
CD4044	Fairchild	F4044	
	Mitel	SIL4044	
	Motorola	MC14044	
	National	CD4044	
	NEC America	μPD4044	
	Solitron	CM4044	
	SSS	SCL4044	
	TI	TP4044	
	Toshiba	TC4044	
CD4045	SGS	HBF4045	
	Solitron	CM4045	
	SSS	SCL4445	
CD4046	Fairchild	F4046	
	Mitel	SIL4046	
	Motorola	MC14046	
	National	CD4046	
	Solitron	CM4046	
	SSS	SCL4046	
CD4047	Fairchild	F4047	
	National	CD4047	
	Solitron	CM4047	
	Toshiba	TC4047	
CD4048	National	CD4048	
	Solitron	CM4048	
CD4049	Fairchild	F4049	
	Mitel	SIL4049	
	Motorola	MC14049	
	National	CD4049	
	NEC America	μPD4049	
	SGS	HBF4049	
	Solitron	CM4049	
	SSS	SCL4049	
	TI	TP4049	
	Toshiba	TC4049	
CD4050	Fairchild	F4050	
	Mitel	SIL4050	
	Motorola	MC14050	
	National	CD4050	
	NEC America	μPD4050	
	SGS	HBF4050	
	Solitron	CM4050	
CD4050	SSS	SCL4050	
	TI	TP4050	
	Toshiba	TC4050	
CD4051	Fairchild	F4051	
	Mitel	SIL4051	
	Motorola	MC14051	
	National	CD4051	
	NEC America	μPD4051	
	Solitron	CM4051	
	SSS	SCL4051	
	TI	TP4051	
	Toshiba	TC4051	
CD4052	Fairchild	F4052	
	Mitel	SIL4052	
	Motorola	MC14052	
	National	CD4052	
	NEC America	μPD4052	
	Solitron	CM4052	
	SSS	SCL4052	
	TI	TP4052	
	Toshiba	TC4052	
CD4053	Fairchild	F4053	
	Mitel	SIL4053	
	Motorola	MC14053	
	National	CD4053	
	NEC America	μPD4053	
	Solitron	CM4053	
	SSS	SCL4053	
	TI	TP4053	
	Toshiba	TC4053	
CD4055	Mitel	SIL4055	
	Motorola	MC14558	
CD4056	Mitel	SIL4056	
	Motorola	MC14543	
	SSS	SCL4543	
CD4060	Mitel	SIL4060	
	National	CD4060	
	SSS	SCL4060	
CD4061	Toshiba	TC4061	
CD4062	Motorola	MC14562	
CD4063	Motorola	MC14066	
		MC14585	
	National	MM74C85	
	NEC America	μPD4063	
	SGS	HBF4066	
	Signetics	N4066	
	Solitron	CM4066	
	SSS	SCL4066	
		SCL4585	
	Toshiba	TC4066	
		TC4585	
CD4066	Fairchild	F4066	
	Mitel	SIL4066	
	Motorola	MC14066	
	National	CD4066	
	NEC America	μPD4066	
	SGS	HBF4066	
	Signetics	N4066	
	Solitron	CM4066	
		CM4116	
	SSS	SCL4066	
	Toshiba	TC4066	
CD4067	Fairchild	F4067	
	Motorola	MC14529	
CD4068	Fairchild	F4068	
	Mitel	SIL4068	
	Motorola	MC14068	
		MC14501	
	NEC America	μPD4068	
	Solitron	CM4068	
	SSS	SCL4068	
	TI	TP4068	
	Toshiba	TC4068	
CD4069	Fairchild	F4069	
	Harris	HD4069	
		HD54C04	
		HD74C04	
	Mitel	SIL4069	
	Motorola	MC14069	
	National	CD4069	
		MM54C04	
		MM74C04	
	NEC America	μPD4069	
	Solitron	CM4069	
	SSS	SCL4069	
	TI	TP4069	
CD4069	Toshiba	TC4069	
CD4070	Fairchild	F4070	
	Mitel	SIL4070	
	Motorola	MC14507	
	National	CD4070	
		CD4507	
		MM74C86	
	RCA	CD4030	
	Solitron	CM4030	
		CM4070	
	SSS	SCL4030	
		SCL4070	
	TI	TP4507	
CD4070A	Motorola	MC14070	
CD4071	Fairchild	F4071	
	Mitel	SIL4071	
	Motorola	MC14071	
	National	CD4071	
	NEC America	μPD4071	
	Solitron	CM4071	
	SSS	SCL4071	
	TI	TP4071	
	Toshiba	TC4071	
CD4072	Fairchild	F4072	
	Mitel	SIL4072	
	Motorola	MC14072	
	SSS	SCL4072	
	TI	TP4072	
	Toshiba	TC4072	
CD4073	Fairchild	F4073	
	Mitel	SIL4073	
	Motorola	MC14073	
	National	CD4073	
	NEC America	μPD4073	
	Solitron	CM4073	
	SSS	SCL4073	
	TI	TP4073	
	Toshiba	TC4073	
CD4075	Fairchild	F4075	
	Mitel	SIL4075	
	Motorola	MC14075	
	National	CD4075	
	NEC America	μPD4075	
	SSS	SCL4075	
	TI	TP4075	
	Toshiba	TC4075	
CD4076	Fairchild	F4076	
	Harris	HD54C173	
		HD74C173	
	Mitel	SIL4076	
	Motorola	MC14076	
	National	CD4076	
		MM54C173	
		MM74C173	
	Solitron	CM4076	
	SSS	SCL4076	
CD4077	Fairchild	F4077	
	Mitel	SIL4077	
	Motorola	MC14077	
	Solitron	CM4077	
	SSS	SCL4077	
CD4078	Fairchild	F4078	
	Mitel	SIL4078	
	Motorola	MC14078	
	NEC America	μPD4078	
	Solitron	CM4078	
	SSS	SCL4078	
	TI	TP4078	
	Toshiba	TC4078	
CD4081	Fairchild	F4081	
	Mitel	SIL4081	
	Motorola	MC14081	
	National	CD4081	
	NEC America	μPD4081	
	Solitron	CM4081	
	SSS	SCL4081	
	TI	TP4081	
	Toshiba	TC4081	
CD4082	Fairchild	F4082	
	Mitel	SIL4082	
	Motorola	MC14082	
	NEC America	μPD4082	
	SSS	SCL4082	
	TI	TP4082	
	Toshiba	TC4082	
CD4085	Fairchild	F4085	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

RCA Solid State Division (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
CD4085	Motorola	MC14506	
CD4086	Fairchild	F4086	
CD4089	National	CD4089	
CD4093	Fairchild	F4093	
	Motorola	MC14093	
	National	CD4093	
	NEC America	μPD4093	
	SSS	SCL4093	
CD4094	NEC America	μPD4094	
	SSS	SCL4094	
CD4098	Mitel	SIL4098	
	Motorola	MC14528	
CD4099	Fairchild	F4099	
	National	CD4099	
	NEC America	μPD4099	
CD4194	NEC America	μPD4194	
CD4502	Mitel	SIL4502	
	Motorola	MC14502	
	SSS	SCL4502	
CD4508	Mitel	SIL4508	
	Motorola	MC14508	
	NEC America	μPD4508	
	Solitron	CM4508	
	SSS	SCL4508	
	Toshiba	TC4508	
CD4510	Fairchild	F4510	
	Mitel	SIL4510	
	Motorola	MC14510	
	National	CD4510	
	NEC America	μPD4510	
	RCA	CD40192	
	SSS	SCL4510	
	Toshiba	TC4510	
CD4511	Fairchild	F4511	
	Mitel	SIL4511	
	Motorola	MC14511	
	National	CD4511	
	NEC America	μPD4511	
	Solitron	CM4511	
	SSS	SCL4511	
	TI	TP4511	
CD4514	Fairchild	F4514	
	Mitel	SIL4514	
	Motorola	MC14514	
	National	CD4514	
	NEC America	μPD4514	
	Solitron	CM4514	
	SSS	SCL4514	
	Toshiba	TC4514	
CD4515	Fairchild	F4515	
	Mitel	SIL4515	
	Motorola	MC14515	
	National	CD4515	
	NEC America	μPD4515	
	Solitron	CM4515	
	SSS	SCL4515	
	Toshiba	TC4515	
CD4516	Fairchild	F4516	
	Mitel	SIL4516	
	Motorola	MC14516	
	National	CD4516	
	NEC America	μPD4516	
	RCA	CD40193	
	SSS	SCL4516	
	Toshiba	TC4516	
CD4518	Fairchild	F4518	
	Mitel	SIL4518	
	Motorola	MC14518	
	National	CD4518	
	NEC America	μPD4518	
	Solitron	CM4518	
	SSS	SCL4518	
	TI	TP4518	
	Toshiba	TC4518	
CD4520	Fairchild	F4520	
	Mitel	SIL4520	
	Motorola	MC14520	
	National	CD4520	
	NEC America	μPD4520	
	Solitron	CM4520	
	SSS	SCL4520	
	TI	TP4520	
CD4520	Toshiba	TC4520	
CD4527	Motorola	MC14527	
	National	CD4527	
	SSS	SCL4527	
CD4528	Fairchild	F4528	
	Motorola	MC14528	
	National	CD4528	
	NEC America	μPD4528	
	SSS	SCL4528	
	Toshiba	TC4528	
CD4532	Fairchild	F4532	
	Motorola	MC14532	
	NEC America	μPD4532	
	Toshiba	TC4532	
CD4555	Fairchild	F4555	
	Motorola	MC14555	
	NEC America	μPD4555	
	SSS	SCL4555	
CD4556	Fairchild	F4556	
	Motorola	MC14556	
	NEC America	μPD4556	
	SSS	SCL4556	
MWS5040	**Harris**	**HM6501**	**1174**
♦MW4104	Mostek	MK4027	

RIFA

PBD352301	Sprague	ULN-2001	
PBD352302	Sprague	ULN-2002	
PBD352303	Sprague	ULN-2003	

Rockwell, Microelectronic Division

R6502	MOS	MCS6502	
	Synertek	SY6502	
R6503	MOS	MCS6503	
	Synertek	SY6503	
R6504	MOS	MCS6504	
	Synertek	SY6504	
R6505	MOS	MCS6505	
	Synertek	SY6505	
R6512	MOS	MCS6512	
	Synertek	SY6512	
R6514	MOS	MCS6514	
	Synertek	SY6514	
R6515	MOS	SY6515	
	Synertek	SY6515	
R6520	MOS	MCS6520	
	Synertek	SY6520	
R6530	MOS	MCS6530	
	Synertek	SY6530	
R6532	MOS	MCS6532	
	Synertek	SY6532	
1103	AMI	S1103A	
1103A	AMI	S1103A	
	Intel	1103A	
	Synertek	1103A	
1604	EA	EA4096	
	Mostek	MK4096	

Sanyo

LA1230	Hitachi	HA1137	
LA1240	Hitachi	HA1197	
LA1352	Motorola	MC1352	
	RCA	CA1352	
LA1353	Motorola	MC1353	
LA1365	Fairchild	μA3065	
	RCA	CA3065	

SGS-ATES Semiconductor

HBF4001	Fairchild	F4001	
	Mitel	SIL4001	
	Motorola	MC14001	
	National	CD4001	
	NEC America	μPD4001	
	RCA	CD4001	
	Solitron	CM4001	
	SSS	SCL4001	
	TI	TP4001	
HBF4001	Toshiba	TC4001	
HBF4002	Fairchild	F4002	
	Mitel	SIL4002	
	Motorola	MC14002	
	National	CD4002	
	NEC America	μPD4002	
	RCA	CD4002	
	Solitron	CM4002	
	SSS	SCL4002	
	TI	TP4002	
	Toshiba	TC4002	
HBF4007	Fairchild	F4007	
	Mitel	SIL4007	
	Motorola	MC14007	
	National	CD4007	
	RCA	CD4007	
	Solitron	CM4007	
	SSS	SCL4007	
	TI	TP4007	
	Toshiba	TC4007	
HBF4008	Fairchild	F4008	
	Motorola	MC14008	
	National	CD4008	
	RCA	CD4008	
	Solitron	CM4008	
	SSS	SCL4008	
	TI	TP4008	
	Toshiba	TC4008	
HBF4009	Mitel	SIL4009	
	National	CD4009	
	RCA	CD4009	
	Solitron	CM4009	
	SSS	SCL4009	
	TI	TP4009	
	Toshiba	TC4009	
HBF4010	Mitel	SIL4010	
	National	CD4010	
	RCA	CD4010	
	Solitron	CM4010	
	SSS	SCL4010	
	TI	TP4010	
	Toshiba	TC4010	
HBF4011	Fairchild	F4011	
	Mitel	SIL4011	
	Motorola	MC14011	
	National	CD4011	
	NEC America	μPD4011	
	RCA	CD4011	
	Solitron	CM4011	
	SSS	SCL4011	
	TI	TP4011	
	Toshiba	TC4011	
HBF4012	Fairchild	F4012	
	Mitel	SIL4012	
	Motorola	MC14012	
	National	CD4012	
	NEC America	μPD4012	
	RCA	CD4012	
	Solitron	CM4012	
	SSS	SCL4012	
	TI	TP4012	
	Toshiba	TC4012	
HBF4013	Fairchild	F4013	
	Mitel	SIL4013	
	Motorola	MC14013	
	National	CD4013	
	NEC America	μPD4013	
	RCA	CD4013	
	Solitron	CM4013	
	SSS	SCL4013	
	TI	TP4013	
	Toshiba	TC4013	
HBF4014	Fairchild	F4014	
	Mitel	SIL4014	
	Motorola	MC14014	
	National	CD4014	
	NEC America	μPD4014	
	RCA	CD4014	
	Solitron	CM4014	
	SSS	SCL4014	
	TI	TP4014	
	Toshiba	TC4014	
HBF4015	Fairchild	F4015	
	Mitel	SIL4015	
	Motorola	MC14015	
	National	CD4015	
HBF4015	NEC America	μPD4015	
	RCA	CD4015	
	Solitron	CM4015	
	SSS	SCL4015	
	TI	TP4015	
	Toshiba	TC4015	
HBF4016	RCA	CD4016	
		CD4066	
	SSS	SCL4016	
HBF4017	Fairchild	F4017	
	Mitel	SIL4017	
	Motorola	MC14017	
	National	CD4017	
	NEC America	μPD4017	
	RCA	CD4017	
	Solitron	CM4017	
	SSS	SCL4017	
	TI	TP4017	
	Toshiba	TC4017	
HBF4018	Fairchild	F4018	
	Mitel	SIL4018	
	National	CD4018	
	RCA	CD4018	
	Solitron	CM4018	
	SSS	SCL4018	
	TI	TP4018	
	Toshiba	TC4018	
HBF4019	Fairchild	F4019	
	Mitel	SIL4019	
	National	CD4019	
	RCA	CD4019	
	Solitron	CM4019	
	SSS	SCL4019	
	TI	TP4019	
	Toshiba	TC4019	
HBF4020	Fairchild	F4020	
	Mitel	SIL4020	
	Motorola	MC14020	
	National	CD4020	
	NEC America	μPD4020	
	RCA	CD4020	
	Solitron	CM4020	
	SSS	SCL4020	
	TI	TP4020	
	Toshiba	TC4020	
HBF4021	RCA	CD4021	
	SSS	SCL4021	
HBF4022	Fairchild	F4022	
	Mitel	SIL4022	
	Motorola	MC14022	
	National	CD4022	
	RCA	CD4022	
	Solitron	CM4022	
	SSS	SCL4022	
	TI	TP4022	
	Toshiba	TC4022	
HBF4023	Fairchild	F4023	
	Mitel	SIL4023	
	Motorola	MC14023	
	National	CD4023	
	NEC America	μPD4023	
	RCA	CD4023	
	Solitron	CM4023	
	SSS	SCL4023	
	TI	TP4023	
	Toshiba	TC4023	
HBF4024	Fairchild	F4024	
	Mitel	SIL4024	
	Motorola	MC14024	
	National	CD4024	
	RCA	CD4024	
	Solitron	CM4024	
	SSS	SCL4024	
	TI	TP4024	
	Toshiba	TC4024	
HBF4025	Fairchild	F4025	
	Mitel	SIL4025	
	Motorola	MC14025	
	National	CD4025	
	NEC America	μPD4025	
	RCA	CD4025	
	Solitron	CM4025	
	SSS	SCL4025	
	TI	TP4025	
	Toshiba	TC4025	
HBF4027	Fairchild	F4027	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

SGS-ATES Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
HBF4027	Mitel	SIL4027	
	Motorola	MC14027	
	National	CD4027	
	NEC America	μPD4027	
	RCA	CD4027	
	Solitron	CM4027	
	SSS	SCL4027	
	TI	TP4027	
	Toshiba	TC4027	
HBF4028	Fairchild	F4028	
	Mitel	SIL4028	
	Motorola	MC14028	
	National	CD4028	
	NEC America	μPD4028	
	RCA	CD4028	
	Solitron	CM4028	
	SSS	SCL4028	
	TI	TP4028	
	Toshiba	TC4028	
HBF4029	Fairchild	F4029	
	Mitel	SIL4029	
	National	CD4029	
	NEC America	μPD4029	
	RCA	CD4029	
	Solitron	CM4029	
	SSS	SCL4029	
	TI	TP4029	
	Toshiba	TC4029	
HBF4030	Fairchild	F4030	
	Mitel	SIL4030	
	National	CD4030	
	NEC America	μPD4030	
	RCA	CD4030	
	Solitron	CM4030	
	SSS	SCL4030	
	TI	TP4030	
	Toshiba	TC4030	
HBF4033	RCA	CD4033	
	Solitron	CM4033	
	SSS	SCL4033	
HBF4035	Fairchild	F4035	
	Mitel	SIL4035	
	Motorola	MC14035	
	National	CD4035	
	NEC America	μPD4035	
	RCA	CD4035	
	Solitron	CM4035	
	SSS	SCL4035	
	TI	TP4035	
	Toshiba	TC4035	
HBF4040	RCA	CD4040	
	SSS	SCL4040	
HBF4042	Fairchild	F4042	
	Mitel	SIL4042	
	Motorola	MC14042	
	National	CD4042	
	NEC America	μPD4042	
	RCA	CD4042	
	Solitron	CM4042	
	SSS	SCL4042	
	TI	TP4042	
	Toshiba	TC4042	
HBF4045	RCA	CD4045	
	Solitron	CM4045	
	SSS	SCL4445	
HBF4049	Fairchild	F4049	
	Mitel	SIL4049	
	Motorola	MC14049	
	National	CD4049	
	NEC America	μPD4049	
	RCA	CD4049	
	Solitron	CM4049	
	SSS	SCL4049	
	TI	TP4049	
	Toshiba	TC4049	
HBF4050	Fairchild	F4050	
	Mitel	SIL4050	
	Motorola	MC14050	
	National	CD4050	
	NEC America	μPD4050	
	RCA	CD4050	
	Solitron	CM4050	
HBF4050	SSS	SCL4050	
	TI	TP4050	
	Toshiba	TC4050	
HBF4066	Fairchild	F4066	
	Mitel	SIL4066	
	Motorola	MC14066	
	National	CD4066	
	NEC America	μPD4066	
	RCA	CD4063	
		CD4066	
	Signetics	N4066	
	Solitron	CM4066	
	SSS	SCL4066	
	Toshiba	TC4066	
L201	Exar	XR2201	
	Fairchild	9665	
	Motorola	MC1411	
	Silicon G	SG2001	
	Sprague	ULN-2001	
	TI	ULN2001	
L202	Exar	XR2202	
	Fairchild	9666	
	Motorola	MC1412	
	Silicon G	SG2002	
	Sprague	ULN-2002	
	TI	ULN2002	
L203	Exar	XR2203	
	Fairchild	9667	
	Motorola	MC1413	
	Silicon G	SG2003	
	Sprague	ULN-2003	
	TI	ULN2003	
M1024	ITT	SAA1024	
M1025	ITT	SAA1025	
TAA661	NPC	TAA661	
TAA930	NPC	TAA930	
TBA510	Fairchild	TBA510	
TBA520	Fairchild	TBA520	
TBA530	Fairchild	TBA530	
TBA540	Fairchild	TBA540	
TBA560	Fairchild	TBA560	
TBA641	Fairchild	μA706	
		TBA641	
TBA800	Fairchild	TBA800	
	NPC	TBA800	
	Plessey	TBA800	
TBA810	Fairchild	TBA810	
	Motorola	MC1384	
	RCA	CA810	
	SGS	TBA810	
	Signetics	TBA810	
TBA920	Fairchild	TBA920	
	NPC	TBA920	
TBA970	Fairchild	TBA970	
TBA990	Fairchild	TBA990	
TCA900	NPC	TCA900	
TDA1190	Sprague	ULN-2290	

Siemens

Manufacturer Device	Replacement Source	Device	IC Master Page
TBA120	Plessey	TBA120	
TBA440	Plessey	TBA440	

Signetics

Manufacturer Device	Replacement Source	Device	IC Master Page
μA709	Fairchild	μA709	
	Motorola	MC1709	
	National	LM709	
	Raytheon	RC709	
		RM709	
	TI	μA709	
μA710	Fairchild	μA710	
	Motorola	MC1710	
	National	LM710	
	Raytheon	RC710	
		RM710	
	Silicon G	SG710	
	TI	μA710	
μA711	Fairchild	μA711	
	Motorola	MC1711	
	National	LM711	
	Raytheon	RC711	
		RM711	
	Silicon G	SG711	
μA711	TI	μA711	
μA723	AMD	723	
	Fairchild	μA723	
	Intersil	723	
	Motorola	MC1723	
	National	LM723	
	Raytheon	RC723	
		RM723	
	RCA	CA723	
	Silicon G	SG723	
	TI	μA723	
μA733	AMD	733	
	Motorola	MC1733	
	National	LM733	
	Raytheon	RC733	
		RM733	
	Silicon G	SG733	
	TI	μA733	
μA740	Fairchild	μA740	
	Intersil	740	
	National	LH740	
μA741	AD	AD741	
	AMD	741	
	Fairchild	μA741	
	Intersil	741	
	Motorola	MC1741	
	National	LM741	
	PMI	**SSS741**	**839**
	Raytheon	RC741	
		RM741	
	RCA	CA741	
	Silicon G	SG741	
	TI	μA741	
μA747	AMD	747	
	Fairchild	μA747	
	Motorola	MC1747	
	National	LM747	
	PMI	**SSS747**	**844**
	Raytheon	RC747	
		RM747	
	RCA	CA747	
	Silicon G	SG747	
	TI	μA747	
μA748	AMD	748	
	Fairchild	μA748	
	Intersil	748	
	Motorola	MC1748	
	National	LM748	
	Raytheon	RC748	
		RM748	
	RCA	CA748	
	Silicon G	SG748	
	TI	μA748	
μA78G	Fairchild	μA78G	
μA78L02	TI	μA78L02	
μA78L05	Fairchild	μA78L05	
	TI	μA78L05	
μA78L06	TI	μA78L06	
μA78L12	Fairchild	μA78L12	
	TI	μA78L12	
μA78L15	Fairchild	μA78L15	
	TI	μA78L15	
μA78L62	Fairchild	μA78L06	
μA78MG	Fairchild	μA78MG	
μA78M05	Fairchild	μA78M05	
	TI	μA78M05	
μA78M06	Fairchild	μA78M06	
	TI	μA78M06	
μA78M08	Fairchild	μA78M08	
	TI	μA78M08	
μA78M12	Fairchild	μA78M12	
	TI	μA78M12	
μA78M15	Fairchild	μA78M15	
	TI	μA78M15	
μA78M20	Fairchild	μA78M20	
	TI	μA78M20	
μA78M24	Fairchild	μA78M24	
	TI	μA78M24	
μA7805	Fairchild	μA7805	
μA7806	Fairchild	μA7806	
μA7808	Fairchild	μA7808	
μA7812	Fairchild	μA7812	
μA7815	Fairchild	μA7815	
μA7818	Fairchild	μA7818	
μA7824	Fairchild	μA7824	
μA79G	Fairchild	μA79G	
μA79L05	Motorola	MC79L05	
μA79L12	Motorola	MC79L12	
μA79L15	Motorola	MC79L15	
μA79MG	Fairchild	μA79MG	
DS3611	National	DS3611	
DS3612	National	DS3612	
DS3613	National	DS3613	
DS3614	National	DS3614	
DS7820	AMD	DM7820	
	TI	SN55182	
DS7830	AMD	DM7830	
	TI	SN55183	
DS8800	TI	SN5480	
DS8820	AMD	DM8820	
	TI	SN75182	
DS8830	AMD	DM8830	
	TI	SN75183	
DS8880	National	DS8880	
ISP-8A/600	**National**	**ISP-8A/600**	**1692**
LF155	**National**	**LF155**	**786**
LF156	**National**	**LF156**	**786**
LF157	**National**	**LF157**	**786**
LF255	**National**	**LF255**	**786**
LF256	**National**	**LF256**	**786**
LF257	**National**	**LF257**	**786**
LF355	**National**	**LF355**	**786**
LF356	**National**	**LF356**	**786**
LF357	**National**	**LF357**	**786**
LM101	AMD	LM101	
	Fairchild	μA101	
	Intersil	LM101	
	Motorola	LM101	
	RCA	CA101	
	Silicon G	SG101	
	TI	LM101	
LM107	AMD	LM107	
	Fairchild	μA107	
	Intersil	LM107	
	Motorola	LM107	
	Raytheon	LM107	
	RCA	CA107	
	Silicon G	SG107	
	TI	LM107	
LM108	AMD	LM108	
	Fairchild	μA108	
	Motorola	LM108	
	Raytheon	LM108	
	RCA	CA108	
	Silicon G	SG108	
LM109	Fairchild	μA109	
	Motorola	LM109	
	Silicon G	SG109	
	TI	LM109	
LM111	AMD	LM111	
	Motorola	LM111	
	Silicon G	SG111	
	TI	LM111	
LM119	AMD	LM119	
LM124	AMD	LM124	
	Motorola	LM124	
	Silicon G	SG124	
	TI	LM124	
LM139	AMD	LM139	
	Motorola	LM139	
	RCA	CA139	
	Silicon G	SG139	
	TI	LM139	
LM193	National	LM193	
LM201	AMD	LM201	
	Fairchild	μA201	
	Intersil	LM201	
	Motorola	LM201	
	RCA	CA201	
	Silicon G	SG201	
	Teledyne S	LM201	
	TI	LM201	
LM207	AMD	LM207	
	Fairchild	μA207	
	Intersil	LM207	
	Motorola	LM207	
	Raytheon	LM207	
	RCA	CA207	
	Silicon G	SG207	
	TI	LM207	
LM208	AMD	LM208	
	Motorola	LM208	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
LM208	RCA	CA208	
	Silicon G	SG208	
LM209	Fairchild	μA209	
	Motorola	LM209	
	Raytheon	LM209	
	Silicon G	SG209	
	TI	LM209	
LM211	AMD	LM211	
	Motorola	LM211	
	Silicon G	SG211	
	TI	LM211	
LM219	AMD	LM219	
LM224	AMD	LM224	
	Motorola	LM224	
	RCA	CA224	
	Silicon G	SG224	
	TI	LM224	
LM239	AMD	LM239	
	Motorola	LM239	
	RCA	CA239	
	Silicon G	SG239	
	TI	LM239	
LM293	National	LM293	
LM301	AMD	LM301	
	Fairchild	μA301	
	Intersil	LM301	
	Motorola	LM301	
	National	LM301	
	Raytheon	LM301	
	RCA	CA301	
	Silicon G	SG301	
	TI	LM301	
LM307	AMD	LM307	
	Fairchild	μA307	
	Intersil	LM307	
	Motorola	LM307	
	National	LM307	
	Raytheon	LM307	
	RCA	CA307	
	Silicon G	SG307	
	TI	LM307	
LM308	AMD	LM308	
	Fairchild	μA308	
	Motorola	LM308	
	National	LM308	
	Raytheon	LM308	
	RCA	CA308	
	Silicon G	SG308	
LM309	Fairchild	μA309	
	Motorola	LM309	
	Raytheon	LM309	
	Silicon G	SG309	
	TI	LM309	
LM311	AMD	LM311	
	Motorola	LM311	
	Raytheon	LM311	
	RCA	CA311	
	Silicon G	SG311	
LM319	AMD	LM319	
LM324	AMD	LM324	
	Motorola	LM324	
	RCA	CA324	
	Silicon G	SG324	
	TI	LM324	
LM329	TI	LM329	
LM339	AMD	LM339	
	Motorola	LM339	
	Silicon G	SG339	
	TI	LM339	
LM393	National	LM393	
MC1399	Motorola	MC1399	
MC1408	Datel	DAC-IC8BC	
	Motorola	MC1408	
MC1456	Motorola	MC1456	
	Raytheon	RC1556	
	Silicon G	SG1456	
MC1458	Exar	XR1458	
	Fairchild	MC1458	
	Motorola	MC1458	
	National	LM1458	
	Raytheon	RC1458	
	RCA	CA1458	
	Silicon G	SG1458	
MC1458	TI	MC1458	
MC1488	AMD	MC1488	
	Exar	XR1488	
	TI	SN75188	
MC1489	AMD	MC1489	
	TI	SN75189	
MC1489A	Exar	XR1489A	
MC1496	Motorola	MC1496	
	National	LM1496	
	Silicon G	SG1496	
MC1508	Datel	DAC-IC8BM	
MC1556	Motorola	MC1556	
	Raytheon	RM1556	
	Silicon G	SG1556	
MC1558	Exar	XR1558	
	Motorola	MC1558	
	Raytheon	RM1558	
	RCA	CA1558	
	Silicon G	SG1558	
	TI	MC1558	
MC1596	Motorola	MC1596	
	Silicon G	SG1596	
MC3302	Motorola	MC3302	
MP8080A	AMD	9080A	
	Intel	8080A	
	National	**INS8080A**	**1656,1670**
	NEC Micro	**μPD8080AF**	**1736**
	TI	TMS8080A	
NE5009	**PMI**	**DAC-08**	**919**
NE529	National	LM361	
NE531	Raytheon	RC4531	
NE532	TI	LM358	
NE535	Motorola	MC1741S	
NE536	Fairchild	μA740	
	Intersil	NE536	
NE555	AMD	NE555	
	Exar	XR555	
	Fairchild	μA555	
	Intersil	NE555	
	Motorola	MC1455	
	Raytheon	RC555	
	RCA	CA555	
	Silicon G	SG555	
	TI	NE555	
NE556	AMD	NE556	
	Exar	XR556	
	Fairchild	μA556	
	Motorola	MC3456	
	Raytheon	RC556	
	Silicon G	SG556	
	TI	NE556	
NE565	Motorola	LM565	
NE567	Exar	XR567	
NE592	AMD	AM592	
	Motorola	MC1733	
		NE592	
♦N1004	Motorola	MC1004	
♦N1006	Motorola	MC1006	
♦N1010	Motorola	MC1010	
♦N1011	Motorola	MC1011	
♦N1012	Motorola	MC1012	
♦N1013	Motorola	MC1013	
♦N1014	Motorola	MC1014	
♦N1015	Motorola	MC1015	
♦N1016	Motorola	MC1016	
♦N1017	Motorola	MC1017	
♦N1024	Motorola	MC1024	
♦N1025	Motorola	MC1025	
♦N1027	Motorola	MC1027	
♦N1033	Motorola	MC1033	
♦N1039	Motorola	MC1039	
♦N2010	Motorola	MC1160/236	
N2901	AMD	AM2901A	
	Fairchild	F2901A	
		9409	
	Motorola	MC2901	
	National	**IDM2901A**	**1656,1680**
	NEC Micro	**μPB2901**	**1850**
	Raytheon	AM2901A	
N3002	Intel	3002	
N3101A	NEC Micro	μPB2089	
N4066	Fairchild	F4066	
	Mitel	SIL4066	
	Motorola	MC14066	
N4066	National	CD4066	
	NEC America	μPD4066	
	RCA	CD4063	
		CD4066	
	SGS	HBF4066	
	Solitron	CM4066	
	SSS	SCL4066	
	Toshiba	TC4066	
♦N5065	Motorola	MC1358	
	RCA	CA3065	
	Sprague	ULN-2165	
♦N5070	RCA	CA3070	
	Sprague	ULN-2124	
♦N5071	Fairchild	μA781	
	Sprague	ULN-2127	
♦N5072	Fairchild	μA746	
	Sprague	ULN-2114	
N5111	Sprague	ULN-2113	
♦N521	Motorola	MC7521	
♦N5556	Motorola	MC1456	
N5558	Exar	XR1458	
N5558F	Motorola	MC1458	
N5570	Fairchild	μA780	
♦N5595	Motorola	MC1495	
N5596	Motorola	MC1496	
♦N5709	Signetics	μA709	
♦N5710	Signetics	μA710	
♦N5711	Signetics	μA711	
♦N5723	Signetics	μA723	
♦N5733	Signetics	μA733	
♦N5741	Signetics	μA741	
♦N5747	Signetics	μA747	
♦N5748	Signetics	μA748	
N8H16	National	DM54H20	
N8H70	ITT	ITT74H11	
	National	DM74H10	
	TI	SN74H11	
N8H80	ITT	ITT74H00	
	National	DM74H00	
	TI	SN74H00	
N8H90	ITT	ITT74H04	
	National	DM74H04	
	TI	SN74H04	
N8T09	Raytheon	RC8T09	
N8T10	National	DM8551	
	Raytheon	RC8T10	
	TI	SN74173	
N8T13	Fairchild	8T13	
	Motorola	MC8T13	
	National	DS7521	
	TI	N8T13	
		SN75121	
N8T14	Fairchild	8T14	
	Motorola	MC8T14	
	National	DS75122	
	TI	N8T14	
		SN75122	
N8T22	ITT	ITT74122	
	National	DM8601	
	TI	SN74122	
N8T23	Fairchild	8T23	
	Motorola	MC8T23	
	National	DS75123	
	TI	N8T23	
		SN75123	
N8T24	Fairchild	8T24	
	Motorola	MC8T24	
	National	DS75124	
	TI	N8T24	
		SN75124	
N8T25	Motorola	MC6880	
	National	**DS3625**	**514**
N8T26	Motorola	MC8T26	
	National	DS8826	
N8T28	Motorola	MC8T28	
N8T34	National	DS8834	
N8T37	Motorola	MC3437	
	National	DS8837	
N8T38	Motorola	MC3438	
	National	DS8838	
N8T380	National	DS8836	
N8T51	National	DS8856	
N8T54	National	DM7448	
N8T59	National	DS8857	
N8T74	Fairchild	9374	
	National	DS8672	
N8T95	Motorola	MC8T95	
	National	DM8095	
N8T96	Motorola	MC8T96	
	National	DM8096	
N8T97	Motorola	MC8T97	
	National	DM8097	
N8T98	Motorola	MC8T98	
	National	DM8098	
		DN7098	
		DS8674	
N82S02	Raytheon	RC5330	
N82S06	MMI	6531	
	Raytheon	RC5340	
	TI	SN74S200A	
		SN74S201	
N82S07	Fairchild	93411	
	MMI	6530	
	TI	SN74S300	
		SN74S301	
N82S08	**Fairchild**	**93415**	**1137**
		93421	
	TI	SN74S314	
N82S10	**Fairchild**	**93415**	**1137**
	TI	SN74S314	
N82S11	**Fairchild**	**93425**	**1137**
	TI	SN74S214	
N82S110	TI	SN74S314	
N82S111	TI	SN74S214	
N82S115	**NEC Micro**	**μPB425**	**1466**
N82S116	MMI	6531	
	National	**DM74S206**	**1297**
	TI	SN74S200A	
		SN74S201	
N82S117	**National**	**DM74S206**	**1297**
	TI	SN74S300	
		SN74S301	
N82S123	**Harris**	**HM7603**	**1192**
	Intersil	IM5610	
	MMI	**6331**	**1252**
	National	DM8578	
	TI	SN74S288	
N82S126	Harris	HPROM1024A	
	Intel	3601	
	MMI	**5300**	**1248**
		6300	**1252**
	National	**DM74S387**	**1264**
	NEC Micro	**μPB403**	**1462**
	TI	SN54S387	
		SN74S387	
N82S129	Harris	HPROM1024	
	Intel	3621-1	
	Intersil	IM5623	
	MMI	**5301**	**1248**
		6301	**1252**
	National	**DM74S287**	**1264**
	TI	SN54S287	
		SN74S287	
N82S130	**Fairchild**	**93436**	**1151**
	Harris	**HM7620**	**1192**
		HM7620A	**1202**
	MMI	**6305**	**1252**
	TI	SN74170	
N82S131	**Fairchild**	**93446**	**1151**
	Harris	**HM7621**	**1192**
		HM7621A	**1202**
	MMI	**6306**	**1252**
	National	**DM74S571**	**1266**
N82S136	**Harris**	**HM7642**	**1192**
	Intel	3605	
	MMI	**6352**	**1252**
	National	**DM74S572**	**1268**
	NEC Micro	**μPB406**	**1470**
N82S137	**Harris**	**HM7643**	**1192**
	Intel	3625	
	MMI	**6353**	**1252**
	NEC Micro	**μPB426**	**1470**
N82S140	Intel	3604	
	National	**DM87S295**	**1270**
	NEC Micro	μPB405	
N82S141	Intel	3624	
	National	**DM87S296**	**1270**
	NEC Micro	**μPB425**	**1466**
N82S16	Fairchild	93421	
	MMI	6531	
	National	DM74S200	
	NEC Micro	μPB2206	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
N82S16	Raytheon	RC5340	
	TI	SN54S201	
		SN74S200A	
		SN74S201	
N82S17	Fairchild	93411	
	MMI	6530	
	National	**DM74S206**	**1297**
	NEC Micro	μPB2200	
	Raytheon	RC5330	
	TI	SN54S301	
		SN74S300	
		SN74S301	
N82S180	**Harris**	**HM7680**	**1220**
	Intel	3608	
	National	DM85S229	
N82S181	**Harris**	**HM7681**	**1220**
	Intel	3628	
	National	DM85S228	
N82S184	**Harris**	**HM7684**	**1242**
N82S195	Harris	HM7647	
N82S226	Fairchild	93416	
	Intersil	IM5603	
	MMI	**6300**	**1252**
	TI	SN54187	
		SN74187	
N82S229	TI	SN74S287	
N82S23	AMD	AM27S09	
	Harris	**HM7602**	**1192**
	MMI	**6330**	**1252**
	TI	SN54S188	
		SN74S188	
N82S230	TI	SN54S270	
		SN74S270	
N82S231	TI	SN54S370	
		SN74S370	
N82S24	Intersil	IM5600	
	TI	SN54S301	
N82S25	National	DM74S289	
	TI	SN74S289	
N82S26	Fairchild	93416	
	Intersil	IM5603	
	MMI	**6300**	**1252**
	NEC Micro	**μPB403**	**1462**
	TI	SN74S387	
N82S2708	**Harris**	**HM7608**	**1235**
N82S29	Fairchild	93426	
	Intersil	IM5623	
	MMI	**6301**	**1252**
	TI	SN54S287	
		SN74S287	
N82S30	National	DM8312	
N82S41	National	DM74LS386	
N82S52	National	DM8301	
N82S80	National	DM74LS196	
N82S81	National	DM74LS197	
N82S90	National	DM74LS196	
	TI	SN74S196	
N82S91	National	DM74LS197	
	TI	SN74S197	
N8200	Raytheon	RC8200	
N8201	Raytheon	RC8201	
N8202	Raytheon	RC8202	
N8203	Raytheon	RC8203	
N8206	TI	SN74S200A	
		SN74S201	
N8207	TI	SN74S300	
		SN74S301	
N82147	National	DM74147	
	TI	SN74147	
N82148	National	DM74148	
	TI	SN74148	
N8223	Harris	HPROM8256	
	Intersil	IM5600	
	MMI	**6330**	**1252**
	National	DM8577	
	TI	SN74S188	
N8224	Intersil	IM5600	
	National	DM7488	
	TI	SN7488	
N8225	AMD	3101	
	Motorola	MCM4064	
	Raytheon	RC8225	
	TI	SN74S289	
N8230	Hitachi	HD2549	
	ITT	ITT9312	
	Motorola	MC7230	
	National	DM8312	
	Raytheon	RC8230	
	TI	SN29312	
N8231	Motorola	MC7230	
	Raytheon	RC8231	
N8232	Motorola	MC7230	
	Raytheon	RC8232	
N8233	Motorola	MC8233	
	Raytheon	RC8233	
N8234	Motorola	MC8234	
	Raytheon	RC8234	
N8241	Hitachi	HD2526	
	Motorola	MC7241	
		MC7242	
	National	DM74LS386	
	Raytheon	RC8241	
N8242	Motorola	MC7242	
	Raytheon	RC8242	
	TI	SN74LS266	
N8250	Motorola	MC7250	
		MC7251	
	Raytheon	RC8250	
N8251	Hitachi	HD2536	
	Motorola	MC7250	
		MC7251	
	Raytheon	RC8251	
N8252	Motorola	MC7250	
		MC7251	
	National	DM8301	
	Raytheon	RC8252	
	TI	SN29301	
N8255	AMD	3101	
	MMI	6560	
	Motorola	MCM4064	
	Raytheon	RC8225	
	TI	SN74S289	
N8260	Motorola	MC7260	
	Raytheon	RC8260	
N8261	Hitachi	HD2562	
	Motorola	MC7261	
	Raytheon	RC8261	
N8262	Raytheon	RC8262	
N8263	Raytheon	RC8263	
N8264	Raytheon	RC8264	
N8266	Motorola	MC7266	
	Raytheon	RC8266	
N8267	Motorola	MC7267	
	Raytheon	RC8267	
N8268	ITT	ITT7480	
	Motorola	MC7268	
	TI	SN7480	
N8269	National	DM8200	
N8270	Motorola	MC7270	
	Raytheon	RC8270	
	TI	SN74178	
N8271	Motorola	MC7271	
	Raytheon	RC8271	
	TI	SN74179	
N8277	Motorola	MC7277	
	Raytheon	RC8277	
N8280	Motorola	MC7280	
	National	DM8280	
	Raytheon	RC8280	
	TI	SN74176	
N8281	Motorola	MC7281	
	National	DM8281	
	Raytheon	RC8281	
	TI	SN54177	
N8284	Motorola	MC7284	
	Raytheon	RC8284	
N8285	Motorola	MC7285	
	Raytheon	RC8285	
N8288	Motorola	MC7288	
	National	DM8288	
N8290	National	DM8290	
	Raytheon	RC8290	
	TI	SN74196	
N8291	National	DM8291	
	Raytheon	RC8291	
	TI	SN74197	
N8292	National	DM74LS196	
	TI	SN74LS196	
N8293	National	DM74LS197	
N8293	TI	SN74LS197	
N8415	National	DM1800	
N8455	Motorola	MC7440	
	National	DM7440	
	TI	SN7440	
N8470	ITT	ITT7410	
	Motorola	MC7410	
	National	DM7410	
	TI	SN7410	
N8471	ITT	ITT7412	
	Motorola	MC7412	
	National	DM74LS12	
	TI	SN7412	
N8480	ITT	ITT7400	
	National	DM7400	
	TI	SN7400	
N8481	ITT	ITT7403	
	Motorola	MC7403	
	National	DM7403	
	TI	SN7403	
N8490	ITT	ITT7404	
	Motorola	MC7404	
	National	DM7404	
	TI	SN7404	
N8555	ITT	ITT7440	
N8806	Motorola	MC7460	
	National	DM7406	
	TI	SN7460	
N8808	ITT	ITT7430	
	Motorola	MC7430	
	National	DM7430	
	TI	SN7430	
N8813	National	DM7425	
N8815	National	DM7425	
	TI	SN7425	
N8824	Motorola	MC7474	
	TI	SN7474	
N8825	Motorola	MC7470	
	TI	SN7470	
N8828	ITT	ITT7474	
	Motorola	MC7479	
	National	DM7474	
	TI	SN7474	
N8829	Motorola	MC7472	
	TI	SN74110	
N8840	ITT	ITT7450	
	Motorola	MC7450	
	National	DM7451	
	TI	SN7450	
N8848	ITT	ITT74H74	
	Motorola	MC7453	
	TI	SN74H53	
N8859	National	DM7440	
	TI	SN7450	
N8875	Motorola	MC7427	
	National	DM7427	
	TI	SN7427	
N8879	TI	SN7410	
N8881	ITT	ITT7401	
	Motorola	MC7401	
	National	DM7401	
	TI	SN7401	
N8890	ITT	ITT7404	
	National	DM7404	
	TI	SN7404	
N8891	ITT	ITT7405	
	National	DM7405	
	TI	SN7405	
N93415A	**NEC Micro**	**μPB2205**	**1418**
N9602	AMD	9602	
SE5009	**PMI**	**DAC-08**	**919**
SE529	National	LM161	
SE531	Raytheon	RM4531	
SE550	National	LM550	
SE555	AMD	SE555	
	Exar	XR555	
		XR555M	
	Intersil	SE555	
	Motorola	MC1555	
	National	LM555	
	Raytheon	RM555	
	RCA	CA555	
	Silicon G	SG555	
	TI	SE555	
SE556	Exar	XR556M	
	Motorola	MC3556	
SE556	Raytheon	RM556	
	Silicon G	SG556	
	TI	SE556	
SE565	National	LM565	
SE566	National	LM566	
SE567	National	LM567	
SE5733	TI	μA733	
SE592	Motorola	MC1733	
		SE592	
SP380	National	DS8640	
SU536	Intersil	SU536	
S3532	TI	LM158	
◆S5709	Signetics	μA709	
◆S5710	Signetics	μA710	
◆S5711	Signetics	μA711	
◆S5723	Signetics	μA723	
◆S5733	Signetics	μA733	
◆S5741	Signetics	μA741	
S7280	National	DM7280	
S7281	National	DM7281	
S7290	National	DM7290	
S7291	National	DM7291	
S8H16	National	DM54H20	
S8H70	National	DM54H10	
	TI	SN54H11	
S8H80	National	DM54H00	
	TI	SN54H00	
S8H90	National	DM54H04	
	TI	SN54H04	
S8T09	Raytheon	RM8T09	
S8T10	National	DM7551	
	Raytheon	RM8T10	
	TI	SN54173	
S8T13	Fairchild	8T13	
	TI	SN55121	
S8T14	Fairchild	8T14	
	TI	SN55122	
S8T22	Fairchild	9601	
	National	DM9601	
	TI	SN29601	
S8T26	AMD	S8T26	
S8T28	AMD	S8T28	
S8T54	National	DM5448	
S8T95	National	DM7095	
S8T96	National	DM7096	
S8T97	National	DM7097	
S8T98	National	DM7098	
S82LS29	TI	SN54S287	
S82S06	Raytheon	RM5340	
	TI	SN54S201	
S82S07	Raytheon	RM5330	
	TI	SN54S301	
S82S115	Intel	M3624	
S82S123	**Harris**	**HM7603**	**1192**
	MMI	**5331**	**1248**
	National	DM7578	
	TI	SN54S288	
S82S126	**Harris**	**HM7610**	**1192**
		HM7610A	**1200**
		HPROM1024A	
	MMI	**5300**	**1248**
	National	**DM54S387**	**1264**
	TI	SN54S387	
S82S129	**Harris**	**HM7611**	**1192**
		HM7611A	**1200**
		HPROM1024	
	National	**DM54S287**	**1264**
	TI	SN54S287	
S82S130	**Harris**	**HM7620**	**1192**
		HM7620A	**1202**
	MMI	**5305**	**1248**
S82S131	**Harris**	**HM7621**	**1192**
		HM7621A	**1202**
	MMI	**5306**	**1248**
	National	**DM54S571**	**1266**
S82S136	**Harris**	**HM7642**	**1192**
	MMI	**5352**	**1563**
	National	**DM54S572**	**1268**
S82S137	**Harris**	**HM7643**	**1192**
	MMI	**5353**	**1563**
S82S140	**National**	**DM77S295**	**1270**
S82S141	**National**	**DM77S296**	**1270**
S82S16	National	DM54S200	
	TI	SN54S201	
S82S17	**National**	**DM54S206**	**1297**
	TI	SN54S301	

◆ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
S82S180	National	DM75S229	
S82S181	National	DM75S228	
S82S226	TI	SN54187	
S82S229	TI	SN54S287	
S82S23	**Harris**	**HM7602**	**1192**
	MMI	**5330**	**1248**
	TI	SN54S188	
S82S230	TI	SN54S270	
S82S231	TI	SN54S370	
S82S25	TI	SN54S289	
		SN54S301	
S82S26	AMD	82S26	
	TI	SN54S387	
S82S30	Fairchild	93S12	
S82S41	National	DM54LS386	
S82S62	Fairchild	93S62	
S82S80	National	DM54LS196	
S82S81	National	DM54LS197	
S82S90	National	DM54LS196	
S82S91	National	DM54LS197	
S8200	Raytheon	RM8200	
S8201	Raytheon	RM8201	
S8202	Raytheon	RM8202	
S8203	Raytheon	RM8203	
S8207	TI	SN54S301	
S82147	National	DM54147	
S82148	National	DM54148	
S8223	Harris	HPROM8256	
	Intersil	IM5600	
	MMI	**5330**	**1248**
	National	DM7577	
	TI	SN54S188	
S8224	National	DM5488	
	TI	SN5488A	
S8225	Fairchild	93403	
	TI	SN54S289	
S8230	Fairchild	9312	
	National	DM9312	
	Raytheon	RM8230	
	TI	SN39312	
S8231	Fairchild	9313	
	Raytheon	RM8231	
S8241	National	DM54LS386	
	Raytheon	RM8241	
S8242	Fairchild	9386	
	Raytheon	RM8242	
	TI	SN54LS266	
S8250	Raytheon	RM8250	
S8251	Raytheon	RM8251	
S8252	Fairchild	9301	
	National	DM9301	
	Raytheon	RM8252	
	TI	SN39301	
S8260	Raytheon	RM8260	
S8261	Raytheon	RM8261	
S8262	Raytheon	RM8262	
S8263	Raytheon	RM8263	
S8264	Raytheon	RM8264	
S8266	Raytheon	RM8266	
S8267	Raytheon	RM8267	
S8268	TI	SN5480	
S8269	National	DM7200	
S8270	Fairchild	93178	
	Raytheon	RM8270	
	TI	SN54178	
S8271	Fairchild	93179	
	Raytheon	RM8271	
	TI	SN54179	
S8277	Fairchild	9328	
	Raytheon	RM8277	
S8280	Fairchild	93176	
	Raytheon	RM8280	
	TI	SN54176	
S8281	Fairchild	93177	
	Raytheon	RM8281	
	TI	SN54177	
S8288	National	DM7288	
S8290	Fairchild	93196	
	Raytheon	RM8290	
	TI	SN54196	
S8291	Fairchild	93197	
	Raytheon	RM8291	
	TI	SN54197	
S8292	National	DM54LS196	
	TI	SN54LS196	
S8293	National	DM54LS197	
	TI	SN54LS197	
S8455	National	DM5440	
	TI	SN5440	
S8470	National	DM5410	
	TI	SN5410	
S8471	National	DM54LS12	
	TI	SN5412	
S8480	National	DM5400	
	TI	SN5400	
S8481	National	DM5403	
	TI	SN5403	
S8490	National	DM5404	
	TI	SN5404	
S8806	National	DM5460	
	TI	SN5460	
S8808	National	DM5430	
	TI	SN5430	
S8815	National	DM5425	
	TI	SN5425	
S8828	National	DM5474	
	TI	SN5474	
S8840	National	DM5451	
	TI	SN5450	
S8848	National	DM54LS54	
	TI	SN54H53	
S8859	National	DM5440	
S8875	National	DM5427	
	TI	SN5427	
S8881	National	DM5401	
	TI	SN5401	
S8890	National	DM5404	
	TI	SN5404	
S8891	National	DM5405	
	TI	SN5405	
TBA520	Plessey	TBA520	
TBA530	Plessey	TBA530	
TBA540	Plessey	TBA540	
~~TBA550~~	~~Plessey~~	~~TBA550~~	
TBA560	Plessey	TBA560	
TBA750	Plessey	TBA750	
TBA920	Plessey	TBA920	
TBA990	Plessey	TBA990	
TCA800	Plessey	TCA800	
♦TDA1034	Signetics	NE5534	
UDN5711	Sprague	UDN-5711	
UDN5712	Sprague	UDN-5712	
UDN5713	Sprague	UDN-5713	
UDN5714	Sprague	UDN-5714	
ULN2001	Exar	XR2201	
	Sprague	ULN-2001	
ULN2002	Exar	XR2202	
	Sprague	ULN-2002	
ULN2003	Exar	XR2203	
	Sprague	ULN2003	
ULN2004	Exar	XR2204	
	Sprague	ULN-2004	
ULN2111	Motorola	MC1357	
	RCA	CA2111	
	Sprague	ULN-2111	
10100	Fairchild	F10100	
	Motorola	MC10100	
	NEC America	μPB10100	
	Plessey	SP10100	
10101	Fairchild	F10101	
	Hitachi	HD10101	
	Motorola	MC10101	
	NEC America	μPB10101	
	Plessey	SP10101	
10102	Fairchild	F10102	
	Hitachi	HD10102	
	Motorola	MC10102	
	NEC America	μPB10102	
	Plessey	SP10102	
10103	Fairchild	F10103	
	Motorola	MC10103	
	NEC America	μPB10103	
	Plessey	SP10103	
10104	Fairchild	F10104	
	Hitachi	HD10104	
	Motorola	MC10104	
	Plessey	SP10104	
10105	Fairchild	F10105	
	Hitachi	HD10105	
10105	Motorola	MC10105	
	National	DM10105	
	NEC America	μPB10105	
	Plessey	SP10105	
10106	Fairchild	F10106	
	Hitachi	HD10106	
	Motorola	MC10106	
	National	DM10106	
	NEC America	μPB10106	
	Plessey	SP10106	
10107	Fairchild	F10107	
	Hitachi	HD10107	
	Motorola	MC10107	
	NEC America	μPB10107	
	Plessey	SP10107	
10109	Fairchild	F10109	
	Hitachi	HD10109	
	Motorola	MC10109	
	National	DM10109	
	NEC America	μPB10109	
	Plessey	SP10109	
10110	Fairchild	F10110	
	Hitachi	HD10110	
	Motorola	MC10110	
	NEC America	μPB10110	
	Plessey	SP10110	
10111	Fairchild	F10111	
	Hitachi	HD10111	
	Motorola	MC10111	
	National	DM10111	
	NEC America	μPB10111	
	Plessey	SP10111	
10112	National	DM10112	
	Plessey	SP10112	
10113	Fairchild	F10113	
	Motorola	MC10113	
	Plessey	SP10113	
10114	Fairchild	F10114	
	Motorola	MC10114	
	Plessey	SP10114	
10115	~~Fairchild~~	~~F10115~~	
	Motorola	MC10115	
	National	DM10115	
	NEC America	μPB10115	
	Plessey	SP10115	
10116	Fairchild	F10116	
	Hitachi	HD10116	
	Motorola	MC10116	
	National	DM10116	
	Plessey	SP10116	
10117	Fairchild	F10117	
	Hitachi	HD10117	
	Motorola	MC10117	
	National	DM10117	
	NEC America	μPB10117	
	Plessey	SP10117	
10118	Fairchild	F10118	
	Hitachi	HD10118	
	Motorola	MC10118	
	National	DM10118	
	NEC America	μPB10118	
	Plessey	SP10118	
10119	Fairchild	F10119	
	Hitachi	HD10119	
	Motorola	MC10119	
	National	DM10119	
	Plessey	SP10119	
10121	Fairchild	F10121	
	Hitachi	HD10121	
	Motorola	MC10121	
	National	DM10121	
	Plessey	SP10121	
10123	Fairchild	F10123	
	Motorola	MC10123	
	Plessey	SP10123	
10124	Fairchild	F10124	
	Hitachi	HD10124	
	Motorola	MC10124	
	National	DM10124	
	NEC America	μPB10124	
	Plessey	SP10124	
10125	Fairchild	F10125	
	Hitachi	HD10125	
	Motorola	MC10125	
	Plessey	SP10125	
10129	Motorola	MC10129	
10129	Plessey	SP10129	
10130	Fairchild	F10130	
	Hitachi	HD10130	
	Motorola	MC10130	
	Plessey	SP10130	
10131	Fairchild	F10131	
	Hitachi	HD10131	
	Motorola	MC10131	
	NEC America	μPB10131	
	Plessey	SP10131	
10132	Fairchild	F10132	
	Hitachi	HD10132	
	Motorola	MC10132	
10133	Fairchild	F10133	
	Hitachi	HD10133	
	Motorola	MC10133	
	NEC America	μPB10133	
	Plessey	SP10133	
10134	Fairchild	F10134	
	Hitachi	HD10134	
	Motorola	MC10134	
	Plessey	SP10134	
10135	Fairchild	F10135	
	Motorola	MC10135	
	Plessey	SP10135	
10136	Fairchild	F10136	
	Hitachi	HD10136	
	Motorola	MC10136	
	Plessey	SP10136	
10137	Fairchild	F10137	
	Motorola	MC10137	
	Plessey	SP10137	
10139	TI	SN10139	
10140	Plessey	SP10140	
	TI	SN10140	
10141	Fairchild	F10141	
	Motorola	MCM10141	
		MC10141	
	Plessey	SP10141	
10144	Fairchild	F10410	
	Motorola	MC10144	
	NEC America	μPB10144	
	Plessey	SP10144	
	Raytheon	RC10144	
	TI	SN10144	
10145	Fairchild	F10145	
	Hitachi	HD10145	
	Motorola	MCM10145	
		MC10145	
	Plessey	SP10145	
	TI	SN10145	
10148	Hitachi	HD10148	
	NEC America	μPB10148	
	Plessey	SP10148	
	TI	SN10148	
♦10149	Fairchild	10149	
	Motorola	MCM10149	
		MC10149	
10158	Fairchild	F10158	
	Motorola	MC10158	
	NEC America	μPB10158	
10159	Fairchild	F10159	
	Motorola	MC10159	
10160	Fairchild	F10160	
	Hitachi	HD10160	
	Motorola	MC10160	
	Plessey	SP10160	
10161	Fairchild	F10161	
	Hitachi	HD10161	
	Motorola	MC10161	
	NEC America	μPB10161	
	Plessey	SP10161	
10162	Fairchild	F10162	
	Hitachi	HD10162	
	Motorola	MC10162	
	NEC America	μPB10162	
	Plessey	SP10162	
10164	Fairchild	F10164	
	Hitachi	HD10164	
	Motorola	MC10164	
	NEC America	μPB10164	
	Plessey	SP10164	
	TI	SN10164	
10165	Fairchild	F10165	
	Hitachi	HD10165	
	Motorola	MC10165	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
10165	Plessey	SP10165	
10170	Fairchild	F10170	
	Motorola	MC10170	
10171	Fairchild	F10171	
	Motorola	MC10171	
	Plessey	SP10171	
10172	Fairchild	F10172	
	Motorola	MC10172	
	Plessey	SP10172	
10173	Fairchild	F10173	
	Motorola	MC10173	
	Plessey	SP10173	
10174	Fairchild	F10174	
	Hitachi	HD10174	
	Motorola	MC10174	
	NEC America	μPB10174	
	Plessey	SP10174	
	TI	SN10174	
10175	Fairchild	F10175	
	Hitachi	HD10175	
	Motorola	MC10175	
	Plessey	SP10175	
10176	Fairchild	F10176	
	Motorola	MC10176	
	Plessey	SP10176	
10179	Fairchild	F10179	
	Hitachi	HD10179	
	Motorola	MC10179	
	Plessey	SP10179	
10180	Fairchild	F10180	
	Hitachi	HD10180	
	Motorola	MC10180	
	NEC America	μPB10180	
	Plessey	SP10180	
10181	Fairchild	F10181	
	Hitachi	HD10181	
	Motorola	MC10181	
	NEC Micro	μPB10181	
	Plessey	SP10181	
10191	Motorola	MC10191	
10192	Fairchild	F10192	
10210	Motorola	MC10210	
10211	Motorola	MC10211	
10212	Motorola	MC10212	
1103	TI	TMS1103	
11031	Motorola	MC10131	
1702	Intel	1702A	
21F02	Fairchild	2102	
		21021	
	Intel	2102A	
21L02	AMD	91L02	
	Fairchild	21026	
2101	Intel	2101	
	NEC Micro	**μPD2101AL**	**1424**
2102	AMD	2102	
	Fairchild	21021	
		21022	
	Mostek	MK4102	
	National	**MM2102**	**1300**
	NEC Micro	**μPD2102AL**	**1429**
	TI	TMS4035	
2111	Intel	2111	
	NEC Micro	**μPD2111AL**	**1433**
2112	Intel	2112	
2115	Intel	2115	
2125	Intel	2125	
2316	**NEC Micro**	**μPD2316**	**1481**
2352	SGS	M142	
2400	AMI	S8773	
2441	AMI	S8773	
2451	AMI	S8773	
2461	AMI	S8773	
2462	AMI	S8773	
25L01	Intersil	IM7512	
	Mostek	MK4007	
2501	Intersil	IM7501	
	Mostek	MK4007	
2502	SGS	M141	
	Synertek	SY1402	
2503	AMI	S2503A	
	SGS	M136	
	Synertek	SY1403	
2504	SGS	M140	
2504	Synertek	SY1404	
2505	AMD	AM2505	
	AMI	S505A	
2512	AMD	AM2806	
	AMI	S2512A	
	Intersil	IM7712	
	Nortec	2512	
2513	GI	RO3-2513	
2517	AMD	1507	
2521	AMD	AM2521	
	AMI	S2181	
	TI	TMS3128	
2522	AMI	S2181	
	TI	TMS3129	
2524	AMD	AM2807	
	AMI	S1685	
2525	AMD	AM2808	
	Intersil	IM7722	
2526	AMI	S8564	
2527	Synertek	SY2527	
2532	AMI	S2181	
	Fairchild	3347	
		3357	
	Intersil	IM7780	
	Mostek	MK1007	
	TI	TMS3120	
2533	AMD	AM2833	
	Synertek	SY2533	
2536	GI	AY3-1014A	
		AY3-1015	
		AY5-1013A	
	TI	TMS6011	
♦2548	Nortec	6003	
♦2554	SGS	M130	
2600	EA	4600	
2601	**NEC Micro**	**μPD2101AL**	**1424**
♦2602	Intersil	IM7752	
	Mostek	MK4102	
	TI	TMS4033	
		TMS4035	
2607	EA	EA2308A	
	Synertek	SY2308A	
2608	Motorola	MCM6830	
2609	Motorola	MCM6570	
	Nitron	NC6570	
2611	**NEC Micro**	**μPD2111AL**	**1433**
2613	TI	TMS4044	
2614	TI	TMS4045	
2616	Intel	2316B	
2617	AMD	9216	
2650	**National**	**INS2650**	**1656**
2651	National	INS2651	
2652	National	INS2652	
	SMC	COM5025	
2656	National	INS2656	
2660	Mostek	MK4096	
2670	**National**	**MM5270**	**1325**
2680	TI	TMS4060	
3207	Fairchild	9607	
	ITT	ITT75361	
54H00	Fairchild	54H00	
		9H00	
	ITT	ITT54H00	
	National	DM54H00	
	Raytheon	54H00	
	TI	SN54H00	
54H01	Fairchild	54H01	
	ITT	ITT54H01	
	National	DM54H01	
	Raytheon	54H01	
	TI	SN54H01	
54H04	Fairchild	54H04	
	ITT	ITT54H04	
	National	DM54H04	
	Raytheon	54H04	
	TI	SN54H04	
54H05	Fairchild	54H05	
	ITT	ITT54H05	
	National	DM54H05	
	Raytheon	54H05	
	TI	SN54H05	
54H08	Fairchild	54H08	
	National	DM54H08	
54H10	Fairchild	54H10	
	ITT	ITT54H10	
	National	DM54H10	
54H10	Raytheon	54H10	
	TI	SN54H10	
54H101	Fairchild	54H101	
	TI	SN54H101	
54H102	Fairchild	54H102	
	TI	SN54H102	
54H103	Fairchild	54H103	
	National	DM54H103	
	TI	SN54H103	
54H106	Fairchild	54H106	
	National	DM54H106	
	TI	SN54H106	
54H108	Fairchild	54H108	
	National	DM54H108	
	TI	SN54H108	
54H11	Fairchild	54H11	
	ITT	ITT54H11	
	National	DM54H11	
	Raytheon	54H11	
	TI	SN54H11	
54H20	Fairchild	54H20	
	ITT	ITT54H20	
	National	DM54H20	
	Raytheon	54H20	
	TI	SN54H20	
54H21	Fairchild	54H21	
	ITT	ITT54H21	
	National	DM54H21	
54H22	Fairchild	54H22	
	National	DM54H22	
	Raytheon	54H22	
	TI	SN54H22	
54H30	Fairchild	54H30	
	ITT	ITT54H30	
	National	DM54H30	
	TI	SN54H30	
54H40	Fairchild	54H40	
	ITT	ITT54H40	
	National	DM54H40	
	Raytheon	54H40	
	TI	SN54H40	
54H50	Fairchild	54H50	
	ITT	ITT54H50	
	National	DM54H50	
	TI	SN54H50	
54H51	Fairchild	54H51	
	ITT	ITT54H51	
	National	DM54H51	
	TI	SN54H51	
54H52	Fairchild	54H52	
	National	DM54H52	
	TI	SN54H52	
54H53	Fairchild	54H53	
	ITT	ITT54H53	
	National	DM54H53	
	TI	SN54H53	
54H54	Fairchild	54H54	
	ITT	ITT54H54	
	National	DM54H54	
	TI	SN54H54	
54H55	Fairchild	54H55	
	National	DM54H55	
	TI	SN54H55	
54H60	Fairchild	54H60	
	ITT	ITT54H60	
	National	DM54H60	
	TI	SN54H60	
54H61	Fairchild	54H61	
	National	DM54H61	
	TI	SN54H61	
54H62	Fairchild	54H62	
	National	DM54H62	
	TI	SN54H62	
54H71	Fairchild	54H71	
	National	DM54H71	
	TI	SN54H71	
54H72	Fairchild	54H72	
		54H73	
	ITT	ITT54H72	
	National	DM54H72	
	TI	SN54H72	
54H73	Fairchild	54H73	
	ITT	ITT54H73	
	National	DM54H73	
	TI	SN54H73	
54H74	Fairchild	54H74	
54H74	ITT	ITT54H74	
	National	DM54H74	
	Raytheon	54H74	
	TI	SN54H74	
54H76	Fairchild	54H76	
	National	DM54H76	
	TI	SN54H76	
54LS00	Fairchild	54LS00	
	Motorola	SN54LS00	
	National	DM54LS00	
	Raytheon	54LS00	
	TI	SN54LS00	
54LS01	Fairchild	54LS01	
	National	DM54LS01	
	Raytheon	54LS01	
	TI	SN54LS01	
54LS02	Fairchild	54LS02	
	Motorola	SN54LS02	
	National	DM54LS02	
	Raytheon	54LS02	
	TI	SN54LS02	
54LS03	Fairchild	54LS03	
	Motorola	SN54LS03	
	National	DM54LS03	
	Raytheon	54LS03	
	TI	SN54LS03	
54LS04	Fairchild	54LS04	
	Motorola	SN54LS04	
	National	DM54LS04	
	Raytheon	54LS04	
	TI	SN54LS04	
54LS05	Fairchild	54LS05	
	Motorola	SN54LS05	
	National	DM54LS05	
	Raytheon	54LS05	
	TI	SN54LS05	
54LS08	Fairchild	54LS08	
	Motorola	SN54LS08	
	National	DM54LS08	
	Raytheon	54LS08	
	TI	SN54LS08	
54LS09	Fairchild	54LS09	
	Motorola	SN54LS09	
	National	DM54LS09	
	Raytheon	54LS09	
	TI	SN54LS09	
54LS10	Fairchild	54LS10	
	Motorola	SN54LS10	
	National	DM54LS10	
	Raytheon	54LS10	
	TI	SN54LS10	
54LS107	Fairchild	54LS107	
	Motorola	SN54LS107	
	National	DM54LS107	
	Raytheon	54LS107	
	TI	SN54LS107	
54LS109	Fairchild	54LS109	
	Motorola	SN54LS109	
	National	DM54LS109	
	Raytheon	54LS109	
	TI	SN54LS109	
54LS11	Fairchild	54LS11	
	Motorola	SN54LS11	
	National	DM54LS11	
	Raytheon	54LS11	
	TI	SN54LS11	
54LS112	Fairchild	54LS112	
	National	DM54LS112	
	Raytheon	54LS112	
	TI	SN54LS112	
54LS113	Fairchild	54LS113	
	National	DM54LS113	
	Raytheon	54LS113	
	TI	SN54LS113	
54LS114	Fairchild	54LS114	
	Motorola	SN54LS114	
	National	DM54LS114	
	Raytheon	54LS114	
	TI	SN54LS114	
54LS12	Fairchild	54LS12	
	National	DM54LS12	
	Raytheon	54LS12	
	TI	SN54LS12	
54LS125	Fairchild	54LS125	
	National	DM54LS125	
	Raytheon	54LS125	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
54LS125	TI	SN54LS125A	
54LS126	Fairchild	54LS126	
	Motorola	SN54LS126	
	National	DM54LS126	
	Raytheon	54LS126	
	TI	SN54LS126A	
54LS13	Motorola	SN54LS13	
	National	DM54LS13	
	Raytheon	**54LS13**	**264**
	TI	SN54LS13	
54LS132	Fairchild	54LS132	
	Motorola	SN54LS132	
	National	DM54LS132	
	Raytheon	**54LS132**	**264**
	TI	SN54LS132	
54LS136	Fairchild	54LS136	
	Motorola	SN54LS136	
	Raytheon	54LS136	
	TI	SN54LS136	
54LS138	Fairchild	54LS138	
	Motorola	SN54LS138	
	National	DM54LS138	
	Raytheon	54LS138	
	TI	SN54LS138	
54LS139	Raytheon	54LS139	
54LS14	Fairchild	54LS14	
	Motorola	SN54LS14	
	National	DM54LS14	
	Raytheon	**54LS14**	**264**
	TI	SN54LS14	
54LS15	Fairchild	54LS15	
	Motorola	SN54LS15	
	National	DM54LS15	
	Raytheon	54LS15	
	TI	SN54LS15	
54LS151	AMD	SN54LS151	
	Fairchild	54LS151	
	Motorola	SN54LS151	
	National	DM54LS151	
	Raytheon	54LS151	
	TI	SN54LS151	
54LS153	AMD	SN54LS153	
	Fairchild	54LS153	
	Motorola	SN54LS153	
	National	DM54LS153	
	Raytheon	54LS153	
	TI	SN54LS153	
54LS154	National	DM54LS154	
54LS157	AMD	SN54LS157	
	Fairchild	54LS157	
	Motorola	SN54LS157	
	National	DM54LS157	
	Raytheon	54LS157	
	TI	SN54LS157	
54LS158	Fairchild	54LS158	
	Motorola	SN54LS158	
	National	DM54LS158	
	Raytheon	54LS158	
	TI	SN54LS158	
54LS160	Raytheon	54LS160	
54LS161	AMD	SN54LS161	
	Fairchild	54LS161	
	Motorola	SN54LS161	
	National	DM54LS161	
	Raytheon	54LS161	
	TI	SN54LS161	
54LS162	Raytheon	54LS162	
54LS163	AMD	SN54LS163	
	Fairchild	54LS163	
	Motorola	SN54LS163	
	National	DM54LS163	
	Raytheon	54LS163	
	TI	SN54LS163	
54LS164	AMD	SN54LS164	
	Fairchild	54LS164	
	Motorola	SN54LS164	
	National	DM54LS164	
	Raytheon	**54LS164**	**272**
	TI	SN54LS164	
54LS170	AMD	SN54LS170	
	Fairchild	54LS170	
	Motorola	SN54LS170	
	National	DM54LS170	
54LS170	Raytheon	54LS170	
	TI	SN54LS170	
54LS173	Fairchild	54LS173	
	National	DM54LS173	
	TI	SN54LS173	
54LS174	AMD	SN54LS174	
	Fairchild	54LS174	
	National	DM54LS174	
	Raytheon	54LS174	
	TI	SN54LS174	
54LS175	AMD	SN54LS175	
	Fairchild	54LS175	
	Motorola	SN54LS175	
	National	DM54LS175	
	Raytheon	54LS175	
	TI	SN54LS175	
54LS181	AMD	SN54LS181	
	Fairchild	54LS181	
	Motorola	SN54LS181	
	Raytheon	54LS181	
	TI	SN54LS181	
54LS190	AMD	SN54LS190	
	Fairchild	54LS190	
	Motorola	SN54LS190	
	National	DM54LS190	
	Raytheon	54LS190	
	TI	SN54LS190	
54LS191	AMD	SN54LS191	
	Fairchild	54LS191	
	Motorola	SN54LS191	
	National	DM54LS191	
	Raytheon	54LS191	
	TI	SN54LS191	
54LS192	AMD	SN54LS192	
	Fairchild	54LS192	
	Motorola	SN54LS192	
	National	DM54LS192	
	Raytheon	54LS192	
	TI	SN54LS192	
54LS193	AMD	SN54LS193	
	Fairchild	54LS193	
	Motorola	SN54LS193	
	National	DM54LS193	
	Raytheon	54LS193	
	TI	SN54LS193	
54LS194A	Raytheon	54LS194A	
54LS195A	AMD	SN54LS195A	
	Fairchild	54LS195	
	Motorola	SN54LS195	
	Raytheon	54LS195A	
	TI	SN54LS195A	
54LS196	Raytheon	54LS196	
54LS197	Raytheon	54LS197	
54LS20	Fairchild	54LS20	
	Motorola	SN54LS20	
	National	DM54LS20	
	Raytheon	54LS20	
	TI	SN54LS20	
54LS21	Fairchild	54LS21	
	Motorola	SN54LS21	
	National	DM54LS21	
	Raytheon	54LS21	
	TI	SN54LS21	
54LS22	Fairchild	54LS22	
	Motorola	SN54LS22	
	National	DM54LS22	
	Raytheon	54LS22	
	TI	SN54LS22	
54LS221	National	DM54LS221	
	Raytheon	**54LS221**	**275**
	TI	SN54LS221	
54LS251	AMD	SN54LS251	
	Fairchild	54LS251	
	Motorola	SN54LS251	
	Raytheon	54LS251	
	TI	SN54LS251	
54LS253	AMD	SN54LS253	
	Fairchild	54LS253	
	Motorola	SN54LS253	
	National	DM54LS253	
	Raytheon	54LS253	
	TI	SN54LS253	
54LS257	Fairchild	54LS257	
	Motorola	SN54LS257	
	National	DM54LS257	
	Raytheon	54LS257	
54LS257	TI	SN54LS257	
54LS26	Fairchild	54LS26	
	National	DM54LS26	
	Raytheon	54LS26	
	TI	SN54LS26	
54LS261	**Raytheon**	**54LS261**	**284**
	TI	SN54LS261	
54LS266	Fairchild	54LS266	
	Motorola	SN54LS266	
	Raytheon	54LS266	
	TI	SN54LS266	
54LS27	Fairchild	54LS27	
	Motorola	SN54LS27	
	National	DM54LS27	
	Raytheon	54LS27	
	TI	SN54LS27	
54LS279	Fairchild	54LS279	
	Motorola	SN54LS279	
	National	DM54LS279	
	Raytheon	74LS279	
	TI	SN54LS279	
54LS28	Raytheon	54LS28	
	TI	SN54LS28	
54LS283	Raytheon	54LS283	
54LS290	Fairchild	54LS290	
	TI	SN54LS290	
54LS293	Fairchild	54LS293	
	TI	SN54LS293	
54LS295A	Raytheon	54LS295A	
54LS30	Fairchild	54LS30	
	Motorola	SN54LS30	
	National	DM54LS30	
	Raytheon	54LS30	
	TI	SN54LS30	
54LS32	Fairchild	54LS32	
	Motorola	SN54LS32	
	National	DM54LS32	
	Raytheon	54LS32	
	TI	SN54LS32	
54LS33	Fairchild	54LS33	
	Raytheon	54LS33	
	TI	SN54LS33	
54LS365	Fairchild	54LS365	
	Motorola	SN54LS365	
	Raytheon	**54LS365**	**286**
	TI	SN54LS365	
54LS366	Fairchild	54LS366	
	Motorola	SN54LS366	
	Raytheon	**54LS366**	**286**
	TI	SN54LS366	
54LS367	Fairchild	54LS367	
	Motorola	SN54LS367	
	Raytheon	**54LS367**	**286**
	TI	SN54LS367	
54LS368	Fairchild	54LS368	
	Motorola	SN54LS368	
	Raytheon	**54LS368**	**286**
	TI	SN54LS368	
54LS37	Fairchild	54LS37	
	Motorola	SN54LS37	
	National	DM54LS37	
	Raytheon	54LS37	
	TI	SN54LS37	
54LS375	TI	SN54LS375	
54LS38	Fairchild	54LS38	
	Motorola	SN54LS38	
	National	DM54LS38	
	Raytheon	54LS38	
	TI	SN54LS38	
54LS386	Raytheon	SN54LS386	
	TI	SN54LS386	
54LS395	Fairchild	54LSO95	
	National	DM54LS395	
	Raytheon	**54LS395**	**291**
	TI	SN54LS395	
54LS40	Fairchild	54LS40	
	Motorola	SN54LS40	
	National	DM54LS40	
	Raytheon	54LS40	
	TI	SN54LS40	
54LS42	Fairchild	54LS42	
	Motorola	SN54LS42	
	National	DM54LS42	
	Raytheon	**54LS42**	**266**
	TI	SN54LS42	
54LS51	Fairchild	54LS51	
54LS51	Motorola	SN54LS51	
	National	DM54LS51	
	Raytheon	54LS51	
	TI	SN54LS51	
54LS54	Fairchild	54LS54	
	Motorola	SN54LS54	
	National	DM54LS54	
	Raytheon	54LS54	
	TI	SN54LS54	
54LS55	Fairchild	54LS55	
	Motorola	SN54LS55	
	National	DM54LS55	
	Raytheon	54LS55	
	TI	SN54LS55	
54LS670	AMD	SN54LS670	
	Fairchild	54LS670	
	Motorola	SN54LS670	
	National	DM54LS670	
	Raytheon	54LS670	
	TI	SN54LS670	
54LS73	Fairchild	54LS73	
	Motorola	SN54LS73	
	National	DM54LS73	
	Raytheon	54LS73	
	TI	SN54LS73	
54LS74	Fairchild	54LS74	
	Motorola	SN54LS74	
	National	DM54LS74	
	Raytheon	54LS74	
	TI	SN54LS74	
54LS75	Fairchild	54LS75	
	National	DM54LS75	
	Raytheon	54LS75	
	TI	SN54LS75	
54LS76	National	DM54LS76	
	Raytheon	54LS76	
	TI	SN54LS76	
54LS78	National	DM54LS78	
	Raytheon	54LS78	
	TI	SN54LS78	
54LS80	Raytheon	54LS80A	
54LS85	Fairchild	54LS85	
	National	DM54LS85	
	Raytheon	54LS85	
	TI	SN54LS85	
54LS86	Fairchild	54LS86	
	Motorola	SN54LS86	
	Raytheon	54LS86	
	TI	SN54LS86	
54LS90	Fairchild	54LS90	
	Motorola	SN54LS90	
	Raytheon	**54LS90**	**268**
	TI	SN54LS90	
54LS92	Motorola	SN54LS92	
	Raytheon	**54LS92**	**268**
	TI	SN54LS92	
54LS93	Fairchild	54LS93	
	Motorola	SN54LS93	
	Raytheon	**54LS93**	**268**
	TI	SN54LS93	
54LS95B	Raytheon	54LS95B	
54LS96	TI	SN54LS96	
54S00	Fairchild	54S00	
		9S00	
	TI	SN54S00	
54S02	Fairchild	54S02	
	TI	SN54S02	
54S04	Fairchild	54S04	
	TI	SN54S04	
54S05	Fairchild	54S05	
	TI	SN54S05	
54S08	Fairchild	54S08	
	TI	SN54S08	
54S09	Fairchild	54S09	
	TI	SN54S09	
54S11	Fairchild	54S11	
	TI	SN54S11	
54S139	AMD	SN54S139	
	Fairchild	54S139	
	TI	SN54S139	
54S140	AMD	SN54S140	
	TI	SN54S140	
54S15	Fairchild	54S15	
	TI	SN54S15	
54S151	AMD	SN54S151	
	Fairchild	54S151	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
54S151	TI	SN54S151	
54S153	AMD	SN54S153	
	Fairchild	54S153	
	TI	SN54S153	
54S157	AMD	SN54S157	
	Fairchild	54S157	
	TI	SN54S157	
54S158	AMD	SN54S158	
	Fairchild	54S158	
	TI	SN54S158	
54S181	AMD	SN54S181	
	Fairchild	54S181	
	TI	SN54S181	
54S22	Fairchild	54S22	
	National	DM54S22	
	TI	SN54S22	
54S251	AMD	SN54S251	
	Fairchild	54S251	
	TI	SN54S251	
54S253	AMD	SN54S253	
	Fairchild	54S253	
54S257	AMD	SN54S257	
	Fairchild	54S257	
	TI	SN74S257	
54S258	AMD	SN54S258	
	Fairchild	54S258	
	TI	SN54S258	
54S32	Fairchild	54S32	
	TI	SN54S32	
54S37	TI	SN54S37	
54S85	TI	SN54S85	
54S86	Fairchild	54S86	
	TI	SN54S86	
5400	Fairchild	5400	
		9N00	
	ITT	ITT5400	
	Motorola	MC5400	
	National	DM5400	
	Raytheon	5400	
	TI	SN5400	
5401	Fairchild	5401	
	ITT	ITT5401	
	Motorola	MC5401	
	National	DM5401	
	Raytheon	5401	
	TI	SN5401	
5402	Fairchild	5402	
	ITT	ITT5402	
	Motorola	MC5402	
	National	DM5402	
	TI	SN5402	
5403	Fairchild	5403	
	ITT	ITT5403	
	Motorola	MC5403	
	National	DM5403	
	Raytheon	5403	
	TI	SN5403	
5404	Fairchild	5404	
	ITT	ITT5404	
	Motorola	MC5404	
	National	DM5404	
	Raytheon	5404	
	TI	SN5404	
5405	Fairchild	5405	
	ITT	ITT5405	
	Motorola	MC5405	
	National	DM5405	
	Raytheon	5405	
	TI	SN5405	
5406	Fairchild	5406	
	ITT	ITT5406	
	Motorola	MC5406	
	National	DM5406	
	TI	SN5406	
5407	Fairchild	5407	
	ITT	ITT5407	
	Motorola	MC5407	
	National	DM5407	
	TI	SN5407	
5408	Fairchild	5408	
	ITT	ITT5408	
	Motorola	MC5408	
	National	DM5408	
5408	Raytheon	5408	
	TI	SN5408	
5409	Fairchild	5409	
	ITT	ITT5409	
	Motorola	MC5409	
	National	DM5409	
	Raytheon	5409	
	TI	SN5409	
5410	Fairchild	5410	
	ITT	ITT5410	
	Motorola	MC5410	
	National	DM5410	
	Raytheon	5410	
	TI	SN5410	
54100	Motorola	MC54100	
	TI	SN54100	
54107	Fairchild	54107	
	ITT	ITT54107	
	Motorola	MC54107	
	National	DM54107	
	TI	SN54107	
54109	National	DM54109	
	TI	SN54109	
5411	Fairchild	5411	
	ITT	ITT5411	
	National	DM5411	
	Raytheon	5411	
	TI	SN5411	
54116	Fairchild	54116	
	TI	SN54116	
5412	Fairchild	5412	
	ITT	ITT5412	
	Raytheon	5412	
	TI	SN5412	
54121	Fairchild	54121	
	ITT	ITT54121	
	Motorola	MC54121	
	National	DM54121	
	TI	SN54121	
54123	AMD	SN54123	
	Fairchild	54123	
	ITT	ITT54123	
	Motorola	MC54123	
	National	DM54123	
	Raytheon	54123	
	TI	SN54123	
54125	Fairchild	54125	
	National	DM54125	
	TI	SN54125	
54126	Fairchild	54126	
	National	DM54126	
	TI	SN54126	
54128	TI	SN54128	
5413	Fairchild	5413	
	ITT	ITT5413	
	Motorola	MC5413	
	National	DM5413	
	TI	SN5413	
54132	Fairchild	54132	
	Motorola	MC54132	
	National	DM54132	
	TI	SN54132	
5414	Fairchild	5414	
	Motorola	MC5414	
	National	DM5414	
	TI	SN5414	
54145	Fairchild	54145	
	ITT	ITT54145	
	Motorola	MC54145	
	National	DM54145	
	Raytheon	54145	
	TI	SN54145	
54147	National	DM54147	
	TI	SN54147	
54148	National	DM54148	
	TI	SN54148	
54150	Fairchild	54150	
	Motorola	MC54150	
	National	DM54150	
	Raytheon	54150	
	TI	SN54150	
54151	Fairchild	54151	
	ITT	ITT54151	
	Motorola	MC54151	
	National	DM54151	
	Raytheon	54151	
54151	TI	SN54151	
54152	Fairchild	54152	
	Motorola	MC54152	
	Raytheon	54152	
	TI	SN54152	
54153	Fairchild	54153	
	ITT	ITT54153	
	Motorola	MC54153	
	National	DM54153	
	Raytheon	54153	
	TI	SN54153	
54154	AMD	SN54154	
	Fairchild	54154	
	Motorola	MC54154	
	National	DM54154	
	Raytheon	54154	
	TI	SN54154	
54155	Fairchild	54155	
	ITT	ITT54155	
	Motorola	MC54155	
	National	DM54155	
	Raytheon	54155	
	TI	SN54155	
54156	Fairchild	54156	
	ITT	ITT54156	
	Motorola	MC54156	
	National	DM54156	
	Raytheon	54156	
	TI	SN54156	
54157	AMD	SN54157	
	Fairchild	54157	
	ITT	ITT54157	
	Motorola	MC54157	
	National	DM54157	
	Raytheon	54157	
	TI	SN54157	
54158	Raytheon	54158	
5416	Fairchild	5416	
	ITT	ITT5416	
	Motorola	MC5416	
	National	DM5416	
	TI	SN5416	
54160	AMD	SN54160	
	Fairchild	54160	
	ITT	ITT54160	
	Motorola	MC54160	
	National	DM54160	
	Raytheon	54160	
	TI	SN54160	
54161	AMD	SN54161	
	Fairchild	54161	
	ITT	ITT54161	
	Motorola	MC54161	
	National	DM54161	
	Raytheon	54161	
	TI	SN54161	
54162	AMD	SN54162	
	Fairchild	54162	
	ITT	ITT54162	
	Motorola	MC54162	
	National	DM54162	
	Raytheon	54162	
	TI	SN54162	
54163	AMD	SN54163	
	Fairchild	54163	
	ITT	ITT54163	
	Motorola	MC54163	
	National	DM54163	
	Raytheon	54163	
	TI	SN54163	
54164	AMD	SN54164	
	Fairchild	54164	
	ITT	ITT54164	
	National	DM54164	
	Raytheon	54164	
	TI	SN54164	
54165	Fairchild	54165	
	Motorola	MC54165	
	National	DM54165	
	Raytheon	54165	
	TI	SN54165	
54166	Fairchild	54166	
	National	DM54166	
	Raytheon	54166	
	TI	SN54166	
5417	Fairchild	5417	
5417	ITT	ITT5417	
	Motorola	MC5417	
	National	DM5417	
	TI	SN5417	
54170	Fairchild	54170	
	National	DM54170	
	Raytheon	54170	
	TI	SN54170	
54174	AMD	SN74174	
	Fairchild	54174	
	Motorola	MC54174	
	National	DM54174	
	Raytheon	54174	
	TI	SN54174	
54175	AMD	SN54175	
	Fairchild	54175	
	Motorola	MC54175	
	National	DM54175	
	Raytheon	54175	
	TI	SN54175	
54176	Fairchild	54176	
	Motorola	MC54176	
	National	DM54176	
	TI	SN54176	
54177	Fairchild	54177	
	Motorola	MC54177	
	National	DM54177	
	TI	SN54177	
54180	Fairchild	54180	
	ITT	ITT54180	
	Motorola	MC54180	
	National	DM54180	
	Raytheon	54180	
	TI	SN54180	
54181	AMD	SN54181	
	Fairchild	54181	
	Motorola	MC54181	
	National	DM54181	
	Raytheon	54181	
	TI	SN54181	
54182	AMD	SN54182	
	Fairchild	54182	
	ITT	ITT54182	
	Motorola	MC54182	
	National	DM54182	
	Raytheon	54182	
	TI	SN54182	
54190	Fairchild	54190	
	ITT	ITT54190	
	Motorola	MC54190	
	National	DM54190	
	Raytheon	54190	
	TI	SN54190	
54191	Fairchild	54191	
	ITT	ITT54191	
	Motorola	MC54191	
	National	DM54191	
	Raytheon	54191	
	TI	SN54191	
54192	AMD	SN54192	
	Fairchild	54192	
	ITT	ITT54192	
	Motorola	MC54192	
	National	DM54192	
	Raytheon	54192	
	TI	SN54192	
54193	AMD	SN54193	
	Fairchild	54193	
	ITT	ITT54193	
	Motorola	MC54193	
	National	DM54193	
	Raytheon	54193	
	TI	SN54193	
54194	AMD	SN54194	
	Fairchild	54194	
	ITT	ITT54194	
	Motorola	MC54194	
	National	DM54194	
	TI	SN54194	
54195	AMD	SN54195	
	Fairchild	54195	
	ITT	ITT54195	
	Motorola	MC54195	
	National	DM54195	
	Raytheon	54195	
	TI	SN54195	

◆ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
54196	Fairchild	54196	
	Motorola	MC54196	
	National	DM54196	
	TI	SN54196	
54197	Fairchild	54197	
	Motorola	MC54197	
	National	DM54197	
	TI	SN54197	
54198	Fairchild	54198	
	National	DM54198	
	Raytheon	54198	
	TI	SN54198	
54199	Fairchild	54199	
	National	DM54199	
	Raytheon	54199	
	TI	SN54199	
5420	Fairchild	5420	
	ITT	ITT5420	
	Motorola	MC5420	
	National	DM5420	
	Raytheon	5420	
	TI	SN5420	
5421	Fairchild	5421	
	ITT	ITT5421	
	Raytheon	5421	
5426	Fairchild	5426	
	ITT	ITT5426	
	Motorola	MC5426	
	National	DM5426	
	TI	SN5426	
54279	Fairchild	54279	
	TI	SN54279	
54298	Fairchild	54298	
	Motorola	MC54298	
	TI	SN54298	
5430	Fairchild	5430	
	ITT	ITT5430	
	Motorola	MC5430	
	National	DM5430	
	TI	SN5430	
5432	Fairchild	5432	
	ITT	ITT5432	
	National	DM5432	
	TI	SN5432	
5437	Fairchild	5437	
	ITT	ITT5437	
	Motorola	MC5437	
	National	DM5437	
	Raytheon	5437	
	TI	SN5437	
5438	Fairchild	5438	
	ITT	ITT5438	
	Motorola	MC5438	
	National	DM5438	
	Raytheon	5438	
	TI	SN5438	
5440	Fairchild	5440	
	ITT	ITT5440	
	Motorola	MC5440	
	National	DM5440	
	TI	SN5440	
5442	Fairchild	5442	
	ITT	ITT5442	
	Motorola	MC5442	
	National	DM5442	
	Raytheon	5442	
	TI	SN5442	
5443	Fairchild	5443	
	ITT	ITT5443	
	Motorola	MC5443	
	Raytheon	5443	
	TI	SN5443	
5444	Fairchild	5444	
	ITT	ITT5444	
	Motorola	MC5444	
	Raytheon	5444	
	TI	SN5444	
5445	Fairchild	5445	
	ITT	ITT5445	
	Motorola	MC5445	
	National	DM5445	
	Raytheon	5445	
	TI	SN5445	
5446	Fairchild	5446	
	ITT	ITT5446	
	Motorola	MC5446	
	National	DM5446	
	TI	SN5446	
5447	Fairchild	5447	
	ITT	ITT5447	
	Motorola	MC5447	
	National	DM5447	
	TI	SN5447	
5448	Fairchild	5448	
	ITT	ITT5448	
	Motorola	MC5448	
	National	DM5448	
	TI	SN5448	
5450	Fairchild	5450	
	ITT	ITT5450	
	Motorola	MC5450	
	National	DM5450	
	TI	SN5450	
5451	Fairchild	5451	
	ITT	ITT5451	
	Motorola	MC5451	
	National	DM5451	
	TI	SN5451	
5453	Fairchild	5453	
	ITT	ITT5453	
	Motorola	MC5453	
	National	DM5453	
	TI	SN5453	
5454	Fairchild	5454	
	ITT	ITT5454	
	Motorola	MC5454	
	National	DM5454	
	TI	SN5454	
5460	Fairchild	5460	
	Motorola	MC5460	
	National	DM5460	
	TI	SN5460	
5472	Fairchild	5472	
	ITT	ITT5472	
	Motorola	MC5472	
	National	DM5472	
	TI	SN5472	
5473	Fairchild	5473	
	ITT	ITT5473	
	Motorola	MC5473	
	National	DM5473	
	TI	SN5473	
5474	Fairchild	5474	
	ITT	ITT5474	
	Motorola	MC5474	
	National	DM5474	
	Raytheon	5474	
	TI	SN5474	
5475	Fairchild	5475	
	ITT	ITT5475	
	Motorola	MC5475	
	National	DM5475	
	TI	SN5475	
5476	Fairchild	5476	
	ITT	ITT5476	
	Motorola	MC5476	
	National	DM5476	
	TI	SN5476	
5477	Fairchild	5477	
	Motorola	MC5477	
	TI	SN5477	
5480	Fairchild	5480	
	ITT	ITT5480	
	Motorola	MC5480	
	TI	SN5480	
5485	Fairchild	5485	
	Motorola	MC5485	
	National	DM5485	
	TI	SN5485	
5486	Fairchild	5486	
	ITT	ITT5486	
	Motorola	MC5486	
	National	DM5486	
	Raytheon	5486	
	TI	SN5486	
5490	Fairchild	5490	
	ITT	ITT5490	
	Motorola	MC5490	
	National	DM5490	
5490	TI	SN5490	
5491	Fairchild	5491	
	ITT	ITT5491	
	Motorola	MC5491	
	National	DM5491	
	TI	SN5491	
5492	Fairchild	5492	
	ITT	ITT5492	
	Motorola	MC5492	
	National	DM5492	
	TI	SN5492	
5495	Fairchild	5495	
	ITT	ITT5495	
	Motorola	MC5495	
	National	DM5495	
	TI	SN5495	
5496	Fairchild	5496	
	ITT	ITT5496	
	Motorola	MC5496	
	National	DM5496	
	TI	SN5496	
55325	TI	SN55325	
55450	TI	SN55450	
55451	TI	SN55451	
55452	TI	SN55452	
55453	TI	SN55453	
55454	TI	SN55454	
72S180	National	DM85S229	
72S52	National	DM8301	
7293	National	DM74LS197	
74H00	Fairchild	74H00	
		9H00	
	National	DM74H00	
	NEC America	μPB74H00	
	Raytheon	74H00	
	TI	SN74H00	
74H01	Fairchild	74H01	
	ITT	ITT74H01	
	National	DM74H01	
	NEC America	μPB74H01	
	Raytheon	74H01	
	TI	SN74H01	
74H04	Fairchild	74H04	
	ITT	ITT74H04	
	National	DM74H04	
	NEC America	μPB74H04	
	Raytheon	74H04	
	TI	SN74H04	
74H05	Raytheon	74H05	
	TI	SN74H05	
74H08	Fairchild	74H08	
	National	DM74H08	
74H10	Fairchild	74H10	
	ITT	ITT74H10	
	National	DM74H10	
	NEC America	μPB74H10	
	Raytheon	74H10	
	TI	SN74H10	
74H102	Fairchild	74H102	
	TI	SN74H102	
74H103	Fairchild	74H103	
	National	DM74H103	
	TI	SN74H103	
74H106	Fairchild	74H106	
	National	DM74H106	
	TI	SN74H106	
74H108	Fairchild	74H108	
	National	DM74H108	
	TI	SN74H108	
74H11	Fairchild	74H11	
	ITT	ITT74H11	
	National	DM74H11	
	Raytheon	74H11	
	TI	SN74H11	
74H20	Fairchild	74H20	
	ITT	ITT74H20	
	National	DM74H20	
	NEC America	μPB74H20	
	Raytheon	74H20	
	TI	SN74H20	
74H21	Fairchild	74H21	
	ITT	ITT74H21	
	National	DM74H21	
	TI	SN74H21	
74H22	Fairchild	74H22	
	National	DM74H22	
74H22	Raytheon	74H22	
	TI	SN74H22	
74H30	Fairchild	74H30	
	ITT	ITT74H30	
	National	DM74H30	
	NEC America	μPB74H30	
	TI	SN74H30	
74H40	Fairchild	74H40	
	ITT	ITT74H40	
	National	DM74H40	
	NEC America	μPB74H40	
	Raytheon	74H40	
	TI	SN74H40	
74H50	Fairchild	74H50	
	ITT	ITT74H50	
	National	DM74H50	
	TI	SN74H50	
74H51	Fairchild	74H51	
	ITT	ITT74H51	
	National	DM74H51	
	NEC America	μPB74H51	
	TI	SN74H51	
74H52	Fairchild	74H52	
	National	DM74H52	
	TI	SN74H52	
74H53	Fairchild	74H53	
	ITT	ITT74H53	
	National	DM74H53	
	TI	SN74H53	
74H54	Fairchild	74H54	
	ITT	ITT74H54	
	National	DM74H54	
	TI	SN74H54	
74H55	Fairchild	74H55	
	National	DM74H55	
	TI	SN74H55	
74H60	Fairchild	74H60	
	ITT	ITT74H60	
	National	DM74H60	
	TI	SN74H60	
74H61	Fairchild	74H61	
	TI	SN74H61	
74H62	Fairchild	74H62	
	National	DM74H62	
	TI	SN74H62	
74H71	Fairchild	74H71	
	National	DM74H71	
	TI	SN74H71	
74H72	Fairchild	74H72	
	ITT	ITT74H72	
	National	DM74H72	
	TI	SN74H72	
74H73	Fairchild	74H73	
	ITT	ITT74H73	
	National	DM74H73	
	TI	SN74H73	
74H74	Fairchild	74H74	
	ITT	ITT74H74	
	National	DM74H74	
	Raytheon	74H74	
	TI	SN74H74	
74H76	Fairchild	74H76	
	National	DM74H76	
	TI	SN74H76	
74LS00	Fairchild	74LS00	
	ITT	ITT74LS00	
	Motorola	SN74LS00	
	National	DM74LS00	
	NEC America	μPB74LS00	
	Raytheon	74LS00	
	TI	SN74LS00	
74LS01	Fairchild	74LS01	
	ITT	ITT74LS01	
	National	DM74LS01	
	Raytheon	74LS01	
	TI	SN74LS01	
74LS02	Fairchild	74LS02	
	ITT	ITT74LS02	
	Motorola	SN74LS02	
	National	DM74LS02	
	NEC America	μPB74LS02	
	Raytheon	74LS02	
	TI	SN74LS02	
74LS03	Fairchild	74LS03	
	ITT	ITT74LS03	
	Motorola	SN74LS03	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
74LS03	National	DM74LS03	
	NEC America	μPB74LS03	
	Raytheon	74LS03	
	TI	SN74LS03	
74LS04	Fairchild	74LS04	
	ITT	ITT74LS04	
	Motorola	SN74LS04	
	National	DM74LS04	
	NEC America	μPB74LS04	
	Raytheon	74LS04	
	TI	SN74LS04	
74LS05	Fairchild	74LS05	
	ITT	ITT74LS05	
	Motorola	SN74LS05	
	National	DM74LS05	
	NEC America	μPB74LS05	
	Raytheon	74LS05	
	TI	SN74LS05	
74LS08	Fairchild	74LS08	
	ITT	ITT74LS08	
	Motorola	SN74LS08	
	National	DM74LS08	
	NEC America	μPB74LS08	
	Raytheon	74LS08	
	TI	SN74LS08	
74LS09	Fairchild	74LS09	
	ITT	ITT74LS09	
	Motorola	SN74LS09	
	National	DM74LS09	
	Raytheon	74LS09	
	TI	SN74LS09	
74LS10	Fairchild	74LS10	
	ITT	ITT74LS10	
	Motorola	SN74LS10	
	National	DM74LS10	
	NEC America	μPB74LS10	
	Raytheon	74LS10	
	TI	SN74LS10	
74LS107	Fairchild	74LS107	
	ITT	ITT74LS107	
	National	DM74LS107	
	Raytheon	74LS107	
	TI	SN74LS107	
74LS109	Fairchild	74LS109	
	ITT	ITT74LS109A	
	Motorola	SN74LS109	
	National	DM74LS109	
	NEC America	μPB74LS109	
	Raytheon	**74LS109**	
	TI	SN74LS109	
74LS11	Fairchild	74LS11	
	ITT	ITT74LS11	
	Motorola	SN74LS11	
	National	DM74LS11	
	NEC America	μPB74LS11	
	Raytheon	74LS11	
	TI	SN74LS11	
74LS112	Fairchild	74LS112	
	ITT	ITT74LS112	
	National	DM74LS112	
	NEC America	μPB74LS112	
	Raytheon	74LS112	
	TI	SN74LS112	
74LS113	Fairchild	74LS113	
	ITT	ITT74LS113	
	National	DM74LS113	
	NEC America	μPB74LS113	
	Raytheon	74LS113	
	TI	SN74LS113	
74LS114	Fairchild	74LS114	
	ITT	ITT74LS114	
	Motorola	SN74LS114	
	National	DM74LS114	
	Raytheon	74LS114	
	TI	SN74LS114	
74LS12	Fairchild	74LS12	
	National	DM74LS12	
	Raytheon	74LS12	
	TI	SN74LS12	
74LS125	Fairchild	74LS125	
	ITT	ITT74LS125	
	National	DM74LS125	
	Raytheon	74LS125	
74LS125	TI	SN74LS125A	
74LS126	Fairchild	74LS126	
	ITT	ITT74LS126	
	Motorola	SN74LS126	
	National	DM74LS126	
	Raytheon	74LS126	
	TI	SN74LS126A	
74LS13	Fairchild	74LS13	
	ITT	ITT74LS13	
	Motorola	SN74LS13	
	National	DM74LS13	
	Raytheon	**74LS13**	**264**
	TI	SN74LS13	
74LS132	Fairchild	74LS132	
	ITT	ITT74LS132	
	Motorola	SN74LS132	
	National	DM74LS132	
	Raytheon	**74LS132**	**264**
	TI	SN74LS132	
74LS136	Fairchild	74LS136	
	ITT	ITT74LS136	
	Motorola	SN74LS136	
	National	DM74LS136	
	Raytheon	74LS136	
	TI	SN74LS136	
74LS138	AMD	SN74LS138	
	Fairchild	74LS138	
	ITT	ITT74LS138	
	Motorola	SN74LS138	
	National	DM74LS138	
	NEC America	μPB74LS138	
	Raytheon	74LS138	
	TI	SN74LS138	
74LS139	AMD	SN54LS139	
		SN74LS139	
	Fairchild	54LS139	
		74LS139	
	ITT	ITT74LS139	
	Motorola	SN54LS139	
		SN74LS139	
	National	DM54LS139	
		DM74LS139	
	NEC America	μPB74LS139	
	Raytheon	54LS139	
		74LS139	
	TI	SN54LS139	
		SN74LS139	
74LS14	Fairchild	74LS14	
	ITT	ITT74LS14	
	Motorola	SN74LS14	
	National	DM74LS14	
	Raytheon	**74LS14**	**264**
	TI	SN74LS14	
74LS145	Fairchild	74LS145	
	TI	SN74LS145	
74LS15	Fairchild	74LS15	
	ITT	ITT74LS15	
	Motorola	SN74LS15	
	National	DM74LS15	
	Raytheon	74LS15	
	TI	SN74LS15	
74LS151	AMD	SN74LS151	
	Fairchild	74LS151	
	ITT	ITT74LS151	
	Motorola	SN74LS151	
	National	DM74LS151	
	NEC America	μPB74LS151	
	Raytheon	74LS151	
	TI	SN74LS151	
74LS152	Raytheon	74LS152	
74LS153	AMD	SN74LS153	
	Fairchild	74LS153	
	ITT	ITT74LS153	
	Motorola	SN74LS153	
	National	DM74LS153	
	NEC America	μPB74LS153	
	Raytheon	74LS153	
	TI	SN74LS153	
74LS154	National	DM74LS154	
74LS155	Fairchild	74LS155	
	ITT	ITT74LS155	
	Motorola	SN74LS155	
	National	DM74LS155	
	NEC America	μPB74LS155	
	Raytheon	74LS155	
	TI	SN74LS155	
74LS156	Fairchild	74LS156	
	ITT	ITT74LS156	
	Motorola	SN74LS156	
	National	DM74LS156	
	Raytheon	74LS156	
	TI	SN74LS156	
74LS157	AMD	SN74LS157	
	Fairchild	74LS157	
	ITT	ITT74LS157	
	Motorola	SN74LS157	
	National	DM74LS157	
	NEC America	μPB74LS157	
	Raytheon	74LS157	
	TI	SN74LS157	
74LS158	AMD	SN74LS158	
	Fairchild	74LS158	
	ITT	ITT74LS158	
	Motorola	SN74LS158	
	National	DM74LS158	
	Raytheon	74LS158	
	TI	SN74LS158	
74LS160	AMD	SN74LS160	
	Fairchild	74LS160	
	ITT	ITT74LS160	
	Motorola	SN74LS160	
	National	DM74LS160	
	Raytheon	74LS160	
	TI	SN74LS160	
74LS161	AMD	SN74LS161	
	Fairchild	74LS161	
	ITT	ITT74LS161	
	Motorola	SN74LS161	
	National	DM74LS161	
	NEC America	μPB74LS161	
	Raytheon	74LS161	
	TI	SN74LS161	
74LS162	AMD	SN74LS162	
	Fairchild	74LS162	
	ITT	ITT74LS162	
	Motorola	SN74LS162	
	National	DM74LS162	
	Raytheon	74LS162	
	TI	SN74LS162	
74LS163	AMD	SN74LS163	
	Fairchild	74LS163	
	ITT	ITT74LS163	
	Motorola	SN74LS163	
	National	DM74LS163	
	Raytheon	74LS163	
	TI	SN74LS163	
74LS164	AMD	SN74LS164	
	Fairchild	74LS164	
	ITT	ITT74LS164	
	Motorola	SN74LS164	
	National	DM74LS164	
	NEC America	μPB74LS164	
	Raytheon	**74LS164**	**272**
	TI	SN74LS164	
74LS170	AMD	SN74LS170	
	Fairchild	74LS170	
	ITT	ITT74LS170	
	Motorola	SN74LS170	
	National	DM74LS170	
	Raytheon	74LS170	
	TI	SN74LS170	
74LS173	Fairchild	74LS173	
	National	DM74LS173	
	TI	SN74LS173	
74LS174	AMD	SN74LS174	
	Fairchild	74LS174	
	ITT	ITT74LS174	
	Motorola	SN74LS174	
	National	DM74LS174	
	Raytheon	74LS174	
	TI	SN74LS174	
74LS175	AMD	SN74LS175	
	Fairchild	74LS175	
	ITT	ITT74LS175	
	Motorola	SN74LS175	
	National	DM74LS175	
	NEC America	μPB74LS175	
	Raytheon	74LS175	
	TI	SN74LS175	
74LS181	AMD	SN74LS181	
	Fairchild	74LS181	
	Motorola	SN74LS181	
74LS181	Raytheon	74LS181	
	TI	SN74LS181	
74LS190	AMD	SN74LS190	
	Fairchild	74LS190	
	ITT	ITT74LS190	
	Motorola	SN74LS190	
	National	DM74LS190	
	Raytheon	74LS190	
	TI	SN74LS190	
74LS191	AMD	SN74LS191	
	Fairchild	74LS191	
	ITT	ITT74LS191	
	Motorola	SN74LS191	
	National	DM74LS191	
	Raytheon	74LS191	
	TI	SN74LS191	
74LS192	AMD	SN74LS192	
	Fairchild	74LS192	
	ITT	ITT74LS192	
	Motorola	SN74LS192	
	National	DM74LS192	
	NEC America	μPB74LS192	
	Raytheon	74LS192	
	TI	SN74LS192	
74LS193	AMD	SN74LS193	
	Fairchild	74LS193	
	ITT	ITT74LS193	
	Motorola	SN74LS193	
	National	DM74LS193	
	NEC America	μPB74LS193	
	Raytheon	74LS193	
	TI	SN74LS193	
74LS194A	AMD	SN74LS194A	
	Fairchild	74LS194	
	ITT	ITT74LS194A	
	Motorola	SN74LS194	
	National	DM74LS194	
	NEC America	μPB74LS194	
	Raytheon	74LS194A	
	TI	SN74LS194A	
74LS195A	AMD	SN74LS195A	
	Fairchild	74LS195	
	ITT	ITT74LS195A	
	Motorola	SN74LS195	
	National	DM74LS195	
	NEC America	μPB74LS195	
	Raytheon	74LS195A	
	TI	SN74LS195A	
74LS196	Fairchild	74LS196	
	ITT	ITT74LS196	
	Motorola	SN74LS196	
	National	DM74LS196	
	Raytheon	74LS196	
	TI	SN74LS196	
74LS197	Fairchild	74LS197	
	ITT	ITT74LS197	
	Motorola	SN74LS197	
	National	DM74LS197	
	Raytheon	74LS197	
	TI	SN74LS197	
74LS20	Fairchild	74LS20	
	ITT	ITT74LS20	
	Motorola	SN74LS20	
	National	DM74LS20	
	NEC America	μPB74LS20	
	Raytheon	74LS20	
	TI	SN74LS20	
74LS21	Fairchild	74LS21	
	ITT	ITT74LS21	
	Motorola	SN74LS21	
	National	DM74LS21	
	NEC America	μPB74LS21	
	Raytheon	74LS21	
	TI	SN74LS21	
74LS22	Fairchild	74LS22	
	ITT	ITT74LS22	
	Motorola	SN74LS22	
	National	DM74LS22	
	Raytheon	74LS22	
	TI	SN74LS22	
74LS221	Fairchild	74LS221	
	ITT	ITT74LS221	
	Motorola	SN74LS221	
	National	DM74LS221	
	Raytheon	**74LS221**	**275**
	TI	SN74LS221	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
74LS240	AMD	SN74LS240	
	Fairchild	74LS240	
	ITT	ITT74LS240	
	MMI	74LS240	
	Motorola	SN74LS240	
	Raytheon	**74LS240**	**279**
	TI	SN74LS240	
74LS241	AMD	SN74LS241	
	Fairchild	74LS241	
	ITT	ITT74LS241	
	MMI	74LS241	
	Motorola	SN74LS241	
	Raytheon	**74LS241**	**279**
	TI	SN74LS241	
74LS242	AMD	SN74LS242	
	Fairchild	74LS242	
	ITT	ITT74LS242	
	Motorola	SN74LS242	
	Raytheon	**74LS242**	**282**
	TI	SN74LS242	
74LS243	AMD	SN74LS243	
	Fairchild	74LS243	
	ITT	ITT74LS243	
	Motorola	SN74LS243	
	Raytheon	**74LS243**	**282**
	TI	SN74LS243	
74LS244	AMD	SN74LS244	
	Fairchild	74LS244	
	ITT	ITT74LS244	
	MMI	74LS244	
	Motorola	SN74LS244	
	Raytheon	**74LS244**	**279**
	TI	SN74LS244	
74LS251	AMD	SN74LS251	
	Fairchild	74LS251	
	ITT	ITT74LS251	
	Motorola	SN74LS251	
	~~National~~	~~DM74LS251~~	
	NEC America	μPB74LS251	
	Raytheon	74LS251	
	TI	SN74LS251	
74LS253	AMD	SN74LS253	
	Fairchild	74LS253	
	ITT	ITT74LS253	
	Motorola	SN74LS253	
	National	DM74LS253	
	NEC America	μPB74LS253	
	Raytheon	74LS253	
	TI	SN74LS253	
74LS257	AMD	SN74LS257	
	Fairchild	74LS257	
	ITT	ITT74LS257	
	Motorola	SN74LS257	
	National	DM74LS257	
	NEC America	μPB74LS257	
	Raytheon	74LS257	
	TI	SN74LS257	
74LS258	AMD	SN74LS258	
	Fairchild	74LS258	
	ITT	ITT74LS258	
	Motorola	SN74LS258	
	National	DM74LS258	
	NEC America	μPB74LS258	
	Raytheon	74LS258	
	TI	SN74LS258	
74LS26	Fairchild	74LS26	
	National	DM74LS26	
	Raytheon	74LS26	
	TI	SN74LS26	
74LS260	Fairchild	74LS260	
74LS261	ITT	ITT74LS261	
	Raytheon	**74LS261**	**284**
	TI	SN74LS261	
74LS266	Fairchild	74LS266	
	ITT	ITT74LS266	
	Motorola	SN74LS266	
	Raytheon	74LS266	
	TI	SN74LS266	
74LS27	Fairchild	74LS27	
	ITT	ITT74LS27	
	Motorola	SN74LS27	
	National	DM74LS27	
	NEC America	μPB74LS27	
74LS27	Raytheon	74LS27	
	TI	SN74LS27	
74LS273	AMD	SN74LS273	
	Fairchild	74LS273	
	ITT	ITT74LS273	
	TI	SN74LS273	
74LS279	Fairchild	74LS279	
	ITT	ITT74LS279	
	Motorola	SN74LS279	
	National	DM74LS279	
	NEC America	μPB74LS279	
	Raytheon	74LS279	
	TI	SN74LS279	
74LS28	Fairchild	74LS28	
	ITT	ITT74LS28	
	Raytheon	74LS28	
	TI	SN74LS28	
74LS283	Fairchild	74LS283	
	ITT	ITT74LS283	
	Motorola	SN74LS283	
	National	DM74LS283	
	Raytheon	74LS283	
	TI	SN74LS283	
74LS290	Fairchild	74LS290	
	ITT	ITT74LS290	
	Motorola	SN74LS290	
	National	DM74LS290	
	TI	SN74LS290	
74LS293	Fairchild	74LS293	
	ITT	ITT74LS293	
	Motorola	SN74LS293	
	National	DM74LS293	
	TI	SN74LS293	
74LS295	Fairchild	74LS295	
	Motorola	SN74LS295	
	NEC America	μPB74LS295	
	Raytheon	74LS295A	
	TI	SN74LS295B	
74LS295A	Raytheon	74LS295A	
74LS298	Fairchild	74LS298	
	~~Motorola~~	~~SN74LS298~~	
	Raytheon	74LS298	
	TI	SN74LS298	
74LS30	Fairchild	74LS30	
	ITT	ITT74LS30	
	Motorola	SN74LS30	
	National	DM74LS30	
	NEC America	μPB74LS30	
	Raytheon	74LS30	
	TI	SN74LS30	
74LS32	Fairchild	74LS32	
	ITT	ITT74LS32	
	Motorola	SN74LS32	
	National	DM74LS32	
	NEC America	μPB74LS32	
	Raytheon	74LS32	
	TI	SN74LS32	
74LS33	Raytheon	74LS33	
	TI	SN74LS33	
74LS365	Fairchild	74LS365	
	ITT	ITT74LS365	
	Motorola	SN74LS365	
	National	DM74LS365	
	NEC America	μPB74LS365	
	Raytheon	**74LS365**	**286**
	TI	SN74LS365	
74LS366	Fairchild	74LS366	
	ITT	ITT74LS366	
	Motorola	SN74LS366	
	National	DM74LS366	
	NEC America	μPB74LS366	
	Raytheon	**74LS366**	**286**
	TI	SN74LS366	
74LS367	Fairchild	74LS367	
	ITT	ITT74LS367	
	Motorola	SN74LS367	
	National	DM74LS367	
	NEC America	μPB74LS367	
	Raytheon	**74LS367**	**286**
	TI	SN74LS367	
74LS368	Fairchild	74LS368	
	ITT	ITT74LS368	
	Motorola	SN74LS368	
	National	DM74LS368	
	NEC America	μPB74LS368	
	Raytheon	**74LS368**	**286**
74LS368	TI	SN74LS368	
74LS37	Fairchild	74LS37	
	ITT	ITT74LS37	
	Motorola	SN74LS37	
	National	DM74LS37	
	NEC America	μPB74LS37	
	Raytheon	74LS37	
	TI	SN74LS37	
74LS373	AMD	SN74LS373	
	Fairchild	74LS373	
	ITT	ITT74LS373	
	MMI	74LS373	
	Raytheon	**74LS373**	**288**
	TI	SN74LS373	
74LS375	ITT	ITT74LS375	
	Motorola	SN74LS375	
	NEC America	μPB74LS375	
	Raytheon	74LS375	
	TI	SN74LS375	
74LS377	AMD	SN74LS377	
	Fairchild	74LS377	
	ITT	ITT74LS377	
	Raytheon	**74LS377**	**288**
	TI	SN74LS377	
74LS378	AMD	SN74LS378	
	Fairchild	74LS378	
	ITT	ITT74LS378	
	TI	SN74LS378	
74LS38	Fairchild	74LS38	
	ITT	ITT74LS38	
	Motorola	SN74LS38	
	National	DM74LS38	
	NEC America	μPB74LS38	
	Raytheon	74LS38	
	TI	SN74LS38	
74LS386	Fairchild	74LS386	
	ITT	ITT74LS386	
	Motorola	SN74LS386	
	National	DM74LS386	
	Raytheon	74LS386	
	~~TI~~	~~SN74LS386~~	
74LS395	Fairchild	74LS395	
	National	DM74LS395	
	Raytheon	**74LS395**	**291**
	TI	SN74LS395	
74LS40	Fairchild	74LS40	
	ITT	ITT74LS40	
	Motorola	SN74LS40	
	National	DM74LS40	
	NEC America	μPB74LS40	
	Raytheon	74LS40	
	TI	SN74LS40	
74LS42	Fairchild	74LS42	
	ITT	ITT74LS42	
	Motorola	SN74LS42	
	National	DM74LS42	
	NEC America	μPB74LS42	
	Raytheon	**74LS42**	**266**
	TI	SN74LS42	
74LS51	Fairchild	74LS51	
	ITT	ITT74LS51	
	Motorola	SN74LS51	
	National	DM74LS51	
	NEC America	μPB74LS51	
	Raytheon	74LS51	
	TI	SN74LS51	
74LS54	Fairchild	74LS54	
	ITT	ITT74LS54	
	Motorola	SN74LS54	
	National	DM74LS54	
	NEC America	μPB74LS54	
	Raytheon	74LS54	
	TI	SN74LS54	
74LS55	Fairchild	74LS55	
	Motorola	SN74LS55	
	National	DM74LS55	
	NEC America	μPB74LS55	
	Raytheon	74LS55	
	TI	SN74LS55	
74LS670	AMD	SN74LS670	
	Fairchild	74LS670	
	Motorola	SN74LS670	
	National	DM74LS670	
	Raytheon	74LS670	
	TI	SN74LS670	
74LS73	Fairchild	74LS73	
74LS73	ITT	ITT74LS73	
	Motorola	SN74LS73	
	National	DM74LS73	
	Raytheon	74LS73	
	TI	SN74LS73	
74LS74	Fairchild	74LS74	
	ITT	ITT74LS74	
	Motorola	SN74LS74	
	National	DM74LS74	
	NEC America	μPB74LS74	
	Raytheon	74LS74	
	TI	SN74LS74	
74LS75	Fairchild	74LS75	
	ITT	ITT74LS75	
	National	DM74LS75	
	Raytheon	74LS75	
	TI	SN74LS75	
74LS76	ITT	ITT74LS76	
	National	DM74LS76	
	Raytheon	74LS76	
	TI	SN74LS76	
74LS78	ITT	ITT74LS78	
	National	DM74LS78	
	Raytheon	74LS78	
	TI	SN74LS78	
74LS83	Fairchild	74LS83	
	ITT	ITT74LS83A	
	Motorola	SN74LS83	
	National	DM74LS83	
		DM74LS83A	
	Raytheon	74LS83	
		74LS83A	
	TI	SN74LS83A	
74LS85	Fairchild	74LS85	
	ITT	ITT74LS85	
	Motorola	SN74LS85	
	National	DM74LS85	
	Raytheon	74LS85	
	TI	SN74LS85	
74LS86	Fairchild	74LS86	
	ITT	ITT74LS86	
	Motorola	SN74LS86	
	NEC America	μPB74LS86	
	Raytheon	74LS86	
	TI	SN74LS86	
74LS90	Fairchild	74LS90	
	ITT	ITT74LS90	
	Motorola	SN74LS90	
	Raytheon	**74LS90**	**268**
	TI	SN74LS90	
74LS92	Fairchild	74LS92	
	Motorola	SN74LS92	
	Raytheon	**74LS92**	**268**
	TI	SN74LS92	
74LS93	Fairchild	74LS93	
	ITT	ITT74LS93	
	Motorola	SN74LS93	
	Raytheon	**74LS93**	**268**
	TI	SN74LS93	
74LS95B	Fairchild	74LS95	
	ITT	ITT74LS95B	
	Motorola	SN74LS95	
	Raytheon	74LS95B	
	TI	SN74LS95B	
74LS96	TI	SN74LS96	
74S00	Fairchild	74S00	
		9S00	
	Hitachi	HD74S00	
	Mitsubishi	M5S000	
	National	DM74S00	
	TI	SN74S00	
74S02	Fairchild	74S02	
	National	DM74S02	
	TI	SN74S32	
74S03	Fairchild	74S03	
	Hitachi	HD74S03	
	Mitsubishi	M5S003	
	National	DM74S03	
	TI	SN74S03	
74S04	Fairchild	74S04	
	Hitachi	HD74S04	
	Mitsubishi	M5S004	
	National	DM74S04	
	TI	SN74S04	
74S05	Fairchild	74S05	
	Hitachi	HD74S05	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
74S05	Mitsubishi	M5S005	
	National	DM74S05	
	TI	SN74S05	
74S08	Fairchild	74S08	
	TI	SN74S08	
74S09	Fairchild	74S09	
	Signetics	74S09	
	TI	SN74S09	
74S10	Fairchild	74S10	
	Hitachi	HD74S10	
	Mitsubishi	M5S010	
	National	DM74S10	
	TI	SN74S10	
74S11	Fairchild	74S11	
	Hitachi	HD74S11	
	Mitsubishi	M5S011	
	National	DM74S11	
	TI	SN74S11	
74S112	Fairchild	74S112	
	Hitachi	HD74S112	
	Mitsubishi	M5S112	
	Motorola	SN74S112	
	National	DM74S112	
	TI	SN74S112	
74S113	Fairchild	74S113	
	Hitachi	HD74S113	
	Mitsubishi	M5S113	
	Motorola	SN74S113	
	National	DM74S113	
	TI	SN74S113	
74S114	Fairchild	74S114	
	Hitachi	HD74S114	
	Mitsubishi	M5S114	
	National	DM74S114	
	TI	SN74S114	
74S133	Fairchild	74S133	
	Hitachi	HD74S133	
	Mitsubishi	M5S133	
	National	DM74S133	
	TI	SN74S133	
74S134	Fairchild	74S134	
	Hitachi	HD74S134	
	National	DM74S134	
	TI	SN74S134	
74S135	Fairchild	74S135	
	Hitachi	HD74S135	
	National	DM74S135	
	TI	SN74S135	
74S138	AMD	SN74S138	
	Fairchild	74S138	
	Mitsubishi	M5S138	
	National	DM74S138	
	TI	SN74S138	
74S139	AMD	SN74S139	
	Fairchild	74S139	
	National	DM74S139	
	TI	SN74S139	
74S140	Fairchild	74S140	
	Hitachi	HD74S140	
	National	DM74S140	
	TI	SN74S140	
74S15	Fairchild	74S15	
	Hitachi	HD74S15	
	Mitsubishi	M5S015	
	National	DM74S15	
	TI	SN74S15	
74S151	AMD	SN74S151	
	Fairchild	74S151	
	Hitachi	HD74S151	
	Mitsubishi	M5S151	
	National	DM74S151	
	TI	SN74S151	
74S153	AMD	SN74S153	
	Fairchild	74S153	
	Mitsubishi	M5S153	
	National	DM74S153	
	TI	SN74S153	
74S157	AMD	SN74S157	
	Fairchild	74S157	
	Mitsubishi	M5S157	
	National	DM74S157	
	TI	SN74S157	
74S158	AMD	SN74S158	
74S158	Fairchild	74S158	
	Mitsubishi	M5S158	
	National	DM74S158	
	TI	SN74S158	
74S174	AMD	SN74S174	
	Fairchild	74S174	
	Hitachi	HD74S174	
	Mitsubishi	M5S174	
	National	DM74S174	
	TI	SN74S174	
74S175	AMD	SN74S175	
	Fairchild	74S175	
	Hitachi	HD74S175	
	Mitsubishi	M5S175	
	National	DM74S175	
	TI	SN74S175	
74S181	AMD	SN74S181	
	Fairchild	74S181	
	Hitachi	HD74S181	
	Mitsubishi	M5S181	
	TI	SN74S181	
74S182	Fairchild	74S182	
	Mitsubishi	M5S182	
	National	DM74S182	
	TI	SN74S182	
74S194	AMD	SN74S194	
	Fairchild	74S194	
	TI	SN74S194	
♦74S195	AMD	SN74S195	
	Fairchild	74S195	
	TI	SN74S195	
74S196	TI	SN74S196	
74S197	TI	SN74S197	
74S20	Fairchild	74S20	
	Hitachi	HD74S20	
	Mitsubishi	M5S020	
	National	DM74S20	
	TI	SN74S20	
74S200	National	DM74S200	
	NEC Micro	μPB2200	
74S201	MMI	6531	
	NEC Micro	μPB2202	
	TI	SN74S201	
74S22	Fairchild	74S22	
	Hitachi	HD74S22	
	Mitsubishi	M5S22	
	National	DM74S22	
	TI	SN74S22	
74S251	AMD	SN74S251	
	Fairchild	74S251	
	Hitachi	HD74S251	
	Mitsubishi	M5S251	
	National	DM74S251	
	TI	SN74S251	
74S253	AMD	SN74S253	
	Fairchild	74S253	
	National	DM74S253	
74S257	AMD	SN74S257	
	Fairchild	74S257	
	Mitsubishi	M5S257	
	National	DM74S257	
	TI	SN74S257	
74S258	AMD	SN74S258	
	Fairchild	74S258	
	Mitsubishi	M5S258	
	TI	SN74S258	
74S280	National	DM74S280	
	TI	SN74S280	
74S32	Fairchild	74S32	
74S37	TI	SN74S37	
74S40	Fairchild	74S40	
	Hitachi	HD74S40	
	Mitsubishi	M5S040	
	National	DM74S40	
	TI	SN74S40	
74S51	Fairchild	74S51	
	Mitsubishi	M5S051	
	National	DM74S51	
	TI	SN74S51	
74S64	Fairchild	74S64	
	Hitachi	HD74S64	
	National	DM74S64	
	TI	SN74S64	
74S65	Fairchild	74S65	
	Hitachi	HD74S65	
	National	DM74S65	
74S65	TI	SN74S65	
74S85	Mitsubishi	M5S085	
	TI	SN74S85	
74S86	Fairchild	74S86	
	Hitachi	HD74S86	
	National	DM74S86	
	TI	SN74S86	
74S89	NEC Micro	μPB2089	
7400	Fairchild	7400	
		9N00	
	Hitachi	HD2503	
		HD7400	
	ITT	ITT7400	
	Mitsubishi	M53200	
	Motorola	MC7400	
	National	DM7400	
	NEC America	μPB7400	
	Raytheon	7400	
	TI	SN7400	
	Toshiba	TC7400	
	TRW	7400	
7401	Fairchild	7401	
	Hitachi	HD2509	
	ITT	ITT7401	
	Mitsubishi	M53201	
	Motorola	MC7401	
	National	DM7401	
	Raytheon	7401	
	TI	SN7401	
	TRW	7401	
7402	Fairchild	7402	
	Hitachi	HD2511	
		HD7402	
	ITT	ITT7402	
	Mitsubishi	M53202	
	Motorola	MC7402	
	National	DM7402	
	NEC America	μPB7402	
	TI	SN7402	
	TRW	7402	
7403	Fairchild	7403	
	Hitachi	HD2528	
		HD7403	
	ITT	ITT7403	
	Mitsubishi	M53203	
	Motorola	MC7403	
	National	DM7403	
	Raytheon	7403	
	TI	SN7403	
	TRW	7403	
7404	Fairchild	7404	
	Hitachi	HD2522	
		HD7404	
	ITT	ITT7404	
	Mitsubishi	M53204	
	Motorola	MC7404	
	National	DM7404	
	NEC America	μPB7404	
	Raytheon	7404	
	TI	SN7404	
	Toshiba	TC7404	
	TRW	7404	
7405	Fairchild	7405	
	Hitachi	HD2523	
		HD7405	
	ITT	ITT7405	
	Mitsubishi	M53205	
	Motorola	MC7405	
	National	DM7405	
	NEC America	μPB7405	
	Raytheon	7405	
	TI	SN7405	
	TRW	7405	
7406	Fairchild	7406	
	Hitachi	HD7406	
	ITT	ITT7406	
	Mitsubishi	M53206	
	Motorola	MC7406	
	National	DM7406	
	TI	SN7406	
	TRW	7406	
7407	Fairchild	7407	
	Hitachi	HD7407	
	ITT	ITT7407	
	Mitsubishi	M53207	
	Motorola	MC7407	
7407	National	DM7407	
	TI	SN7407	
	TRW	7407	
7408	Fairchild	7408	
	Hitachi	HD2550	
	ITT	ITT7408	
	Mitsubishi	M53208	
	Motorola	MC7408	
	National	DM7408	
	Raytheon	7408	
	TI	SN7408	
	Toshiba	TC7408	
	TRW	7408	
7409	Fairchild	7409	
	Hitachi	HD7409	
	ITT	ITT7409	
	Mitsubishi	M53209	
	Motorola	MC7409	
	National	DM7409	
	Raytheon	7409	
	TI	SN7409	
	TRW	7409	
7410	Fairchild	7410	
	Hitachi	HD2507	
		HD7410	
	ITT	ITT7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
	National	DM7410	
	NEC America	μPB7410	
	Raytheon	7410	
	TI	SN7410	
		SN7427	
	Toshiba	TC7410	
	TRW	7410	
74100	Motorola	MC74100	
	TI	SN74100	
74107	Fairchild	74107	
	Hitachi	HD2530	
		HD74107	
	ITT	ITT74107	
	Mitsubishi	M53307	
	Motorola	MC74107	
	National	DM74107	
	NEC America	μPB74107	
	TI	SN74107	
74109	Fairchild	74109	
	National	DM74109	
	TI	SN74109	
7411	Fairchild	7411	
	Hitachi	HD7411	
	ITT	ITT7411	
	National	DM7411	
	Raytheon	7411	
74116	Fairchild	74116	
	TI	SN74116	
♦7412	Fairchild	7412	
	Hitachi	HD7412	
	ITT	ITT7412	
	Raytheon	7412	
	TI	SN7412	
	TRW	7412	
74121	Fairchild	74121	
	Hitachi	HD74121	
	ITT	ITT74121	
	Mitsubishi	M53321	
	Motorola	MC74121	
	National	DM74121	
	TI	SN74121	
	TRW	74121	
74122	Fairchild	74122	
	ITT	ITT74122	
	Mitsubishi	M53322	
	Motorola	MC74122	
	TI	SN74122	
74123	AMD	SN74123	
	Fairchild	74123	
	ITT	ITT74123	
	Mitsubishi	M53323	
	Motorola	MC74123	
	National	DM74123	
	NEC America	μPB74123	
	Raytheon	74123	
	TI	SN74123	
	TRW	74123	
74125	Fairchild	74125	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
74125	Hitachi	HD74125	
	Mitsubishi	M53325	
	National	DM74125	
	TI	SN74125	
74126	Fairchild	74126	
	Hitachi	HD74126	
	Mitsubishi	M53326	
	National	DM74126	
	TI	SN74126	
74128	TI	SN74128	
7413	Fairchild	7413	
	ITT	ITT7413	
	Mitsubishi	M53213	
	Motorola	MC7413	
	National	DM7413	
	NEC America	μPB7413	
	TI	SN7413	
	TRW	7413	
74132	Fairchild	74132	
	Hitachi	HD74132	
	Mitsubishi	M53332	
	Motorola	MC74132	
	National	DM74132	
	TI	SN74132	
♦74136	Raytheon	74136	
7414	Fairchild	7414	
	Hitachi	HD7414	
	Mitsubishi	M53214	
	Motorola	MC7414	
	National	DM7414	
	TI	SN7414	
74145	Fairchild	74145	
	ITT	ITT74145	
	Mitsubishi	M53345	
	Motorola	MC74145	
	National	DM74145	
	Raytheon	74145	
	TI	SN74145	
	TRW	74145	
74147	Hitachi	HD74147	
	Mitsubishi	M53347	
	National	DM74147	
	NEC America	μPB74147	
	TI	SN74147	
74148	Hitachi	HD74148	
	Mitsubishi	M53348	
	National	DM74148	
	NEC America	μPB74148	
	TI	SN74148	
♦7415	Raytheon	7415	
74150	Fairchild	74150	
	Hitachi	HD74150	
	Mitsubishi	M53350	
	Motorola	MC74150	
	National	DM74150	
	NEC America	μPB74150	
	Raytheon	74150	
	TI	SN74150	
	TRW	74150	
74151	Fairchild	74151	
	Hitachi	HD74151	
	ITT	ITT74151	
	Mitsubishi	M53351	
	Motorola	MC74151	
	National	DM74151	
	NEC America	μPB74151	
	Raytheon	74151	
	TI	SN74151	
	TRW	74151	
74152	Raytheon	74152	
74153	Fairchild	74153	
	ITT	ITT74153	
	Mitsubishi	M53353	
	Motorola	MC74153	
	National	DM74153	
	NEC America	μPB74153	
	Raytheon	74153	
	TI	SN74153	
	TRW	74153	
74154	AMD	SN74154	
	Fairchild	74154	
	Mitsubishi	M53354	
	Motorola	MC74154	
74154	National	DM74154	
	NEC America	μPB74154	
	Raytheon	74154	
	TI	SN74154	
	TRW	74154	
74155	Fairchild	74155	
	ITT	ITT74155	
	Mitsubishi	M53355	
	Motorola	MC74155	
	National	DM74155	
	NEC America	μPB74155	
	Raytheon	74155	
	TI	SN74155	
	TRW	74155	
74156	Fairchild	74156	
	Hitachi	HD74156	
	ITT	ITT74156	
	Mitsubishi	M53356	
	Motorola	MC74156	
	National	DM74156	
	NEC America	μPB74156	
	Raytheon	74156	
	TI	SN74156	
	TRW	74156	
74157	AMD	SN74157	
	Fairchild	74157	
	Hitachi	HD74157	
	ITT	ITT74157	
	Mitsubishi	M53357	
	Motorola	MC74157	
	National	DM74157	
	NEC America	μPB74157	
	Raytheon	74157	
	TI	SN74157	
74158	Mitsubishi	M53358	
	Raytheon	74158	
♦74159	Raytheon	74159	
7416	Fairchild	7416	
	Hitachi	HD7416	
	ITT	ITT7416	
	Mitsubishi	M53216	
	Motorola	MC7416	
	National	DM7416	
	TI	SN7416	
	TRW	7416	
74160	AMD	SN74160	
	Fairchild	74160	
	Hitachi	HD74160	
	ITT	ITT74160	
	Mitsubishi	M53360	
	Motorola	MC74160	
	National	DM74160	
	Raytheon	74160	
	TI	SN74160	
	TRW	74160	
74161	AMD	SN74161	
	Fairchild	74161	
	Hitachi	HD74161	
	ITT	ITT74161	
	Mitsubishi	M53361	
	Motorola	MC74161	
	National	DM74161	
	NEC America	μPB74161	
	Raytheon	74161	
	TI	SN74161	
	TRW	74161	
74162	AMD	SN74162	
	Fairchild	74162	
	Hitachi	HD74162	
	ITT	ITT74162	
	Mitsubishi	M53362	
	Motorola	MC74162	
	National	DM74162	
	Raytheon	74162	
	TI	SN74162	
	TRW	74162	
74163	AMD	SN74163	
	Fairchild	74163	
	Hitachi	HD74163	
	ITT	ITT74163	
	Mitsubishi	M53363	
	Motorola	MC74163	
	National	DM74163	
	Raytheon	74163	
	TI	SN74163	
	TRW	74163	
74164	AMD	74164	
	Fairchild	74164	
	Hitachi	HD74164	
	ITT	ITT74164	
	Mitsubishi	M53364	
	National	DM74164	
	NEC America	μPB74164	
	Raytheon	74164	
	TI	SN74164	
74165	Fairchild	74165	
	Mitsubishi	M53365	
	Motorola	MC74165	
	National	DM74165	
	Raytheon	74165	
	TI	SN74165	
74166	Fairchild	74166	
	Hitachi	HD74166	
	Mitsubishi	M53366	
	National	DM74166	
	Raytheon	74166	
	TI	SN74166	
7417	Fairchild	7417	
	Hitachi	HD7417	
	ITT	ITT7417	
	Mitsubishi	M53217	
	Motorola	MC7417	
	National	DM7417	
	TI	SN7417	
	TRW	7417	
74170	Fairchild	74170	
	Mitsubishi	M53370	
	National	DM74170	
	NEC America	μPB74170	
	Raytheon	74170	
	TI	SN74170	
74172	TI	SN74172	
74174	AMD	SN74174	
	Fairchild	74174	
	Hitachi	HD74174	
	Mitsubishi	M53374	
	Motorola	MC74174	
	National	DM74174	
	Raytheon	74174	
	TI	SN74174	
74175	AMD	SN74175	
	Fairchild	74175	
	Hitachi	HD74175	
	Mitsubishi	M53375	
	Motorola	MC74175	
	National	DM74175	
	NEC America	μPB74175	
	Raytheon	74175	
	TI	SN74175	
74176	Fairchild	74176	
	Mitsubishi	M53376	
	Motorola	MC74176	
	National	DM74176	
	TI	SN74176	
74177	Fairchild	74177	
	Mitsubishi	M53377	
	Motorola	MC74177	
	National	DM74177	
	TI	SN74177	
74180	Fairchild	74180	
	Hitachi	HD74180	
	ITT	ITT74180	
	Mitsubishi	M53380	
	Motorola	MC74180	
	National	DM74180	
	NEC America	μPB74180	
	Raytheon	74180	
	TI	SN74180	
	TRW	74180	
74181	AMD	SN74181	
	Fairchild	74181	
	Mitsubishi	M53381	
	Motorola	MC74181	
	National	DM74181	
	NEC America	μPB74181	
	Raytheon	74181	
	TI	SN74181	
74182	AMD	SN74182	
	Fairchild	74182	
	ITT	ITT74182	
	Mitsubishi	M53382	
	Motorola	MC74182	
74182	National	DM74182	
	NEC America	μPB74182	
	Raytheon	74182	
	TI	SN74182	
74190	Fairchild	74190	
	Hitachi	HD74190	
	ITT	ITT74190	
	Mitsubishi	M53390	
	Motorola	MC74190	
	National	DM74190	
	Raytheon	74190	
	TI	SN74190	
74191	Fairchild	74191	
	Hitachi	HD74191	
	ITT	ITT74191	
	Mitsubishi	M53391	
	Motorola	MC74191	
	National	DM74191	
	Raytheon	74191	
	TI	SN74191	
74192	AMD	SN74192	
	Fairchild	74192	
	ITT	ITT74192	
	Mitsubishi	M53392	
	Motorola	MC74192	
	National	DM74192	
	NEC America	μPB74192	
	Raytheon	74192	
	TI	SN74192	
74193	AMD	SN74193	
	Fairchild	74193	
	ITT	ITT74193	
	Mitsubishi	M53393	
	Motorola	MC74193	
	National	DM74193	
	NEC America	μPB74193	
	Raytheon	74193	
	TI	SN74193	
74194	AMD	SN74194	
	Fairchild	74194	
	Hitachi	HD74194	
	ITT	ITT74194	
	Motorola	MC74194	
	National	DM74194	
	Raytheon	74194	
	TI	SN74194	
74195	AMD	SN74195	
	Fairchild	74195	
	ITT	ITT74195	
	Motorola	MC74195	
	National	DM74195	
	NEC America	μPB74195	
	Raytheon	74195	
	TI	SN74195	
74196	Fairchild	74196	
	Motorola	MC74196	
	National	DM74196	
	TI	SN74196	
74197	Fairchild	74197	
	Motorola	MC74197	
	National	DM74197	
	TI	SN74197	
74198	Fairchild	74198	
	Hitachi	HD74198	
	Mitsubishi	M53398	
	National	DM74198	
	NEC America	μPB74198	
	Raytheon	74198	
	TI	SN74198	
74199	Fairchild	74199	
	Mitsubishi	M53399	
	National	DM74199	
	Raytheon	74199	
	TI	SN74199	
7420	Fairchild	7420	
	Hitachi	HD2504	
		HD7420	
	ITT	ITT7420	
	Mitsubishi	M53220	
	Motorola	MC7420	
	National	DM7420	
	NEC America	μPB7420	
	Raytheon	7420	
	TI	SN7420	
	Toshiba	TC7420	
	TRW	7420	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
7421	Fairchild	7421	
	ITT	ITT7421	
	Raytheon	7421	
♦7422	Raytheon	7422	
74221	TI	SN74221	
7426	Fairchild	7426	
	Hitachi	HD7426	
	ITT	ITT7426	
	Motorola	MC7426	
	National	DM7426	
	TI	SN7426	
	TRW	7426	
7427	Fairchild	7427	
	Hitachi	HD7427	
	Mitsubishi	M53227	
	Motorola	MC7427	
	National	DM7427	
74279	Fairchild	74279	
	TI	SN74279	
7428	TI	SN7428	
♦74283	Raytheon	74283	
74298	Fairchild	74298	
	Motorola	MC74298	
	TI	SN74298	
7430	Fairchild	7430	
	Hitachi	HD2508	
		HD7430	
	ITT	ITT7430	
	Mitsubishi	M53230	
	Motorola	MC7430	
	National	DM7430	
	NEC America	μPB7430	
	TI	SN7430	
	TRW	7430	
7432	Fairchild	7432	
	Hitachi	HD7432	
	ITT	ITT7432	
	National	DM7432	
	TI	SN7432	
7433	TI	SN7433	
7437	Fairchild	7437	
	ITT	ITT7437	
	Mitsubishi	M53237	
	Motorola	MC7437	
	National	DM7437	
	NEC America	μPB7437	
	Raytheon	7437	
	TI	SN7437	
	TRW	7437	
7438	Fairchild	7438	
	ITT	ITT7438	
	Mitsubishi	M53238	
	Motorola	MC7438	
	National	DM7438	
	NEC America	μPB7438	
	Raytheon	7438	
	TI	SN7438	
	TRW	7438	
7439	Fairchild	7439	
7440	Fairchild	7440	
	Hitachi	HD2501	
		HD7440	
	ITT	ITT7440	
	Mitsubishi	M53240	
	Motorola	MC7440	
	National	DM7440	
	NEC America	μPB7440	
	TI	SN7440	
	TRW	7440	
♦7441	Hitachi	HD2518	
	TI	SN74141	
7442	Fairchild	7442	
	Hitachi	HD7442	
	ITT	ITT7442	
	Mitsubishi	M53242	
	Motorola	MC7442	
	National	DM7442	
	NEC America	μPB7442	
	Raytheon	7442	
	TI	SN7442	
7443	Fairchild	7443	
	Hitachi	HD7443	
	ITT	ITT7443	
7443	Mitsubishi	M53243	
	Motorola	MC7443	
	Raytheon	7443	
	TI	SN7443	
7444	Fairchild	7444	
	Hitachi	HD7444	
	ITT	ITT7444	
	Mitsubishi	M53244	
	Motorola	MC7444	
	Raytheon	7444	
	TI	SN7444	
7445	Fairchild	7445	
	ITT	ITT7445	
	Mitsubishi	M53245	
	Motorola	MC7445	
	National	DM7445	
	NEC America	μPB7445	
	Raytheon	7445	
	TI	SN7445	
	TRW	7445	
7446	Fairchild	7446	
	ITT	ITT7446	
	Motorola	MC7446	
	National	DM7446	
	TI	SN7446	
7447	Fairchild	7447	
	ITT	ITT7447	
	Mitsubishi	M53247	
	Motorola	MC7447	
	National	DM7447	
	NEC America	μPB7447	
	TI	SN7447	
7448	Fairchild	7448	
	ITT	ITT7448	
	Mitsubishi	M53248	
	Motorola	MC7448	
	National	DM7448	
	TI	SN7448	
7450	Fairchild	7450	
	Hitachi	HD7450	
	ITT	ITT7450	
	Mitsubishi	M53250	
	Motorola	MC7450	
	National	DM7450	
	NEC America	μPB7450	
	TI	SN7450	
	TRW	7450	
7451	Fairchild	7451	
	Hitachi	HD2505	
		HD7451	
	ITT	ITT7451	
	Motorola	MC7451	
	National	DM7451	
	NEC America	μPB7451	
	TI	SN7451	
	TRW	7451	
7453	Fairchild	7453	
	Hitachi	HD2512	
		HD7453	
	ITT	ITT7453	
	Mitsubishi	M53253	
	Motorola	MC7453	
	National	DM7453	
	NEC America	μPB7453	
	TI	SN7453	
	TRW	7453	
7454	Fairchild	7454	
	Hitachi	HD2514	
		HD7454	
	ITT	ITT7454	
	Motorola	MC7454	
	National	DM7454	
	NEC America	μPB7454	
	TI	SN7454	
	TRW	7454	
7460	Fairchild	7460	
	Hitachi	HD2502	
		HD7460	
	Mitsubishi	M53260	
	Motorola	MC7460	
	National	DM7460	
	NEC America	μPB7460	
	TI	SN7460	
	TRW	7460	
7470	Fairchild	7470	
	Hitachi	HD2539	
7470	ITT	ITT7470	
	Mitsubishi	M53270	
	Motorola	MC7470	
	National	DM7470	
	TI	SN7470	
7472	Fairchild	7472	
	Hitachi	HD2520	
		HD7472	
	ITT	ITT7472	
	Mitsubishi	M53272	
	Motorola	MC7472	
	National	DM7472	
	TI	SN7472	
	TRW	7472	
7473	Fairchild	7473	
	Hitachi	HD2515	
	ITT	ITT7473	
	Mitsubishi	M53273	
	Motorola	MC7473	
	National	DM7473	
	NEC America	μPB7473	
	TI	SN7473	
7474	Fairchild	7474	
	Hitachi	HD2510	
		HD7474	
	ITT	ITT7474	
	Mitsubishi	M53274	
	Motorola	MC7474	
	National	DM7474	
	NEC America	μPB7474	
	Raytheon	7474	
	TI	SN7474	
	TRW	7474	
7475	Fairchild	7475	
	Hitachi	HD2517	
		HD7475	
	ITT	ITT7475	
	Mitsubishi	M53275	
	Motorola	MC7475	
	National	DM7475	
	TI	SN7475	
	TRW	7475	
7476	Fairchild	7476	
	Hitachi	HD2516	
	ITT	ITT7476	
	Mitsubishi	M53276	
	Motorola	MC7476	
	National	DM7476	
	NEC America	μPB7476	
	TI	SN7476	
	TRW	7476	
7477	Fairchild	7477	
	Motorola	MC7477	
	TI	SN7477	
7480	Fairchild	7480	
	ITT	ITT7480	
	Mitsubishi	M53280	
	Motorola	MC7480	
	NEC America	μPB7480	
	TI	SN7480	
7483	Fairchild	7483	
	ITT	ITT7483	
	Mitsubishi	M53283	
	Motorola	MC7483	
	National	DM7483	
	Raytheon	7483	
	TI	SN7483	
7485	Fairchild	7485	
	Hitachi	HD7485	
	Mitsubishi	M53285	
	Motorola	MC7485	
	National	DM7485	
	NEC America	μPB7485	
	TI	SN7485	
	TRW	7485	
7486	Fairchild	7486	
	Hitachi	HD7486	
	ITT	ITT7486	
	Mitsubishi	M53286	
	Motorola	MC7486	
	National	DM7486	
	NEC America	μPB7486	
	Raytheon	7486	
	TI	SN7486	
	TRW	7486	
7488	TI	SN7488A	
7489	Hitachi	HD2502	
	Raytheon	7489	
	TI	SN7489	
7490	Fairchild	7490	
	Hitachi	HD2519	
		HD7490	
	ITT	ITT7490	
	Mitsubishi	M53290	
	Motorola	MC7490	
	National	DM7490	
	TI	SN7490	
		SN7490A	
	TRW	7490	
7491	Fairchild	7491	
	Hitachi	HD2524	
	ITT	ITT7491	
	Mitsubishi	M53291	
	Motorola	MC7491	
	National	DM7491	
	NEC America	μPB7491	
	TI	SN7491	
		SN7491A	
7492	Fairchild	7492	
	Hitachi	HD2521	
		HD7492	
	ITT	ITT7492	
	Mitsubishi	M53292	
	Motorola	MC7492	
	National	DM7492	
	TI	SN7492	
		SN7492A	
	TRW	7492	
7493	Fairchild	7493	
	Hitachi	HD2520	
		HD7493	
	ITT	ITT7493	
	Mitsubishi	M53293	
	Motorola	MC7493	
	National	DM7493	
	TI	SN7493	
		SN7493A	
	TRW	7493	
7494	Hitachi	HD2533	
	TI	SN7494	
7495	Fairchild	7495	
	Hitachi	HD2534	
	ITT	ITT7495	
	Mitsubishi	M53295	
	Motorola	MC7495	
	National	DM7495	
	TI	SN7495	
		SN7495A	
7496	Fairchild	7496	
	Hitachi	HD2546	
		HD7496	
	ITT	ITT7496	
	Mitsubishi	M53296	
	Motorola	MC7496	
	National	DM7496	
	TI	SN7496	
	TRW	7496	
75S107	TI	SN75S107	
75S108	TI	SN75S108	
75107	AMD	SN75107	
	National	**DS75107**	**504**
	Raytheon	RC75107	
	TI	SN75107	
75108	AMD	SN75108	
	National	**DS75108**	**504**
	Raytheon	RC75108	
	TI	SN75108	
7520	AMD	SN7520	
	ITT	ITT7520	
	Motorola	MC7520	
	National	DS7520	
	Silicon G	SG7520	
	TI	SN7520	
♦7521	AMD	SN7521	
	Motorola	MC7521	
	National	DS7521	
	Silicon G	SG7521	
	TI	SN7520	
7522	ITT	ITT7522	
	Motorola	MC7522	
	National	DS7522	
	Silicon G	SG7522	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
7522	TI	SN7522	
♦7523	Motorola	MC7523	
	National	DS7523	
	Silicon G	SG7523	
	TI	SN7522	
75232	TI	SN75232	
75234	TI	SN75234	
7524	AMD	SN7524	
	Fairchild	7524	
	ITT	ITT7524	
	Motorola	MC7524	
	National	DS7524	
	Silicon G	SG7524	
	TI	SN7524	
♦7525	Fairchild	7525	
	Motorola	MC7525	
		SN7525	
	National	DS7525	
	Silicon G	SG7525	
	TI	SN7524	
7526	TI	SN7526	
75325	TI	SN75325	
75450	Fairchild	75450	
	National	DS75450	
	Raytheon	RC75450	
	Silicon G	SG75450	
	TI	SN75450	
75451	Fairchild	75451	
	National	DS75451	
	Raytheon	RC75451	
	Silicon G	SG75451	
	TI	SN75451	
75452	TI	SN75452	
75453	TI	SN75453	
75454	TI	SN75454	
7550	Hitachi	HD2506	
82S115	Harris	HM7647	
~~82S123~~	~~Harris~~	~~HM5610~~	
	Intersil	IM5610	
	MMI	**6331**	**1252**
	National	**DM74S288**	**1262**
	TI	SN74S288	
82S126	**Fairchild**	**93417**	**1151**
	Harris	**HM7610**	**1192**
	Intel	3601	
	Intersil	IM5603A	
	MMI	**6300-1**	**1248**
	National	**DM74S387**	**1264**
	TI	SN74S387	
82S129	**Fairchild**	**93427**	**1151**
	Harris	**HM7611**	**1192**
	Intel	3621	
	Intersil	IM5623A	
	MMI	**6301-1**	**1248**
	National	**DM74S287**	**1264**
	TI	SN74S287	
82S130	**Fairchild**	**93436**	**1151**
	Harris	**HM7620**	**1192**
	Intel	3602	
	Intersil	IM5604	
	MMI	**6305-1**	**1248**
	National	**DM74S570**	**1266**
82S131	**Fairchild**	**93446**	**1151**
	Harris	**HM7621**	**1192**
	Intel	3622	
	Intersil	IM5624	
	MMI	**6306-1**	**1248**
	National	**DM74S571**	**1266**
82S136	**Fairchild**	**93452**	**1151**
	Harris	**HM7642**	**1192**
	Intel	3605	
	Intersil	IM56S06	
	MMI	**6352-1**	**1248**
	National	**DM74S572**	**1268**
	TI	SN74S477	
82S137	**Fairchild**	**93453**	**1151**
	Harris	**HM7643**	**1192**
	Intel	3625	
	Intersil	IM56S26	
	MMI	**6353-1**	**1248**
	National	**DM74S573**	**1268**
	TI	SN74S476	
82S140	**Fairchild**	**93438**	**1151**
82S140	**Harris**	**HM7640**	**1192**
	Intel	3604	
	Intersil	IM5606	
	MMI	**6340-1**	**1248**
	National	**DM87S295**	**1270**
	TI	SN74S475	
82S141	**Fairchild**	**93448**	**1151**
	Harris	**HM7641**	**1192**
	Intel	3624	
	Intersil	IM5625	
	MMI	**6341-1**	**1248**
	National	**DM87S296**	**1270**
	TI	SN74S474	
82S146	**MMI**	**6348**	**1252**
	National	**DM74S473**	**1272**
	TI	SN74S473	
82S147	**MMI**	**6349**	**1252**
	National	DM74S472	
	TI	SN74S472	
82S180	**Harris**	**HM7680**	**1220**
	Intel	3608	
	MMI	3680	
	National	DM85S229	
82S181	**Harris**	**HM7681**	**1220**
	Intel	3628	
	MMI	6381	
	National	DM85S228	
82S184	**Harris**	**HM7684**	**1242**
82S185	**Harris**	**HM7685**	**1242**
82S23	**Harris**	**HM7602**	**1192**
	Intersil	IM5600	
	MMI	**6330**	**1252**
	National	DM74S133	
	TI	SN74S133	
82S2508	MMI	6385	
82S2708	**Harris**	**HM7608**	**1235**
93410	Fairchild	93410	
	TI	SN54S301	
		SN74S301	

Silicon General

Manufacturer Device	Replacement Source	Device	IC Master Page
SG101	AMD	LM101	
	Intersil	LM101	
	Motorola	LM101	
	National	LM101	
	RCA	CA101	
		CA748	
	Signetics	LM101	
	TI	LM101	
SG102	Motorola	LM110	
SG104	Motorola	LM104	
	TI	LM104	
SG105	AMD	LM105	
	Intersil	LM105	
	Motorola	LM105	
	National	LM105	
	Raytheon	LM105	
	TI	LM105	
SG107	AMD	LM107	
	Intersil	LM107	
	Motorola	LM107	
	National	LM107	
	Raytheon	LM107	
	RCA	CA107	
	Signetics	LM107	
	TI	LM107	
SG108	AMD	LM108	
	Intersil	LM108	
	Motorola	LM108	
	National	LM108	
	Raytheon	LM108	
	RCA	CA108	
	Signetics	LM108	
SG109	Motorola	LM109	
	National	LM109	
	Raytheon	LM109	
	Signetics	LM109	
	TI	LM109	
SG110	AMD	LM110	
	Intersil	LM110	
	Motorola	LM110	
	National	LM110	
SG111	AMD	LM111	
	Intersil	LM111	
SG111	Motorola	LM111	
	National	LM111	
	Raytheon	LM111	
	RCA	CA111	
	TI	LM111	
SG124	Motorola	LM124	
SG139	Motorola	MLM139	
SG1436	Motorola	MC1436	
SG1456	Motorola	MC1456	
	TI	MC1456	
SG1458	Exar	XR1458	
	Harris	**HA-2655**	**704**
	Motorola	MC1458	
	PMI	**SSS1458**	**844**
	Raytheon	RC1458	
	RCA	CA1458	
	TI	MC1458	
SG1468	Motorola	MC1468	
SG1488	AMD	MC1488	
	Exar	XR1488	
	National	DS1488	
	Raytheon	RC1488	
	Signetics	MC1488	
SG1489	AMD	MC1489	
	Exar	XR1489	
	National	DS1489	
	Raytheon	RC1489	
	Signetics	MC1489	
SG1489A	Exar	XR1489	
	Signetics	MC1489A	
SG1495	Motorola	MC1495	
SG1496	Motorola	MC1496	
	Signetics	MC1496	
SG1501	Motorola	MC1568	
SG1524	Exar	XR1524	
	TI	SG1524	
SG1536	Motorola	MC1536	
SG1556	Motorola	MC1556	
	TI	MC1556	
SG1558	Exar	XR1558	
	~~Harris~~	~~HA-2650~~	~~704~~
	Motorola	MC1558	
	PMI	**SSS1558**	**844**
	Raytheon	RM1558	
	RCA	CA1558	
	TI	MC1558	
SG1595	Motorola	MC1595	
SG1596	Motorola	MC1596	
	Signetics	MC1496	
SG1741S	Motorola	SG1741S	
SG2001	Exar	XR2201	
	Fairchild	9665	
	SGS	L201	
	Signetics	NE5501	
		ULN2001	
	Sprague	ULN-2001	
	TI	ULN2001	
SG2002	Exar	XR2202	
	Fairchild	9666	
	SGS	L202	
	Signetics	NE5502	
		ULN2002	
	Sprague	ULN-2002	
	TI	ULN2002	
SG2003	Exar	XR2203	
	Fairchild	9667	
	SGS	L203	
	Signetics	NE5503	
		ULN2003	
	Sprague	ULN-2003	
	TI	ULN2003	
SG2004	Exar	XR2204	
	Fairchild	9668	
	Sprague	ULN-2004	
	TI	ULN2004	
SG201	AMD	LM201	
	Intersil	LM201	
	Motorola	LM201	
	National	LM201	
	RCA	CA201	
	Signetics	LM201	
	TI	LM201	
SG202	Motorola	LM210	
SG204	Motorola	LM204	
SG205	AMD	LM205	
	Intersil	LM205	
SG205	Motorola	LM205	
	National	LM205	
	Raytheon	LM205	
SG207	AMD	LM207	
	Intersil	LM207	
	Motorola	LM207	
	National	LM207	
	Raytheon	LM207	
	RCA	CA207	
	TI	LM207	
SG208	AMD	LM208	
	Intersil	LM208	
	Motorola	LM208	
	National	LM208	
	Raytheon	LM208	
	RCA	CA208	
SG209	Motorola	LM209	
	National	LM209	
	Signetics	LM209	
	TI	SG209	
SG210	AMD	LM210	
	Intersil	LM210	
	Motorola	LM210	
	National	LM210	
SG211	AMD	LM211	
	Intersil	LM211	
	Motorola	LM211	
	National	LM211	
	Raytheon	LM211	
	RCA	CA211	
	TI	LM211	
SG2206	Exar	XR2206	
SG224	Motorola	LM224	
SG239	RCA	CA239	
SG2501	Motorola	MC1468	
SG2524	Exar	XR2524	
	TI	SG2524	
SG301	AMD	LM301	
	Motorola	LM301	
	National	LM301	
	~~Raytheon~~	~~LM301~~	
	RCA	CA301	
	Signetics	LM301	
	TI	LM301	
SG302	Motorola	LM310	
SG304	Motorola	LM304	
	Raytheon	LM304	
	TI	LM304	
SG305	AMD	LM305	
	Motorola	LM305	
	National	LM305	
	Raytheon	LM305	
	TI	LM305	
SG3058	RCA	CA3058	
SG3059	RCA	CA3059	
SG307	AMD	LM307	
	Motorola	LM307	
	National	LM307	
	Raytheon	LM307	
	RCA	CA307	
	Signetics	LM307	
	TI	LM307	
SG3079	RCA	CA3079	
SG308	AMD	LM308	
	Motorola	LM308	
	National	LM308	
	Raytheon	LM308	
	RCA	CA308	
SG3081	RCA	CA3081	
SG3082	RCA	CA3082	
SG3083	RCA	CA3083	
	Signetics	CA3083	
SG3086	Motorola	MC3386	
SG309	Motorola	LM309	
	National	LM309	
	Raytheon	LM309	
	Signetics	LM309	
	TI	LM309	
SG310	Motorola	LM310	
	National	LM310	
SG311	AMD	LM311	
	Motorola	LM311	
	National	LM311	
	Raytheon	LM311	
	RCA	CA311	
	TI	LM311	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Silicon General (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
SG3183	Signetics	CA3183	
SG324	Motorola	LM324	
	RCA	CA324	
SG339	Motorola	LM339	
	RCA	CA339	
SG340	Motorola	LM324	
SG340-12	Motorola	MC7812	
SG340-15	Motorola	MC7815	
SG340-18	Motorola	MC7818	
SG340-24	Motorola	MC7824	
SG340-5	Motorola	MC7805	
SG340-6	Motorola	MC7806	
SG340-8	Motorola	MC7808	
SG3501	Motorola	MC1468	
	Raytheon	RC555	
		RM555	
	RCA	CA555	
SG3524	Exar	XR3524	
	TI	SG3524	
SG3851	Signetics	NE5501	
SG3852	Signetics	NE5502	
SG3853	Signetics	NE5503	
SG4250	National	LM4250	
SG4501	Motorola	MC1468	
SG555	Exar	XR555	
	Motorola	MC1455	
		MC1555	
	TI	NE555	
		SE555	
SG556	Exar	XR556	
	Motorola	MC3456	
		MC3556	
SG709	Motorola	MC1709	
	National	LM709	
	Raytheon	RM709	
	Signetics	µA709	
	TI	µA709	
SG710	Motorola	MC1710	
	National	LM710	
	Raytheon	RC710	
		RM710	
	Signetics	µA710	
	TI	µA710	
SG711	Motorola	MC1711	
	National	LM711	
	Raytheon	RC711	
		RM711	
	Signetics	µA711	
	TI	µA711	
SG723	AMD	723	
	Intersil	723	
	Motorola	MC1723	
	National	LM723	
	Raytheon	RC723	
		RM723	
	RCA	CA723	
	Signetics	µA723	
	TI	µA723	
SG733	AMD	733	
	Motorola	MC1733	
	Raytheon	RC733	
		RM733	
	Signetics	µA733	
	TI	µA733	
SG741	AMD	741	
	Motorola	MC1741	
	National	LM741	
	PMI	**SSS741**	**839**
	Raytheon	RC741	
		RM741	
	RCA	CA741	
	Signetics	µA741	
	TI	µA741	
SG747	AMD	747	
	Motorola	MC1747	
	National	LM747	
	PMI	**SSS747**	**844**
	Raytheon	RC747	
		RM747	
	RCA	CA747	
	TI	µA747	
SG748	AMD	748	
	Motorola	MC1748	
SG748	Raytheon	RC748	
		RM748	
	RCA	CA748	
	Signetics	µA748	
	TI	µA748	
SG7520	National	DS7520	
	Signetics	7520	
	TI	SN7520	
SG7521	National	DS7521	
SG7522	Motorola	MC7522	
	National	DS7522	
	Signetics	7522	
	TI	SN7522	
SG7523	Motorola	MC7523	
	National	DS7523	
SG7524	Motorola	MC7524	
	National	DS7524	
	Signetics	SN7524	
	TI	SN7524	
SG7525	Motorola	MC7525	
	National	DS7525	
SG7528	Motorola	MC7528	
	TI	SN7528	
SG7529	Motorola	MC7529	
SG7805	Motorola	MC7805	
SG7806	Motorola	MC7806	
SG7808	Motorola	MC7808	
SG7812	Motorola	MC7812	
SG7815	Motorola	MC7815	
SG7818	Motorola	MC7818	
SG7824	Motorola	MC7824	

Siliconix

Manufacturer Device	Replacement Source	Device	IC Master Page
DG126	Intersil	DG126	
	National	AH0126	
DG129	Intersil	DG129	
	National	AH0129	
DG133	Intersil	DG133	
	National	AH0133	
DG134	Intersil	DG134	
	National	AH0134	
DG139	Intersil	DG139	
	National	AH0139	
DG140	Intersil	DG140	
	National	AH0140	
DG142	Intersil	DG142	
	National	AH0142	
DG143	Intersil	DG143	
	National	AH0143	
DG144	Intersil	DG144	
	National	AH0144	
DG145	Intersil	DG145	
	National	AH0145	
DG146	Intersil	DG146	
	National	AH0146	
DG151	Intersil	DF151	
	National	AH0151	
DG153	Intersil	DG153	
	National	AH0153	
DG154	Intersil	DG154	
	National	AM0154	
DG163	Intersil	DG163	
	National	AM0163	
DG164	Intersil	DG164	
	National	AM0164	
DG180	Intersil	DG180	
DG181	Intersil	DG181	
	Siliconix	**DG381**	**530**
DG182	Intersil	DG182	
	TI	TL182	
DG183	Intersil	DG183	
DG184	Intersil	DG184	
	Siliconix	DG384	
DG185	Intersil	DG185	
	TI	TL185	
DG186	Intersil	DG186	
DG187	Intersil	DG187	
	Siliconix	**DG387**	**530**
DG188	Intersil	DG188	
	TI	TL188	
DG189	Intersil	DG189	
DG190	Intersil	DG190	
	Siliconix	**DG390**	**530**
DG191	Intersil	DG191	
DG191	TI	TL191	
DG200	AD	AD7513	
	Micro Power	MPS7513	
DG506	AD	AD7506	
	Harris	**HI506**	**418**
	Intersil	IH5060	
	Micro Power	MPS7506	
DG507	AD	AD7507	
	DDC	1507	
	Micro Power	MPS7507	
DG509	Harris	HI509A	
LD110	Intersil	LD110	
LD111	Intersil	LD111	
	Motorola	MC1405	
LD114	Intersil	LD114	
LM101	Motorola	LM101	
	RCA	CA101	
	TI	LM101	

Solid State Scientific

Manufacturer Device	Replacement Source	Device	IC Master Page
F40175	NEC America	µPD4175	
F4034	NEC America	µPD4034	
F4522	NEC America	µPD4522	
F4526	NEC America	µPD4526	
F4532	NEC America	µPD4532	
SCL4000	Mitel	SIL4000	
	Motorola	MC14000	
	National	CD4000	
	RCA	CD4000	
	Solitron	CM4000	
	TI	TP4000	
SCL4001	Fairchild	F4001	
	Mitel	SIL4001	
		SIL4901	
	Motorola	MC14001	
	National	CD4001	
	NEC America	µPD4001	
	RCA	CD4001	
	SGS	HBF4001	
	Solitron	CM4001	
	TI	TP4001	
	Toshiba	TC4001	
SCL4002	Fairchild	F4002	
	Mitel	SIL4002	
	Motorola	MC14002	
	National	CD4002	
	NEC America	µPD4002	
	RCA	CD4002	
	SGS	HBF4002	
	Solitron	CM4002	
	TI	TP4002	
	Toshiba	TC4002	
SCL4006	Fairchild	F4006	
	Motorola	MC14006	
	National	CD4006	
	NEC America	µPD4006	
	RCA	CD4006	
	Solitron	CM4006	
SCL4007	Fairchild	F4007	
	Mitel	SIL4007	
	Motorola	MC14007	
	National	CD4007	
	RCA	CD4007	
	SGS	HBF4007	
	Solitron	CM4007	
	TI	TP4007	
	Toshiba	TC4007	
SCL4008	Fairchild	F4008	
	Motorola	MC14008	
	National	CD4008	
	RCA	CD4008	
	SGS	HBF4008	
	Solitron	CM4008	
	TI	TP4008	
	Toshiba	TC4008	
SCL4009	Mitel	SIL4009	
	National	CD4009	
	RCA	CD4009	
	SGS	HBF4009	
	Solitron	CM4009	
	TI	TP4009	
	Toshiba	TC4009	
SCL4010	Mitel	SIL4010	
	National	CD4010	
SCL4010	RCA	CD4010	
	SGS	HBF4010	
	Solitron	CM4010	
	TI	TP4010	
	Toshiba	TC4010	
SCL4011	Fairchild	F4011	
	Mitel	SIL4011	
		SIL4911	
	Motorola	MC14011	
	National	CD4011	
	NEC America	µPD4011	
	RCA	CD4011	
	SGS	HBF4011	
	Solitron	CM4011	
	TI	TP4011	
	Toshiba	TC4011	
SCL4012	Fairchild	F4012	
	Mitel	SIL4012	
		SIL4912	
	Motorola	MC14012	
	National	CD4012	
	NEC America	µPD4012	
	RCA	CD4012	
	SGS	HBF4012	
	Solitron	CM4012	
	TI	TP4012	
	Toshiba	TC4012	
SCL4013	Fairchild	F4013	
	Mitel	SIL4013	
	Motorola	MC14013	
	National	CD4013	
	NEC America	µPD4013	
	RCA	CD4013	
	SGS	HBF4013	
	Solitron	CM4013	
	TI	TP4013	
	Toshiba	TC4013	
SCL4014	Fairchild	F4014	
	Mitel	SIL4014	
	Motorola	MC14014	
	National	CD4014	
	NEC America	µPD4014	
	RCA	CD4014	
	SGS	HBF4014	
	Solitron	CM4014	
	TI	TP4014	
	Toshiba	TC4014	
SCL4015	Fairchild	F4015	
	Mitel	SIL4015	
	Motorola	MC14015	
	National	CD4015	
	NEC America	µPD4015	
	RCA	CD4015	
	SGS	HBF4015	
	Solitron	CM4015	
	TI	TP4015	
	Toshiba	TC4015	
SCL4016	AD	AD7516	
	Fairchild	F4016	
	Micro Power	MPS7516	
	Mitel	SIL4016	
	Motorola	MC14016	
	National	CD4016	
	RCA	CD4016	
		CD4066	
	Solitron	CM4016	
	TI	TP4016	
SCL4017	Fairchild	F4017	
	Mitel	SIL4017	
	Motorola	MC14017	
	National	CD4017	
	NEC America	µPD4017	
	RCA	CD4017	
	SGS	HBF4017	
	Solitron	CM4017	
	TI	TP4017	
	Toshiba	TC4017	
SCL4018	Fairchild	F4018	
	Mitel	SIL4018	
	National	CD4018	
	RCA	CD4018	
	SGS	HBF4018	
	Solitron	CM4018	
	TI	TP4018	
	Toshiba	TC4018	
SCL4019	Fairchild	F4019	

◆ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Solid State Scientific (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
SCL4019	Mitel	SIL4019	
	National	CD4019	
	NEC America	μPD4019	
	RCA	CD4019	
	SGS	HBF4019	
	Solitron	CM4019	
	TI	TP4019	
	Toshiba	TC4019	
SCL4020	Fairchild	F4020	
	Mitel	SIL4020	
	Motorola	MC14020	
	National	CD4020	
	NEC America	μPD4020	
	RCA	CD4020	
	SGS	HBF4020	
	Solitron	CM4020	
	TI	TP4020	
	Toshiba	TC4020	
SCL4021	Fairchild	F4021	
	Mitel	SIL4021	
	Motorola	MC14021	
	National	CD4021	
	NEC America	μPD4021	
	RCA	CD4021	
	Solitron	CM4021	
	TI	TP4021	
	Toshiba	TC4021	
SCL4022	Fairchild	F4022	
	Mitel	SIL4022	
	Motorola	MC14022	
	National	CD4022	
	RCA	CD4022	
	SGS	HBF4022	
	Solitron	CM4022	
	TI	TP4022	
	Toshiba	TC4022	
SCL4023	Fairchild	F4023	
	Mitel	SIL4023	
		SIL4923	
	Motorola	MC14023	
	National	CD4023	
	NEC America	μPD4023	
	RCA	CD4023	
	SGS	HBF4023	
	Solitron	CM4023	
	TI	TP4023	
	Toshiba	TC4023	
SCL4024	Fairchild	F4024	
	Mitel	SIL4024	
	Motorola	MC14024	
	National	CD4024	
	NEC America	μPD4024	
	RCA	CD4024	
	SGS	HBF4024	
	Solitron	CM4024	
	TI	TP4024	
	Toshiba	TC4024	
SCL4025	Fairchild	F4025	
	Mitel	SIL4025	
		SIL4925	
	Motorola	MC14025	
	National	CD4025	
	NEC America	μPD4025	
	RCA	CD4025	
	SGS	HBF4025	
	Solitron	CM4025	
	TI	TP4025	
	Toshiba	TC4025	
SCL4026	RCA	CD4026	
	Solitron	CM4026	
SCL4027	Fairchild	F4027	
	Mitel	SIL4027	
	Motorola	MC14027	
	National	CD4027	
	NEC America	μPD4027	
	RCA	CD4027	
	SGS	HBF4027	
	Solitron	CM4027	
	TI	TP4027	
	Toshiba	TC4027	
SCL4028	Fairchild	F4028	
	Mitel	SIL4028	
	Motorola	MC14028	
SCL4028	National	CD4028	
	NEC America	μPD4028	
	RCA	CD4028	
	SGS	HBF4028	
	Solitron	CM4028	
	TI	TP4028	
	Toshiba	TC4028	
SCL4029	Fairchild	F4029	
	Mitel	SIL4029	
	National	CD4029	
	NEC America	μPD4029	
	RCA	CD4029	
	SGS	HBF4029	
	Solitron	CM4029	
	TI	TP4029	
	Toshiba	TC4029	
SCL4030	Fairchild	F4030	
	Mitel	SIL4030	
	Motorola	MC14507	
	National	CD4030	
		CD4070	
		CD4507	
		MM74C86	
	NEC America	μPD4030	
	RCA	CD4030	
		CD4070	
	SGS	HBF4030	
	Solitron	CM4030	
	TI	TP4030	
		TP4507	
	Toshiba	TC4030	
SCL4033	RCA	CD4033	
	SGS	HBF4033	
	Solitron	CM4033	
SCL4034	Fairchild	F4034	
	Motorola	MC14034	
	National	CD4034	
	NEC America	μPD4034	
	RCA	CD4034	
	Solitron	CM4034	
	Toshiba	TC4034	
SCL4035	Fairchild	F4035	
	Mitel	SIL4035	
	Motorola	MC14035	
	National	CD4035	
	NEC America	μPD4035	
	RCA	CD4035	
	SGS	HBF4035	
	Solitron	CM4035	
	TI	TP4035	
	Toshiba	TC4035	
SCL4040	Fairchild	F4040	
	Mitel	SIL4040	
	Motorola	MC14040	
	National	CD4040	
	NEC America	μPD4040	
	RCA	CD4040	
	Solitron	CM4040	
	TI	TP4040	
	Toshiba	TC4040	
SCL4041	Fairchild	F4041	
	National	CD4041	
	RCA	CD4041	
	Solitron	CM4041	
	SSS	CL4041	
SCL4042	Fairchild	F4042	
	Mitel	SIL4042	
	Motorola	MC14042	
	National	CD4042	
	NEC America	μPD4042	
	RCA	CD4042	
	SGS	HBF4042	
	Solitron	CM4042	
	TI	TP4042	
	Toshiba	TC4042	
SCL4043	Fairchild	F4043	
	Mitel	SIL4043	
	Motorola	MC14043	
	National	CD4043	
	NEC America	μPD4043	
	RCA	CD4043	
	Solitron	CM4043	
	TI	TP4043	
	Toshiba	TC4043	
SCL4044	Fairchild	F4044	
	Mitel	SIL4043	
SCL4044	Mitel	SIL4044	
	Motorola	MC14044	
	National	CD4044	
	NEC America	μPD4044	
	RCA	CD4044	
	Solitron	CM4044	
	TI	TP4044	
	Toshiba	TC4044	
SCL4045	RCA	CD4045	
SCL4046	Fairchild	F4046	
	Mitel	SIL4046	
	Motorola	MC14046	
	National	CD4046	
	RCA	CD4046	
	Solitron	CM4046	
SCL4049	Fairchild	F4049	
	Mitel	SIL4049	
	Motorola	MC14049	
	National	CD4049	
	NEC America	μPD4049	
	RCA	CD4049	
	SGS	HBF4049	
	Solitron	CM4049	
	TI	TP4049	
	Toshiba	TC4049	
SCL4050	Fairchild	F4050	
	Mitel	SIL4050	
	Motorola	MC14050	
	National	CD4050	
	NEC America	μPD4050	
	RCA	CD4050	
	SGS	HBF4050	
	Solitron	CM4050	
	TI	TP4050	
	Toshiba	TC4050	
SCL4051	Fairchild	F4051	
	Mitel	SIL4051	
	Motorola	MC14051	
	National	CD4051	
	NEC America	μPD4051	
	RCA	CD4051	
	Solitron	CM4051	
	TI	TP4051	
	Toshiba	TC4051	
SCL4052	Fairchild	F4052	
	Mitel	SIL4052	
	Motorola	MC14052	
	National	CD4052	
	NEC America	μPD4052	
	RCA	CD4052	
	Solitron	CM4052	
	TI	TP4052	
	Toshiba	TC4052	
SCL4053	Fairchild	F4053	
	Mitel	SIL4053	
	Motorola	MC14053	
	National	CD4053	
	NEC America	μPD4053	
	RCA	CD4053	
	Solitron	CM4053	
	Toshiba	TC4053	
SCL4060	Mitel	SIL4060	
	National	CD4060	
	RCA	CD4060	
SCL4066	Fairchild	F4066	
	Mitel	SIL4066	
	Motorola	MC14066	
	National	CD4066	
	NEC America	μPD4066	
	RCA	CD4063	
		CD4066	
	SGS	HBF4066	
	Signetics	N4066	
	Solitron	CM4066	
	Toshiba	TC4066	
SCL4068	Fairchild	F4068	
	Mitel	SIL4068	
		SIL4968	
	Motorola	MC14068	
	NEC America	μPD4068	
	RCA	CD4068	
	Solitron	CM4068	
	TI	TP4068	
	Toshiba	TC4068	
SCL4069	Fairchild	F4069	
	Harris	HD74C04	
SCL4069	Mitel	SIL4069	
	Motorola	MC14069	
	National	CD4069	
		MM74C04	
	NEC America	μPD4069	
	RCA	CD4069	
	Solitron	CM4069	
	TI	TP4069	
	Toshiba	TC4069	
SCL4070	Fairchild	F4070	
	Mitel	SIL4070	
	National	CD4070	
		MM74C86	
	RCA	CD4070	
	Solitron	CM4070	
SCL4071	Fairchild	F4071	
	Mitel	SIL4071	
	Motorola	MC14071	
	National	CD4071	
	NEC America	μPD4071	
	RCA	CD4071	
	Solitron	CM4071	
	TI	TP4071	
	Toshiba	TC4071	
SCL4072	Fairchild	F4072	
	Mitel	SIL4072	
	Motorola	MC14072	
	RCA	CD4072	
	TI	TP4072	
	Toshiba	TC4072	
SCL4073	Fairchild	F4073	
	Mitel	SIL4073	
	Motorola	MC14073	
	National	CD4073	
	NEC America	μPD4073	
	RCA	CD4073	
	Solitron	CM4073	
	TI	TP4073	
	Toshiba	TC4073	
SCL4075	Fairchild	F4075	
	Mitel	SIL4075	
	Motorola	MC14075	
	National	CD4075	
	NEC America	μPD4075	
	RCA	CD4075	
	TI	TP4075	
	Toshiba	TC4075	
SCL4076	Fairchild	F4076	
	Harris	HD74C173	
	Mitel	SIL4076	
	Motorola	MC14076	
	National	CD4076	
		MM74C173	
	RCA	CD4076	
	Solitron	CM4076	
SCL4077	Fairchild	F4077	
	Mitel	SIL4077	
	Motorola	MC14077	
	RCA	CD4077	
	Solitron	CM4077	
SCL4078	Fairchild	F4078	
	Mitel	SIL4078	
		SIL4978	
	Motorola	MC14078	
	NEC America	μPD4078	
	RCA	CD4078	
	Solitron	CM4078	
	Toshiba	TC4078	
SCL4081	Fairchild	F4081	
	Mitel	SIL4081	
	Motorola	MC14081	
	National	CD4081	
	NEC America	μPD4081	
	RCA	CD4081	
	Solitron	CM4081	
	TI	TP4081	
	Toshiba	TC4081	
SCL4082	Fairchild	F4082	
	Mitel	SIL4082	
	Motorola	MC14082	
	NEC America	μPD4082	
	RCA	CD4082	
	TI	TP4082	
	Toshiba	TC4082	
SCL4094	NEC America	μPD4094	
	RCA	CD4094	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Solid State Scientific (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
SCL4402	RCA	CD4048	
SCL4412	RCA	CD4068	
SCL4445	RCA	CD4045	
	SGS	HBF4045	
	Solitron	CM4045	
SCL4449	RCA	CD4069	
SCL4502	Mitel	SIL4502	
	Motorola	MC14502	
	RCA	CD4502	
SCL4508	Mitel	SIL4508	
	Motorola	MC14508	
	NEC America	μPD4508	
	RCA	CD4508	
	Toshiba	TC4508	
SCL4510	Fairchild	F4510	
	Mitel	SIL4510	
	Motorola	MC14510	
	National	CD4510	
	NEC America	μPD4510	
	RCA	CD40192	
		CD4510	
	Toshiba	TC4510	
SCL4511	Fairchild	F4511	
	Mitel	SIL4511	
	Motorola	MC14511	
	National	CD4511	
	NEC America	μPD4511	
	RCA	CD4511	
	Solitron	CM4511	
	TI	TP4511	
SCL4512	Fairchild	F4512	
	Mitel	SIL4512	
	Motorola	MC14512	
	National	CD4512	
	NEC America	μPD4512	
	TI	TP4512	
	Toshiba	TC4512	
SCL4514	Fairchild	F4514	
	Mitel	SIL4514	
	Motorola	MC14514	
	National	CD4514	
	NEC America	μPD4514	
	RCA	CD4514	
	Solitron	CM4514	
	Toshiba	TC4514	
SCL4515	Fairchild	F4515	
	Mitel	SIL4515	
	Motorola	MC14515	
	National	CD4515	
	NEC America	μPD4515	
	RCA	CD4515	
	Solitron	CM4515	
	Toshiba	TC4515	
SCL4516	Fairchild	F4516	
	Mitel	SIL4516	
	Motorola	MC14516	
	National	CD4516	
	NEC America	μPD4516	
	RCA	CD40193	
		CD4516	
	Toshiba	TC4516	
SCL4517	Motorola	MC14517	
	NEC America	μPD4517	
SCL4518	Fairchild	F4518	
	Mitel	SIL4518	
	Motorola	MC14518	
	National	CD4518	
	NEC America	μPD4518	
	RCA	CD4518	
	Solitron	CM4518	
	TI	TP4518	
	Toshiba	TC4518	
SCL4520	Fairchild	F4520	
	Mitel	SIL4520	
	Motorola	MC14520	
	National	CD4520	
	NEC America	μPD4520	
	RCA	CD4520	
	Solitron	CM4520	
	TI	TP4520	
	Toshiba	TC4520	
SCL4522	Fairchild	F4522	
	Motorola	MC14522	
SCL4522	National	CD4522	
	NEC America	μPD4522	
	RCA	CD4018	
	TI	TP4522	
SCL4526	Fairchild	F4526	
	Motorola	MC14526	
	NEC America	μPD4526	
	TI	TP4526	
SCL4527	Motorola	MC14527	
	National	CD4527	
	RCA	CD4527	
SCL4528	Fairchild	F4528	
	Mitel	SIL4528	
	Motorola	MC14528	
	National	CD4528	
	NEC America	μPD4528	
	RCA	CD4098	
		CD4528	
	Toshiba	TC4528	
SCL4531	Fairchild	F4531	
	Motorola	MC14531	
	RCA	CD40101	
	TI	TP4531	
SCL4543	Motorola	MC14543	
	National	CD4543	
	RCA	CD4056	
SCL4555	Fairchild	F4555	
	Motorola	MC14555	
	NEC America	μPD4555	
	RCA	CD4555	
SCL4556	Fairchild	F4556	
	Motorola	MC14556	
	NEC America	μPD4556	
	RCA	CD4556	
SCL4581	Motorola	MC14581	
	RCA	CD40181	
	TI	TP4581	
SCL4582	Fairchild	F4582	
	Motorola	MC14582	
	RCA	CD40182	
	TI	TP4582	
SCL4584	Motorola	MC14584	
	National	CD4584	
		MM74C14	
	NEC America	μPD4584	
	RCA	CD4016	
SCL4585	Motorola	MC14585	
	National	MM74C85	
	RCA	CD4063	
	Toshiba	TC4585	
◆SCL5437	Mostek	MK50040	

Solitron Devices

μA2556	Mostek	MK4007	
μA2656	Mostek	MK4007	
μA3556	Mostek	MK4007	
μA3656	Mostek	MK4007	
CM4000	Mitel	SIL4000	
	Motorola	MC14000	
	National	CD4000	
	RCA	CD4000	
	SSS	SCL4000	
	TI	TP4000	
CM4001	Fairchild	F4001	
	Mitel	SIL4001	
	Motorola	MC14001	
	National	CD4001	
	NEC America	μPD4001	
	RCA	CD4001	
	SGS	HBF4001	
	SSS	SCL4001	
	TI	TP4001	
	Toshiba	TC4001	
CM4002	Fairchild	F4002	
	Mitel	SIL4002	
	Motorola	MC14002	
	National	CD4002	
	NEC America	μPD4002	
	RCA	CD4002	
	SGS	HBF4002	
	SSS	SCL4002	
	TI	TP4002	
	Toshiba	TC4002	
CM4006	Fairchild	F4006	
CM4006	Motorola	MC14006	
	National	CD4006	
	RCA	CD4006	
	SSS	SCL4006	
CM4007	Fairchild	F4007	
	Mitel	SIL4007	
	Motorola	MC14007	
	National	CD4007	
	RCA	CD4007	
	SGS	HBF4007	
	SSS	SCL4007	
	TI	TP4007	
	Toshiba	TC4007	
CM4008	Fairchild	F4008	
	Motorola	MC14008	
	National	CD4008	
	RCA	CD4008	
	SGS	HBF4008	
	SSS	SCL4008	
	TI	TP4008	
	Toshiba	TC4008	
CM4009	Mitel	SIL4009	
	National	CD4009	
	RCA	CD4009	
	SGS	HBF4009	
	SSS	SCL4009	
	TI	TP4009	
	Toshiba	TC4009	
CM4010	Mitel	SIL4010	
	National	CD4010	
	RCA	CD4010	
	SGS	HBF4010	
	SSS	SCL4010	
	TI	TP4010	
	Toshiba	TC4010	
CM4011	Fairchild	F4011	
	Mitel	SIL4011	
	Motorola	MC14011	
	National	CD4011	
	NEC America	μPD4011	
	RCA	CD4011	
	SGS	HBF4011	
	SSS	SCL4011	
	TI	TP4011	
	Toshiba	TC4011	
CM4012	Fairchild	F4012	
	Mitel	SIL4012	
	Motorola	MC14012	
	National	CD4012	
	NEC America	μPD4012	
	RCA	CD4012	
	SGS	HBF4012	
	SSS	SCL4012	
	TI	TP4012	
	Toshiba	TC4012	
CM4013	Fairchild	F4013	
	Mitel	SIL4013	
	Motorola	MC14013	
	National	CD4013	
	NEC America	μPD4013	
	RCA	CD4013	
	SGS	HBF4013	
	SSS	SCL4013	
	TI	TP4013	
	Toshiba	TC4013	
CM4014	Fairchild	F4014	
	Mitel	SIL4014	
	Motorola	MC14014	
	National	CD4014	
	NEC America	μPD4014	
	RCA	CD4014	
	SGS	HBF4014	
	SSS	SCL4014	
	TI	TP4014	
	Toshiba	TC4014	
CM4015	Fairchild	F4015	
	Mitel	SIL4015	
	Motorola	MC14015	
	National	CD4015	
	NEC America	μPD4015	
	RCA	CD4015	
	SGS	HBF4015	
	SSS	SCL4015	
	TI	TP4015	
	Toshiba	TC4015	
CM4016	AD	AD7516	
CM4016	Fairchild	F4016	
	Micro Power	MPS7516	
	Mitel	SIL4016	
	Motorola	MC14016	
	National	CD4016	
	RCA	CD4016	
		CD4066	
	SSS	SCL4016	
	TI	TP4016	
CM4017	Fairchild	F4017	
	Mitel	SIL4017	
	Motorola	MC14017	
	National	CD4017	
	NEC America	μPD4017	
	RCA	CD4017	
	SGS	HBF4017	
	SSS	SCL4017	
	TI	TP4017	
	Toshiba	TC4017	
CM4018	Fairchild	F4018	
	Mitel	SIL4018	
	National	CD4018	
	RCA	CD4018	
	SGS	HBF4018	
	SSS	SCL4018	
	TI	TP4018	
	Toshiba	TC4018	
CM4019	Fairchild	F4019	
	Mitel	SIL4019	
	Motorola	MC14519	
	National	CD4019	
	RCA	CD4019	
	SGS	HBF4019	
	SSS	SCL4019	
	TI	TP4019	
	Toshiba	TC4019	
CM4020	Fairchild	F4020	
	Mitel	SIL4020	
	Motorola	MC14020	
	National	CD4020	
	NEC America	μPD4020	
	RCA	CD4020	
	SGS	HBF4020	
	SSS	SCL4020	
	TI	TP4020	
	Toshiba	TC4020	
CM4021	Fairchild	F4021	
	Mitel	SIL4021	
	Motorola	MC14021	
	National	CD4021	
	NEC America	μPD4021	
	RCA	CD4021	
	SSS	SCL4021	
	TI	TP4021	
	Toshiba	TC4021	
CM4022	Fairchild	F4022	
	Mitel	SIL4022	
	Motorola	MC14022	
	National	CD4022	
	RCA	CD4022	
	SGS	HBF4022	
	SSS	SCL4022	
	TI	TP4022	
	Toshiba	TC4022	
CM4023	Fairchild	F4023	
	Mitel	SIL4023	
	Motorola	MC14023	
	National	CD4023	
	NEC America	μPD4023	
	RCA	CD4023	
	SGS	HBF4023	
	SSS	SCL4023	
	TI	TP4023	
	Toshiba	TC4023	
CM4024	Fairchild	F4024	
	Mitel	SIL4024	
	Motorola	MC14024	
	National	CD4024	
	RCA	CD4024	
	SGS	HBF4024	
	SSS	SCL4024	
	TI	TP4024	
	Toshiba	TC4024	
CM4025	Fairchild	F4025	
	Mitel	SIL4025	
	Motorola	MC14025	

◆ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Solitron Devices (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
CM4025	National	CD4025	
	NEC America	μPD4025	
	RCA	CD4025	
	SGS	HBF4025	
	SSS	SCL4025	
	TI	TP4025	
	Toshiba	TC4025	
CM4026	RCA	CD4026	
	SSS	SCL4026	
CM4027	Fairchild	F4027	
	Mitel	SIL4027	
	Motorola	MC14027	
	National	CD4027	
	NEC America	μPD4027	
	RCA	CD4027	
	SGS	HBF4027	
	SSS	SCL4027	
	TI	TP4027	
	Toshiba	TC4027	
CM4028	Fairchild	F4028	
	Mitel	SIL4028	
	Motorola	MC14028	
	National	CD4028	
	NEC America	μPD4028	
	RCA	CD4028	
	SGS	HBF4028	
	SSS	SCL4028	
	TI	TP4028	
	Toshiba	TC4028	
CM4029	Fairchild	F4029	
	Mitel	SIL4029	
	National	CD4029	
	NEC America	μPD4029	
	RCA	CD4029	
	SGS	HBF4029	
	SSS	SCL4029	
	TI	TP4029	
	Toshiba	TC4029	
CM4030	Fairchild	F4030	
	Mitel	SIL4030	
	National	CD4030	
	NEC America	μPD4030	
	RCA	CD4030	
		CD4070	
	SGS	HBF4030	
	SSS	SCL4030	
	TI	TP4030	
	Toshiba	TC4030	
CM4032	Motorola	MC14032	
	RCA	CD4032	
	Toshiba	TC4032	
CM4033	RCA	CD4033	
	SGS	HBF4033	
	SSS	SCL4033	
CM4034	Fairchild	F4034	
	Motorola	MC14034	
	National	CD4034	
	RCA	CD4034	
	SSS	SCL4034	
	Toshiba	TC4034	
CM4035	Fairchild	F4035	
	Mitel	SIL4035	
	Motorola	MC14035	
	National	CD4035	
	NEC America	μPD4035	
	RCA	CD4035	
	SGS	HBF4035	
	SSS	SCL4035	
	TI	TP4035	
	Toshiba	TC4035	
CM4036	RCA	CD4036	
CM4037	RCA	CD4037	
CM4038	Motorola	MC14038	
		MC14308	
	RCA	CD4038	
	Toshiba	TC4038	
CM4039	RCA	CD4039	
CM4040	Fairchild	F4040	
	Mitel	SIL4040	
	Motorola	MC14040	
	National	CD4040	
	NEC America	μPD4040	
	RCA	CD4040	
CM4040	SSS	SCL4040	
	TI	TP4040	
	Toshiba	TC4040	
CM4041	Fairchild	F4041	
	National	CD4041	
	RCA	CD4041	
	SSS	CL4041	
		SCL4041	
CM4042	Fairchild	F4042	
	Mitel	SIL4042	
	Motorola	MC14042	
	National	CD4042	
	NEC America	μPD4042	
	RCA	CD4042	
	SGS	HBF4042	
	SSS	SCL4042	
	TI	TP4042	
	Toshiba	TC4042	
CM4043	Fairchild	F4043	
	Mitel	SIL4043	
	Motorola	MC14023	
		MC14043	
	National	CD4023	
		CD4043	
	NEC America	μPD4043	
	RCA	CD4023	
		CD4043	
	SSS	SCL4023	
		SCL4043	
	TI	TP4043	
	Toshiba	TC4043	
CM4044	Fairchild	F4044	
	Mitel	SIL4044	
	Motorola	MC14044	
	National	CD4044	
	NEC America	μPD4044	
	RCA	CD4044	
	SSS	SCL4044	
	TI	TP4044	
	Toshiba	TC4044	
CM4045	RCA	CD4045	
	SGS	HBF4045	
	SSS	SCL4445	
CM4046	Fairchild	F4046	
	Mitel	SIL4046	
	Motorola	MC14046	
	National	CD4046	
	RCA	CD4046	
	SSS	SCL4046	
CM4047	Fairchild	F4047	
	RCA	CD4047	
	Toshiba	TC4047	
CM4048	RCA	CD4048	
CM4049	Fairchild	F4049	
	Mitel	SIL4049	
	Motorola	MC14049	
	National	CD4049	
	NEC America	μPD4049	
	RCA	CD4049	
	SGS	HBF4049	
	SSS	SCL4049	
	TI	TP4049	
	Toshiba	TC4049	
CM4050	Fairchild	F4050	
	Mitel	SIL4050	
	Motorola	MC14050	
	National	CD4050	
	NEC America	μPD4050	
	RCA	CD4050	
	SGS	HBF4050	
	SSS	SCL4050	
	TI	TP4050	
	Toshiba	TC4050	
CM4051	Fairchild	F4051	
	Mitel	SIL4051	
	Motorola	MC14051	
	National	CD4051	
	RCA	CD4051	
	SSS	SCL4051	
	TI	TP4051	
	Toshiba	TC4051	
CM4052	Fairchild	F4052	
	Mitel	SIL4052	
	Motorola	MC14052	
	National	CD4052	
	RCA	CD4052	
CM4052	SSS	SCL4052	
	TI	TP4052	
	Toshiba	TC4052	
CM4053	Fairchild	F4053	
	Mitel	SIL4053	
	Motorola	MC14053	
	National	CD4053	
	RCA	CD4053	
	SSS	SCL4053	
	Toshiba	TC4053	
CM4066	Fairchild	F4066	
	Mitel	SIL4066	
	Motorola	MC14066	
	National	CD4066	
	NEC America	μPD4066	
	RCA	CD4063	
		CD4066	
	SGS	HBF4066	
	Signetics	N4066	
	SSS	SCL4066	
	Toshiba	TC4066	
CM4068	Fairchild	F4068	
	Mitel	SIL4068	
	Motorola	MC14068	
	RCA	CD4068	
	SSS	SCL4068	
	TI	TP4068	
	Toshiba	TC4068	
CM4069	Fairchild	F4069	
	Harris	HD74C04	
	Mitel	SIL4069	
	Motorola	MC14069	
	National	CD4069	
		MM74C04	
	NEC America	μPD4069	
	RCA	CD4069	
	SSS	SCL4069	
	TI	TP4069	
	Toshiba	TC4069	
CM4070	Fairchild	F4070	
	Mitel	SIL4070	
	National	CD4070	
		MM74C86	
	RCA	CD4070	
	SSS	SCL4070	
CM4071	Fairchild	F4071	
	Mitel	SIL4071	
	Motorola	MC14071	
	National	CD4071	
	NEC America	μPD4071	
	RCA	CD4071	
	SSS	SCL4071	
	TI	TP4071	
	Toshiba	TC4071	
CM4073	Fairchild	F4073	
	Mitel	SIL4073	
	Motorola	MC14073	
	National	CD4073	
	RCA	CD4073	
	SSS	SCL4073	
	TI	TP4073	
	Toshiba	TC4073	
CM4075	RCA	CD4075	
CM4076	Fairchild	F4076	
	Harris	HD74C173	
	Mitel	SIL4076	
	Motorola	MC14076	
	National	CD4076	
		MM74C173	
	RCA	CD4076	
	SSS	SCL4076	
CM4077	Fairchild	F4077	
	Mitel	SIL4077	
	Motorola	MC14077	
	RCA	CD4077	
	SSS	SCL4077	
CM4078	Fairchild	F4078	
	Mitel	SIL4078	
	Motorola	MC14078	
	RCA	CD4078	
	SSS	SCL4078	
	Toshiba	TC4078	
CM4081	Fairchild	F4081	
	Mitel	SIL4081	
	Motorola	MC14081	
	National	CD4081	
CM4081	NEC America	μPD4081	
	RCA	CD4081	
	SSS	SCL4081	
	TI	TP4081	
	Toshiba	TC4081	
CM4510	National	CD4510	
	RCA	CD4510	
CM4511	Fairchild	F4511	
	Mitel	SIL4511	
	Motorola	MC14511	
	National	CD4511	
	RCA	CD4511	
	SSS	SCL4511	
	TI	TP4511	
CM4514	Fairchild	F4514	
	Mitel	SIL4514	
	Motorola	MC14514	
	RCA	CD4514	
	SSS	SCL4514	
	Toshiba	TC4514	
CM4515	Mitel	SIL4515	
	Motorola	MC14515	
	RCA	CD4515	
	SSS	SCL4515	
	Toshiba	TC4515	
CM4516	National	CD4516	
CM4518	Fairchild	F4518	
	Mitel	SIL4518	
	Motorola	MC14518	
	National	CD4518	
	RCA	CD4518	
	SSS	SCL4518	
	TI	TP4518	
	Toshiba	TC4518	
CM4520	Fairchild	F4520	
	Mitel	SIL4520	
	Motorola	MC14520	
	National	CD4520	
	NEC America	μPD4520	
	RCA	CD4520	
	SSS	SCL4520	
	TI	TP4520	
	Toshiba	TC4520	
UC4250	Intersil	LM4250	
	National	LM4250	
	Silicon G	SG4250	
UC4741	**PMI**	**SSS741**	**839**
	RCA	CA741	

Sprague Electric Company

Manufacturer Device	Replacement Source	Device	IC Master Page
UDN-5711	Motorola	MC1471	
	Signetics	UDN5711	
UDN-5712	Motorola	MC1472	
	Signetics	UDN5712	
UDN-5713	Motorola	MC1473	
	Signetics	UDN5713	
UDN-5714	Motorola	MC1474	
	Signetics	UDN5714	
ULN-2001	Exar	XR2201	
	Fairchild	9665	
	Motorola	ULN-2001	
	SGS	L201	
	Signetics	NE5601	
		ULN2001	
	Silicon G	SG2001	
	TI	ULN2001	
ULN-2002	Exar	XR2202	
	Fairchild	9666	
	Motorola	ULN-2002	
	SGS	L202	
	Signetics	NE5502	
		ULN2002	
	Silicon G	SG2002	
	TI	ULN2002	
ULN-2003	Exar	XR2203	
	Fairchild	9667	
	Motorola	ULN-2003	
	SGS	L203	
	Signetics	NE5503	
		ULN2003	
	Silicon G	SG2003	
	TI	ULN2003	
ULN-2004	Exar	XR2204	
	Fairchild	9668	

◆ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Sprague Electric Company (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
ULN-2004	Motorola	ULN-2004	
	Signetics	NE5504	
		ULN2004	
	Silicon G	SG2004	
	TI	ULN2004	
ULN-2021	Signetics	NE5501	
ULN 2022	Signetics	NE5502	
ULN-2023	Signetics	NE5503	
ULN-2024	Signetics	NE5504	
ULN-2111	Fairchild	μA2136	
	Motorola	MC1357	
	National	LM2111	
	RCA	CA2111	
ULN-2114	Fairchild	μA746	
	RCA	CA3072	
♦ULN-2120	Fairchild	μA732	
ULN-2124	Fairchild	μA780	
	RCA	CA3070	
ULN-2125	RCA	CA3120	
♦ULN-2126	Exar	XR4739	
	Fairchild	μA739	
	SGS	TBA231	
ULN-2127	Fairchild	μA781	
	RCA	CA3071	
♦ULN-2128	Fairchild	μA767	
ULN-2129	Motorola	MC1375	
♦ULN-2131	Fairchild	μA753	
ULN-2136	Fairchild	μA2136	
	Motorola	MC1356	
ULN-2137	Fairchild	μA720	
	RCA	CA3123	
ULN-2165	Fairchild	μA3065	
	Motorola	MC1358	
	RCA	CA3065	
ULN-2209	Fairchild	μA753	
ULN-2210	Exar	XR1310	
	Motorola	MC1310	
	RCA	CA1310	
ULN-2211	Motorola	MC1310	
	RCA	CA3011	
ULN-2212	RCA	CA3012	
ULN-2224	Motorola	MC1324	
ULN-2244	Fairchild	μA758	
	RCA	CA758	
♦ULN-2262	Fairchild	μA787	
	RCA	CA3126	
ULN-2264	Fairchild	μA3064	
	Motorola	MC1364	
	RCA	CA3064	
♦ULN-2266	RCA	CA3066	
♦ULN-2267	Fairchild	μA3067	
ULN-2269	RCA	CA3121	
ULN-2278	Fairchild	μA705	
ULN-2289	Fairchild	μA3089	
	RCA	CA3089	
ULN-2298	Motorola	MC1398	
	RCA	CA1398	
ULN-2741	National	LM741	
	RCA	CA741	
	TI	μA741	
♦ULN-2747	RCA	CA747	
	TI	μA747	
ULN-3304	Micro Comp	MCC102	
ULN-3305	Micro Comp	MCC122	
ULS-	Sprague	See ULN-	

Standard Microsystems Corporation

CG400	Mostek	MK2002	
	TI	TMS4100	
COM1671	Western	UC1671	
COM2017	**AMI**	**S1883**	**354,1587**
	TI	TMS6011	
	Western	TR1602	
COM2502	GI	AY3-1014A	
		AY3-1015	
	Western	TR1602A	
COM2505	GI	AY5-1013	
COM2601	**AMI**	**S2350**	**368,1589**
COM5016	Western	BR1941	
COM5025	Signetics	2652	
KR2376	GI	AY5-2376	
KR3600	GI	AY5-3600	

Stewart-Warner Microcircuits

♦SW1800	Motorola	MC1800	
	TI	SN151800	
♦SW1801	Motorola	MC1801	
	TI	SN151801	
♦SW1802	Motorola	MC1802	
	TI	SN151802	
♦SW1805	Motorola	MC1805	
	TI	SN15805	
♦SW1806	Motorola	MC1806	
	TI	SN151806	
♦SW1807	Motorola	MC1807	
	TI	SN151807	
♦SW1808	Motorola	MC1808	
	TI	SN151808	
♦SW1810	Motorola	MC1810	
	TI	SN151810	
♦SW1812	Motorola	MC1812	
	TI	SN151812	
♦SW1814	Motorola	MC1814	
♦SW1900	Motorola	MC1900	
	TI	SN151900	
♦SW1901	Motorola	MC1901	
	TI	SN151901	
♦SW1902	Motorola	MC1902	
	TI	SN151902	
♦SW1905	Motorola	MC1905	
	TI	SN151905	
♦SW1906	Motorola	MC1906	
	TI	SN151906	
♦SW1907	Motorola	MC1907	
	TI	SN151907	
♦SW1908	Motorola	MC1908	
	TI	SN151908	
♦SW1910	Motorola	MC1910	
	TI	SN151910	
♦SW1912	Motorola	MC1912	
	TI	SN151912	
♦SW1914	Motorola	MC1914	
♦SW301	Motorola	MC301	
♦SW302	Motorola	MC302	
♦SW303	Motorola	MC303	
♦SW304	Motorola	MC304	
♦SW305	Motorola	MC305	
♦SW306	Motorola	MC306	
♦SW307	Motorola	MC307	
♦SW308	Motorola	MC308	
♦SW309	Motorola	MC309	
♦SW310	Motorola	MC310	
♦SW311	Motorola	MC311	
♦SW351	Motorola	MC351	
♦SW352	Motorola	MC352	
♦SW353	Motorola	MC353	
♦SW354	Motorola	MC354	
♦SW355	Motorola	MC355	
♦SW356	Motorola	MC356	
♦SW357	Motorola	MC357	
♦SW358	Motorola	MC358	
♦SW359	Motorola	MC359	
♦SW360	Motorola	MC360	
♦SW361	Motorola	MC361	
♦SW4001	RCA	CD4001	
♦SW4002	RCA	CD4002	
♦SW4011	RCA	CD4011	
♦SW4012	RCA	CD4012	
♦SW4013	RCA	CD4013	
♦SW4015	RCA	CD4015	
♦SW4016	RCA	CD4016	
		CD4066	
♦SW4017	RCA	CD4017	
♦SW4019	RCA	CD4019	
♦SW4020	RCA	CD4020	
♦SW4021	RCA	CD4021	
♦SW4023	RCA	CD4023	
♦SW4024	RCA	CD4024	
♦SW4025	RCA	CD4025	
♦SW4027	RCA	CD4027	
♦SW4028	RCA	CD4028	
♦SW4029	RCA	CD4029	
♦SW4030	RCA	CD4030	
♦SW4030	RCA	CD4070	
♦SW4049	RCA	CD4049	
♦SW4050	RCA	CD4050	
♦SW705-1	Motorola	MC853	
	TI	SN159093	
♦SW705-2	Motorola	MC853	
	TI	SN158093	
♦SW706-1	TI	SN15952	
♦SW706-2	Motorola	MC852	
		MC952	
	TI	SN15852	
♦SW708-1	Motorola	MC956	
	TI	SN15956	
♦SW708-2	Motorola	MC856	
	TI	SN15856	
♦SW709-1	Motorola	MC955	
	TI	SN15955	
♦SW709-2	Motorola	MC855	
	TI	SN15855	
♦SW930-1	Motorola	MC930	
	TI	SN15930	
♦SW930-2	Motorola	MC830	
	TI	SN15830	
♦SW932-1	Motorola	MC932	
	TI	SN15932	
♦SW932-2	Motorola	MC832	
	TI	SN15832	
♦SW933-1	Motorola	MC933	
	TI	SN15933	
♦SW933-2	Motorola	MC833	
	TI	SN15833	
♦SW935-1	Motorola	MC940	
	TI	SN15935	
♦SW935-2	Motorola	MC840	
	TI	SN15835	
♦SW936-1	Motorola	MC936	
	TI	SN15936	
♦SW936-2	Motorola	MC836	
	TI	SN15836	
♦SW937-1	Motorola	MC937	
	TI	SN15937	
♦SW937-2	Motorola	MC837	
	TI	SN15837	
♦SW941-1	Motorola	MC941	
	TI	SN15941	
♦SW941-2	Motorola	MC841	
	TI	SN15841	
♦SW944-1	Motorola	MC944	
	TI	SN15944	
♦SW944-2	Motorola	MC844	
	TI	SN15844	
♦SW945-2	TI	SN15845	
♦SW945-1	Motorola	MC945	
	TI	SN15945	
♦SW945-2	Motorola	MC845	
♦SW946-1	Motorola	MC946	
	TI	SN15946	
♦SW946-2	Motorola	MC846	
	TI	SN15846	
♦SW948-1	Motorola	MC948	
	TI	SN15948	
♦SW948-2	Motorola	MC848	
	TI	SN15848	
♦SW949-1	Motorola	MC949	
	TI	SN15949	
♦SW949-2	Motorola	MC649	
	TI	SN15849	
♦SW950-1	Motorola	MC950	
	TI	SN15950	
♦SW950-2	Motorola	MC850	
	TI	SN15850	
♦SW951-1	Motorola	MC951	
	TI	SN15951	
♦SW951-2	Motorola	MC851	
	TI	SN15851	
♦SW957-1	Motorola	MC957	
	TI	SN15957	
♦SW957-2	Motorola	MC857	
	TI	SN15857	
♦SW958-1	Motorola	MC958	
	TI	SN15958	
♦SW958-2	Motorola	MC858	
	TI	SN15858	
♦SW961-1	Motorola	MC961	
	TI	SN15961	
♦SW961-2	Motorola	MC861	
♦SW961-2	TI	SN15861	
♦SW962-1	Motorola	MC962	
	TI	SN15962	
♦SW962-2	Motorola	MC862	
	TI	SN15862	
♦SW963-1	Motorola	MC963	
	TI	SN15963	
♦SW963-2	Motorola	MC863	
	TI	SN15863	
♦1001	Motorola	MC1001	
♦1004	Motorola	MC1004	
♦1006	Motorola	MC1006	
♦1007	Motorola	MC1007	
♦1010	Motorola	MC1010	
♦1011	Motorola	MC1011	
♦1013	Motorola	MC1013	
♦1014	Motorola	MC1014	
♦1015	Motorola	MC1015	
♦1016	Motorola	MC1016	
♦1017	Motorola	MC1017	
♦1018	Motorola	MC1018	
♦1019	Motorola	MC1019	
♦1020	Motorola	MC1020	
♦1021	Motorola	MC1021	
♦1024	Motorola	MC1024	
♦1025	Motorola	MC1025	
♦1029	Motorola	MC1029	
♦1030	Motorola	MC1030	
♦1031	Motorola	MC1031	
♦1033	Motorola	MC1033	
♦1201	Motorola	MC1201	
♦1202	Motorola	MC1202	
♦1203	Motorola	MC1203	
♦1204	Motorola	MC1204	
♦1205	Motorola	MC1205	
♦1206	Motorola	MC1206	
♦1207	Motorola	MC1207	
♦1208	Motorola	MC1208	
♦1209	Motorola	MC1209	
♦1210	Motorola	MC1210	
♦1211	Motorola	MC1211	
♦1213	Motorola	MC1213	
♦1214	Motorola	MC1214	
♦1215	Motorola	MC1215	
♦1216	Motorola	MC1216	
♦1217	Motorola	MC1217	
♦1218	Motorola	MC1218	
♦1219	Motorola	MC1219	
♦1220	Motorola	MC1220	
♦1221	Motorola	MC1221	
♦1224	Motorola	MC1224	
♦1225	Motorola	MC1225	
♦1230	Motorola	MC1230	
♦1231	Motorola	MC1231	
♦1233	Motorola	MC1233	

Synertek

SY1103	AMI	S1103A	
SY1103A	AMI	S1103A	
	intel	1103A	
	Rockwell	1103A	
SY1402	Signetics	2502	
SY1403	Signetics	2503	
SY1404	Signetics	2504	
SY21H02	Fairchild	3542	
SY21L02	Fairchild	2102L	
	Signetics	21L02	
SY2101	Fairchild	2102	
		21021	
	Signetics	2101	
SY2102	Signetics	21F02	
SY2111	Signetics	2111	
SY2112	Signetics	2112	
SY2114	Fairchild	2114	
	Intel	2114	
	TI	TMS4045	
SY2316A	Mostek	MK31000	
SY2316B	Mostek	MK34000	
SY2533	Signetics	2533	
SY6502	MOS	MCS6502	
	Rockwell	R6502	
SY6503	MOS	MCS6503	
	Rockwell	R6503	
SY6504	MOS	MCS6504	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Synertek (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
SY6504	Rockwell	R6504	
SY6505	MOS	MCS6505	
	Rockwell	R6505	
SY6512	MOS	MCS6512	
	Rockwell	R6512	
SY6514	MOS	MCS6514	
	Rockwell	R6514	
SY6515	MOS	MCS6515	
	Rockwell	R6515	
SY6520	MOS	MCS6520	
	Rockwell	R6520	
SY6522	MOS	MCS6522	
SY6530	MOS	MCS6530	
	Rockwell	R6530	
SY6532	MOS	MCS6532	
	Rockwell	R6532	

Teledyne Crystalonics

CDR125	Siliconix	D125	

Teledyne Philbrick

1321	Datel	AM-462-2	
	Harris	**HA-2625**	**692**
1322	Datel	AM-452-2	
	Harris	**HA-2525**	**680**
1323	**Harris**	**HA-2705**	**708**
1324	**Harris**	**HA-2505**	**672**
1430	Datel	AM-500C	
1431	**Harris**	**HA-2065A**	**664**
4551	Datel	MXD-807	
	Harris	**HI507A**	**424**
4552	Datel	MX-1606	
	Harris	**Hi506A**	**424**
4856	**Datel**	**SHM-IC-1**	**393**
	Harris	**HA-2425**	**746**

Teledyne Semiconductor

Manufacturer Device	Replacement Source	Device	IC Master Page
♦D555	Exar	XR2556	
♦LM101	AD	AD101	
	AMD	LM101	
	Fairchild	μA101	
	Intersil	LM101	
	Motorola	LM101	
	National	LM101	
	RCA	CA101	
	Signetics	LM101	
	Silicon G	SG101	
	Siliconix	LM101	
	TI	LM101	
♦LM104	Motorola	LM104	
	Silicon G	SG104	
	TI	LM104	
♦LM105	AMD	LM105	
	Fairchild	μA105	
	Intersil	LM105	
	Motorola	LM105	
	National	LM105	
	Raytheon	LM105	
	Silicon G	SG105	
	TI	LM105	
♦LM107	AMD	LM107	
	Fairchild	μA107	
	Intersil	LM107	
	Motorola	LM107	
	National	LM107	
	Raytheon	LM107	
	RCA	CA107	
	Signetics	LM107	
	Silicon G	SG107	
	TI	LM107	
♦LM108	AD	AD108	
	Motorola	LM108	
	RCA	CA108	
	Silicon G	SG108	
♦LM111	AMD	LM111	
	Fairchild	μA111	
	Intersil	LM111	
♦LM111	Motorola	MLM111	
	Raytheon	LM111	
	RCA	CA111	
	Signetics	LM111	
	Silicon G	SG111	
	TI	LM111	
♦LM124	Motorola	LM124	
	Raytheon	LM124	
	RCA	CA124	
	Signetics	LM124	
	Silicon G	SG124	
	TI	LM124	
♦LM139	Motorola	LM139	
	Raytheon	LM139	
	RCA	CA139	
	Silicon G	SG139	
	TI	LM139	
♦LM201	AD	AD201	
	AMD	LM201	
	Fairchild	μA201	
	Intersil	LM201	
	Motorola	LM201	
	National	LM201	
	RCA	CA201	
	Signetics	LM201	
	Silicon G	SG201	
	TI	LM201	
♦LM204	Fairchild	μA204	
	Motorola	LM204	
	Raytheon	LM204	
	Silicon G	SG204	
	TI	LM204	
♦LM205	AMD	LM205	
	Fairchild	μA205	
	Intersil	LM205	
	Motorola	LM205	
	National	LM205	
	Raytheon	LM205	
	Silicon G	SG205	
	TI	LM205	
♦LM207	AMD	LM207	
	Fairchild	μA207	
	Intersil	LM207	
	Motorola	LM207	
	Raytheon	LM207	
	RCA	CA207	
	Signetics	LM207	
	Silicon G	SG207	
	TI	LM207	
♦LM208	Motorola	LM208	
	National	LM208	
	RCA	CA208	
	Silicon G	SG208	
♦LM211	AMD	LM211	
	Fairchild	μA211	
	Intersil	LM211	
	Motorola	LM211	
	National	LM211	
	Raytheon	LM211	
	RCA	CA211	
	Signetics	LM211	
	Silicon G	SG211	
	TI	LM211	
♦LM224	Motorola	LM224	
	Raytheon	LM224	
	RCA	CA224	
	Signetics	LM224	
	Silicon G	SG224	
	TI	LM224	
♦LM239	Motorola	LM239	
	Raytheon	LM239	
	RCA	CA239	
	Silicon G	SG239	
	TI	LM239	
♦LM301	AD	AD301	
	AMD	LM301	
	Fairchild	μA301	
	Intersil	LM301	
	Motorola	LM301	
	National	LM301	
	RCA	CA301	
	Signetics	LM301	
	Silicon G	SG301	
	TI	LM301	
♦LM304	Fairchild	μA304	
	Motorola	LM304	
♦LM304	Raytheon	LM304	
	Silicon G	SG304	
	TI	LM304	
♦LM305	AMD	LM305	
	Fairchild	μA305	
	Intersil	LM305	
	Motorola	LM305	
	National	LM305	
	Silicon G	SG305	
	TI	LM305	
♦LM307	AMD	LM307	
	Fairchild	μA307	
	Intersil	LM307	
	Motorola	LM307	
	National	LM307	
	Raytheon	LM307	
	RCA	CA307	
	Signetics	LM307	
	Silicon G	SG307	
	TI	LM307	
♦LM308	AMD	LM308	
	Fairchild	μA308	
	Motorola	LM308	
	National	LM308	
	Signetics	LM308	
	Silicon G	SG308	
♦LM311	AMD	LM311	
	Fairchild	μA311	
	Intersil	LM311	
	Motorola	LM311	
	National	LM311	
	Raytheon	LM311	
	RCA	CA311	
	Signetics	LM311	
	Silicon G	SG311	
	TI	LM311	
♦LM324	Motorola	LM324	
	National	LM324	
	Raytheon	LM324	
	RCA	CA324	
	Signetics	LM324	
	Silicon G	SG324	
	TI	LM324	
♦LM339	National	LM339	
	RCA	CA339	
	Silicon G	SG339	
	TI	LM339	
♦LM376	Fairchild	μA376	
♦MM54C00	Harris	HD54C00	
♦MM54C02	Harris	HD54C02	
	National	MM54C02	
♦MM54C04	Harris	HD54C04	
	National	MM54C04	
♦MM54C10	Harris	HD54C10	
	National	MM54C10	
♦MM54C107	Harris	HD54C107	
	National	MM54C107	
♦MM54C151	Harris	HD54C151	
	National	MM54C151	
♦MM54C154	Harris	HD54C154	
	National	MM54C154	
♦MM54C157	Harris	HD54C157	
	National	MM54C157	
♦MM54C160	Harris	HD54C160	
	National	MM54C160	
♦MM54C161	Harris	HD54C161	
	National	MM54C161	
♦MM54C162	Harris	HD54C162	
	National	MM54C162	
♦MM54C163	Harris	HD54C163	
	National	MM54C163	
♦MM54C164	Harris	HD54C164	
	National	MM54C164	
♦MM54C173	Harris	HD54C173	
	National	MM54C173	
♦MM54C192	Harris	HD54C192	
	National	MM54C192	
♦MM54C193	Harris	HD54C193	
	National	MM54C193	
♦MM54C195	Harris	HD54C195	
♦MM54C20	Harris	HD54C20	
	National	MM54C20	
♦MM54C200	**National**	**MM54C200**	**1355**
♦MM54C42	Harris	HD54C42	
	National	MM54C42	
♦MM54C48	National	MM54C48	
♦MM54C73	Harris	HD54C73	
	National	MM54C73	
♦MM54C74	Harris	HD54C74	
	National	MM54C74	
♦MM54C76	Harris	HD54C76	
	National	MM54C76	
♦MM54C86	Harris	HD54C86	
	National	MM54C86	
♦MM54C89	Harris	HD54C89	
	National	**MM54C89**	**1352**
♦MM54C95	Harris	HD54C95	
	National	MM54C95	
♦MM74C00	Harris	HD74C00	
	National	MM74C00	
	RCA	CD4011	
♦MM74C02	Harris	HD74C02	
	National	MM74C02	
	RCA	CD4001	
♦MM74C04	Harris	HD74C04	
	National	MM74C04	
	RCA	CD4069	
♦MM74C10	Harris	HD74C10	
	National	MM74C10	
	RCA	CD4023	
♦MM74C107	Harris	HD74C107	
	National	MM74C107	
♦MM74C14	National	MM74C14	
♦MM74C151	Harris	HD74C151	
	National	MM74C151	
♦MM74C154	Harris	HD74C154	
	National	MM74C154	
♦MM74C157	Harris	HD74C157	
	National	MM74C157	
♦MM74C160	Harris	HD74C160	
	National	MM74C160	
♦MM74C161	Harris	HD74C161	
	National	MM74C161	
♦MM74C162	Harris	HD74C162	
	National	MM74C162	
♦MM74C163	Harris	HD74C163	
	National	MM74C163	
♦MM74C164	Harris	HD74C164	
	National	MM74C164	
♦MM74C173	Harris	HD74C173	
	National	MM74C173	
	RCA	CD4076	
♦MM74C192	Harris	HD74C192	
	National	MM74C192	
	RCA	CD40192	
♦MM74C193	Harris	HD74C193	
	National	MM74C193	
	RCA	CD40193	
♦MM74C195	Harris	HD74C195	
	National	MM74C195	
♦MM74C20	Harris	HD74C20	
	National	MM74C20	
	RCA	CD4012	
♦MM74C200	**National**	**MM74C200**	**1355**
♦MM74C42	Harris	HD74C42	
	National	MM74C42	
	RCA	CD4028	
♦MM74C48	Harris	HD74C48	
	National	MM74C48	
♦MM74C73	Harris	HD74C73	
	National	MM74C73	
♦MM74C74	Harris	HD74C74	
	National	MM74C74	
	RCA	CD4013	
♦MM74C76	Harris	HD74C76	
	National	MM74C76	
	RCA	CD4027	
♦MM74C86	Harris	HD74C86	
	National	MM74C86	
♦MM74C89	Harris	HD74C89	
	National	**MM74C89**	**1352**
♦MM74C95	Harris	HD74C95	
	National	MM74C95	
♦TP1301	AD	AD509	
♦TP1322	AD	AD509	
♦TP301	AD	AD507	
♦TP321	AD	AD507	
♦1458	Exar	XR1458	
	Fairchild	μA1458	
	Harris	**HA-2655**	**704**
	Motorola	MC1458	
	National	LM1458	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Teledyne Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
♦1458	Raytheon	RC1458	
	RCA	CA1458	
	Signetics	MC1458	
	Silicon G	SG1458	
	TI	MC1458	
♦1556	Fairchild	μA1558	
	Harris	HA-2650	704
	Motorola	MC1558	
	National	LM1558	
	RCA	CA1458	
	Signetics	MC1558	
	Silicon G	SG1558	
	TI	MC1558	
♦555	Exar	XR555	
	Motorola	MC1455	
	National	LM555	
	Silicon G	SG555	
	TI	NE555	
		SE555	
♦556	Exar	XR556	
	Motorola	MC3456	
	Silicon G	SG556	
	TI	NE556	
		SE556	
♦558	Silicon G	SG558	
♦709	Fairchild	μA709	
	Motorola	MC1709	
	Raytheon	RC709	
	Signetics	μA709	
	TI	μA709	
♦710	Fairchild	μA710	
	Motorola	MC1710	
	National	LM710	
	Raytheon	RC710	
	RCA	CA710	
	Signetics	μA710	
	Silicon G	SG710	
	TI	μA710	
♦711	Fairchild	μA711	
	Motorola	MC1711	
	National	LM711	
	Raytheon	RC711	
	RCA	CA711	
	Silicon G	SG711	
	TI	μA711	
♦723	AMD	723	
	Intersil	723	
	Motorola	MC1723	
	National	LM723	
	Raytheon	RC723	
	Signetics	μA723	
	Silicon G	SG723	
	TI	μA723	
♦741	AD	AD741	
	AMD	741	
	Fairchild	μA741	
	Intersil	741	
	Motorola	MC1741	
	National	LM741	
	Raytheon	RC741	
	RCA	CA741	
	Signetics	μA741	
	Silicon G	SG741	
	TI	μA741	
♦747	AMD	747	
	Motorola	MC1747	
	National	LM747	
	Raytheon	RC747	
	RCA	CA747	
	Signetics	μA747	
	Silicon G	SG747	
♦748	Intersil	748	
	Motorola	MC1748	
	National	LM748	
	Raytheon	RC748	
	RCA	CA748	
	Signetics	μA748	
	TI	μA748	
♦8700	Datel	ADC-EK8B	
♦8701	Datel	ADC-EK10B	
♦8702	Datel	ADC-EK12B	
8750	Datel	ADC-EK12D	
9400C	Datel	VFC-1	

Telefunken

Manufacturer Device	Replacement Source	Device	IC Master Page
TCA830	SGS	TCA830	
TDA1083	Sprague	ULN-2204	
TDA440	Plessey	TDA440	
	SGS	TDA440	
TL1723	Signetics	μA723	
TL3723	Signetics	μA723	

Texas Instruments

Manufacturer Device	Replacement Source	Device	IC Master Page
μA702	Fairchild	μA702	
	Motorola	MC1712	
	Raytheon	RC702	
		RM702	
μA709	Fairchild	μA709	
	Motorola	MC1709	
	National	LM709	
	Raytheon	RC709	
		RM709	
	Signetics	μA709	
μA710	Fairchild	μA710	
	Motorola	MC1710	
	National	LM710	
	Raytheon	RC710	
		RM710	
	Signetics	μA710	
	Silicon G	SG710	
μA711	Fairchild	μA711	
	Motorola	MC1711	
	National	LM711	
	Raytheon	RC711	
		RM711	
	Signetics	μA711	
	Silicon G	SG711	
μA723	AMD	723	
	Fairchild	μA723	
	Intersil	723	
	Motorola	MC1723	
	National	LM723	
	Raytheon	RC723	
		RM723	
	RCA	CA723	
	Signetics	μA723	
	Silicon G	SG723	
μA733	AMD	733	
	Fairchild	μA733	
	Motorola	MC1733	
	National	LM733	
	Raytheon	RC733	
		RM733	
	Signetics	μA733	
	Silicon G	SG733	
μA741	AMD	741	
	Fairchild	μA741	
	Intersil	741	
	Motorola	MC1741	
	National	LM741	
	PMI	**OP-02**	**839**
		PM741	**839**
		SSS741	**839**
	Raytheon	RC741	
		RM741	
	RCA	CA741	
	Signetics	μA741	
	Silicon G	SG741	
μA747	AMD	747	
	Fairchild	μA747	
	Motorola	MC1747	
	National	LM747	
	PMI	**PM747**	**844**
		SSS747	**844**
	Raytheon	RC747	
		RM747	
	RCA	CA747	
	Silicon G	SG747	
μA748	AMD	748	
	Fairchild	μA748	
	Intersil	748	
	Motorola	MC1748	
	National	LM748	
	Raytheon	RC748	
μA748	Raytheon	RM748	
	RCA	CA748	
	Signetics	μA748	
	Silicon G	SG748	
μA777	Fairchild	μA777	
	Intersil	777	
	Silicon G	SG777	
μA78L02	Signetics	μA78L02	
μA78L05	Signetics	μA78L05	
μA78L06	Signetics	μA78L06	
μA78L08	Signetics	μA78L08	
μA78L12	Signetics	μA78L12	
μA78L15	Signetics	μA78L15	
μA78M05	Signetics	μA78M05	
μA78M06	Signetics	μA78M06	
μA7805	Signetics	μA7805	
μA7806	Signetics	μA7806	
μA7808	Signetics	μA7808	
μA7812	Signetics	μA7812	
μA7815	Signetics	μA7815	
μA7818	Signetics	μ7818	
μA7824	Signetics	μA7824	
μA79M05	Signetics	μA79M05	
μA79M06	Signetics	μA79M06	
μA79M08	Signetics	μA79M08	
μA79M12	Signetics	μA79M12	
μA79M15	Signetics	μA79M15	
μA79M24	Signetics	μA79M24	
μA7905	Signetics	μA7905	
μA7906	Signetics	μA7906	
μA7908	Signetics	μA7908	
μA7912	Signetics	μA7912	
μA7918	Signetics	μA7918	
μA7924	Signetics	μA7924	
LF155	AMD	LF155	
	Fairchild	μAF155	
	Intersil	LF155	
	Motorola	LF155	
	National	**LF155**	**786**
	PMI	**PM155**	**871**
	Raytheon	LF155	
	Signetics	LF155	
LF156	AMD	LF156	
	Fairchild	μAF156	
	Intersil	LF156	
	Motorola	LF156	
	National	**LF156**	**786**
	PMI	**PM156**	**877**
	Raytheon	LF156	
	Signetics	LF156	
LF157	AMD	LF157	
	Fairchild	μAF157	
	Intersil	LF157	
	Motorola	LF157	
	National	**LF157**	**786**
	PMI	**PM157**	**882**
	Raytheon	LF157	
	Signetics	LF157	
LF255	AMD	LF255	
	Fairchild	μAF255	
	Intersil	LF255	
	Motorola	LF255	
	National	**LF255**	**786**
	PMI	**PM255**	**871**
	Raytheon	LF255	
	Signetics	LF255	
LF256	AMD	LF256	
	Fairchild	μAF256	
	Intersil	LF256	
	Motorola	LF256	
	National	**LF256**	**786**
	PMI	**PM256**	**877**
	Raytheon	LF256	
	Signetics	LF256	
LF257	AMD	LF257	
	Fairchild	μAF257	
	Intersil	LF257	
	Motorola	LF257	
	National	**LF257**	**786**
	PMI	**PM257**	**882**
	Raytheon	LF257	
	Signetics	LF257	
LF355	AMD	LF355	
	Fairchild	μAF355	
	Intersil	LF355	
	Motorola	LF355	
LF355	**National**	**LF355**	**786**
	PMI	**PM355**	**871**
	Raytheon	LF355	
	Signetics	LF355	
LF356	AMD	LF356	
	Fairchild	μAF356	
	Intersil	LF356	
	Motorola	LF356	
	National	**LF356**	**786**
	PMI	**PM356**	**877**
	Raytheon	LF356	
	Signetics	LF356	
LF357	AMD	LF357	
	Fairchild	μAF357	
	Intersil	LF357	
	Motorola	LF357	
	National	**LF357**	**786**
	PMI	**PM357**	**882**
	Raytheon	LF357	
	Signetics	LF357	
LM101	AMD	LM101	
	Fairchild	μA101	
	Intersil	LM101	
	Motorola	LM101	
	National	LM101	
	RCA	CA101	
	Signetics	LM101	
	Silicon G	SG101	
LM104	Motorola	LM104	
	Silicon G	SG104	
LM105	AMD	LM105	
	Intersil	LM105	
	Motorola	LM105	
	National	LM105	
	Raytheon	LM105	
	Silicon G	SG105	
LM106	AMD	LM106	
LM107	AMD	LM107	
	Fairchild	μA107	
	Intersil	LM107	
	Motorola	LM107	
	National	LM107	
	Raytheon	LM107	
	RCA	CA107	
	Signetics	LM107	
	Silicon G	SG107	
LM108	AMD	LM108	
LM111	AMD	LM111	
	Intersil	LM111	
	National	LM111	
	Raytheon	LM111	
	RCA	CA111	
	Signetics	LM111	
	Silicon G	SG111	
LM118	AMD	LM118	
LM301	AMD	LM301	
	Fairchild	μA301	
	Intersil	LM301	
	Motorola	LM301	
	National	LM301	
	Raytheon	LM301	
	RCA	CA301	
	Signetics	LM301	
	Silicon G	SG301	
LM304	Fairchild	μA304	
	Motorola	LM304	
	Silicon G	SG304	
LM305	AMD	LM305	
	Fairchild	μA305	
	Intersil	LM305	
	Motorola	LM305	
	Raytheon	LM305	
	Silicon G	SG305	
LM306	AMD	LM306	
LM307	AMD	LM307	
	Fairchild	μA307	
	Intersil	LM307	
	Motorola	LM307	
	National	LM307	
	Raytheon	LM307	
	RCA	CA307	
	Signetics	LM307	
	Silicon G	SG307	
LM308	AMD	LM308	
LM311	AMD	LM311	
	Fairchild	μA311	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Texas Instruments (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
LM311	Intersil	LM311	
	Motorola	LM311	
	Raytheon	LM311	
	RCA	CA311	
	Signetics	LM311	
	Silicon G	SG311	
LM318	AMD	LM318	
LM340-12	**National**	**LM340-12**	**806**
LM340-15	**National**	**LM340-15**	**806**
LM340-18	**National**	**LM340-18**	**806**
LM340-24	**National**	**LM340-24**	**806**
LM340-5	**National**	**LM340-5**	**806**
LM340-6	**National**	**LM340-6**	**806**
LM340-8	**National**	**LM340-8**	**806**
LM376	Fairchild	μA376	
MC1458	Exar	XR1458	
	Fairchild	μA1458	
	Harris	**HA-2655**	**704**
	Motorola	MC1458	
	National	LM1458	
	PMI	**OP-14**	**844**
		SSS1458	**844**
	Raytheon	RC1458	
		RC4558	
	RCA	CA1458	
	Signetics	MC1458	
	Silicon G	SG1458	
MC1489A	Signetics	MC1489A	
MC1558	Exar	XR1558	
	Fairchild	μA1558	
	Harris	**HA-2650**	**704**
	Motorola	MC1558	
	National	LM1558	
	PMI	**PM1558**	**844**
		SSS1558	**844**
	Raytheon	RM1558	
		RM4558	
	RCA	CA1558	
	Silicon G	SG1558	
NE555	AMD	NE555	
	Exar	XR555	
	Fairchild	μA555	
	Intersil	NE555	
	Motorola	MC1455	
	Raytheon	RC555	
	RCA	CA555	
	Signetics	NE555	
	Silicon G	SG555	
NE556	Exar	XR556	
	Fairchild	μA556	
	Motorola	MC3456	
	Silicon G	SG556	
RC4136	Exar	XR4136	
	Raytheon	RC4136	
RC4558	Exar	XR4558	
	Motorola	MC4558	
	Raytheon	RC4558	
RM4136	Exar	XR4136	
	Raytheon	RC4136	
RM4558	Exar	XR4558	
	Motorola	MC4558	
	Raytheon	RM4558	
SE555	AMD	SE555	
	Exar	XR555M	
	Intersil	SE555	
	Motorola	MC1555	
	Raytheon	RM555	
	RCA	CA555	
	Signetics	SE555	
	Silicon G	SG555	
SG1524	Exar	XR1524	
SG2524	Exar	XR2524	
SG3624	Exar	XR3524	
♦SN10101	Motorola	MC10101	
♦SN10102	Motorola	MC10102	
	NEC America	μPB10142	
	Plessey	SP10142	
♦SN10104	Motorola	MC10104	
♦SN10105	Motorola	MC10105	
♦SN10106	Motorola	MC10106	
♦SN10107	Motorola	MC10107	
♦SN10109	Motorola	MC10109	
♦SN10110	Motorola	MC10110	
♦SN10111	Motorola	MC10111	
♦SN10115	Motorola	MC10115	
♦SN10116	Motorola	MC10116	
♦SN10117	Motorola	MC10117	
♦SN10118	Motorola	MC10118	
♦SN10119	Motorola	MC10119	
♦SN10121	Motorola	MC10121	
♦SN10130	Motorola	MC10130	
♦SN10131	Motorola	MC10131	
♦SN10133	Motorola	MC10133	
SN10140	Plessey	SP10140	
	Signetics	10140	
SN10144	Motorola	MC10144	
	NEC America	μPB10144	
	Plessey	SP10144	
	Raytheon	RC10144	
	Signetics	10144	
SN10147	Fairchild	F10405	
SN10148	Hitachi	HD10148	
	NEC America	μPB10148	
	Plessey	SP10148	
	Signetics	10148	
♦SN10160	Motorola	MC10160	
♦SN10161	Motorola	MC10161	
SN10164	Fairchild	F10164	
	Hitachi	HD10164	
	Motorola	MC10164	
	NEC America	μPB10164	
	Plessey	SP10164	
	Signetics	10164	
SN10174	Fairchild	F10174	
	Hitachi	HD10174	
	Motorola	MC10174	
	NEC America	μPB10174	
	Plessey	SP10174	
	Signetics	10174	
SN10175	Motorola	MC10175	
♦SN10179	Motorola	MC10179	
♦SN10181	Motorola	MC10181	
SN151800	Motorola	MC1800	
	National	DM1800	
SN151801	Motorola	MC1801	
	National	DM1801	
SN151802	Motorola	MC1802	
SN151803	Motorola	MC1803	
SN151804	Motorola	MC1804	
SN151805	Motorola	MC1805	
SN151806	Motorola	MC1806	
SN151807	Motorola	MC1807	
SN151808	Motorola	MC1808	
SN151809	Motorola	MC1809	
SN151810	Motorola	MC1810	
SN151811	Motorola	MC1811	
SN151812	Motorola	MC1812	
SN151820	Motorola	MC1820	
SN151900	Motorola	MC1900	
SN151901	Motorola	MC1901	
SN151902	Motorola	MC1902	
SN151904	Motorola	MC1904	
SN151905	Motorola	MC1905	
SN151906	Motorola	MC1906	
SN151907	Motorola	MC1907	
SN151908	Motorola	MC1908	
SN151909	Motorola	MC1909	
SN151910	Motorola	MC1910	
SN151911	Motorola	MC1911	
SN151912	Motorola	MC1912	
SN151920	Motorola	MC1920	
SN158093	Motorola	MC853	
	National	DM9093	
SN158094	Motorola	MC856	
	National	DM9094	
SN158097	Motorola	MC855	
	National	DM9097	
SN158099	Motorola	MC852	
	National	DM9099	
SN15830	Hitachi	HD2204	
	Motorola	MC830	
	National	DM930	
SN15831	Motorola	MC831	
SN15832	Hitachi	HD2201	
	Motorola	MC832	
	National	DM932	
SN15833	Hitachi	HD2202	
	Motorola	MC833	
	National	DM933	
SN15834	Motorola	MC834	
SN15835	Motorola	MC840	
	National	DM935	
SN15836	Hitachi	HD2206	
	Motorola	MC836	
	National	DM936	
SN15837	Motorola	MC837	
	National	DM937	
SN15838	Motorola	MC835	
SN15844	Hitachi	HD2209	
	Motorola	MC844	
	National	DM944	
SN15845	Hitachi	HD2205	
	Motorola	MC845	
	National	DM945	
SN15846	Hitachi	HD2203	
	Motorola	MC846	
	National	DM946	
SN15848	Motorola	MC848	
	National	DM948	
SN15849	Motorola	MC849	
	National	DM949	
SN15850	Motorola	MC850	
SN15851	Motorola	MC851	
SN15857	Motorola	MC857	
	National	DM957	
SN15858	Motorola	MC858	
	National	DM958	
SN15861	Motorola	MC861	
	National	DM961	
SN15862	Hitachi	HD2207	
	Motorola	MC862	
	National	DM962	
SN15863	Motorola	MC863	
	National	DM963	
SN159093	Motorola	MC953	
	Raytheon	RM993	
SN159094	Motorola	MC956	
	Raytheon	RM994	
SN159097	Motorola	MC955	
	Raytheon	RM997	
SN159099	Motorola	MC952	
	Raytheon	RM999	
SN15930	Motorola	MC930	
	Raytheon	RM930	
SN15931	Motorola	MC931	
	Raytheon	RM931	
SN15932	Motorola	MC932	
	Raytheon	RM932	
SN15933	Motorola	MC933	
	Raytheon	RM933	
SN15934	Motorola	MC934	
	Raytheon	RM934	
SN15935	Motorola	MC940	
	Raytheon	RM935	
SN15936	Motorola	MC936	
	Raytheon	RM936	
SN15937	Motorola	MC937	
	Raytheon	RM937	
SN15938	Motorola	MC935	
SN15944	Motorola	MC944	
	Raytheon	RM944	
SN15945	Motorola	MC945	
	Raytheon	RM945	
SN15946	Motorola	MC946	
	Raytheon	RM946	
SN15948	Motorola	MC948	
	Raytheon	RM948	
SN15949	Motorola	MC949	
	Raytheon	RM949	
SN15950	Motorola	MC950	
	Raytheon	RM950	
SN15951	Motorola	MC951	
	Raytheon	RM951	
SN15957	Motorola	MC957	
SN15958	Motorola	MC958	
SN15961	Motorola	MC961	
	Raytheon	RM961	
SN15962	Motorola	MC962	
	Raytheon	RM962	
SN15963	Motorola	MC963	
	Raytheon	RM963	
SN29000	Fairchild	9000	
SN29001	Fairchild	9001	
	ITT	ITT9001	
SN29002	ITT	ITT9002	
SN29002	National	DM9002	
SN29003	ITT	ITT9003	
	National	DM9003	
SN29004	National	DM9004	
SN29005	ITT	ITT9005	
	National	DM9005	
SN29006	National	DM9006	
SN29008	ITT	ITT9008	
	National	DM9008	
SN29009	ITT	ITT9009	
	National	DM9009	
SN29012	ITT	ITT9012	
	National	DM9012	
SN29016	ITT	ITT9016	
	National	DM9016	
SN29024	National	DM8024	
SN29300	AMD	9300	
	National	DM8300	
	Raytheon	RM9300	
SN29301	AMD	9301	
	Fairchild	9301	
	National	DM8301	
		DM9301	
SN29308	AMD	9308	
	Fairchild	9308	
	Raytheon	RC9308	
		RM9308	
SN29309	AMD	9309	
	Fairchild	9309	
	National	DM8309	
SN29310	AMD	9310	
	National	DM8310	
	Raytheon	RM9310	
SN29311	AMD	9311	
	National	DM8311	
	Raytheon	RM9311	
SN29312	AMD	9312	
	ITT	ITT9312	
	National	DM8312	
	Raytheon	RC9312	
		RM9312	
SN29316	AMD	9316	
	National	DM8316	
	Raytheon	RM9316	
SN29318	AMD	9318	
	National	DM8318	
SN29322	AMD	9322	
	National	DM8322	
SN29334	National	DM8334	
SN29601	AMD	9601	
	ITT	ITT9601	
	Motorola	MC9601	
	National	DM8601	
	Raytheon	RF9601	
SN29602	National	DM8602	
	Raytheon	RM9322	
SN39000	Fairchild	9000	
SN39001	Fairchild	9001	
SN39024	National	DM9024	
SN39300	National	DM9300	
SN39301	Fairchild	9301	
	National	DM9301	
SN39308	Fairchild	9308	
SN39309	Fairchild	9309	
	National	DM9309	
SN39310	National	DM9310	
SN39311	National	DM9311	
SN39312	Fairchild	9312	
	National	DM9312	
SN39316	National	DM9316	
SN39318	National	DM9318	
SN39322	National	DM9322	
SN39334	National	DM9334	
SN39601	National	DM9601	
SN39602	National	DM9602	
SN429301	ITT	ITT9301	
♦SN52L022	TI	TL022M	
♦SN52L044	TI	TL044M	
♦SN52101	TI	LM101	
SN52104	TI	LM104	
♦SN52105	TI	LM105	
♦SN52106	TI	LM106	
♦SN52107	TI	LM107	
♦SN52108	AMD	LM108	
	Intersil	LM108	
	Motorola	LM108	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
♦SN52108	National	LM108	
	Raytheon	LM108	
	RCA	CA108	
	Silicon G	SG108	
♦SN52109	TI	LM109	
SN52110	AMD	LM110	
	Intersil	LM110	
	Motorola	LM110	
	National	LM110	
	Silicon G	SG110	
♦SN52111	TI	LM111	
♦SN52118	TI	LM118	
SN52197	Signetics	S8291	
♦SN52506	TI	TL506	
♦SN52510	TI	TL510	
♦SN52514	TI	TL514	
♦SN52555	TI	SE555	
♦SN52558	TI	MC1558	
♦SN52702	TI	TL702	
♦SN52702A	TI	μA702	
♦SN52709	TI	μA709	
♦SN52710	TI	TL710	
♦SN52711	TI	μA711	
♦SN52723	TI	μA723	
♦SN52733	TI	μA733	
♦SN52741	TI	μA741	
♦SN52747	TI	μA747	
♦SN52748	TI	μA748	
♦SN52771	Signetics	MC1556	
♦SN52777	TI	μA777	
♦SN52810	TI	TL810	
♦SN52811	TI	TL811	
♦SN52820	TI	TL820	
SN54H00	Fairchild	54H00	
		9H00	
	ITT	ITT54H00	
	National	DM54H00	
	Raytheon	54H00	
	Signetics	54H00	
SN54H01	Fairchild	54H01	
		9H01	
	ITT	ITT54H01	
	National	DM54H01	
	Raytheon	54H01	
	Signetics	54H01	
SN54H04	Fairchild	54H04	
		9H04	
	ITT	ITT54H04	
	National	DM54H04	
	Raytheon	54H04	
	Signetics	54H04	
SN54H05	Fairchild	**54H05**	
		9H05	
	ITT	ITT54H05	
	National	DM54H05	
	Raytheon	54H05	
	Signetics	54H05	
SN54H10	Fairchild	54H10	
		9H10	
	ITT	ITT54H10	
	National	DM54H10	
	Raytheon	54H10	
	Signetics	54H10	
SN54H101	Fairchild	54H101	
		9H101	
	Signetics	54H101	
SN54H102	Fairchild	54H102	
		9H102	
	Signetics	54H102	
SN54H103	Fairchild	54H103	
		9H103	
	National	DM54H103	
	Signetics	54H103	
SN54H106	Fairchild	54H106	
		9H106	
	National	DM54H106	
	Signetics	54H106	
SN54H108	Fairchild	54H108	
		9H108	
	National	DM54H108	
	Signetics	54H108	
SN54H11	Fairchild	54H11	
	ITT	ITT54H11	
SN54H11	National	DM54H11	
	Raytheon	54H11	
	Signetics	54H11	
SN54H15	Fairchild	54H15	
	Raytheon	54H15	
SN54H183	Fairchild	54H183	
		93H183	
SN54H20	Fairchild	54H20	
		9H20	
	ITT	ITT54H20	
	National	DM54H20	
	Raytheon	54H20	
	Signetics	54H20	
SN54H21	Fairchild	54H21	
		9H21	
	ITT	ITT54H21	
	National	DM54H21	
	Signetics	54H21	
SN54H22	Fairchild	54H22	
		9H22	
	National	DM54H22	
	Raytheon	54H22	
	Signetics	54H22	
SN54H30	Fairchild	54H30	
		9H30	
	ITT	ITT54H30	
	National	DM54H30	
	Signetics	54H30	
SN54H40	Fairchild	54H40	
		9H40	
	ITT	ITT54H40	
	National	DM54H40	
	Raytheon	54H40	
	Signetics	54H40	
SN54H50	Fairchild	54H50	
		9H50	
	ITT	ITT54H50	
	National	DM54H50	
	Signetics	54H50	
SN54H51	Fairchild	54H51	
		9H51	
	ITT	ITT54H51	
	National	DM54H51	
	Signetics	54H51	
SN54H52	Fairchild	54H52	
		9H52	
	National	DM54H52	
	Signetics	54H52	
SN54H53	Fairchild	54H53	
		9H53	
	ITT	ITT54H53	
	National	DM54H53	
	Signetics	54H53	
SN54H54	Fairchild	54H54	
		9H54	
	ITT	ITT54H54	
	National	DM54H54	
	Signetics	54H54	
SN54H55	Fairchild	54H55	
		9H55	
	National	DM54H55	
	Signetics	54H55	
SN54H60	Fairchild	54H60	
		9H60	
	ITT	ITT54H60	
	National	DM54H60	
	Signetics	54H60	
SN54H61	Fairchild	54H61	
		9H61	
	National	DM54H61	
	Signetics	54H61	
SN54H62	Fairchild	54H62	
		9H62	
	National	DM54H62	
	Signetics	54H62	
SN54H71	Fairchild	54H71	
		9H71	
	National	DM54H71	
	Signetics	54H71	
SN54H72	Fairchild	54H72	
		54H73	
		9H72	
	ITT	ITT54H72	
	National	DM54H72	
	Signetics	54H72	
SN54H73	Fairchild	54H73	
SN54H73	Fairchild	9H73	
	ITT	ITT54H73	
	National	DM54H73	
	Signetics	54H73	
SN54H74	Fairchild	54H74	
		9H74	
	ITT	ITT54H74	
	National	DM54H74	
	Raytheon	54H74	
	Signetics	54H74	
SN54H76	Fairchild	54H76	
		9H76	
	National	DM54H76	
	Signetics	54H76	
SN54H78	Fairchild	54H78	
		9H78	
	National	DM54H78	
SN54H87	Fairchild	54H87	
		93H87	
SN54LS00	Fairchild	54LS00	
	Motorola	SN54LS00	
	National	DM54LS00	
	Raytheon	54LS00	
	Signetics	54LS00	
SN54LS01	Fairchild	54LS01	
	National	DM54LS01	
	Raytheon	54LS01	
	Signetics	54LS01	
SN54LS02	Fairchild	54LS02	
	Motorola	SN54LS02	
	National	DM54LS02	
	Raytheon	54LS02	
	Signetics	54LS02	
SN54LS03	Fairchild	54LS03	
	Motorola	SN54LS03	
	National	DM54LS03	
	Raytheon	54LS03	
	Signetics	54LS03	
SN54LS04	Fairchild	54LS04	
	Motorola	SN54LS04	
	National	DM54LS04	
	Raytheon	54LS04	
	Signetics	54LS04	
SN54LS05	Fairchild	54LS05	
	Motorola	SN54LS05	
	National	DM54LS05	
	Raytheon	54LS05	
	Signetics	54LS05	
SN54LS08	Fairchild	54LS08	
	Motorola	SN54LS08	
	National	DM54LS08	
	Raytheon	54LS08	
	Signetics	54LS08	
SN54LS09	Fairchild	54LS09	
	Motorola	SN54LS09	
	National	DM54LS09	
	Raytheon	54LS09	
	Signetics	54LS09	
SN54LS10	Fairchild	54LS10	
	Motorola	SN54LS10	
	National	DM54LS10	
	Raytheon	54LS10	
	Signetics	54LS10	
SN54LS107	Fairchild	54LS107	
	Motorola	SN54LS107	
	National	DM54LS107	
	Raytheon	54LS107	
	Signetics	54LS107	
SN54LS109	Fairchild	54LS109	
	Motorola	SN54LS109	
	National	DM54LS109	
	Raytheon	54LS109	
	Signetics	54LS109	
SN54LS11	Fairchild	54LS11	
	Motorola	SN54LS11	
	National	DM54LS11	
	Raytheon	54LS11	
	Signetics	54LS11	
SN54LS112	Fairchild	54LS112	
	National	DM54LS112	
	Raytheon	54LS112	
	Signetics	54LS112	
SN54LS113	Fairchild	54LS113	
	National	DM54LS113	
	Raytheon	54LS113	
	Signetics	54LS113	
SN54LS114	Fairchild	54LS114	
	Motorola	SN54LS114	
	National	DM54LS114	
	Raytheon	54LS114	
	Signetics	54LS114	
SN54LS12	Fairchild	54LS12	
	National	DM54LS12	
	Raytheon	54LS12	
	Signetics	54LS12	
SN54LS122	National	DM54LS122	
	Raytheon	**54LS122**	**275**
SN54LS123	AMD	SN54LS123	
	National	DM54LS123	
	Raytheon	**54LS123**	**275**
SN54LS125A	Fairchild	54LS125	
	National	DM54LS125	
	Raytheon	54LS125	
	Signetics	54LS125	
SN54LS126A	Fairchild	54LS126	
	Motorola	SN54LS126	
	National	DM54LS126	
	Raytheon	54LS126	
	Signetics	54LS126	
SN54LS13	Motorola	SN54LS13	
	National	DM54LS13	
	Raytheon	**54LS13**	**264**
	Signetics	54LS13	
SN54LS132	Fairchild	54LS132	
	Motorola	SN54LS132	
	National	DM54LS132	
	Signetics	54LS132	
SN54LS136	Fairchild	54LS136	
	Motorola	SN54LS136	
	Raytheon	54LS136	
	Signetics	54LS136	
SN54LS138	AMD	SN54LS138	
	Fairchild	54LS138	
	Motorola	SN54LS138	
	National	DM54LS138	
	Raytheon	54LS138	
	Signetics	54LS138	
SN54LS139	AMD	SN54LS139	
	Fairchild	54LS139	
	Motorola	SN54LS139	
	National	DM54LS139	
	Raytheon	54LS139	
	Signetics	54LS139	
		74LS139	
SN54LS14	Fairchild	54LS14	
	Motorola	SN54LS14	
	National	DM54LS14	
	Raytheon	**54LS14**	**264**
	Signetics	54LS14	
SN54LS148	AMD	SN54LS148	
SN54LS15	Fairchild	54LS15	
	Motorola	SN54LS15	
	National	DM54LS15	
	Raytheon	54LS15	
	Signetics	54LS15	
SN54LS151	AMD	SN54LS151	
	Fairchild	54LS151	
	Motorola	SN54LS151	
	National	DM54LS151	
	Raytheon	54LS151	
	Signetics	54LS151	
SN54LS152	Fairchild	54LS152	
	Motorola	SN54LS152	
	Raytheon	54LS152	
SN54LS153	AMD	SN54LS153	
	Fairchild	54LS153	
	Motorola	SN54LS153	
	National	DM54LS153	
	Raytheon	54LS153	
	Signetics	54LS153	
SN54LS155	Fairchild	54LS155	
	Motorola	SN54LS155	
	National	DM54LS155	
	Raytheon	54LS156	
		74LS155	
SN54LS156	Fairchild	54LS156	
	Motorola	SN54LS156	
	National	DM54LS156	
	Raytheon	54LS156	
SN54LS157	AMD	SN54LS157	
	Fairchild	54LS157	
	Motorola	SN54LS157	

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Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN54LS157	National	DM54LS157	
	Raytheon	54LS157	
	Signetics	54LS157	
SN54LS158	AMD	SN54LS158	
	Fairchild	54LS158	
	Motorola	SN54LS158	
	National	DM54LS158	
	Raytheon	54LS158	
	Signetics	54LS158	
SN54LS160	AMD	SN54LS160	
	Fairchild	54LS160	
	Motorola	SN54LS160	
	National	DM54LS160	
	Raytheon	54LS160	
SN54LS161	AMD	SN54LS161	
	Fairchild	54LS161	
	Motorola	SN54LS161	
	National	DM54LS161	
	Raytheon	54LS161	
	Signetics	54LS161	
SN54LS162	AMD	SN54LS162	
	Fairchild	54LS162	
	Motorola	SN54LS162	
	National	DM54LS162	
	Raytheon	54LS162	
SN54LS163	AMD	SN54LS163	
	Fairchild	54LS163	
	Motorola	SN54LS163	
	National	DM54LS163	
	Raytheon	54LS163	
	Signetics	54LS163	
SN54LS164	AMD	SN54LS164	
	Fairchild	54LS164	
	Motorola	SN54LS164	
	National	DM54LS164	
	Raytheon	**54LS164**	**272**
	Signetics	54LS164	
SN54LS165	Fairchild	54LS165	
SN54LS168	AMD	SN54LS168	
	Fairchild	54LS168	
	National	DM54LS168	
SN54LS169	AMD	SN54LS169	
	Fairchild	54LS169	
	National	DM54LS169	
SN54LS170	AMD	SN54LS170	
	Fairchild	54LS170	
	Motorola	SN54LS170	
	National	DM54LS170	
	Raytheon	54LS170	
	Signetics	54LS170	
SN54LS173	Fairchild	54LS173	
	National	DM54LS173	
	Signetics	54LS173	
SN54LS174	AMD	SN54LS174	
	Fairchild	54LS174	
	National	DM54LS174	
	Raytheon	54LS174	
	Signetics	54LS174	
SN54LS175	AMD	SN54LS175	
	Fairchild	54LS175	
	Motorola	SN54LS175	
	National	DM54LS175	
	Raytheon	54LS175	
	Signetics	54LS175	
SN54LS181	AMD	SN54LS181	
	Fairchild	54LS181	
	Motorola	SN54LS181	
	Raytheon	54LS181	
	Signetics	54LS181	
SN54LS188	**MMI**	**5330**	**1248**
SN54LS190	AMD	SN54LS190	
	Fairchild	54LS190	
	Motorola	SN54LS190	
	National	DM54LS190	
	Raytheon	54LS190	
	Signetics	54LS190	
SN54LS191	AMD	SN54LS191	
	Fairchild	54LS191	
	Motorola	SN54LS191	
	National	DM54LS191	
	Raytheon	54LS191	
	Signetics	54LS191	
SN54LS192	AMD	SN54LS192	
SN54LS192	Fairchild	54LS192	
	Motorola	SN54LS192	
	National	DM54LS192	
	Raytheon	54LS192	
	Signetics	54LS192	
SN54LS193	AMD	SN54LS193	
	Fairchild	54LS193	
	Motorola	SN54LS193	
	National	DM54LS193	
	Raytheon	54LS193	
	Signetics	54LS193	
SN54LS194A	AMD	SN54LS194A	
	Fairchild	54LS194	
	Motorola	SN54LS194	
	Raytheon	54LS194A	
SN54LS195A	AMD	SN54LS195A	
	Fairchild	54LS195	
	Motorola	SN54LS195	
	Raytheon	54LS195A	
	Signetics	54LS195A	
SN54LS196	Fairchild	54LS196	
	Motorola	SN54LS196	
	National	DM54LS196	
	Raytheon	54LS196	
SN54LS197	Fairchild	54LS197	
	Motorola	SN54LS197	
	National	DM54LS197	
	Raytheon	54LS197	
SN54LS20	Fairchild	54LS20	
	Motorola	SN54LS20	
	National	DM54LS20	
	Raytheon	54LS20	
	Signetics	54LS20	
SN54LS21	Fairchild	54LS21	
	Motorola	SN54LS21	
	National	DM54LS21	
	Raytheon	54LS21	
	Signetics	54LS21	
SN54LS22	Fairchild	54LS22	
	Motorola	SN54LS22	
	National	DM54LS22	
	Raytheon	54LS22	
	Signetics	54LS22	
SN54LS221	National	DM54LS221	
	Raytheon	**54LS221**	**275**
	Signetics	54LS221	
SN54LS240	AMD	SN54LS240	
	Fairchild	54LS240	
	MMI	54LS240	
SN54LS241	AMD	SN54LS241	
	Fairchild	54LS241	
	MMI	54LS241	
SN54LS242	AMD	SN54LS242	
	Raytheon	**54LS242**	**282**
SN54LS243	AMD	SN54LS243	
	Raytheon	**54LS243**	**282**
SN54LS244	MMI	54LS244	
SN54LS247	National	DM54LS247	
SN54LS248	National	DM54LS248	
SN54LS249	National	DM54LS249	
SN54LS251	AMD	SN54LS251	
	Fairchild	54LS251	
	Motorola	SN54LS251	
	Raytheon	54LS251	
	Signetics	54LS251	
SN54LS253	AMD	SN54LS253	
	Fairchild	54LS253	
	Motorola	SN54LS253	
	National	DM54LS253	
	Raytheon	54LS253	
	Signetics	54LS253	
SN54LS257	AMD	SN54LS257	
	Fairchild	54LS257	
	Motorola	SN54LS257	
	National	DM54LS257	
	Raytheon	54LS257	
	Signetics	54LS257	
SN54LS258	AMD	SN54LS258	
	Fairchild	54LS258	
	Motorola	SN54LS258	
	Raytheon	54LS258	
	Signetics	54LS258	
SN54LS259	Fairchild	54LS259	
	Motorola	SN54LS259	
SN54LS26	Fairchild	54LS26	
	National	DM54LS26	
SN54LS26	Raytheon	54LS26	
	Signetics	54LS26	
SN54LS261	**Raytheon**	**54LS261**	**284**
	Signetics	54LS261	
SN54LS266	Fairchild	54LS266	
	Motorola	SN54LS266	
	Raytheon	54LS266	
	Signetics	54LS266	
SN54LS27	Fairchild	54LS27	
	Motorola	SN54LS27	
	National	DM54LS27	
	Raytheon	54LS27	
	Signetics	54LS27	
SN54LS273	AMD	SN54LS273	
SN54LS279	Fairchild	54LS279	
	Motorola	SN54LS279	
	National	DM54LS279	
	Raytheon	74LS279	
	Signetics	54LS279	
SN54LS28	Raytheon	54LS28	
	Signetics	54LS28	
SN54LS280	Fairchild	54LS280	
SN54LS281	AMD	SN54LS281	
SN54LS283	Fairchild	54LS283	
	Motorola	SN54LS283	
	National	DM54LS283	
	Raytheon	54LS283	
SN54LS290	Fairchild	54LS290	
	Signetics	54LS290	
SN54LS293	Fairchild	54LS293	
	Signetics	54LS293	
SN54LS295B	Fairchild	54LS295	
	Motorola	SN54LS295	
	Raytheon	54LS295A	
	Signetics	54LS295A	
SN54LS298	Fairchild	54LS298	
	Motorola	SN54LS298	
	Raytheon	54LS298	
SN54LS299	AMD	SN54LS299	
	Fairchild	54LS299	
	Raytheon	54LS299	
SN54LS30	Fairchild	54LS30	
	Motorola	SN54LS30	
	National	DM54LS30	
	Raytheon	54LS30	
	Signetics	54LS30	
SN54LS32	Fairchild	54LS32	
	Motorola	SN54LS32	
	National	DM54LS32	
	Raytheon	54LS32	
	Signetics	54LS32	
SN54LS322	AMD	AM25LS22	
		SN54LS322	
SN54LS323	AMD	AM25LS23	
SN54LS33	Fairchild	54LS33	
	Raytheon	54LS33	
	Signetics	54LS33	
SN54LS352	Fairchild	54LS352	
	National	DM54LS352	
SN54LS353	Fairchild	54LS353	
	National	DM54LS353	
SN54LS363	MMI	54LS363	
SN54LS365	Fairchild	54LS365	
	Motorola	SN54LS365	
	Raytheon	**54LS365**	**286**
	Signetics	54LS365	
SN54LS366	Fairchild	54LS366	
	Motorola	SN54LS366	
	Raytheon	**54LS366**	**286**
	Signetics	54LS366	
SN54LS367	Fairchild	54LS367	
	Motorola	SN54LS367	
	Raytheon	**54LS367**	**286**
	Signetics	54LS367	
SN54LS368	Fairchild	54LS368	
	Motorola	SN54LS368	
	Raytheon	**54LS368**	**286**
	Signetics	54LS368	
SN54LS37	Fairchild	54LS37	
	Motorola	SN54LS37	
	National	DM54LS37	
	Raytheon	54LS37	
	Signetics	54LS37	
SN54LS373	MMI	54LS373	
SN54LS374	AMD	SN54LS374	
	MMI	54LS374	
SN54LS375	Signetics	54LS375	
SN54LS377	AMD	SN54LS377	
SN54LS378	AMD	SN54LS378	
SN54LS379	AMD	AM25LS08	
		SN54LS379	
SN54LS38	Fairchild	54LS38	
	Motorola	SN54LS38	
	National	DM54LS38	
	Raytheon	54LS38	
	Signetics	54LS38	
SN54LS381	AMD	SN54LS381	
SN54LS384	AMD	AM25LS14	
		SN54LS384	
SN54LS385	AMD	AM25LS15	
		SN54LS385	
SN54LS386	Raytheon	54LS386	
	Signetics	54LS386	
SN54LS390	Fairchild	54LS390	
SN54LS393	Fairchild	54LS393	
SN54LS395	Fairchild	54LSO95	
	National	DM54LS395	
	Raytheon	**54LS395**	**291**
	Signetics	54LS395	
SN54LS399	AMD	AM25LS09	
		SN54LS399	
SN54LS40	Fairchild	54LS40	
	Motorola	SN54LS40	
	National	DM54LS40	
	Raytheon	54LS40	
	Signetics	54LS40	
SN54LS42	Fairchild	54LS42	
	Motorola	SN54LS42	
	National	DM54LS42	
	Raytheon	**54LS42**	**266**
	Signetics	54LS42	
SN54LS424	AMD	SN54LS424	
SN54LS490	Fairchild	54LS490	
SN54LS51	Fairchild	54LS51	
	Motorola	SN54LS51	
	National	DM54LS51	
	Raytheon	54LS51	
	Signetics	54LS51	
SN54LS54	Fairchild	54LS54	
	Motorola	SN54LS54	
	National	DM54LS54	
	Raytheon	54LS54	
	Signetics	54LS54	
SN54LS55	Fairchild	54LS55	
	Motorola	SN54LS55	
	National	DM54LS55	
	Raytheon	54LS55	
	Signetics	54LS55	
SN54LS670	AMD	SN54LS670	
	Fairchild	54LS670	
	Motorola	54LS670	
	National	DM54LS670	
	Raytheon	54LS670	
	Signetics	54LS670	
SN54LS73	Fairchild	54LS73	
	Motorola	SN54LS73	
	National	DM54LS73	
	Raytheon	54LS73	
	Signetics	54LS73	
SN54LS74	Fairchild	54LS74	
	Motorola	SN54LS74	
	National	DM54LS74	
	Raytheon	54LS74	
	Signetics	54LS74	
SN54LS75	Fairchild	54LS75	
	National	DM54LS75	
	Raytheon	54LS75	
	Signetics	54LS75	
SN54LS76	National	DM54LS76	
	Raytheon	54LS76	
	Signetics	54LS76	
SN54LS77	Fairchild	54LS77	
	Raytheon	54LS77	
SN54LS78	National	DM54LS78	
	Raytheon	54LS78	
	Signetics	54LS78	
SN54LS83A	Fairchild	54LS83	
	Motorola	SN54LS83	
	National	DM54LS83	
	Raytheon	54LS83A	
SN54LS85	Fairchild	54LS85	
	National	DM54LS85	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN54LS85	Raytheon	54LS85	
	Signetics	54LS85	
SN54LS86	Fairchild	54LS86	
	Motorola	SN54LS86	
	Raytheon	54LS86	
	Signetics	54LS86	
SN54LS90	Fairchild	54LS90	
	Motorola	SN54LS90	
	Raytheon	**54LS90**	**268**
	Signetics	54LS90	
SN54LS91	**Raytheon**	**54LS91**	**272**
SN54LS92	Motorola	SN54LS92	
	Raytheon	**54LS92**	**268**
	Signetics	S54LS92	
		54LS92	
SN54LS93	Fairchild	54LS93	
	Motorola	SN54LS93	
	Raytheon	**54LS93**	**268**
	Signetics	54LS93	
SN54LS95B	Fairchild	54LS95	
		54LS95B	
	Motorola	SN54LS95B	
	Raytheon	54LS95B	
SN54LS96	Signetics	54LS96	
SN54L00	National	DM54L00	
SN54L01	National	DM54L01	
SN54L02	National	DM54L02	
SN54L03	National	DM54L03	
SN54L04	National	DM54L04	
SN54L10	National	DM54L10	
♦SN54L123	National	DM54L123	
SN54L154	National	DM54L154A	
SN54L157	National	DM54L157A	
SN54L164	National	DM54L164	
SN54L192	National	DM54L192	
SN54L193	National	DM54L193	
SN54L20	National	DM54L20	
SN54L30	National	DM54L30	
SN54L42A	National	DM54L42A	
SN54L51	National	DM54L51	
SN54L54	National	DM54L54	
SN54L55	National	DM54L55	
SN54L71	National	DM54L71	
SN54L72	National	DM54L72	
SN54L73	National	DM54L73	
SN54L74	National	DM54L74	
♦SN54L75	National	DM54L75	
SN54L78	National	DM54L78	
SN54L85	National	DM54L85	
SN54L86	National	DM54L86	
SN54L90	National	DM54L90	
SN54L91	National	DM54L91	
SN54L93	National	DM54L93	
SN54L95	National	DM54L95	
SN54L98	National	DM54L98	
SN54S00	Fairchild	54S00	
		9S00	
SN54S02	Fairchild	54S02	
	Signetics	54S02	
SN54S03	Fairchild	54S03	
		9S03	
SN54S04	Fairchild	54S04	
		9S04	
	Signetics	54S04	
SN54S05	Fairchild	54S05	
		9S05	
	Signetics	54S05	
SN54S08	Fairchild	54S08	
	Signetics	54S08	
SN54S09	Fairchild	54S09	
	Signetics	54S09	
SN54S10	Fairchild	54S10	
SN54S11	Fairchild	54S11	
	Signetics	54S11	
SN54S112	Fairchild	54S112	
		9S112	
	Motorola	SN54S112	
SN54S113	Fairchild	54S113	
		9S113	
	Motorola	SN54S113	
SN54S114	Fairchild	54S114	
		9S114	
SN54S132	Fairchild	54S132	
SN54S133	Fairchild	54S133	
		9S133	
SN54S134	Fairchild	54S134	
		9S134	
SN54S135	Fairchild	54S135	
SN54S138	AMD	SN54S138	
	Fairchild	54S138	
SN54S139	AMD	SN54S139	
	Fairchild	54S139	
	Signetics	54S139	
SN54S140	AMD	SN54S140	
	Fairchild	54S140	
		9S140	
	National	DM54S140	
	Signetics	54S140	
SN54S15	Fairchild	54S15	
	Signetics	54S15	
SN54S151	AMD	SN54S151	
	Fairchild	54S151	
	Signetics	54S151	
SN54S153	AMD	SN54S153	
	Fairchild	54S153	
	Signetics	54S153	
SN54S157	AMD	SN54S157	
	Fairchild	54S157	
	Signetics	54S157	
SN54S158	AMD	SN54S158	
	Fairchild	54S158	
	Signetics	54S158	
SN54S174	AMD	SN54S174	
	Fairchild	54S174	
SN54S175	AMD	SN54S175	
	Fairchild	54S175	
SN54S181	AMD	SN54S181	
	Fairchild	54S181	
		93S41	
	Signetics	54S181	
SN54S182	Fairchild	54S182	
		93S42	
SN54S188	AMD	AM27S09	
	Harris	**HM7602**	**1192**
SN54S188A	**MMI**	**5330**	**1248**
SN54S189	AMD	AM27S03	
		SN54S189	
	National	**DM54S189**	**1292**
SN54S194	AMD	SN54S194	
	Fairchild	54S194	
SN54S195	AMD	SN54S195	
	Fairchild	54S195	
		93S00	
SN54S20	Fairchild	54S20	
		9S20	
♦SN54S200	MMI	5531	
	National	DM54S200	
	Raytheon	RM5340	
	Signetics	54S200	
	TI	SN54S201	
SN54S201	National	DM54S200	
SN54S206	Fairchild	93411	
	MMI	**5205**	**1252**
	National	**DM54S206**	**1297**
	Raytheon	RM5330	
	TI	SN74S301	
SN54S22	Fairchild	54S22	
		9S22	
	National	DM54S22	
	Signetics	54S22	
SN54S240	AMD	SN54S240	
	MMI	**54S240**	**462**
	Raytheon	54S240	
SN54S241	AMD	SN54S241	
	MMI	**54S241**	**462**
	Raytheon	54S241	
SN54S251	AMD	SN54S251	
	Fairchild	54S251	
	Signetics	54S251	
SN54S257	AMD	SN54S257	
SN54S258	AMD	SN54S258	
	Fairchild	54S258	
	Signetics	54S258	
SN54S270	**MMI**	**5205**	**1252**
SN54S287	**Harris**	**HM7611**	**1192**
		HM7611A	**1200**
	MMI	**5301**	**1248**
SN54S288	**Harris**	**HM7603**	**1192**
	MMI	**5331**	**1248**
SN54S288	National	DM7578	
SN54S289	AMD	AM27S02	
		SN54S289	
	National	DM54S289	
SN54S30	Fairchild	54S30	
SN54S301	**National**	**DM54S206**	**1297**
SN54S32	Fairchild	54S32	
	Signetics	54S32	
SN54S37	Signetics	54S37	
SN54S370	**MMI**	**5206**	**1252**
SN54S373	**MMI**	**54S373**	**460**
SN54S374	**MMI**	**54S374**	**460**
SN54S387	**Harris**	**HM7610**	**1192**
		HM7610A	**1200**
	Intel	M3601	
		3601	
	MMI	**5300**	**1248**
		6300	**1252**
	National	**DM54S387**	**1264**
	Signetics	S82S126	
SN54S40	Fairchild	54S40	
		9S40	
SN54S412	AMD	SN54S412	
SN54S470	**MMI**	**5308-1**	**1248**
SN54S471	**MMI**	**5309-1**	**1248**
SN54S472	**MMI**	**5349-1**	**1248**
SN54S473	**MMI**	**5348-1**	**1248**
SN54S51	Fairchild	54S51	
SN54S64	Fairchild	54S64	
		9S64	
SN54S65	Fairchild	54S65	
		9S65	
SN54S74	Fairchild	54S74	
		9S74	
SN54S85	Signetics	54S85	
SN54S86	Fairchild	54S86	
	Signetics	54S86	
SN5400	Fairchild	5400	
		9N00	
	ITT	ITT5400	
	Motorola	MC5400	
	National	DM5400	
	Raytheon	5400	
	Signetics	5400	
SN5401	Fairchild	5401	
		9N01	
	ITT	ITT5401	
	Motorola	MC5401	
	National	DM5401	
	Raytheon	5401	
	Signetics	5401	
SN5402	Fairchild	5402	
		9N02	
	ITT	ITT5402	
	Motorola	MC5402	
	National	DM5402	
	Signetics	5402	
SN5403	Fairchild	5403	
		9N03	
	ITT	ITT5403	
	Motorola	MC5403	
	National	DM5403	
	Raytheon	5403	
	Signetics	5403	
SN5404	Fairchild	5404	
		9N04	
	ITT	ITT5404	
	Motorola	MC5404	
	National	DM5404	
	Raytheon	5404	
	Signetics	5404	
SN5405	Fairchild	5405	
		9N05	
	ITT	ITT5405	
	Motorola	MC5405	
	National	DM5405	
	Raytheon	5405	
	Signetics	5405	
SN5406	Fairchild	5406	
		9N06	
	ITT	ITT5406	
	Motorola	MC5406	
	National	DM5406	
	Signetics	5406	
SN5407	Fairchild	5407	
		9N07	
SN5407	ITT	ITT5407	
	Motorola	MC5407	
	National	DM5407	
	Signetics	5407	
SN5408	Fairchild	5408	
		9N08	
	ITT	ITT5408	
	Motorola	MC5408	
	National	DM5408	
	Raytheon	5408	
	Signetics	5408	
SN5409	Fairchild	5409	
		9N09	
	ITT	ITT5409	
	Motorola	MC5409	
	National	DM5409	
	Raytheon	5409	
	Signetics	5409	
SN5410	Fairchild	5410	
		9N10	
	ITT	ITT5410	
	Motorola	MC5410	
	National	DM5410	
	Raytheon	5410	
	Signetics	5410	
SN54100	Motorola	MC54100	
	Signetics	54100	
SN54107	AMD	SN54107	
	Fairchild	54107	
		9N107	
	ITT	ITT54107	
	Motorola	MC54107	
	National	DM54107	
	Signetics	54107	
SN54109	National	DM54109	
	Signetics	54109	
SN5411	Fairchild	5411	
	ITT	ITT5411	
	National	DM5411	
	Raytheon	5411	
	Signetics	5411	
SN54116	Fairchild	54116	
	Signetics	54116	
SN5412	Fairchild	5412	
		9N12	
	ITT	ITT5412	
	Raytheon	5412	
	Signetics	5412	
SN54120	Motorola	MC54120	
SN54121	Fairchild	54121	
		9603	
	ITT	ITT54121	
	Motorola	MC54121	
		MC9603	
	National	DM54121	
	Signetics	54121	
SN54122	Fairchild	54122	
	ITT	ITT54122	
	Motorola	MC54122	
SN54123	AMD	AM26123	
		SN54123	
	Fairchild	54123	
	ITT	ITT54123	
	Motorola	MC54123	
	National	DM54123	
	Raytheon	54123	
	Signetics	54123	
SN54125	Fairchild	54125	
	National	DM54125	
		DM7093	
	Signetics	54125	
SN54126	Fairchild	54126	
	National	DM54126	
		DM7094	
	Signetics	54126	
SN54128	Signetics	54128	
SN5413	Fairchild	5413	
		9N13	
	ITT	ITT5413	
	Motorola	MC5413	
	National	DM5413	
	Signetics	5413	
SN54132	Fairchild	54132	
	Motorola	MC54132	
	National	DM54132	
	Signetics	54132	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Texas Instruments (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
SN54136	Raytheon	54136	
SN5414	Fairchild	5414	
	Motorola	MC5414	
	National	DM5414	
	Signetics	5414	
SN54141	Motorola	MC54141	
	National	DM54141	
	Signetics	54141	
SN54145	Fairchild	54145	
		93145	
	ITT	ITT54145	
	Motorola	MC54145	
	National	DM54145	
	Raytheon	54145	
	Signetics	54145	
SN54147	National	DM54147	
	Signetics	54147	
SN54148	National	DM54148	
	Signetics	54148	
SN54150	Fairchild	54150	
		93150	
	Motorola	MC54150	
	National	DM54150	
	Raytheon	54150	
	Signetics	54150	
♦SN54151	Fairchild	54151	
		93151	
	ITT	ITT54151	
	Motorola	MC54151	
	National	DM54151	
	Raytheon	54151	
	Signetics	54151	
	TI	SN54151A	
♦SN54152	Fairchild	54152	
		93152	
	Motorola	MC54152	
	Raytheon	54152	
	Signetics	54152	
	TI	SN54152A	
SN54153	AMD	SN54153	
	Fairchild	54153	
		93153	
	ITT	ITT54153	
	Motorola	MC54153	
	National	DM54153	
	Raytheon	54153	
	Signetics	54153	
SN54154	AMD	SN54154	
	Fairchild	54154	
		9311	
	Motorola	MC54154	
	National	DM54154	
	Raytheon	54154	
	Signetics	54154	
SN54155	Fairchild	54155	
		93155	
	ITT	ITT54155	
	Motorola	MC54155	
	National	DM54155	
	Raytheon	54155	
	Signetics	54155	
SN54156	Fairchild	54156	
		93156	
	ITT	ITT54156	
	Motorola	MC54156	
	National	DM54156	
	Raytheon	54156	
	Signetics	54156	
SN54157	AMD	SN54157	
	Fairchild	54157	
		9322	
	ITT	ITT54157	
	Motorola	MC54157	
	National	DM54157	
		DM9322	
	Raytheon	54157	
	Signetics	54157	
SN54159	Raytheon	54159	
SN5416	Fairchild	5416	
		9N16	
	ITT	ITT5416	
	Motorola	MC5416	
	National	DM5416	
SN5416	Signetics	5416	
SN54160	AMD	SN54160	
	Fairchild	54160	
		9310	
	ITT	ITT54160	
	Motorola	MC54160	
	National	DM54160	
	Raytheon	54160	
	Signetics	54160	
SN54161	AMD	SN54161	
	Faircnild	54161	
		9316	
	ITT	ITT54161	
	Motoroia	MC54161	
	National	DM54161	
	Raytheon	54161	
	Signetics	54161	
SN54162	AMD	SN54162	
	Fairchild	54162	
	ITT	ITT54162	
	Motorola	MC54162	
	National	DM54162	
	Raytheon	54162	
	Signetics	54162	
SN54163	AMD	SN54163	
	Fairchild	54163	
	ITT	ITT54163	
	Motorola	MC54163	
	National	DM54163	
	Raytheon	54163	
	Signetics	54163	
SN54164	AMD	SN54164	
	Fairchild	54164	
		93164	
	ITT	ITT54164	
	National	DM54164	
		DM7570	
	Raytheon	54164	
	Signetics	54164	
SN54165	Faircnild	54165	
		93165	
	Motoroia	MC54165	
	National	DM54165	
		DM7590	
	Raytheon	54165	
	Signetics	54165	
SN54166	Fairchild	54166	
		93166	
	National	DM54166	
	Raytheon	54166	
	Signetics	54166	
SN54167	Motorola	MC54167	
SN5417	Fairchild	5417	
		9N17	
	ITT	ITT5417	
	Motorola	MC5417	
	National	DM5417	
	Signetics	5417	
SN54170	Fairchild	54170	
	National	DM54170	
	Raytheon	54170	
	Signetics	54170	
SN54173	Fairchild	54173	
	National	DM54173	
		DM7551	
SN54174	AMD	SN54174	
		SN74174	
	Fairchild	54174	
		93174	
	Motorola	MC54174	
	National	DM54174	
	Raytheon	54174	
	Signetics	54174	
SN54175	AMD	SN54175	
	Fairchild	54175	
		93175	
	Motorola	MC54175	
	National	DM54175	
	Raytheon	54175	
	Signetics	54175	
SN54176	Fairchild	54176	
		93176	
	Motorola	MC54176	
	National	DM54176	
		DM7280	
	Signetics	S8280	
SN54176	Signetics	54176	
SN54177	Fairchild	54177	
		93177	
	Motorola	MC54177	
	National	DM54177	
		DM7281	
	Signetics	S8281	
		54177	
SN54178	Fairchild	54178	
		93178	
	Signetics	S8270	
SN54179	Fairchild	54179	
		93179	
SN54180	Fairchild	54180	
		93180	
	ITT	ITT54180	
	Motorola	MC54180	
	National	DM54180	
	Raytheon	54180	
	Signetics	54180	
SN54181	AMD	SN54181	
		9341	
	Fairchild	54181	
		9341	
	Motorola	MC54181	
	National	DM54181	
	Raytheon	54181	
	Signetics	54181	
SN54182	AMD	SN54182	
		9342	
	Fairchild	54182	
		9342	
	ITT	ITT54182	
	Motorola	MC54182	
	National	DM54182	
	Raytheon	54182	
	Signetics	54182	
SN54184	National	DM54184	
SN54185	National	DM54185	
SN54185A	National	DM54185A	
SN54186	Harris	HPROM0512	
SN54187	**Intersil**	**IM5603**	
	MMI	**5200**	**1252**
	National	DM54187	
SN54188	**Harris**	**HM7602**	**1192**
SN54188A	**MMI**	**5330**	**1248**
	National	DM7577	
SN54190	Fairchild	54190	
		93190	
	ITT	ITT54190	
	Motorola	MC54190	
	National	DM54190	
	Raytheon	54190	
	Signetics	54190	
SN54191	Fairchild	54191	
		93191	
	ITT	ITT54191	
	Motorola	MC54191	
	National	DM54191	
	Raytheon	54191	
	Signetics	54191	
SN54192	AMD	SN54192	
		9360	
	Fairchild	54192	
		9360	
	ITT	ITT54192	
	Motorola	MC54192	
	National	DM54192	
		DM7560	
	Raytheon	54192	
	Signetics	54192	
SN54193	AMD	SN54193	
		9366	
	Fairchild	54193	
		9366	
	ITT	ITT54193	
	Motorola	MC54193	
	National	DM54193	
		DM7563	
	Raytheon	54193	
	Signetics	54193	
SN54194	AMD	SN54194	
	Fairchild	54194	
	ITT	ITT54194	
	Motorola	MC54194	
	National	DM54194	
SN54194	Raytheon	54194	
	Signetics	54194	
SN54195	AMD	SN54195	
	Fairchild	54195	
		9300	
	ITT	ITT54195	
	Motorola	MC54195	
	National	DM54195	
		DM9300	
	Raytheon	54195	
	Signetics	54195	
SN54196	Fairchild	54196	
		93196	
	Motorola	MC54196	
	National	DM54196	
	Signetics	S8290	
		54196	
SN54197	Fairchild	54197	
		93197	
	Motorola	MC54197	
	National	DM54197	
	Signetics	54197	
SN54198	Fairchild	54198	
		93198	
	National	DM54198	
	Raytheon	54198	
	Signetics	54198	
SN54199	Fairchild	54199	
	National	DM54199	
	Raytheon	54199	
	Signetics	54199	
SN5420	Fairchild	5420	
		9N20	
	ITT	ITT5420	
	Motorola	MC5420	
	National	DM5420	
	Raytheon	5420	
	Signetics	S8819	
		5420	
♦SN54200	MMI	5531	
	TI	SN54S201	
SN54206	**MMI**	**5530**	
	National	**DM54S206**	**1297**
	TI	SN54S301	
SN5422	Fairchild	5422	
	Raytheon	5422	
SN54221	AMD	SN54221	
SN5423	Fairchild	5423	
		9N23	
	Motorola	MC5423	
	National	DM5423	
SN5425	Fairchild	5425	
		9N25	
	ITT	ITT5425	
	Motorola	MC5425	
	National	DM5425	
SN54251	National	DM7121	
		SM54251	
SN54259	AMD	SN54259	
SN5426	Fairchild	5426	
		9N26	
	ITT	ITT5426	
	Motorola	MC5426	
	National	DM5426	
	Signetics	S8T18	
		5426	
SN5427	Fairchild	5427	
		9N27	
	Motorola	MC5427	
	National	DM5427	
SN54270	**MMI**	**5205**	**1252**
SN54278	Motorola	MC54278	
SN54279	Fairchild	54279	
	Motorola	MC54279	
	Signetics	54279	
SN54280	Raytheon	54280	
SN54283	Fairchild	54283	
	Raytheon	54283	
SN54284	National	DM7875A	
SN54285	National	DM7875B	
SN54290	Motorola	MC54290	
SN54293	Motorola	MC54293	
SN54298	Fairchild	54298	
	Motorola	MC54298	
	Signetics	54298	
SN5430	Fairchild	5430	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN5430	Fairchild	9N30	
	ITT	ITT5430	
	Motorola	MC5430	
	National	DM5430	
	Signetics	S8808	
		5430	
SN5432	Fairchild	5432	
		9N32	
	ITT	ITT5432	
	National	DM5432	
	Signetics	5432	
SN54365	National	DM7095	
SN54366	National	DM7096	
SN54367	National	DM7097	
SN54368	National	DM7098	
SN5437	Fairchild	5437	
		9N37	
	ITT	ITT5437	
	Motorola	MC5437	
	National	DM5437	
	Raytheon	5437	
	Signetics	5437	
SN54370	**MMI**	**5206**	**1252**
SN5438	Fairchild	5438	
		9N38	
	ITT	ITT5438	
	Motorola	MC5438	
	National	DM5438	
	Raytheon	5438	
	Signetics	5438	
SN5440	Fairchild	5440	
		9N40	
	ITT	ITT5440	
	Motorola	MC5440	
	National	DM5440	
	Signetics	5440	
♦SN5442	Fairchild	5442	
		9352	
	ITT	ITT5442	
	Motorola	MC5442	
	National	DM5442	
	Raytheon	5442	
	Signetics	5442	
	TI	SN5442A	
SN54425	National	DM7093	
SN54426	National	DM7094	
SN5443	Fairchild	5443	
♦SN5443	Fairchild	5443	
		9353	
	ITT	ITT5443	
	Motorola	MC5443	
	Raytheon	5443	
	Signetics	5443	
	TI	SN5443A	
SN5444	Fairchild	5444	
♦SN5444	Fairchild	5444	
		9354	
	ITT	ITT5444	
	Motorola	MC5444	
	Raytheon	5444	
	Signetics	5444	
	TI	SN5444A	
SN5445	Fairchild	5445	
		9345	
	ITT	ITT5445	
	Motorola	MC5445	
	National	DM5445	
	Raytheon	5445	
	Signetics	5445	
SN5446	Fairchild	5446	
♦SN5446	Fairchild	5446	
		9357	
	ITT	ITT5446	
	Motorola	MC5446	
	National	DM5446	
	Signetics	5446	
	TI	SN5446A	
SN5447	Fairchild	5447	
♦SN5447	Fairchild	5447	
		9357	
	ITT	ITT5447	
	Motorola	MC5447	
	National	DM5447	
♦SN5447	Signetics	5447	
	TI	SN5447A	
SN5448	Fairchild	5448	
		9358	
	ITT	ITT5448	
	Motorola	MC5448	
	National	DM5448	
	Signetics	5448	
SN5449	Fairchild	5449	
		9359	
	Motorola	MC5449	
SN5450	Fairchild	5450	
		9N50	
	ITT	ITT5450	
	Motorola	MC5450	
	National	DM5450	
	Signetics	5450	
SN5451	Fairchild	5451	
		9N91	
	ITT	ITT5451	
	Motorola	MC5451	
	National	DM5451	
	Signetics	5451	
SN5453	Fairchild	5453	
		9N53	
	ITT	ITT5453	
	Motorola	MC5453	
	National	DM5453	
	Signetics	5453	
SN5454	Fairchild	5454	
		9N54	
	ITT	ITT5454	
	Motorola	MC5454	
	National	DM5454	
	Signetics	5454	
SN5460	Fairchild	5460	
		9N60	
	Motorola	MC5460	
	National	DM5460	
	Signetics	5460	
SN5470	Fairchild	5470	
		9N70	
	ITT	ITT5470	
	Motorola	MC5470	
	National	DM5470	
	Signetics	5470	
SN5472	Fairchild	5472	
		9N72	
	ITT	ITT5472	
	Motorola	MC5472	
	National	DM5472	
	Signetics	5472	
SN5473	Fairchild	5473	
		9N73	
	ITT	ITT5473	
	Motorola	MC5473	
	National	DM5473	
	Signetics	5473	
SN5474	Fairchild	5474	
		9N74	
	ITT	ITT5474	
	Motorola	MC5474	
	National	DM5474	
	Raytheon	5474	
	Signetics	5474	
SN5475	Fairchild	5475	
		9375	
	ITT	ITT5475	
	Motorola	MC5475	
	National	DM5475	
	Signetics	5475	
SN5476	Fairchild	5476	
		9N76	
	ITT	ITT5476	
	Motorola	MC5476	
	National	DM5476	
	Signetics	5476	
SN5477	Fairchild	5477	
		9377	
	Motorola	MC5477	
	Signetics	5477	
SN5480	Fairchild	5480	
		9380	
	ITT	ITT5480	
	Motorola	MC5480	
	Signetics	5480	
♦SN5481	Fairchild	93407	
	TI	SN5481A	
SN5482	Fairchild	5482	
		9382	
	ITT	ITT5482	
	Motorola	MC5482	
♦SN5483	Fairchild	5483	
		9383	
	ITT	ITT5483	
	National	DM5483	
	Raytheon	5483	
	Signetics	5483	
	TI	SN5483A	
SN5485	Fairchild	5485	
	Motorola	MC5485	
	National	DM5485	
	Signetics	5485	
SN5486	Fairchild	5486	
		9N86	
	ITT	ITT5486	
	Motorola	MC5486	
	National	DM5486	
	Raytheon	5486	
	Signetics	5486	
♦SN5488	Intersil	IM5600	
	MMI	**5230**	**1252**
	National	DM5488	
	TI	SN5488A	
♦SN5489	AMD	SN5489	
		5889	
	Fairchild	5489	
		93403	
	MMI	5560	
	National	**DM5489**	**1287**
	Raytheon	5489	
	Signetics	S8225	
	TI	SN54S189	
♦SN5490	Fairchild	5490	
		9390	
	ITT	ITT5490	
	Motorola	MC5490	
	National	DM5490	
	Signetics	5490	
	TI	SN5490A	
♦SN5491	Fairchild	5491	
		9391	
	ITT	ITT5491	
	Motorola	MC5491	
	National	DM5491	
	Signetics	5491	
	TI	SN5491A	
SN5492	Fairchild	5492	
♦SN5492	Fairchild	5492	
		9392	
	ITT	ITT5492	
	Motorola	MC5492	
	National	DM5492	
	Signetics	5492	
	TI	SN5492A	
SN5493	Fairchild	5493	
♦SN5493	Fairchild	5493	
		9393	
	ITT	ITT5493	
	Motorola	MC5493	
	National	DM5493	
	Signetics	5493	
	TI	SN5493A	
SN5494	Fairchild	5494	
		9394	
	Motorola	MC5494	
	Signetics	5494	
SN5495	Fairchild	5495	
♦SN5495	Fairchild	5495	
		9395	
	ITT	ITT5495	
	Motorola	MC5495	
	National	DM5495	
	Signetics	5495	
	TI	SN5495A	
SN5496	Fairchild	5496	
		9396	
	ITT	ITT5496	
	Motorola	MC5496	
	National	DM5496	
	Signetics	5496	
SN5497	Fairchild	5497	
SN5497	Motorola	MC5497	
♦SN5510	Motorola	MC1510	
SN55107	AMD	SN55107	
	Fairchild	55107	
	Motorola	MC55107	
	National	**DS55107**	**504**
	Raytheon	RM55107	
	Silicon G	SG107	
SN55108	AMD	SN55108B	
	Fairchild	55108	
	Motorola	MC55108	
	National	**DS55108**	**504**
	Raytheon	RM55108	
	Silicon G	SG108	
SN55109	AMD	SN55109	
	Fairchild	55109	
	Raytheon	RM55109	
	Silicon G	SG109	
SN55110	AMD	SN55110	
	Fairchild	55110	
	Raytheon	RM55110	
	Silicon G	SG110	
SN55112	Fairchild	55112	
SN55114	AMD	9614	
	Fairchild	96114	
	ITT	ITT9614	
SN55115	AMD	9615	
	Fairchild	96115	
	ITT	ITT9615	
SN55121	Fairchild	55121	
	National	DS55121	
SN55122	Fairchild	55122	
	National	DS55122	
SN55123	Fairchild	55123	
	Silicon G	SG123	
SN55124	Fairchild	55124	
	Silicon G	SG124	
SN55138	Silicon G	SG55138	
SN55180	National	DS7800	
SN55182	AMD	DM7820	
	National	DS7820	
	Signetics	DS7820	
SN55183	AMD	DM7830	
	National	DS7830	
	Signetics	DS7830	
SN5520	AMD	SN5520	
		SN5521	
	National	DS5520	
	Silicon G	SG5520	
SN55207	Fairchild	55207	
	Silicon G	SG207	
SN55208	Fairchild	55208	
	Silicon G	SG208	
♦SN5521	National	DS5521	
	Silicon G	SG5521	
SN5522	Motorola	MC5522	
	National	DS5522	
	Silicon G	SG5522	
SN55224	Fairchild	55224	
SN55225	Fairchild	55225	
♦SN5523	Motorola	MC5523	
	National	DS5523	
	Silicon G	SG5523	
SN55232	Fairchild	55232	
SN55233	Fairchild	55233	
SN55234	AMD	SN55234	
	Fairchild	55234	
SN55235	AMD	SN55235	
	Fairchild	55235	
SN55238	AMD	SN55238	
	Fairchild	55238	
SN55239	AMD	SN55239	
	Fairchild	55239	
	Silicon G	SG239	
SN5524	AMD	SN5524	
	Fairchild	5524	
	Motorola	MC5524	
	National	DS5524	
	Silicon G	SG5524	
SN55244	AMD	MC1544	
	Motorola	MC1544	
♦SN5525	AMD	SN5525	
	Fairchild	5525	
	Motorola	MC5525	
	National	DS5525	
	Silicon G	SG5525	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN5528	Fairchild	5528	
	Motorola	MC5528	
	National	DS5528	
	Silicon G	SG5528	
♦SN5529	Fairchild	5529	
	Motorola	MC5529	
	National	DS5529	
	Silicon G	SG5529	
SN55325	AMD	SN55325	
	Fairchild	55325	
	Motorola	MC55325	
	National	**DS55325**	**520**
	Raytheon	RM55325	
	Silicon G	SG55325	
SN55326	Fairchild	55326	
SN55327	Fairchild	55327	
♦SN5534	Fairchild	5534	
	National	DS5534	
	Silicon G	SG5534	
SN5535	Fairchild	5535	
	National	DS5535	
	Silicon G	SG5535	
SN55361	National	DS55361	
SN55365	National	DS55365	
SN55369	AMD	MMH0020	
	National	**DS0026**	**503**
♦SN5538	Fairchild	5538	
	National	DS5538	
	Silicon G	SG5538	
♦SN5539	Fairchild	5539	
	National	DS5539	
	Silicon G	SG5539	
SN55450	Fairchild	55450	
	National	DS55450	
	Raytheon	RM55450	
	Silicon G	SG55450	
SN55451	Fairchild	55451	
	National	DS55451	
	Raytheon	RM55451	
	Silicon G	SG55451	
SN55452	Fairchild	55452	
	National	DS55452	
	Raytheon	RM55452	
	Silicon G	SG55452	
SN55453	Fairchild	55453	
	National	DS55453	
	Raytheon	RM55453	
	Silicon G	SG55453	
SN55454	Fairchild	55454	
	National	DS55454	
	Raytheon	RM55454	
	Silicon G	SG55454	
SN55460	Fairchild	55460	
	National	DS55460	
	Silicon G	SG55460	
SN55461	Fairchild	55461	
	National	DS55461	
	Silicon G	SG55461	
SN55462	Fairchild	55462	
	National	DS55462	
	Silicon G	SG55462	
SN55463	Fairchild	55463	
	National	DS55463	
	Silicon G	SG55463	
SN55464	Fairchild	55464	
	National	DS55464	
	Silicon G	SG55464	
SN55470	Fairchild	55470	
SN55471	Fairchild	55471	
SN55472	Fairchild	55472	
SN55473	Fairchild	55473	
SN55474	Fairchild	55474	
SN55480	National	DS7880	
SN55493	National	DS55493	
SN55494	National	DS55494	
♦SN56502	TI	TL441	
♦SN72L022	TI	TL022	
♦SN72L044	TI	TL044	
♦SN72301A	TI	LM301	
♦SN72304	TI	LM304	
♦SN72305	TI	LM305	
♦SN72306	TI	LM306	
♦SN72307	TI	LM307	
♦SN72308	AMD	LM308	
	Fairchild	μA308	
	Intersil	LM308	
	Motorola	LM308	
	Raytheon	LM308	
	RCA	CA308	
	Silicon G	SG308	
♦SN72309	TI	LM309	
♦SN72310	AMD	LM310	
	Fairchild	μA310	
	Intersil	LM310	
	Motorola	MLM310	
	Silicon G	SG310	
♦SN72311	TI	LM311	
♦SN72318	TI	LM318	
♦SN72376	TI	LM376	
♦SN72440	TI	TL440	
♦SN72506	TI	TL506	
♦SN72510	TI	TL510	
♦SN72514	TI	TL514	
♦SN72555	TI	NE555	
♦SN72558	TI	MC1458	
♦SN72560	TI	TL560	
♦SN72702	TI	TL702	
♦SN72709	TI	μA709	
♦SN72710	TI	TL710	
♦SN72711	TI	μA711	
♦SN72720	TI	TL720	
♦SN72723	TI	μA723	
♦SN72733	TI	μA733	
♦SN72741	TI	μA741	
♦SN72747	TI	μA747	
♦SN72748	TI	μA748	
♦SN72777	TI	μA777	
♦SN72810	TI	TL810	
♦SN72811	TI	TL811	
♦SN72820	TI	TL820	
♦SN72905	Motorola	MC7905	
♦SN72906	Motorola	MC7906	
♦SN72908	Motorola	MC7908	
♦SN72912	Motorola	MC7912	
♦SN72915	Motorola	MC7915	
♦SN72918	Motorola	MC7918	
♦SN72924	Motorola	MC7924	
SN74H00	Fairchild	74H00	
		9H00	
	ITT	ITT74H00	
	Motorola	MC74H00	
	National	DM74H00	
	NEC America	μPB74H00	
	Raytheon	74H00	
	Signetics	74H00	
SN74H01	Fairchild	74H01	
		9H01	
	ITT	ITT74H01	
	Motorola	MC74H01	
	National	DM74H01	
	NEC America	μPB74H01	
	Raytheon	74H01	
	Signetics	74H01	
SN74H04	Fairchild	74H04	
		9H04	
	ITT	ITT74H04	
	Motorola	MC74H04	
	National	DM74H04	
	NEC America	μPB74H04	
	Raytheon	74H04	
	Signetics	74H04	
SN74H05	Fairchild	74H05	
		9H05	
	ITT	ITT74H05	
	Motorola	MC74H05	
	National	DM74H05	
	Raytheon	74H05	
	Signetics	74H05	
SN74H10	Fairchild	74H10	
		9H10	
	ITT	ITT74H10	
	Motorola	MC74H10	
	National	DM74H10	
	NEC America	μPB74H10	
	Raytheon	74H10	
	Signetics	74H10	
SN74H101	Motorola	MC74H101	
	Signetics	74H101	
SN74H102	Fairchild	74H102	
SN74H102	Motorola	MC74H102	
	Signetics	74H102	
SN74H103	Fairchild	74H103	
	National	DM74H103	
	Signetics	74H103	
SN74H106	Fairchild	74H106	
		9H106	
	National	DM74H106	
	Signetics	74H106	
SN74H108	Fairchild	74H108	
		9H108	
	Motorola	MC74H108	
	National	DM74H108	
	Signetics	74H108	
SN74H11	Fairchild	74H11	
		9H11	
	ITT	ITT74H11	
	Motorola	MC74H11	
	National	DM74H11	
	Raytheon	74H11	
	Signetics	74H11	
SN74H15	Fairchild	74H15	
	Raytheon	74H15	
SN74H183	Fairchild	74H183	
		93H183	
	Hitachi	HD2563	
SN74H20	Fairchild	74H20	
		9H20	
	ITT	ITT74H20	
	Motorola	MC74H20	
	National	DM74H20	
	NEC America	μPB74H20	
	Raytheon	74H20	
	Signetics	74H20	
SN74H21	Fairchild	74H21	
		9H21	
	ITT	ITT74H21	
	Motorola	MC74H21	
	National	DM74H21	
	Signetics	74H21	
SN74H22	Fairchild	74H22	
		9H22	
	Motorola	MC74H22	
	National	DM74H22	
	Raytheon	74H22	
	Signetics	74H22	
SN74H30	Fairchild	74H30	
		9H30	
	ITT	ITT74H30	
	Motorola	MC74H30	
	National	DM74H30	
	NEC America	μPB74H30	
	Signetics	74H30	
SN74H40	Fairchild	74H40	
		9H40	
	ITT	ITT74H40	
	Motorola	MC74H40	
	National	DM74H40	
	NEC America	μPB74H40	
	Raytheon	74H40	
	Signetics	74H40	
SN74H50	Fairchild	74H50	
		9H50	
	ITT	ITT74H50	
	Motorola	MC74H50	
	National	DM74H50	
	Signetics	74H50	
SN74H51	Fairchild	74H51	
		9H51	
	ITT	ITT74H51	
	Motorola	MC74H51	
	National	DM74H51	
	NEC America	μPB74H51	
	Signetics	74H51	
SN74H52	Fairchild	74H52	
		9H52	
	Motorola	MC74H52	
	National	DM74H52	
	Signetics	74H52	
SN74H53	Fairchild	74H53	
		9H53	
	ITT	ITT74H53	
	Motorola	MC74H53	
	National	DM74H53	
	Signetics	74H53	
SN74H54	Fairchild	74H54	
SN74H54	Fairchild	9H54	
	ITT	ITT74H54	
	Motorola	MC74H54	
	National	DM74H54	
	Signetics	74H54	
SN74H55	Fairchild	74H55	
		9H55	
	Motorola	MC74H55	
	National	DM74H55	
	Signetics	74H55	
SN74H60	Fairchild	74H60	
		9H60	
	ITT	ITT74H60	
	Motorola	MC74H60	
	National	DM74H60	
	Signetics	74H60	
SN74H61	Fairchild	74H61	
		9H61	
	Motorola	MC74H61	
	National	DM74H61	
	Signetics	74H61	
SN74H62	Fairchild	74H62	
		9H62	
	Motorola	MC74H62	
	National	DM74H62	
	Signetics	74H62	
SN74H71	Fairchild	74H71	
		9H71	
	Motorola	MC74H71	
	National	DM74H71	
	Signetics	74H71	
SN74H72	Fairchild	74H72	
		9H72	
	ITT	ITT74H72	
	Motorola	MC74H72	
	National	DM74H72	
	Signetics	74H72	
SN74H73	Fairchild	74H73	
		9H73	
	ITT	ITT74H73	
	Motorola	MC74H73	
	National	DM74H73	
	Signetics	74H73	
SN74H74	Fairchild	74H74	
		9H74	
	ITT	ITT74H74	
	Motorola	MC74H74	
	National	DM74H74	
	Raytheon	74H74	
	Signetics	74H74	
SN74H76	Fairchild	74H76	
		9H76	
	Motorola	MC74H76	
	National	DM74H76	
	Signetics	74H76	
SN74H78	Fairchild	74H78	
		9H78	
	National	DM74H78	
SN74H87	Fairchild	74H87	
		93H87	
	Motorola	MC74H87	
SN74LS00	Fairchild	74LS00	
	ITT	ITT74LS00	
	Motorola	SN74LS00	
	National	DM74LS00	
	NEC America	μPB74LS00	
	Raytheon	74LS00	
	Signetics	74LS00	
SN74LS01	Fairchild	74LS01	
	ITT	ITT74LS01	
	National	DM74LS01	
	Raytheon	74LS01	
	Signetics	74LS01	
SN74LS02	Fairchild	74LS02	
	ITT	ITT74LS02	
	Motorola	SN74LS02	
	National	DM74LS02	
	NEC America	μPB74LS02	
	Raytheon	74LS02	
	Signetics	74LS02	
SN74LS03	Fairchild	74LS03	
	ITT	ITT74LS03	
	Motorola	SN74LS03	
	National	DM74LS03	
	NEC America	μPB74LS03	
	Raytheon	74LS03	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN74LS03	Signetics	74LS03	
SN74LS04	Fairchild	74LS04	
	ITT	ITT74LS04	
	Motorola	SN74LS04	
	National	DM74LS04	
	NEC America	μPB74LS04	
	Raytheon	74LS04	
	Signetics	74LS04	
SN74LS05	Fairchild	74LS05	
	ITT	ITT74LS05	
	Motorola	SN74LS05	
	National	DM74LS05	
	NEC America	μPB74LS05	
	Raytheon	74LS05	
	Signetics	74LS05	
SN74LS08	Fairchild	74LS08	
	ITT	ITT74LS08	
	Motorola	SN74LS08	
	National	DM74LS08	
	NEC America	μPB74LS08	
	Raytheon	74LS08	
	Signetics	74LS08	
SN74LS09	Fairchild	74LS09	
	ITT	ITT74LS09	
	Motorola	SN74LS09	
	National	DM74LS09	
	Raytheon	74LS09	
	Signetics	74LS09	
SN74LS10	Fairchild	74LS10	
	ITT	ITT74LS10	
	Motorola	SN74LS10	
	National	DM74LS10	
	NEC America	μPB74LS10	
	Raytheon	74LS10	
	Signetics	74LS10	
SN74LS107	Fairchild	74LS107	
	National	DM74LS107	
	Raytheon	74LS107	
	Signetics	74LS107	
SN74LS109	Fairchild	74LS109	
	ITT	ITT74LS109A	
	Motorola	SN74LS109	
	National	DM74LS109	
	NEC America	μPB74LS109	
	Raytheon	74LS109	
	Signetics	74LS109	
SN74LS11	Fairchild	74LS11	
	ITT	ITT74LS11	
	Motorola	SN74LS11	
	National	DM74LS11	
	NEC America	μPB74LS11	
	Raytheon	74LS11	
	Signetics	74LS11	
SN74LS112	Fairchild	74LS112	
	ITT	ITT74LS112	
	National	DM74LS112	
	NEC America	μPB74LS112	
	Raytheon	74LS112	
	Signetics	74LS112	
SN74LS113	Fairchild	74LS113	
	ITT	ITT74LS113	
	National	DM74LS113	
	NEC America	μPB74LS113	
	Raytheon	74LS113	
	Signetics	74LS113	
SN74LS114	Fairchild	74LS114	
	ITT	ITT74LS114	
	Motorola	SN74LS114	
	National	DM74LS114	
	Raytheon	74LS114	
	Signetics	74LS114	
SN74LS12	Fairchild	74LS12	
	National	DM74LS12	
	Raytheon	74LS12	
	Signetics	74LS12	
SN74LS122	National	DM74LS122	
	Raytheon	74LS122	275
SN74LS123	AMD	SN74LS123	
	ITT	ITT74LS123	
	National	DM74LS123	
	Raytheon	74LS123	275
SN74LS125A	Fairchild	74LS125	
	ITT	ITT74LS125	
SN74LS125A	National	DM74LS125	
	Raytheon	74LS125	
	Signetics	74LS125	
SN74LS126A	Fairchild	74LS126	
	ITT	ITT74LS126	
	Motorola	SN74LS126	
	National	DM74LS126	
	Raytheon	74LS126	
	Signetics	74LS126	
SN74LS13	Fairchild	74LS13	
	ITT	ITT74LS13	
	Motorola	SN74LS13	
	National	DM74LS13	
	Raytheon	74LS13	264
	Signetics	74LS13	
SN74LS132	Fairchild	74LS132	
	ITT	ITT74LS132	
	Motorola	SN74LS132	
	National	DM74LS132	
	Raytheon	74LS132	264
	Signetics	74LS132	
SN74LS133	ITT	ITT74LS133	
SN74LS136	Fairchild	74LS136	
	ITT	ITT74LS136	
	Motorola	SN74LS136	
	National	DM74LS136	
	Raytheon	74LS136	
	Signetics	74LS136	
SN74LS138	AMD	SN74LS138	
	Fairchild	74LS138	
	ITT	ITT74LS138	
	Motorola	SN74LS138	
	National	DM74LS138	
	NEC America	μPB74LS138	
	Raytheon	74LS138	
	Signetics	74LS138	
SN74LS139	AMD	SN74LS139	
	Fairchild	74LS139	
	ITT	ITT74LS139	
	Motorola	SN74LS139	
	National	DM74LS139	
	NEC America	μPB74LS139	
	Raytheon	74LS139	
	Signetics	74LS139	
SN74LS14	Fairchild	74LS14	
	ITT	ITT74LS14	
	Motorola	SN74LS14	
	National	DM74LS14	
	Raytheon	74LS14	264
	Signetics	74LS14	
SN74LS145	Fairchild	74LS145	
	Signetics	74LS145	
SN74LS148	AMD	SN74LS148	
SN74LS15	Fairchild	74LS15	
	ITT	ITT74LS15	
	Motorola	SN74LS15	
	National	DM74LS15	
	Raytheon	74LS15	
	Signetics	74LS15	
SN74LS151	AMD	SN74LS151	
	Fairchild	74LS151	
	ITT	ITT74LS151	
	Motorola	SN74LS151	
	National	DM74LS151	
	NEC America	μPB74LS151	
	Raytheon	74LS151	
	Signetics	74LS151	
SN74LS152	Fairchild	74LS152	
	Raytheon	74LS152	
SN74LS153	AMD	SN74LS153	
	Fairchild	74LS153	
	ITT	ITT74LS153	
	Motorola	SN74LS153	
	National	DM74LS153	
	NEC America	μPB74LS153	
	Raytheon	74LS153	
	Signetics	74LS153	
SN74LS155	Fairchild	74LS155	
	ITT	ITT74LS155	
	Motorola	SN74LS155	
	National	DM74LS155	
	NEC America	μPB74LS155	
	Raytheon	74LS155	
	Signetics	74LS155	
SN74LS156	Fairchild	74LS156	
	ITT	ITT74LS156	
SN74LS156	Motorola	SN74LS156	
	National	DM74LS156	
	Raytheon	74LS156	
	Signetics	74LS156	
SN74LS157	AMD	SN74LS157	
	Fairchild	74LS157	
	ITT	ITT74LS157	
	Motorola	SN74LS157	
	National	DM74LS157	
	NEC America	μPB74LS157	
	Raytheon	74LS157	
	Signetics	74LS157	
SN74LS158	AMD	SN74LS158	
	Fairchild	74LS158	
	ITT	ITT74LS158	
	Motorola	SN74LS158	
	National	DM74LS158	
	Raytheon	74LS158	
	Signetics	74LS158	
SN74LS160	AMD	SN74LS160	
	Fairchild	74LS160	
	ITT	ITT74LS160	
	Motorola	SN74LS160	
	National	DM74LS160	
	Raytheon	74LS160	
	Signetics	74LS160	
SN74LS161	AMD	SN74LS161	
	Fairchild	74LS161	
	ITT	ITT74LS161	
	Motorola	SN74LS161	
	National	DM74LS161	
	NEC America	μPB74LS161	
	Raytheon	74LS161	
		75LS161	
	Signetics	74LS161	
SN74LS162	AMD	SN74LS162	
	Fairchild	74LS162	
	ITT	ITT74LS162	
	Motorola	SN74LS162	
	National	DM74LS162	
	Raytheon	74LS162	
	Signetics	74LS162	
SN74LS163	AMD	SN74LS163	
	Fairchild	74LS163	
	ITT	ITT74LS163	
	Motorola	SN74LS163	
	National	DM74LS163	
	Raytheon	74LS163	
	Signetics	74LS163	
SN74LS164	AMD	SN74LS164	
	Fairchild	74LS164	
	ITT	ITT74LS164	
	Motorola	SN74LS164	
	National	DM74LS164	
	NEC America	μPB74LS164	
	Raytheon	74LS164	272
	Signetics	74LS164	
SN74LS165	Fairchild	74LS165	
SN74LS168	AMD	SN74LS168	
	Fairchild	74LS168	
	National	DM74LS168	
SN74LS169	AMD	SN74LS169	
	Fairchild	74LS169	
	National	DM74LS169	
SN74LS170	AMD	SN74LS170	
	Fairchild	74LS170	
	ITT	ITT74LS170	
	Motorola	SN74LS170	
	National	DM74LS170	
	Raytheon	74LS170	
	Signetics	74LS170	
SN74LS173	Fairchild	74LS173	
	National	DM74LS173	
	Signetics	74LS173	
SN74LS174	AMD	SN74LS174	
	Fairchild	74LS174	
	ITT	ITT74LS174	
	Motorola	SN74LS174	
	National	DM74LS174	
	Raytheon	74LS174	
	Signetics	74LS174	
SN74LS175	AMD	SN74LS175	
	Fairchild	74LS175	
	ITT	ITT74LS175	
SN74LS175	NEC America	μPB74LS175	
	Raytheon	74LS175	
	Signetics	74LS175	
SN74LS181	AMD	SN74LS181	
	Fairchild	74LS181	
	Motorola	SN74LS181	
	Raytheon	74LS181	
	Signetics	74LS181	
SN74LS190	AMD	SN74LS190	
	Fairchild	74LS190	
	ITT	ITT74LS190	
	Motorola	SN74LS190	
	National	DM74LS190	
	Raytheon	74LS190	
	Signetics	74LS190	
SN74LS191	AMD	SN74LS191	
	Fairchild	74LS191	
	ITT	ITT74LS191	
	Motorola	SN74LS191	
	National	DM74LS191	
	Raytheon	74LS191	
	Signetics	74LS191	
SN74LS192	AMD	SN74LS192	
	Fairchild	74LS192	
	ITT	ITT74LS192	
	Motorola	SN74LS192	
	National	DM74LS192	
	NEC America	μPB74LS192	
	Raytheon	74LS192	
	Signetics	74LS192	
SN74LS193	AMD	SN74LS193	
	Fairchild	74LS193	
	ITT	ITT74LS193	
	Motorola	SN74LS193	
	National	DM74LS193	
	NEC America	μPB74LS193	
	Raytheon	74LS193	
	Signetics	74LS193	
SN74LS194A	AMD	SN74LS194	
		SN74LS194A	
	Fairchild	74LS194	
	ITT	ITT74LS194A	
	Motorola	SN74LS194	
	NEC America	μPB74LS194	
	Raytheon	74LS194A	
	Signetics	74LS194A	
SN74LS195A	AMD	SN74LS195A	
	Fairchild	74LS195	
	ITT	ITT74LS195A	
	Motorola	SN74LS195	
	NEC America	μPB74LS195	
	Raytheon	74LS195A	
	Signetics	74LS195A	
SN74LS196	Fairchild	74LS196	
	ITT	ITT74LS196	
	Motorola	SN74LS196	
	National	DM74LS196	
	Raytheon	74LS196	
	Signetics	74LS196	
SN74LS197	Fairchild	74LS197	
	ITT	ITT74LS197	
	Motorola	SN74LS197	
	National	DM74LS197	
	Raytheon	74LS197	
	Signetics	74LS197	
SN74LS20	Fairchild	74LS20	
	ITT	ITT74LS20	
	Motorola	SN74LS20	
	National	DM74LS20	
	NEC America	μPB74LS20	
	Raytheon	74LS20	
	Signetics	74LS20	
SN74LS21	Fairchild	74LS21	
	ITT	ITT74LS21	
	Motorola	SN74LS21	
	National	DM74LS21	
	NEC America	μPB74LS21	
	Raytheon	74LS21	
	Signetics	74LS21	
SN74LS22	Fairchild	74LS22	
	ITT	ITT74LS22	
	Motorola	SN74LS22	
	National	DM74LS22	
	Raytheon	74LS22	
	Signetics	74LS22	
SN74LS221	Fairchild	74LS221	

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Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN74LS221	ITT	ITT74LS221	
	Motorola	SN74LS221	
	National	DM74LS221	
	Raytheon	**74LS221**	**275**
	Signetics	74LS221	
SN74LS240	AMD	SN74LS240	
	Fairchild	74LS240	
	ITT	ITT74LS240	
	MMI	74LS240	
	Motorola	SN74LS240	
	Raytheon	**74LS240**	**279**
	Signetics	74LS240	
SN74LS241	AMD	SN74LS241	
	Fairchild	74LS241	
	ITT	ITT74LS241	
	MMI	74LS241	
	Motorola	SN74LS241	
	Raytheon	**74LS241**	**279**
	Signetics	74LS241	
SN74LS242	AMD	SN74LS242	
	Fairchild	74LS242	
	ITT	ITT74LS242	
	Motorola	SN74LS242	
	Raytheon	**74LS242**	**282**
	Signetics	74LS242	
SN74LS243	AMD	SN74LS243	
	Fairchild	74LS243	
	ITT	ITT74LS243	
	Motorola	SN74LS243	
	Raytheon	**74LS243**	**282**
	Signetics	74LS243	
SN74LS244	AMD	SN74LS244	
	Fairchild	74LS244	
	ITT	ITT74LS244	
	MMI	74LS244	
	Motorola	SN74LS244	
	Raytheon	**74LS244**	**279**
	Signetics	74LS244	
SN74LS247	**Fairchild**	**74LS247**	
	National	DM74LS247	
SN74LS248	Fairchild	74LS248	
	National	DM74LS248	
SN74LS249	Fairchild	74LS249	
	National	DM74LS249	
SN74LS251	AMD	SN74LS251	
	Fairchild	74LS251	
	ITT	ITT74LS251	
	Motorola	SN74LS251	
	National	DM74LS251	
	NEC America	μPB74LS251	
	Raytheon	74LS251	
	Signetics	74LS251	
SN74LS253	AMD	SN74LS253	
	Fairchild	74LS253	
	ITT	ITT74LS253	
	Motorola	SN74LS253	
	National	DM74LS253	
	NEC America	μPB74LS253	
	Raytheon	74LS253	
	Signetics	74LS253	
SN74LS257	AMD	SN74LS257	
	Fairchild	74LS257	
	ITT	ITT74LS257	
	Motorola	SN74LS257	
	National	DM74LS257	
	NEC America	μPB74LS257	
	Raytheon	74LS257	
	Signetics	74LS257	
SN74LS258	AMD	SN74LS258	
	Fairchild	74LS258	
	ITT	ITT74LS258	
	Motorola	SN74LS258	
	National	DM74LS258	
	NEC America	μPB74LS258	
	Raytheon	74LS258	
	Signetics	74LS258	
SN74LS259	Fairchild	74LS259	
	ITT	ITT74LS259	
	Motorola	SN74LS259	
SN74LS26	Fairchild	74LS26	
	National	DM74LS26	
	Raytheon	74LS26	
	Signetics	74LS26	
SN74LS260	Fairchild	74LS260	
	Signetics	74LS260A	
SN74LS261	ITT	ITT74LS261	
	Raytheon	**74LS261**	**284**
	Signetics	74LS261	
SN74LS266	Fairchild	74LS266	
	ITT	ITT74LS266	
	Motorola	SN74LS266	
	Raytheon	74LS266	
	Signetics	74LS266	
SN74LS27	Fairchild	74LS27	
	ITT	ITT74LS27	
	Motorola	SN74LS27	
	National	DM74LS27	
	NEC America	μPB74LS27	
	Raytheon	74LS27	
	Signetics	74LS27	
SN74LS273	AMD	SN74LS273	
	Fairchild	74LS273	
	ITT	ITT74LS273	
	Signetics	74LS273	
SN74LS279	Fairchild	74LS279	
	ITT	ITT74LS279	
	Motorola	SN74LS279	
	National	DM74LS279	
	NEC America	μPB74LS279	
	Raytheon	74LS279	
	Signetics	74LS279	
SN74LS28	Fairchild	74LS28	
	ITT	ITT74LS28	
	Raytheon	74LS28	
	Signetics	74LS28	
SN74LS280	Fairchild	74LS280	
SN74LS281	AMD	SN74LS281	
SN74LS283	Fairchild	74LS283	
	ITT	ITT74LS283	
	Motorola	SN74LS283	
	National	DM74LS283	
	Raytheon	74LS283	
	Signetics	74LS283	
SN74LS290	Fairchild	74LS290	
	ITT	ITT74LS290	
	Motorola	SN74LS290	
	National	DM74LS290	
	Signetics	74LS290	
SN74LS293	Fairchild	74LS293	
	ITT	ITT74LS293	
	Motorola	SN74LS293	
	National	DM74LS293	
	Signetics	74LS293	
SN74LS295B	Fairchild	74LS295	
	Motorola	SN74LS295	
	NEC America	μPB74LS295	
	Raytheon	74LS295A	
	Signetics	74LS295	
SN74LS298	Fairchild	74LS298	
	Motorola	SN74LS298	
	Raytheon	74LS298	
	Signetics	74LS298	
SN74LS299	AMD	SN74LS299	
	Fairchild	74LS299	
	ITT	ITT74LS299	
	Raytheon	74LS299	
SN74LS30	Fairchild	74LS30	
	ITT	ITT74LS30	
	Motorola	SN74LS30	
	National	DM74LS30	
	NEC America	μPB74LS30	
	Raytheon	74LS30	
	Signetics	74LS30	
SN74LS32	Fairchild	74LS32	
	ITT	ITT74LS32	
	Motorola	SN74LS32	
	National	DM74LS32	
	NEC America	μPB74LS32	
	Raytheon	74LS32	
	Signetics	74LS32	
SN74LS322	AMD	AM25LS22	
		SN74LS322	
SN74LS323	AMD	AM25LS23	
		SN74LS323	
	ITT	ITT74LS323	
	Raytheon	74LS323	
SN74LS33	Raytheon	74LS33	
	Signetics	74LS33	
SN74LS352	Fairchild	74LS352	
SN74LS352	National	DM74LS352	
SN74LS353	Fairchild	74LS353	
	National	DM74LS353	
SN74LS365	Fairchild	74LS365	
	ITT	ITT74LS365	
	Motorola	SN74LS365	
	National	DM74LS365	
	NEC America	μPB74LS365	
	Raytheon	**74LS365**	**286**
	Signetics	74LS365	
SN74LS366	Fairchild	74LS366	
	ITT	ITT74LS366	
	Motorola	SN74LS366	
	National	DM74LS366	
	NEC America	μPB74LS366	
	Raytheon	**74LS366**	**286**
	Signetics	74LS366	
SN74LS367	Fairchild	74LS367	
	ITT	ITT74LS367	
	Motorola	SN74LS367	
	National	DM74LS367	
	NEC America	μPB74LS367	
	Raytheon	**74LS367**	**286**
	Signetics	74LS367	
SN74LS368	Fairchild	74LS368	
	ITT	ITT74LS368	
	Motorola	SN74LS368	
	National	DM74LS368	
	NEC America	μPB74LS368	
	Raytheon	**74LS368**	**286**
	Signetics	74LS368	
SN74LS37	Fairchild	74LS37	
	ITT	ITT74LS37	
	Motorola	SN74LS37	
	National	DM74LS37	
	NEC America	μPB74LS37	
	Raytheon	74LS37	
	Signetics	74LS37	
SN74LS373	AMD	SN74LS373	
	Fairchild	74LS373	
	ITT	ITT74LS373	
	MMI	74LS373	
	Raytheon	**74LS373**	**288**
	Signetics	74LS373	
SN74LS374	AMD	SN74LS374	
	Fairchild	74LS374	
	ITT	ITT74LS374	
	MMI	74LS374	
	National	DM74LS374	
	Raytheon	**74LS374**	**288**
SN74LS375	ITT	ITT74LS375	
	Motorola	SN74LS375	
	NEC America	μPB74LS375	
	Raytheon	74LS375	
	Signetics	74LS375	
SN74LS377	AMD	SN74LS377	
	Fairchild	74LS377	
	ITT	ITT74LS377	
	Raytheon	**74LS377**	**288**
	Signetics	74LS377	
SN74LS378	AMD	SN74LS378	
	Fairchild	74LS378	
	ITT	ITT74LS378	
	Signetics	74LS378	
SN74LS379	AMD	AM25LS08	
		SN74LS379	
SN74LS38	Fairchild	74LS38	
	ITT	ITT74LS38	
	Motorola	SN74LS38	
	National	DM74LS38	
	NEC America	μPB74LS38	
	Raytheon	74LS38	
	Signetics	74LS38	
SN74LS381	AMD	SN74LS381	
	ITT	ITT74LS381	
SN74LS384	AMD	AM25LS14	
		SN74LS384	
SN74LS385	AMD	AM25LS15	
		SN74LS385	
SN74LS386	Fairchild	74LS386	
	ITT	ITT74LS386	
	Motorola	SN74LS386	
	National	DM74LS386	
	Raytheon	74LS386	
	Signetics	74LS386	
SN74LS390	Fairchild	74LS390	
SN74LS393	Fairchild	74LS393	
SN74LS395	Fairchild	74LS395	
	National	DM74LS395	
	Raytheon	**74LS395**	**291**
	Signetics	74LS395	
SN74LS399	AMD	AM25LS09	
		SN74LS399	
SN74LS40	Fairchild	74LS40	
	ITT	ITT74LS40	
	Motorola	SN74LS40	
	National	DM74LS40	
	NEC America	μPB74LS40	
	Raytheon	74LS40	
	Signetics	74LS40	
SN74LS42	Fairchild	74LS42	
	ITT	ITT74LS42	
	Motorola	SN74LS42	
	National	DM74LS42	
	NEC America	μPB74LS42	
	Raytheon	**74LS42**	**266**
	Signetics	74LS42	
SN74LS424	AMD	SN74LS424	
	NEC Micro	**μPB8224**	**1764**
SN74LS490	Fairchild	74LS490	
SN74LS51	Fairchild	74LS51	
	ITT	ITT74LS51	
	Motorola	SN74LS51	
	National	DM74LS51	
	NEC America	μPB74LS51	
	Raytheon	74LS51	
	Signetics	74LS51	
SN74LS54	Fairchild	74LS54	
	ITT	ITT74LS54	
	Motorola	SN74LS54	
	National	DM74LS54	
	NEC America	μPB74LS54	
	Raytheon	74LS54	
	Signetics	74LS54	
SN74LS55	Fairchild	74LS55	
	Motorola	SN74LS55	
	National	DM74LS55	
	NEC America	μPB74LS55	
	Raytheon	74LS55	
	Signetics	74LS55	
SN74LS670	AMD	SN74LS670	
	Fairchild	74LS670	
	Motorola	SN74LS670	
	National	DM74LS670	
	Raytheon	74LS670	
	Signetics	74LS670	
SN74LS73	Fairchild	74LS73	
	ITT	ITT74LS73	
	Motorola	SN74LS73	
	National	DM74LS73	
	Raytheon	74LS73	
	Signetics	74LS73	
SN74LS74	Fairchild	74LS74	
	ITT	ITT74LS74	
	Motorola	SN74LS74	
	National	DM74LS74	
	NEC America	μPB74LS74	
	Raytheon	74LS74	
	Signetics	74LS74	
SN74LS75	Fairchild	74LS75	
	ITT	ITT74LS75	
	National	DM74LS75	
	Raytheon	74LS75	
	Signetics	74LS75	
SN74LS76	ITT	ITT74LS76	
	National	DM74LS76	
	Raytheon	74LS76	
	Signetics	74LS76	
SN74LS78	ITT	ITT74LS78	
	National	DM74LS78	
	Raytheon	74LS78	
	Signetics	74LS78	
SN74LS83A	Fairchild	74LS83	
	ITT	ITT74LS83A	
	Motorola	SN74LS83	
	National	DM74LS83	
		DM74LS83A	
	Raytheon	74LS83A	
	Signetics	74LS83	
		74LS83A	
SN74LS85	Fairchild	74LS85	
	ITT	ITT74LS85	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN74LS85	Motorola	SN74LS85	
	National	DM74LS85	
	Raytheon	74LS85	
	Signetics	74LS85	
SN74LS86	Fairchild	74LS86	
	ITT	ITT74LS86	
	Motorola	SN74LS86	
	NEC America	μPB74LS86	
	Raytheon	74LS86	
	Signetics	74LS86	
SN74LS90	Fairchild	74LS90	
	ITT	ITT74LS90	
	Motorola	SN74LS90	
	Raytheon	**74LS90**	**268**
	Signetics	74LS90	
SN74LS91	**Raytheon**	**74LS91**	**272**
SN74LS92	Fairchild	74LS92	
	Motorola	SN74LS92	
	Raytheon	**74LS92**	**268**
	Signetics	74LS92	
SN74LS93	Fairchild	74LS93	
	ITT	ITT74LS93	
	Motorola	SN74LS93	
	Raytheon	**74LS93**	**268**
	Signetics	74LS93	
SN74LS95B	Fairchild	74LS95	
	ITT	ITT74LS95B	
	Motorola	SN74LS95	
	Raytheon	74LS95B	
	Signetics	74LS95B	
SN74LS96	ITT	ITT74LS96	
	Signetics	74LS96	
SN74L00	National	DM74L00	
SN74L01	National	DM74L01	
SN74L02	National	DM74L02	
SN74L03	National	DM74L03	
SN74L04	National	DM74L04	
SN74L10	National	DM74L10	
SN74L123	National	DM74L123	
SN74L154	National	DM74L154A	
SN74L157	National	DM74L157A	
SN74L164	National	DM74L164	
SN74L192	National	DM74L192	
SN74L193	National	DM74L193	
SN74L20	National	DM74L20	
SN74L30	National	DM74L30	
SN74L42	National	DM74L42A	
SN74L51	National	DM74L51	
SN74L54	National	DM74L54	
SN74L55	National	DM74L55	
SN74L71	National	DM74L71	
SN74L72	National	DM74L72	
SN74L73	National	DM74L73	
SN74L74	National	DM74L74	
♦SN74L75	National	DM74L75	
SN74L78	National	DM74L78	
SN74L85	National	DM74L85	
SN74L86	National	DM74L86	
SN74L90	National	DM74L90	
SN74L91	National	DM74L91	
SN74L93	National	DM74L93	
SN74L95	National	DM74L95	
SN74L98	National	DM74L98	
SN74S00	Fairchild	74S00	
		9S00	
	Hitachi	HD74S00	
	Mitsubishi	M5S000	
	National	DM74S00	
	Signetics	74S00	
SN74S02	**MMI**	**74S373**	**460**
	TI	SN74S373	
SN74S03	Fairchild	74S03	
		9S03	
	Hitachi	HD74S03	
	Mitsubishi	M5S003	
	National	DM74S03	
	Signetics	74S03	
SN74S04	Fairchild	74S04	
		9S04	
	Hitachi	HD74S04	
	Mitsubishi	M5S004	
	National	DM74S04	
	Signetics	74S04	
SN74S05	Fairchild	74S05	
		9S05	
	Hitachi	HD74S05	
	Mitsubishi	M5S005	
	National	DM74S05	
	Signetics	74S05	
SN74S08	Fairchild	74S08	
	Signetics	74S08	
SN74S09	Fairchild	74S09	
	Signetics	74S09	
SN74S10	Fairchild	74S10	
	Hitachi	HD74S10	
	Mitsubishi	M5S010	
	National	DM74S10	
	Signetics	74S10	
SN74S109	Fairchild	9S109	
SN74S11	Fairchild	74S11	
		9S11	
	Hitachi	HD74S11	
	Mitsubishi	M5S011	
	National	DM74S11	
	Signetics	74S11	
SN74S112	Fairchild	74S112	
		9S112	
	Hitachi	HD74S112	
	Mitsubishi	M5S112	
	Motorola	SN74S112	
	National	DM74S112	
	Signetics	74S112	
SN74S113	Fairchild	74S113	
		9S113	
	Hitachi	HD74S113	
	Mitsubishi	M5S113	
	Motorola	SN74S113	
	National	DM74S113	
	Signetics	74S113	
SN74S114	Fairchild	74S114	
		9S114	
	Hitachi	HD74S114	
	Mitsubishi	M5S114	
	National	DM74S114	
	Signetics	74S114	
SN74S132	Fairchild	74S132	
SN74S133	Fairchild	74S133	
		9S133	
	Hitachi	HD74S133	
	Mitsubishi	M5S133	
	National	DM74S133	
	Signetics	74S133	
SN74S134	Fairchild	74S134	
		9S134	
	Hitachi	HD74S134	
	National	DM74S134	
	Signetics	74S134	
SN74S135	Fairchild	74S135	
	Hitachi	HD74S135	
	National	DM74S135	
	Signetics	74S135	
SN74S138	AMD	SN74S138	
	Fairchild	74S138	
	Mitsubishi	M5S138	
	National	DM74S138	
	Signetics	74S138	
SN74S139	AMD	SN74S139	
	Fairchild	74S139	
	National	DM74S139	
	Signetics	74S139	
SN74S140	Fairchild	74S140	
		9S140	
	Hitachi	HD74S140	
	National	DM74S140	
	Signetics	74S140	
SN74S15	Fairchild	74S15	
	Hitachi	HD74S15	
	Mitsubishi	M5S015	
	National	DM74S15	
	Signetics	74S15	
SN74S151	AMD	SN74S151	
	Fairchild	74S151	
	Hitachi	HD74S151	
	Mitsubishi	M5S151	
	National	DM74S151	
	Signetics	74S151	
SN74S153	AMD	SN74S153	
	Fairchild	74S153	
		93S153	
SN74S153	Mitsubishi	M5S153	
	National	DM74S153	
	Signetics	74S153	
SN74S157	AMD	SN74S157	
	Fairchild	74S157	
		93S157	
	Mitsubishi	M5S157	
	National	DM74S157	
	Signetics	74S157	
SN74S158	AMD	SN74S158	
	Fairchild	74S158	
		93S158	
	Mitsubishi	M5S158	
	National	DM74S158	
	Signetics	74S158	
SN74S174	AMD	SN74S174	
	Fairchild	74S174	
	Hitachi	HD74S174	
	Mitsubishi	M5S174	
	National	DM74S174	
	Signetics	74S174	
SN74S175	AMD	SN74S175	
	Fairchild	74S175	
		93S175	
	Hitachi	HD74S175	
	Mitsubishi	M5S175	
	National	DM74S175	
	Signetics	74S175	
SN74S181	AMD	SN74S181	
	Fairchild	74S181	
		93S41	
	Hitachi	HD74S181	
	Mitsubishi	M5S181	
	Signetics	74S181	
SN74S182	Fairchild	74S182	
	Mitsubishi	M5S182	
	National	DM74S182	
	Signetics	74S182	
SN74S188	AMD	AM27S09	
	Harris	**HM7602**	**1192**
	MMI	**6330**	**1252**
	Signetics	N82S23	
SN74S189	AMD	AM27S03	
		SN74S189	
	Fairchild	93405	
	National	**DM74S189**	**1292**
SN74S194	AMD	SN74S194	
	Fairchild	74S194	
		93S194	
	Signetics	74S194	
SN74S195	AMD	SN74S195	
	Fairchild	74S195	
		93S00	
	National	DM74S195	
	Signetics	74S195	
SN74S196	Fairchild	82S90	
SN74S197	Fairchild	82S91	
	Signetics	74S197	
SN74S20	Fairchild	74S20	
		9S20	
	Hitachi	HD74S20	
	Mitsubishi	M5S020	
	National	DM74S20	
	Signetics	74S20	
SN74S200	Fairchild	93421	
	MMI	6531	
	National	DM74S200	
	NEC Micro	μPB2200	
	Raytheon	RC5340	
	Signetics	74S200	
	TI	SN74S201	
SN74S201	MMI	6531	
	National	DM74S200	
	NEC Micro	μPB2202	
	Signetics	74S201	
SN74S206	Fairchild	93411	
	MMI	**6205**	**1252**
	National	**DM74S206**	**1297**
	Raytheon	RC5330	
	Signetics	N82S17	
	TI	SN74S301	
SN74S22	Fairchild	74S22	
		9S22	
	Hitachi	HD74S22	
	Mitsubishi	M5S22	
	National	DM74S22	
SN74S22	Signetics	74S22	
SN74S240	AMD	SN74S240	
	MMI	**74S240**	**462**
	Raytheon	74S240	
SN74S241	AMD	SN74S241	
	MMI	**74S241**	**462**
	Raytheon	74S241	
SN74S251	AMD	SN74S251	
	Fairchild	74S251	
	Hitachi	HD74S251	
	Mitsubishi	M5S251	
	National	DM74S251	
	Signetics	74S251	
SN74S257	AMD	SN54S257	
		SN74S257	
	Fairchild	54S257	
		74S257	
	Mitsubishi	M5S257	
	National	DM74S257	
	Signetics	54S257	
		74S257	
SN74S258	AMD	SN74S258	
	Fairchild	74S258	
		93S258	
	Mitsubishi	M5S258	
	Signetics	74S258	
SN74S270	Intersil	IM5604	
	MMI	**6205**	**1252**
	Signetics	82S130	
SN74S280	National	DM74S280	
	Signetics	74S280	
SN74S281	National	DM74S281	
SN74S287	**Harris**	**HM7611**	**1192**
		HM7611A	**1200**
	Intel	3621-1	
	Intersil	IM5623	
	MMI	**6301**	**1252**
	National	**DM74S287**	**1264**
	Signetics	N82S129	
SN74S288	**Harris**	**HM7603**	**1192**
	MMI	**6331**	**1252**
	National	DM8578	
	Signetics	N82S123	
SN74S289	AMD	SN74S289	
	Fairchild	93404	
	National	DM74S289	
	NEC Micro	μPB2089	
		μPB2289	
	Signetics	N82S25	
		3101A	
SN74S30	Fairchild	74S30	
	Mitsubishi	M5S030	
	National	DM74S30	
SN74S301	**National**	**DM74S206**	**1297**
	NEC Micro	μPB2200	
	Signetics	74S301	
SN74S314	**NEC Micro**	**μPB2205**	**1418**
SN74S32	Fairchild	74S02	
	National	DM74S02	
	Signetics	74S02	
SN74S37	Signetics	74S37	
SN74S370	**MMI**	**6206**	**1252**
	Signetics	82S131	
SN74S373	**MMI**	**74S373**	**460**
	TI	SN74S02	
SN74S374	**MMI**	**74S374**	**460**
SN74S387	**Harris**	**HM7610**	**1192**
		HM7610A	**1200**
	Intel	3601-1	
	MMI	**6300**	**1252**
	National	**DM74S387**	**1264**
	NEC Micro	**μPB403**	**1462**
	Signetics	N82S126	
SN74S40	Fairchild	74S40	
		9S40	
	Hitachi	HD74S40	
	Mitsubishi	M5S040	
	National	DM74S40	
	Signetics	74S40	
SN74S412	AMD	SN74S412	
	NEC Micro	**μPB8212**	**1804**
SN74S428	**NEC Micro**	**μPB8228**	**1769**
SN74S438	**NEC Micro**	**μPB8238**	**1769**
SN74S44	**NEC Micro**	**μPB425**	**1466**
SN74S470	**MMI**	**6308-1**	**1248**
	National	DM74S470	

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN74S471	**MMI**	**6309-1**	**1248**
	National	DM74S471	
SN74S472	**Harris**	**HM7649**	**1218**
	MMI	**6349-1**	**1248**
	National	DM74S472	
SN74S473	**Harris**	**HM7648**	**1218**
	MMI	**6348-1**	**1248**
	National	**DM74S473**	**1272**
SN74S475	NEC Micro	μPB405	
SN74S51	Fairchild	74S51	
	Mitsubishi	M5S051	
	National	DM74S51	
	Signetics	74S51	
SN74S64	Fairchild	74S64	
		9S64	
	Hitachi	HD74S64	
	National	DM74S64	
	Signetics	74S64	
SN74S65	Fairchild	74S65	
		9S65	
	Hitachi	HD74S65	
	National	DM74S65	
	Signetics	74S65	
SN74S74	Fairchild	74S74	
		9S74	
	Hitachi	HD74S74	
	Mitsubishi	M5S074	
	National	DM74S74	
	Signetics	74S74	
SN74S85	Mitsubishi	M5S085	
	Signetics	74S85	
SN74S86	Fairchild	74S86	
	Hitachi	HD74S86	
	National	DM74S86	
	Signetics	74S86	
SN7400	Fairchild	7400	
		9N00	
	Hitachi	HD2503	
		HD7400	
	ITT	ITT7400	
	Mitsubishi	M53200	
	Motorola	MC7400	
	National	DM7400	
	NEC America	μPB7400	
	Raytheon	7400	
	Signetics	7400	
	Toshiba	TC7400	
	TRW	7400	
SN7401	Fairchild	7401	
		9N01	
	Hitachi	HD2509	
	ITT	ITT7401	
	Mitsubishi	M53201	
	Motorola	MC7401	
	National	DM7401	
	Raytheon	7401	
	Signetics	7401	
	TRW	7401	
SN7402	Fairchild	7402	
		9N02	
	Hitachi	HD2511	
		HD7402	
	ITT	ITT7402	
	Mitsubishi	M53202	
	Motorola	MC7402	
	National	DM7402	
	NEC America	μPB7402	
	Signetics	7402	
	TRW	7402	
SN7403	Fairchild	7403	
		9N03	
	Hitachi	HD2528	
		HD7403	
	ITT	ITT7403	
	Mitsubishi	M53203	
	Motorola	MC7403	
	National	DM7403	
	Raytheon	7403	
	Signetics	7403	
	TRW	7403	
SN7404	Fairchild	7404	
		9N04	
	Hitachi	HD2522	
SN7404	Hitachi	HD7404	
	ITT	ITT7404	
	Mitsubishi	M53204	
	Motorola	MC7404	
	National	DM7404	
	NEC America	μPB7404	
	Raytheon	7404	
	Signetics	7404	
	Toshiba	TC7404	
	TRW	7404	
SN7405	Fairchild	7405	
		9N05	
	Hitachi	HD2523	
		HD7405	
	ITT	ITT7405	
	Mitsubishi	M53205	
	Motorola	MC7405	
	National	DM7405	
	NEC America	μPB7405	
	Raytheon	7405	
	Signetics	7405	
	TRW	7405	
SN7406	Fairchild	7406	
		9N06	
	Hitachi	HD7406	
	ITT	ITT7406	
	Mitsubishi	M53206	
	Motorola	MC7406	
	National	DM7406	
	Signetics	7406	
	TRW	7406	
SN7407	Fairchild	7407	
		9N07	
	Hitachi	HD7407	
	ITT	ITT7407	
	Mitsubishi	M53207	
	Motorola	MC7407	
	National	DM7407	
	Signetics	7407	
	TRW	7407	
SN7408	Fairchild	7408	
		9N08	
	Hitachi	HD2550	
	ITT	ITT7408	
	Mitsubishi	M53208	
	Motorola	MC7408	
	National	DM7408	
	Raytheon	7408	
	Signetics	7408	
	Toshiba	TC7408	
	TRW	7408	
SN7409	Fairchild	7409	
		9N09	
	Hitachi	HD2551	
		HD7409	
	ITT	ITT7409	
	Mitsubishi	M53209	
	Motorola	MC7409	
	National	DM7409	
	Raytheon	7409	
	Signetics	7409	
	TRW	7409	
SN7410	Fairchild	7410	
		9N10	
	Hitachi	HD2507	
		HD7410	
	ITT	ITT7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
	National	DM7410	
	NEC America	μPB7410	
	Raytheon	7410	
	Signetics	7410	
	TI	SN7427	
	Toshiba	TC7410	
	TRW	7410	
SN74100	Motorola	MC74100	
	Signetics	74100	
♦SN74104	TI	SN29000	
♦SN74105	TI	SN29001	
SN74107	AMD	SN74107	
	Fairchild	74107	
		9N107	
	Hitachi	HD2530	
		HD74107	
	ITT	ITT74107	
SN74107	Mitsubishi	M53307	
	Motorola	MC74107	
	National	DM74107	
	NEC America	μPB74107	
	Signetics	74107	
SN74109	Fairchild	74109	
	National	DM74109	
	Signetics	74109	
SN74111	TRW	74111	
SN74116	Fairchild	74116	
	Signetics	74116	
SN7412	Fairchild	7412	
		9N12	
	Hitachi	HD7412	
	ITT	ITT7412	
	Motorola	MC7412	
	Raytheon	7412	
	Signetics	7412	
	TRW	7412	
SN74120	Motorola	MC74120	
SN74121	Fairchild	74121	
		9603	
	Hitachi	HD2543	
		HD74121	
	ITT	ITT74121	
	Mitsubishi	M53321	
	Motorola	MC74121	
	National	DM74121	
	Signetics	74121	
	TRW	74121	
SN74122	Fairchild	74122	
	ITT	ITT74122	
	Mitsubishi	M53322	
	Motorola	MC74122	
	National	DM74122	
	Signetics	74122	
		8T22	
SN74123	AMD	AM26123	
		SN74123	
	Fairchild	74123	
	Hitachi	HD2561	
	ITT	ITT74123	
	Mitsubishi	M53323	
	Motorola	MC74123	
	National	DM74123	
	NEC America	μPB74123	
	Raytheon	74123	
	Signetics	74123	
	TRW	74123	
SN74125	Fairchild	74125	
	Hitachi	HD74125	
	Mitsubishi	M53325	
	National	DM74125	
		DM8093	
	Signetics	74125	
SN74126	Fairchild	74126	
	Hitachi	HD74126	
	Mitsubishi	M53326	
	National	DM74126	
	Signetics	74126	
SN74128	Signetics	74128	
SN74129	National	DM74193	
SN7413	Fairchild	7413	
		9N13	
	Hitachi	HD2545	
	ITT	ITT7413	
	Mitsubishi	M53213	
	Motorola	MC7413	
	National	DM7413	
	NEC America	μPB7413	
	Signetics	7413	
	TRW	7413	
SN74132	Fairchild	74132	
	Hitachi	HD74132	
	Mitsubishi	M53332	
	Motorola	MC74132	
	National	DM74132	
	Signetics	74132	
SN74136	Hitachi	HD74136	
	Motorola	MC74136	
	Raytheon	74136	
	TRW	74136	
SN7414	Fairchild	7414	
	Hitachi	HD7414	
	Mitsubishi	M53214	
	Motorola	MC7414	
SN7414	National	DM7414	
	Signetics	7414	
SN74141	Fairchild	74141	
		93141	
	Hitachi	HD2558	
	Motorola	MC74141	
	National	DM74141	
		DM7441	
	NEC America	μPB74141	
	Signetics	74141	
		7441	
SN74145	Fairchild	74145	
		93145	
	Hitachi	HD2555	
	ITT	ITT74145	
	Mitsubishi	M53345	
	Motorola	MC74145	
	National	DM74145	
	Raytheon	74145	
	Signetics	74145	
	TRW	74145	
SN74147	Hitachi	HD74147	
	Mitsubishi	M53347	
	National	DM74147	
	NEC America	μPB74147	
	Signetics	74147	
SN74148	Hitachi	HD74148	
	Mitsubishi	M53348	
	National	DM74148	
	NEC America	μPB74148	
	Signetics	74148	
SN74150	Fairchild	74150	
		93150	
	Hitachi	HD2548	
		HD74150	
	Mitsubishi	M53350	
	Motorola	MC74150	
	National	DM74150	
	NEC America	μPB74150	
	Raytheon	74150	
	Signetics	74150	
	TRW	74150	
SN74151	Fairchild	74151	
♦SN74151	Fairchild	74151	
		93151	
	Hitachi	HD2549	
		HD74151	
	ITT	ITT74151	
	Mitsubishi	M53351	
	Motorola	MC74151	
	National	DM74151	
	NEC America	μPB74151	
	Raytheon	74151	
	Signetics	74151	
	TI	SN74151A	
	TRW	74151	
♦SN74152	Fairchild	74152	
		93152	
	Motorola	MC74152	
	Raytheon	74152	
	TRW	74152	
SN74153	AMD	SN74153	
	Fairchild	74153	
		93153	
	Hitachi	HD2564	
	ITT	ITT74153	
	Mitsubishi	M53353	
	Motorola	MC74153	
	National	DM74153	
	NEC America	μPB74153	
	Raytheon	74153	
	Signetics	74153	
	TRW	74153	
SN74154	AMD	SN74154	
	Fairchild	74154	
		9311	
	Hitachi	HD2580	
	Mitsubishi	M53354	
	Motorola	MC74154	
	National	DM74154	
	NEC America	μPB74154	
	Raytheon	74154	
	Signetics	74154	
	TRW	74154	
SN74155	Fairchild	74155	
		93155	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Texas Instruments (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
SN74155	ITT	ITT74155	
	Mitsubishi	M53355	
	Motorola	MC74155	
	National	DM74155	
	NEC America	μPB74155	
	Raytheon	74155	
	Signetics	74155	
	TRW	74155	
SN74156	Fairchild	74156	
		93156	
	Hitachi	HD74156	
	ITT	ITT74156	
	Mitsubishi	M53356	
	Motorola	MC74156	
	National	DM74156	
	NEC America	μPB74156	
	Raytheon	74156	
	Signetics	74156	
	TRW	74156	
SN74157	AMD	SN74157	
	Fairchild	74157	
		9322	
	Hitachi	HD74157	
	ITT	ITT74157	
		ITT9322	
	Mitsubishi	M53357	
	Motorola	MC74157	
	National	DM74157	
		DM8322	
	NEC America	μPB74157	
	Raytheon	74157	
	Signetics	74157	
SN74159	Raytheon	74159	
SN7416	Fairchild	7416	
		9N16	
	Hitachi	HD7416	
	ITT	ITT7416	
	Mitsubishi	M53216	
	Motorola	MC7416	
	National	DM7416	
	Signetics	7416	
	TRW	7416	
SN74160	AMD	SN74160	
	Fairchild	74160	
		9310	
	Hitachi	HD74160	
	ITT	ITT74160	
	Mitsubishi	M53360	
	Motorola	MC74160	
	National	DM74160	
	Raytheon	74160	
	Signetics	74160	
	TRW	74160	
SN74161	AMD	SN74161	
	Fairchild	74161	
		9316	
	Hitachi	HD74161	
	ITT	ITT74161	
		ITT9316	
	Mitsubishi	M53361	
	Motorola	MC74161	
	National	DM74161	
	NEC America	μPB74161	
	Raytheon	74161	
	Signetics	74161	
	TRW	74161	
SN74162	AMD	SN74162	
	Fairchild	74162	
	Hitachi	HD74162	
	ITT	ITT74162	
	Mitsubishi	M53362	
	Motorola	MC74162	
	National	DM74162	
	Raytheon	74162	
	Signetics	74162	
	TRW	74162	
SN74163	AMD	SN74163	
	Fairchild	74163	
	Hitachi	HD74163	
	ITT	ITT74163	
	Mitsubishi	M53363	
	Motorola	MC74163	
	National	DM74163	
SN74163	Raytheon	74163	
	Signetics	74163	
	TRW	74163	
SN74164	AMD	SN74164	
		74164	
	Fairchild	74164	
		93164	
	Hitachi	HD74164	
	ITT	ITT74164	
	Mitsubishi	M53364	
	National	DM74164	
		DM8570	
	NEC America	μPB74164	
	Raytheon	74164	
	Signetics	74164	
SN74165	Fairchild	74165	
		93165	
	Mitsubishi	M53365	
	Motorola	MC74165	
	National	DM74165	
		DM8590	
	Raytheon	74165	
	Signetics	74165	
SN74166	Fairchild	74166	
		93166	
	Hitachi	HD74166	
	Mitsubishi	M53366	
	Motorola	MC74166	
	National	DM74166	
	Raytheon	74166	
	Signetics	74166	
SN74167	Motorola	MC74167	
SN7417	Fairchild	7417	
		9N17	
	Hitachi	HD7417	
	ITT	ITT7417	
	Mitsubishi	M53217	
	Motorola	MC7417	
	National	DM7417	
	Signetics	7417	
	TRW	7417	
SN74170	Fairchild	74170	
	Hitachi	HD2540	
	Mitsubishi	M53370	
	National	DM74170	
	NEC America	μPB74170	
	Raytheon	74170	
	Signetics	74170	
SN74172	Signetics	74172	
SN74173	Fairchild	74173	
	National	DM74173	
		DM8551	
SN74174	AMD	SN74174	
	Fairchild	74174	
		93174	
	Hitachi	HD74174	
	Mitsubishi	M53374	
	Motorola	MC74174	
	National	DM74174	
	Raytheon	74174	
	Signetics	74174	
SN74175	AMD	SN74175	
	Fairchild	74175	
		93175	
	Hitachi	HD74175	
	Mitsubishi	M53375	
	Motorola	MC74175	
	National	DM74175	
	NEC America	μPB74175	
	Raytheon	74175	
	Signetics	74175	
SN74176	Fairchild	74176	
		82S90	
		93176	
	Mitsubishi	M53376	
	Motorola	MC74176	
	National	DM74176	
		DM8280	
	Signetics	N8280	
		74176	
SN74177	Fairchild	74177	
		82S91	
		93177	
	Mitsubishi	M53377	
	Motorola	MC74177	
	National	DM74177	
SN74177	National	DM8281	
	Signetics	N8281	
		74177	
SN74178	Fairchild	74178	
		82S70	
		93178	
	Motorola	MC74178	
	Signetics	N8270	
SN74179	Fairchild	74179	
		82S72	
		93179	
	Motorola	MC74179	
	Signetics	N8271	
SN74180	Fairchild	74180	
		93180	
	Hitachi	HD2525	
		HD74180	
	ITT	ITT74180	
	Mitsubishi	M53380	
	Motorola	MC74180	
	National	DM74180	
	NEC America	μPB74180	
	Raytheon	74180	
	Signetics	74180	
	TRW	74180	
SN74181	AMD	SN74181	
		9341	
	Fairchild	74181	
		9341	
	Hitachi	HD2547	
	Mitsubishi	M53381	
	Motorola	MC74181	
	National	DM74181	
	NEC America	μPB74181	
	Raytheon	74181	
	Signetics	74181	
SN74182	AMD	SN74182	
		9342	
	Fairchild	74182	
		9342	
	Hitachi	HD2562	
	ITT	ITT74182	
	Mitsubishi	M53382	
	Motorola	MC74182	
	National	DM74182	
	NEC America	μPB74182	
	Raytheon	74182	
	Signetics	74182	
SN74184	National	DM74184	
SN74185	Mitsubishi	M53385	
	National	DM74185	
SN74185A	National	DM74185A	
SN74186	Harris	HPROM0512	
SN74187	Intersil	IM5603	
	MMI	**6200**	**1252**
	National	DM74187	
	Signetics	N82S226	
SN74188	Harris	HPROM8256	
	Intersil	IM5600	
	Signetics	N82S23	
	TI	SN74188A	
SN74188A	**MMI**	**6330**	**1252**
	National	DM8577	
SN74190	Fairchild	74190	
		93190	
	Hitachi	HD74190	
	ITT	ITT74190	
	Mitsubishi	M53390	
	Motorola	MC74190	
	National	DM74190	
	Raytheon	74190	
	Signetics	74190	
SN74191	Fairchild	74191	
		93191	
	Hitachi	HD74191	
	ITT	ITT74191	
	Mitsubishi	M53391	
	Motorola	MC74191	
	National	DM74191	
	Raytheon	74191	
	Signetics	74191	
SN74192	AMD	SN74192	
		9360	
	Fairchild	74192	
		9360	
	ITT	ITT74192	
SN74192	Mitsubishi	M53392	
	Motorola	MC74192	
	National	DM74192	
		DM8560	
	NEC America	μPB74192	
	Raytheon	74192	
	Signetics	74192	
SN74193	AMD	SN74193	
		9366	
	Fairchild	74193	
		9366	
	ITT	ITT74193	
	Mitsubishi	M53393	
	Motorola	MC74193	
	National	DM74193	
		DM8563	
	NEC America	μPB74193	
	Raytheon	74193	
	Signetics	74193	
SN74194	AMD	SN74194	
	Fairchild	74194	
	Hitachi	HD74194	
	ITT	ITT74194	
	Motorola	MC74194	
	National	DM74194	
	Raytheon	74194	
	Signetics	74194	
SN74195	AMD	SN74195	
	Fairchild	74195	
		9300	
	ITT	ITT74195	
		ITT9300	
	Motorola	MC74195	
	National	DM74195	
		DM8300	
	NEC America	μPB74195	
	Raytheon	74195	
	Signetics	74195	
SN74196	Fairchild	74196	
		82S90	
		93196	
	Motorola	MC74196	
	National	DM74196	
	Signetics	N8290	
		74196	
SN74197	Fairchild	74197	
		82S91	
		93197	
	Motorola	MC74197	
	National	DM74197	
	Signetics	N8291	
		74197	
SN74198	Fairchild	74198	
		93198	
	Hitachi	HD74198	
	Mitsubishi	M53398	
	Motorola	MC74198	
	National	DM74198	
	NEC America	μPB74198	
	Raytheon	74198	
	Signetics	74198	
SN74199	Fairchild	74199	
		93199	
	Mitsubishi	M53399	
	Motorola	MC74199	
	National	DM74199	
	Raytheon	74199	
	Signetics	74199	
SN7420	Fairchild	7420	
		9N20	
	Hitachi	HD2504	
		HD7420	
	ITT	ITT7420	
	Mitsubishi	M53220	
	Motorola	MC7420	
	National	DM7420	
	NEC America	μPB7420	
	Raytheon	7420	
	Signetics	7420	
	Toshiba	TC7420	
	TRW	7420	
SN74200	Fairchild	93421	
	MMI	6531	
	Raytheon	RC5340	
	Signetics	N82S06	
	TI	SN74S201	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN74206	Intersil	IM5533	
	MMI	6530	
	National	**DM74S206**	**1297**
	Raytheon	RC5330	
	TI	SN74S301	
SN7422	Fairchild	7422	
	Hitachi	HD7422	
	Raytheon	7422	
SN74221	AMD	SN74221	
SN7423	Fairchild	7423	
		9N23	
	Motorola	MC7423	
	National	DM7423	
SN7425	Fairchild	7425	
		9N25	
	ITT	ITT7425	
	Mitsubishi	M53225	
	Motorola	MC7425	
	National	DM7425	
SN74251	National	DM74251	
SN74259	AMD	SN74259	
SN7426	Fairchild	7426	
		9N26	
	Hitachi	HD2560	
		HD7426	
	ITT	ITT7426	
	Motorola	MC7426	
	National	DM7426	
	Signetics	N8T18	
		7426	
	TRW	7426	
SN7427	Fairchild	7410	
		7427	
		9N27	
	Hitachi	HD7410	
	ITT	ITT7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
		MC7427	
	National	DM7410	
		DM7427	
	NEC America	μPB7410	
	Raytheon	7410	
	Signetics	7410	
	TI	SN7410	
	Toshiba	TC7410	
	TRW	7410	
SN74270	**MMI**	**6205**	**1252**
SN74278	Mitsubishi	M53478	
SN74279	Fairchild	74279	
	Signetics	74279	
SN7428	Signetics	7428	
SN74283	Fairchild	74283	
	Mitsubishi	M53483	
	NEC America	μPB74283	
	Raytheon	74283	
SN74284	National	DM8875A	
SN74285	National	DM8875B	
SN74287	Fairchild	93426	
SN74290	Fairchild	74290	
	Mitsubishi	M53490	
	Motorola	MC74290	
	TRW	74290	
SN74293	Fairchild	74293	
	Mitsubishi	M53493	
	Motorola	MC74293	
	TRW	74293	
SN74298	Fairchild	74298	
	Motorola	MC74298	
	Signetics	74298	
SN7430	Fairchild	7430	
		9N30	
	Hitachi	HD2508	
		HD7430	
	ITT	ITT7430	
	Mitsubishi	M53230	
	Motorola	MC7430	
	National	DM7430	
	NEC America	μPB7430	
	Signetics	7430	
	TRW	7430	
SN7432	Fairchild	7432	
		9N32	
SN7432	Hitachi	HD7432	
	ITT	ITT7432	
	National	DM7432	
	Signetics	7432	
SN7433	Signetics	7433	
SN74365	National	DM8095	
SN74366	National	DM8096	
SN74367	National	DM8097	
SN74368	National	DM8098	
SN7437	Fairchild	7437	
		9N37	
	Hitachi	HD2552	
	ITT	ITT7437	
	Mitsubishi	M53237	
	Motorola	MC7437	
	National	DM7437	
	NEC America	μPB7437	
	Raytheon	7437	
	Signetics	7437	
	TRW	7437	
SN74370	**MMI**	**6206**	**1252**
SN7438	Fairchild	7438	
		9N38	
	Hitachi	HD2544	
	ITT	ITT7438	
	Mitsubishi	M53238	
	Motorola	MC7438	
	National	DM7438	
	NEC America	μPB7438	
	Raytheon	7438	
	Signetics	7438	
	TRW	7438	
SN74387	Fairchild	93416	
SN7440	Fairchild	7440	
		9N40	
	Hitachi	HD2501	
		HD7440	
	ITT	ITT7440	
	Mitsubishi	M53240	
	Motorola	MC7440	
	National	DM7440	
	NEC America	μPB7440	
	Signetics	7440	
	TRW	7440	
♦SN7441A	National	DM7441A	
	TI	SN74141	
SN7442	Fairchild	7442	
♦SN7442	Fairchild	7442	
		9352	
	Hitachi	HD2536	
		HD7442	
	ITT	ITT7442	
	Mitsubishi	M53242	
	Motorola	MC7442	
	National	DM7442	
	NEC America	μPB7442	
	Raytheon	7442	
	Signetics	7442	
	TI	SN7442A	
♦SN7443	Fairchild	7443	
		9353	
	Hitachi	HD2537	
		HD7443	
	ITT	ITT7443	
	Mitsubishi	M53243	
	Motorola	MC7443	
	Raytheon	7443	
	Signetics	7443	
	TI	SN7443A	
♦SN7444	Fairchild	7444	
		9354	
	Hitachi	HD2538	
		HD7444	
	ITT	ITT7444	
	Mitsubishi	M53244	
	Motorola	MC7444	
	Raytheon	7444	
	Signetics	7444	
	TI	SN7444A	
SN7445	Fairchild	7445	
		9345	
	Hitachi	HD2531	
	ITT	ITT7445	
	Mitsubishi	M53245	
	Motorola	MC7445	
	National	DM7445	
SN7445	NEC America	μPB7445	
	Raytheon	7445	
	Signetics	7445	
	TRW	7445	
♦SN7446	Fairchild	7446	
		9357	
	Hitachi	HD2553	
	ITT	ITT7446	
	Motorola	MC7446	
	National	DM7446	
	Signetics	7446	
	TI	SN7446A	
♦SN7447	Fairchild	7447	
	Hitachi	HD2532	
	ITT	ITT7447	
	Mitsubishi	M53247	
	Motorola	MC7447	
	National	DM7447	
	NEC America	μPB7447	
	Signetics	7447	
	TI	SN7447A	
SN7448	Fairchild	7448	
		9358	
	ITT	ITT7448	
	Mitsubishi	M53248	
	Motorola	MC7448	
	National	DM7448	
	Signetics	7448	
SN7449	Fairchild	7449	
		9359	
	Motorola	MC7449	
SN7450	Fairchild	7450	
		9N50	
	Hitachi	HD2506	
		HD7450	
	ITT	ITT7450	
	Mitsubishi	M53250	
	Motorola	MC7450	
	National	DM7450	
	NEC America	μPB7450	
	Signetics	7450	
	TRW	7450	
SN7451	Fairchild	7451	
		9N51	
	Hitachi	HD2505	
		HD7451	
	ITT	ITT7451	
	Motorola	MC7451	
	National	DM7451	
	NEC America	μPB7451	
	Signetics	7451	
	TRW	7451	
SN7453	Fairchild	7453	
		9N53	
	Hitachi	HD2512	
		HD7453	
	ITT	ITT7453	
	Mitsubishi	M53253	
	Motorola	MC7453	
	National	DM7453	
	NEC America	μPB7453	
	Signetics	7453	
	TRW	7453	
SN7454	Fairchild	7454	
		9N54	
	Hitachi	HD2514	
		HD7454	
	ITT	ITT7454	
	Motorola	MC7454	
	National	DM7454	
	NEC America	μPB7454	
	Signetics	7454	
	TRW	7454	
SN7460	Fairchild	7460	
		9N60	
	Hitachi	HD2502	
		HD7460	
	Mitsubishi	M53260	
	Motorola	MC7460	
	National	DM7460	
	NEC America	μPB7460	
	Signetics	7460	
	TRW	7460	
SN7470	Fairchild	7470	
		9N70	
	Hitachi	HD2539	
SN7470	ITT	ITT7470	
	Mitsubishi	M53270	
	Motorola	MC7470	
	National	DM7470	
	Signetics	7470	
SN7472	Fairchild	7472	
		9N72	
	Hitachi	HD2529	
		HD7472	
	ITT	ITT7472	
	Mitsubishi	M53272	
	Motorola	MC7472	
	National	DM7472	
	Signetics	7472	
	TRW	7472	
SN7473	Fairchild	7473	
		9N73	
	Hitachi	HD2515	
	ITT	ITT7473	
	Mitsubishi	M53273	
	Motorola	MC7473	
	National	DM7473	
	NEC America	μPB7473	
	Signetics	7473	
SN7474	Fairchild	7474	
		9N74	
	Hitachi	HD2510	
		HD7474	
	ITT	ITT7474	
	Mitsubishi	M53274	
	Motorola	MC7474	
	National	DM7474	
	NEC America	μPB7474	
	Raytheon	7474	
	Signetics	7474	
	TRW	7474	
SN7475	Fairchild	7475	
		9375	
	Hitachi	HD2517	
		HD7475	
	ITT	ITT7475	
	Mitsubishi	M53275	
	Motorola	MC7475	
	National	DM7475	
	Signetics	7475	
	TRW	7475	
SN7476	Fairchild	7476	
		9N76	
	Hitachi	HD2516	
	ITT	ITT7476	
	Mitsubishi	M53276	
	Motorola	MC7476	
	National	DM7476	
	NEC America	μPB7476	
	Signetics	7476	
	TRW	7476	
♦SN7477	Fairchild	7477	
		9377	
	Motorola	MC7477	
	Signetics	7477	
♦SN7480	Fairchild	7480	
		9380	
	ITT	ITT7480	
	Mitsubishi	M53280	
	Motorola	MC7480	
	NEC America	μPB7480	
	Signetics	7480	
		8268	
♦SN7481	Fairchild	93407	
	Hitachi	HM2501	
	Motorola	MC4004	
	TI	SN7481A	
	TRW	7481	
SN7482	Fairchild	7482	
		9382	
	Hitachi	HD2513	
	ITT	ITT7482	
	Motorola	MC7482	
	National	DM7482	
SN7483	Fairchild	7483	
♦SN7483	Fairchild	7483	
		9383	
	Hitachi	HD2535	
	ITT	ITT7483	
	Mitsubishi	M53283	
	Motorola	MC7483	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
♦SN7483	National	DM7483	
	Raytheon	7483	
	Signetics	7483	
	TI	SN7483A	
♦SN7484	Mitsubishi	M53284	
	TI	SN7484A	
SN7485	Fairchild	7485	
	Hitachi	HD7485	
	Mitsubishi	M53285	
	Motorola	MC7485	
	National	DM7485	
	NEC America	μPB7485	
	Signetics	7485	
	TRW	7485	
SN7486	Fairchild	7486	
		9N86	
	Hitachi	HD2526	
		HD7486	
	ITT	ITT7486	
	Mitsubishi	M53286	
	Motorola	MC7486	
	National	DM7486	
	NEC America	μPB7486	
	Raytheon	7486	
	Signetics	7486	
	TRW	7486	
♦SN7488	Intersil	IM5600	
	MMI	**6230**	**1252**
	Motorola	MCM4002	
	National	DM7488	
	TI	SN7488A	
SN7489	AMD	SN7489	
	Fairchild	7489	
	Hitachi	HM2502	
	Mitsubishi	M53289	
	National	**DM7489**	**1287**
	NEC Micro	μPB2089	
	Raytheon	7489	
	Signetics	N82S25	
	TRW	7489	
♦SN7490	Fairchild	7490	
		9390	
	Hitachi	HD2519	
		HD7490	
	ITT	ITT7490	
	Mitsubishi	M53290	
	Motorola	MCM4023	
		MC7490	
	National	DM7490	
	Signetics	7490	
	TI	SN7490A	
	TRW	7490	
♦SN7491	Fairchild	7491	
		9391	
	Hitachi	HD2524	
	ITT	ITT7491	
	Mitsubishi	M53291	
	Motorola	MC7491	
	National	DM7491	
	NEC America	μPB7491	
	Signetics	7491	
	TI	SN7491A	
♦SN7492	Fairchild	7492	
		9392	
	Hitachi	HD2521	
		HD7492	
	ITT	ITT7492	
	Mitsubishi	M53292	
	Motorola	MC7492	
	National	DM7492	
	Signetics	7492	
	TI	SN7492A	
	TRW	7492	
♦SN7493	Fairchild	7493	
		9393	
	Hitachi	HD2520	
		HD7493	
	ITT	ITT7493	
	Mitsubishi	M53293	
	Motorola	MC7493	
	National	DM7493	
	Signetics	7493	
	TI	SN7493A	
♦SN7493	TRW	7493	
SN7494	Fairchild	7494	
		9394	
	Hitachi	HD2533	
	Motorola	MC7494	
	Signetics	7494	
♦SN7495	Fairchild	7495	
		9395	
	Hitachi	HD2534	
	ITT	ITT7495	
	Mitsubishi	M53295	
	Motorola	MC7495	
	National	DM7495	
	Signetics	7495	
	TI	SN7495A	
SN7496	Fairchild	7496	
		9396	
	Hitachi	HD2546	
		HD7496	
	ITT	ITT7496	
	Mitsubishi	M53296	
	Motorola	MC7496	
	National	DM7496	
	Signetics	7496	
	TRW	7496	
SN7497	Fairchild	7497	
	Motorola	MC7497	
♦SN7510	Motorola	MC1410	
SN75107	AMD	SN75107	
	Fairchild	75107	
	ITT	ITT75107	
	Motorola	MC75107	
	National	**DS75107**	**504**
	Raytheon	RC75107A	
SN75108	AMD	SN74108	
	Fairchild	75108	
	ITT	ITT75108	
	Motorola	MC75108	
	National	**DS75108**	**504**
	Raytheon	RC75108A	
SN75109	AMD	SN75109	
	Fairchild	75109	
	ITT	ITT75109	
	Raytheon	RC75109	
SN75110	AMD	SN75110	
	Fairchild	75110	
	ITT	ITT75110	
	Motorola	MC75110	
	Raytheon	RC75110	
SN75112	Fairchild	75112	
SN75114	AMD	9614	
	Fairchild	9614	
SN75115	AMD	9615	
	Fairchild	9615	
SN75121	Fairchild	75121	
	Motorola	MC8T13	
	National	DS75121	
SN75122	Fairchild	75122	
	Motorola	MC8T14	
	National	DS75122	
SN75123	Fairchild	75123	
	Motorola	MC8T23	
	National	DS75123	
SN75124	Fairchild	75124	
	Motorola	MC8T24	
SN75125	National	DS75125	
SN75138	Silicon G	SG75138	
SN75140	Motorola	MC75140	
SN75150	Fairchild	75150	
	Raytheon	RC75150	
SN75152	Fairchild	9627	
SN75154	Fairchild	75154	
	National	DS75154	
	Raytheon	RC75154	
SN75180	National	DS8800	
SN75182	AMD	DM8820	
	National	DS8820	
	Signetics	DS8820	
SN75183	AMD	DM8830	
	National	DS8830	
	Signetics	DS8830	
SN75188	AMD	MC1488	
	ITT	ITT1488	
	Motorola	MC1488	
	National	DS1488	
	Signetics	MC1488	
SN75189	AMD	MC1489	
	ITT	ITT1489	
	Motorola	MC1489	
	National	DS1489	
	Signetics	MC1489	
SN75189A	Exar	XR1489A	
SN7520	AMD	SN7520	
		SN7521	
	ITT	ITT7520	
	Motorola	MC7520	
	National	DS7520	
	Signetics	7520	
	Silicon G	SG7520	
SN75207	AMD	SN75207	
	Fairchild	75207	
SN75208	AMD	SN75208	
	Fairchild	75208	
SN7521	Motorola	MC7521	
	National	DS7521	
	Signetics	7521	
	Silicon G	SG7521	
SN7522	ITT	ITT7522	
	National	DS7522	
	Signetics	7522	
	Silicon G	SG7522	
SN75224	Fairchild	75224	
SN75225	Fairchild	75225	
SN7523	National	DS7523	
	Signetics	7523	
	Silicon G	SG7523	
SN75232	Fairchild	75232	
SN75233	Fairchild	75233	
SN75234	AMD	SN75234	
	Fairchild	75234	
	ITT	ITT75234	
SN75235	AMD	SN75235	
	Fairchild	75235	
	Motorola	MC75235	
SN75236	ITT	ITT75236	
SN75238	AMD	SN75238	
	Fairchild	75238	
SN75239	AMD	SN75239	
	Fairchild	75239	
SN7524	AMD	SN7524	
		7525	
	Fairchild	7524	
	ITT	ITT7524	
	Motorola	MC7524	
	National	DS7524	
	Signetics	7524	
	Silicon G	SG7524	
♦SN7525	Fairchild	7525	
	Motorola	MC7525	
	National	DS7525	
	Signetics	7525	
	Silicon G	SG7525	
SN7528	Fairchild	7528	
	ITT	ITT7528	
	Motorola	MC7528	
	National	DS7528	
	Silicon G	SG7528	
♦SN7529	Fairchild	7529	
	Motorola	MC7529	
	National	DS7529	
	Silicon G	SG7529	
SN75324	**National**	**DS75324**	**522**
	Raytheon	RC75324	
SN75325	AMD	SN75325	
	Fairchild	75325	
	ITT	ITT75325	
	Motorola	MC75325	
	National	**DS75325**	**520**
	Raytheon	RC75325	
	Silicon G	SG75325	
SN75326	Fairchild	75326	
	ITT	ITT75326	
SN75327	Fairchild	75327	
	ITT	ITT75327	
♦SN7534	Fairchild	7534	
	ITT	ITT7534	
	National	DS7534	
	Silicon G	SG7534	
♦SN7535	Fairchild	7535	
	National	DS7535	
	Silicon G	SG7535	
SN75361	ITT	ITT75361	
SN75361	**National**	**DS75361**	**523**
SN75362	**National**	**DS75362**	**524**
SN75365	ITT	ITT75365	
	Motorola	MC75365	
	National	**DS75365**	**526**
SN75368	Motorola	MC75368	
SN75369	AMD	MH0026	
	Motorola	MMH0026	
	National	**DS0026**	**503**
♦SN7538	Fairchild	7538	
	National	DS7538	
	Silicon G	SG7538	
♦SN7539	Fairchild	7539	
	National	DS7539	
	Silicon G	SG7539	
SN75450	Fairchild	75450	
	Hitachi	HD2574	
	ITT	ITT75450	
	Motorola	MC75450	
	National	DS75450	
	Raytheon	RC75450	
	Signetics	75450	
	Silicon G	SG75450	
SN75451	Fairchild	75451	
	Hitachi	HD2575	
	ITT	ITT75451	
	Motorola	MC75451	
	National	DS75451	
	Raytheon	RC75451	
	Signetics	75451	
	Silicon G	SG75451	
SN75452	Fairchild	75452	
	Hitachi	HD2577	
	ITT	ITT75452	
	Motorola	MC75452	
	National	DS75452	
	Raytheon	RC75452	
	Signetics	75452	
	Silicon G	SG75452	
SN75453	Fairchild	75453	
	Hitachi	HD2578	
	ITT	ITT75453	
	Motorola	MC75453	
	National	DS75453	
	Raytheon	RC75453	
	Signetics	75453	
	Silicon G	SG75453	
SN75454	Fairchild	75454	
	Hitachi	HD2579	
	ITT	ITT75453	
	Motorola	MC75454	
	National	DS75454	
	Raytheon	RC75454	
	Signetics	75454	
	Silicon G	SG75454	
SN75460	Fairchild	75460	
	ITT	ITT75460	
	Motorola	MC75460	
	National	DS75460	
	Silicon G	SG75460	
SN75461	Fairchild	75461	
	ITT	ITT75461	
	Motorola	MC75461	
	National	DS75461	
	Silicon G	SG75461	
SN75462	Fairchild	75462	
	ITT	ITT75462	
	Motorola	MC75462	
	National	DS75462	
	Silicon G	SG75462	
SN75463	Fairchild	75463	
	ITT	ITT75463	
	Motorola	MC75463	
	National	DS75463	
	Silicon G	SG75463	
SN75464	Fairchild	75464	
	ITT	ITT75464	
	Motorola	MC75464	
	National	DS75464	
		SG75464	
SN75466	Motorola	MC1411	
	Signetics	NE5501	
SN75467	Motorola	MC1412	
	Signetics	NE5502	
SN75468	Motorola	MC1413	
	Signetics	NE5503	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN75469	Signetics	NE5504	
SN75470	Fairchild	75470	
SN75471	Fairchild	75471	
SN75472	Fairchild	75472	
SN75473	Fairchild	75473	
SN75474	Fairchild	75474	
SN75475	Motorola	MC1472	
SN75476	Sprague	UDN-5711	
SN75477	Sprague	UDN-5712	
SN75478	Sprague	UDN-5713	
SN75479	Sprague	UDN-5714	
SN75480	National	DS8880	
SN75491	Fairchild	75491	
	Motorola	MC75491	
	National	DS75491	
SN75492	Fairchild	75492	
	Motorola	MC75492	
	National	DS75492	
SN75493	National	DS75493	
SN75494	National	DS75494	
SN76001	SGS	TBA820	
SN76104	Fairchild	μA732	
SN76111	Fairchild	μA767	
SN76115	Motorola	MC1310	
	RCA	CA1310	
	Sprague	ULN-2210	
SN76116	Fairchild	μA758	
	RCA	CA758	
	Sprague	ULN-2244	
SN76131	Exar	XR4739	
	Fairchild	μA739	
	SGS	TBA231	
SN76149	Exar	XR4739	
	Fairchild	μA749	
SN76177	Sprague	ULN-2277	
SN76226	Sprague	ULN-2216	
SN76227	Plessey	SL1327	
	Sprague	ULN-2217	
SN76228	Sprague	ULN-2218	
SN76242	Fairchild	μA780	
	RCA	CA3070	
	Sprague	ULN-2124	
SN76243	Fairchild	μA781	
	Sprague	ULN-2127	
SN76246	Fairchild	μA746	
	RCA	CA3071	
	Sprague	ULN-2114	
SN76266	RCA	CA3066	
SN76267	Fairchild	μA3067	
	RCA	CA3067	
SN76298	Motorola	MC1398	
	Sprague	ULN-2298	
♦SN76502	TI	TL441	
SN76514	Motorola	MC1496	
SN76530	Motorola	MC1330	
SN76544	Plessey	SL76544	
SN76564	Fairchild	3064	
	Motorola	MC1364	
	RCA	CA3064	
	Sprague	ULN-2264	
SN76565	Motorola	MC1364	
SN76591	Fairchild	μA1391	
	Motorola	MC1391	
SN76594	Fairchild	μA1394	
	Motorola	MC1394	
SN76600	Motorola	MC1350	
SN76635	Fairchild	μA720	
	Sprague	ULN-2137	
SN76642	Motorola	MC1357	
	Sprague	ULN-2113	
SN76643	Fairchild	2136	
	Signetics	ULN2111	
	Sprague	ULN-2111	
SN76650	Motorola	MC1352	
	RCA	CA1352	
SN76651	Motorola	MC1351	
SN76665	Fairchild	μA3064	
	Motorola	MC1364	
	RCA	CA3065	
	Sprague	ULN-2165	
SN76666	Fairchild	μA3065	
	Motorola	MC1358	
	Sprague	ULN-2165	
SN76669	Fairchild	μA2136	
	Motorola	MC1356	
	Sprague	ULN-2136	
SN76675	Fairchild	μA3075	
	Motorola	MC1375	
SN76678	Fairchild	μA753	
	Sprague	ULN-2209	
SN76689	Fairchild	μA3089	
	Sprague	ULN-2289	
TL081	**PMI**	**OP-16**	**877**
TL089	**Harris**	**HA-2905**	**724**
TL430	Signetics	TL430	
TL514	Motorola	MC1514	
	Raytheon	RC1414	
		RM1514	
TL720	National	LM1414	
TMS0803	GI	C-593	
TMS0851	GI	CF-593	
TMS1101	Intersil	IM7501	
♦TMS1103	Signetics	1103	
TMS2101	NEC Micro	μPD2101A	
♦TMS2102	Intersil	IM7552	
	NEC Micro	μPD2102A	
♦TMS2300	AMI	S8773	
♦TMS2500	AMI	S8773	
♦TMS2600	AMI	S8773	
	National	MM4230	
		MM5230	
TMS2708	AMD	2708	
	EA	EA2708	
	Fujitsu	MB8518	
	Intel	2708	
	Mostek	MK2708	
	Motorola	MCM2708	
	National	MM2708	
♦TMS2800	National	MM4210	
♦TMS2900	AMI	S8773	
♦TMS3003	SGS	M127	
TMS3064	**Fairchild**	**F464**	**1083**
♦TMS3112	Fairchild	3348	
	Signetics	2518	
TMS3113	AMI	S2181A	
TMS3114	AMD	3114	
	AMI	S2181A	
TMS3120	Fairchild	3347	
	SGS	M142	
	Signetics	2532	
♦TMS3121	Fairchild	3342	
♦TMS3122	Signetics	2518	
TMS3128	Signetics	2521	
♦TMS3133	Fairchild	3355	
	Signetics	2533	
♦TMS3304	Motorola	MC1141	
TMS3409	Fairchild	3357	
	Intersil	IM7780	
	Mostek	MK1007	
	Plessey	MP3409	
	SGS	M142	
TMS3412	AMI	S1685	
	SGS	M141	
TMS3413	SGS	M136	
♦TMS3414	AMI	S1685	
	SGS	M130	
TMS3417	Fairchild	3342	
	Plessey	MP3417	
TMS4000	GI	RO5-8192	
TMS4027	**Fairchild**	**M4027**	**1118**
	Mostek	MK4027	
	Motorola	MCM4027	
	NEC Micro	**μPD414**	**1395**
TMS4030	Intel	2107A	
TMS4033	Fairchild	21021	
	Mostek	MK4102	
	National	**MM2102**	**1300**
	NEC Micro	μPD2102A	
		μPD2102AL	**1429**
	SGS	M330	
	Signetics	21F02	
		2102-2B	
TMS4034	Fairchild	21022	
	National	**MM2102**	**1300**
	NEC Micro	μPD2102A	
	Signetics	2102	
TMS4035	Fairchild	21022	
	National	MM2101	
	Signetics	2102	
TMS4039	NEC Micro	μPD2101A	
TMS4042	NEC Micro	μPD2111A	
		μPD2111AL	**1433**
	Signetics	2535	
		2602	
TMS4045	Intel	2114	
TMS4050	AMD	9050	
	NEC Micro	**μPD418**	**1412**
	Synertek	SY4050	
TMS4051	**NEC Micro**	**μPD418**	**1412**
TMS4060	AMD	9060	
	EA	EA4060	
	Intel	2107	
	Intersil	7280	
	National	**MM5280**	**1336**
	NEC Micro	**μPD411**	**1375**
	Signetics	2680	
TMS4062	Nortec	6002	
TMS4070	Zilog	Z6116	
TMS4116	**Fairchild**	**F16K**	**1110**
	Intel	2116	
	Intersil	7116	
	Mostek	MK4116	
	Motorola	MCM4116	
	NEC Micro	**μPD416**	**1402**
	Signetics	2690	
TMS4700	Mostek	MK30000	
TMS4732	**NEC Micro**	**μPD2332**	**1485**
	Signetics	2633	
TMS4800	EA	EA4800	
		EA4900	
	Mostek	MK28000	
TMS5001	GI	AY5-3600	
TMS54071	Mostek	MK4116	
TMS6010	AMI	S1757	
	GI	AY5-1013A	
TMS6011	**AMI**	**S1883**	**354,1587**
	GI	AY3-1014A	
		AY3-1015	
	SMC	COM2017	
	Western	TR1602	
TMS7001	Intersil	7001	
TMS8080A	AMD	9080A	
	Intel	8080A	
	National	**INS8080A**	
			1656,1670
	NEC Micro	**μPD8080AF**	**1736**
	Signetics	MP8080A	
TMS9900	**AMI**	**S9900**	**1575**
TMS9901	**AMI**	**S9901**	**1577**
TMS9902	**AMI**	**S9902**	**1579**
TMS9903	**AMI**	**S9903**	**1581**
TMS9940	**AMI**	**S9940**	**1583**
TMS9980	**AMI**	**S9980**	**1585**
TPO237	AMI	2733	
TP4000	Mitel	SIL4000	
	Motorola	MC14000	
	National	CD4000	
	RCA	CD4000	
	Solitron	CM4000	
	SSS	SCL4000	
TP4001	Fairchild	F4001	
	Mitel	SIL4001	
	Motorola	MC14001	
	National	CD4001	
	NEC America	μPD4001	
	RCA	CD4001	
	Solitron	CM4001	
	SSS	SCL4001	
	Toshiba	TC4001	
TP4002	Fairchild	F4002	
	Mitel	SIL4002	
	Motorola	MC14002	
	National	CD4002	
	NEC America	μPD4002	
	RCA	CD4002	
	SGS	HBF4002	
	Solitron	CM4002	
	SSS	SCL4002	
	Toshiba	TC4002	
TP4007	Fairchild	F4007	
	Mitel	SIL4007	
	Motorola	MC14007	
	National	CD4007	
	RCA	CD4007	
	SGS	HBF4007	
TP4007	Solitron	CM4007	
	SSS	SCL4007	
	Toshiba	TC4007	
TP4008	Fairchild	F4008	
	Motorola	MC14008	
	National	CD4008	
	RCA	CD4008	
	SGS	HBF4008	
	Solitron	CM4008	
	SSS	SCL4008	
	Toshiba	TC4008	
TP4009	Mitel	SIL4009	
	National	CD4009	
	RCA	CD4009	
	SGS	HBF4009	
	Solitron	CM4009	
	SSS	SCL4009	
	Toshiba	TC4009	
TP4010	Mitel	SIL4010	
	National	CD4010	
	RCA	CD4010	
	SGS	HBF4010	
	Solitron	CM4010	
	SSS	SCL4010	
	Toshiba	TC4010	
TP4011	Fairchild	F4011	
	Mitel	SIL4011	
	Motorola	MC14011	
	National	CD4011	
	NEC America	μPD4011	
	RCA	CD4011	
	SGS	HBF4011	
	Solitron	CM4011	
	SSS	SCL4011	
	Toshiba	TC4011	
TP4012	Fairchild	F4012	
	Mitel	SIL4012	
	Motorola	MC14012	
	National	CD4012	
	NEC America	μPD4012	
	RCA	CD4012	
	SGS	HBF4012	
	Solitron	CM4012	
	SSS	SCL4012	
	Toshiba	TC4012	
TP4013	Fairchild	F4013	
	Mitel	SIL4013	
	Motorola	MC14013	
	National	CD4013	
	NEC America	μPD4013	
	RCA	CD4013	
	SGS	HBF4013	
	Solitron	CM4013	
	SSS	SCL4013	
	Toshiba	TC4013	
TP4014	Fairchild	F4014	
	Mitel	SIL4014	
	Motorola	MC14014	
	National	CD4014	
	NEC America	μPD4014	
	RCA	CD4014	
	SGS	HBF4014	
	Solitron	CM4014	
	SSS	SCL4014	
	Toshiba	TC4014	
TP4015	Fairchild	F4015	
	Mitel	SIL4015	
	Motorola	MC14015	
	National	CD4015	
	NEC America	μPD4015	
	RCA	CD4015	
	SGS	HBF4015	
	Solitron	CM4015	
	SSS	SCL4015	
	Toshiba	TC4015	
TP4016	AD	AD7516	
	Fairchild	F4016	
	Micro Power	MPS7516	
	Mitel	SIL4016	
	Motorola	MC14016	
	National	CD4016	
	RCA	CD4016	
		CD4066	
	Solitron	CM4016	
	SSS	SCL4016	
TP4017	Fairchild	F4017	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Texas Instruments (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
TP4017	Mitel	SIL4017	
	Motorola	MC14017	
	National	CD4017	
	NEC America	μPD4017	
	RCA	CD4017	
	SGS	HBF4017	
	Solitron	CM4017	
	SSS	SCL4017	
	Toshiba	TC4017	
TP4018	Fairchild	F4018	
	Mitel	SIL4018	
	National	CD4018	
	RCA	CD4018	
	SGS	HBF4018	
	Solitron	CM4018	
	SSS	SCL4018	
	Toshiba	TC4018	
TP4019	Fairchild	F4019	
	Mitel	SIL4019	
	National	CD4019	
	RCA	CD4019	
	SGS	HBF4019	
	Solitron	CM4019	
	SSS	SCL4019	
	Toshiba	TC4019	
TP4020	Fairchild	F4020	
	Mitel	SIL4020	
	Motorola	MC14020	
	National	CD4020	
	NEC America	μPD4020	
	RCA	CD4020	
	SGS	HBF4020	
	Solitron	CM4020	
	SSS	SCL4020	
	Toshiba	TC4020	
TP4021	Fairchild	F4021	
	Mitel	SIL4021	
	Motorola	MC14021	
	National	CD4021	
	NEC America	μPD4021	
	RCA	CD4021	
	Solitron	CM4021	
	SSS	SCL4021	
	Toshiba	TC4021	
TP4022	Fairchild	F4022	
	Mitel	SIL4022	
	Motorola	MC14022	
	National	CD4022	
	RCA	CD4022	
	SGS	HBF4022	
	Solitron	CM4022	
	SSS	SCL4022	
	Toshiba	TC4022	
TP4023	Fairchild	F4023	
	Mitel	SIL4023	
	Motorola	MC14023	
	National	CD4023	
	NEC America	μPD4023	
	RCA	CD4023	
	SGS	HBF4023	
	Solitron	CM4023	
	SSS	SCL4023	
	Toshiba	TC4023	
TP4024	Fairchild	F4024	
	Mitel	SIL4024	
	Motorola	MC14024	
	National	CD4024	
	RCA	CD4024	
	SGS	HBF4024	
	Solitron	CM4024	
	SSS	SCL4024	
	Toshiba	TC4024	
TP4025	Fairchild	F4025	
	Mitel	SIL4025	
	Motorola	MC14025	
	National	CD4025	
	NEC America	μPD4025	
	RCA	CD4025	
	SGS	HBF4025	
	Solitron	CM4025	
	SSS	SCL4025	
	Toshiba	TC4025	
TP4027	Fairchild	F4027	
TP4027	Mitel	SIL4027	
	Motorola	MC14027	
	National	CD4027	
	NEC America	μPD4027	
	RCA	CD4027	
	SGS	HBF4027	
	Solitron	CM4027	
	SSS	SCL4027	
	Toshiba	TC4027	
TP4028	Fairchild	F4028	
	Mitel	SIL4028	
	Motorola	MC14028	
	National	CD4028	
	NEC America	μPD4028	
	RCA	CD4028	
	SGS	HBF4028	
	Solitron	CM4028	
	SSS	SCL4028	
	Toshiba	TC4028	
TP4029	Fairchild	F4029	
	Mitel	SIL4029	
	National	CD4029	
	NEC America	μPD4029	
	RCA	CD4029	
	SGS	HBF4029	
	Solitron	CM4029	
	SSS	SCL4029	
	Toshiba	TC4029	
TP4030	Fairchild	F4030	
	Mitel	SIL4030	
	National	CD4030	
	NEC America	μPD4030	
	RCA	CD4030	
	SGS	HBF4030	
	Solitron	CM4030	
	SSS	SCL4030	
	Toshiba	TC4030	
TP4035	Fairchild	F4035	
	Mitel	SIL4035	
	Motorola	MC14035	
	National	CD4035	
	NEC America	μPD4035	
	RCA	CD4035	
	SGS	HBF4035	
	Solitron	CM4035	
	SSS	SCL4035	
	Toshiba	TC4035	
TP4040	Fairchild	F4040	
	Mitel	SIL4040	
	National	CD4040	
	NEC America	μPD4040	
	RCA	CD4040	
	Solitron	CM4040	
	SSS	SCL4040	
	Toshiba	TC4040	
TP4042	Fairchild	F4042	
	Mitel	SIL4042	
	Motorola	MC14042	
	National	CD4042	
	NEC America	μPD4042	
	RCA	CD4042	
	SGS	HBF4042	
	Solitron	CM4042	
	SSS	SCL4042	
	Toshiba	TC4042	
TP4043	Fairchild	F4043	
	Mitel	SIL4043	
	Motorola	MC14043	
	National	CD4043	
	NEC America	μPD4043	
	RCA	CD4043	
	Solitron	CM4043	
	SSS	SCL4043	
	Toshiba	TC4043	
TP4044	Fairchild	F4044	
	Mitel	SIL4044	
	Motorola	MC14044	
	National	CD4044	
	NEC America	μPD4044	
	RCA	CD4044	
	Solitron	CM4044	
	SSS	SCL4044	
	Toshiba	TC4044	
♦TP4047	Fairchild	F4047	
	Motorola	MC14047	
	RCA	CD4047	
♦TP4047	Solitron	CM4047	
	Toshiba	TC4047	
TP4049	Fairchild	F4049	
	Mitel	SIL4049	
	Motorola	MC14049	
	National	CD4049	
	NEC America	μPD4049	
	RCA	CD4049	
	SGS	HBF4049	
	Solitron	CM4049	
	SSS	SCL4049	
	Toshiba	TC4049	
TP4050	Fairchild	F4050	
	Mitel	SIL4050	
	Motorola	MC14050	
	National	CD4050	
	NEC America	μPD4050	
	RCA	CD4050	
	SGS	HBF4050	
	Solitron	CM4050	
	SSS	SCL4050	
	Toshiba	TC4050	
TP4051	Fairchild	F4051	
	GI	MEM4051	
	Mitel	SIL4051	
	Motorola	MC14051	
	National	CD4051	
	RCA	CD4051	
	Solitron	CM4051	
	SSS	SCL4051	
	Toshiba	TC4051	
TP4052	Fairchild	F4052	
	Mitel	SIL4052	
	Motorola	MC14052	
	National	CD4052	
	RCA	CD4052	
	Solitron	CM4052	
	SSS	SCL4052	
	Toshiba	TC4052	
TP4053	RCA	CD4053	
TP4068	Fairchild	F4068	
	Mitel	SIL4068	
	Motorola	MC14068	
	RCA	CD4068	
	Solitron	CM4068	
	SSS	SCL4068	
	Toshiba	TC4068	
TP4069	Fairchild	F4069	
	Harris	HD74C04	
	Mitel	SIL4069	
	Motorola	MC14069	
	National	CD4069	
		MM74C04	
	NEC America	μPD4069	
	RCA	CD4069	
	Solitron	CM4069	
	SSS	SCL4069	
	Toshiba	TC4069	
♦TP4070	Fairchild	F4070	
	Mitel	SIL4070	
	National	CD4070	
		MM74C86	
	RCA	CD4070	
	Solitron	CM4070	
	SSS	SCL4070	
TP4071	Fairchild	F4071	
	Mitel	SIL4071	
	Motorola	MC14071	
	National	CD4071	
	NEC America	μPD4071	
	RCA	CD4071	
	Solitron	CM4071	
	SSS	SCL4071	
	Toshiba	TC4071	
TP4072	Fairchild	F4072	
	Mitel	SIL4072	
	Motorola	MC14072	
	RCA	CD4072	
	SSS	SCL4072	
	Toshiba	TC4072	
TP4073	Fairchild	F4073	
	Mitel	SIL4073	
	Motorola	MC14073	
	National	CD4073	
	RCA	CD4073	
	Solitron	CM4073	
TP4073	SSS	SCL4073	
	Toshiba	TC4073	
TP4075	Fairchild	F4075	
	Mitel	SIL4075	
	Motorola	MC14075	
	National	CD4075	
	RCA	CD4075	
	SSS	SCL4075	
	Toshiba	TC4075	
♦TP4076	Fairchild	F4076	
	Harris	HD74C173	
	Mitel	SIL4076	
	Motorola	MC14076	
	National	CD4076	
		MM74C173	
	RCA	CD4076	
	Solitron	CM4076	
	SSS	SCL4076	
TP4078	Motorola	MC14078	
	RCA	CD4078	
TP4081	Fairchild	F4081	
	Mitel	SIL4081	
	Motorola	MC14081	
	National	CD4081	
	NEC America	μPD4081	
	RCA	CD4081	
	Solitron	CM4081	
	SSS	SCL4081	
	Toshiba	TC4081	
TP4082	Fairchild	F4082	
	Mitel	SIL4082	
	Motorola	MC14082	
	RCA	CD4082	
	SSS	SCL4082	
	Toshiba	TC4082	
♦TP4085	Fairchild	F4085	
	RCA	CD4085	
♦TP4093	Fairchild	F4093	
	Motorola	MC14093	
	National	CD4093	
	RCA	CD4093	
♦TP4099	Fairchild	F4099	
	National	CD4099	
	RCA	CD4099	
TP4315	RCA	CD4069	
TP4320	RCA	CD4067	
TP4360	Fairchild	F40160	
	Motorola	MC14160	
	National	MM74C160	
TP4361	Fairchild	F40161	
	Motorola	MC14161	
	National	MM74C161	
TP4362	Fairchild	F40162	
	Motorola	MC14162	
	National	MM74C162	
TP4363	Fairchild	F40163	
	Motorola	MC14163	
	National	MM74C163	
TP4507	Motorola	MC14507	
	National	CD4070	
		CD4507	
		MM74C86	
	RCA	CD4030	
		CD4070	
	SSS	SCL4030	
TP4511	Fairchild	F4511	
	Mitel	SIL4511	
	Motorola	MC14511	
	National	CD4511	
	RCA	CD4511	
	Solitron	CM4511	
	SSS	SCL4511	
TP4512	Fairchild	F4512	
	Mitel	SIL4512	
	Motorola	MC14512	
	National	CD4512	
	NEC America	μPD4512	
	SSS	SCL4512	
	Toshiba	TC4512	
♦TP4516	Fairchild	F4516	
	Mitel	SIL4516	
	Motorola	MC14516	
	National	CD4516	
	RCA	CD40193	
		CD4516	
	SSS	SCL4516	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Texas Instruments (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
♦TP4516	Toshiba	TC4516	
TP4518	Fairchild	F4518	
	Mitel	SIL4518	
	Motorola	MC14518	
	National	CD4518	
	RCA	CD4518	
	Solitron	CM4518	
	SSS	SCL4518	
	Toshiba	TC4518	
TP4519	Fairchild	F4519	
	Motorola	MC14519	
	National	CD4519	
	NEC America	μPD4519	
	RCA	CD4019	
TP4520	Fairchild	F4520	
	Mitel	SIL4520	
	Motorola	MC14520	
	National	CD4520	
	NEC America	μPD4520	
	RCA	CD4520	
	Solitron	CM4520	
	SSS	SCL4520	
	Toshiba	TC4520	
TP4522	Fairchild	F4522	
	Motorola	MC14522	
	National	CD4522	
	RCA	CD4018	
	SSS	SCL4522	
TP4526	Fairchild	F4526	
	Motorola	MC14526	
	SSS	SCL4526	
TP4531	Fairchild	F4531	
	Motorola	MC14531	
	RCA	CD40101	
	SSS	SCL4531	
TP4581	Motorola	MC14581	
	RCA	CD40181	
	SSS	SCL4581	
TP4582	Fairchild	F4582	
	Motorola	MC14582	
	RCA	CD40182	
	SSS	SCL4582	
ULN2001	Exar	XR2201	
	Fairchild	9665	
	SGS	L201	
	Signetics	ULN2001	
	Silicon G	SG2001	
	Sprague	ULN-2001	
ULN2002	Exar	XR2202	
	Fairchild	9666	
	SGS	L202	
	Signetics	ULN2002	
	Silicon G	SG2002	
	Sprague	ULN-2002	
ULN2003	Exar	XR2203	
	Fairchild	9667	
	SGS	L203	
	Signetics	ULN2003	
	Silicon G	SG2003	
	Sprague	ULN-2003	
ULN2004	Exar	XR2204	
	Fairchild	9668	
	Signetics	ULN2004	
	Silicon G	SG2004	
	Sprague	ULN-2004	

Toshiba

Manufacturer Device	Replacement Source	Device	IC Master Page
TA7613	Sprague	ULN-2204	
TC4001	Fairchild	F4001	
	Mitel	SIL4001	
	Motorola	MC14001	
	National	CD4001	
	NEC America	μPD4001	
	RCA	CD4001	
	SGS	HBF4001	
	Solitron	CM4001	
	SSS	SCL4001	
	TI	TP4001	
TC4002	Fairchild	F4002	
	Mitel	SIL4002	
	Motorola	MC14002	
TC4002	National	CD4002	
	NEC America	μPD4002	
	RCA	CD4002	
	SGS	HBF4002	
	Solitron	CM4002	
	SSS	SCL4002	
	TI	TP4002	
TC4007	Fairchild	F4007	
	Mitel	SIL4007	
	Motorola	MC14007	
	National	CD4007	
	RCA	CD4007	
	SGS	HBF4007	
	Solitron	CM4007	
	SSS	SCL4007	
	TI	TP4007	
TC4008	Fairchild	F4008	
	Motorola	MC14008	
	National	CD4008	
	RCA	CD4008	
	SGS	HBF4008	
	Solitron	CM4008	
	SSS	SCL4008	
	TI	TP4008	
TC4009	Mitel	SIL4009	
	National	CD4009	
	RCA	CD4009	
	SGS	HBF4009	
	Solitron	CM4009	
	SSS	SCL4009	
	TI	TP4009	
TC4010	Mitel	SIL4010	
	National	CD4010	
	RCA	CD4010	
	SGS	HBF4010	
	Solitron	CM4010	
	SSS	SCL4010	
	TI	TP4010	
TC4011	Fairchild	F4011	
	Mitel	SIL4011	
	Motorola	MC14011	
	National	CD4011	
	NEC America	μPD4011	
	RCA	CD4011	
	SGS	HBF4011	
	Solitron	CM4011	
	SSS	SCL4011	
	TI	TP4011	
TC4012	Fairchild	F4012	
	Mitel	SIL4012	
	Motorola	MC14012	
	National	CD4012	
	NEC America	μPD4012	
	RCA	CD4012	
	SGS	HBF4012	
	Solitron	CM4012	
	SSS	SCL4012	
	TI	TP4012	
TC4013	Fairchild	F4013	
	Mitel	SIL4013	
	Motorola	MC14013	
	National	CD4013	
	NEC America	μPD4013	
	RCA	CD4013	
	SGS	HBF4013	
	Solitron	CM4013	
	SSS	SCL4013	
	TI	TP4013	
TC4014	Fairchild	F4014	
	Mitel	SIL4014	
	Motorola	MC14014	
	National	CD4014	
	NEC America	μPD4014	
	RCA	CD4014	
	SGS	HBF4014	
	Solitron	CM4014	
	SSS	SCL4014	
	TI	TP4014	
TC4015	Fairchild	F4015	
	Mitel	SIL4015	
	Motorola	MC14015	
	National	CD4015	
	NEC America	μPD4015	
	RCA	CD4015	
	SGS	HBF4015	
	Solitron	CM4015	
TC4015	SSS	SCL4015	
	TI	TP4015	
TC4017	Fairchild	F4017	
	Mitel	SIL4017	
	Motorola	MC14017	
	National	CD4017	
	NEC America	μPD4017	
	RCA	CD4017	
	SGS	HBF4017	
	Solitron	CM4017	
	SSS	SCL4017	
	TI	TP4017	
TC4018	Fairchild	F4018	
	Mitel	SIL4018	
	National	CD4018	
	RCA	CD4018	
	SGS	HBF4018	
	Solitron	CM4018	
	SSS	SCL4018	
	TI	TP4018	
TC4019	Fairchild	F4019	
	Mitel	SIL4019	
	National	CD4019	
	RCA	CD4019	
	SGS	HBF4019	
	Solitron	CM4019	
	SSS	SCL4019	
	TI	TP4019	
TC4020	Fairchild	F4020	
	Mitel	SIL4020	
	Motorola	MC14020	
	National	CD4020	
	NEC America	μPD4020	
	RCA	CD4020	
	SGS	HBF4020	
	Solitron	CM4020	
	SSS	SCL4020	
	TI	TP4020	
TC4021	Fairchild	F4021	
	Mitel	SIL4021	
	Motorola	MC14021	
	National	CD4021	
	NEC America	μPD4021	
	RCA	CD4021	
	Solitron	CM4021	
	SSS	SCL4021	
	TI	TP4021	
TC4022	Fairchild	F4022	
	Mitel	SIL4022	
	Motorola	MC14022	
	National	CD4022	
	RCA	CD4022	
	SGS	HBF4022	
	Solitron	CM4022	
	SSS	SCL4022	
	TI	TP4022	
TC4023	Fairchild	F4023	
	Mitel	SIL4023	
	Motorola	MC14023	
	National	CD4023	
	NEC America	μPD4023	
	RCA	CD4023	
	SGS	HBF4023	
	Solitron	CM4023	
	SSS	SCL4023	
	TI	TP4023	
TC4024	Fairchild	F4024	
	Mitel	SIL4024	
	Motorola	MC14024	
	National	CD4024	
	RCA	CD4024	
	SGS	HBF4024	
	Solitron	CM4024	
	SSS	SCL4024	
	TI	TP4024	
TC4025	Fairchild	F4025	
	Mitel	SIL4025	
	Motorola	MC14025	
	National	CD4025	
	NEC America	μPD4025	
	RCA	CD4025	
	SGS	HBF4025	
	Solitron	CM4025	
	SSS	SCL4025	
	TI	TP4025	
TC4027	Fairchild	F4027	
TC4027	Mitel	SIL4027	
	Motorola	MC14027	
	National	CD4027	
	NEC America	μPD4027	
	RCA	CD4027	
	SGS	HBF4027	
	Solitron	CM4027	
	SSS	SCL4027	
	TI	TP4027	
TC4028	Fairchild	F4028	
	Mitel	SIL4028	
	Motorola	MC14028	
	National	CD4028	
	NEC America	μPD4028	
	RCA	CD4028	
	SGS	HBF4028	
	Solitron	CM4028	
	SSS	SCL4028	
	TI	TP4028	
TC4029	Fairchild	F4029	
	Mitel	SIL4029	
	National	CD4029	
	NEC America	μPD4029	
	RCA	CD4029	
	SGS	HBF4029	
	Solitron	CM4029	
	SSS	SCL4029	
	TI	TP4029	
TC4030	Fairchild	F4030	
	Mitel	SIL4030	
	National	CD4030	
	NEC America	μPD4030	
	RCA	CD4030	
	SGS	HBF4030	
	Solitron	CM4030	
	SSS	SCL4030	
	TI	TP4030	
TC4032	Motorola	MC14032	
	RCA	CD4032	
	Solitron	CM4032	
TC4034	Fairchild	F4034	
	Motorola	MC14034	
	National	CD4034	
	RCA	CD4034	
	Solitron	CM4034	
	SSS	SCL4034	
TC4035	Fairchild	F4035	
	Mitel	SIL4035	
	Motorola	MC14035	
	National	CD4035	
	NEC America	μPD4035	
	RCA	CD4035	
	SGS	HBF4035	
	Solitron	CM4035	
	SSS	SCL4035	
	TI	TP4035	
TC4038	Motorola	MC14308	
	RCA	CD4038	
	Solitron	CM4038	
TC4040	Fairchild	F4040	
	Mitel	SIL4040	
	National	CD4040	
	NEC America	μPD4040	
	RCA	CD4040	
	Solitron	CM4040	
	SSS	SCL4040	
	TI	TP4040	
TC4042	Fairchild	F4042	
	Mitel	SIL4042	
	Motorola	MC14042	
	National	CD4042	
	NEC America	μPD4042	
	RCA	CD4042	
	SGS	HBF4042	
	Solitron	CM4042	
	SSS	SCL4042	
	TI	TP4042	
TC4043	Fairchild	F4043	
	Mitel	SIL4043	
	Motorola	MC14043	
	National	CD4043	
	NEC America	μPD4043	
	RCA	CD4043	
	Solitron	CM4043	
	SSS	SCL4043	
	TI	TP4043	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Toshiba (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
TC4044	Fairchild	F4044	
	Mitel	SIL4044	
	Motorola	MC14044	
	National	CD4044	
	NEC America	µPD4044	
	RCA	CD4044	
	Solitron	CM4044	
	SSS	SCL4044	
	TI	TP4044	
TC4047	Fairchild	F4047	
	RCA	CD4047	
	Solitron	CM4047	
TC4049	Fairchild	F4049	
	Mitel	SIL4049	
	Motorola	MC14049	
	National	CD4049	
	NEC America	µPD4049	
	RCA	CD4049	
	SGS	HBF4049	
	Solitron	CM4049	
	SSS	SCL4049	
	TI	TP4049	
TC4050	Fairchild	F4050	
	Mitel	SIL4050	
	Motorola	MC14050	
	National	CD4050	
	NEC America	µPD4050	
	RCA	CD4050	
	SGS	HBF4050	
	Solitron	CM4050	
	SSS	SCL4050	
	TI	TP4050	
TC4051	Fairchild	F4051	
	Mitel	SIL4051	
	Motorola	MC14051	
	National	CD4051	
	RCA	CD4051	
	Solitron	CM4051	
	SSS	SCL4051	
	TI	TP4051	
TC4052	Fairchild	F4052	
	Mitel	SIL4052	
	Motorola	MC14052	
	National	CD4052	
	RCA	CD4052	
	Solitron	CM4052	
	SSS	SCL4052	
	TI	TP4052	
TC4053	Fairchild	F4053	
	GI	MEM4053	
	Mitel	SIL4053	
	Motorola	MC14053	
	National	CD4053	
	RCA	CD4053	
	Solitron	CM4053	
	SSS	SCL4053	
TC4061	RCA	CD4061	
TC4066	Fairchild	F4066	
	Mitel	SIL4066	
	Motorola	MC14066	
	National	CD4066	
	NEC America	µPD4066	
	RCA	CD4063	
		CD4066	
	SGS	HBF4066	
	Signetics	N4066	
	Solitron	CM4066	
	SSS	SCL4066	
TC4068	Fairchild	F4068	
	Mitel	SIL4068	
	Motorola	MC14068	
	RCA	CD4068	
	Solitron	CM4068	
	SSS	SCL4068	
	TI	TP4068	
TC4069	Fairchild	F4069	
	Harris	HD74C04	
	Mitel	SIL4069	
	Motorola	MC14069	
	National	CD4069	
		MM74C04	
	NEC America	µPD4069	
	RCA	CD4069	
TC4069	Solitron	CM4069	
	SSS	SCL4069	
	TI	TP4069	
TC4071	Fairchild	F4071	
	Mitel	SIL4071	
	Motorola	MC14071	
	National	CD4071	
	NEC America	µPD4071	
	RCA	CD4071	
	Solitron	CM4071	
	SSS	SCL4071	
	TI	TP4071	
TC4072	Fairchild	F4072	
	Mitel	SIL4072	
	Motorola	MC14072	
	RCA	CD4072	
	SSS	SCL4072	
	TI	TP4072	
TC4073	Fairchild	F4073	
	Mitel	SIL4073	
	Motorola	MC14073	
	National	CD4073	
	RCA	CD4073	
	Solitron	CM4073	
	SSS	SCL4073	
	TI	TP4073	
TC4075	Fairchild	F4075	
	Mitel	SIL4075	
	Motorola	MC14075	
	National	CD4075	
	RCA	CD4075	
	SSS	SCL4075	
	TI	TP4075	
TC4078	Fairchild	F4078	
	Mitel	SIL4078	
	Motorola	MC14078	
	RCA	CD4078	
	Solitron	CM4078	
	SSS	SCL4078	
TC4081	Fairchild	F4081	
	Mitel	SIL4081	
	Motorola	MC14081	
	National	CD4081	
	NEC America	µPD4081	
	RCA	CD4081	
	Solitron	CM4081	
	SSS	SCL4081	
	TI	TP4081	
TC4082	Fairchild	F4082	
	Mitel	SIL4082	
	Motorola	MC14082	
	RCA	CD4082	
	SSS	SCL4082	
	TI	TP4082	
TC4508	Mitel	SIL4508	
	Motorola	MC14508	
	RCA	CD4508	
	SSS	SCL4508	
TC4510	Fairchild	F4510	
	Mitel	SIL4510	
	Motorola	MC14510	
	National	CD4510	
	RCA	CD40192	
		CD4510	
	SSS	SCL4510	
TC4512	Fairchild	F4512	
	Mitel	SIL4512	
	Motorola	MC14512	
	National	CD4512	
	NEC America	µPD4512	
	SSS	SCL4512	
	TI	TP4512	
TC4514	Fairchild	F4514	
	Mitel	SIL4514	
	Motorola	MC14514	
	National	CD4514	
	RCA	CD4514	
	Solitron	CM4514	
	SSS	SCL4514	
TC4515	Fairchild	F4515	
	Mitel	SIL4515	
	Motorola	MC14515	
	National	CD4515	
	RCA	CD4515	
	Solitron	CM4515	
	SSS	SCL4515	
TC4516	Fairchild	F4516	
	Mitel	SIL4516	
	Motorola	MC14516	
	National	CD4516	
	RCA	CD40193	
		CD4516	
	SSS	SCL4516	
TC4518	Fairchild	F4518	
	Mitel	SIL4518	
	Motorola	MC14518	
	National	CD4518	
	RCA	CD4518	
	Solitron	CM4518	
	SSS	SCL4518	
	TI	TP4518	
TC4520	Fairchild	F4520	
	Mitel	SIL4520	
	Motorola	MC14520	
	National	CD4520	
	NEC America	µPD4520	
	RCA	CD4520	
	Solitron	CM4520	
	SSS	SCL4520	
	TI	TP4520	
TC4528	Fairchild	F4528	
	Motorola	MC14528	
	NEC America	µPD4528	
	RCA	CD4528	
	SSS	SCL4528	
TC4532	Fairchild	F4532	
	Motorola	MC14532	
	RCA	CD4532	
TC4539	Fairchild	F4539	
	Motorola	MC14539	
	NEC America	µPD4539	
TC4583	Fairchild	F4583	
	Motorola	MC14583	
	RCA	CD40100	
TC4585	Motorola	MC14585	
	National	MM74C85	
	RCA	CD4063	
	SSS	SCL4585	
TC7400	Fairchild	7400	
	Hitachi	HD7400	
	ITT	ITT7400	
	Mitsubishi	M53200	
	Motorola	MC7400	
	National	DM7400	
	NEC America	µPB7400	
	Raytheon	7400	
	Signetics	7400	
	TI	SN7400	
	TRW	7400	
TC7404	Fairchild	7404	
	Hitachi	HD7404	
	ITT	ITT7404	
	Mitsubishi	M53204	
	Motorola	MC7404	
	National	DM7404	
	NEC America	µPB7404	
	Raytheon	7404	
	Signetics	7404	
	TI	SN7404	
	TRW	7404	
TC7408	Fairchild	7408	
	ITT	ITT7408	
	Mitsubishi	M53208	
	Motorola	MC7408	
	National	DM7408	
	Raytheon	7408	
	Signetics	7408	
	TI	SN7408	
	TRW	7408	
TC7410	Fairchild	7410	
	Hitachi	HD7410	
	ITT	ITT7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
	National	DM7410	
	NEC America	µPB7410	
	Raytheon	7410	
	Signetics	7410	
	TI	SN7410	
		SN7427	
	TRW	7410	
TC7420	Fairchild	7420	
TC7420	Hitachi	HD7420	
	ITT	ITT7420	
	Mitsubishi	M53220	
	Motorola	MC7420	
	National	DM7420	
	NEC America	µPB7420	
	Raytheon	7420	
	Signetics	7420	
	TI	SN7420	
	TRW	7420	

TRW

Manufacturer Device	Replacement Source	Device	IC Master Page
7400	Fairchild	7400	
	Hitachi	HD7400	
	ITT	ITT7400	
	Mitsubishi	M53200	
	Motorola	MC7400	
	National	DM7400	
	NEC America	µPB7400	
	Raytheon	7400	
	Signetics	7400	
	TI	SN7400	
	Toshiba	TC7400	
7401	Fairchild	7401	
	ITT	ITT7401	
	Mitsubishi	M53201	
	Motorola	MC7401	
	National	DM7401	
	Raytheon	7401	
	Signetics	7401	
	TI	SN7401	
7402	Fairchild	7402	
	Hitachi	HD7402	
	ITT	ITT7402	
	Mitsubishi	M53202	
	Motorola	MC7402	
	National	DM7402	
	NEC America	µPB7402	
	Signetics	7402	
	TI	SN7402	
7403	Fairchild	7403	
	Hitachi	HD7403	
	ITT	ITT7403	
	Mitsubishi	M53203	
	Motorola	MC7403	
	National	DM7403	
	Raytheon	7403	
	Signetics	7403	
	TI	SN7403	
7404	Fairchild	7404	
	Hitachi	HD7404	
	ITT	ITT7404	
	Mitsubishi	M53204	
	Motorola	MC7404	
	National	DM7404	
	NEC America	µPB7404	
	Raytheon	7404	
	Signetics	7404	
	TI	SN7404	
	Toshiba	TC7404	
7405	Fairchild	7405	
	Hitachi	HD7405	
	ITT	ITT7405	
	Mitsubishi	M53205	
	Motorola	MC7405	
	National	DM7405	
	NEC America	µPB7405	
	Raytheon	7405	
	Signetics	7405	
	TI	SN7405	
7406	Fairchild	7406	
	Hitachi	HD7406	
	ITT	ITT7406	
	Mitsubishi	M53206	
	Motorola	MC7406	
	National	DM7406	
	Signetics	7406	
	TI	SN7406	
7407	Fairchild	7407	
	Hitachi	HD7407	
	ITT	ITT7407	
	Mitsubishi	M53207	
	Motorola	MC7407	
	National	DM7407	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

TRW (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
7407	Signetics	7407	
	TI	SN7407	
7408	Fairchild	7408	
	ITT	ITT7408	
	Mitsubishi	M53208	
	Motorola	MC7408	
	National	DM7408	
	Raytheon	7408	
	Signetics	7408	
	TI	SN7408	
	Toshiba	TC7408	
7409	Fairchild	7409	
	Hitachi	HD7409	
	ITT	ITT7409	
	Mitsubishi	M53209	
	Motorola	MC7409	
	National	DM7409	
	Raytheon	7409	
	Signetics	7409	
	TI	SN7409	
7410	Fairchild	7410	
	Hitachi	HD7410	
	ITT	ITT7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
	National	DM7410	
	NEC America	μPB7410	
	Raytheon	7410	
	Signetics	7410	
	TI	SN7410	
		SN7427	
	Toshiba	TC7410	
74111	TI	SN74111	
7412	Fairchild	7412	
	Hitachi	HD7412	
	ITT	ITT7412	
	Raytheon	7412	
	Signetics	7412	
	TI	SN7412	
74121	Fairchild	74121	
	Hitachi	HD74121	
	ITT	ITT74121	
	Mitsubishi	M53321	
	Motorola	MC74121	
	National	DM74121	
	Signetics	74121	
	TI	SN74121	
74123	AMD	SN74123	
	Fairchild	74123	
	ITT	ITT74123	
	Mitsubishi	M53323	
	Motorola	MC74123	
	National	DM74123	
	NEC America	μPB74123	
	Raytheon	74123	
	Signetics	74123	
	TI	SN74123	
7413	Fairchild	7413	
	ITT	ITT7413	
	Mitsubishi	M53213	
	Motorola	MC7413	
	National	DM7413	
	NEC America	μPB7413	
	Signetics	7413	
	TI	SN7413	
74136	Hitachi	HD74136	
	Motorola	MC74136	
	Raytheon	74136	
	TI	SN74136	
74145	Fairchild	74145	
	ITT	ITT74145	
	Mitsubishi	M53345	
	Motorola	MC74145	
	National	DM74145	
	Raytheon	74145	
	Signetics	74145	
	TI	SN74145	
74150	Fairchild	74150	
	Hitachi	HD74150	
	Mitsubishi	M53350	
	Motorola	MC74150	
	National	DM74150	
	NEC America	μPB74150	
74150	Raytheon	74150	
	Signetics	74150	
	TI	SN74150	
74151	Fairchild	74151	
	Hitachi	HD74151	
	ITT	ITT74151	
	Mitsubishi	M53351	
	Motorola	MC74151	
	National	DM74151	
	NEC America	μPB74151	
	Raytheon	74151	
	Signetics	74151	
	TI	SN74151	
74152	Fairchild	74152	
	Motorola	MC74152	
	Raytheon	74152	
74153	Fairchild	74153	
	ITT	ITT74153	
	Mitsubishi	M53353	
	Motorola	MC74153	
	National	DM74153	
	NEC America	μPB74153	
	Raytheon	74153	
	Signetics	74153	
	TI	SN74153	
74154	AMD	SN74154	
	Fairchild	74154	
	Mitsubishi	M53354	
	Motorola	MC74154	
	National	DM74154	
	NEC America	μPB74154	
	Raytheon	74154	
	Signetics	74154	
	TI	SN74154	
74155	Fairchild	74155	
	ITT	ITT74155	
	Mitsubishi	M53355	
	Motorola	MC74155	
	National	DM74155	
	NEC America	μPB74155	
	Raytheon	74155	
	Signetics	74155	
	TI	SN74155	
74156	Fairchild	74156	
	Hitachi	HD74156	
	ITT	ITT74156	
	Mitsubishi	M53356	
	Motorola	MC74156	
	National	DM74156	
	NEC America	μPB74156	
	Raytheon	74156	
	Signetics	74156	
	TI	SN74156	
7416	Fairchild	7416	
	Hitachi	HD7416	
	ITT	ITT7416	
	Mitsubishi	M53216	
	Motorola	MC7416	
	National	DM7416	
	Signetics	7416	
	TI	SN7416	
74160	AMD	SN74160	
	Fairchild	74160	
	Hitachi	HD74160	
	ITT	ITT74160	
	Mitsubishi	M53360	
	Motorola	MC74160	
	National	DM74160	
	Raytheon	74160	
	Signetics	74160	
	TI	SN74160	
74161	AMD	SN74161	
	Fairchild	74161	
	Hitachi	HD74161	
	ITT	ITT74161	
	Mitsubishi	M53361	
	Motorola	MC74161	
	National	DM74161	
	NEC America	μPB74161	
	Raytheon	74161	
	Signetics	74161	
	TI	SN74161	
74162	AMD	SN74162	
	Fairchild	74162	
	Hitachi	HD74162	
	ITT	ITT74162	
74162	Mitsubishi	M53362	
	Motorola	MC74162	
	National	DM74162	
	Raytheon	74162	
	Signetics	74162	
	TI	SN74162	
74163	AMD	SN74163	
	Fairchild	74163	
	Hitachi	HD74163	
	ITT	ITT74163	
	Mitsubishi	M53363	
	Motorola	MC74163	
	National	DM74163	
	Raytheon	74163	
	Signetics	74163	
	TI	SN74163	
7417	Fairchild	7417	
	Hitachi	HD7417	
	ITT	ITT7417	
	Mitsubishi	M53217	
	Motorola	MC7417	
	National	DM7417	
	Signetics	7417	
	TI	SN7417	
74180	Fairchild	74180	
	Hitachi	HD74180	
	ITT	ITT74180	
	Mitsubishi	M53380	
	Motorola	MC74180	
	National	DM74180	
	NEC America	μPB74180	
	Raytheon	74180	
	Signetics	74180	
	TI	SN74180	
7420	Fairchild	7420	
	Hitachi	HD7420	
	ITT	ITT7420	
	Mitsubishi	M53220	
	Motorola	MC7420	
	National	DM7420	
	NEC America	μPB7420	
	Raytheon	7420	
	Signetics	7420	
	TI	SN7420	
	Toshiba	TC7420	
7426	Fairchild	7426	
	Hitachi	HD7426	
	ITT	ITT7426	
	Motorola	MC7426	
	National	DM7426	
	Signetics	7426	
	TI	SN7426	
74290	Fairchild	74290	
	Mitsubishi	M53490	
	Motorola	MC74290	
	TI	SN74290	
74293	Fairchild	74293	
	Mitsubishi	M53493	
	Motorola	MC74293	
	TI	SN74293	
7430	Fairchild	7430	
	Hitachi	HD7430	
	ITT	ITT7430	
	Mitsubishi	M53230	
	Motorola	MC7430	
	National	DM7430	
	NEC America	μPB7430	
	Signetics	7430	
	TI	SN7430	
7437	Fairchild	7437	
	ITT	ITT7437	
	Mitsubishi	M53237	
	Motorola	MC7437	
	National	DM7437	
	NEC America	μPB7437	
	Raytheon	7437	
	Signetics	7437	
	TI	SN7437	
7438	Fairchild	7438	
	ITT	ITT7438	
	Mitsubishi	M53238	
	Motorola	MC7438	
	National	DM7438	
	NEC America	μPB7438	
	Raytheon	7438	
	Signetics	7438	
7438	TI	SN7438	
7440	Fairchild	7440	
	Hitachi	HD7440	
	ITT	ITT7440	
	Mitsubishi	M53240	
	Motorola	MC7440	
	National	DM7440	
	NEC America	μPB7440	
	Signetics	7440	
	TI	SN7440	
7445	Fairchild	7445	
	ITT	ITT7445	
	Mitsubishi	M53245	
	Motorola	MC7445	
	National	DM7445	
	NEC America	μPB7445	
	Raytheon	7445	
	Signetics	7445	
	TI	SN7445	
7450	Fairchild	7450	
	Hitachi	HD7450	
	ITT	ITT7450	
	Mitsubishi	M53250	
	Motorola	MC7450	
	National	DM7450	
	NEC America	μPB7450	
	Signetics	7450	
	TI	SN7450	
7451	Fairchild	7451	
	Hitachi	HD7451	
	ITT	ITT7451	
	Motorola	MC7451	
	National	DM7451	
	NEC America	μPB7451	
	Signetics	7451	
	TI	SN7451	
7453	Fairchild	7453	
	Hitachi	HD7453	
	ITT	ITT7453	
	Mitsubishi	M53253	
	Motorola	MC7453	
	National	DM7453	
	NEC America	μPB7453	
	Signetics	7453	
	TI	SN7453	
7454	Fairchild	7454	
	Hitachi	HD7454	
	ITT	ITT7454	
	Motorola	MC7454	
	National	DM7454	
	NEC America	μPB7454	
	Signetics	7454	
	TI	SN7454	
7460	Fairchild	7460	
	Hitachi	HD7460	
	Mitsubishi	M53260	
	Motorola	MC7460	
	National	DM7460	
	NEC America	μPB7460	
	Signetics	7460	
	TI	SN7460	
7472	Fairchild	7472	
	Hitachi	HD7472	
	ITT	ITT7472	
	Mitsubishi	M53272	
	Motorola	MC7472	
	National	DM7472	
	Signetics	7472	
	TI	SN7472	
7474	Fairchild	7474	
	Hitachi	HD7474	
	ITT	ITT7474	
	Mitsubishi	M53274	
	Motorola	MC7474	
	National	DM7474	
	NEC America	μPB7474	
	Raytheon	7474	
	Signetics	7474	
	TI	SN7474	
7475	Fairchild	7475	
	Hitachi	HD7475	
	ITT	ITT7475	
	Mitsubishi	M53275	
	Motorola	MC7475	
	National	DM7475	
	Signetics	7475	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Manufacturer Device	Replacement Source	Device	IC Master Page
TRW (cont'd)			
7475	TI	SN7475	
7476	Fairchild	7476	
	ITT	ITT7476	
	Mitsubishi	M53276	
	Motorola	MC7476	
	National	DM7476	
	NEC America	μPB7476	
	Signetics	7476	
	TI	SN7476	
7481	TI	SN7481	
7485	Fairchild	7485	
	Hitachi	HD7485	
	Mitsubishi	M53285	
	Motorola	MC7485	
	National	DM7485	
	NEC America	μPB7485	
	Signetics	7485	
	TI	SN7485	
7486	Fairchild	7486	
	Hitachi	HD7486	
	ITT	ITT7486	
	Mitsubishi	M53286	
	Motorola	MC7486	
	National	DM7486	
	NEC America	μPB7486	
	Raytheon	7486	
	Signetics	7486	
	TI	SN7486	
7489	AMD	SN7489	
	Fairchild	7489	
	Mitsubishi	M53289	
	National	**DM7489**	**1287**
	TI	SN7489	
7490	Fairchild	7490	
	Hitachi	HD7490	
	ITT	ITT7490	
	Mitsubishi	M53290	
	Motorola	MC7490	
	National	DM7490	
	Signetics	7490	
	TI	SN7490	
7492	Fairchild	7492	
	Hitachi	HD7492	
	ITT	ITT7492	
	Mitsubishi	M53292	
	Motorola	MC7492	
	National	DM7492	
	Signetics	7492	
	TI	SN7492	
7493	Fairchild	7493	
	Hitachi	HD7493	
	ITT	ITT7493	
	Mitsubishi	M53293	
	Motorola	MC7493	
	National	DM7493	
	Signetics	7493	
	TI	SN7493	
7496	Fairchild	7496	
	Hitachi	HD7496	
	ITT	ITT7496	
	Mitsubishi	M53296	
	Motorola	MC7496	
	National	DM7496	
	Signetics	7496	
	TI	SN7496	
Western Digital			
BR1941	SMC	COM5016	
FD1771	National	INS1771	
♦RM1701	Intel	2107	
	TI	TMS4030	
		TMS4060	
♦RM4096	Mostek	MK4096	
TR1402	SMC	COM2502	
TR1402A	GI	AY5-1013A	
	SMC	COM2502H	
TR1602	**AMI**	**S1883**	**354,1587**
	GI	AY3-1014A	
		AY3-1015	
		AY5-1013A	
	SMC	COM2017	
TR1602	SMC	COM2502	
	TI	TMS6011	
UC1671	National	INS1671	
	SMC	COM1671	
Zilog			
Z6116	**Fairchild**	**F16K**	**1110**
	Intel	2117	
	Intersil	7116	
	Mostek	MK4116	
	Motorola	MCM4116	
	NEC Micro	**μPD416**	**1402**
	TI	TMS4070	
Z80	**NEC Micro**	**μPDZ-80**	**1850**
Z80-CPU	Mostek	MK3880	
Z80-CTC	Mostek	MK3882	
Z80-DMA	Mostek	MK3883	
Z80-PIO	Mostek	MK3881	
Z80-SIO	Mostek	MK3884	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

ABBREVIATIONS OF COMPANY NAMES

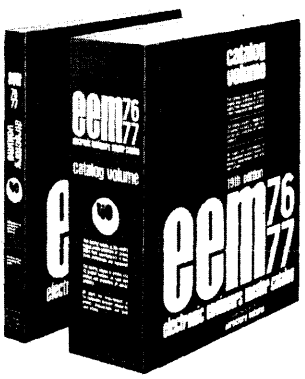
AD	Analog Devices
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Analogic	Analogic Corp.
Beckman	Beckman Instruments, Helipot Division
Burr-Brown	Burr-Brown Research
Cermetek	Cermetek
CMA	Consumer Microcircuits of America
Cybernetic	Cybernetic Micro Systems
Data General	Data General
Datel	Datel Systems
DDC	Data Devices Corp.
Delco	Delco Electronics
EA	Electronic Arrays
EMM/Semi	EMM Semi, Div. of Electronic Memories & Magnetics
Essex	Essex International
Exar	Exar Integrated Systems
Fairchild	Fairchild
Ferranti	Ferranti Electric
Fujitsu	Fujitsu
GI	General Instrument
Harris	Harris Semiconductor
Hitachi	Hitachi America Ltd.
Hughes	Hughes Aircraft Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
IMI	International Microcircuits, Inc.
Intech/FMI	Intech/Function Modules Inc.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
IPI	Integrated Photomatrix, Inc.
ITT	ITT Semiconductors
Lambda	Lambda Electronics
LSI	LSI Computer Systems
Master Logic	Master Logic
Micro Comp	Micro Components
Micro Net	Micro Networks
Micropac	Micropac Industries
Micro Power	Micro Power Systems
Micro Tech	Microcircuits Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electric Co.
MMI	Monolithic Memories, Inc.
MOS	MOS Technology
Mostek	Mostek
Motorola	Motorola Semiconductor
National	National Semiconductor
NCR	NCR Corp., Microelectronics Division
NEC	NEC America
NEC	NEC Microcomputers
Nippon	Nippon Electric Co.
Nitron	Nitron
Nortec	Nortec Electronics
Novonics	Novonics
OEI	Optical Electronics, Inc.
Panasonic	Panasonic, Matsushita Electric Corp.
Photo Therm	Photo Therm
Plessey	Plessey Semiconductors
PMI	Precision Monolithics, Inc.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell Microelectronic Division
RTC	Real Time Corp.
Sanken	Sanken Electric
Sanyo	Sanyo Electric
SGS	SGS-Ates Semiconductor
Siemens	Siemens
Signetics	Signetics (Philips)
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys.	Silicon Systems, Inc.
Silitronics	Silitronics
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSM	Solid State Music
SSS	Solid State Scientific
Synertek	Synertek
Tektronix	Tektronix
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	AEG-Telefunken
TI	Texas Instruments
TMX	TMX
Toshiba	Toshiba
Trans-Data	Trans-Data
TRW	TRW
Western	Western Digital
Zilog	Zilog

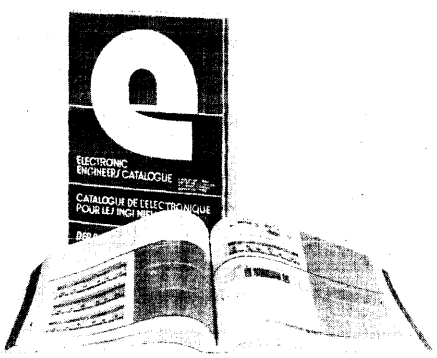
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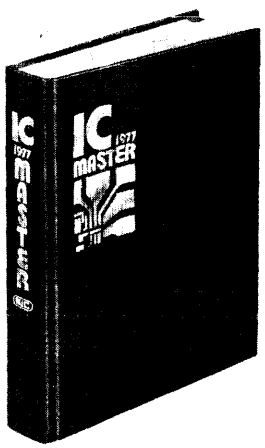
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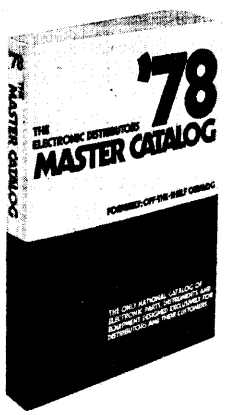
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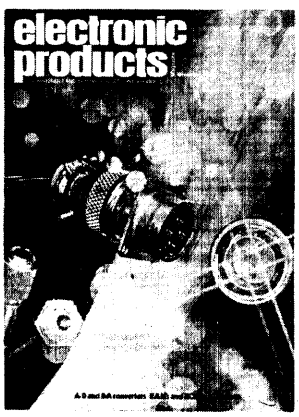
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Burr-Brown, (714) 835-0712
CO **Denver**
Sales Office, Enterprise 6730
CT **Southbury**
Sales Representative, (800) 645-8212; (516) 466-2650
FL **Orlando**
BCS Assocs., (305) 896-4881
IL **Addison**
Burr-Brown, (312) 832-6520
MA **Reading**
MECO, (617) 944-6660
MD **Bethesda**
Powell-Pendergraph, (301) 656-4535
MI **Brighton**
Sheridan Marketing, (313) 227-1786
Grand Rapids
Sheridan Marketing, (616) 942-2504
MN **Bloomington**
Electronic Sales, (612) 884-8291
MO **Florissant**
Sheridan Marketing, (314) 837-5200
NC **Greensboro**
BCS Assocs., (919) 273-1918
NM **Albuquerque**
Sales Office, Enterprise 6730
NY **Clinton**
Advanced Comps. Corp., (315) 853-6438
Endicott
Advanced Comps. Corp., (607) 785-3191
Great Neck, L.I.
Burr-Brown, (516) 466-2650
Scottsville
Advanced Comps. Corp., (716) 889-1429
Syracuse
Advanced Components, (315) 699-2671
OH **Cleveland**
Sheridan Marketing, (216) 292-2982
Dayton
Sheridan Marketing, (513) 435-3181
OK **Tulsa**
Norvell Assocs., (918) 663-1247
PA **Hatboro**
QED Electronics, (215) 674-9600
Pittsburgh
Sheridan Marketing, (412) 782-5120
TX **Ausfin**
Norvell Assocs., (512) 458-8106
Dallas
Norvell Assocs., (214) 233-0020
Houston
Norvell Assocs., (713) 777-1666
UT **Salt Lake City**
Sales Office, Zenith 6730
VA **Richmond**
Powell Pendergraph, (804) 264-2341
WA **Lynnwood**
Industrial Electronics Instruments, (206) 775-3516
Can **Calgary, Alberta**
Allan Crawford Assocs., (403) 276-9658
Dartmouth, Nova Scotia
Allan Crawford Assocs., (902) 469-7865
Longueuil, Quebec
Allan Crawford Assocs., (514) 670-1212
Mississauga, Ontario
Allan Crawford Assocs., (416) 678-1500
Ottawa, Ontario
Allan Crawford Assocs., (613) 829-9651
Voncouver, B.C.
Allan Crawford Assocs., (604) 980-4831
Intl **Australia**
Burwood, Victoria
Kenelec Systems (Pty.) Ltd., Tel: (03) 288-7100
Intl **Austria, Wien**
Dipl. Ing. Peter Marchetti, Tel: 57 82 30
Intl **Belgium, Brussels**
BETEA, Tel: (02) 49 99 00
Intl **Denmark, Copenhagen O**
Mer-el A/S, Tel: 20 74 44
Intl **England, Watford**
Burr-Brown International, Ltd., Tel: (0923) 33837
Intl **Finland, Helsinki**
Nores & Company OY, Tel: 13360
Intl **France, Le Chesnay**
Burr-Brown International S.A. Tel: 954-3558
Intl **Germany**
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Burr-Brown International, Ltd., Tel: 0421/61 22 73
Leinfelden Stuttgart
Burr-Brown International GmbH, Tel: (0711) 75 30 21
Munchen
Burr-Brown International, Ltd., Tel: 089/61 7737
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Hellenci Scientific Representations Lts., Tel: 7705 960
Intl **Holland, Schiphol Oost**
Burr-Brown International, Ltd., Tel: (020) 470590
Intl **Japan, Tokyo**
Burr-Brown International, Ltd., Tel: (03) 586-8141
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Oriole Services & Consultants Pty., Ltd., Tel: 551973
Intl **New Zealand, Aukland**
W. & K. McLean LtLd., Tel: 587 037
Intl **Norway, Oslo**
Hugo Riso A/S, Tel: 23 2580
Intl **Pakistan, Karachi**
I & S Corporation, Tel: 437669
Intl **Portugal, Lisbon**
Telectra, Tel: 686072
Intl **So. Africa, Johannesburg**
David Pollock (Pty.) Ltd., Tel: 724 8274
Intl **Spain, Madrid**
Anadig Ingenieros, S.A., Tel: 443-24-12
Intl **Sweden, Vallingby**
Teleinstrument AB, Tel: 08380370
Intl **Switzerland, Rüschlikon**
Burr-Brown International, Ltd., Tel: 01/724 0428
Intl **Turkey, Istanbul**
Telekom, Tel: 49 40 40

Cermetek

Cermetek, Incorporated
660 National Avenue
Mountain View, California 94043
(415) 969-9433
TWX: 910-379-6931

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Nakoma, (602) 931-9103
CA **Costa Mesa**
Relcom, (714) 549-3674
Los Altos,
PM Sales, (415) 941-4444
Marina del Ray
Relcom, (213)822-1187
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Kitchen & Kutchin, Inc., (203) 239-0212
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Brennan Associates, Inc., (813) 446-5006
IL **Chicago**
I.R.I., (312) 647-7755
MA **Framingham**
Field Sales Office (617) 879-3250
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Kitchen & Kutchin, Inc., (617) 862-8230
MN **Minneapolis**
Jos Co/Melius, Inc., (612) 861-3343
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Compar New York, (201) 546-3660
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Canavan-Scanlon Assoc., Inc., (716) 442-0720
Syracuse
Canavan-Scanlon Assoc., Inc., (315) 437-1271
NM **Albuquerque**
Tritronix/Albuquerque, (505) 265-8400
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Marlow Assoc., (216) 932-0900
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Marlow Assoc., (513) 866-4991
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Rivco, Inc., (215) 265-5211
Pittsburgh
Marlow Assoc., (412) 831-6113
TX **Austin**
The Cunningham Co., (512) 459-8947
Dallas
The Cunningham Co., (214) 233-4303
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The Cunningham Company (713) 461-4197
VA **Arlington**
H. J. Heffernan Company, (703) 522-6666
WI **Milwaukee**
I.R.I., (414) 259-0966
Can **Montreal, Quebec**
Consolidated Cybernetics Controls Ltd., (514) 934-0000
Intl **Palo Alto, California**
Western International Trade Corp., Tel: (415) 321-1240

Consumer Microcircuits of America

Consumer Microcircuits of America
114 E. Simmons Street
Galesburg, IL 61401
(309) 342-5311 or (309) 342-8196

Sales Offices & Representatives

DC **Washington, D.C.**
Dou Boyle, (703) 620-9598
IL **Chicago**
Bob Bode, (312) 774-1952

Cybernetic Micro Systems

Cybernetic Micro Systems
2460 Embarcadero Way
Palo Alto, CA 94303
(415) 321-0410

Data Device Corp.

ILC Data Device Corp.
Airport International Plaza
Bohemia, New York 11716
(516) 567-5600
TWX: (510) 228-7324

Sales Offices & Representatives

AL **Huntsville**
REP Inc., (205) 881-9270
AZ **Phoenix**
ILC Data Device Corporation, (602) 249-0703
Scottsdale
OEM Specialties, (602) 948-3360
CA **Culver City**
DeAngelo, Rothman & Co., Inc., (213) 398-6239
North Hollywood
ILC Data Device Corporation, (213) 982-6454
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Coherent Marketing Asssociates, (415) 327-2217
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DeAngelo, Rothman & Co., Inc., (714) 560-5707
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Herb Bass Associates, (303) 499-7509
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EIR, Inc., (305) 830-9600
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REP Inc., (404) 938-4358
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Data Systems Marketing, (DSM) (301) 933-6111
MI **Southfield**
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MN **St. Paul**
DYTEC/North, Inc., (612) 645-5816
MO **Hazelwood**
DYTEC/South, Inc., (314) 731-5400
NC **Raleigh**
REP Inc., (919) 851-3007
NM **Albuquerque**
Trembly Associates, (506) 266-8616
NY **East Syracuse**
Nycom, Inc., (315) 437-8343
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Measurement Technology, Inc., (516) 482-3500, (212) 895-7177
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Luebbe Sales Company, (216) 333-0425
Dayton
Luebbe Sales Company, (513) 294-0426
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RIVCO, Inc., (215) 265-5211
TN **Jefferson City**
REP Inc., (615) 475-4105
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Martin, Zienkosky & Browne, (214) 233-5535
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Martin, Zienkosky & Browne, (713) 523-7333
WA **Redmond**
DESCO, Northwest, (206) 455-9325
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Ottawa, Ontario
Associated Test Equipment Ltd., (613) 728-3717
Scarborough, Ontario
Associated Test Equipment Ltd., (416) 497-2208
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Associated Test Equipment Ltd., (604) 734-2012

Data General

Data General Corporation
Route 9
Southboro, Massachusetts 01772
(617) 485-9100
TWX: (710) 390-0309
Telex: 94-8460

Specific product information:
MicroNOVA: (800) 225-9497

Datel Systems

Datel Systems
1020 Turnpike Street
Canton, Massachusetts 02021
(617) 828-8000
TWX: (710) 348-0135
Telex: 92-4461

Specific Product Information:
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Application Engineering:
Eugene Murphy .....ext. 141
Literature:
Arlene Constantine .....ext. 126
Price and Delivery:
Mary Pimantel .....ext. 131
Follow up an order:
Bill Collins .....ext. 194

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Datel Systems, Inc., (714) 835-2751, 2752, or 2753
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Datel Systems, Inc., (408) 733-2424
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Cleveland Enterprises of Colorado, (303) 751-3252
CT **Glastonbury**
Datel Systems, Inc., (203) 633-1778
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Saber Associates, Inc., (305) 422-3686, (800) 432-3007
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IL **Chicago**
Carter Electronics, Inc., (312) 585-5485
IN **Indianapolis**
Carter Electronics, Inc., (317) 293-0696
KS **Olathe**
Technical Representatives, Inc., (913) 732-1177
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Datel Systems, Inc., (617) 828-8000
MD **Gaithersburg**
Datel Systems, Inc., (301) 840-9490 or 9491
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George R. Peters Associates, (313) 362-1220
MN **Minneapolis**
Carter Electronics, Inc., (612) 559-1976
MO **Hazelwood**
Technical Representatives, Inc., (314) 731-5200
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Eastern Instrumentation, Inc., (201) 567-9505, (201) 661-2000

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Instrumentation Systems, Inc., (513) 294-2838
Cleveland
Instrumentation Systems, Inc., (216) 486-0782
OK **Tulsa**
Component Specialties, (918) 664-2820
PA **Pittsburgh**
Instrumentation Systems, Inc., (412) 243-1111
TX **Austin**
Component Specialties, (512) 459-3308
Dallas
Component Specialties, (214) 357-6511
Houston
Component Specialties, (713) 771-7237.
Datel Systems, Inc., (713) 932-1130, (713) 932-1132
WA **Bellevue**
Tasco, Inc., (206) 453-1414
WI **Milwaukee**
Carter Electronics, Inc., (414) 464-5555
Can **Mississauga, Ontario**
Prelco Electronics, Ltd., (416) 678-0401
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Prelco Electronics, Ltd., (514) 389-8051
Ottawa, Ontario
Multilek, Inc., (613) 825-4695
Prelco Electronics, Ltd., (613) 226-3491
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Sydney
Digital Electronics (Marketing) Pty Ltd., Tel: 438-2444
East Hawthorne, Victoria
Digital Electronics, Tel: 20-7839
Intl **Austria, Vienna**
Bacher Elektronische Gerate Ges. M.B.H., Tel: 83 62 96 0° or 83 71 52 0°
Unitechnik, Tel: (0222) 95 10 433
Intl **Belgium, Brussels**
Simac Electronics sprl, Tel: 02-6724556
Intl **Chile, Santiago**
Alta Internacional, Tel: 723740, 723754
Intl **Denmark, Vaiby**
Paratron A/S, Tel: (01) 74-44-66
Intl **England, Andover, Hants**
Datel (UK) Ltd., Tel: Anover (0264) 51055
Intl **Finland, Helsinki**
Havulinna OY, Tel: (90) 661 451
Intl **France, Paris**
Datel Systems, S.A.R.L., Tel: 620-06-74
Intl **Germany**
Berlin
Ing. — Buero Brieger, Tel: 030-3664433
Muenchen
Datelek Systems, GmbH, Tel: 5212855
Intl **Greece, Piraeus**
General Electronics, Ltd., Tel: 491-3595
Intl **India, Bombay**
Electronic Enterprises, Tel: 443096
Smitronix International, Tel: 536238
Intl **Israel, Tel-Aviv**
MTI Engineering Ltd., Tel: 244090 or 236334
Intl **Italy, Milano**
3G Electronics S.R.L., Tel: 544291 or 543096
Intl **Japan, Tokyo**
Datel KK, Tel: 793-1031
Intl **Korea, Seoul**
Dong-IL Commerce & Co. Ltd., Tel: 75-6841-5
Korea United Trading Corp., Tel: 76-2501; 2502
Intl **Netherlands, Veldhoven**
Simac Electronics b.v., Tel: 040-533725
Intl **New Zealand, Auckland**
David Reid Professional Productions Ltd., Tel: 492-189
Intl **Norway, Oslo**
Morgenstierne & Co. A/D, Tel: 37 29 40
Intl **Portugal, Porto**
Commercial Laborum, Lda., Tel: 62925
Intl **South Africa, Johannesburg**
Peter Jones Electronic Equipment (Pty.) Ltd., Tel: 22-3658
Intl **Spain**
Barcelona
Aupoca Electronica y Sistemas, Tel: 257 48 98
Madrid
Aupoca Electronica y Sistemas, Tel: 457 53 12
Intl **Sweden, Stockholm**
Martinsson & Company, AB, Tel: 08-63 11 05
Intl **Switzerland, Zurich**
Traco Electronic Company Ltd., Tel: 01/ 36 07 11
Intl **Taiwan, Taipei**
C C T Associates, Inc., Tel: (02) 393-5760, 321-4542
Industrial Electronics, Tel: 774257
Multitech $nternational Corp., Tel: (02) 7681232, 7650492

Delco Electronics

Delco Electronics Division
700 East Firmin St.
Kokomo, Indiana 46901
(317) 459-2175
William J. Gressman

Delco Electronics Division
4600 Park Road
Charlotte, North Carolina 28209
(704) 527-4444
Anthony E. Manes

Electronic Arrays

Electronic Arrays, Inc.
550 E. Middlefield Road
Mountain View, California 94043
(415) 964-4321
TWX: (910) 379-6985
Toll Free WATS: (800) 227-9962

Specific Product Information:
LSI Products ..... Mike Cassidy
Memory Products ..... Maurice O'Shea
Literature
Marketing Services ..... Debbie Dunkley
Price and Delivery:
Local Field Sales Offices (preferred), or Customer Service
Follow-up on Order:
Customer Service
All Other Information:
Marketing Services ..... Debbie Dunkley

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AZ **Phoenix**
Chaparral-Dorton, (602) 263-0414
CA **Goleta**
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Los Angeles
The Thorson Company, (213) 476-1241
Mountain View
Caltron Components Corp., (415) 964-3244
Regional Sales Office, (415) 964-4321
San Diego
Cerco Sales Engineers, (714) 560-9143
Tustin
The Thorson Company, (714) 544-5121
CO **Denver**
The Thorson Company, (303) 759-0809
CT **Greenwich**
Crane & Egbert Corp., (203) 622-9191
Wallingford
Com-Sale, (203) 269-7964
FL **Ft. Lauderdale**
Electrocomp Associates, Inc., (305) 491-4141
IL **Oak Brook**
Regional Sales Office, (312) 920-1410
Westchester
Gassner & Clark Company, (312) 345-4245
IN **Ft. Wayne**
M. S. Sales, (219) 484-3925
MA **Carlisle**
Regional Sales Office, (617) 369-2982
Waltham
Com-Sale, Inc., (617) 890-0011
MN **Bloomington**
Electronic Sales Agency, (612) 884-8291
NH **Londonberry, Manchester**
Com-Sale, Inc., (603) 668-1440
NM **Albuquerque**
The Thorson Company, (505) 265-5655
NY **Buffalo**
Quality Component, Inc., (716) 839-4170
Elmont
Crane & Egbert Corp., (516) 488-2100
Manlius
Quality Component, Inc., (315) 682-8885
OH **Chagrin Falls**
Midwest Marketing Associates, (216) 247-6655
Dayton
Midwest Marketing Associates, (513) 433-2511
OR **Beaverton**
N. R. Schultz Company, (503) 643-1644
PA **Bala Cynwyd**
Vantage Sales Co., (215) 667-0990
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J. Clay Co., (214) 350-1281
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Boyle Associates, (703) 620-9558
WA **Bellevue**
N. R. Schultz Co., (206) 454-0300
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Repco Engineering Co., (514) 683-7956
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Intl **Belgium, Brussels**
Betea Spri., Tel: 02 649 99 00
Intl **Denmark, Hoersholm**
C-88, Tel: 02-813332
Intl **Finland, Helsinki**
S.W. Instruments, Tel: 738265/713575
Intl **France, Paris**
Technology Resources S.A., Tel: 01 747 4717
Intl **Germany, Munchen**
Electronic Array GmbH, Tel: 089/7853168
Intl **Holland, Breda**
Famatra Benelux, Tel: 076-133457
Intl **Hong Kong, Kowloon**
S.S.I. Far East Limited, Tel: 3-672112-3. 3-680411
Intl **Hungary, Budapest**
Hinicoop, Tel: 1 429779
Intl **India, Bombay**
Hinditron Services Pvt. Ltd., Tel: 36 5 3 44
Intl **Israel, Ramat-Gan**
Telsys, Ltd., Tel: 739865, 722362
Intl **Italy, Milano**
Comprel Elettronica, Tel: 2.6438519/763
Intl **Japan**
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Rikel Corporation, Tel: 06 (374) 1771
Tokyo
Rikel Corporation, Tel: 03-591-5241
Intl **Korea, Seoul**
Caduceus, Ltd., Tel: 777-2325
Intl **Norway, Kjellergy**
Kjell Bakke, Tel: 02 711872
Intl **South and Central America, Mountain View, California**
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Intl **Spain, Madrid**
Belport Electronica, Tel: 01 262 88 37/8
Intl **Sweden, Vallingby**
Svensk Tele Industri, Tel: 08/89 04 35
Intl **Switzerland, Zurich**
Dimos AG, Tel: 01-626 140
Intl **United Kingdom, Molesey, Surrey**
Analog Devices, Ltd., Tel: 01 941 0466
Intl **Yugoslavia, Maribor**
Ellyptic AG, Tel: (062) 31041

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Weatherford Company, (213) 966-8461
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Intermark Electronics, (714) 540-1322
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Intermark Electronics, (714) 453-9005
Weatherford Company, (714) 278-7400

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IN **Indianapolis**
Advent Electronics, Inc., (317) 297-4910
IA **Cedar Rapids**
Advent Electronics, Inc., (319) 363-0221
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Zeus Components, Inc., (516) 752-9551
TX **Dallas**
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Houston
Quality Components, Inc., (713) 772-7100
UT **Salt Lake City**
Century Electronics, (801) 847-8551
WA **Seattle**
Weatherford Company, (206) 243-6340

EMM/Semi

EMM/Semi
3883 North 28th Avenue
Phoenix, Arizona 85017
(602) 263-0202
TWX: (910) 951-1383

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EMM/Semi, (213) 644-9681
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EMM/Semi, (213) 598-8705
El Segundo
Varigon, (213) 322-1120
FL **Orlando**
Gentry Assoc., (305) 894-4401
GA **Atlanta**
Gentry Assoc., (404) 455-1206
IL **Des Plains**
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EMM/Semi, (617) 861-9650
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EMM/Semi, (612) 933-7115
NC **Burlington**
Gentry Assoc, (919) 227-3639
NJ **Cherry Hill**
EMM/Semi, (606) 779-7911
NY **Melville**
EMM/Semi, (516) 423-5800
TX **Dallas**
EMM/Semi, (214) 231-2539
Young Sales, (214) 341-2900
WA **Bellevue**
Thorson Company, 206) 455-9180
Can **Montreal**
Cantec, (514) 620-3121
Ottawa
Contec, (613) 225-0363
Toronto
Cantec, (416) 457-4455
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Intl **England, Feltham**
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Intl **France, Paris**
EMM, c/o CLIp, (01) 754-2319
Intl **Germany, Bad Homburg**
EMM, GmbH 6172-6629
Intl **Israel, Tel-Aviv**
STG International

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Sterling Eectronics, (415) 592-2353
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Semicomp Corp., (408) 736-2330
CO **Wheat Ridge**
Century Electronics, (303) 424-1985
CT **Hamden**
Arrow, (203) 248-3801
FL **Ft. Lauderdale**
Arrow, (305) 776-7790
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Sterling Eectronics, (617) 926-9720
MD **Baltimore**
Arrow, (301) 247-5200, (202) 737-1700
MN **Bloomington**
Arrow, (612) 888-5522
NJ **Moorestown....**
Arrow, (609) 235-1900
Perth Amboy
Sterling Eectronics, (201) 442-8000
Saddlebrook
Arrow, (201) 797-5800
NM **Albuquerque**
Century Electronics, (505) 292-2700
Sterling Electronics, (505) 345-6601
NY **Farmingdale**
Arrow, (516) 694-6800
Fishkill
Arrow, (914) 896-7530
OH **Cleveland**
Arrow, (216) 464-2000
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Arrow, (513) 253-9176
Kettering
Arrow, (513) 253-9176
TX **Dallas**
Sterling Electronics, (214) 357-9131
Houston
Sterling Electronics, (713) 627-9800
UT **Salt Lake City**
Century Electronics, (801) 487-8551
WA **Seattle**
Sterling Electronics, (206) 762-9100
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Arrow, (414) 782-2801
Can **Montreal, Quebec**
Future Electronics, (514) 735-5775
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Ottawo, Ontario
Zentronics, (613) 238-6411
Toronto, Ontario
Future Electronics, (416) 677-7820
Zentronics, (416) 635-2822
Vancouver
Future Electronics, (604) 261-1335
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Sharon Hites
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Integrated Circuits
464 Ellis Street
Mountain View, California 94042
(415) 962-5011
TWX:(910)379-6345

Fairchild Camera and Instrument Corp..
Microsystems
1725 Technology Drive
San Jose, California 95110
(408) 998-0123
TWX: (910) 338-0558

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Pan Electron Inc., Tel: 045-471-8811

Intl **Mexico**
Mexitek, S.A., Tel: 5-36-09-10 or 5-43-03-77

Intl **Singapore, Senbawang**
Electronic & Engineering (Pte.) Ltd., Tel: 2570211, 591141 Ex. 5201

LSI Computer Systems

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1235 Walt Whitman Road
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Literature:
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Price and delivery:
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Follow-up an order:
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San Diego
MESA, (714) 278-8021

IL **Bellwood**
Fiat Engineering Associates, (312) 547-6200

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Gans, Fryling, & Pugh, Inc., (301) 837-6311

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Mech-Tron Company, (603) 424-5300

NJ **Wallington**
Comp-Tech Sales, (201) 935-5454

NY **New Hyde Park**
Comp-Tech Sales, (516) 593-2628
Penfield
Barthel Enterprises, (716) 377-3018

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Components, Inc., (216) 243-9200

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Jackson Arnold Company, (713) 783-9522

Intl **Argentina, Buenos Aires**
Nucles, Tel: 46-9549

Intl **Japan, Tokyo**
Corton Trading Company, Tel: (03) 49907141/2

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Master Logic Corporation
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Micro Components

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Florence and Meyer, Inc., (316) 838-7226

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Micropac Industries, Incorporated
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Intl **Denmark, Copenhagen**
E. V. Johanssen Electronik A-S, Tel: 45-1-839022
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Nabla Elektronikka Oy, Tel: 90-46 28 29
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Tekelec-Airtronic, Tel: (1) 027-75-35
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Intl **Korea, Seoul**
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ITT Semiconductors

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Consumer ..... ext. 247
Linear ..... ext. 233
Automotive ..... ext. 233
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Literature:
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All other information:
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ITT Far East & Pacic, Inc., Tel: 347-8817

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IPC/Diplomat, (201) 785-1830
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Freeport
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Sheridan Sales Co., (412) 244-1640
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SC **Greenville**
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Comptoir Commercial D'Importation
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Application engineering:
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Literature:
Jack Cutone .....ext. 220, 221, 222
Price and delivery:
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Follow-up an order:
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AR **Tempe**
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FL **Winter Park**
Young & Lawrence, (305) 647-6929
HA **Honolulu**
Aloha Associates, (808) 841-1575
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Intl **Austria, Vienna**
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Telecommunication LSI ..... Tam Nguyen
Application engineering ..... Tam Nguyen
Literature ..... Wendy Hartley
Place an order:
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Follow-up an order ..... Armand Poirer
All other information: ..... John Reeve

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Future Electronics, (604) 261-1335
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Melco Sales, Inc.
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Cameradio Electronics, (412) 288-2600
Pioneer/Pittsburgh, (412) 782-2300

SC **Greenville**
Hammond Electronics of Carolina, (803) 233-4121

National Semiconductor (cont)

TX **Austin**
Hall-Mark Electronics Corp., (512) 837-2814
Dallas
Hall-Mark Electronics Corp., (214) 231-6111
Hamilton/Avnet Electronics, (214) 661-8661
Sterling Electronics, (214) 357-9131
El Paso
Hall-Mark Electronics Corp., (915) 545-7163
Houston
Hall-Mark Electronics Corp., (713) 781-6100
Hamilton/Avnet Electronics, (713) 526-4661
Sterling Electronics, (713) 623-6600

UT **Salt Lake City**
Century Electronics, (801) 478-8551
Hamilton/Avnet Electronics, (801) 262-8451

WA **Bellevue**
Hamilton/Avnet Electronics, (206) 746-8750
Seattle
Almac/Stroum Electronics, (206) 763-8200
Liberty Electronics Northwest, (206) 763-8200

WI **Milwaukee**
Taylor Electric Company, (414) 241-4321

Can **Calgary, Alberta**
L. A. Varah, Ltd., (403) 276-8818
Dorval, Quebec
Semad Electronics, Ltd., (514) 636-4614
Downsview, Ontario
Semad Electronics, Ltd., (416) 635-9880
Edmonton, Alberta
Bowtek Electric Co., Ltd., (403) 426-1072
Mississauga, Ontario
Hamilton/Avnet Electronics, Ltd., (416) 677-7432
Prelco Electronics, Ltd., (416) 678-0401
Montreal, Quebec
Prelco Eectronics, Ltd., (514) 389-8051
Ottawa, Ontario
Hamilton/Avnet Electronics, (613) 725-3071
St. Laurent, Quebec
Hamilton/Avnet Electronics, Ltd., (514) 331-6443
Vancouver, B.C.
Bowtek Electric Co., Ltd., (604) 736-1141
L. A. Varah, Ltd., (604) 873-3211
Willowdale, Ontario
Electro Sonic, Inc., (416) 494-1666
Winnipeg, Manitoba
Bowtek Electric Co., Ltd., (204) 786-7521
L. A. Varah, Ltd., (204) 633-6190

NCR Corp.

NCR Corp.
Microelectronics Division
8181 Byers Road
Miamisburg, Ohio 45342
(513) 866-7471
Telex: 28-8010

All information:
Marketing Department
Specific product information:
Larry Hatt
Application engineering:
Vern Reinhardt
Literature:
Vern Reinhardt
Price and delivery:
Vern Reinhardt
Follow-up an order:
Vern Reinhardt
All other information:
Vern Reinhardt

NEC America

NEC America, Inc.
3070 Lawrence Expressway
Santa Clara, California 95051
(408) 738-2180
Telex: 357475

Product marketing manager:
Terry Trumbull

Sales Offices & Representatives

AL **Huntsville**
W. A. Brown Components, (205) 539-4411

AZ **Scottsdale**
Paul Carter Associates, (602) 947-4355

CA **Fullerton**
Electronic Component Mkt., (714) 879-9460
Redwood City
Heaton Company, Inc., (415) 367-9000
San Diego
Cerco, (714) 560-9143

CT **Wallingford**
Com-Sales, Inc., (203) 269-6252

FL **Altamonte Springs**
Dyne-A-Mark Corporation, (305) 831-2097
Clearwater
Dyne-A-Mark Corporation, (813) 441-4702
Ft. Lauderdale
Dyne-A-Mark Corporation, (305) 771-6501
Largo
Perrott Associates, (813) 585-3327

GA **Chamblee**
W. A. Brown Components, (404) 455-0405

IN **Ft. Wayne**
ACS-Fort Wayne, (219) 484-0722
Indianapolis
Advanced Components, (317) 545-6441

KS **Mission**
Admack Sales Co., (913) 432-5550

MA **Waltham**
Com-Sales, Inc., (617) 890-0011

MD **Baltimore**
C&D Sales, Inc., (301) 661-4306
Lutherville
C&D Sales, Inc., (301) 321-7891

MI **Southfield**
R. C. Nordstrom & Co., (313) 559-7373
St. Joseph
R. C. Nordstrom, (616) 429-7672

MN **Bloomington**
Thomas Marketing, (612) 888-5551

NC **Raleigh**
W. A. Brown Components, (919) 781-9426

NH **Londonderry**
Com-Sales, Inc., (603) 772-4586

NM **Albuquerque**
Rontek, (505) 299-4124

NY **Melville**
Comtronic Associates, (516) 249-0505
Rochester
Ontec, Inc., (716) 464-8636

OR **Portland**
Components West, Inc., (503) 643-5588

PA **Willow Grove**
Harry Nash Associates, (215) 657-2213

TN **Knoxville**
W. A. Brown Components, (615) 637-3523

TX **Dallas**
Merino Sales Company, (214) 233-6002

WA **Seattle**
Components West, Inc., (206) 243-2133

Can **Delta, B.C.**
Kaytronics, (604) 581-7611
Ontario
Kaytronics, (416) 638-5515
Quebec
Kaytronics, (514) 487-3434

Distributors

AZ **Phoenix**
Kachina Electronics, (602) 269-6201

CA **San Diego**
Intermark Electronics, (714) 279-5200
Sunnyvale
Western Microtechnology Sales, (408) 737-1660

MA **West Newton**
A. W. Mayer Co., Inc., (617) 965-1111

MD **Baltimore**
ASI Electronics, (301) 265-5100

NJ **Hanover**
State Electronic Parts Corp., (201) 887-2550

NEC Microcomputer

NEC Microcomputer
5 Militia Drive
Lexington, MA 02173
(617) 862-6410
Telex: 92-3434

Sales Offices & Representatives

AL **Huntsville**
20th Century Marketing, Inc., (205) 772-9237

AZ **Scottsdale**
Summit Sales, (602) 994-4587

CA **Fullerton**
Electronic Component Marketing, (714) 879-9460
San Diego
Cerco, (714) 560-9143
Sunnyvale
Trident Associates, (408) 734-5900

CO **Denver**
D/Z Associates, Inc., (303) 534-3649

FL **Clearwater**
Perrott Associates, Inc., (813) 585-3327
Fort Lauderdale
Perrott Associates, Inc., (305) 792-2211
Orlando
Perrott Associates, Inc., (305) 275-1132

IL **Palatine**
Technology Sales, Inc., (312) 991-6600

MA **Burlington**
Contact Sales, Inc., (617) 273-1520

MD **Baltimore**
C & D Sales, Inc., (301) 661-4306

MI **Benton Harbor**
R. C. Nordstrome & Co., (616) 429-8560
Lathrup Village
R. C. Mordstrome & Co., (313) 559-7373

MN **Minneapolis**
Electronic Innovators, Inc., (612) 884-7471

MO **Grandview**
K-MAR Enigneering & Sales, (816) 763-5385

MS **Corinth**
20th Century Marketing, (601) 287-2493

NC **Raleigh**
Wolffs Sales Service Co., (919) 851-2800

NM **Albuquerque**
Tri-Tronix, (505) 265-8409

NY **Clay**
Tech-Mark Inc., (315) 699-2261
Endicott
Tech-Mark, Inc., (607) 748-7473
Great Neck
Trionic Associates, Inc., (516) 466-2300
Liverpoll
Tech-Mark, (315) 652-6229
Melville
Rome, (516) 249-0011

OH **Cleveland**
Imtech, Inc., (216) 862-3400
Dayton
Imtech, Inc., (513) 278-6507

PA **Willow Grove**
Harry Nash Associates, (215) 657-2213

TN **Greenville**
20th Century Marketing, (615) 628-4021

TX **Fort Worth**
W. Pat Fralia Co., (817) 640-9101 or 649-8981
Houston
W. Pat Fralia Co., (713) 772-1572

WA **Mercer Island**
Tri-Tronix, (206) 232-4993

Can **Dollard Des Ormeaux, Quebec**
R.F.Q. Limited, (514) 626-8324
Etobicoke, Ontario
R.F.Q. Limited, (416) 626-1445

Distributors

AZ **Phoenix**
Mirco Electronic Distributors, (602) 997-5961
Sterling Electronics, (602) 258-4531

CA **Costa Mesa**
Semicomp, Inc., (714) 549-8600; (213) 971-5253
Irvine
Semiconductor Speciaists, Inc., (714) 549-5215
Los Angeles
Sterling Electronics, (213) 767-5030
San Diego
Intermark Electronics, (714) 279-5200 or 543-9005
Sterling Eectronics, (714) 565-2441
Santa Ana
Intermark Electronics, (714) 540-1322
Sunnyvale
Diplomat/Westland, Inc., (408) 734-1900

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G. S. Marshall, (408) 731-1100
Intermark Electronics, (408) 738-1111
Western Microtechnology, (408) 737-1660

CO **Wheatridge**
Century Electronics, (303) 424-1985

CT **Norwalk**
Harvey Electronics, (203) 853-1515

FL **Clearwater**
Diplomat/Southland, Inc., (813) 443-4514

LL **Chicago**
Semiconductor Specialists, Inc., (312) 279-1000
Elk Grove
Diplomat/Lakeland, Inc., (312) 595-1000

IN **Indianapolis**
Semiconductor Specialists, Inc., (317) 243-8271

LA **New Orleans**
Sterling Electronics, (504) 926-9407

MA **Burlington**
Semiconductor Specialists, Inc., (617) 272-1610
Chicopee Falls
Diplomat/I.P.C. of Mass., (413) 592-9441
Lexington
Harvey Electronics, (617) 861-9200
Watertown
Sterling Electronics, (617) 926-9720

MD **Baltimore**
A.S.I. Electronics, (301) 265-5100
Columbia
Technico, Inc., (301) 461-2200

MI **Farmington**
Diplomat/Northland, Inc., (313) 477-3200
Semiconductor Specialists, Inc., (313) 478-2700
Kentwood
R.M. Electronics Company, (616) 531-9300
Madison Heights
R.M. Electronics Company, (313) 689-8300

MN **Minneapolis**
Diplomat Electro-Com Corp., (612) 788-8601
Semiconductor Specialists, Inc., (612) 854-8841

MO **Hazelwood**
Semiconductor Specialists, Inc., (314) 731-2400
Kansas City
Semiconductor Specialists, Inc., (816) 452-3900
St. Louis
Diplomat/St. Louis, Inc., (314) 645-8550

NC **Raleigh**
Resco/Raleigh, (919) 832-2077

NJ **Fairfield**
Harvey Electronics, (201) 277-1262
Mount Laurel
Diplomat/I.P.C. Corp., (609) 234-8080
Totowa
Diplomat/I.P.C. Corp., (201) 785-1830

NM Albuquerque
Century Electronics, (505) 292-2700
Sterling Electronics, (505) 345-6601

NY **Buffalo**
Summit Distributors, Inc., (716) 804-3450
Elmsford
Zeus Components, (914) 592-4120
Rochester
Summit Elec. of Rochester, Inc., (716) 442-3494
Woodbury
Diplomat Electronics, Inc., (516) 921-9373
Harvey Electronics, (516) 921-8700

OH **Dayton**
Semiconductor Specialists, (513) 278-9455

PA **Philadelphia**
Almo Electronics Corp., (215) 698-4000
Pittsburgh
Semiconductor Specialists, Inc., (412) 781-8120

TX **Dallas**
Semiconductor Specialists, Inc., (214) 358-5211
Sterling Electronics, (214) 357-9131
Houston
Sterling Electronics, (713) 623-6600

UT **Salt Lake City**
Century Electronics, (801) 972-6969
Diplomat/Alta-Land, Inc., (801) 486-7227

VA **Roanoke**
Technico, Inc., (703) 563-4975

WA **Bellevue**
Bell Industries, (206) 747-1515
Seattle
Sterling Electronics, (206) 762-9100

WI **Milwaukee**
Semiconductor Specialists, Inc., (414) 257-1330

Can **Malton, Ontario**
Semiconductor Specialists, Inc:. (416) 678-1444
Montreal, Quebec
Future Electronics Corp., (514) 735-5775
Ottawa, Ontario
Future Electronics Corp., (613) 232-7757
Réxdale, Ontario
Future Electronics Corp., (416) 677-7820

Nitron

Nitron
A Division of McDonnell Douglas Corporation
10420 Bubb Road
Cupertino, California 95014
(408) 255-7550
TWX: (910) 338-0222

Sales Offices & Representatives

CA **Glendale**
Orion Sales, (213) 240-3151
Los Gatos
R. W. Thompson Associates, Inc., (408) 358-2671
San Diego
Col-Rob Electronics, (714) 565-6814
Tustin
Orion Sales, (714) 832-9687

CO **Englewood**
Dynatech, (303) 773-2830

CT **Guilford**
R. H. Sturdy Co., (203) 453-5424

FL Indian Rocks Beach
Tech Rep Associates, (813) 595-2834

IL **Chicago**
Carlson Electronic Sales Co., (312) 956-8240
Nitron, (312) 693-6303

IN **Milwaukee**
Carlson Electronic Sales Co., (317) 253-5610

MA **Wellesley Hills**
R. H. Sturdy Co., (617) 235-2330

MD **Glen Burnie**
New Era Sales, (301) 768-6666

MI **Warren**
DEM Electronic Saes, (313) 575-9444

MN **Minneapolis**
S & R Component Sales, (612) 544-3022

NC **Raleigh**
Bob Dean, (919) 851-2065

NY **East Syracuse**
Nycom, (315) 437-8343
Jericho
Electro Rep, (516) 938-0540

OH **Chagrin Falls**
Midwest Marketing Assoc., (216) 247-6655
Dayton
Midwest Marketing Assoc., (513) 433-2511

OR **Portland**
C. K. Shanks & Assoc., (503) 292-5656

PA **Birchrunville**
Jadelectronic Assoc., (215) 647-5151

TX **Addison**
Robert R. Thomas Company, (214) 233-8235

VA **Falls Church**
Nitron, (703) 534-3300

WA **Seattle**
C. K. Shanks & Assoc., (206) 632-4290

WI **Milwaukee**
Carlson Electronic Sales Co., (414) 476-2790

UT **Salt Lake City**
Omega, Ltd., (801) 278-6920

Can **Dollard des Ormeaux, Quebec**
Munro Electronic Components, Ltd., (514) 626-6723
Mississauga, Ontario
Munro Electronic Components, Ltd., (416) 676-1042

Intl **Denmark, Lyngby**
Knud Kamuk A/S, Tel: 02-88 38 33

Intl **France, Sevres**
Tekelec Airtronic, Tel: 626 02 35

Intl **Italy, Milano**
Silverstar, Ltd., Tel: 4996

Intl **Japan, Tokyo**
Kyokuto Boeki Kaisha, Ltd., Tel: 244-3511

Intl **Netherlands, Breda**
Klaasing Electronics B.V., Tel: 01600-22555

Intl **Sweden, Upplands-Vasby**
Johan Lagercrantz KB, Tel: 0760/86120

Intl **Switzerland, Mutschellen**
W. Stolz AG, Tel: 057 5 46 55

Intl **United Kingdom, Oxfordshire**
Peter Gray Electronics, Ltd., Tel: Henley 6543

Intl **West Germany**
Hamburg
Infratron Ing., Tel: 040-81 75 78
Munchen
Infratron Ing., Tel: 089-52 41 81

Nortec Electronics

Nortec Electronics Corporation
3697 Tahoe Way
Santa Clara, California 95051
(408) 732-2204
Telex: 348359

Specific product information:
Paul Burneikis
Application engineering:
Cindy Dooley
Price and delivery:
Mike Ferrera
Place an order:
Mike Ferrera
Follow-up an order:
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Novonics

Novonics
602 Sciandro Drive
Greensburg, PA 15601
(412) 423-6633

Nucleonic Products Co.

Nucleonic Products Co.
6660 Variel Avenue
Canoga Park, California 91303
(213) 887-1010
TWX: (910) 494-1954

Specific product information .....ext. 214 or 203
Application engineering .....ext. 214 or 203
Literature .....ext. 214
Price and delivery .....ext. 214 or 203
Follow-up an order .....ext. 257
All other information .....ext. 214 or 203

Sales Offices & Representatives

AZ **Phoenix**
Chaparral-Dorton, (602) 263-0414

CA **Los Angeles**
De Angelo, Rotham & Co., Inc., (213) 398-6239
Redwood City
Logan Sales, (415) 369-6726
San Diego
Earl Associates, Inc., (714) 278-5441

CO **Denver**
B-5 Inc., (303) 426-0222

FL **Hollywood**
"C" Associates, (305) 922-5230

IL **Franklin Park**
Dekotech, Inc., (312) 455-5100

IN **Indianapolis**
Frank J. Campisano Co., (317) 247-8623

IA **Cedar Rapids**
J. R. Sales Engineering, Inc., (319) 303-2232

MA **Waltham**
Conti-Younger Assoc., Inc., (617) 890-4582

MD **Baltimore**
Component Sales, Inc., (301) 484-3647

MI **Bloomfield Hills**
ENCO Marketing, (313) 642-0203

MN **Minneapolis**
Quantum Sales Inc., (612) 831-8583

Nucleonic Products Co. (cont)

MO **Hazelwood**
Dy-Tronix, Inc., (314) 731-5799
MS **Meridian**
Herron Assoc., (601) 483-9306
NY **Buffalo**
Quality Components, Inc., (716) 839-4170
Hemstead
Kahgan Sales, (516) 538-2300
Larchmont
Hingston-Walsh, (914) 834-4423
Manlius
Quality Components, Inc., (315) 682-8885
NC **Raleigh**
Component Sales, Inc., (919) 782-8433
OH **Cincinnati**
Frank J. Campisano Co., (513) 662-1616
Cleveland
Frank J. Campisano Co., (216) 468-1515
OR **Portland**
Northwest Marketing Assoc., (503) 297-2581
PA **Narberth**
Jerry Bresson Associates, (215) 839-6770
TX **Dallas**
Ammon & Rizos, (214) 233-5591
Houston
Ammon & Rizos, (713) 781-6240
WA **Bellvue**
Northwest Marketing Assoc., (206) 455-5846

Optical Electronics Inc.

Optical Electronics Inc.
P.O. Box 11140
Tuscon, Arizona 85734
(602) 624-8358
TWX: (910) 952-1283

Panasonic

Panasonic
Matsushita Electric Corporation
Industrial Division
1 Panasonic Way
Secaucus, New Jersey 07094
(201) 348-7275

Specific product information:
IC's and Solid State Products Product Manager, Terry Kobayashi
Application engineering:
Chicago, Arthur Suyama ..... ext. (312) 455-3105
New Jersey, Terry Kobayashi ext. (201) 348-7275
Price and delivery:
See Local Representatives
Place an order:
See Local Representatives
Follow-up an order:
See Local Representatives

Sales Offices & Representatives

AL **Huntsville**
Rep, Inc., (205) 881-9270
AZ **Phoenix**
Shefler-Kahn Co., Inc., (602) 257-9015
CA **Newport Beach**
West, Inc., (714) 540-9040
San Jose
Allgood North, (408) 288-6731
CO **Englewood**
Shefler-Kahn Co., Inc., (303) 761-3668 & 761-2590
FL **Casselberry**
EIR, Inc., (305) 830-9600
Coral Springs
EIR, Inc., (305) 752-9227
Plantation
EIR, Inc., (305) 791-8243
GA **Tucker**
Rep Inc., (404) 938-4358
IA **Des Moines**
B.E.A.M.S., Inc., (515) 255-1148
IL **Chicago**
Brock & Cushman, (312) 622-4110
KS **Shawnee Mission**
B.E.A.M.S., Inc., (913) 631-0300
MA **Allston**
Vector Sales, (617) 787-2790
MD **Ellicott City**
Tom Davis Marketers, (301) 461-2209
MI **Detroit**
Nicon Assoc., (313) 341-7688
MN **Minneapolis**
Jos-Co/ Melius, (612) 861-3343
MO **St. Louis**
B.E.A.M.S., Inc., (314) 569-1060
NC **Winston-Salem**
Murcota Corp., (919) 722-9445
NJ **Painfield**
Meg Electronic Sales, (201) 757-4332, (212) 233-9059
NM **Albuquerque**
Shefler-Kahn Co., Inc., (505) 296-0740, (505) 296-0749
OH **Columbus**
Tom Mulligan & Assoc., (614) 457-2242
OR **Portland**
Electronic Sources, (503) 292-0634
PA **King of Prussia**
Monteiro Assoc., Inc., (215) 265-0634
TN **Jefferson City**
Rep Inc., (615) 475-4105
TX **Addison**
Dunbar Assoc., (214) 239-7151
UT **Salt Lake City**
Shefler-Kahn Co., Inc., (801) 484-4222
VA **Fairfax**
Tom Davis Marketers, (703) 591-7390
WA **Bellevue**
Electronic Sources, (206) 453-0800
Can **Dollard Des Ormeaux, Quebec**
R.F.Q., Ltd., (514) 626-8324
Etabicoke, Ontario
R.F.Q., Ltd., (416) 626-1445

Distributors

AL **Huntsville**
Resistacap, (205) 881-9270
CA **Los Angeles**
Western Electromotive/Shephard, (213) 820-3777
CO **Denver**
Ratel Electronic, (303) 934-5813
FL **Dania**
Arco Distributors, (305) 925-1999
West Palm Beach
Nurmi Industrial Division, (305) 684-0320
MN **Thief River Falls**
Digi-Key Corp., (218) 681-2550
NJ **Plainfield**
Mars Electronic, (201) 757-4332, (212) 233-9059
NY **Ontario Center**
Pace Electronic Products, (315) 524-2491
OR **Portland**
Almac/Stroum Elec., (503) 292-3534
PA **Levittown**
Indisco, (215) 785-6565
TX **Addison**
Computer Components Corp., (214) 239-7151
WA **Seattle**
Almac/Stroum Elec., (206) 763-2300

Philips

See listings under Signetics

Photo Therm

Photo Therm
110 Sewell Ave.
Trenton, N.J. 08610
(609) 396-1456

Plessey Semiconductors

Plessey Semiconductors
1641 Kaiser
Irvine, CA 92714
(714) 540-9979
TWX: 595-1930

Applications engineering:
Walt Boris ..... ext. 33
Literature:
Maureen Greenwood ..... ext. 36
Price and delivery:
Ann Gilmore ..... ext. 31
Follow-up an order:
Ann Gilmore ..... ext. 31

Sales Offices & Representatives

AL **Huntsville**
REMCO, (205) 883-9260
AZ **Phoenix**
Eltron, (602) 997-1042
The Thorson Company, (602) 956-5300
CA **Goleta**
The Thorson Comany, (805) 964-8751
La Jolla
Littlefield & Smith Associates, (714) 455-0055
Marina del Rey
Relcom, (213) 822-1187
Mountain View
Thresum Associates, Inc., (415) 965-9180
CO **Denver**
Thorson/Denver, (303) 759-0809
CT **Milford**
Wayland Engineering Sales/Conn., (203) 878-3755
FL **St. Petersburg**
Kirkwood Associates, (813) 894-8240
IL **Elk Grove Village**
R-Tech, (312) 439-9090
KS **Prairie Village**
Engineering Services Co., (913) 649-4000
MA **Natick**
Wayland Engineering Sales, (617) 655-6080
MD **Ellicott City**
Applied Engineering Consultants, (301) 465-1272
MI **Southfield**
Luebbe Sales Company, (313) 357-0355
MO **St. Louis**
Engineering Services Co., (314) 997-1515
NC **Raleigh**
Remco, (919) 828-3009
NM **Eden Prairie**
Technical Associates Inc., (612) 944-3034
NY **Plainview**
Robert Smith Associates, (516) 681-3155
Skaneateles
Robtron, Inc., (315) 685-5731
Spring Valley
Robert Smith, (914) 354-6067
OH **Cincinnati**
Luebbe Saes Company, (513) 871-4211
Cleveland
Luebbe Sales Company, (216) 333-0425
Dayton
Luebbe Sales Company, (513) 294-0426
PA **Huntingdon Valley**
Dick Knowles Associates, (215) 947-5641
TX **Fort Worth**
W. Pat Fralia Company, Inc., (817) 640-9101
Houston
W. Pat Fralia Company, Inc., (713) 772-1572
Richardson
W. Pat Fralia Company, Inc.
VA **Arlington**
Applied Engineering Consultants, (703) 524-6630
Woodbridge
Applied Engineering Consultants, (703) 550-9429
WA **Olympia**
Bergford & Associates, (206) 866-2001
Can **Islington, Ontario**
MacKay Associates, (416) 626-3805

Distributors

CA **Culver City**
JSH Electronics, Inc., (213) 559-5780
San Diego
Intermark, (714) 453-9005
Sunnyvale
Semicomp Corp., (408) 736-2330
IL **Chicago**
Semiconductor Specialists, (312) 279-1000
MD **Ellicott City**
Applied Engineering Consultants, (301) 465-1272
NY **Plainview**
Plainview Electronics Supply Corp., (516) 822-5357
TX **Arlington**
Patco Supply, (817) 649-8981

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Precision Monolithics

Precision Monolithics Inc.
1500 Space Park Dr.
Santa Clara, CA 95050
(408) 246-9222

Specific product information ..... ext. 162
Application engineering ..... ext. 162
Literature ..... ext. 162
Price and delivery ..... ext. 171
Follow-up an order ..... ext. 171
All other information ..... ext. 162

Sales Offices & Representatives

AL **Huntsville**
W. A. Brown Components, (205) 539-4411
AZ **Tempe**
Argus Sales, (602) 967-8709
CA **Los Angeles**
Regional Office, (213) 670-3791
Mountain View
Thresum Associates, (415) 965-9180
San Diego
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RCA, Ltd., (403) 243-6051
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Turkelek Elektronik Ltd., Tel: 18 94 83
Intl **United Kingdom, Bucks, England**
Memec, Ltd., Tel: (029) 664) 366 & 7 & 8
Harlow, Essex, England
Distronic, Ltd., Tel: 32947/39701
Surrey, England
Consort Electronics, Ltd., Tel: (0252) 871717
Intl **Venezuela, Caracas**
Arelinea, Tel: 71.05.29

Distributors

AL **Huntsville**
Hallmark Electronics, (205) 837-8700
AZ **Phoenix**
Micro Electronics, (602) 944-2281
Weatherford Co., (602) 727-7144
CA **Anaheim**
R. V. Weatherford Co., (714) 547-0891
Aurora
Jet Eectronics Co., Inc., (303) 364-1000
Gardena
Bell Industries, (213) 321-5802
Glendale
R. V. Weatherford Co., (213) 849-3451
Newport
Semicomp Corporation, (714) 833-3070
Palo Alto
R. V. Weatherford Co., (415) 493-5373
Pomona
R. V. Weatherford Co., (714) 623-1261
San Diego
Intermark Electronics, (714) 279-5200
R. V. Weatherford Co., (714) 278-7400
Santa Ana
Intermark Electronics, (714) 540-1322
Sunnyvale
Bell Industries, (408) 734-8570
Intermark Electronics, (408) 738-1111
Woodland Hills
Semiconductor Concepts, (213) 884-4560
CO **Aurora**
Jet Eectronics Supply Co., (303) 364-1000
Englewood
R. V. Weatherford Co., (303) 761-5432
Wheat Ridge
Century Electronics, (303) 424-1985
FL **Ft. Lauderdale**
Hallmark Electronics, (305) 971-9280
Orlando
Hallmark Electronics, (305) 855-4020
Miami
All American, (305) 754-5531
GA **Lawrenceville**
Hall-Mark Electronic Corp., (800) 633-2918
HI **Honolulu**
Victor Kim Electronic, (808) 533-7132
IL **Elk Grove Village**
Hallmark Electronics, (312) 437-8801
Patatine
OHM/Electronics, (312) 359-5500
IN **Fort Wayne**
Fort Wayne Electronics Supply, (219) 423-3422
KS **Lenexa**
Hall-Mark Electronics Corp., (913) 888-4747
LA **Schreveport**
Industrial Electronic Supply, (318) 636-7100
MA **Dedham**
Gerber Electronics, (617) 329-2400
MD **Baltimore**
Hall-Mark Electronics Corp., (301) 796-9300
Columbia
Technico, (301) 461-2200
MI **Grand Rapids**
R. M. Electronics, (616) 531-9300
Livonia
Reptron Electronic, (313) 525-2700
MN **Minneapolis**
The Joel Company, (612) 545-5669
Industrial Components, (612) 831-2666
Blumington
Hall-Mark Electronic Corp., (612) 884-9056
MO **Earth City**
Hall-Mark Electronic Corp., (314) 291-5350
NC **Raleigh**
Hall-Mark Electronic Corp., (919) 832-4465
Winstom-Salem
Kirkman Electronics., (919) 722-9131
NM **Albuquerque**
R. V. Weatherford Co., (505) 842-0868
NY **North Bellmore**
Hygrade Electronics, (516) 785-6200
Buffalo
Summit Distributors, (716) 884-3450
Elmsford
Zeus Components, (914) 592-4120
Farmingdale
Harrison Electronics, (516) 293-7990
Hauppage
Jaco Electronics, Inc., (516) 273-1234
New York
Calvert Electronics, (212) 481-5300
Rochester
Rochester Radio Supply, (716) 454-7800
Rome
Rome Electronics, (315) 337-5400
Woodbury
Diplomat Eectronics, (516) 921-9373
Yorktown Heights
Kenric Electric Corp., (914) 962-5539
OH **Columbus**
Reptron/Ohio, (614) 443-0231
Dayton
Arrow Electronics, (513) 253-9176
ESCO, (513) 226-1133
Hallmark Electronic Corp., (513) 294-0437
Koehike, (513) 293-2122
OK **Tulsa**
Component Spec., Inc., (918) 664-2820
Hall-Mark Electronic Corp., (918) 835-8458
PA **Huntingdon Valley**
Hallmark Electronics, (215) 355-7300
Philadelphia
Herbach & Rademan, (215) 426-1700
TN **Kingsport**
Radio Electronics Supply Co., (515) 247-8111
TX **Austin**
Hall-Mark Electronic Corp., (512) 837-2814
Dallas
Component Specialties, (214) 357-6511
Hall-Mark Electronic Corp., (214) 231-6111
R. V. Weatherford Co., (214) 243-1571
Houston
Component Spec., Inc., (713) 771-7237
Hall-Mark Electronic Corp., (713) 781-6100
Harrison Equipment Co., (713) 652-4750
R. V. Weatherford Co., (713) 688-7406
UT **Salt Lake City**
Century Electronics, (801) 487-8551
Diplomat-Alta, (801) 486-7227
WA **Bellevue**
Bell Industries, (206) 747-1515
Seattle
R. V. Weatherford Co., (206) 243-6340
WI **Milwaukee**
Marsh Electronics, Inc., (414) 476-6000
West Allis
Hall-Mark Electronic Corp., (414) 476-1270
Can **Scarborough, Ontario**
Intl. Rectifier C. Ltd., (416) 755-7793
Dorval, Quebec
Intl. Rectifier C. Ltd., (514) 631-4696

Sprague Electric Company

Sprague Electric Company
Semiconductor Division
115 Northeast Cutoff
Worcester, Massachusetts 01606
(617) 853-5000
Telex: 920467

Specific product information:
Automotive ..... B. Marshall
Consumer ..... R. Milewski
Camera ..... B. Marshall
Digital ..... G. Tully
Transistor Arrays ..... G. Tully
Operational Amplifiers ..... G. Tully
Display Driver ..... P. Emerald
MOS ..... G. Tufly

Application engineering:
Same as above

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Sprague Electric Company (cont)

Literature:
647 Marshall Street, North Adams, Massachusetts 01247, (413) 664-4411 ..... ext. 2572
Price and delivery:
Same as product information:
Place an order:
Same as above
Follow-up an order:
Same as above

Sales Offices & Representatives

Contact these offices for names of distributors

AL Huntsville
Sprague Electric Company, (205) 883-0520
AZ **Phoenix**
Stitzer-Dodd, (602) 944-2237
Tempe
Sprague Electric Company, (602) 279-5435
CA **Burlingame**
William J. Purdy Company, (415) 347-7701
Inglewood
Sprague Eectric Company, (213) 649-2600
Sacramento
William J. Purdy Company, (916) 422-0128
San Diego
KCÉ Corp., (714) 278-7640
CO **Denver**
William J. Purdy Company, (303) 777-1411
CT **Trumbull**
Sprague Electric Company, (203) 261-2551
DC **Washington**
Sprague Electric Company, (Gov't sales only) (202) 244-6006
FL **Ft. Lauderdale**
UniRep, Inc., (305) 527-1556
Longwood
Sprague Electric Company, (305) 831-3636
HI **Honolulu**
Hawaii Electrónic Sales, (808) 845-8207
IL **Chicago**
D. Dolin Sales Company, (312) 286-6200
Schiller Park
Sprague Electric Company, (312) 678-2262
IN **Indianapolis**
Sprague Electric Company, (317) 253-4247
Mulberry
Maish Sales, (317) 638-8484 (For Indianapolis)
Maish Sales, (317) 296-2322 (For Mulberry Area)
MA **North Adams**
Sprague Electric Company, (413) 664-4411
Sprague Products Company, (413) 664-4481
Norwood
Ray Perron & Company, (617) 762-8114
Waltham
Sprague Eectric Company, (617) 899-9100
Sprague Products Company, (617) 899-9840
MI **Jackson**
Sprague Electric Company, (517) 787-3934
MN **Minneapolis**
HMR, Inc., (612) 920-8200
MO **Kansas City**
Nevco, (816) 421-1751
St. Louis
Nevco, (314) 843-7406
Sprague Electric Company, (314) 781-2420
NC **Winston Salem**
Electronic Marketing Assoc., (919) 722-5151
NJ **Cherry Hill**
Sprague Electric Company, (609) 795-2299
Trinkle Sales Inc., (609) 795-4200
Wayne
Sprague Electric Company, (201) 696-8200
NM **Albuquerque**
William J. Purdy Company, (505) 266-7959
NY **Mamaroneck**
William Rutt, (914) 698-8600
Melville
Sprague Electric Company, (516) 549-4141
Syracuse
Mar-Com Assoc., (315) 437-2843
Paston-Hunter Company, (315) 437-2992
Sprague Electric Company, (315) 437-7311
OH **Beachwood**
Electronic Salesmasters, Inc., (216) 831-9555
Dayton
Sprague Electric Company, (513) 278-0781
PA **Philadelphia**
Trinkle Sales, (215) 922-2080
SC **Greenville**
Electronic Marketing Assoc., (803) 268-1125
TX **Dallas**
Lund & Company, (214) 387-4634
Richardson
Sprague Electric Company, (214) 235-1256
VA **Lexington**
Sprague Electric Company, (703) 463-9161
WA **Seattle**
Fleehart & Sullivan, (206) 522-1533
Sprague Electric Company, (206) 632-7761
Can **Montreal, P.Q.**
Sprague Eectric of Canada, (514) 747-7811
Toronto, Ontario
Sprague Electric of Canada, (416) 766-6123
Intl **Belgium, Ronse (Renaix)**
Sprague-Benelux, Tel: 215-351 (055)
Intl **England, Yiewsley**
Sprague Electric (U.K.) Ltd., Tel: 44627
Intl **France, Bagneux**
Sprague France S.A.R.L., Tel: 1-655 19 19
Intl **Germany, Frankfurt**
Sprague GmbH, Tel: 0611-439407
Intl **Hong Kong**
Sprague World Trade Crp., Tel: 5-626231-4
Intl **Italy**
Milan
Sprague-Italiana, S.p.A., Tel: 02 47 91 21
Rome
Sprague-Italiana, S.p.A., Tel: 06 83 33 69
Intl **Switzerland, Geneva**
Sprague World Trade Corp., Tel: 98 4021
Intl **Taiwan, Taipei**
Sprague Taiwan Corp., Tel: 7310748

Standard Microsystems

Standard Microsystems Corporation
35 Marcus Boulevard
Hauppauge, New York 11787
(516) 273-3100
TWX: (510) 227-8898

Specific Product Information:
Applications Eng.
Application Engineering:
Applications Eng.
Literature:
Literature
Price and Delivery:
Sales
Follow up an order:
Order Entry
All other information:
Sales

Sales Offices & Representatives

AL **Huntsville**
EMA, (205) 533-6640
AZ **Scottsdale**
Dar-C, Inc., (602) 948-2240
CA **Culver City**
DeAngelo, Rothman & Co., (213) 398-6239
Irvine
Turk Enterprises, (714) 955-1575
Palo Alto
NOR-CAL Associates, (415) 961-8121
San Diego
DeAngelo, Rothmen & Co., (714) 560-5707
CO **Denver**
Z/D Associates, Inc., (303) 534-3649
FL **Hollywood**
"C" Associates, (305) 922-5230/8917
IL **Skokie**
Mar-Con, (312) 675-6450
MA **Burlington**
Contact Sales, Inc., (617) 273-1520
MD **Baltimore**
Burgin-Kreh Assoc., (301) 788-5200
MI **Plymouth**
A.P.J. Assoc., Inc., (313) 459-1200
MN **New Brighton**
TWC, (612) 636-1770
MO **Florissant**
S.A.I. Marketing, (314) 837-5200
NC **Winston-Salem**
Burgin-Kreh Assoc., (919) 768-4174
NJ **Keasbey**
Addem, (516) 549-8400
NY **Hauppauge**
Eastern Area Sales Office, (516) 273-3100
Melville
Addem, (516) 549-8400
OH **Cincinnati**
G & H Sales Co., (513) 771-8231
Grove City
G & H Sales Co., (614) 878-1128
PA **Hatboro**
QED Electronics, Inc., (215) 674-9600
TX **Dallas**
Kruvand Assoc., Inc., (214) 691-4592
Houston
Kruvand Assoc., Inc., (713) 780-9710
VA **Lynchburg**
Burgin-Kreh Assoc., (804) 845-5600
WA **Bellevue**
SDR² Products & Sales Co., (206) 747-9424
Can **Etobicoke, Ontario**
R.F.Q., Ltd., (416) 626-1445
Dollard Des Ormeaux, Quebec
R.F.Q., Ltd., (514) 626-8324
Intl **Australia, Prospect**
A. J. Ferguson Pty., Ltd., Tel: 516 895
Intl **Austria, Vienna**
Bacher Eektronische, Tel: (222) 837152
Intl **Finland, Helsinki**
Havulinna Oy, Tel: (90) 661-451
Intl **France, Serves**
Tekelec Airtronic, Tel: 027-7535
Intl **Great Britain, Hammersmith, London**
Rastra Electronics, Ltd., Tel: (1) 7483143
Intl **Japan, Tokyo**
Teijin Advanced, Tel: (506) 4670-6
Intl **Netherlands, Breda**
Famatra Benelux, Tel: (76) 133457
Intl **Norway, Oslo**
EGA A/S, Tel: (2) 221900
Intl **Switzerland, Zurich**
Dimos AG, Tel: (51) 626140
Intl **West Germany, Munich**
Atlantik Elektronik GmbH, Tel: (89) 7853112

Distributors

AZ **Phoenix**
Kachina Electronic Dist., (602) 269-6201
CA **Culver City**
NESCO, (213) 391-6294
San Dimas
Zeus/West, Inc., (714) 990-1911
Sunnyvale
Diplomat/Westland, Inc., (408) 734-1900
CO **Wheatridge**
Century Eectronics, (303) 424-1985
FL **Clearwater**
Diplomat/Southland, Inc., (813) 443-4514
Pompano Beach
Zeus/ Components Florida, (305) 942-4312
IL **Elk Grove Village**
Diplomat/Lakeland, Inc., (312) 595-1000
Skokie
Mar-Con Sales, (312) 675-6450
IN **Indianapolis**
Sheridan Sales Co., (317) 297-3146
MA **Burington**
RC Components, (617) 273-1860
Zeus/New Engand, Inc., (617) 273-0750
Chicopee
Diplomat/I.P.C. of MA., (415) 592-9441
Holliston
Diplomat/New England, Inc., (617) 429-4120
Waltham
QPL, (617) 891-0460
MD **Baltimore**
Blanco, (301) 788-4200
MI **Farmington**
Diplomat/Northland, Inc., (313) 477-3200
Sheridan Sales Co., (313) 477-3800
Grand Rapids
Sheridan Sales Co., (616) 942-2504
MN **Minneapolis**
Cassidy Electronics, (612) 835-7746
Diplomat/Electro-Comm Corp., (612) 788-8601
MO **Florissant**
Sheridan Sales Co., (314) 837-5200
St. Louis
Diplomat/St. Louis, Inc., (314) 645-8550

Standard Microsystems (cont)

NJ **Mt. Laurel**
Diplomat/I.P.C., (201) 234-8080
Totowa
Diplomat/I.P.C., (201) 785-1830
NM **Albuquerque**
Century Electronics, (505) 292-2700
NY **Elmsford**
Zeus Components, Inc., (914) 592-4120
Farmingdale
Norelcom Electronics, (516) 249-7262
Woodbury
Diplomat Electronics Corp., (516) 921-9373
OH **Beachwood**
Sheridan Sales Co., (216) 831-0130
Cincinnati
Sheridan Sales Co., (800) 543-4695, (513) 761-5432
Dayton
Sheridan Sales Co., (513) 223-3332
PA **Hatboro**
QED Electronics, Inc., (215) 674-9600
Pittsburgh
Sheridan Sales Co., (412) 244-1640
TX **Austin**
Quality Components, Inc., (512) 458-4181
Dallas
Quality Components, Inc., (214) 387-4949
Houston
Quality Components, Inc., (713) 772-7100
UT **Salt Lake City**
Century Electronics, (801) 487-8551
Diplomat/Aita-Land, Inc., (801) 486-4134
Can **Montreal**
Future Electronics, (514) 735-5775
Ontario
Westburne, (416) 635-2950
Intl **Australia, Prospect**
A. J. Ferguson, Pty., Ltd., Tel: 514 895
Intl **Austria, Vienna**
Bacher Elektronische, Tel: (222) 837152
Intl **France, Serves**
Tekelec Airtronic, Tel: 027-75-35
Intl **Great Britain, London**
Rastra Electronics, Ltd., Tel: (1) 7483143
Intl **Japan, Tokyo**
Teijin Advanced Prod. Corp., Tel: (506) 4670-6
Intl **Netherlands, Breda**
Famatra Benelux, Tel: 133457
Intl **Norway, Oslo**
EGA A/S, Tel: (2) 221900
Intl **Switzerland, Zurich**
Dimos AG, Tel: (51) 626140
Intl **West Germany, Munich**
Atlantik Elektronik GmbH, Tel: (89) 7853112

Stewart Warner Microcircuits

Stewart-Warner Microcircuits
730 East Evelyn Avenue
Sunnyvale, California 94086
(408) 245-9200
TWX: (910) 339-9210

Synertek

Synertek
3050 Coranado Drive
Santa Clara, California 95051
(408) 241-4300

Specific Product Information:
Product Marketing ..... ext. 222
Application Engineering:
Conrad Boisvert ..... ext. 320
Literature:
Janet Huggins ..... ext. 327
Price and Delivery:
Product Marketing ..... ext. 222
Follow up an order:
Customer Service ..... ext. 284, 238

Sales Offices & Representatives

AL **Huntsville**
Macro Marketing, (205) 883-9630
AZ **Phoenix**
MR Engineering Sales Co., (602) 959-5150
CA **Newport Beach**
Babco Associates, Inc., (714) 751-8375
Palo Alto
Nor-Cal Associates, (415) 961-8121
San Diego
Littlefield & Smith Assoc., (714) 455-0055
CO **Englewood**
Checkmate Sales, Inc., (303) 773-0666
CT **Weston**
Representatives, Inc., (203) 239-2507
FL **Altamonte Springs**
Dyne-A-Mark Corp., (305) 831-2097
Clearwater
Dyne-A-Mark Corp., (813) 441-4702, 3
Ft. Lauderdale
Dyne-A-Mark Corp., (305) 771-6501, 2, 3
Maitland
Dyne-A-Mark Corp., (305) 831-2097
IA **Cedar Rapids**
Comstrand, Inc., (319) 377-1575
IL **Elk Grove Village**
Carlson Electronic Sales Co., (312) 956-8240
IN **Ft. Wayne**
J & B Engineering Sales Co., (219) 483-2813
MA **Waltham**
Dynasel Assoc., (617) 890-6777
MD **Baltimore**
Conroy Sales, (301) 296-2444
MI **Farmington**
Miltmore Sales, Inc., (312) 476-2446
MN **Minneapolis**
Comstrand, Inc., (612) 571-0000
NJ **Haddonfield**
Sunday O'Brien, (609) 429-4013
NY **Camillus**
Ontec, Inc., (716) 464-8636
Fayetteville
Ontec, Inc., (716) 464-8636
Grand Island
Ontec, Inc., (716) 464-8636
Melville, L.I.
Comtronic Assoc., Inc., (516) 249-0505
Rochester
Ontec, Inc., (716) 464-8636
OH **Brunswick**
Kimconics, (216) 225-6111
Dayton
Kimconics, (513) 898-1783
PA **Waterford**
Kimconics, (412) 367-3013
TX **Houston**
Semiconductor Sales, (713) 661-0681
Richardson
Semiconductor Sales, (214) 231-6181
WA **Tukwila**
General Electronics, (206) 575-4030
Vancouver
Sales Office, (206) 575-4030

Distributors

AZ **Phoenix**
Kierulff Eectronics, (602) 243-4101
CA **Costa Mesa**
Semicomp Corp., (714) 549-8600
Los Angeles
Kierulff Electronics, (213) 685-5511
Palo Alto
Kierulff Electronics, (415) 968-6292
San Diego
Intermark Electronics, (714) 453-9005
Kierulff Electronics, (714) 278-2112
Santa Ana
Intermark Electronics, (714) 540-1322
Sunnyvale
Intermark Electronics, (408) 738-1111
Semicomp Corp., (408) 736-2330
CO **Denver**
Kierulff Electronics, (303) 371-6500
FL **Pompano**
Zeus Components, (305) 942-4312
IA **Cedar Rapids**
Advent Electronics, (319) 363-0221
IL **Elk Grove Village**
Kierulff Electronics, (312) 640-0200
Rosemount
Advent Electronics, (312) 297-6200
IN **Indianapolis**
Advent Electronics, (317) 297-4910
Sheridan Sales Company, (327) 297-3146/3147
MA **Billerica**
Kierulff Electronics, (617) 667-8331
Newton
Greene-Shaw Co., Inc., (617) 969-8900
MD **Columbia**
Technico, Inc., (301) 461-2200
Gaithersburg
Kierulff Eectronics, (301) 948-0250
MI **Farmington**
Advent Electronics, (313) 477-1650
Sheridan Sales Co., (313) 477-3800
MN **Minneapolis**
Dawn Electronics, Inc., (612) 546-2215
MO **Florissant**
Sheridan Sales Co., (314) 837-5200
NJ **Camden**
General Radio & Suppy, (609) 964-8560
Ruthersford
Kierulff Electronics, (201) 935-2120
NM **Albuquerque**
Alliance Electronics, Inc., (505) 292-3360
NY **Elmsford**
Zeus Components, (914) 592-4120
Hicksville
Kierulff Electronics, (516) 433-5530
OH **Beachwood**
Sheridan Sales Co., (216) 831-0132
Dayton
Sheridan Sales Co., (513) 223-3332
Reading
Sheridan Sales Co., (513) 761-5432
PA **Pittsburgh**
Sheridan Sales Co., (412) 244-1640
TX **Austin**
Quality Components, Inc., (512) 458-4181
Dallas
Quality Components, Inc., (214) 387-4949
Houston
Quality Components, Inc., (713) 772-7100
UT **Salt Lake City**
Cairon Electric, (801) 487-7451
WA **Tukwila**
Kierulff Eectronics, (206) 575-4420
WI **Milwaukee**
Taylor Electric Co., (414) 241-4321
Can **Montreal, Quebec**
Future Electronics, (514) 735-5775

Tektronix

Tektronix, Incorporated
P.O. Box 500
Beaverton, Oregon 97077
(503) 644-0161
TWX: 910-467-8708

Sales Offices & Representatives

AL **Huntsville**
Field Engineering Office, (205) 881-2912
AZ **Phoenix**
Field Engineering Office, (602) 244-9795
CA **Concord**
Field Engineering Office, (415) 689-2710
Irvine
Field Engineering Office, (714) 556-8080/89, (213) 778-5225/6
Los Angeles
Field Engineering Office, (213) 999-1711
Los Gatos
Field Engineering Office, (408) 358-3491
San Diego
Field Engineering Office, (714) 292-7330
Santa Clara
Field Engineering Office, (408) 249-5500
CO **Denver**
Fied Engineering Office, (303) 773-1011
CT **Milford**
Field Engineering Office, (203) 877-1494
FL **Fort Lauderdale**
Field Engineering Office, (305) 731-1220
Orlando
Field Engineering Office, (305) 894-3911
Pensacola
Field Engineering Office, (904) 476-1897
GA **Norcross**
Field Engineering Office, (404) 449-4770
HI **Honolulu**
Field Engineering Office, (808) 845-4531
Honolulu Service Center, (808) 847-1138
IL **Chicago**
Field Engineering Office, (312) 259-7580

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Tektronix (cont)

IN **Indianapolis**
Field Engineering Office, (317) 545-2351
KS **Kansas City**
Field Engineering Office, (913) 341-3344
LA **New Orleans**
Field Engineering Office, (504) 837-8454
MA **Boston**
Field Engineering Office, (617) 861-6800
MD **Baltimore**
Fied Engineering Office, (301) 321-7000
Rockville
Field Office/Service Center, (301) 948-7151
MI **Detroit**
Field Engineering Office, (313) 478-5200
MN **St. Paul**
Field Engineering Office, (612) 484-8571
MO **St. Louis**
Field Enginering Office, (314) 731-4696
NC **Raleigh**
Field Engineering Office, (919) 782-5624
NJ **Springfield**
Field Engineering Office, (201) 379-1670
NM **Albuquerque**
Field Engineering Office, (505) 265-5541
NY **Albany**
Field Engineering Office, (518) 785-3353
Long Island
Field Engineering Office, (516) 364-9069, (212) 895-9215
Poughkeepsie
Field Engineering Office, (914) 454-7540
Rochester
Field Engineering Office, (716) 244-2600
Syracuse
Field Engineering Office, (315) 455-6661
OH **Cleveland**
Field Engineering Office, (216) 884-6558
Dayton
Field Engineering Office, (513) 859-3681
OK **Oklahoma City**
Field Engineering Office, (405) 848-3361
OR **Portland**
Field Engineering Office, (503) 620-9100
PA **Philadelphia**
Field Engineering Office, (215) 825-6400
Pittsburgh
Field Engineering Office, (412) 373-3250
TX **Dallas**
Field Engineering Office, (214) 233-7791
Houston
Field Engineering Office, (713) 783-1910
San Antonio
Field Engineering Office, (512) 434-4334
UT **Salt Lake City**
Field Engineering Office, (801) 484-8501
VA **Hampton**
Field Engineering Office, (804) 826-4020
WA **Seattle**
Fied Engineering Office, (206) 575-0180
Can **Calgary**
Tektronix Canada Ltd., (403) 269-3138
Edmonton
Tektronix Canada Ltd., (403) 434-9466
Halifax
Tektronix Canada Ltd., (902) 469-9476
Montreal
Tektronix Canada Ltd., (514) 697-5340
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Tektronix Canada Ltd., (614) 676-2728
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Tektronix Canada Ltd., (604) 438-4321
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Roma
Silverstar Spa, Ltd.
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Silverstar Spa, Ltd.
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Osaka-shi
Sony/Tektronix Corporation
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Intl **Kuwait, Safat**
TAREQ Company
Intl **Lebanon, Beirut**
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Mecomb Malaysia Sdn. Bhd.
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Mofat Engineering Co., Ltd.
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Paardeneiland
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Solna
Tektronix AB
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Tektronix International A.G.
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Intl **Taiwan, Taipei**
Heighten Trading Co., Ltd.
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El Eslek
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Coasin Uruguaya S.R.L.
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Intl **Zambia**
Lusaka
Baird and Tatlock (Zambia) Ltd.

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Teledyne Crystalonics

Teledyne Crystalonics
147 Sherman Street
Cambridge, Massachusetts 02140
(617) 491-1670

Specific Product Information:
Richard Antalik
Application Engineering:
Richard Antalik
Literature:
Susan McTighe
Price and Delivery:
W. J. Kilgarriff
Follow up an order:
W. J. Kilgarriff
All other information:
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Comp-Tech Sales, (201) 935-5454
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Comp-Tech Sales, (516) 593-2623
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James Semple Assoc., (716) 544-8583
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Dayton
KW Elect. Sales, (513) 890-2150
PA **Allison Park**
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Bala Cynwyd
Vantage Sales, (215) 667-0990
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E. M. A., Inc., (803) 268-1125
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Southland Comp., (214) 233-0603
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SD-R², (206) 9424
Doryal, Quebec
Vitel Electronics, (514) 331-7393
Intl **Austria**
Kinsington, London
G.E. Electronics, Tel: 01-7270711/3 & 5008
Intl **France, Paris**
Composants et Produits Electroniques, Tel: 968-70-08
Intl **Germany, Heilbronn**
Sinus Electronics, Tel: 07131-82904
Intl **Israel, Tel-Aviv**
STG International, Tel: 53459
Intl **Italy, Milano**
Kimates, Tel: 02-8562
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MCA Tronix, Tel: 70/548890
Intl **Spain, Barcelona**
Sisteco, Tel: 70/548890
Intl **Sweden, Wallingby**
Svensk Tele Industri AB, Tel: 890435
Intl **Switzerland, Zurich**
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Intl **United Kingdom**
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Century Elect., (910) 938-0393
FL **Clearwater**
Southland Elect., (813) 443-4515
Deerfield
American Elect., (305) 428-0262
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Bodelle Co., (312) 323-9670
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R&D Elect., (617) 861-9200
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Technico, (301) 461-2200
Savage
Pyttronics, (301) 792-7000
MI **Livonia**
Reptron, (313) 525-2700
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Tory Sales, (201) 935-3531
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Zeus Components, (914) 592-4120
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Freeport Elect., (516) 546-6000
Hauppauge
Components Plus, (516) 231-9200
Utica
O'Tronics, (315) 732-4118
Woodbury
Diplomat Elect., (516) 921-9373
OH **Englewood**
Argent Ind., (513) 836-8633
TX **Austin**
Quality Components, (512) 458-4181
Dallas
Solid State, (214) 352-2601
Quality Components, (214) 387-4949
Houston
Quality Components, (713) 772-7100
UT **Salt Lake City**
Century Elect., (801) 487-8551
Intl **Austria**
Kinsington, London
G. E. Electronics, Tel: 01-7270711/3 & 5008
Intl **France, Paris**
Composants et Produits Electroniques, Tel: 968-70-08
Intl **Germany, Heilbronn**
Sinus Electronics, Tel: 07131-82904
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Intl **Spain, Barcelona**
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Teledyne Philbrick

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Application engineering:
Sales Department
Literature:
Publications Dept.
Price and delivery:
Sales Department
Follow-up an order:
Customer Service Dept.
All other information:
Product Sales Dept.

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T. Louis Snitzer Co., (213) 836-6170
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Tekdata, (203) 693-0710
CO **Denver**
PLS Associates, (303) 773-1218
FL **Largo**
Col-Ins-Co., (800) 432-4480
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Col-Ins-Co., (305) 423-7615
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BC Electronic Sales, Inc., (913) 888-6680
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Elmeasco Instruments Pty., Ltd., Tel: 233-4044
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Neltronic (N.I.) Ltd., Tel: Larne 5321
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Hispano Electronica s.a., Tel: 259 04 22, 259 04 23
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Teledyne Semiconductor

Teledyne Semiconductor
1300 Terra Bella Avenue
Mountain View, California 94043
(415) 968-9241
TWX: (910) 379-6494

Specific product information:
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Application engineering:
..... ext. 241
Literature:
..... ext. 305
Price and delivery:
..... ext. 378
..... ext. 378
Follow-up an order:
..... ext. 441/442
All other information:
..... ext. 378

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Vitel Electronics, (514) 331-7393
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Vitel Electronics, (416) 622-6300
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Teledyne Semiconductor, Tel: (44) 01-897-2503
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G.D.S. Sales Ltd., Tel: Slough
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Teledyne Semiconductor, Tel: 7741-5066

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Rosemont
Advent Eectronics, (312) 298-4210
Skokie
Bell Industries, (312) 965-7500
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KS **Wichita**
Radio Supply, (316) 267-5213
MD **Columbia**
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Gaithersburg
Kierulff Eectronics Co., Inc., (301) 948-0250
Savage
Pytronic Industries, (301) 792-0780
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Dedham
Gerber Electronics, (617) 329-2400
Natick
Future Electronics, (617) 879-0860
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Diplomat/Northland, (313) 477-3200
MN **Minneapolis**
Diplomat/Electro-Com. Corp., (612) 788-8601
MO **Kansas City**
Walters Radio Supply, (816) 531-7015
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Wilshire Electronics, (201) 340-1900
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Kierulff Electronics Co., Inc., (201) 935-2120
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Zeus Components, Inc., (914) 592-4120
Endwell
Wilshire Electronics, (607) 754-1570
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Milgray Electronics, (516) 546-6000
Hauppauge, L.I.
JACO Electronics, (516) 275-5500
Hicksville, L.I.
Kierulff Electronics Co., Inc., (516) 221-1815
Rochester
Summit Electronics of Rochester, (716) 334-8110
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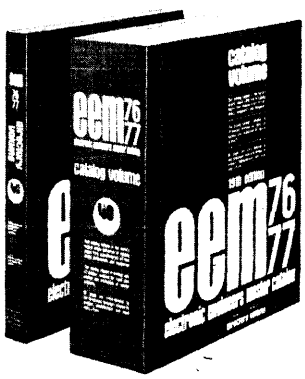
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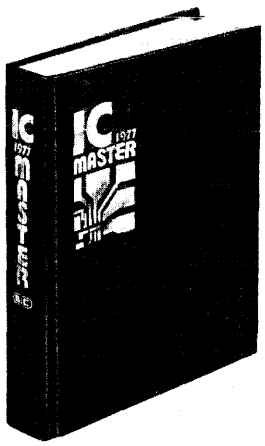
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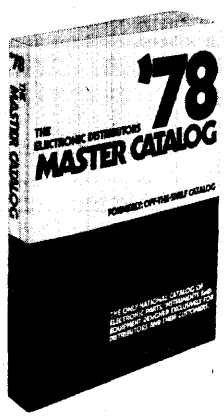
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PRODUCT INDEX

This index shows the page and the line on that page of every device in the Master Selection Guide and the Application Note Directory. It is organized alphabetically by manufacturer and for each manufacturer, alpha-numerically by device. Bold face listings lead to data on important products which have been supplied for you by the manufacturers. If you want to determine which products are in the book from a given manufacturer, simply check the Product Index.

how to use the product index

The Product Index contains the same references as the Part Number Index, but in this case the listings are sorted by manufacturer.

As in the Part Number Index, the model numbers are sorted alpha-numerically from **left** to **right.** Here the manufacturer's prefixes are included so that devices with alphabetic prefixes appear before those without them (i.e., LM101 would be before 1101). Application note pages are indicated by a ¶ sign and data by a ★ sign. The numbers preceding the dash are the page numbers, while those following the dash indicate the location on the device on the page.

When you use the Master to find data on a particular manufacturer's products, this index provides the fastest way to find all the information.

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54161	227 - 184
54162	229 - 178
54163	227 - 134
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	1027 - 63
54165	252 - 190
	1027 - 33
54166	253 - 11
	1027 - 45
54167	254 - 127
5417	233 - 97
54170	247 - 30

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54177	227 - 69
54178	252 - 79
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54179	252 - 91
	1025 - 83
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54182	224 - 96
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54192	230 - 107
54193	228 - 117
54194	251 - 189
	1025 - 85
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54198	252 - 148
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54199	252 - 133
	1027 - 11
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5423	245 - 61
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5427	245 - 85
54279	246 - 166
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55122	¶ 109 - 7
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74H183	223 - 117
74H20	240 - 46
74H21	238 - 99
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74H30	239 - 155
74H40	240 - 119
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74H51	243 - 138
74H52	242 - 194
74H53	243 - 83
74H54	243 - 50
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74H60	254 - 69
74H61	254 - 80
74H62	254 - 88
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74H74	236 - 183
74H76	236 - 117
74H78	235 - 52
74H87	254 - 61
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7414	255 - 177
74141	327 - 10
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74151	249 - 175
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74153	248 - 197
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75123	331 - 32
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75124	¶ 109 - 7
75124C	335 - 17
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75326C	344 - 19
75327C	344 - 25
7534C	347 - 124
7535C	347 - 125
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7539C	347 - 152
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75470B	344 - 82
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DAC-76B	★ **935**
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DAC-76C	★ **935**
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DAC-76D	321 - 49
DAC-76E	★ **935**
	321 - 50
DAC-86	★ **935**
	324 - 40
	598 - 39
DAC-87	★ **935**
	598 - 40
DAC-87C	★ **935**
	321 - 51
	322 - 76
DAC-87E	★ **935**
	321 - 52
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DDD562	★ **957**
LM148	★ **864**
MAT-01	★ **887**
	547 - 26
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MAT-01A	★ **887**
	547 - 27
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MAT-01F	★ **887**
	547 - 28
	547 - 43
MAT-01G	★ **887**
	547 - 29
	547 - 44
MAT-01H	★ **887**
MUX-08	★ **958**
MUX-08A	★ **958**
	315 - 19
MUX-08AQ	★ **958**
MUX-08B	★ **958**
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MUX-16	★ **959**
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MUX-16A	★ **959**
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MUX-16AQ	★ **959**
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MUX-16F	★ **959**
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MUX-24	★ **960**
MUX-24A	★ **960**
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MUX-24AQ	★ **960**
MUX-24B	★ **960**
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MUX-24BQ	★ **960**
MUX-24E	★ **960**
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MUX-24EQ	★ **960**
MUX-24F	★ **960**
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MUX-24FQ	★ **960**
MUX-28	★ **961**
MUX-28A	★ **961**
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MUX-28AQ	★ **961**
MUX-28B	★ **961**
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MUX-28BQ	★ **961**
MUX-28E	★ **961**
	315 - 81
MUX-28EQ	★ **961**
MUX-28F	★ **961**
	315 - 84
MUX-28FQ	★ **961**
MUX-88	★ **962**
MUX-88A	★ **962**
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MUX-88AQ	★ **962**
MUX-88B	★ **962**
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MUX-88BQ	★ **962**
MUX-88E	★ **962**
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MUX-88EQ	★ **962**
MUX-88F	★ **962**
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MUX-88FQ	★ **962**
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OP-01	★ **837**
	571 - 19
OP-01C	★ **837**
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OP-01E	★ **837**
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OP-01F	★ **837**
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OP-01G	★ **837**
	580 - 11
OP-01H	★ **837**
	571 - 20
OP-02	★ **839**
	564 - 31
	574 - 36
OP-02A	★ **839**
	571 - 11
OP-02C	★ **839**
	574 - 37
OP-02E	★ **839**
	571 - 12
OP-04	★ **844**
	588 - 51
OP-04A	★ **844**
	588 - 34
OP-04C	★ **844**
	588 - 52
OP-04E	★ **844**
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OP-05	★ **849**
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OP-05A	★ **849**
	566 - 51
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OP-05C	566 - 87
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OP-05E	566 - 56
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OP-07	★ **853**
	566 - 82
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OP-07A	★ **853**
	566 - 57
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OP-07C	★ **853**
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OP-07D	★ **853**
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OP-07E	★ **853**
	566 - 83
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OP-08	★ **858**
	566 - 148
OP-08A	★ **858**
	569 - 40
OP-08B	★ **858**
	570 - 7
OP-08C	★ **858**
	572 - 7
OP-08E	★ **858**
	569 - 41
OP-08F	★ **858**
	570 - 8
OP-08G	★ **858**
	572 - 8
OP-09	★ **864**
OP-09A	★ **864**
	592 - 25
OP-09B	★ **864**
	592 - 34
OP-09E	★ **864**
	592 - 26
OP-09F	★ **864**
	592 - 35
OP-10	★ **857**
	566 - 78
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OP-10C	566 - 90
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OP-11	★ **864**
OP-11A	★ **864**
	592 - 27
OP-11B	★ **864**
	592 - 36
OP-11E	★ **864**
	592 - 28
OP-11F	★ **864**
	592 - 37
OP-12	★ **858**
	566 - 149
OP-12A	★ **858**
	569 - 38
OP-12B	★ **858**
	570 - 5
OP-12C	★ **858**
	572 - 5
OP-12E	★ **858**
	569 - 39
OP-12F	★ **858**
OP-12F	570 - 6
OP-12G	★ **858**
	572 - 6
OP-14	★ **844**
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OP-14A	★ **844**
	588 - 36
OP-14C	★ **844**
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OP-14E	★ **844**
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OP-15	★ **871**
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OP-15A	★ **871**
	570 - 21
OP-15B	★ **871**
	571 - 47
OP-15C	★ **871**
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OP-15E	★ **871**
	570 - 22
OP-15F	★ **871**
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OP-15G	★ **871**
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OP-16	★ **877**
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OP-16A	★ **877**
	570 - 23
OP-16B	★ **877**
	571 - 49
OP-16C	★ **877**
	576 - 29
OP-16E	★ **877**
	570 - 24
OP-16F	★ **877**
	571 - 50
OP-16G	★ **877**
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OP-17	★ **882**
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OP-17A	★ **882**
	570 - 27
OP-17B	★ **882**
	571 - 53
OP-17C	★ **882**
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OP-17E	★ **882**
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OP-17F	★ **882**
	572 - 4
OP-17G	★ **882**
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PM108	★ **858**
	566 - 150
	574 - 12
PM108A	★ **858**
	570 - 43
PM1458	★ **844**
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	591 - 4
PM155	★ **871**
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	578 - 29
PM155A	★ **871**
	573 - 4
PM1558	★ **844**
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PM156	★ **877**
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PM156A	★ **877**
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PM157	★ **882**
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PM157A	★ **882**
	573 - 42
PM208	574 - 13
PM208A	570 - 44
PM255	★ **871**
	578 - 30
PM255A	★ **871**
PM256	★ **877**
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PM256A	★ **877**
PM257	★ **882**
	579 - 10
PM257A	★ **882**
PM308	583 - 48
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PM355	★ **871**
	585 - 23
PM355A	★ **871**
	573 - 5
PM356	★ **877**
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PM356A	★ **877**
	573 - 25
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PM741C	★ **839**
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PM747	★ **844**
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PM747C	★ **844**
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REF-01	★ **890**
	★ **894**
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	★ **894**
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REF-01C	★ **890**
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REF-01D	★ **890**
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REF-01E	★ **890**
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REF-01H	★ **890**
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REF-02	★ **894**
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	614 - 119
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REF-02D	★ **894**
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REF-02E	★ **894**
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REF-02H	★ **894**
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SMP-81	★ **899**
SMP-81E	★ **899**
SMP-81F	★ **899**
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SSS1408A	★ **919**
SSS1408A-6	★ **919**
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SSS1408A-7	★ **919**
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SSS1408A-8	★ **919**
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SSS1458	★ **844**
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SSS1508A	★ **919**
SSS1508A-6	★ **919**
SSS1508A-7	★ **919**
SSS1508A-8	★ **919**
SSS1508A-8	320 - 54
SSS1558	★ **844**
	589 - 45
SSS562	★ **955**
SSS562A	★ **955**
SSS562A/BCD	★ **930**
	★ **955**
	322 - 88
SSS562A/BIN	★ **930**
	★ **955**
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SSS562ABIN	★ **955**
SSS562BCD	★ **930**
SSS562BIN	★ **930**
SSS562K/BCD	★ **930**
	★ **955**
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SSS562K/BIN	★ **930**
	★ **955**
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SSS562S/BCD	★ **930**
	★ **955**
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SSS562S/BIN	★ **930**
	★ **955**
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SSS562SBIN	★ **955**
SSS725	★ **849**
	566 - 74
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SSS741B	★ **839**
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SSS741C	★ **839**
	582 - 33
SSS741G	★ **839**
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SSS747	★ **844**
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SSS747G	★ **844**
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LF155A	573 - 8
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LF156A	573 - 26
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LF157A	573 - 44
LF255	578 - 32
LF256	578 - 53
LF257	579 - 12
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LF356	585 - 33
LF356A	573 - 27
LF357	585 - 42
LF357A	573 - 45
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LM108	566 - 151
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LM109H	601 - 28
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LM111	549 - 43
LM118	565 - 80
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LM124	567 - 138
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LM129	614 - 135
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LM149	593 - 21
LM199	614 - 137
LM199A	614 - 140
LM201	584 - 35
LM201A	575 - 26
LM204	610 - 72
LM205	610 - 7
LM206	549 - 15
LM207	574 - 59
LM208	574 - 15
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LM218	577 - 51
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25LS22M	★ **297**
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25LS23	★ **300**
25LS23C	★ **300**
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25LS23M	★ **300**
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25LS240C	256 - 124
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25LS240M	256 - 125
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25LS241C	256 - 156
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25LS241M	256 - 157
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25LS251C	250 - 64
25LS251M	250 - 65
25LS253C	249 - 74
25LS253M	249 - 75
25LS257C	248 - 129
25LS257M	248 - 130
25LS258C	248 - 96
25LS258M	248 - 97
25LS299C	★ **302**
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25LS299M	★ **302**
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25LS373C	246 - 48
25LS373M	246 - 49
25LS670C	247 - 86
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25LS670M	247 - 87
	1010 - 51
26S10C	256 - 95
26S10M	256 - 96
26S11C	256 - 97
26S11M	256 - 98
29600	★**1494**
29600C	★**1494**
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29600M	★**1494**
	1004 - 25
29601	★**1494**
29601C	★**1494**
	1004 - 18
29601M	★**1494**
	1004 - 27
29610	★**1494**
29610C	★**1494**
	1004 - 77
29610M	★**1494**
	1004 - 102
29611	★**1494**
29611C	★**1494**
	1004 - 79
29611M	★**1494**
	1004 - 105
29612	★**1494**
29612C	★**1494**
	1004 - 83
29612M	★**1494**
	1004 - 107
29613	★**1494**
29613C	★**1494**
	1004 - 87
29613M	★**1494**
	1004 - 109
29620	★**1494**
29620C	★**1494**
	1005 - 7
29620M	★**1494**
	1005 - 34
29621	★**1494**
29621C	★**1494**
	1005 - 10
29621M	★**1494**
	1005 - 44
29622	★**1494**
29622C	★**1494**
	1005 - 27
29622M	★**1494**
	1005 - 60
29623	★**1494**
29623C	★**1494**
	1005 - 30
29623M	★**1494**
	1005 - 67
29624	★**1494**
29624C	★**1494**
	1005 - 9
29624M	★**1494**
	1005 - 42
29625	★**1494**
29625C	★**1494**
	1005 - 12
29625M	★**1494**
	1005 - 53
29626	★**1494**
29626C	★**1494**
	1005 - 29
29626M	★**1494**
	1005 - 65
29627	★**1494**
29627C	★**1494**
	1005 - 32
29627M	★**1494**
	1005 - 72
29640	★**1494**
29640C	★**1494**
	1006 - 53
29640M	★**1494**
	1006 - 82
29641	★**1494**
29641C	★**1494**
	1006 - 62
29641M	★**1494**
	1006 - 83
29642	★**1494**
29642C	★**1494**
	1006 - 77
29642M	★**1494**
	1006 - 88
29643	★**1494**
29643C	★**1494**
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29643M	★**1494**
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29645	★**1494**
29645C	★**1494**
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29645M	★**1494**
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29647	★**1494**
29647C	★**1494**
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29647M	★**1494**
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29660	★**1494**
29660C	★**1494**
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29660M	★**1494**
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29661	★**1494**
29661C	★**1494**
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29661M	★**1494**
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29662	★**1494**
29662C	★**1494**
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29663	★**1494**
29663C	★**1494**

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54LS04	226 - 29
54LS05	226 - 105
54LS08	239 - 42
54LS09	239 - 95
54LS10	241 - 40
54LS107	236 - 54
54LS109	235 - 84
54LS11	238 - 137
54LS112	235 - 165
54LS113	235 - 104
54LS114	235 - 138
54LS12	241 - 94
54LS122	★ **275**
	250 - 179
54LS123	★ **275**
	251 - 72
54LS125	225 - 82
54LS126	225 - 114
54LS13	★ **264**
	255 - 135
54LS132	★ **264**
	255 - 165
54LS136	244 - 160
54LS138	232 - 201
54LS139	232 - 157
54LS14	★ **264**
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54LS15	238 - 182
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54LS152	249 - 142
54LS153	249 - 37
54LS155	232 - 89
54LS156	232 - 125
54LS157	247 - 178
54LS158	248 - 61
54LS160	229 - 163
54LS161	228 - 35
54LS162	230 - 6
54LS163	227 - 170
54LS164	★ **272**
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54LS170	247 - 59
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54LS174	237 - 199
54LS175	237 - 78
54LS181	224 - 54
54LS190	230 - 93
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54LS194A	252 - 20
54LS195	1026 - 20
54LS195A	251 - 132
54LS196	229 - 102
54LS197	227 - 116
54LS20	240 - 39
54LS21	238 - 92
54LS22	240 - 166
54LS221	★ **275**
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54LS240	★ **279**
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54LS241	★ **279**
	256 - 158
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54LS242	★ **282**
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54LS243	★ **282**
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	340 - 10
54LS244	★ **279**
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54LS251	250 - 66
54LS253	249 - 76
54LS255	232 - 136
54LS257	248 - 131
54LS258	248 - 98
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54LS266	244 - 190
54LS27	245 - 111
54LS279	246 - 184
54LS28	245 - 163
54LS283	223 - 79
54LS295A	252 - 43
54LS298	237 - 141
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54LS299	252 - 180
54LS30	239 - 148
54LS32	245 - 29
54LS33	245 - 190
54LS365	★ **286**
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54LS366	★ **286**
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54LS367	★ **286**
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54LS368	★ **286**
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54LS37	242 - 12
54LS373	★ **288**
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54LS374	★ **288**
54LS377	★ **288**
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54LS38	242 - 159
54LS386	244 - 113
54LS395	★ **291**
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54LS42	★ **266**
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54LS43	★ **266**
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54LS44	★ **266**
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54LS76	236 - 110
54LS77	246 - 118
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54LS86	244 - 109
54LS90	★ **268**
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54LS91	★ **272**
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54LS92	★ **268**
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54LS93	★ **268**
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54R05	226 - 121
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54R113	235 - 121
54R114	235 - 29
54R15	238 - 192
54R181	224 - 62
54R182	224 - 115
54R20	240 - 56
54R22	240 - 180
54R40	240 - 131
54R64	243 - 95
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54S241	256 - 169
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54S244	256 - 192
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5401	242 - 48
5403	242 - 50
5404	226 - 9
5405	226 - 83
5408	239 - 22
5409	239 - 76
5410	241 - 20
5411	238 - 120
5412	241 - 81
54123	251 - 54
54136	244 - 144
54145	232 - 5
5415	238 - 169
54150	250 - 105
54151	249 - 189
54152	249 - 128
54153	249 - 12
54154	233 - 70
54155	232 - 67
54156	232 - 107
54157	247 - 151
54158	248 - 40
54159	233 - 85
54160	229 - 132
54161	228 - 7
54162	229 - 188
54163	227 - 146
54164	253 - 43
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54165	252 - 199
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54166	253 - 19
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54170	247 - 38
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54174	237 - 177
54175	237 - 52
54180	255 - 19
54181	224 - 33
54182	224 - 109
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54191	228 - 80
54192	230 - 122
54193	228 - 134
54194	251 - 200
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54195	251 - 107
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54199	252 - 141
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5420	240 - 19
5421	238 - 75
5422	240 - 151
54255	232 - 132
54283	223 - 46
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5443	231 - 84
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74LS01	242 - 83
74LS02	245 - 160
74LS03	242 - 87
74LS04	226 - 30
74LS05	226 - 106
74LS08	239 - 43
74LS09	239 - 96
74LS10	241 - 41
74LS107	236 - 55
74LS109	235 - 85
74LS11	238 - 138
74LS112	235 - 166
74LS113	235 - 105
74LS114	235 - 139
74LS12	241 - 95
74LS122	★ **275**
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74LS123	★ **275**
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74LS125	225 - 83
74LS126	225 - 115
74LS13	★ **264**
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74LS132	★ **264**
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74LS136	244 - 161
74LS138	232 - 202
74LS139	232 - 158
74LS14	★ **264**
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74LS15	238 - 183
74LS151	250 - 13
74LS152	249 - 143
74LS153	249 - 38
74LS155	232 - 90
74LS156	232 - 126
74LS157	247 - 179
74LS158	248 - 62
74LS160	229 - 164
74LS161	228 - 36
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74LS163	227 - 171
74LS164	★ **272**
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74LS170	247 - 60
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74LS174	237 - 200
74LS175	237 - 79
74LS181	224 - 55
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74LS191	228 - 104
74LS192	230 - 152
74LS193	228 - 163
74LS194A	252 - 21
74LS195	1026 - 21
74LS195A	251 - 133
74LS196	229 - 103
74LS197	227 - 117
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74LS221	★ **275**
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74LS240	★ **279**
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74LS241	★ **279**
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74LS242	★ **282**
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74LS243	★ **282**
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74LS244	★ **279**
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74LS251	250 - 67
74LS253	249 - 77
74LS255	232 - 137
74LS257	248 - 132
74LS258	248 - 99
74LS26	242 - 181
74LS261	★ **284**
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74LS266	244 - 191
74LS27	245 - 112
74LS279	246 - 185
74LS28	245 - 164
74LS283	223 - 80
74LS295A	252 - 44
74LS298	237 - 142
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74LS299	252 - 181
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74LS32	245 - 30
74LS33	245 - 191
74LS365	★ **286**
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74LS366	★ **286**
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74LS367	★ **286**
	225 - 163
74LS368	★ **286**
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74LS37	242 - 13
74LS373	★ **288**
	246 - 51
74LS374	★ **288**
	238 - 31
74LS377	★ **288**
	238 - 59
74LS38	242 - 160
74LS386	244 - 114
74LS395	★ **291**
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74LS40	240 - 113
74LS42	★ **266**
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74LS43	★ **266**
	231 - 93
74LS44	★ **266**
	231 - 113
74LS51	243 - 171
74LS54	243 - 43
74LS55	243 - 189
74LS670	247 - 89
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74LS73	236 - 51
74LS74	236 - 177
74LS75	246 - 156
74LS76	236 - 111
74LS77	246 - 119
74LS78	235 - 46
74LS83A	223 - 76
74LS85	225 - 22
74LS86	244 - 110
74LS90	★ **268**
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74LS91	★ **272**
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74LS92	★ **268**
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74LS93	★ **268**
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74R114	235 - 30
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74S241	256 - 170
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74S244	256 - 193
7400	241 - 124
7401	242 - 49
7403	242 - 51
7404	226 - 10
7405	226 - 84
7408	239 - 23
7409	239 - 77
7410	241 - 21
7411	238 - 121
7412	241 - 82
74123	251 - 55
74136	244 - 145
74145	232 - 6
7415	238 - 170
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74151	249 - 190
74152	249 - 129
74153	249 - 13
74154	233 - 71
74155	232 - 71
74156	232 - 108
74157	247 - 152
74158	248 - 41
74159	233 - 86
74160	229 - 133
74161	228 - 8
74162	229 - 189
74163	227 - 147
74164	253 - 44
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74165	252 - 200
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74166	253 - 20
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74170	247 - 39
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74174	237 - 178
74175	237 - 53
74180	255 - 20
74181	224 - 34
74182	224 - 110
74190	230 - 71
74191	228 - 81
74192	230 - 123
74193	228 - 135
74194	251 - 201
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74195	251 - 108
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74198	252 - 156
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7420	240 - 20
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9LS05C	226 - 103
9LS05M	226 - 104
9LS08C	239 - 40
9LS08M	239 - 41
9LS09C	239 - 93
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9LS112C	235 - 163
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9LS123	★ 275
9LS123C	★ 275 251 - 68
9LS123M	★ 275 251 - 69
9LS125C	225 - 80
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9LS13C	★ 264 255 - 133
9LS13M	★ 264 255 - 134
9LS132	★ 264
9LS132C	★ 264 255 - 163
9LS132M	★ 264 255 - 164
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9LS14C	★ 264 255 - 197
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9LS153C	249 - 33
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9LS181M	224 - 53
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9LS196C	229 - 100
9LS196M	229 - 101
9LS197C	227 - 114
9LS197M	227 - 115
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9LS21C	238 - 90
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9LS240M	★ 279 332 - 63
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9LS241M	★ 279 332 - 31
9LS242	★ 282
9LS242C	★ 282 340 - 54
9LS242M	★ 282 340 - 7
9LS243	★ 282
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9LS244	★ 279
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9LS366	★ 286
9LS366C	★ 286 226 - 174
9LS366M	★ 286 226 - 175
9LS367	★ 286
9LS367C	★ 286 225 - 160
9LS367M	★ 286 225 - 161
9LS368	★ 286
9LS368C	★ 286 226 - 178
9LS368M	★ 286 226 - 179
9LS37C	242 - 10
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9LS373C	★ 288
9LS373M	★ 288
9LS374	★ 288
9LS374C	★ 288
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9LS377	★ 288
9LS377C	★ 288
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9LS42C	★ 266 231 - 171
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9LS43	★ 266
9LS43C	★ 266 231 - 90
9LS43M	★ 266 231 - 91
9LS44	★ 266
9LS44C	★ 266 231 - 110
9LS44M	★ 266 231 - 111
9LS51C	243 - 168
9LS51M	243 - 169
9LS54C	243 - 40
9LS54M	243 - 41
9LS55C	243 - 186
9LS55M	243 - 187
9LS670C	247 - 84
9LS670M	247 - 85
9LS73C	236 - 48
9LS73M	236 - 49
9LS74C	236 - 174
9LS74M	236 - 175
9LS75C	246 - 153
9LS75M	246 - 154
9LS76C	236 - 108
9LS76M	236 - 109
9LS77C	246 - 116
9LS77M	246 - 117
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